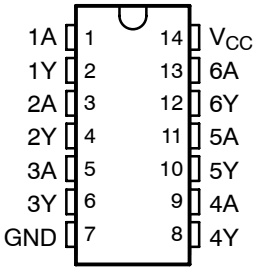
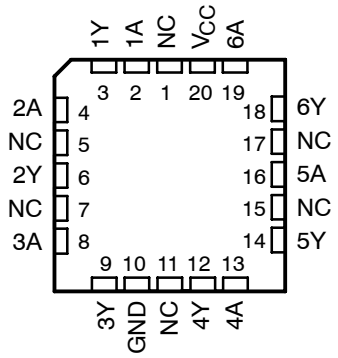
SCLS085F – DECEMBER 1982 – REVISED DECEMBER 2010

- **Wide Operating Voltage Range of 2 V to 6 V**
- **Outputs Can Drive Up To 10 LSTTL Loads**
- **Low Power Consumption, 20-μA Max $I_{CC}$**
- **Typical $t_{pd}$ = 11 ns**
- **±4-mA Output Drive at 5 V**
- **Low Input Current of 1 μA Max**

**SN54HC14 . . . J OR W PACKAGE**
**SN74HC14 . . . D, DB, N, NS, OR PW PACKAGE**
**(TOP VIEW)**




**SN54HC14 . . . FK PACKAGE**
**(TOP VIEW)**




NC – No internal connection

## description/ordering information

These Schmitt-trigger devices contain six independent inverters. They perform the Boolean function $Y = \overline{A}$ in positive logic.

Datasheet.Company

**ORDERING INFORMATION**

| $T_A$ | PACKAGE† | | ORDERABLE PART NUMBER | TOP-SIDE MARKING |
|---|---|---|---|---|
| −40°C to 85°C | PDIP – N | Tube of 25 | SN74HC14N | SN74HC14N |
| | SOIC – D | Tube of 50 | SN74HC14D | HC14 |
| | | Reel of 2500 | SN74HC14DRG3 | |
| | | Reel of 250 | SN74HC14DT | |
| | SOP – NS | Reel of 2000 | SN74HC14NSR | HC14 |
| | SSOP – DB | Reel of 2000 | SN74HC14DBR | HC14 |
| | TSSOP – PW | Tube of 90 | SN74HC14PW | HC14 |
| | | Reel of 2000 | SN74HC14PWR | |
| | | Reel of 250 | SN74HC14PWT | |
| −55°C to 125°C | CDIP – J | Tube | SNJ54HC14J | SNJ54HC14J |
| | CFP – W | Tube | SNJ54HC14W | SNJ54HC14W |
| | LCCC – FK | Tube | SNJ54HC14FK | SNJ54HC14FK |

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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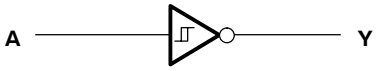
On products compliant to MIL-PRF-38535, all parameters are tested unless otherwise noted. On all other products, production processing does not necessarily include testing of all parameters.

**FUNCTION TABLE**
**(each inverter)**

| INPUT A | OUTPUT Y |
|---|---|
| H | L |
| L | H |

## logic diagram (positive logic)




## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, $V_{CC}$ . . . . . –0.5 V to 7 V
Input clamp current, $I_{IK}$ ($V_I < 0$ or $V_I > V_{CC}$) (see Note 1) . . . . . ±20 mA
Output clamp current, $I_{OK}$ ($V_O < 0$ or $V_O > V_{CC}$) (see Note 1) . . . . . ±20 mA
Continuous output current, $I_O$ ($V_O = 0$ to $V_{CC}$) . . . . . ±25 mA
Continuous current through $V_{CC}$ or GND . . . . . ±50 mA
Package thermal impedance, $\theta_{JA}$ (see Note 2): D package . . . . . 86°C/W
DB package . . . . . 96°C/W
N package . . . . . 80°C/W
NS package . . . . . 76°C/W
PW package . . . . . 113°C/W
Storage temperature range, $T_{stg}$ . . . . . –65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The package thermal impedance is calculated in accordance with JESD 51-7.

## recommended operating conditions (see Note 3)

| | | SN54HC14 | | | SN74HC14 | | | UNIT |
|---|---|---|---|---|---|---|---|---|
| | | MIN | NOM | MAX | MIN | NOM | MAX | |
| $V_{CC}$ | Supply voltage | 2 | 5 | 6 | 2 | 5 | 6 | V |
| $V_I$ | Input voltage | 0 | | $V_{CC}$ | 0 | | $V_{CC}$ | V |
| $V_O$ | Output voltage | 0 | | $V_{CC}$ | 0 | | $V_{CC}$ | V |
| $T_A$ | Operating free-air temperature | –55 | | 125 | –40 | | 85 | °C |

NOTE 3: All unused inputs of the device must be held at $V_{CC}$ or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | | $V_{CC}$ | $T_A$ = 25°C | | | SN54HC14 | | SN74HC14 | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
| $V_{T+}$ | | | 2 V | 0.7 | 1.2 | 1.5 | 0.7 | 1.5 | 0.7 | 1.5 | V |
| | | | 4.5 V | 1.55 | 2.5 | 3.15 | 1.55 | 3.15 | 1.55 | 3.15 | |
| | | | 6 V | 2.1 | 3.3 | 4.2 | 2.1 | 4.2 | 2.1 | 4.2 | |
| $V_{T-}$ | | | 2 V | 0.3 | 0.6 | 1 | 0.3 | 1 | 0.3 | 1 | V |
| | | | 4.5 V | 0.9 | 1.6 | 2.45 | 0.9 | 2.45 | 0.9 | 2.45 | |
| | | | 6 V | 1.2 | 2 | 3.2 | 1.2 | 3.2 | 1.2 | 3.2 | |
| $V_{T+} - V_{T-}$ | | | 2 V | 0.2 | 0.6 | 1.2 | 0.2 | 1.2 | 0.2 | 1.2 | V |
| | | | 4.5 V | 0.4 | 0.9 | 2.1 | 0.4 | 2.1 | 0.4 | 2.1 | |
| | | | 6 V | 0.5 | 1.3 | 2.5 | 0.5 | 2.5 | 0.5 | 2.5 | |
| $V_{OH}$ | $V_I = V_{IH}$ or $V_{IL}$ | $I_{OH}$ = –20 μA | 2 V | 1.9 | 1.998 | | 1.9 | | 1.9 | | V |
| | | | 4.5 V | 4.4 | 4.499 | | 4.4 | | 4.4 | | |
| | | | 6 V | 5.9 | 5.999 | | 5.9 | | 5.9 | | |
| | | $I_{OH}$ = –4 mA | 4.5 V | 3.98 | 4.3 | | 3.7 | | 3.84 | | |
| | | $I_{OH}$ = –5.2 mA | 6 V | 5.48 | 5.8 | | 5.2 | | 5.34 | | |
| $V_{OL}$ | $V_I = V_{IH}$ or $V_{IL}$ | $I_{OL}$ = 20 μA | 2 V | | 0.002 | 0.1 | | 0.1 | | 0.1 | V |
| | | | 4.5 V | | 0.001 | 0.1 | | 0.1 | | 0.1 | |
| | | | 6 V | | 0.001 | 0.1 | | 0.1 | | 0.1 | |
| | | $I_{OL}$ = 4 mA | 4.5 V | | 0.17 | 0.26 | | 0.4 | | 0.33 | |
| | | $I_{OL}$ = 5.2 mA | 6 V | | 0.15 | 0.26 | | 0.4 | | 0.33 | |
| $I_I$ | $V_I = V_{CC}$ or 0 | | 6 V | | | ±0.1 | ±100 | | ±1000 | | ±1000 | nA |
| $I_{CC}$ | $V_I = V_{CC}$ or 0, $I_O$ = 0 | | 6 V | | | 2 | | 40 | | 20 | μA |
| $C_i$ | | | 2 V to 6 V | | 3 | 10 | | 10 | | 10 | pF |

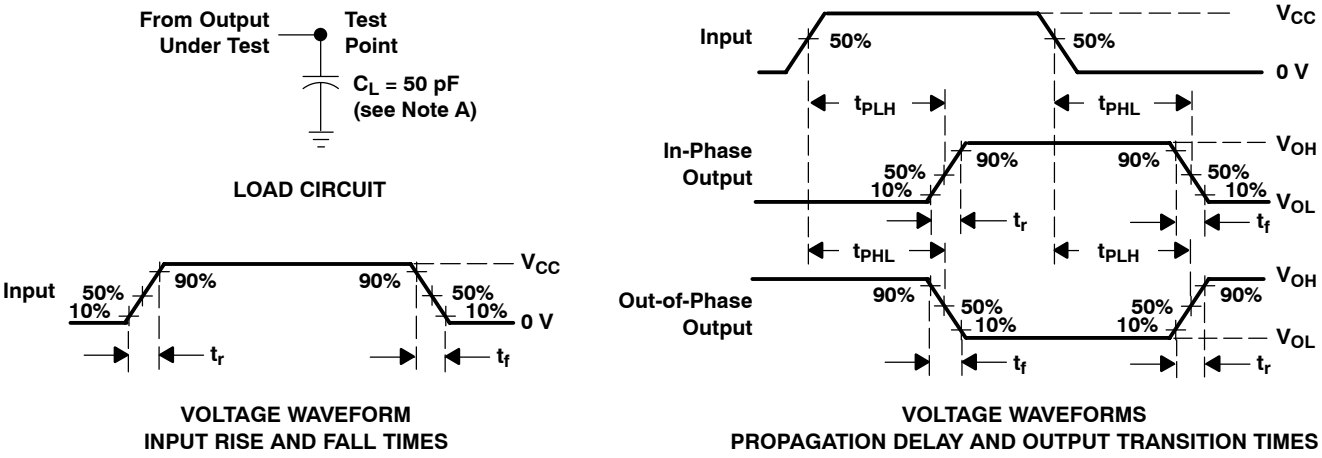
## switching characteristics over recommended operating free-air temperature range, $C_L$ = 50 pF (unless otherwise noted) (see Figure 1)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | $V_{CC}$ | $T_A$ = 25°C | | | SN54HC14 | | SN74HC14 | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
| $t_{pd}$ | A | Y | 2 V | | 55 | 125 | | 190 | | 155 | ns |
| | | | 4.5 V | | 12 | 25 | | 38 | | 31 | |
| | | | 6 V | | 11 | 21 | | 32 | | 26 | |
| $t_t$ | | Y | 2 V | | 38 | 75 | | 110 | | 95 | ns |
| | | | 4.5 V | | 8 | 15 | | 22 | | 19 | |
| | | | 6 V | | 6 | 13 | | 19 | | 16 | |

## operating characteristics, $T_A$ = 25°C

| PARAMETER | | TEST CONDITIONS | TYP | UNIT |
|---|---|---|---|---|
| $C_{pd}$ | Power dissipation capacitance per inverter | No load | 20 | pF |

## PARAMETER MEASUREMENT INFORMATION




NOTES: A. $C_L$ includes probe and test-fixture capacitance.
B. Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, $Z_O$ = 50 Ω, $t_r$ = 6 ns, $t_f$ = 6 ns.
C. The outputs are measured one at a time, with one input transition per measurement.
D. $t_{PLH}$ and $t_{PHL}$ are the same as $t_{pd}$.

**Figure 1. Load Circuit and Voltage Waveforms**

## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/ Ball Finish | MSL Peak Temp (3) | Samples (Requires Login) |
|---|---|---|---|---|---|---|---|---|---|
| 5962-8409101VCA | ACTIVE | CDIP | J | 14 | 1 | TBD | A42 | N / A for Pkg Type | |
| 5962-8409101VDA | ACTIVE | CFP | W | 14 | 1 | TBD | A42 | N / A for Pkg Type | |
| 84091012A | ACTIVE | LCCC | FK | 20 | 1 | TBD | Call TI | Call TI | |
| 8409101CA | ACTIVE | CDIP | J | 14 | 1 | TBD | Call TI | Call TI | |
| 8409101DA | ACTIVE | CFP | W | 14 | 1 | TBD | Call TI | Call TI | |
| JM38510/65702BCA | ACTIVE | CDIP | J | 14 | 1 | TBD | A42 | N / A for Pkg Type | |
| JM38510/65702BDA | ACTIVE | CFP | W | 14 | 1 | TBD | A42 | N / A for Pkg Type | |
| M38510/65702BCA | ACTIVE | CDIP | J | 14 | 1 | TBD | A42 | N / A for Pkg Type | |
| M38510/65702BDA | ACTIVE | CFP | W | 14 | 1 | TBD | A42 | N / A for Pkg Type | |
| SN54HC14J | ACTIVE | CDIP | J | 14 | 1 | TBD | A42 | N / A for Pkg Type | |
| SN74HC14D | ACTIVE | SOIC | D | 14 | 50 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | |
| SN74HC14DBR | ACTIVE | SSOP | DB | 14 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | |
| SN74HC14DBRE4 | ACTIVE | SSOP | DB | 14 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | |
| SN74HC14DBRG4 | ACTIVE | SSOP | DB | 14 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | |
| SN74HC14DE4 | ACTIVE | SOIC | D | 14 | 50 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | |
| SN74HC14DG4 | ACTIVE | SOIC | D | 14 | 50 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | |
| SN74HC14DR | ACTIVE | SOIC | D | 14 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | |
| SN74HC14DRE4 | ACTIVE | SOIC | D | 14 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | |
| SN74HC14DRG3 | ACTIVE | SOIC | D | 14 | 2500 | Green (RoHS & no Sb/Br) | CU SN | Level-1-260C-UNLIM | |
| SN74HC14DRG4 | ACTIVE | SOIC | D | 14 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | |
| SN74HC14DT | ACTIVE | SOIC | D | 14 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | |

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/ Ball Finish | MSL Peak Temp (3) | Samples (Requires Login) |
|---|---|---|---|---|---|---|---|---|---|
| SN74HC14DTE4 | ACTIVE | SOIC | D | 14 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | |
| SN74HC14DTG4 | ACTIVE | SOIC | D | 14 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | |
| SN74HC14N | ACTIVE | PDIP | N | 14 | 25 | Pb-Free (RoHS) | CU NIPDAU | N / A for Pkg Type | |
| SN74HC14N3 | OBSOLETE | PDIP | N | 14 | | TBD | Call TI | Call TI | |
| SN74HC14NE4 | ACTIVE | PDIP | N | 14 | 25 | Pb-Free (RoHS) | CU NIPDAU | N / A for Pkg Type | |
| SN74HC14NSLE | OBSOLETE | SO | NS | 14 | | TBD | Call TI | Call TI | |
| SN74HC14NSR | ACTIVE | SO | NS | 14 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | |
| SN74HC14NSRE4 | ACTIVE | SO | NS | 14 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | |
| SN74HC14NSRG4 | ACTIVE | SO | NS | 14 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | |
| SN74HC14PW | ACTIVE | TSSOP | PW | 14 | 90 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | |
| SN74HC14PWE4 | ACTIVE | TSSOP | PW | 14 | 90 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | |
| SN74HC14PWG4 | ACTIVE | TSSOP | PW | 14 | 90 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | |
| SN74HC14PWLE | OBSOLETE | TSSOP | PW | 14 | | TBD | Call TI | Call TI | |
| SN74HC14PWR | ACTIVE | TSSOP | PW | 14 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | |
| SN74HC14PWRE4 | ACTIVE | TSSOP | PW | 14 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | |
| SN74HC14PWRG4 | ACTIVE | TSSOP | PW | 14 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | |
| SN74HC14PWT | ACTIVE | TSSOP | PW | 14 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | |
| SN74HC14PWTE4 | ACTIVE | TSSOP | PW | 14 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | |
| SN74HC14PWTG4 | ACTIVE | TSSOP | PW | 14 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | |
| SNJ54HC14FK | ACTIVE | LCCC | FK | 20 | 1 | TBD | POST-PLATE | N / A for Pkg Type | |
| SNJ54HC14J | ACTIVE | CDIP | J | 14 | 1 | TBD | A42 | N / A for Pkg Type | |

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/ Ball Finish | MSL Peak Temp (3) | Samples (Requires Login) |
|---|---|---|---|---|---|---|---|---|---|
| SNJ54HC14W | ACTIVE | CFP | W | 14 | 1 | TBD | A42 | N / A for Pkg Type | |

(1) The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
**TBD:** The Pb-Free/Green conversion plan has not been defined.
**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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**OTHER QUALIFIED VERSIONS OF SN54HC14, SN54HC14-SP, SN74HC14 :**

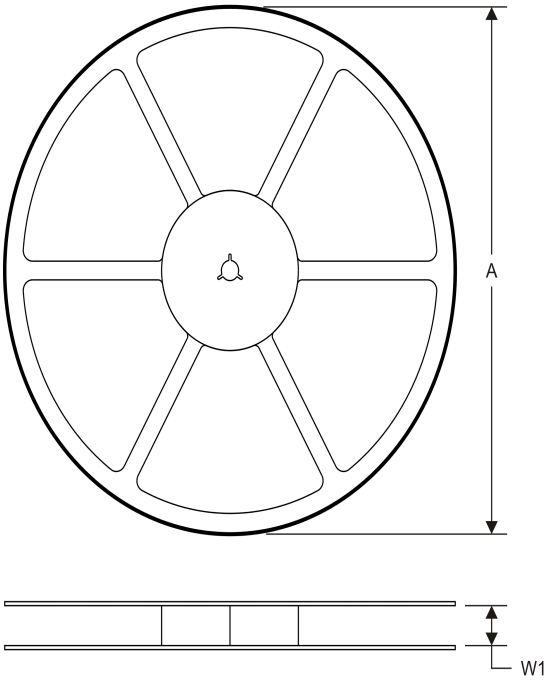
- Catalog: SN74HC14, SN54HC14
- Automotive: SN74HC14-Q1, SN74HC14-Q1
- Military: SN54HC14
- Space: SN54HC14-SP

NOTE: Qualified Version Definitions:

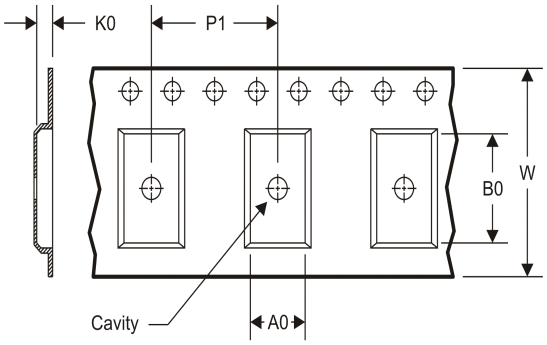
- Catalog - TI's standard catalog product
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects
- Military - QML certified for Military and Defense Applications
- Space - Radiation tolerant, ceramic packaging and qualified for use in Space-based application

## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**




**TAPE DIMENSIONS**



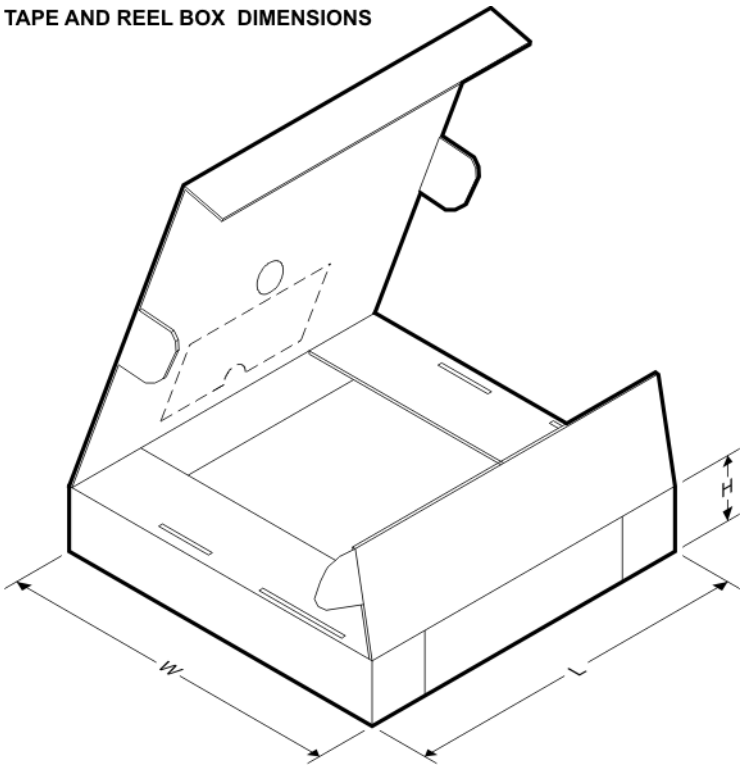

| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

**TAPE AND REEL INFORMATION**

*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| SN74HC14DBR | SSOP | DB | 14 | 2000 | 330.0 | 16.4 | 8.2 | 6.6 | 2.5 | 12.0 | 16.0 | Q1 |
| SN74HC14DR | SOIC | D | 14 | 2500 | 330.0 | 16.4 | 6.5 | 9.0 | 2.1 | 8.0 | 16.0 | Q1 |
| SN74HC14DR | SOIC | D | 14 | 2500 | 330.0 | 16.4 | 6.5 | 9.0 | 2.1 | 8.0 | 16.0 | Q1 |
| SN74HC14DRG4 | SOIC | D | 14 | 2500 | 330.0 | 16.4 | 6.5 | 9.0 | 2.1 | 8.0 | 16.0 | Q1 |
| SN74HC14DRG4 | SOIC | D | 14 | 2500 | 330.0 | 16.4 | 6.5 | 9.0 | 2.1 | 8.0 | 16.0 | Q1 |
| SN74HC14DT | SOIC | D | 14 | 250 | 330.0 | 16.4 | 6.5 | 9.0 | 2.1 | 8.0 | 16.0 | Q1 |
| SN74HC14NSR | SO | NS | 14 | 2000 | 330.0 | 16.4 | 8.2 | 10.5 | 2.5 | 12.0 | 16.0 | Q1 |
| SN74HC14PWR | TSSOP | PW | 14 | 2000 | 330.0 | 12.4 | 6.9 | 5.6 | 1.6 | 8.0 | 12.0 | Q1 |
| SN74HC14PWT | TSSOP | PW | 14 | 250 | 330.0 | 12.4 | 6.9 | 5.6 | 1.6 | 8.0 | 12.0 | Q1 |

**TAPE AND REEL BOX DIMENSIONS**



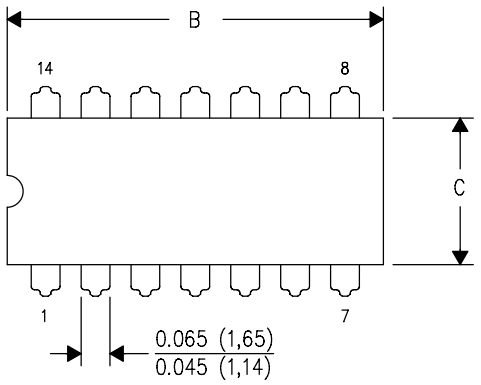

*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| SN74HC14DBR | SSOP | DB | 14 | 2000 | 367.0 | 367.0 | 38.0 |
| SN74HC14DR | SOIC | D | 14 | 2500 | 333.2 | 345.9 | 28.6 |
| SN74HC14DR | SOIC | D | 14 | 2500 | 367.0 | 367.0 | 38.0 |
| SN74HC14DRG4 | SOIC | D | 14 | 2500 | 333.2 | 345.9 | 28.6 |
| SN74HC14DRG4 | SOIC | D | 14 | 2500 | 367.0 | 367.0 | 38.0 |
| SN74HC14DT | SOIC | D | 14 | 250 | 367.0 | 367.0 | 38.0 |
| SN74HC14NSR | SO | NS | 14 | 2000 | 367.0 | 367.0 | 38.0 |
| SN74HC14PWR | TSSOP | PW | 14 | 2000 | 367.0 | 367.0 | 35.0 |
| SN74HC14PWT | TSSOP | PW | 14 | 250 | 367.0 | 367.0 | 35.0 |

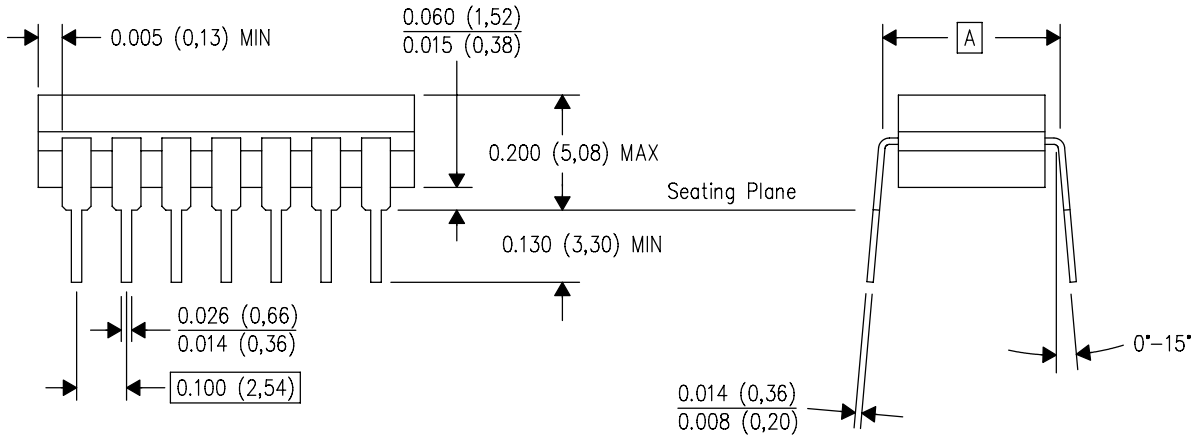
J (R–GDIP–T**)

14 LEADS SHOWN

# CERAMIC DUAL IN–LINE PACKAGE



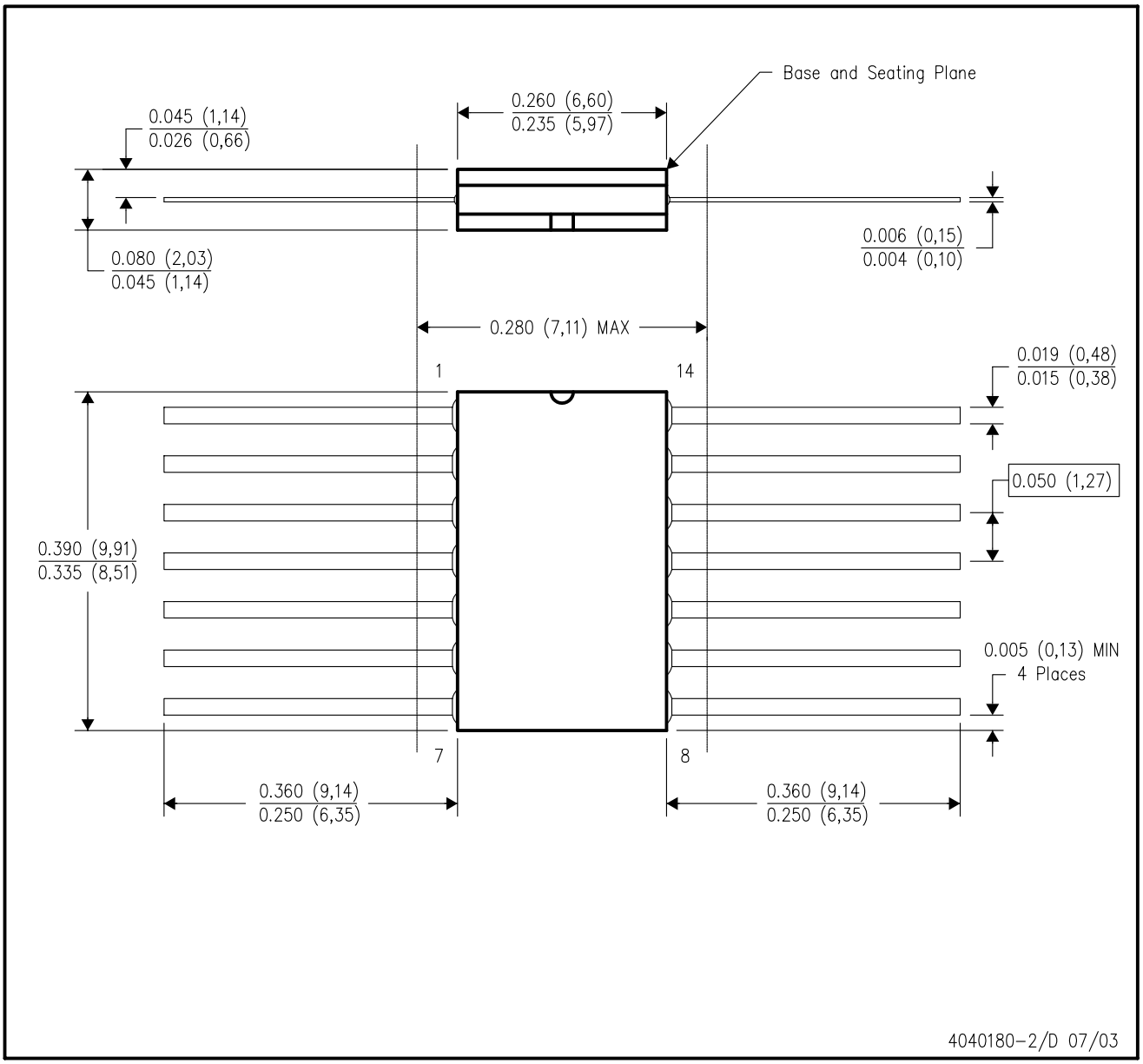

| DIM \ PINS ** | 14 | 16 | 18 | 20 |
|---|---|---|---|---|
| A | 0.300 (7,62) BSC | 0.300 (7,62) BSC | 0.300 (7,62) BSC | 0.300 (7,62) BSC |
| B MAX | 0.785 (19,94) | .840 (21,34) | 0.960 (24,38) | 1.060 (26,92) |
| B MIN | — | — | — | — |
| C MAX | 0.300 (7,62) | 0.300 (7,62) | 0.310 (7,87) | 0.300 (7,62) |
| C MIN | 0.245 (6,22) | 0.245 (6,22) | 0.220 (5,59) | 0.245 (6,22) |




4040083/F 03/03

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package is hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
E. Falls within MIL STD 1835 GDIP1–T14, GDIP1–T16, GDIP1–T18 and GDIP1–T20.

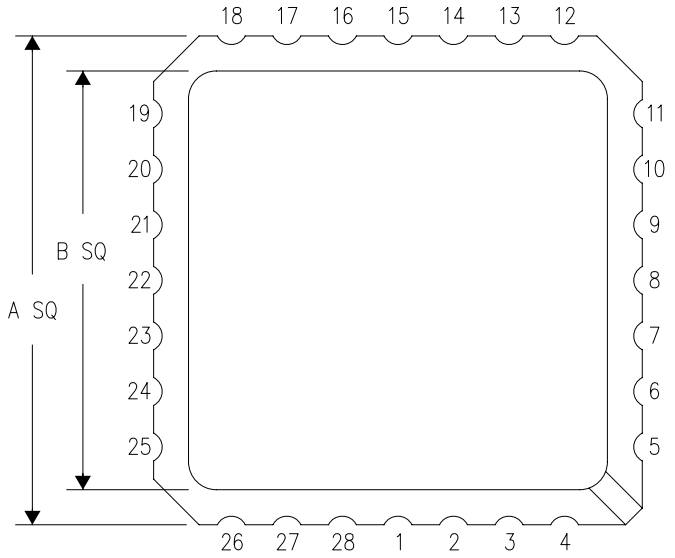
## W (R–GDFP–F14) CERAMIC DUAL FLATPACK



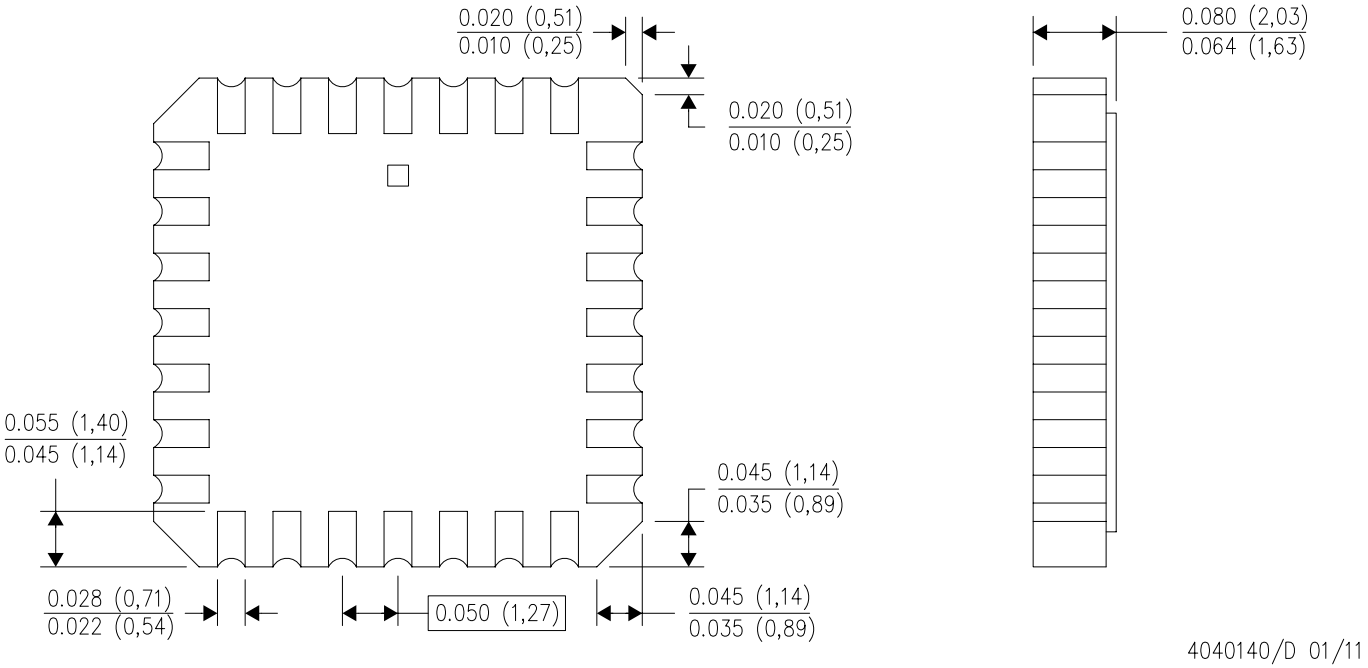

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only.
E. Falls within MIL STD 1835 GDFP1–F14 and JEDEC MO–092AB

FK (S–CQCC–N**) LEADLESS CERAMIC CHIP CARRIER

28 TERMINAL SHOWN




| NO. OF TERMINALS ** | A | | B | |
|---|---|---|---|---|
| | MIN | MAX | MIN | MAX |
| 20 | 0.342 (8,69) | 0.358 (9,09) | 0.307 (7,80) | 0.358 (9,09) |
| 28 | 0.442 (11,23) | 0.458 (11,63) | 0.406 (10,31) | 0.458 (11,63) |
| 44 | 0.640 (16,26) | 0.660 (16,76) | 0.495 (12,58) | 0.560 (14,22) |
| 52 | 0.740 (18,78) | 0.761 (19,32) | 0.495 (12,58) | 0.560 (14,22) |
| 68 | 0.938 (23,83) | 0.962 (24,43) | 0.850 (21,6) | 0.858 (21,8) |
| 84 | 1.141 (28,99) | 1.165 (29,59) | 1.047 (26,6) | 1.063 (27,0) |



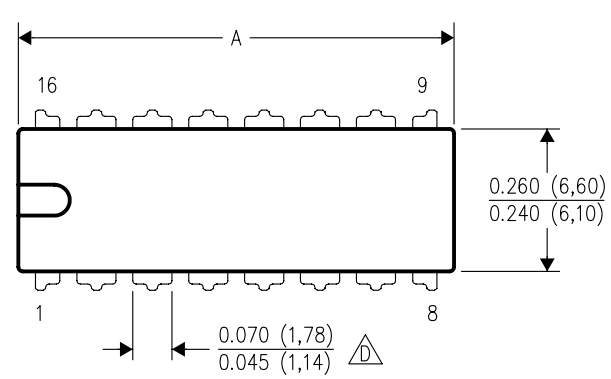

4040140/D 01/11

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a metal lid.
D. Falls within JEDEC MS–004

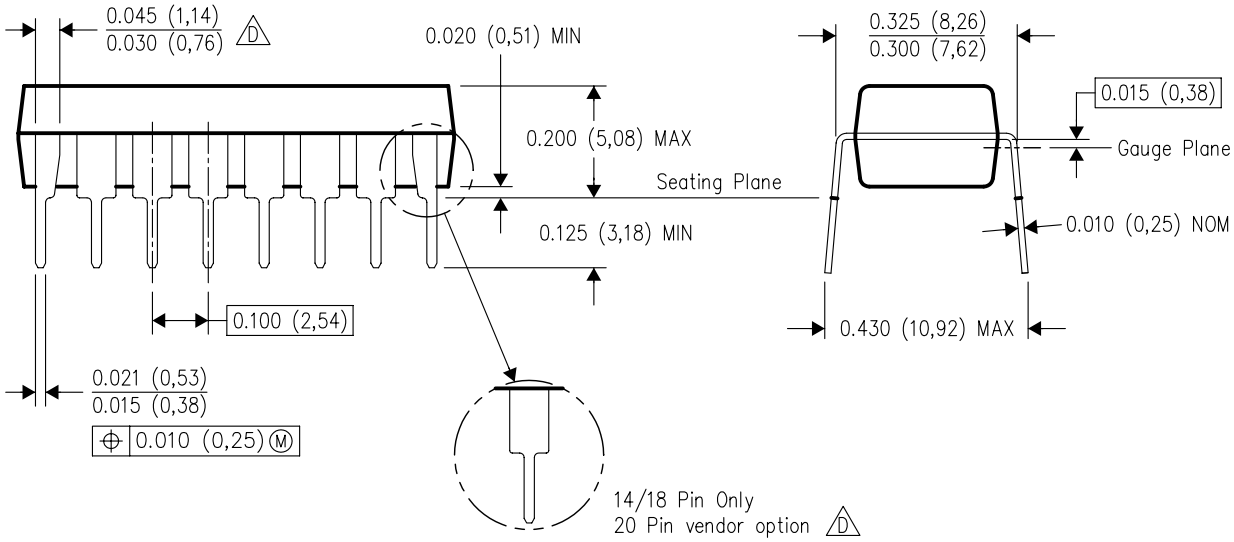
## N (R–PDIP–T**)

## PLASTIC DUAL–IN–LINE PACKAGE

16 PINS SHOWN



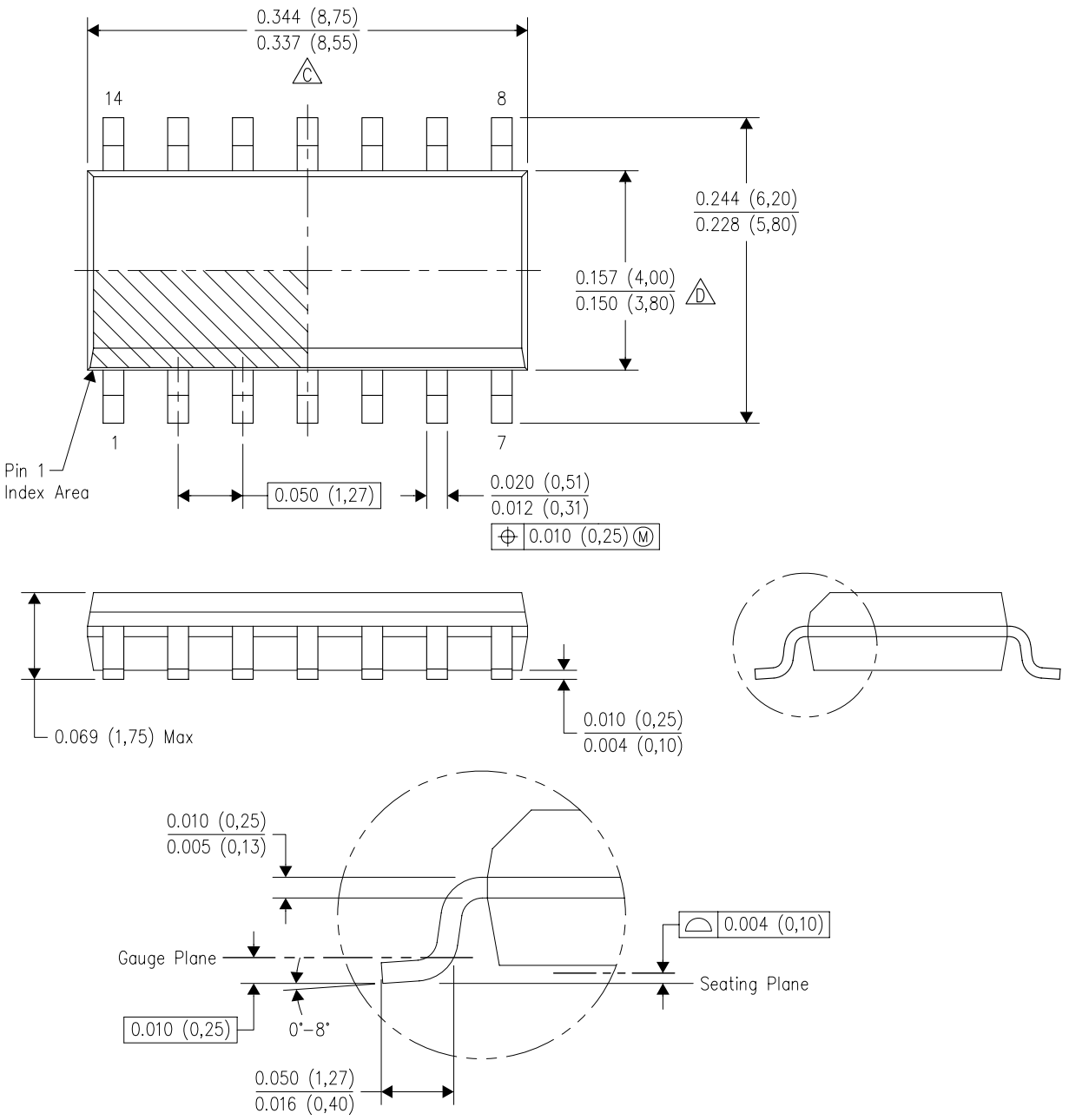

| DIM \ PINS ** | 14 | 16 | 18 | 20 |
|---|---|---|---|---|
| A MAX | 0.775 (19,69) | 0.775 (19,69) | 0.920 (23,37) | 1.060 (26,92) |
| A MIN | 0.745 (18,92) | 0.745 (18,92) | 0.850 (21,59) | 0.940 (23,88) |
| MS–001 VARIATION (C) | AA | BB | AC | AD |




4040049/E 12/2002

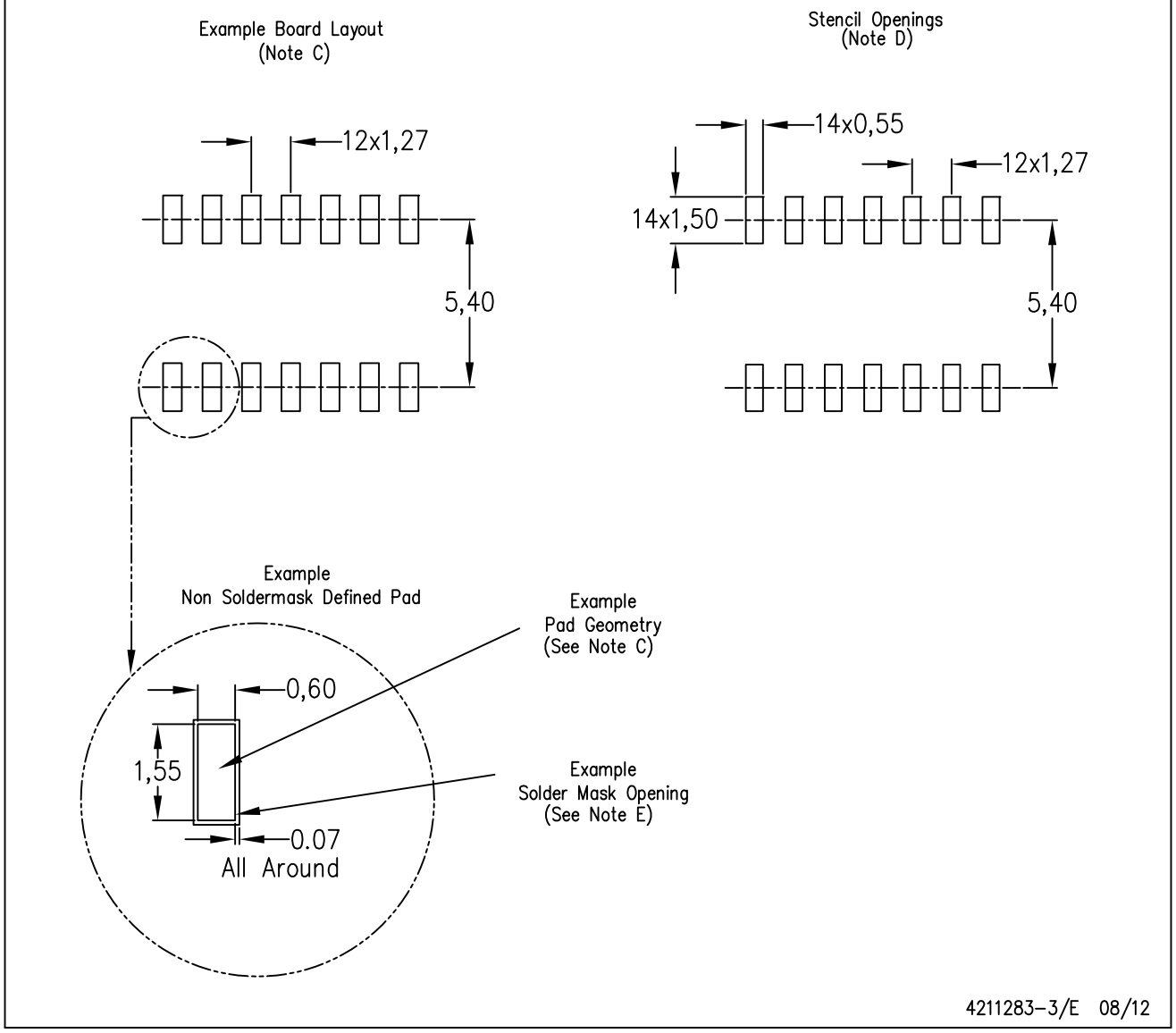
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

D (R–PDSO–G14) PLASTIC SMALL OUTLINE



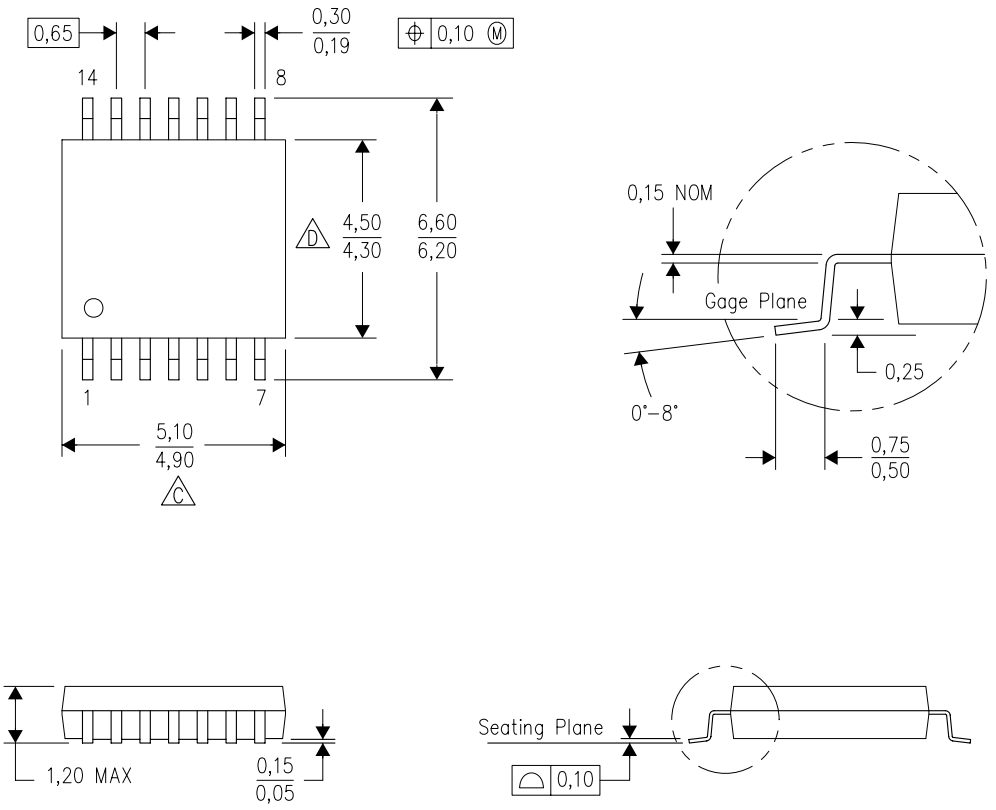

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AB.

D (R–PDSO–G14) PLASTIC SMALL OUTLINE




NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

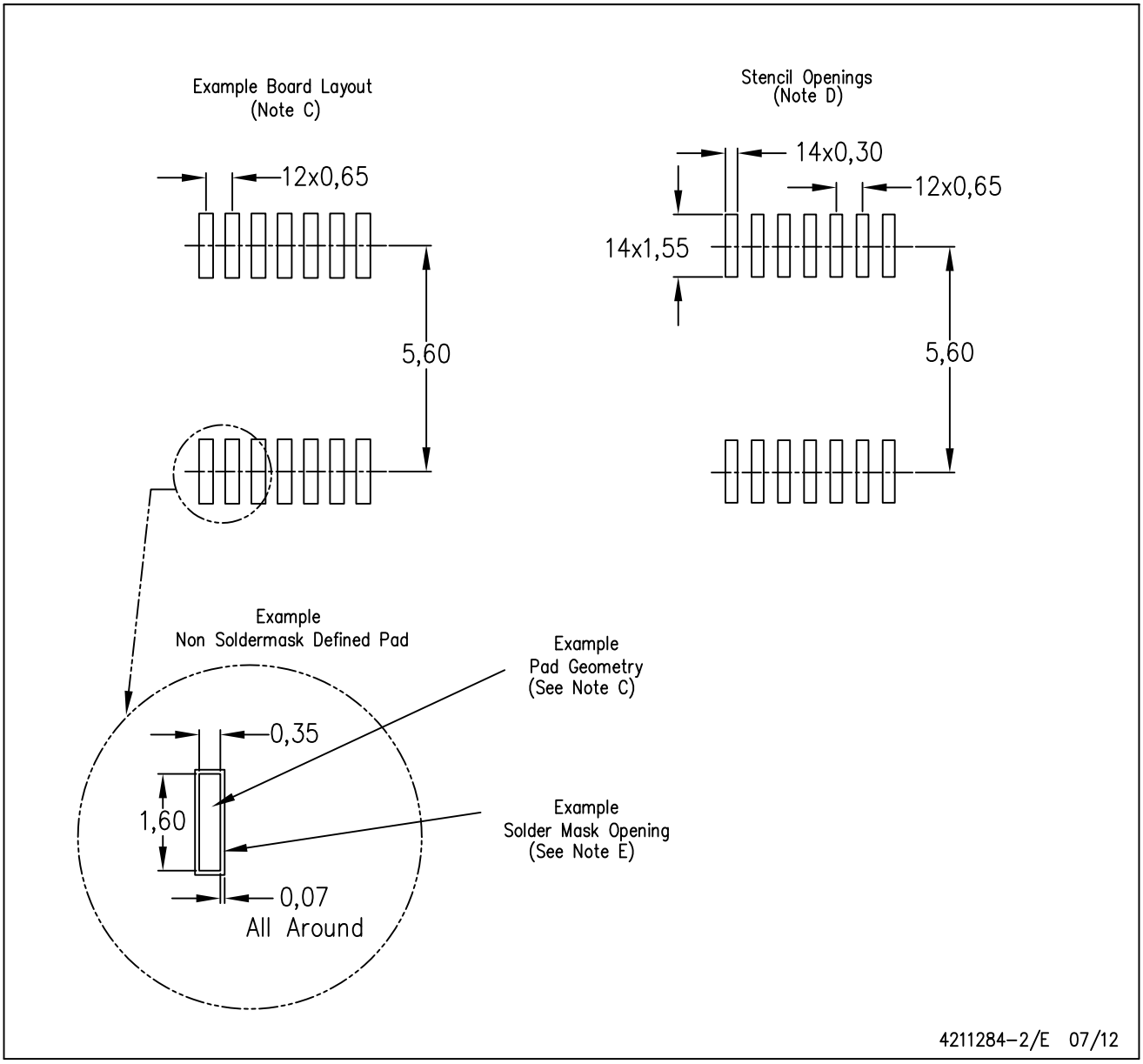
PW (R–PDSO–G14) PLASTIC SMALL OUTLINE




4040064–3/G 02/11

NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
E. Falls within JEDEC MO–153

PW (R–PDSO–G14) PLASTIC SMALL OUTLINE

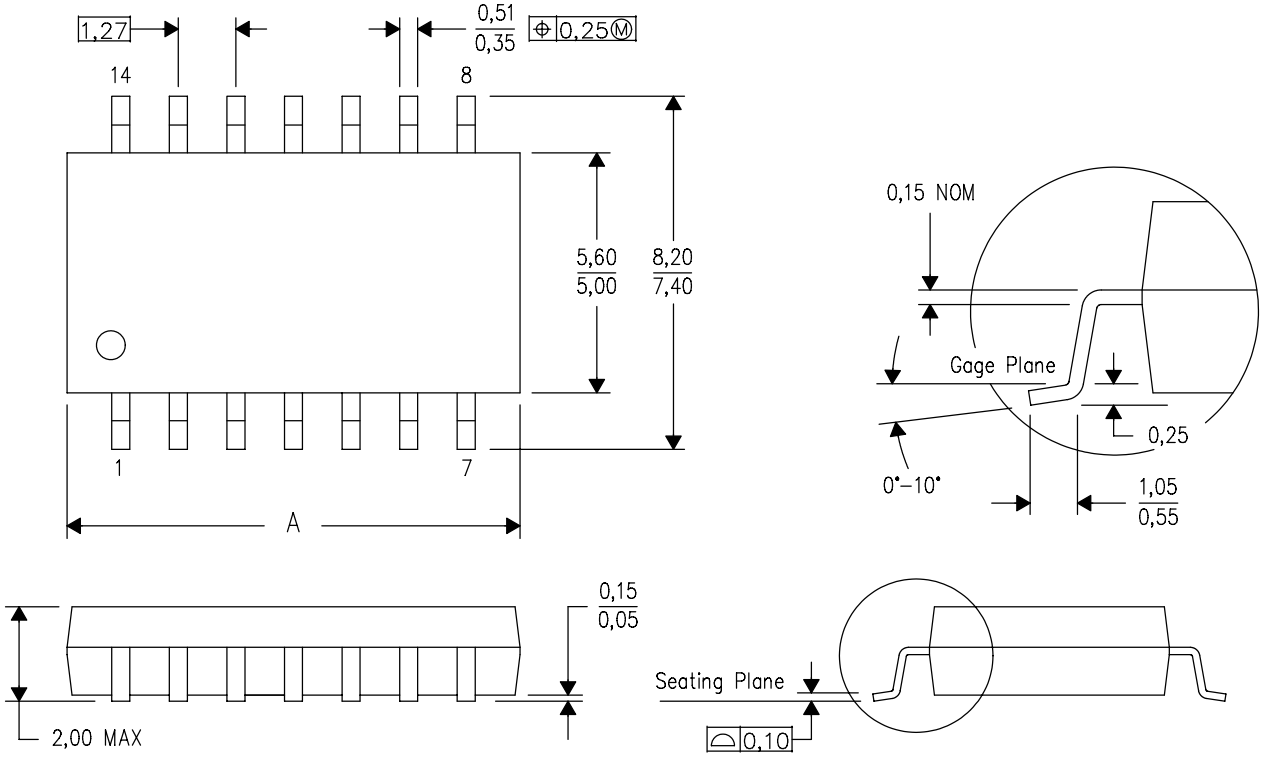



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

## MECHANICAL DATA

**NS (R-PDSO-G**)** **PLASTIC SMALL-OUTLINE PACKAGE**

**14-PINS SHOWN**




| DIM \ PINS ** | 14 | 16 | 20 | 24 |
|---|---|---|---|---|
| A MAX | 10,50 | 10,50 | 12,90 | 15,30 |
| A MIN | 9,90 | 9,90 | 12,30 | 14,70 |

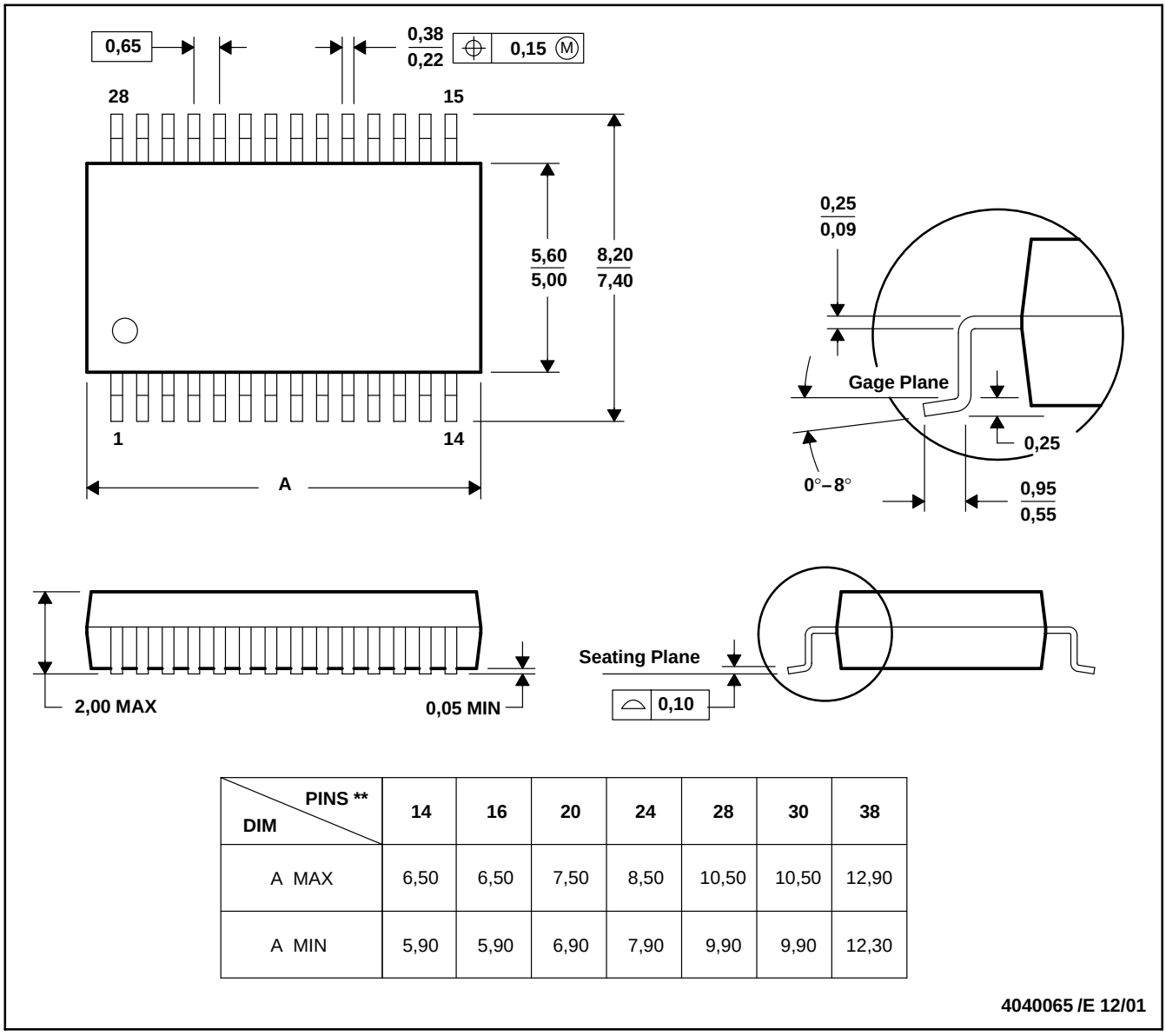
4040062/C 03/03

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

MSSO002E – JANUARY 1995 – REVISED DECEMBER 2001

**DB (R-PDSO-G**)** **PLASTIC SMALL-OUTLINE**

**28 PINS SHOWN**




| DIM \ PINS ** | 14 | 16 | 20 | 24 | 28 | 30 | 38 |
|---|---|---|---|---|---|---|---|
| A MAX | 6,50 | 6,50 | 7,50 | 8,50 | 10,50 | 10,50 | 12,90 |
| A MIN | 5,90 | 5,90 | 6,90 | 7,90 | 9,90 | 9,90 | 12,30 |

**4040065 /E 12/01**

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
D. Falls within JEDEC MO-150

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