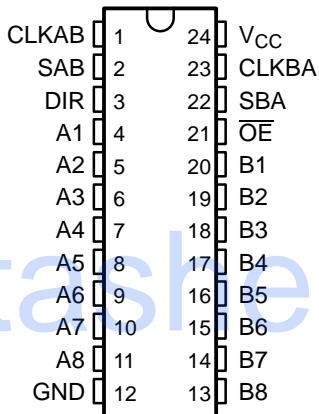


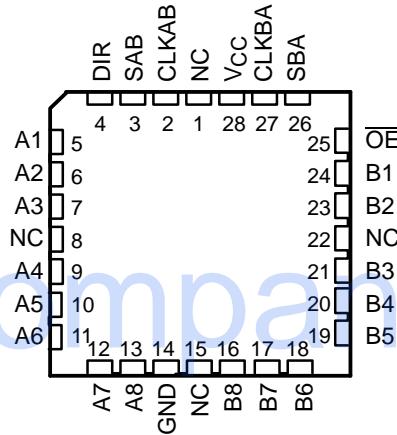
FEATURES

- Operate From 1.65 V to 3.6 V
- Inputs Accept Voltages to 5.5 V
- Max t_{pd} of 7.4 ns at 3.3 V
- Typical V_{OLP} (Output Ground Bounce) <0.8 at $V_{CC} = 3.3$ V, $T_A = 25^\circ\text{C}$
- Typical V_{OHV} (Output V_{OH} Undershoot) >2 V at $V_{CC} = 3.3$ V, $T_A = 25^\circ\text{C}$
- Support Mixed-Mode Signal Operation on All Ports (5-V Input/Output Voltage With 3.3-V V_{CC})
- I_{off} Supports Partial-Power-Down Mode Operation
- Latch-Up Performance Exceeds 250 mA Per JESD 17
- ESD Protection Exceeds JESD 22
 - 2000-V Human-Body Model (A114-A)
 - 200-V Machine Model (A115-A)
 - 1000-V Charged-Device Model (C101)

SN54LVC646A . . . JT OR W PACKAGE
SN74LVC646A . . . DB, DW, NS, OR PW PACKAGE
(TOP VIEW)



SN54LVC646A . . . FK PACKAGE
(TOP VIEW)



NC - No internal connection

DESCRIPTION/ORDERING INFORMATION

The SN54LVC646A octal bus transceiver and register is designed for 2.7-V to 3.6-V V_{CC} operation, and the SN74LVC646A octal bus transceiver and register is designed for 1.65-V to 3.6-V V_{CC} operation.

ORDERING INFORMATION

T_A	PACKAGE ⁽¹⁾	ORDERABLE PART NUMBER	TOP-SIDE MARKING
-40°C to 85°C	SOIC – DW	Tube of 25	SN74LVC646ADW
		Reel of 2000	SN74LVC646ADWR
	SOP – NS	Reel of 2000	SN74LVC646ANSR
	SSOP – DB	Reel of 2000	SN74LVC646ADBR
	TSSOP – PW	Tube of 60	SN74LVC646APW
		Reel of 2000	SN74LVC646APWR
		Reel of 250	SN74LVC646APWT
-55°C to 125°C	CDIP – JT	Tube of 15	SNJ54LVC646AJT
	CFP – W	Tube of 85	SNJ54LVC646AW
	LCCC – FK	Tube of 42	SNJ54LVC646AFK

(1) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

**SN54LVC646A, SN74LVC646A
OCTAL BUS TRANSCEIVERS AND REGISTERS
WITH 3-STATE OUTPUTS**

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DESCRIPTION/ORDERING INFORMATION (CONTINUED)

These devices consist of bus-transceiver circuits, D-type flip-flops, and control circuitry arranged for multiplexed transmission of data directly from the input bus or from the internal registers. Data on the A or B bus is clocked into the registers on the low-to-high transition of the appropriate clock (CLKAB or CLKBA) input. [Figure 1](#) illustrates the four fundamental bus-management functions that are performed with the 'LVC646A devices.

Output-enable (\overline{OE}) and direction-control (DIR) inputs control the transceiver functions. In the transceiver mode, data present at the high-impedance port is stored in either register or in both.

The select-control (SAB and SBA) inputs can multiplex stored and real-time (transparent mode) data. DIR determines which bus receives data when \overline{OE} is low. In the isolation mode (\overline{OE} high), A data is stored in one register and B data can be stored in the other register.

When an output function is disabled, the input function still is enabled and can be used to store and transmit data. Only one of the two buses, A or B, can be driven at a time.

Inputs can be driven from either 3.3-V or 5-V devices. This feature allows the use of these devices as translators in a mixed 3.3-V/5-V system environment.

These devices are fully specified for partial-power-down applications using I_{off} . The I_{off} circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

To ensure the high-impedance state during power up or power down, \overline{OE} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

FUNCTION TABLE

INPUTS						DATA I/O		OPERATION OR FUNCTION
\overline{OE}	DIR	CLKAB	CLKBA	SAB	SBA	A1–A8	B1–B8	
X	X	↑	X	X	X	Input	Unspecified ⁽¹⁾	Store A, B unspecified ⁽¹⁾
X	X	X	↑	X	X	Unspecified ⁽¹⁾	Input	Store B, A unspecified ⁽¹⁾
H	X	↑	↑	X	X	Input	Input	Store and B data
H	X	H or L	H or L	X	X	Input disabled	Input disabled	Isolation, hold storage
L	L	X	X	X	L	Output	Input	Real-time B data to A bus
L	L	X	H or L	X	H	Output	Input	Stored B data to A bus
L	H	X	X	L	X	Input	Output	Real-time A data to B bus
L	H	H or L	X	H	X	Input	Output	Stored A data to B bus

- (1) The data-output functions can be enabled or disabled by various signals at \overline{OE} and DIR. Data-input functions always are enabled; i.e., data at the bus terminals is stored on every low-to-high transition of the clock inputs.

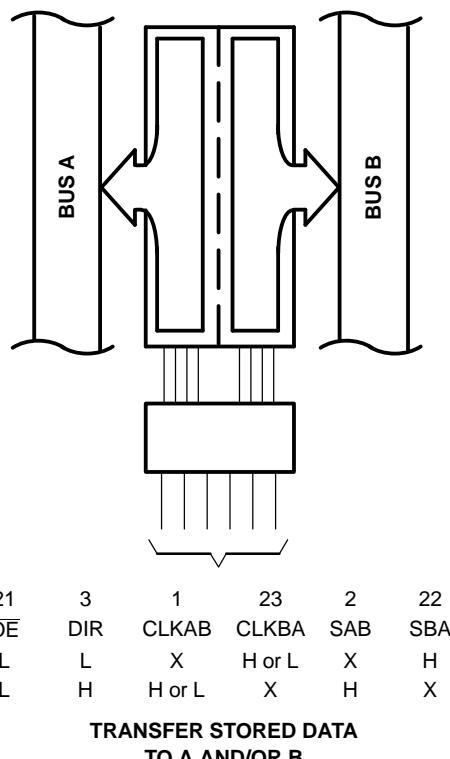
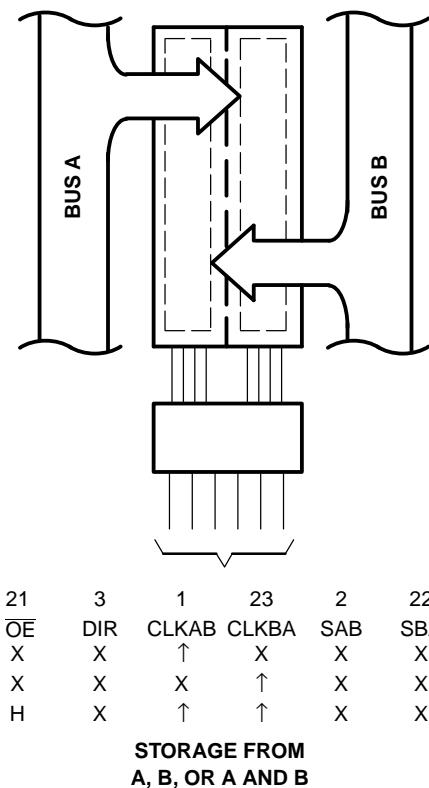
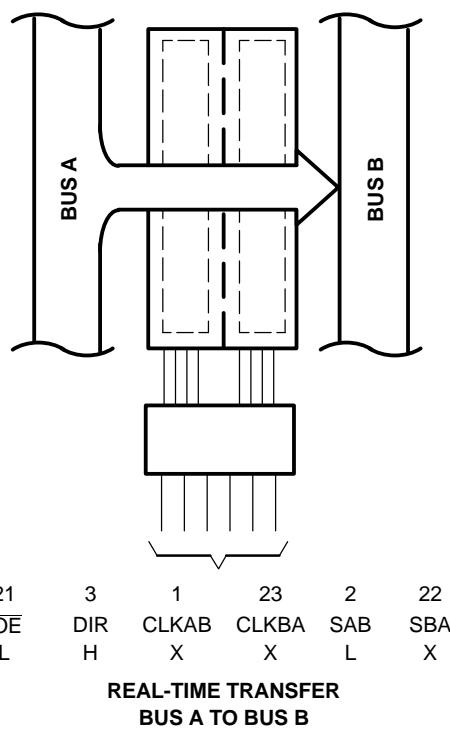
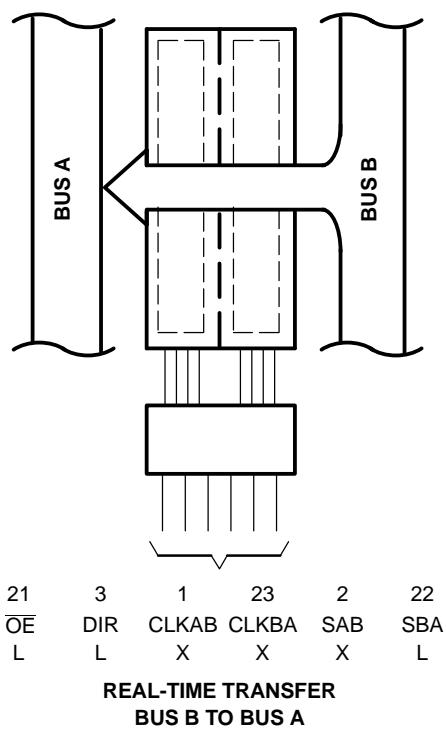


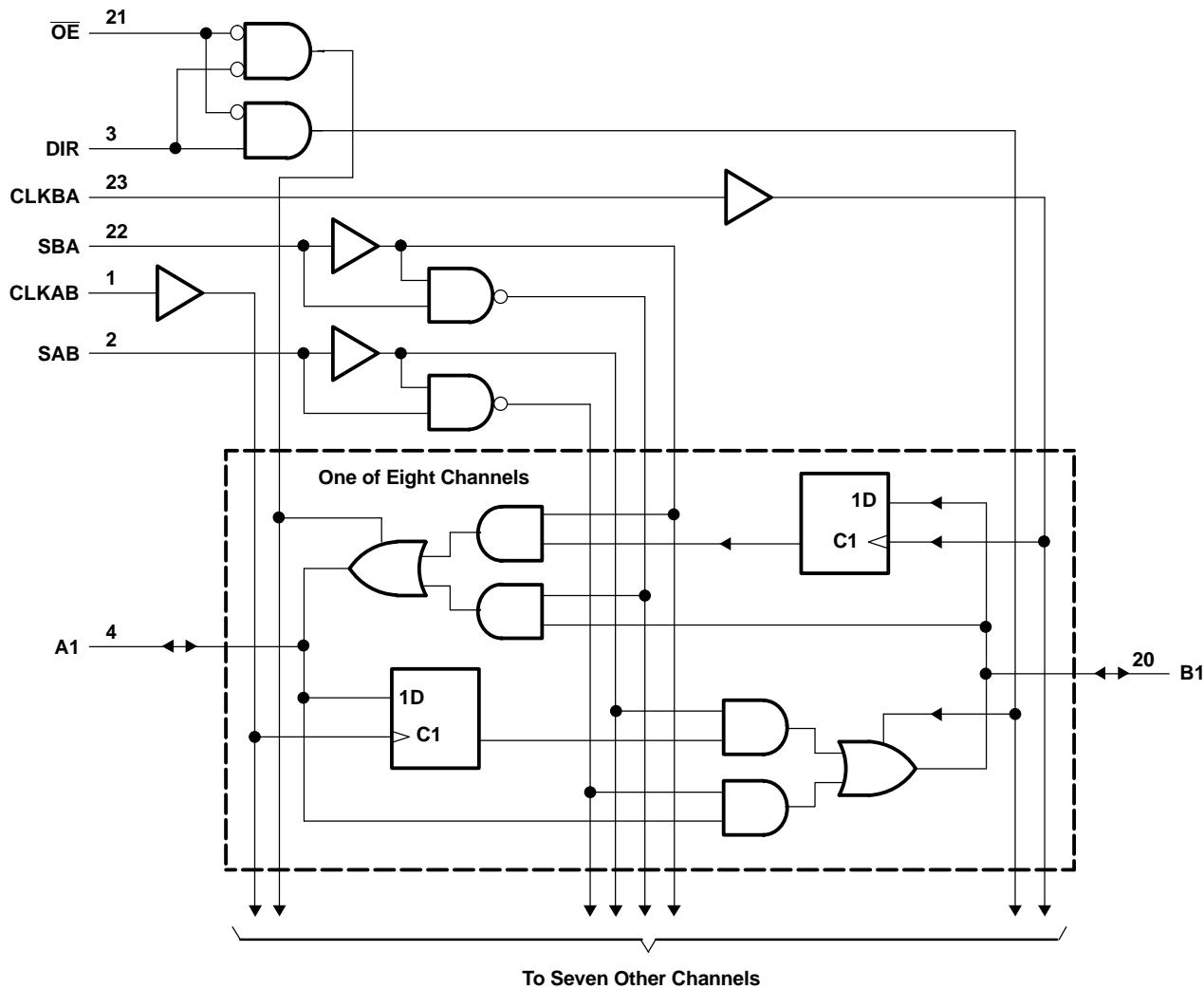
Figure 1. Bus-Management Functions

**SN54LVC646A, SN74LVC646A
OCTAL BUS TRANSCEIVERS AND REGISTERS
WITH 3-STATE OUTPUTS**

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LOGIC DIAGRAM (POSITIVE LOGIC)



Pin numbers shown are for the DB, DW, JT, NS, PW, and W packages.

Absolute Maximum Ratings⁽¹⁾

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V _{CC}	Supply voltage range		-0.5	6.5	V
V _I	Input voltage range ⁽²⁾		-0.5	6.5	V
V _O	Voltage range applied to any output in the high-impedance or power-off state ⁽²⁾		-0.5	6.5	V
V _O	Voltage range applied to any output in the high or low state ⁽²⁾⁽³⁾		-0.5	V _{CC} + 0.5	V
I _{IK}	Input clamp current	V _I < 0		-50	mA
I _{OK}	Output clamp current	V _O < 0		-50	mA
I _O	Continuous output current			±50	mA
	Continuous current through V _{CC} or GND			±100	mA
θ _{JA}	Package thermal impedance ⁽⁴⁾	DB package		63	°C/W
		DW package		46	
		NS package		65	
		PW package		88	
T _{stg}	Storage temperature range		-65	150	°C

- (1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.
- (3) The value of V_{CC} is provided in the recommended operating conditions table.
- (4) The package thermal impedance is calculated in accordance with JESD 51-7.

Recommended Operating Conditions⁽¹⁾

		SN54LVC646A		SN74LVC646A		UNIT	
		MIN	MAX	MIN	MAX		
V _{CC}	Supply voltage	Operating	2	3.6	1.65	3.6	V
		Data retention only	1.5		1.5		
V _{IH}	High-level input voltage	V _{CC} = 1.65 V to 1.95 V		0.65 × V _{CC}		V	
		V _{CC} = 2.3 V to 2.7 V		1.7			
		V _{CC} = 2.7 V to 3.6 V	2	2			
V _{IL}	Low-level input voltage	V _{CC} = 1.65 V to 1.95 V		0.35 × V _{CC}		V	
		V _{CC} = 2.3 V to 2.7 V		0.7			
		V _{CC} = 2.7 V to 3.6 V	0.8	0.8			
V _I	Input voltage	0	5.5	5.5		V	
V _O	Output voltage	High or low state	0	V _{CC}	V _{CC}	V	
		3-state	0	5.5	5.5		
I _{OH}	High-level output current	V _{CC} = 1.65 V			-4	mA	
		V _{CC} = 2.3 V			-8		
		V _{CC} = 2.7 V	-12	-12			
		V _{CC} = 3 V	-24	-24			
I _{OL}	Low-level output current	V _{CC} = 1.65 V			4	mA	
		V _{CC} = 2.3 V			8		
		V _{CC} = 2.7 V	12	12			
		V _{CC} = 3 V	24	24			
Δt/Δv	Input transition rise or fall rate		10	10	ns/V		
T _A	Operating free-air temperature	-55	125	-40	85	°C	

- (1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

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OCTAL BUS TRANSCEIVERS AND REGISTERS
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Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC}	SN54LVC646A			SN74LVC646A			UNIT
			MIN	TYP ⁽¹⁾	MAX	MIN	TYP ⁽¹⁾	MAX	
V _{OH}	I _{OH} = -100 µA	1.65 V to 3.6 V				V _{CC} - 0.2			V
		2.7 V to 3.6 V	V _{CC} - 0.2						
	I _{OH} = -4 mA	1.65 V				1.2			
	I _{OH} = -8 mA	2.3 V				1.7			
	I _{OH} = -12 mA	2.7 V	2.2			2.2			
		3 V	2.4			2.4			
V _{OL}	I _{OL} = 100 µA	1.65 V to 3.6 V				0.2			V
		2.7 V to 3.6 V		0.2					
	I _{OL} = 4 mA	1.65 V				0.45			
	I _{OL} = 8 mA	2.3 V				0.7			
	I _{OL} = 12 mA	2.7 V		0.4		0.4			
	I _{OL} = 24 mA	3 V		0.55		0.55			
I _I	Control inputs	V _I = 0 to 5.5 V	3.6 V		±5		±5		µA
I _{off}		V _I or V _O = 5.5 V	0				±10		µA
I _{OZ} ⁽²⁾		V _O = 0 to 5.5 V	3.6 V		±15		±10		µA
I _{CC}	V _I = V _{CC} or GND 3.6 V ≤ V _I ≤ 5.5 V ⁽³⁾	I _O = 0	3.6 V		10		10		µA
					10		10		
ΔI _{CC}		One input at V _{CC} - 0.6 V, Other inputs at V _{CC} or GND	2.7 V to 3.6 V		500		500		µA
C _i	Control inputs	V _I = V _{CC} or GND	3.3 V		4.5		4.5		pF
C _{io}	A or B port	V _O = V _{CC} or GND	3.3 V		7.5		7.5		pF

(1) All typical values are at V_{CC} = 3.3 V, T_A = 25°C.

(2) For I/O ports, the parameter I_{OZ} includes the input leakage current.

(3) This applies in the disabled state only.

Timing Requirements

over recommended operating free-air temperature range (unless otherwise noted) (see [Figure 2](#))

		SN54LVC646A				UNIT	
		V _{CC} = 2.7 V		V _{CC} = 3.3 V ± 0.3 V			
		MIN	MAX	MIN	MAX		
f _{clock}	Clock frequency			150	150	MHz	
t _w	Pulse duration			3.3	3.3	ns	
t _{su}	Setup time, data before CLK↑			1.6	1.5	ns	
t _h	Hold time, data after CLK↑			1.7	1.7	ns	

Timing Requirements

over recommended operating free-air temperature range (unless otherwise noted) (see [Figure 2](#))

		SN74LVC646A								UNIT	
		$V_{CC} = 1.8 \text{ V} \pm 0.18 \text{ V}$		$V_{CC} = 2.5 \text{ V} \pm 0.2 \text{ V}$		$V_{CC} = 2.7 \text{ V}$		$V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$			
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX		
f_{clock}	Clock frequency	(1)	(1)	(1)	(1)	150	150	150	150	MHz	
t_w	Pulse duration	(1)	(1)	(1)	(1)	3.3	3.3	3.3	3.3	ns	
t_{su}	Setup time, data before CLK↑	(1)	(1)	(1)	(1)	1.6	1.6	1.5	1.5	ns	
t_h	Hold time, data after CLK↑	(1)	(1)	(1)	(1)	1.7	1.7	1.7	1.7	ns	

(1) This information was not available at the time of publication.

Switching Characteristics

over recommended operating free-air temperature range (unless otherwise noted) (see [Figure 2](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN54LVC646A				UNIT	
			$V_{CC} = 2.7 \text{ V}$		$V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$			
			MIN	MAX	MIN	MAX		
f_{max}			150	150	150	150	MHz	
t_{pd}	A or B	B or A	(1)	(1)	7.9	1	7.4	
	CLK		(1)	(1)	8.8	1	8.4	
	SBA or SAB		(1)	(1)	9.9	1	8.6	
t_{en}	\overline{OE}	A	(1)	(1)	10.2	1	8.2	ns
t_{dis}	\overline{OE}	A	(1)	(1)	8.9	1	7.5	ns
t_{en}	DIR	B	(1)	(1)	10.4	1	8.3	ns
t_{dis}	DIR	B	(1)	(1)	8.7	1	7.9	ns

Switching Characteristics

over recommended operating free-air temperature range (unless otherwise noted) (see [Figure 2](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN74LVC646A				UNIT		
			$V_{CC} = 1.8 \text{ V} \pm 0.15 \text{ V}$		$V_{CC} = 2.5 \text{ V} \pm 0.2 \text{ V}$				
			MIN	MAX	MIN	MAX			
f_{max}			(1)	(1)	(1)	(1)	150	150	
t_{pd}	A or B	B or A	(1)	(1)	(1)	(1)	7.9	1	7.4
	CLK		(1)	(1)	(1)	(1)	8.8	1	8.4
	SBA or SAB		(1)	(1)	(1)	(1)	9.9	1	8.6
t_{en}	\overline{OE}	A	(1)	(1)	(1)	(1)	10.2	1	8.2
t_{dis}	\overline{OE}	A	(1)	(1)	(1)	(1)	8.9	1	7.5
t_{en}	DIR	B	(1)	(1)	(1)	(1)	10.4	1	8.3
t_{dis}	DIR	B	(1)	(1)	(1)	(1)	8.7	1	7.9

(1) This information was not available at the time of publication.

**SN54LVC646A, SN74LVC646A
OCTAL BUS TRANSCEIVERS AND REGISTERS
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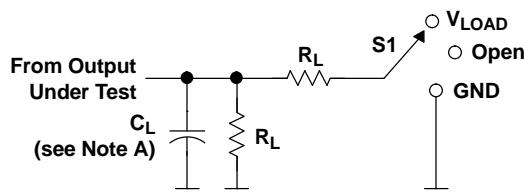
Operating Characteristics

T_A = 25°C

PARAMETER	TEST CONDITIONS	V _{CC} = 1.8 V	V _{CC} = 2.5 V	V _{CC} = 3.3 V	UNIT
		TYP	TYP	TYP	
Cpd Power dissipation capacitance per transceiver	Outputs enabled	(1)	(1)	75	pF
	Outputs disabled	(1)	(1)	9	

(1) This information was not available at the time of publication.

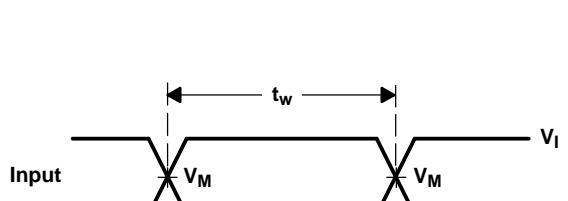
PARAMETER MEASUREMENT INFORMATION



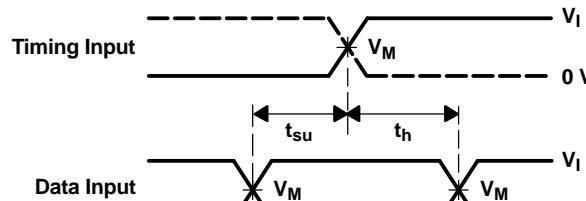
TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	V_{LOAD}
t_{PHZ}/t_{PZH}	GND

LOAD CIRCUIT

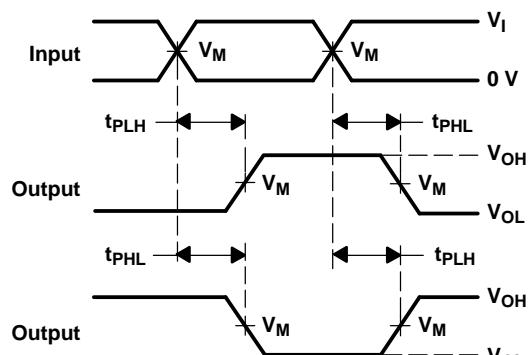
V_{CC}	INPUTS		V_M	V_{LOAD}	C_L	R_L	V_Δ
	V_I	t_r/t_f					
$1.8 \text{ V} \pm 0.15 \text{ V}$	V_{CC}	$\leq 2 \text{ ns}$	$V_{CC}/2$	$2 \times V_{CC}$	30 pF	1 k Ω	0.15 V
$2.5 \text{ V} \pm 0.2 \text{ V}$	V_{CC}	$\leq 2 \text{ ns}$	$V_{CC}/2$	$2 \times V_{CC}$	30 pF	500 Ω	0.15 V
2.7 V	2.7 V	$\leq 2.5 \text{ ns}$	1.5 V	6 V	50 pF	500 Ω	0.3 V
$3.3 \text{ V} \pm 0.3 \text{ V}$	2.7 V	$\leq 2.5 \text{ ns}$	1.5 V	6 V	50 pF	500 Ω	0.3 V



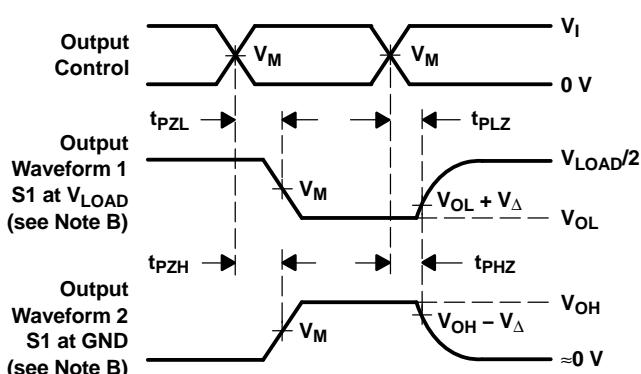
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

NOTES: A. C_L includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR $\leq 10 \text{ MHz}$, $Z_O = 50 \Omega$.
- D. The outputs are measured one at a time, with one transition per measurement.
- E. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
- F. t_{PZL} and t_{PZH} are the same as t_{en} .
- G. t_{PLH} and t_{PHL} are the same as t_{pd} .
- H. All parameters and waveforms are not applicable to all devices.

Figure 2. Load Circuit and Voltage Waveforms

PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
5962-9762601Q3A	ACTIVE	LCCC	FK	28	1	TBD	Call TI	Level-NC-NC-NC
5962-9762601QKA	ACTIVE	CFP	W	24	1	TBD	Call TI	Level-NC-NC-NC
5962-9762601QLA	ACTIVE	CDIP	JT	24	1	TBD	Call TI	Level-NC-NC-NC
SN74LVC646ADBLE	OBsolete	SSOP	DB	24		TBD	Call TI	Call TI
SN74LVC646ADBR	ACTIVE	SSOP	DB	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LVC646ADBRE4	ACTIVE	SSOP	DB	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LVC646ADW	ACTIVE	SOIC	DW	24	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LVC646ADWE4	ACTIVE	SOIC	DW	24	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LVC646ADWR	ACTIVE	SOIC	DW	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LVC646ADWRE4	ACTIVE	SOIC	DW	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LVC646ANSR	ACTIVE	SO	NS	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LVC646ANSRE4	ACTIVE	SO	NS	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LVC646APW	ACTIVE	TSSOP	PW	24	60	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LVC646APWE4	ACTIVE	TSSOP	PW	24	60	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LVC646APWLE	OBsolete	TSSOP	PW	24		TBD	Call TI	Call TI
SN74LVC646APWR	ACTIVE	TSSOP	PW	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LVC646APWRE4	ACTIVE	TSSOP	PW	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LVC646APWT	ACTIVE	TSSOP	PW	24	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LVC646APWTE4	ACTIVE	TSSOP	PW	24	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SNJ54LVC646AFK	ACTIVE	LCCC	FK	28	1	TBD	Call TI	Level-NC-NC-NC
SNJ54LVC646AJT	ACTIVE	CDIP	JT	24	1	TBD	Call TI	Level-NC-NC-NC
SNJ54LVC646AW	ACTIVE	CFP	W	24	1	TBD	Call TI	Level-NC-NC-NC

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBsolete: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS) or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered

at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(³) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

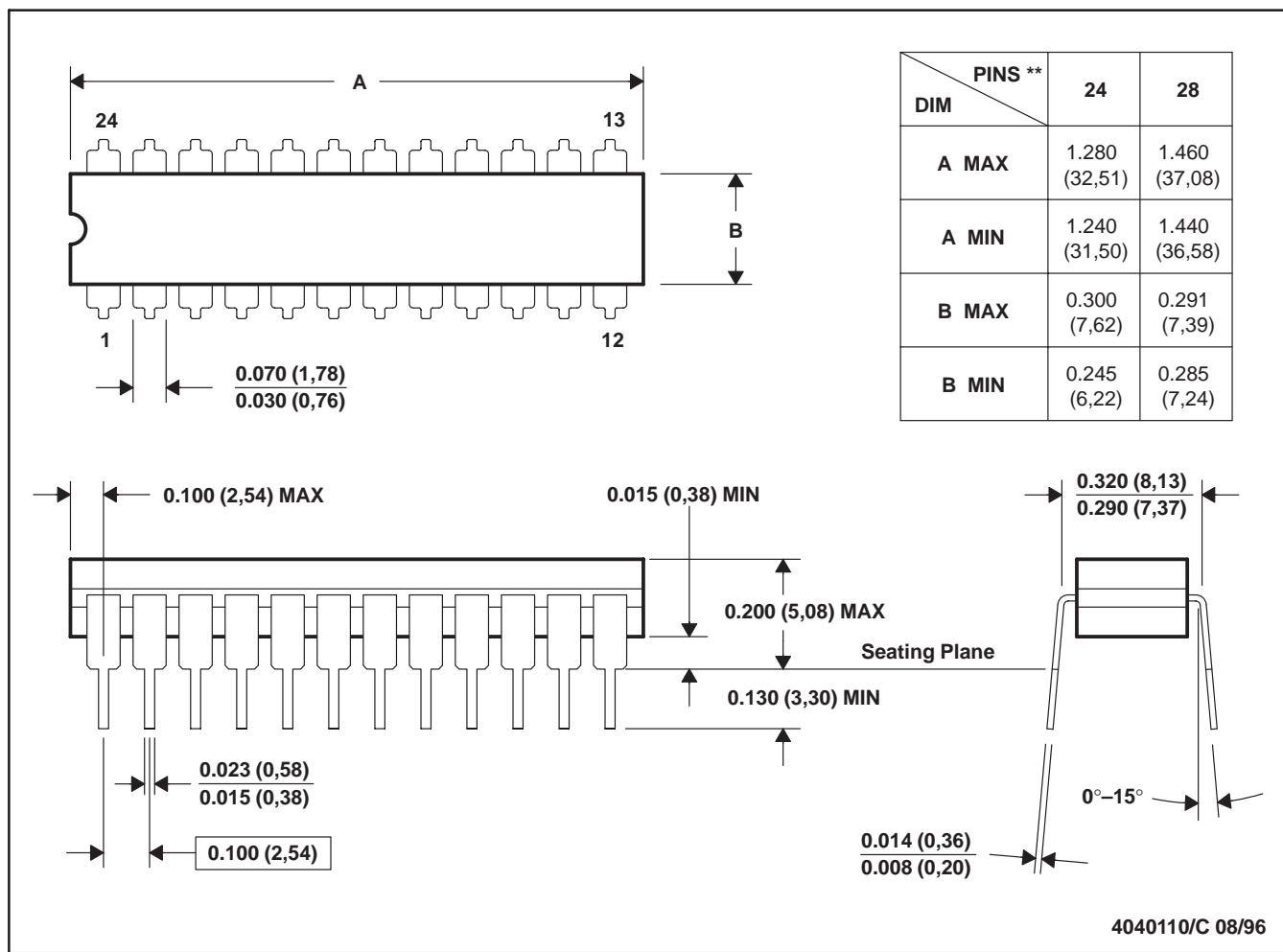
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JT (R-GDIP-T**)

24 LEADS SHOWN

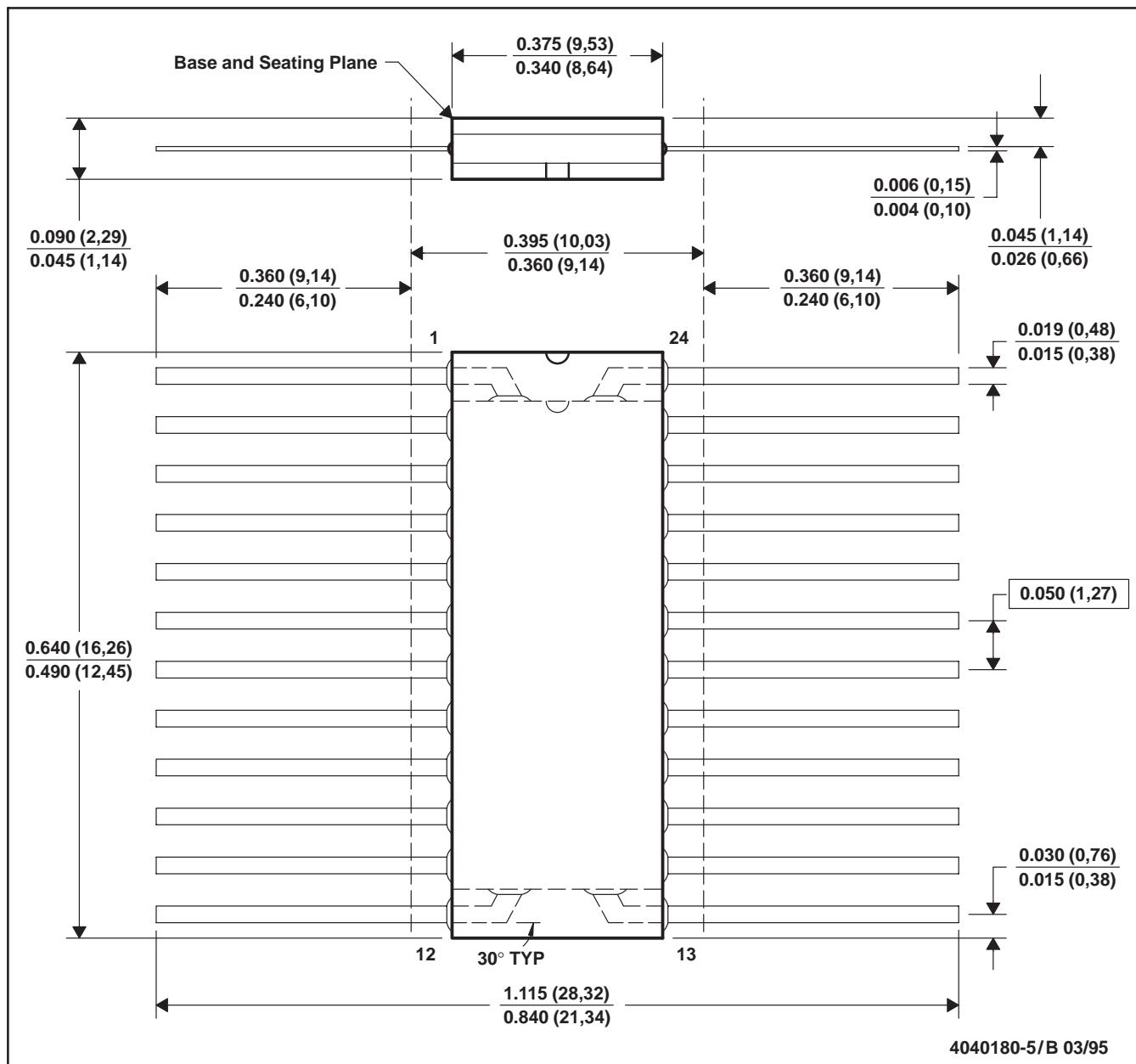
CERAMIC DUAL-IN-LINE



- NOTES:
- All linear dimensions are in inches (millimeters).
 - This drawing is subject to change without notice.
 - This package can be hermetically sealed with a ceramic lid using glass frit.
 - Index point is provided on cap for terminal identification.
 - Falls within MIL STD 1835 GDIP3-T24, GDIP4-T28, and JEDEC MO-058 AA, MO-058 AB

W (R-GDFP-F24)

CERAMIC DUAL FLATPACK

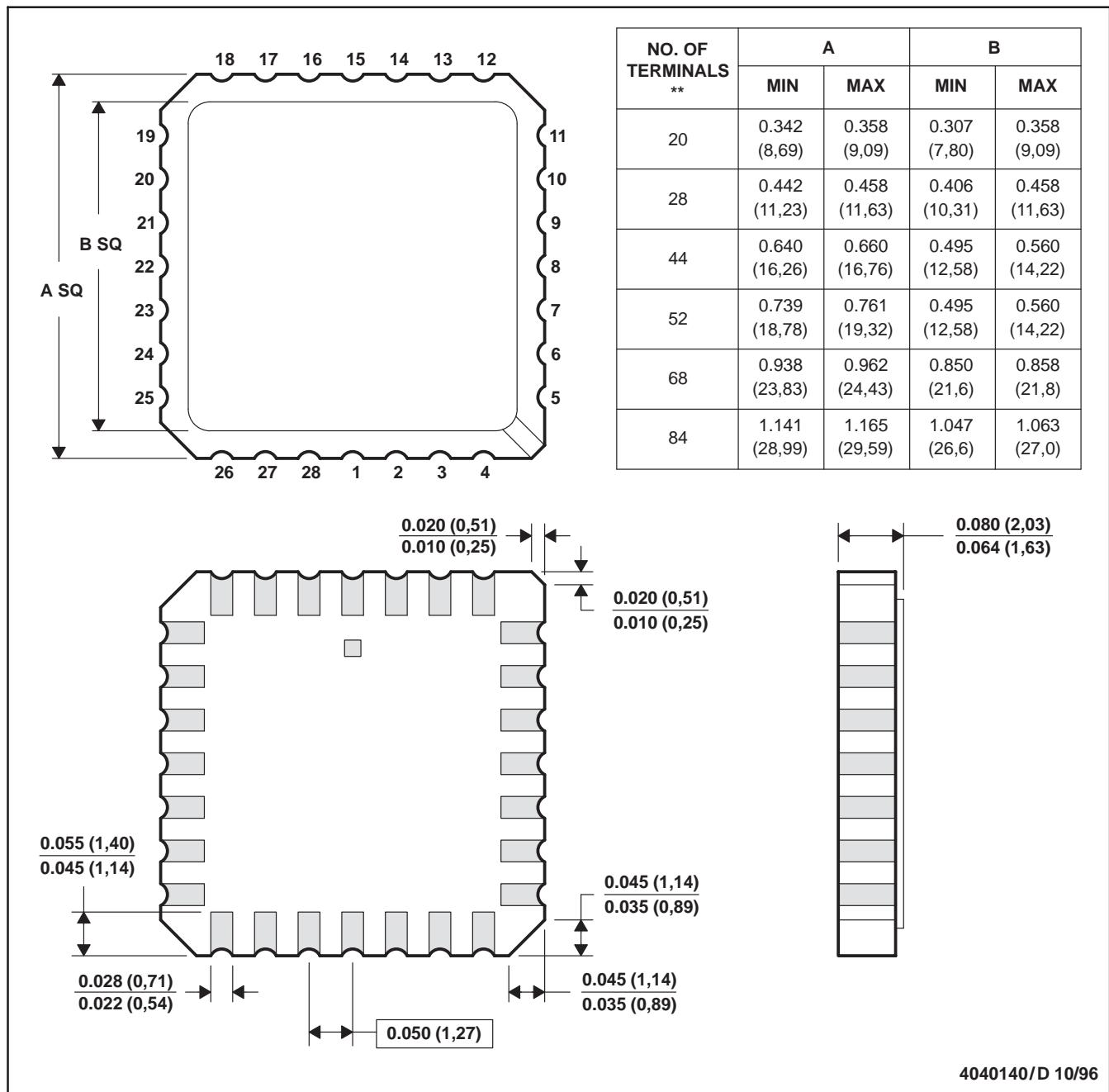


- NOTES: A. All linear dimensions are in inches (millimeters).
 B. This drawing is subject to change without notice.
 C. This package can be hermetically sealed with a ceramic lid using glass frit.
 D. Falls within MIL-STD-1835 GDFP2-F24 and JEDEC MO-070AD
 E. Index point is provided on cap for terminal identification only.

FK (S-CQCC-N**)

LEADLESS CERAMIC CHIP CARRIER

28 TERMINAL SHOWN



NOTES: A. All linear dimensions are in inches (millimeters).

B. This drawing is subject to change without notice.

C. This package can be hermetically sealed with a metal lid.

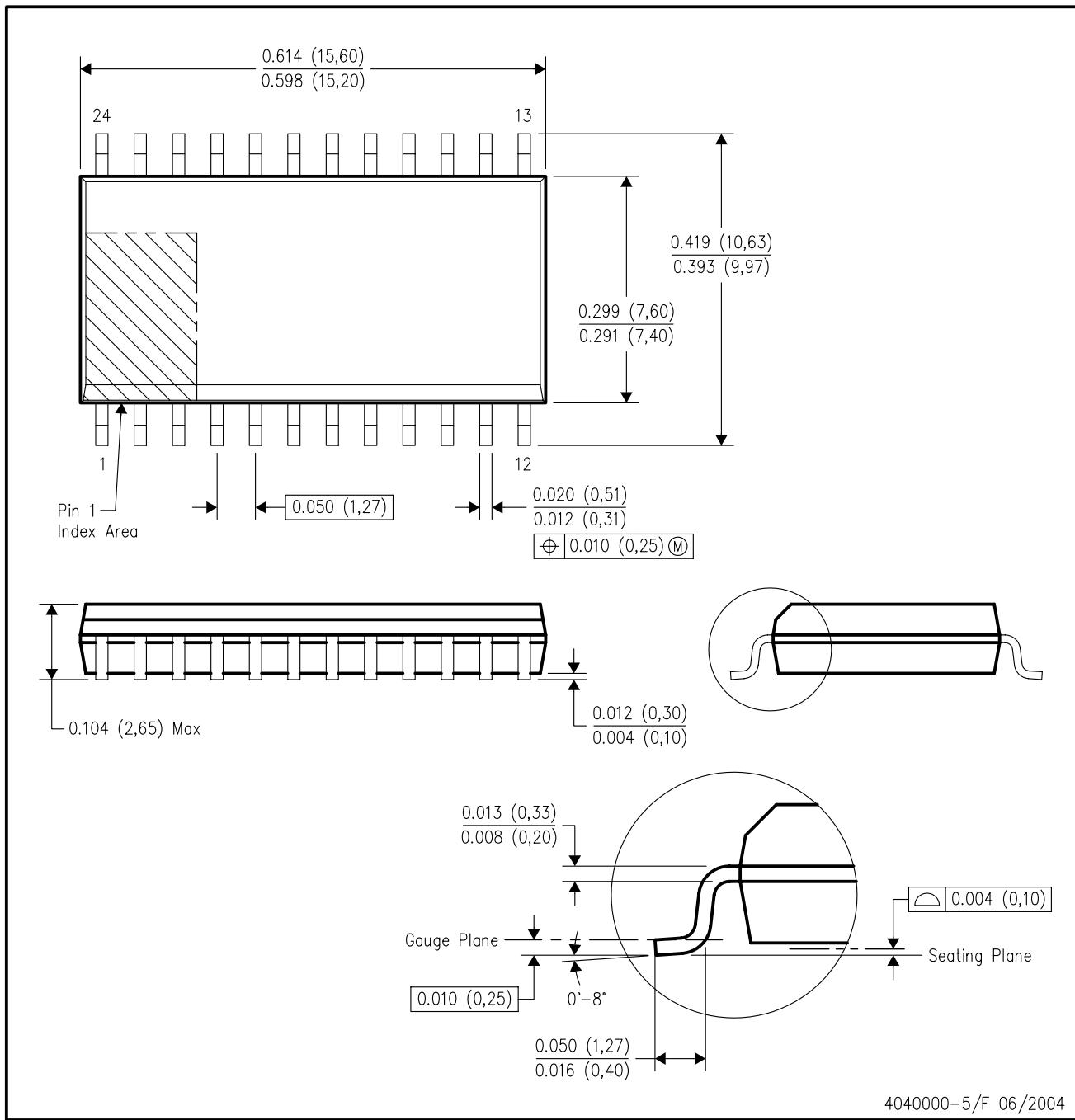
D. The terminals are gold plated.

E. Falls within JEDEC MS-004

4040140/D 10/96

DW (R-PDSO-G24)

PLASTIC SMALL-OUTLINE PACKAGE



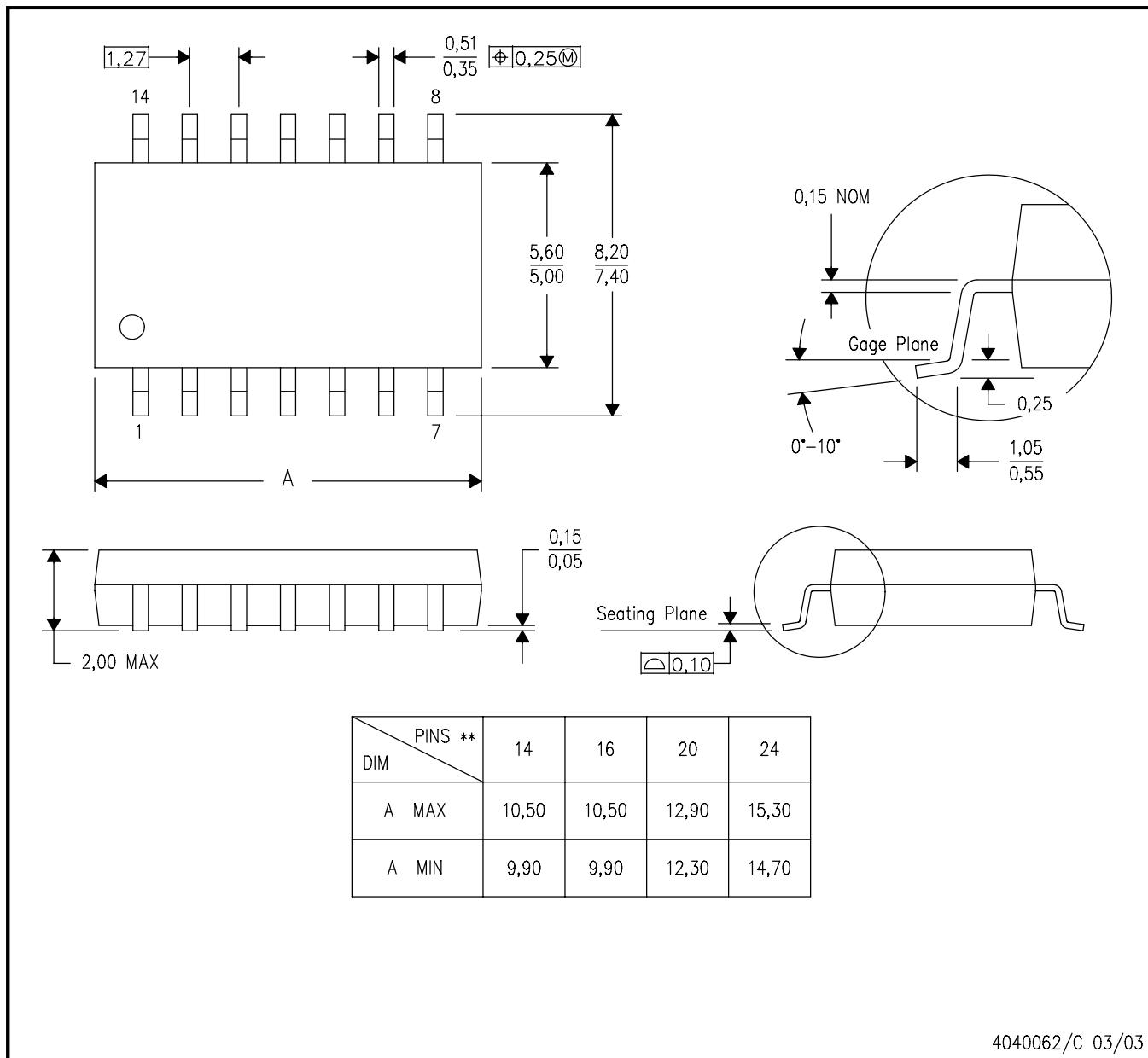
- NOTES:
- All linear dimensions are in inches (millimeters).
 - This drawing is subject to change without notice.
 - Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0.15).
 - Falls within JEDEC MS-013 variation AD.

MECHANICAL DATA

NS (R-PDSO-G)**

14-PINS SHOWN

PLASTIC SMALL-OUTLINE PACKAGE

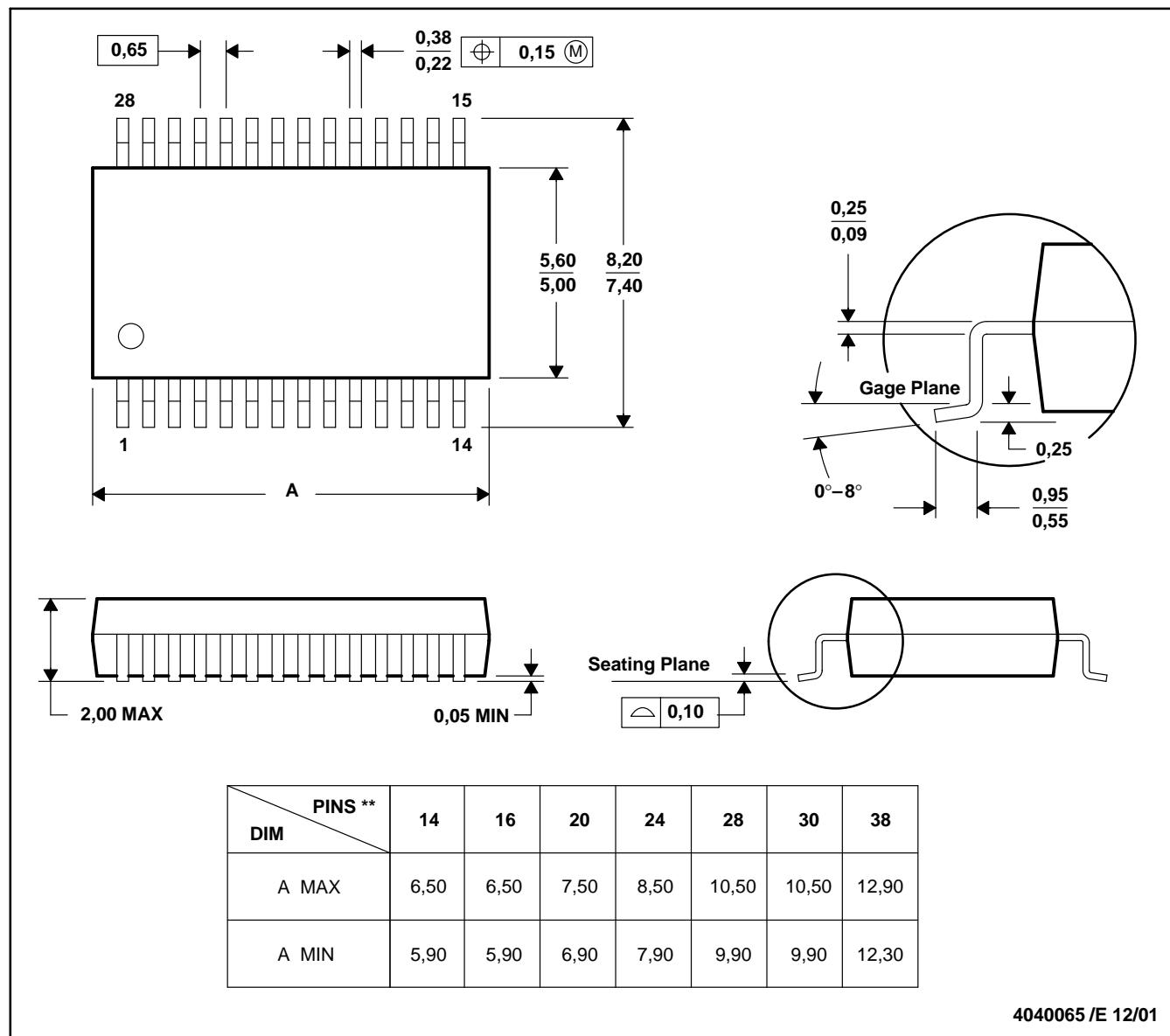


- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

DB (R-PDSO-G**)

PLASTIC SMALL-OUTLINE

28 PINS SHOWN

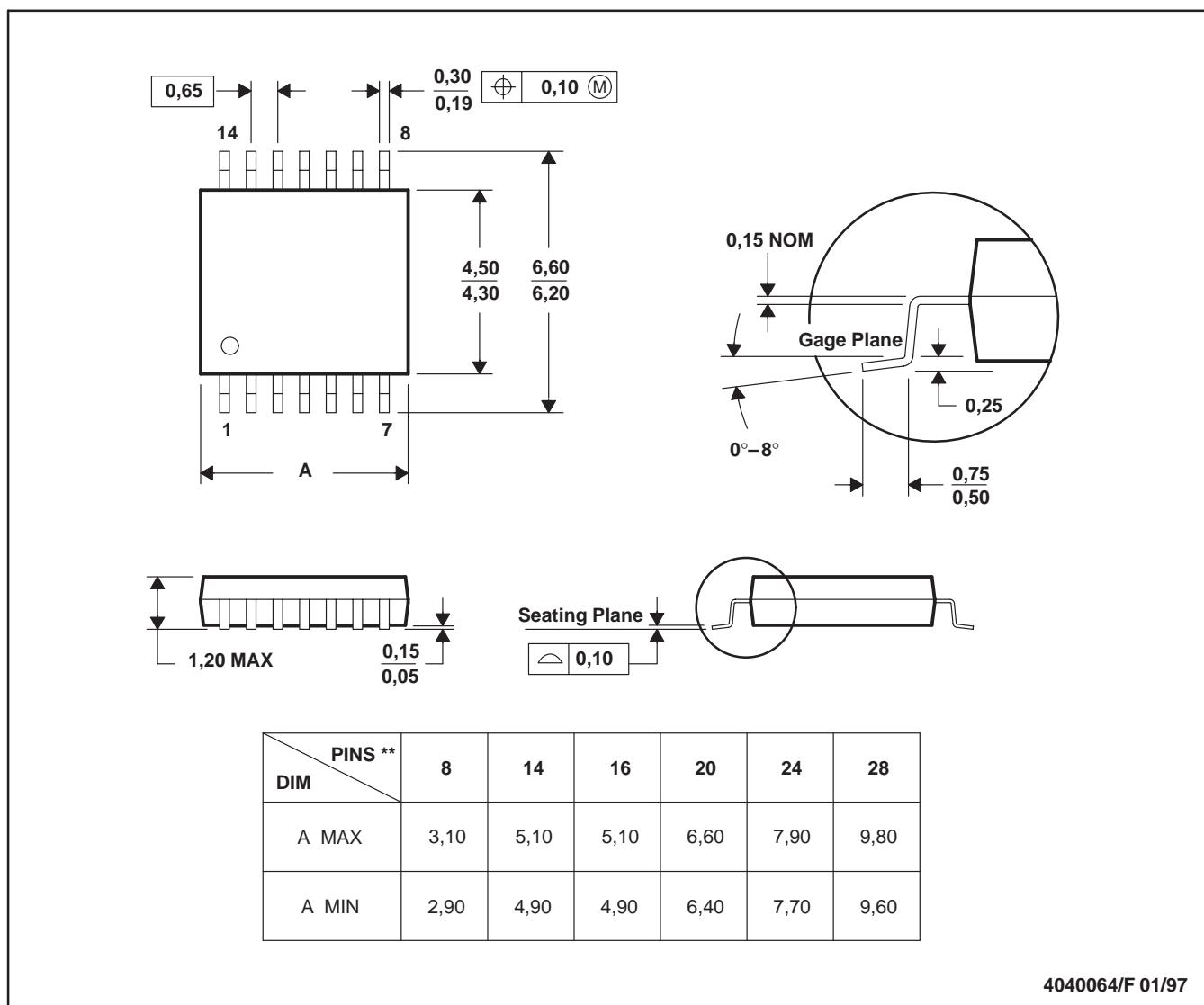


- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
 - D. Falls within JEDEC MO-150

PW (R-PDSO-G^{**})

PLASTIC SMALL-OUTLINE PACKAGE

14 PINS SHOWN



- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Body dimensions do not include mold flash or protrusion not to exceed 0,15.
 - Falls within JEDEC MO-153

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View ROHS Compliant Devices

View RoHS Compliant Devices

 clear gif**SN74LVC646A, Status: ACTIVE**

Octal Bus Transceiver And Register With 3-State Outputs

Output-enable (OE) and direction-control (DIR) inputs control the transceiver functions. In the transceiver mode, data present at the high-impedance port is stored in either register or in both.

The select-control (SAB and SBA) inputs can multiplex stored and real-time (transparent mode) data. DIR determines which bus receives data when OE is low. In the isolation mode (OE high), A data is stored in one register and B data can be stored in the other register.

When an output function is disabled, the input function is still enabled and can be used to store and transmit data. Only one of the two buses, A or B, can be driven at a time.

Inputs can be driven from either 3.3-V or 5-V devices. This feature allows the use of these devices as translators in a mixed 3.3-V/5-V system environment.

These devices are fully specified for partial-power-down applications using I_{off}. The I_{off} circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

To ensure the high-impedance state during power up or power down, OE should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

Pricing/Packaging/CAD Design Tools/Samples

			Price	Packaging			CAD Design Tools	Samples
Device	Status	Temp (°C)	Budget Price (\$US) QTY	Industry Standard (TI Pkg) Pins	Top Side Marking	Standard Pack Quantity	Footprints	Samples
SN74LVC646ADBLE	OBsolete	-40 to 85		SSOP (DB) 24	View		<input type="checkbox"/>	Not Available
SN74LVC646ADBR	ACTIVE	-40 to 85	0.92 1KU	SSOP (DB) 24	View	2000	<input type="checkbox"/>	Contact TI Distributor or Sales Office
SN74LVC646ADBRE4	ACTIVE	-40 to 85	0.92 1KU	SSOP (DB) 24	View	2000	<input type="checkbox"/>	Purchase Samples
SN74LVC646ADW	ACTIVE	-40 to 85	0.92 1KU	SOIC (DW) 24	View	25	<input type="checkbox"/>	Contact TI Distributor or Sales Office
SN74LVC646ADWE4	ACTIVE	-40 to 85	0.92 1KU	SOIC (DW) 24	View	25	<input type="checkbox"/>	Purchase Samples
SN74LVC646ADWR	ACTIVE	-40 to 85	0.92 1KU	SOIC (DW) 24	View	2000	<input type="checkbox"/>	Purchase Samples
SN74LVC646ADWRE4	ACTIVE	-40 to 85	0.92 1KU	SOIC (DW) 24	View	2000	<input type="checkbox"/>	Purchase Samples
SN74LVC646ANSR	ACTIVE	-40 to 85	0.92 1KU	SO (NS) 24	View	2000	<input type="checkbox"/>	Purchase Samples
SN74LVC646ANSRE4	ACTIVE	-40 to 85	0.92 1KU	SO (NS) 24	View	2000	<input type="checkbox"/>	Purchase Samples
SN74LVC646APW	ACTIVE	-40 to 85	0.92 1KU	TSSOP (PW) 24	View	60	<input type="checkbox"/>	Purchase Samples
SN74LVC646APWE4	ACTIVE	-40 to 85	0.92 1KU	TSSOP (PW) 24	View	60	<input type="checkbox"/>	Purchase Samples
SN74LVC646APWLE	OBsolete	-40 to 85		TSSOP (PW) 24	View		<input type="checkbox"/>	Not Available
SN74LVC646APWR	ACTIVE	-40 to 85	0.92 1KU	TSSOP (PW) 24	View	2000	<input type="checkbox"/>	Contact TI Distributor or Sales Office
SN74LVC646APWRE4	ACTIVE	-40 to 85	0.92 1KU	TSSOP (PW) 24	View	2000	<input type="checkbox"/>	Request Free Samples
SN74LVC646APWT	ACTIVE	-40 to 85	0.74 1KU	TSSOP (PW) 24	View	250	<input type="checkbox"/>	Purchase Samples
SN74LVC646APWTE4	ACTIVE	-40 to 85	0.74 1KU	TSSOP (PW) 24	View	250	<input type="checkbox"/>	Purchase Samples

Inventory

TI Inventory Status			Reported Distributor Inventory				
SN74LVC646ADBR	As of 9:06 AM GMT, 29 Nov 2005			As of 9:06 AM GMT, 29 Nov 2005			
	In Stock	In Progress QTY Date	Lead Time	Region	Company	In Stock	Purchase
	0*	4477 20 Dec	6 Weeks	Americas	DigiKey	>1k	<input type="button" value=""/>
		>10k 31 Jan					

[View all Distributors](#)

[Choose a Region](#)



SN74LVC646ADBRE4	As of 9:06 AM GMT, 29 Nov 2005			As of 9:06 AM GMT, 29 Nov 2005			
	In Stock	In Progress QTY Date	Lead Time	Region	Company	In Stock	Purchase
	0*	4477 20 Dec	6 Weeks	None Reported View Distributors			
		>10k 31 Jan					
SN74LVC646ADW	As of 9:06 AM GMT, 29 Nov 2005			As of 9:06 AM GMT, 29 Nov 2005			
	In Stock	In Progress QTY Date	Lead Time	Region	Company	In Stock	Purchase
	0*	4900 12 Dec	4 Weeks	Americas	Avnet	125	
		8598 19 Dec			DigiKey	530	
				Europe	EBV Elektronik	175	
SN74LVC646ADWE4	As of 9:06 AM GMT, 29 Nov 2005			As of 9:06 AM GMT, 29 Nov 2005			
	In Stock	In Progress QTY Date	Lead Time	Region	Company	In Stock	Purchase
	0*	4900 12 Dec	4 Weeks	None Reported View Distributors			
		8598 19 Dec					
SN74LVC646ADWR	As of 9:06 AM GMT, 29 Nov 2005			As of 9:06 AM GMT, 29 Nov 2005			
	In Stock	In Progress QTY Date	Lead Time	Region	Company	In Stock	Purchase
	0*	8607 19 Dec	4 Weeks	None Reported View Distributors			
		>10k 30 Jan					
SN74LVC646ADWRE4	As of 9:06 AM GMT, 29 Nov 2005			As of 9:06 AM GMT, 29 Nov 2005			
	In Stock	In Progress QTY Date	Lead Time	Region	Company	In Stock	Purchase
	0*	8607 19 Dec	4 Weeks	None Reported View Distributors			
		>10k 30 Jan					
SN74LVC646ANSR	As of 9:06 AM GMT, 29 Nov 2005			As of 9:06 AM GMT, 29 Nov 2005			
	In Stock	In Progress QTY Date	Lead Time	Region	Company	In Stock	Purchase
	2000*	2186 30 Nov	4 Weeks	None Reported View Distributors			
		4314 16 Dec					
		2683 27 Jan					
SN74LVC646ANSR	As of 9:06 AM GMT, 29 Nov 2005			As of 9:06 AM GMT, 29 Nov 2005			
	In Stock	In Progress QTY Date	Lead Time	Region	Company	In Stock	Purchase
	2000*	2186 30 Nov	4 Weeks	None Reported View Distributors			
		4314 16 Dec					
		2683 27 Jan					
SN74LVC646APW	As of 9:06 AM GMT, 29 Nov 2005			As of 9:06 AM GMT, 29 Nov 2005			
	In Stock	In Progress QTY Date	Lead Time	Region	Company	In Stock	Purchase

	60*	3540 12 Dec	10 Weeks	None Reported View Distributors			
		4347 23 Dec					
		>10k 3 Feb					
SN74LVC646APWE4	As of 9:06 AM GMT, 29 Nov 2005			As of 9:06 AM GMT, 29 Nov 2005			
	In Stock	In Progress QTY Date	Lead Time	Region	Company	In Stock	Purchase
	60*	3540 12 Dec	10 Weeks	None Reported View Distributors			
		4347 23 Dec					
		>10k 3 Feb					
SN74LVC646APWR	As of 9:06 AM GMT, 29 Nov 2005			As of 9:06 AM GMT, 29 Nov 2005			
	In Stock	In Progress QTY Date	Lead Time	Region	Company	In Stock	Purchase
	0*	2000 12 Dec	10 Weeks	Americas	DigiKey	158	
		4382 23 Dec		Europe	Avnet-SILICA	>1k	
		>10k 3 Feb					
SN74LVC646APWRE4	As of 9:06 AM GMT, 29 Nov 2005			As of 9:06 AM GMT, 29 Nov 2005			
	In Stock	In Progress QTY Date	Lead Time	Region	Company	In Stock	Purchase
	0*	2000 12 Dec	10 Weeks	None Reported View Distributors			
		4382 23 Dec					
		>10k 3 Feb					
SN74LVC646APWT	As of 9:06 AM GMT, 29 Nov 2005			As of 9:06 AM GMT, 29 Nov 2005			
	In Stock	In Progress QTY Date	Lead Time	Region	Company	In Stock	Purchase
	0*	919 6 Jan	10 Weeks	None Reported View Distributors			
		1790 13 Jan					
		1672 20 Jan					
		>10k 3 Feb					
SN74LVC646APWTE4	As of 9:06 AM GMT, 29 Nov 2005			As of 9:06 AM GMT, 29 Nov 2005			
	In Stock	In Progress QTY Date	Lead Time	Region	Company	In Stock	Purchase
	0*	919 6 Jan	10 Weeks	None Reported View Distributors			
		1790 13 Jan					
		1672 20 Jan					
		>10k 3 Feb					

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Quality & Lead (Pb)-Free Data

	Product Content				MTBF/FIT Rate
Device	Eco Plan*	Lead/Ball Finish	MSL Rating/Peak Reflow	Details	Details
SN74LVC646ADBR	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	View	View
SN74LVC646ADBRE4	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	View	View
SN74LVC646ADW	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	View	View
SN74LVC646ADWE4	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	View	View
SN74LVC646ADWR	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	View	View
SN74LVC646ADWRE4	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	View	View
SN74LVC646ANSR	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	View	View
SN74LVC646ANSRE4	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	View	View
SN74LVC646APW	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	View	View
SN74LVC646APWE4	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	View	View
SN74LVC646APWR	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	View	View
SN74LVC646APWRE4	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	View	View
SN74LVC646APWT	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	View	View
SN74LVC646APWTE4	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	View	View

* The planned eco-friendly classification: Pb-Free (RoHS) or Green (RoHS & no Sb/Br) - please click on the Product Content Details "View" link in the table above for the latest availability information and additional product content details.

If the information you are requesting is not available online at this time, contact one of our [Product Information Centers](#) regarding the availability of this information.

Technical Documents

Datasheets

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SN54LVC646A, SN74LVC646A (Rev. J) ([sn74lvc646a.pdf](#), 386 KB)

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Application Notes

Semiconductor Packing Material Electrostatic Discharge (ESD) Protection ([szza047.htm](#), 9 KB)

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Selecting the Right Level Translation Solution (Rev. A) ([scea035a.htm](#), 9 KB)

22 Jun 2004 [Abstract](#)

Shelf-Life Evaluation of Lead-Free Component Finishes ([szza046.htm](#), 9 KB)

24 May 2004 [Abstract](#)

Use of the CMOS Unbuffered Inverter in Oscillator Circuits ([szza043.htm](#), 9 KB)

06 Nov 2003 [Abstract](#)

Understanding and Interpreting Standard-Logic Data Sheets (Rev. B) ([szza036b.htm](#), 8 KB)

28 May 2003 [Abstract](#)

Texas Instruments Little Logic Application Report ([scea029.htm](#), 9 KB)

01 Nov 2002 [Abstract](#)

TI IBIS File Creation, Validation, and Distribution Processes ([szza034.htm](#), 9 KB)

29 Aug 2002 [Abstract](#)

16-Bit Widebus Logic Families in 56-Ball, 0.65-mm Pitch Very Thin Fine-Pitch BGA (Rev. B) ([szza029b.htm](#), 9 KB)

22 May 2002 [Abstract](#)

Power-Up 3-State (PU3S) Circuits in TI Standard Logic Devices ([szza033.htm](#), 9 KB)

10 May 2002 [Abstract](#)

Selecting the Right Texas Instruments Signal Switch ([szza030.htm](#), 9 KB)

07 Sep 2001 [Abstract](#)

Implications of Slow or Floating CMOS Inputs (Rev. C) ([scba004c.htm](#), 9 KB)

01 Feb 1998 [Abstract](#)

Bus-Interface Devices With Output-Damping Resistors Or Reduced-Drive Outputs (Rev. A) ([scba012a.htm](#), 9 KB)

01 Aug 1997 [Abstract](#)

CMOS Power Consumption and CPD Calculation (Rev. B) ([scaa035b.htm](#), 9 KB)

01 Jun 1997 [Abstract](#)

LVC Characterization Information ([scba011.htm](#), 9 KB)

01 Dec 1996 [Abstract](#)

Live Insertion ([sdya012.htm](#), 9 KB)

01 Oct 1996 [Abstract](#)

Input and Output Characteristics of Digital Integrated Circuits ([sdya010.htm](#), 9 KB)

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User Guides

Signal Switch Data Book (Rev. A) (scdd003a.pdf, 19732 KB)

14 Nov 2003 [Download](#)

LVC and LV Low-Voltage CMOS Logic Data Book (Rev. B) (scbd152b.pdf, 13291 KB)

18 Dec 2002 [Download](#)

LOGIC Pocket Data Book (scyd013.pdf, 4835 KB)

05 Dec 2002 [Download](#)

Simulation Models

IBIS Model

IBIS Model of SN74LVC646A (Rev. A) (scem057a.ibs, 38 KB)

01 Nov 2000 [ibis](#) / [zip](#)

More Literature

Logic Selection Guide 2005 (Rev. X) (sdyu001x.pdf, 6909 KB)

15 Mar 2005 [Download](#)

Wireless Infrastructure Solutions Guide (2Q2005) (Rev. E) (sstc001e.pdf, 734 KB)

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Design Summary for WCSP Little Logic (Rev. B) (scet007b.pdf, 295 KB)

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Logic Cross-Reference (Rev. A) (scyb017a.pdf, 2938 KB)

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SN74LVC1G3157 and SNS74LVC2G53 SPDT Analog Switches (scyb014.pdf, 65 KB)

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STANDARD LINEAR AND LOGIC FOR DVD/VCD PLAYERS (scym001.pdf, 5872 KB)

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