# European Analog Seminar - 1997 

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## Amplifiers

- LM6132/4 Dual/Quad Low Power, 10MHz GBW, Rail to Rail I/O OpAmp
- LM6152/4 Dual/Quad High Speed, Low Power, 75MHz GBW RR I/O OpAmp
- LM7301 Low Power, 4MHz GBW, RR I/O OpAmp in Tiny Package


Absolute Maximum Ratings (Note 1)
If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.
ESD Tolerance (Note 2)
Differential Input Voltage
2500V
Voltage at Input/Output Pin
$\left(V^{+}\right)+0.3 V,\left(V^{-}\right)-0.3 V$
Supply Voltage ( $\mathrm{V}^{+}-\mathrm{V}^{-}$)
35 V
Current at Input Pin $\pm 10 \mathrm{~mA}$
Current at Output Pin (Note 3) $\pm 25 \mathrm{~mA}$
Current at Power Supply Pin
50 mA
Lead Temp. (soldering, 10 sec .) $260^{\circ} \mathrm{C}$
Storage Temperature Range $\quad-65^{\circ} \mathrm{C}$ to $+150^{\circ} \mathrm{C}$
Junction Temperature (Note 4)
$150^{\circ} \mathrm{C}$

Operating Ratings (Note 1)

| Supply Voltage | $1.8 \mathrm{~V} \leq \mathrm{V}_{\mathrm{S}} \leq 24 \mathrm{~V}$ |
| :--- | ---: |
| Junction Temperature Range | $-40^{\circ} \mathrm{C} \leq \mathrm{T}_{\mathrm{J}} \leq+85^{\circ} \mathrm{C}$ |
| LM6132, LM6134 |  |
| Thermal resistance $\left(\theta_{\mathrm{JA}}\right)$ | $115^{\circ} \mathrm{C} / \mathrm{W}$ |
| N Package, 8-pin Molded DIP | $193^{\circ} \mathrm{C} / \mathrm{W}$ |
| M Package, 8-pin Surface Mount | $81^{\circ} \mathrm{C} / \mathrm{W}$ |
| N Package, 14-pin Molded DIP | $126^{\circ} \mathrm{C} / \mathrm{W}$ |
| M Package, 14-pin Surface Mount |  |
|  |  |

5.0V DC Electrical Characteristics Unless otherwise specified, all limits guaranteed for $\mathrm{T}_{\mathrm{J}}=25^{\circ} \mathrm{C}, \mathrm{V}+=$ $5.0 \mathrm{~V}, \mathrm{~V}^{-}=0 \mathrm{~V}, \mathrm{~V}_{\mathrm{CM}}=\mathrm{V}_{\mathrm{O}}=\mathrm{V}^{+} / 2$ and $\mathrm{R}_{\mathrm{L}}>1 \mathrm{M} \Omega$ to $\mathrm{V}_{\mathrm{S}} / 2$. Boldface limits apply at the temperature extremes

| Symbol | Parameter | Conditions | $\begin{array}{c}\text { Typ } \\ \text { (Note 5) }\end{array}$ | $\begin{array}{c}\text { LM6134AI } \\ \text { LM6132AI } \\ \text { Limit } \\ \text { (Note 6) }\end{array}$ | $\begin{array}{c}\text { LM6134BI } \\ \text { LM6132BI } \\ \text { Limit } \\ \text { (Note 6) }\end{array}$ | Units |
| :--- | :--- | :--- | :---: | :---: | :---: | :---: |$\}$


| 5.0V DC Electrical Characteristics Unless otherwise specified, all limits guaranteed for $\mathrm{T}_{\mathrm{J}}=25^{\circ} \mathrm{C}, \mathrm{V}^{+}=$ $5.0 \mathrm{~V}, \mathrm{~V}^{-}=0 \mathrm{~V}, \mathrm{~V}_{\mathrm{CM}}=\mathrm{V}_{\mathrm{O}}=\mathrm{V}^{+} / 2$ and $\mathrm{R}_{\mathrm{L}}>1 \mathrm{M} \Omega$ to $\mathrm{V}_{\mathrm{S}} / 2$. Boldface limits apply at the temperature extremes (Continued) |  |  |  |  |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| Symbol | Parameter | Conditions | Typ <br> (Note 5) | LM6134AI <br> LM6132AI <br> Limit <br> (Note 6) | LM6134BI <br> LM6132BI Limit (Note 6) | Units |
| $\mathrm{V}_{\mathrm{O}}$ | Output Swing | 100k Load | 4.992 | $\begin{gathered} 4.98 \\ \mathbf{4 . 9 3} \end{gathered}$ | $\begin{aligned} & 4.98 \\ & 4.93 \end{aligned}$ | $\begin{gathered} \mathrm{V} \\ \mathrm{~min} \end{gathered}$ |
|  |  |  | 0.007 | $\begin{gathered} 0.017 \\ 0.019 \end{gathered}$ | $\begin{gathered} 0.017 \\ 0.019 \end{gathered}$ | $\begin{gathered} \mathrm{V} \\ \max \end{gathered}$ |
|  |  | 10k Load | 4.952 | $\begin{array}{r} 4.94 \\ \mathbf{4 . 8 5} \end{array}$ | $\begin{gathered} 4.94 \\ \mathbf{4 . 8 5} \end{gathered}$ | $\begin{gathered} \mathrm{V} \\ \mathrm{~min} \end{gathered}$ |
|  |  |  | 0.032 | $\begin{aligned} & 0.07 \\ & \mathbf{0 . 0 9} \end{aligned}$ | $\begin{gathered} 0.07 \\ \mathbf{0 . 0 9} \end{gathered}$ | $\begin{gathered} \mathrm{V} \\ \max \end{gathered}$ |
|  |  | 5k Load | 4.923 | $\begin{aligned} & 4.90 \\ & \mathbf{4 . 8 5} \end{aligned}$ | $\begin{aligned} & 4.90 \\ & \mathbf{4 . 8 5} \end{aligned}$ | $\begin{gathered} \mathrm{V} \\ \mathrm{~min} \end{gathered}$ |
|  |  |  | 0.051 | $\begin{aligned} & 0.095 \\ & \mathbf{0 . 1 2} \end{aligned}$ | $\begin{aligned} & 0.095 \\ & \mathbf{0 . 1 2} \end{aligned}$ | $\begin{gathered} \text { V } \\ \max \end{gathered}$ |
| Isc | Output Short Circuit Current | Sourcing | 4.3 | 2 | 2 | $\mathrm{mA}$ $\min$ |
|  |  | Sinking | 4.6 | 1.8 | 1.8 | $\begin{aligned} & \mathrm{mA} \\ & \mathrm{~min} \\ & \hline \end{aligned}$ |
| Is | Supply Current | Per Amplifier | 360 | $\begin{array}{r} 400 \\ \mathbf{4 5 0} \\ \hline \end{array}$ | $\begin{array}{r} 400 \\ \mathbf{4 5 0} \\ \hline \end{array}$ | $\mu \mathrm{A}$ $\max$ |

5.0V AC Electrical Characteristics Unless otherwise specified, all limits guaranteed for $\mathrm{T}_{J}=25^{\circ} \mathrm{C}, \mathrm{V}^{+}=$ $5.0 \mathrm{~V}, \mathrm{~V}^{-}=0 \mathrm{~V}, \mathrm{~V}_{\mathrm{CM}}=\mathrm{V}_{\mathrm{O}}=\mathrm{V}^{+} / 2$ and $\mathrm{R}_{\mathrm{L}}>1 \mathrm{M} \Omega$ to $\mathrm{V}_{\mathrm{S}} / 2$. Boldface limits apply at the temperature extremes

| Symbol | Parameter | Conditions | Typ <br> (Note 5) | LM6134AI <br> LM6132AI <br> Limit <br> (Note 6) | LM6134BI <br> LM6132BI <br> Limit <br> (Note 6) | Units |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| SR | Slew Rate | $\begin{aligned} & \pm 4 \mathrm{~V} @ \mathrm{~V}_{\mathrm{S}}= \pm 6 \mathrm{~V} \\ & \mathrm{R}_{\mathrm{S}}<1 \mathrm{k} \Omega \end{aligned}$ | 14 | $\begin{aligned} & 8 \\ & 7 \end{aligned}$ | $\begin{aligned} & 8 \\ & 7 \end{aligned}$ | $\begin{aligned} & \mathrm{V} / \mu \mathrm{s} \\ & \mathrm{~min} \end{aligned}$ |
| GBW | Gain-Bandwidth Product | $\mathrm{f}=20 \mathrm{kHz}$ | 10 | $\begin{gathered} 7.4 \\ 7 \end{gathered}$ | $\begin{gathered} 7.4 \\ 7 \end{gathered}$ | $\underset{\min }{\mathrm{MHz}}$ |
| $\theta \mathrm{m}$ | Phase Margin | $\mathrm{R}_{\mathrm{L}}=10 \mathrm{k}$ | 33 |  |  | deg |
| $\mathrm{G}_{\mathrm{m}}$ | Gain Margin | $\mathrm{R}_{\mathrm{L}}=10 \mathrm{k}$ | 10 |  |  | dB |
| $e_{n}$ | Input Referred Voltage Noise | $\mathrm{f}=1 \mathrm{kHz}$ | 27 |  |  | $\frac{n \mathrm{~V}}{\sqrt{\mathrm{~Hz}}}$ |
| $\mathrm{i}_{\mathrm{n}}$ | Input Referred Current Noise | $\mathrm{f}=1 \mathrm{kHz}$ | 0.18 |  |  | $\frac{\mathrm{pA}}{\sqrt{\mathrm{Hz}}}$ |


| 2.7V DC Electrical Characteristics Unless otherwise specified, all limits guaranteed for $\mathrm{T}_{\mathrm{J}}=25^{\circ} \mathrm{C}, \mathrm{V}^{+}=$ $2.7 \mathrm{~V}, \mathrm{~V}^{-}=0 \mathrm{~V}, \mathrm{~V}_{\mathrm{CM}}=\mathrm{V}_{\mathrm{O}}=\mathrm{V}^{+} / 2$ and $\mathrm{R}_{\mathrm{L}}>1 \mathrm{M} \Omega$ to $\mathrm{V}_{\mathrm{S}} / 2$. Boldface limits apply at the temperature extreme |  |  |  |  |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| Symbol | Parameter | Conditions | $\begin{gathered} \text { Typ } \\ \text { (Note 5) } \end{gathered}$ | LM6134AI <br> LM6132AI <br> Limit <br> (Note 6) | LM6134BI <br> LM6132BI Limit (Note 6) | Units |
| $\mathrm{V}_{\text {OS }}$ | Input Offset Voltage |  | 0.12 | $\begin{aligned} & 2 \\ & \mathbf{8} \end{aligned}$ | $\begin{gathered} 6 \\ 12 \end{gathered}$ | mV max |
| $\mathrm{I}_{\mathrm{B}}$ | Input Bias Current | $\mathrm{OV} \leq \mathrm{V}_{\mathrm{CM}} \leq 2.7 \mathrm{~V}$ | 90 |  |  | nA |
| los | Input Offset Current |  | 2.8 |  |  | nA |
| $\mathrm{R}_{\text {IN }}$ | Input Resistance |  | 134 |  |  | $\mathrm{M} \Omega$ |
| CMRR | Common Mode Rejection Ratio | $\mathrm{OV} \leq \mathrm{V}_{\mathrm{CM}} \leq 2.7 \mathrm{~V}$ | 82 |  |  | dB |
| PSRR | Power Supply Rejection Ratio | $\pm 1.35 \mathrm{~V} \leq \mathrm{V}_{\mathrm{S}} \leq \pm 12 \mathrm{~V}$ | 80 |  |  | dB |
| $\mathrm{V}_{\mathrm{CM}}$ | Input Common-Mode Voltage Range |  |  | 2.7 | 2.7 | V |
|  |  |  |  | 0 | 0 |  |
| $A_{V}$ | Large Signal Voltage Gain | $\mathrm{R}_{\mathrm{L}}=10 \mathrm{k}$ | 100 |  |  | $\mathrm{V} / \mathrm{mV}$ |
| $\mathrm{V}_{0}$ | Output Swing | $\mathrm{R}_{\mathrm{L}}=10 \mathrm{k}$ | 0.03 | $\begin{gathered} 0.08 \\ \mathbf{0 . 1 1 2} \end{gathered}$ | $\begin{gathered} 0.08 \\ \mathbf{0 . 1 1 2} \end{gathered}$ | V max |
|  |  |  | 2.66 | $\begin{gathered} 2.65 \\ \mathbf{2 . 2 5} \end{gathered}$ | $\begin{aligned} & 2.65 \\ & \mathbf{2 . 2 5} \end{aligned}$ | $\begin{gathered} \mathrm{V} \\ \mathrm{~min} \end{gathered}$ |
| Is | Supply Current | Per Amplifier | 330 |  |  | $\mu \mathrm{A}$ |

2.7V AC Electrical Characteristics Unless otherwise specified, all limits guaranteed for $\mathrm{T}_{\mathrm{J}}=25^{\circ} \mathrm{C}, \mathrm{V}+=$ $2.7 \mathrm{~V}, \mathrm{~V}^{-}=\mathrm{oV}, \mathrm{V}_{\mathrm{CM}}=\mathrm{V}_{\mathrm{O}}=\mathrm{V}+/ 2$ and $\mathrm{R}_{\mathrm{L}}>1 \mathrm{M} \Omega$ to $\mathrm{V}_{\mathrm{S}} / 2$.

| Symbol | Parameter | Conditions | Typ <br> (Note 5) | LM6134AI <br> LM6132AI <br> Limit <br> (Note 6) | LM6134BI <br> LM6132BI <br> Limit <br> (Note 6) | Units |
| :--- | :--- | :--- | :---: | :---: | :---: | :---: |
| GBW | Gain-Bandwidth Product | $\mathrm{R}_{\mathrm{L}}=10 \mathrm{k}, \mathrm{f}=20 \mathrm{kHz}$ | 7 |  |  | MHz |
| $\theta_{\mathrm{m}}$ | Phase Margin | $\mathrm{R}_{\mathrm{L}}=10 \mathrm{k}$ | 23 |  | deg |  |
| $\mathrm{G}_{\mathrm{m}}$ | Gain Margin |  | 12 |  | dB |  |

24V DC Electrical Characteristics Unless otherwise specified, all limits guaranteed for $\mathrm{T}_{\mathrm{J}}=25^{\circ} \mathrm{C}, \mathrm{V}+=$ $24 \mathrm{~V}, \mathrm{~V}^{-}=0 \mathrm{~V}, \mathrm{~V}_{\mathrm{CM}}=\mathrm{V}_{\mathrm{O}}=\mathrm{V}^{+} / 2$ and $\mathrm{R}_{\mathrm{L}}>1 \mathrm{M} \Omega$ to $\mathrm{V}_{\mathrm{S}} / 2$. Boldface limits apply at the temperature extreme

| Symbol | Parameter | Conditions | $\begin{gathered} \text { Typ } \\ \text { (Note 5) } \end{gathered}$ | LM6134AI <br> LM6132AI <br> Limit <br> (Note 6) | LM6134BI <br> LM6132BI <br> Limit <br> (Note 6) | Units |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| $\mathrm{V}_{\text {OS }}$ | Input Offset Voltage |  | 1.7 | $\begin{aligned} & 3 \\ & 5 \end{aligned}$ | $\begin{aligned} & 7 \\ & 9 \end{aligned}$ | $\begin{gathered} \mathrm{mV} \\ \max \end{gathered}$ |
| $\mathrm{I}_{\mathrm{B}}$ | Input Bias Current | $\mathrm{OV} \leq \mathrm{V}_{\mathrm{CM}} \leq 24 \mathrm{~V}$ | 125 |  |  | nA |
| los | Input Offset Current |  | 4.8 |  |  | nA |
| $\mathrm{R}_{\text {IN }}$ | Input Resistance |  | 210 |  |  | $\mathrm{M} \Omega$ |
| CMRR | Common Mode Rejection Ratio | $\mathrm{OV} \leq \mathrm{V}_{\mathrm{CM}} \leq 24 \mathrm{~V}$ | 80 |  |  | dB |
| PSRR | Power Supply Rejection Ratio | $2.7 \mathrm{~V} \leq \mathrm{V}_{\mathrm{S}} \leq 24 \mathrm{~V}$ | 82 |  |  | dB |
| $\mathrm{V}_{\mathrm{CM}}$ | Input Common-Mode Voltage Range |  | -0.25 | 0 | 0 | $V$ min |
|  |  |  | 24.25 | 24 | 24 | $\checkmark$ max |
| $A_{V}$ | Large Signal Voltage Gain | $\mathrm{R}_{\mathrm{L}}=10 \mathrm{k}$ | 102 |  |  | $\mathrm{V} / \mathrm{mV}$ |
| $\mathrm{V}_{0}$ | Output Swing | $\mathrm{R}_{\mathrm{L}}=10 \mathrm{k}$ | 0.075 | 0.15 | 0.15 | $\begin{gathered} \mathrm{V} \\ \max \end{gathered}$ |
|  |  |  | 23.86 | 23.8 | 23.8 | $\begin{gathered} \mathrm{V} \\ \mathrm{~min} \end{gathered}$ |
| Is | Supply Current | Per Amplifier | 390 | $\begin{aligned} & 450 \\ & 490 \end{aligned}$ | $\begin{aligned} & 450 \\ & 490 \end{aligned}$ | $\mu \mathrm{A}$ $\max$ |

24V AC Electrical Characteristics Unless otherwise specified, all limits guaranteed for $\mathrm{T}_{\mathrm{J}}=25^{\circ} \mathrm{C}, \mathrm{V}+=$ $24 \mathrm{~V}, \mathrm{~V}^{-}=0 \mathrm{~V}, \mathrm{~V}_{\mathrm{CM}}=\mathrm{V}_{\mathrm{O}}=\mathrm{V}^{+} / 2$ and $\mathrm{R}_{\mathrm{L}}>1 \mathrm{M} \Omega$ to $\mathrm{V}_{\mathrm{S}} / 2$.

| Symbol | Parameter | Conditions | Typ <br> (Note 5) | LM6134AI <br> LM6132AI <br> Limit <br> (Note 6) | LM6134BI <br> LM6132BI <br> Limit <br> (Note 6) | Units |
| :--- | :--- | :--- | :--- | :---: | :---: | :---: |

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but specific performance is not guaranteed. For guaranteed specifications and the test conditions, see the Electrical characteristics. Note 2: Human body model, $1.5 \mathrm{k} \Omega$ in series with 100 pF .
Note 3: Applies to both single-supply and split-supply operation. Continuous short circuit operation at elevated ambient temperature can result in exceeding the maximum allowed junction temperature of $150^{\circ} \mathrm{C}$.
Note 4: The maximum power dissipation is a function of $T_{J(\max )}, \theta_{\mathrm{JA}}$, and $\mathrm{T}_{\mathrm{A}}$. The maximum allowable power dissipation at any ambient temperature is $\mathrm{P}_{\mathrm{D}}=$ $\left(T_{J(\max )}-T_{A}\right) / \theta_{J A}$. All numbers apply for packages soldered directly into a PC board.
Note 5: Typical Values represent the most likely parametric norm.
Note 6: All limits are guaranteed by testing or statistical analysis.


Typical Performance Characteristics $\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}, \mathrm{R}_{\mathrm{L}}=10 \mathrm{k} \Omega$ unless otherwise specified (Continued)


TL/H/12349-15


TL/H/12349-18
Output Voltage vs Sinking Current



TL/H/12349-16
Output Voltage vs Sinking Current


Output Voltage vs Sourcing Current


> Output Voltage vs Sourcing Current


TL/H/12349-17


Output Voltage vs Sourcing Current


Typical Performance Characteristics $\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}, \mathrm{R}_{\mathrm{L}}=10 \mathrm{k} \Omega$ unless otherwise specified (Continued)







supply Voltage (v)
TL/H/12349-31

## LM6132/34 Application Hints

The LM6132 brings a new level of ease of use to opamp system design.
With greater than rail-to-rail input voltage range concern over exceeding the common-mode voltage range is eliminated.
Rail-to-rail output swing provides the maximum possible dynamic range at the output. This is particularly important when operating on low supply voltages.
The high gain-bandwidth with low supply current opens new battery powered applications, where high power consumption, previously reduced battery life to unacceptable levels.
To take advantage of these features, some ideas should be kept in mind.

## ENHANCED SLEW RATE

Unlike most bipolar opamps, the unique phase reversal pre-vention/speed-up circuit in the input stage eliminates phase reversal and allows the slew rate to be very much a function of the input signal amplitude.
Figure 1 shows how excess input signal is routed around the input collector-base junctions directly to the current mirrors. The LM6132/34 input stage converts the input voltage change to a current change. This current change drives the current mirrors through the collectors of Q1-Q2, Q3-Q4 when the input levels are normal.
If the input signal exceeds the slew rate of the input stage and the differential input voltage rises above a diode drop, the excess signal bypasses the normal input transistors, (Q1-Q4), and is routed in correct phase through the two additional transistors, (Q5, Q6), directly into the current mirrors.
This rerouting of excess signal allows the slew-rate to increase by a factor of 10 to 1 or more. (See Figure 2.)
As the overdrive increases, the opamp reacts better than a conventional opamp. Large fast pulses will raise the slewrate to around 25 V to $30 \mathrm{~V} / \mu \mathrm{s}$.

Slew Rate vs Differential $\mathbf{V I N}_{\text {IN }}$ $\mathrm{V}_{\mathrm{S}}= \pm \mathbf{1 2 V}$


FIGURE 2
This effect is most noticeable at higher supply voltages and lower gains where incoming signals are likely to be large. This speed-up action adds stability to the system when driving large capacitive loads.

## DRIVING CAPACITIVE LOADS

Capacitive loads decrease the phase margin of all opamps. This is caused by the output resistance of the amplifier and the load capacitance forming an R-C phase lag network. This can lead to overshoot, ringing and oscillation. Slew rate limiting can also cause additional lag. Most opamps with a fixed maximum slew-rate will lag further and further behind when driving capacitive loads even though the differential input voltage raises. With the LM6132, the lag causes the slew rate to raise. The increased slew-rate keeps the output following the input much better. This effectively reduces phase lag. After the output has caught up with the input, the differential input voltage drops down and the amplifier settles rapidly.


TL/H/12349-36

## LM6132/34 Application Hints

(Continued)
These features allow the LM6132 to drive capacitive loads as large as 500 pF at unity gain and not oscillate. The scope photos (Figure 3 and 4) above show the LM6132 driving a 500 pF load. In Figure 3, the lower trace is with no capacitive load and the upper trace is with a 500 pF load. Here we are operating on $\pm 12 \mathrm{~V}$ supplies with a $20 \mathrm{Vp}-\mathrm{p}$ pulse. Excellent response is obtained with a $\mathrm{C}_{\mathrm{f}}$ of 39 pF . In Figure 4, the supplies have been reduced to $\pm 2.5 \mathrm{~V}$, the pulse is $4 \mathrm{Vp}-\mathrm{p}$ and $\mathrm{C}_{\mathrm{f}}$ is 39 pF . The best value for the compensation capacitor should be established after the board layout is finished because the value is dependent on board stray capacity, the value of the feedback resistor, the closed loop gain and, to some extent, the supply voltage.
Another effect that is common to all opamps is the phase shift caused by the feedback resistor and the input capacitance. This phase shift also reduces phase margin. This effect is taken care of at the same time as the effect of the capacitive load when the capacitor is placed across the feedback resistor.
The circuit shown in Figure 5 was used for these scope photos.


FIGURE 3


FIGURE 4


FIGURE 5
Figure 6 shows a method for compensating for load capacitance $\left(\mathrm{C}_{0}\right)$ effects by adding both an isolation resistor Ro at the output and a feedback capacitor $\mathrm{C}_{\mathrm{F}}$ directly between the output and the inverting input pin. Feedback capacitor $C_{F}$ compensates for the pole introduced by $R_{0}$ and $C_{0}$, minimizing ringing in the output waveform while the feedback resistor $R_{F}$ compensates for dc inaccuracies introduced by $R_{0}$. Depending on the size of the load capacitance, the value of $R_{0}$ is typically chosen to be between $100 \Omega$ to $1 \mathrm{k} \Omega$.


FIGURE 6

## Typical Applications

## 3 OPAMP INSTRUMENTATION AMP WITH RAIL-TORAIL INPUT AND OUTPUT

Using the LM6134, a 3 opamp instrumentation amplifier with rail-to-rail inputs and rail to rail output can be made. These features make these instrumentation amplifiers ideal for single supply systems.
Some manufacturers use a precision voltage divider array of 5 resistors to divide the common-mode voltage to get an input range of rail-to-rail or greater. The problem with this method is that it also divides the signal, so to even get unity gain, the amplifier must be run at high closed loop gains. This raises the noise and drift by the internal gain factor and lowers the input impedance. Any mismatch in these precision resistors reduces the CMR as well. Using the LM6134, all of these problems are eliminated.

In this example, amplifiers $A$ and $B$ act as buffers to the differential stage (Figure 7). These buffers assure that the input impedance is over $100 \mathrm{M} \Omega$ and they eliminate the requirement for precision matched resistors in the input stage. They also assure that the difference amp is driven from a voltage source. This is necessary to maintain the CMR set by the matching of R1-R2 with R3-R4.


FIGURE 7

## FLAT PANEL DISPLAY BUFFERING

Three features of the LM6132/34 make it a superb choice for TFT LCD applications. First, its low current draw ( $360 \mu \mathrm{~A}$ per amplifier @ 5 V ) makes it an ideal choice for battery powered applications such as in laptop computers. Second, since the device operates down to 2.7 V , it is a natural choice for next generation 3V TFT panels. Last, but not least, the large capacitive drive capability of the LM6132 comes in very handy in driving highly capacitive loads that are characteristic of LCD display drivers.
The large capacitive drive capability of the LM6132/34 allows it to be used as buffers for the gamma correction reference voltage inputs of resistor-DAC type column (Source) drivers in TFT LCD panels. This amplifier is also useful for buffering only the center reference voltage input of Capaci-tor-DAC type column (Source) drivers such as the LMC750X series.
Since for VGA and SVGA displays, the buffered voltages must settle within approximately $4 \mu \mathrm{~s}$, the well known technique of using a small isolation resistor in series with the amplifier's output very effectively dampens the ringing at the output.
With its wide supply voltage range of 2.7 V to 24 V ), the LM6132/34 can be used for a diverse range of applications. The system designer is thus able to choose a single device type that serves many sub-circuits in the system, eliminating the need to specify multiple devices in the bill of materials. Along with its sister parts, the LM6142 and LM6152 that have the same wide supply voltage capability, choice of the LM6132 in a design eliminates the need to search for multiple sources for new designs.




## LM6152 Dual and LM6154 Quad High Speed/Low Power 75 MHz GBW Rail-to-Rail I/O Operational Amplifiers

## General Description

Using patent pending circuit topologies, the LM6152/54 provides new levels of speed vs power performance in applications where low voltage supplies or power limitations previously made compromise necessary. With only $1.4 \mathrm{~mA} /$ amplifier supply current, the 75 MHz gain bandwidth of this device supports new portable applications where higher power devices unacceptably drain battery life. The slew rate of the device increases with increasing input differential voltage, thus allowing the device to handle capacitive loads while maintaining large signal amplitude.
The LM6152/54 can be driven by voltages that exceed both power supply rails, thus eliminating concerns about exceeding the common-mode voltage range. The rail-to-rail output swing capability provides the maximum possible dynamic range at the output. This is particularly important when operating on low supply voltages.
Operating on supplies from 2.7 V to over 24 V , the LM6152/54 is excellent for a very wide range of applications, from battery operated systems with large bandwidth requirements to high speed instrumentation.

## Connection Diagrams



Top View

Features At $^{2}=5 \mathrm{~V}$, Typ unless noted
■ Greater than Rail-to-Rail Input CMVR -0.25 V to 5.25 V
■ Rail-to-Rail Output Swing 0.01V to 4.99V

- Wide Gain-Bandwidth: 75 MHz @ 100 kHz
- Slew Rate:

Small signal $5 \mathrm{~V} / \mu \mathrm{s}$
Large signal $45 \mathrm{~V} / \mu \mathrm{s}$
■ Low supply current $1.4 \mathrm{~mA} /$ amplifier

- Wide supply range 2.7 V to 24 V

■ Fast settling time of $1.1 \mu \mathrm{~s}$ for 2 V step (to $0.01 \%$ )

- Gain 107 dB with $\mathrm{R}_{\mathrm{L}}=10 \mathrm{k} \Omega$
- PSRR 91 dB
- CMRR 84 dB


## Applications

- Portable high speed instrumentation
- Signal conditioning amplifiers/ADC buffers
- Barcode scanners

Absolute Maximum Ratings (Note 1)

ESD Tolerance (Note 2)
Differential Input Voltage
Voltage at Input/Output Pin
Supply Voltage ( $\mathrm{V}^{+}-\mathrm{V}^{-}$)
Current at Input Pin
Current at Output Pin (Note 3)
Current at Power Supply Pin
Lead Temperature (soldering, 10 sec )

2500 V
15 V
$\left(V^{+}\right)+0.3 V,\left(V^{-}\right)-0.3 V$ 35 V

$$
\pm 10 \mathrm{~mA}
$$

$$
\pm 25 \mathrm{~mA}
$$

$$
50 \mathrm{~mA}
$$

$\begin{array}{lr}\text { Storage Temperature Range } & -65^{\circ} \mathrm{C} \text { to }+150^{\circ} \mathrm{C} \\ \text { Junction Temperature (Note 4) } & 150^{\circ} \mathrm{C}\end{array}$
Operating Ratings (Note 1)

| Supply Voltage | $2.7 \mathrm{~V} \leq \mathrm{V}_{\mathrm{S}} \leq 24 \mathrm{~V}$ |
| :--- | ---: |
| Junction Temperature Range | $0^{\circ} \mathrm{C} \leq \mathrm{TJ} \leq+70^{\circ} \mathrm{C}$ |
| $\quad$ LM6152, LM6154 |  |
| Thermal Resistance ( $\phi \mathrm{JA}$ ) | $115^{\circ} \mathrm{C} / \mathrm{W}$ |
| N Package, 8-pin Molded DIP | $193^{\circ} \mathrm{C} / \mathrm{W}$ |
| M Package, 8-pin Surface Mount | $81^{\circ} \mathrm{C} / \mathrm{W}$ |
| N Package, 14-pin Molded DIP | $126^{\circ} \mathrm{C} / \mathrm{W}$ |
| M Package, 14-pin Surface Mount |  |

### 5.0V DC Electrical Characteristics

Unless otherwise specified, all limits guaranteed for $\mathrm{T}_{\mathrm{J}}=25^{\circ} \mathrm{C}, \mathrm{V}+=5.0 \mathrm{~V}, \mathrm{~V}^{-}=0 \mathrm{~V}, \mathrm{~V}_{\mathrm{CM}}=\mathrm{V}_{\mathrm{O}}=\mathrm{V}^{+} / 2$ and $\mathrm{R}_{\mathrm{L}}>1 \mathrm{M} \Omega$ to $\mathrm{V}+/ 2$. Boldface limits apply at the temperature extremes.

| Symbol | Parameter | Conditions | Typ (Note 5) | LM6154AC <br> LM6152AC Limit (Note 6) | LM6154BC <br> LM6152BC Limit (Note 6) | Units |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| V ${ }_{\text {OS }}$ | Input Offset Voltage |  | 0.54 | $\begin{aligned} & 2 \\ & 4 \end{aligned}$ | $\begin{aligned} & 5 \\ & 7 \end{aligned}$ | mV <br> max |
| TCV ${ }_{\text {OS }}$ | Input Offset Voltage Average Drift |  | 10 |  |  | $\mu \mathrm{V} /{ }^{\circ} \mathrm{C}$ |
| $\mathrm{I}_{\mathrm{B}}$ | Input Bias Current | $0 \mathrm{~V} \leq \mathrm{V}_{\mathrm{CM}} \leq 5 \mathrm{~V}$ | $\begin{aligned} & 500 \\ & \mathbf{7 5 0} \end{aligned}$ | $\begin{gathered} 980 \\ \mathbf{1 5 0 0} \end{gathered}$ | $\begin{gathered} 980 \\ 1500 \end{gathered}$ | nA max |
| los | Input Offset Current |  | $\begin{aligned} & 32 \\ & 40 \end{aligned}$ | $\begin{aligned} & 100 \\ & 160 \end{aligned}$ | $\begin{aligned} & 100 \\ & 160 \end{aligned}$ | nA max |
| $\mathrm{R}_{\text {IN }}$ | Input Resistance, CM | $0 \mathrm{~V} \leq \mathrm{V}_{\mathrm{CM}} \leq 4 \mathrm{~V}$ | 30 |  |  | $\mathrm{M} \Omega$ |
| CMRR | Common Mode Rejection Ratio | $\mathrm{OV} \leq \mathrm{V}_{\mathrm{CM}} \leq 4 \mathrm{~V}$ | 94 | 70 | 70 | $\begin{gathered} \mathrm{dB} \\ \mathrm{~min} \end{gathered}$ |
|  |  | $0 \mathrm{~V} \leq \mathrm{V}_{\mathrm{CM}} \leq 5 \mathrm{~V}$ | 84 | 60 | 60 |  |
| PSRR | Power Supply Rejection Ratio | $5 \mathrm{~V} \leq \mathrm{V}^{+} \leq 24 \mathrm{~V}$ | 91 | 80 | 80 | $\begin{gathered} \mathrm{dB} \\ \mathrm{~min} \end{gathered}$ |
| $\mathrm{V}_{\mathrm{CM}}$ | Input Common-Mode Voltage Range | Low | -0.25 | 0 | 0 | V |
|  |  | High | 5.25 | 5.0 | 5.0 | V |
| $A_{V}$ | Large Signal Voltage Gain | $\mathrm{R}_{\mathrm{L}}=10 \mathrm{k} \Omega$ | 214 | 50 | 50 | $\begin{gathered} \mathrm{V} / \mathrm{mV} \\ \mathrm{~min} \\ \hline \end{gathered}$ |
| $\mathrm{V}_{\mathrm{O}}$ | Output Swing | $\mathrm{R}_{\mathrm{L}}=100 \mathrm{k} \Omega$ | 0.006 | $\begin{array}{r} 0.02 \\ \mathbf{0 . 0 3} \\ \hline \end{array}$ | $\begin{gathered} 0.02 \\ \mathbf{0 . 0 3} \\ \hline \end{gathered}$ | $\begin{gathered} \mathrm{V} \\ \max \end{gathered}$ |
|  |  |  | 4.992 | $\begin{aligned} & 4.97 \\ & 4.96 \end{aligned}$ | $\begin{aligned} & 4.97 \\ & 4.96 \end{aligned}$ | $\underset{\min }{ }$ |
|  |  | $\mathrm{R}_{\mathrm{L}}=2 \mathrm{k} \Omega$ | 0.04 | $\begin{aligned} & 0.10 \\ & \mathbf{0 . 1 2} \end{aligned}$ | $\begin{aligned} & 0.10 \\ & \mathbf{0 . 1 2} \end{aligned}$ | $\underset{\max }{V}$ |
|  |  |  | 4.89 | $\begin{aligned} & 4.80 \\ & 4.70 \end{aligned}$ | $\begin{aligned} & 4.80 \\ & 4.70 \end{aligned}$ | $\underset{\mathrm{min}}{\mathrm{~V}}$ |
| Isc | Output Short Circuit Current | Sourcing | 6.2 | $\begin{array}{r} 3 \\ \mathbf{2} .5 \\ \hline \end{array}$ | $\begin{array}{r} 3 \\ \mathbf{2 . 5} \\ \hline \end{array}$ | $\begin{aligned} & \mathrm{mA} \\ & \mathrm{~min} \\ & \hline \end{aligned}$ |
|  |  |  |  | $\begin{aligned} & 27 \\ & \mathbf{1 7} \\ & \hline \end{aligned}$ | $\begin{aligned} & 27 \\ & 17 \\ & \hline \end{aligned}$ | mA <br> max |
|  |  | Sinking | 16.9 | $\begin{aligned} & \hline 7 \\ & 5 \end{aligned}$ | $\begin{aligned} & \hline 7 \\ & 5 \end{aligned}$ | $\begin{aligned} & \mathrm{mA} \\ & \mathrm{~min} \end{aligned}$ |
|  |  |  |  | 40 | 40 | mA <br> max |
| Is | Supply Current | Per Amplifier | 1.4 | $\stackrel{2}{2.25}$ | $\begin{gathered} 2 \\ 2.25 \end{gathered}$ | mA <br> max |

### 5.0V AC Electrical Characteristics

Unless otherwise specified, all limits guaranteed for $\mathrm{T}_{\mathrm{J}}=25^{\circ} \mathrm{C}, \mathrm{V}+=5.0 \mathrm{~V}, \mathrm{~V}^{-}=0 \mathrm{~V}, \mathrm{~V}_{\mathrm{CM}}=\mathrm{V}_{\mathrm{O}}=\mathrm{V}^{+} / 2$ and $\mathrm{R}_{\mathrm{L}}>1 \mathrm{M} \Omega$ to $\mathrm{V}^{+} / 2$. Boldface limits apply at the temperature extremes.

| Symbol | Parameter | Conditions | $\begin{gathered} \text { Typ } \\ \text { (Note 5) } \end{gathered}$ | LM6154AC <br> LM6152AC Limit (Note 6) | LM6154BC <br> LM6152BC <br> Limit <br> (Note 6) | Units |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| SR | Slew Rate | $\begin{aligned} & \pm 4 \mathrm{~V} \text { Step @ } \mathrm{V}_{\mathrm{S}}= \pm 6 \mathrm{~V} \\ & \mathrm{R}_{\mathrm{S}}<1 \mathrm{k} \Omega \end{aligned}$ | 30 | $\begin{aligned} & 24 \\ & 15 \end{aligned}$ | $\begin{aligned} & 24 \\ & 15 \\ & \hline \end{aligned}$ | $\begin{gathered} \mathrm{V} / \mu \mathrm{s} \\ \mathrm{~min} \end{gathered}$ |
| GBW | Gain-Bandwidth Product | $\mathrm{f}=100 \mathrm{kHz}$ | 75 |  |  | MHz |
|  | Amp-to-Amp Isolation | $\mathrm{R}_{\mathrm{L}}=10 \mathrm{k} \Omega$ | 125 |  |  | dB |
| $e_{n}$ | Input-Referred Voltage Noise | $\mathrm{f}=1 \mathrm{kHz}$ | 9 |  |  | $\frac{n V}{\sqrt{H z}}$ |
| $\mathrm{i}_{\mathrm{n}}$ | Input-Referred Current Noise | $\mathrm{f}=1 \mathrm{kHz}$ | 0.34 |  |  | $\frac{p A}{\sqrt{H z}}$ |
| T.H.D. | Total Harmonic Distortion | $\mathrm{f}=10 \mathrm{kHz}, \mathrm{R}_{\mathrm{L}}=10 \mathrm{k} \Omega$ | 0.002 |  |  | \% |
| ts | Settling Time | 2V Step to 0.01\% | 1.1 |  |  | $\mu \mathrm{s}$ |

### 2.7V DC Electrical Characteristics

Unless otherwise specified, all limits guaranteed for $\mathrm{T}_{\mathrm{J}}=25^{\circ} \mathrm{C}, \mathrm{V}^{+}=2.7 \mathrm{~V}, \mathrm{~V}^{-}=0 \mathrm{~V}, \mathrm{~V}_{\mathrm{CM}}=\mathrm{V}_{\mathrm{O}}=\mathrm{V}^{+} / 2$ and $\mathrm{R}_{\mathrm{L}}>1 \mathrm{M} \Omega$ to $\mathrm{V}^{+} / 2$. Boldface limits apply at the temperature extremes.

| Symbol | Parameter | Conditions | Typ <br> (Note 5) | LM6154AC <br> LM6152AC <br> Limit <br> (Note 6) | LM6154BC <br> LM6152BC <br> Limit <br> (Note 6) | Units |
| :--- | :--- | :--- | :---: | :---: | :---: | :---: |

### 2.7V AC Electrical Characteristics

Unless otherwise specified, all limits guaranteed for $T_{J}=25^{\circ} \mathrm{C}, \mathrm{V}+=2.7 \mathrm{~V}, \mathrm{~V}^{-}=0 \mathrm{~V}, \mathrm{~V}_{\mathrm{CM}}=\mathrm{V}_{\mathrm{O}}=\mathrm{V}^{+} / 2$ and $\mathrm{R}_{\mathrm{L}}>1 \mathrm{M} \Omega$ to $\mathrm{V}+/ 2$. Boldface limits apply at the temperature extremes.

| Symbol | Parameter | Conditions | Typ <br> (Note 5) | LM6154AC <br> LM6152AC <br> Limit <br> (Note 6) | LM6154BC <br> LM6152BC <br> Limit <br> (Note 6) | Units |
| :--- | :---: | :---: | :---: | :---: | :---: | :---: |
| GBW | Gain-Bandwidth Product | $\mathrm{f}=100 \mathrm{kHz}, \mathrm{R}_{\mathrm{L}}=1 \mathrm{k} \Omega$ | 9 |  |  | MHz |

## 24V DC Electrical Characteristics

Unless otherwise specified, all limits guaranteed for $T_{J}=25^{\circ} \mathrm{C}, \mathrm{V}^{+}=24 \mathrm{~V}, \mathrm{~V}^{-}=0 \mathrm{~V}, \mathrm{~V}_{\mathrm{CM}}=\mathrm{V}_{\mathrm{O}}=\mathrm{V}^{+} / 2$ and $\mathrm{R}_{\mathrm{L}}>1 \mathrm{M} \Omega$ to $\mathrm{V}+/ 2$. Boldface limits apply at the temperature extremes.

| Symbol | Parameter | Conditions | $\begin{gathered} \text { Typ } \\ \text { (Note 5) } \end{gathered}$ | LM6154AC <br> LM6152AC <br> Limit <br> (Note 6) | LM6154BC <br> LM6152BC <br> Limit <br> (Note 6) | Units |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| $\mathrm{V}_{\text {OS }}$ | Input Offset Voltage |  | 0.3 | $\begin{aligned} & 2 \\ & 4 \end{aligned}$ | $\begin{aligned} & 7 \\ & \mathbf{9} \end{aligned}$ | $\begin{gathered} \mathrm{mV} \\ \max \end{gathered}$ |
| TCV ${ }_{\text {OS }}$ | Input Offset Voltage Average Drift |  | 10 |  |  | $\mu \mathrm{V} /{ }^{\circ} \mathrm{C}$ |
| $\mathrm{I}_{\mathrm{B}}$ | Input Bias Current |  | 500 |  |  | nA |
| los | Input Offset Current |  | 32 |  |  | nA |
| $\mathrm{R}_{\text {IN }}$ | Input Resistance, CM | $\mathrm{OV} \leq \mathrm{V}_{\mathrm{CM}} \leq 23 \mathrm{~V}$ | 60 |  |  | Meg $\Omega$ |
| CMRR | Common Mode Rejection Ratio | $\mathrm{OV} \leq \mathrm{V}_{\mathrm{CM}} \leq 23 \mathrm{~V}$ | 94 |  |  | dB |
|  |  | $\mathrm{OV} \leq \mathrm{V}_{\mathrm{CM}} \leq 24 \mathrm{~V}$ | 84 |  |  |  |
| PSRR | Power Supply <br> Rejection Ratio | $\mathrm{OV} \leq \mathrm{V}_{\mathrm{CM}} \leq 24 \mathrm{~V}$ | 95 |  |  |  |
| $\mathrm{V}_{\mathrm{CM}}$ | Input Common-Mode Voltage Range | Low | $-0.25$ | 0 | 0 | V |
|  |  | High | 24.25 | 24 | 24 | V |
| $A_{V}$ | Large Signal Voltage Gain | $\mathrm{R}_{\mathrm{L}}=10 \mathrm{k} \Omega$ | 55 |  |  | $\mathrm{V} / \mathrm{mV}$ |
| $\mathrm{V}_{\mathrm{O}}$ | Output Swing | $\mathrm{R}_{\mathrm{L}}=10 \mathrm{k} \Omega$ | 0.044 | $\begin{gathered} 0.075 \\ \mathbf{0 . 0 9 0} \end{gathered}$ | $\begin{gathered} 0.075 \\ \mathbf{0 . 0 9 0} \end{gathered}$ | $\begin{gathered} \mathrm{V} \\ \max \end{gathered}$ |
|  |  |  | 23.91 | $\begin{gathered} 23.8 \\ \mathbf{2 3 . 7} \end{gathered}$ | $\begin{gathered} 23.8 \\ \mathbf{2 3 . 7} \end{gathered}$ | $\begin{gathered} \mathrm{V} \\ \mathrm{~min} \end{gathered}$ |
| Is | Supply Current | Per Amplifier | 1.6 | $\begin{aligned} & 2.25 \\ & \mathbf{2 . 5 0} \end{aligned}$ | $\begin{aligned} & 2.25 \\ & \mathbf{2 . 5 0} \end{aligned}$ | mA <br> max |

## 24V AC Electrical Characteristics

Unless otherwise specified, all limits guaranteed for $T_{J}=25^{\circ} \mathrm{C}, \mathrm{V}^{+}=24 \mathrm{~V}, \mathrm{~V}^{-}=0 \mathrm{~V}, \mathrm{~V}_{\mathrm{CM}}=\mathrm{V}_{\mathrm{O}}=\mathrm{V}^{+} / 2$ and $\mathrm{R}_{\mathrm{L}}>1 \mathrm{M} \Omega$ to $\mathrm{V}+/ 2$. Boldface limits apply at the temperature extremes.

| Symbol | Parameter | Conditions | Typ <br> (Note 5) | LM6154AC <br> LM6152AC <br> Limit <br> (Note 6) | LM6154BC <br> LM6152BC <br> Limit <br> (Note 6) | Units |
| :--- | :---: | :---: | :---: | :---: | :---: | :---: |
| GBW | Gain-Bandwidth Product | $\mathrm{f}=100 \mathrm{kHz}$ | 80 |  |  | MHz |

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but specific performance is not guaranteed. For guaranteed specifications and the test conditions, see the Electrical Characteristics. Note 2: Human body model, $1.5 \mathrm{k} \Omega$ in series with 100 pF .
Note 3: Applies to both single-supply and split-supply operation. Continuous short circuit operation at elevated ambient temperature can result in exceeding the maximum allowed junction temperature of $150^{\circ} \mathrm{C}$.
Note 4: The maximum power dissipation is a function of $T_{J(\max )}, \phi_{J A}$, and $T_{A}$. The maximum allowable power dissipation at any ambient temperature is $\mathrm{P}_{\mathrm{D}}=$ $\left(T_{J(\max )}-T_{A}\right) / \phi_{J A}$. All numbers apply for packages soldered directly into a PC board.
Note 5: Typical values represented the most likely parametric norm.
Note 6: All limits are guaranteed by testing or statistical analysis.

Typical Performance Characteristics $\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}, \mathrm{R}_{\mathrm{L}}=10 \mathrm{k} \Omega$, unless otherwise specified











## Typical Performance Characteristics (Continued)

Total Harmonic Distortion vs Frequency<br><br>TL/H/12507-30

## Application Information

The LM6152/6154 is ideally suited for operation with about $10 \mathrm{k} \Omega$ (Feedback Resistor, $\mathrm{R}_{\mathrm{F}}$ ) between the output and the negative input terminal.
With $R_{F}$ set to this value, for most applications requiring a closed loop gain of 10 or less, an additional small compensation capacitor ( $\mathrm{C}_{\mathrm{F}}$ ) (see Figure 1) is recommended across $\mathrm{R}_{\mathrm{F}}$ in order to achieve a reasonable overshoot (10\%) at the output by compensating for stray capacitance across the inputs.
The optimum value for $\mathrm{C}_{\mathrm{F}}$ can best be established experimentally with a trimmer cap in place since its value is dependant on the supply voltage, output driving load, and the operating gain. Below, some typical values used in an inverting configuration and driving a $10 \mathrm{k} \Omega$ load have been tabulated for reference:

TABLE I. Typical BW ( -3 dB ) at Various Supply Voltages and Gains

| $\mathbf{V}_{\mathbf{S}}$ <br> Volts | Gain | $\mathbf{C}_{\mathbf{F}}$ <br> $\mathbf{p F}$ | $\mathbf{B W} \mathbf{( - 3 \mathbf { d B } )}$ <br> $\mathbf{M H z}$ |
| :---: | :---: | :---: | :---: |
| 3 | -1 | 5.6 | 4 |
|  | -10 | 6.8 | 1.97 |
|  | -100 | None | 0.797 |
| 24 | -1 | 2.2 | 6.6 |
|  | -10 | 4.7 | 2.2 |
|  | -100 | None | 0.962 |

In the non-inverting configuration, the LM6152/6154 can be used for closed loop gains of +2 and above. In this case, also, the compensation capacitor ( $\mathrm{C}_{\mathrm{F}}$ ) is recommended across $R_{F}(=10 \mathrm{k} \Omega)$ for gains of 10 or less.


TL/H/12507-29
FIGURE 1. Typical Inverting Gain Circuit $\mathbf{A}_{\mathbf{V}}=\mathbf{- 1}$

Because of the unique structure of this amplifier, when used at low closed loop gains, the realizable BW will be much less than the GBW product would suggest.
The LM6152/6154 brings a new level of ease of use to opamp system design.
The greater than rail-to-rail input voltage range eliminates concern over exceeding the common-mode voltage range.
The rail-to-rail output swing provides the maximum possible dynamic range at the output. This is particularly important when operating on low supply voltages.
The high gain-bandwidth with low supply current opens new battery powered applications where higher power consumption previously reduced battery life to unacceptable levels.
The ability to drive large capacitive loads without oscillating functionally removes this common problem.
To take advantage of these features, some ideas should be kept in mind.
With the LM6152/6154, capacitive loads do not lead to oscillations, in all but the most extreme conditions, but they will result in reduced bandwidth. They also cause increased settling time.

Unlike most bipolar opamps, the unique phase reversal pre-vention/speed-up circuit in the input stage, causes the slew rate to be very much a function of the input pulse amplitude. This results in a 10 to 1 increase in slew rate when the differential input signal increases. Large fast pulses will raise the slew-rate to more than $30 \mathrm{~V} / \mu \mathrm{s}$.


TL/H/12507-20

## FIGURE 2. Slew Rate vs $\mathbf{V}_{\text {diff }}$

The speed-up action adds stability to the system when driving large capacitive loads.
A conventional opamp exhibits a fixed maximum slew-rate even though the differential input voltage rises due to the lagging output voltage. In the LM6152/6154, increasing lag causes the differential input voltage to increase but as it does, the increased slew-rate keeps the output following the input much better. This effectively reduces phase lag. As a result, the LM6152/6154 can drive capacitive loads as large as 470 pF at gain of 2 and above, and not oscillate.
Capacitive loads decrease the phase margin of all opamps. This can lead to overshoot, ringing and oscillation. This is caused by the output resistance of the amplifier and the load capacitance forming an R-C phase shift network. The LM6152/54 senses this phase shift and partly compensates for this effect.


Physical Dimensions inches (millimeters) unless otherwise noted (Continued)

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)

$\frac{0.092}{(2.337)}$ DIA $\frac{0.030}{(0.762)}$ MAX $\begin{aligned} & \text { DEPTH } \\ & \text { OPTION } 1\end{aligned}$
OPS

optow 02

14-Lead ( 0.300 " Wide) Molded Dual-In-Line Package
Order Number LM6154ACN or LM6154BCN
NS Package Number N14A

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| :---: | :---: | :---: | :---: |



Absolute Maximum Ratings (Note 1)
If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.
ESD Tolerance (Note 2)
2500V
Differential Input Voltage
15 V
Voltage at Input/Output Pin
$\left(V^{+}\right)+0.3 V,\left(V^{-}\right)-0.3 V$
Supply Voltage ( $\mathrm{V}^{+}-\mathrm{V}^{-}$)
Current at Input Pin
Current at Output Pin (Note 3)
Current at Power Supply Pin
25 mA
5.0V DC Electrical Characteristics Unless otherwise specified, all limits guaranteed for $\mathrm{T}_{\mathrm{J}}=25^{\circ} \mathrm{C}, \mathrm{V}+=$ $5.0 \mathrm{~V}, \mathrm{~V}^{-}=0 \mathrm{~V}, \mathrm{~V}_{\mathrm{CM}}=\mathrm{V}_{\mathrm{O}}=\mathrm{V}^{+} / 2$ and $\mathrm{R}_{\mathrm{L}}>1 \mathrm{M} \Omega$ to $\mathrm{V}+/ 2$. Boldface limits apply at the temperature extremes

| Symbol | Parameter | Conditions | Typ (Note 5) | LM7301 <br> Limit <br> (Note 6) | Units |
| :---: | :---: | :---: | :---: | :---: | :---: |
| $\mathrm{V}_{\text {OS }}$ | Input Offset Voltage |  | 0.03 | $\begin{aligned} & 6 \\ & 8 \end{aligned}$ | $\begin{gathered} m V \\ \max \end{gathered}$ |
| TCV ${ }_{\text {OS }}$ | Input Offset Voltage Average Drift |  | 2 |  | $\mu \mathrm{V} /{ }^{\circ} \mathrm{C}$ |
| $\mathrm{I}_{\mathrm{B}}$ | Input Bias Current | $\mathrm{V}_{\mathrm{CM}}=0 \mathrm{~V}$ | 90 | $\begin{aligned} & 200 \\ & 250 \end{aligned}$ | nA max |
|  |  | $\mathrm{V}_{\mathrm{CM}}=5 \mathrm{~V}$ | -40 | $\begin{aligned} & -75 \\ & -\mathbf{8 5} \end{aligned}$ | $\begin{gathered} \mathrm{nA} \\ \mathrm{~min} \end{gathered}$ |
| los | Input Offset Current | $\mathrm{V}_{\mathrm{CM}}=0 \mathrm{~V}$ | 0.7 | $\begin{array}{r} 70 \\ \mathbf{8 0} \end{array}$ | $\begin{gathered} \mathrm{nA} \\ \mathrm{max} \end{gathered}$ |
|  |  | $\mathrm{V}_{\mathrm{CM}}=5 \mathrm{~V}$ | 0.7 | $\begin{aligned} & 55 \\ & 65 \end{aligned}$ |  |
| $\mathrm{R}_{\text {IN }}$ | Input Resistance, CM | $0 \mathrm{~V} \leq \mathrm{V}_{\mathrm{CM}} \leq 5 \mathrm{~V}$ | 39 |  | $\mathrm{M} \Omega$ |
| CMRR | Common Mode Rejection Ratio | $0 \mathrm{~V} \leq \mathrm{V}_{\mathrm{CM}} \leq 5 \mathrm{~V}$ | 88 | $\begin{aligned} & 70 \\ & 67 \end{aligned}$ | $\begin{gathered} \mathrm{dB} \\ \mathrm{~min} \end{gathered}$ |
|  |  | $0 \mathrm{~V} \leq \mathrm{V}_{\mathrm{CM}} \leq 3.5 \mathrm{~V}$ | 93 |  |  |
| PSRR | Power Supply Rejection Ratio | $2.2 \mathrm{~V} \leq \mathrm{V}^{+} \leq 30 \mathrm{~V}$ | 104 | $\begin{aligned} & 87 \\ & 84 \end{aligned}$ |  |
| $\mathrm{V}_{\mathrm{CM}}$ | Input Common-Mode Voltage Range | CMRR $\geq 65 \mathrm{~dB}$ | 5.1 |  | V |
|  |  |  | -0.1 |  | V |
| $A_{V}$ | Large Signal Voltage Gain | $\begin{aligned} & \mathrm{R}_{\mathrm{L}}=10 \mathrm{k} \Omega \\ & \mathrm{~V}_{\mathrm{O}}=4.0 \mathrm{~V}_{\mathrm{PP}} \end{aligned}$ | 71 | $\begin{aligned} & 14 \\ & \mathbf{1 0} \end{aligned}$ | $\mathrm{V} / \mathrm{mV}$ min |
| $\mathrm{V}_{0}$ | Output Swing | $\mathrm{R}_{\mathrm{L}}=10 \mathrm{k} \Omega$ | 0.07 | $\begin{gathered} 0.12 \\ \mathbf{0 . 1 5} \\ \hline \end{gathered}$ | $\begin{gathered} \text { V } \\ \max \end{gathered}$ |
|  |  |  | 4.93 | $\begin{aligned} & 4.88 \\ & \mathbf{4 . 8 5} \end{aligned}$ | $\begin{gathered} \mathrm{V} \\ \mathrm{~min} \end{gathered}$ |
|  |  | $\mathrm{R}_{\mathrm{L}}=2 \mathrm{k} \Omega$ | 0.14 | $\begin{aligned} & 0.20 \\ & \mathbf{0 . 2 2} \end{aligned}$ | $\begin{gathered} V \\ \max \end{gathered}$ |
|  |  |  | 4.87 | $\begin{array}{r} 4.80 \\ \mathbf{4 . 7 8} \\ \hline \end{array}$ | $\begin{gathered} \mathrm{V} \\ \mathrm{~min} \end{gathered}$ |
| Isc | Output Short Circuit Current | Sourcing | 11.0 | $\begin{array}{r} 8.0 \\ \mathbf{5 . 5} \\ \hline \end{array}$ | mA <br> min |
|  |  | Sinking | 9.5 | $\begin{array}{r} 6.0 \\ \mathbf{5 . 0} \\ \hline \end{array}$ | mA <br> min |
| Is | Supply Current |  | 0.60 | $\begin{gathered} 1.10 \\ \mathbf{1 . 2 4} \end{gathered}$ | mA <br> max |


| AC Electrical Characteristics$\mathrm{T}_{\mathrm{J}}=25^{\circ} \mathrm{C}, \mathrm{~V}^{+}=2.2 \mathrm{~V} \text { to } 30 \mathrm{~V}, \mathrm{~V}^{-}=0 \mathrm{~V}, \mathrm{~V}_{\mathrm{CM}}=\mathrm{V}_{\mathrm{O}}=\mathrm{V}+/ 2 \text { and } \mathrm{R}_{\mathrm{L}}>1 \mathrm{M} \Omega \text { to } \mathrm{V}+/ 2$ |  |  |  |  |
| :---: | :---: | :---: | :---: | :---: |
| Symbol | Parameter | Conditions | Typ (Note 5) | Units |
| SR | Slew Rate | $\pm 4 \mathrm{~V}$ Step @ $\mathrm{V}_{\mathrm{S}} \pm 6 \mathrm{~V}$ | 1.25 | $\mathrm{V} / \mu \mathrm{s}$ |
| GBW | Gain-Bandwidth Product | $\mathrm{f}=100 \mathrm{kHz}, \mathrm{R}_{\mathrm{L}}=10 \mathrm{k} \Omega$ | 4 | MHz |
| $e_{n}$ | Input-Referred Voltage Noise | $\mathrm{f}=1 \mathrm{kHz}$ | 36 | $\frac{n \mathrm{~V}}{\sqrt{\mathrm{~Hz}}}$ |
| $\mathrm{i}_{\mathrm{n}}$ | Input-Referred Current Noise | $\mathrm{f}=1 \mathrm{kHz}$ | 0.24 | $\frac{\mathrm{pA}}{\sqrt{\mathrm{Hz}}}$ |
| T.H.D. | Total Harmonic Distortion | $\mathrm{f}=10 \mathrm{kHz}$ | 0.006 | \% |


| 2.2V DC Electrical Characteristics Unless otherwise specified, all limits guaranteed for $\mathrm{T}_{\mathrm{J}}=25^{\circ} \mathrm{C}, \mathrm{V}+=$ $2.2 \mathrm{~V}, \mathrm{~V}^{-}=0 \mathrm{~V}, \mathrm{~V}_{\mathrm{CM}}=\mathrm{V}_{\mathrm{O}}=\mathrm{V}^{+} / 2$ and $\mathrm{R}_{\mathrm{L}}>1 \mathrm{M} \Omega$ to $\mathrm{V}^{+} / 2$. Boldface limits apply at the temperature extremes |  |  |  |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: |
| Symbol | Parameter | Conditions |  | LM7301 <br> Limit <br> (Note 6) | Units |
| $\mathrm{V}_{\text {OS }}$ | Input Offset Voltage |  | 0.04 | $\begin{aligned} & 6 \\ & 8 \end{aligned}$ | $\begin{gathered} \mathrm{mV} \\ \max \end{gathered}$ |
| TCV ${ }_{\text {OS }}$ | Input Offset Voltage Average Drift |  | 2 |  | $\mu \mathrm{V} /{ }^{\circ} \mathrm{C}$ |
| $\mathrm{I}_{\mathrm{B}}$ | Input Bias Current | $\mathrm{V}_{\mathrm{CM}}=0 \mathrm{~V}$ | 89 | $\begin{aligned} & 200 \\ & 250 \end{aligned}$ | $\begin{gathered} \mathrm{nA} \\ \mathrm{max} \end{gathered}$ |
|  |  | $\mathrm{V}_{\mathrm{CM}}=2.2 \mathrm{~V}$ | -35 | $\begin{array}{r} -75 \\ -\mathbf{8 5} \end{array}$ | nA <br> min |
| los | Input Offset Current | $\mathrm{V}_{\mathrm{CM}}=0 \mathrm{~V}$ | 0.8 | $\begin{aligned} & 70 \\ & \mathbf{8 0} \end{aligned}$ | $\begin{gathered} \mathrm{nA} \\ \mathrm{max} \end{gathered}$ |
|  |  | $\mathrm{V}_{\mathrm{CM}}=2.2 \mathrm{~V}$ | 0.4 | $\begin{aligned} & 55 \\ & 65 \end{aligned}$ |  |
| $\mathrm{R}_{\text {IN }}$ | Input Resistance | $\mathrm{OV} \leq \mathrm{V}_{\mathrm{CM}} \leq 2.2 \mathrm{~V}$ | 18 |  | $\mathrm{M} \Omega$ |
| CMRR | Common Mode Rejection Ratio | $\mathrm{OV} \leq \mathrm{V}_{\mathrm{CM}} \leq 2.2 \mathrm{~V}$ | 82 | $\begin{aligned} & 60 \\ & 56 \end{aligned}$ | $\begin{gathered} \mathrm{dB} \\ \mathrm{~min} \end{gathered}$ |
| PSRR | Power Supply Rejection Ratio | $2.2 \mathrm{~V} \leq \mathrm{V}^{+} \leq 30 \mathrm{~V}$ | 104 | $\begin{aligned} & 87 \\ & \mathbf{8 4} \end{aligned}$ |  |
| $\mathrm{V}_{\mathrm{CM}}$ | Input Common-Mode Voltage Range | CMRR > 60 dB | 2.3 |  | V |
|  |  |  | -0.1 |  | V |
| $A_{V}$ | Large Signal Voltage Gain | $\begin{aligned} & \mathrm{R}_{\mathrm{L}}=10 \mathrm{k} \Omega \\ & \mathrm{~V}_{\mathrm{O}}=1.6 \mathrm{~V}_{\mathrm{PP}} \end{aligned}$ | 46 | $\begin{array}{r} 6.5 \\ \mathbf{5 . 4} \\ \hline \end{array}$ | $\begin{gathered} \mathrm{V} / \mathrm{mV} \\ \mathrm{~min} \end{gathered}$ |
| $\mathrm{V}_{0}$ | Output Swing | $\mathrm{R}_{\mathrm{L}}=10 \mathrm{k} \Omega$ | 0.05 | $\begin{gathered} 0.08 \\ \mathbf{0 . 1 0} \\ \hline \end{gathered}$ | $\begin{gathered} \text { V } \\ \max \end{gathered}$ |
|  |  |  | 2.15 | $\begin{array}{r} 2.10 \\ \mathbf{2 . 0 0} \\ \hline \end{array}$ | $\begin{gathered} \mathrm{V} \\ \mathrm{~min} \end{gathered}$ |
|  |  | $R_{L}=2 \mathrm{k} \Omega$ | 0.09 | $\begin{gathered} 0.13 \\ \mathbf{0 . 1 4} \end{gathered}$ | $\begin{gathered} \mathrm{V} \\ \max \end{gathered}$ |
|  |  |  | 2.10 | $\begin{aligned} & 2.07 \\ & \mathbf{2 . 0 0} \end{aligned}$ | $\begin{gathered} \mathrm{V} \\ \mathrm{~min} \end{gathered}$ |
| ISC | Output Short Circuit Current | Sourcing | 10.9 | $\begin{array}{r} 8.0 \\ \mathbf{5 . 5} \\ \hline \end{array}$ | $\begin{aligned} & \mathrm{mA} \\ & \mathrm{~min} \end{aligned}$ |
|  |  | Sinking | 7.7 | $\begin{array}{r} 6.0 \\ \mathbf{5 . 0} \\ \hline \end{array}$ | $\begin{aligned} & \mathrm{mA} \\ & \mathrm{~min} \end{aligned}$ |
| Is | Supply Current |  | 0.57 | $\begin{gathered} 0.97 \\ \mathbf{1 . 2 4} \end{gathered}$ | mA max |

30V DC Electrical Characteristics Unless otherwise specified, all limits guaranteed for $\mathrm{T}_{J}=25^{\circ} \mathrm{C}, \mathrm{V}+=$ $30 \mathrm{~V}, \mathrm{~V}^{-}=0 \mathrm{~V}, \mathrm{~V}_{\mathrm{CM}}=\mathrm{V}_{\mathrm{O}}=\mathrm{V}^{+} / 2$ and $\mathrm{R}_{\mathrm{L}}>1 \mathrm{M} \Omega$ to $\mathrm{V}^{+} / 2$. Boldface limits apply at the temperature extremes

| Symbol | Parameter | Conditions | Typ (Note 5) | $\begin{aligned} & \text { LM7301 } \\ & \text { Limit } \\ & \text { (Note 6) } \end{aligned}$ | Units |
| :---: | :---: | :---: | :---: | :---: | :---: |
| Vos | Input Offset Voltage |  | 0.04 | $\begin{aligned} & 6 \\ & 8 \end{aligned}$ | $\begin{aligned} & \mathrm{mV} \\ & \max \end{aligned}$ |
| TCV ${ }_{\text {OS }}$ | Input Offset Voltage Average Drift |  | 2 |  | $\mu \mathrm{V} /{ }^{\circ} \mathrm{C}$ |
| $\mathrm{I}_{\mathrm{B}}$ | Input Bias Current | $\mathrm{V}_{\mathrm{CM}}=0 \mathrm{~V}$ | 103 | $\begin{gathered} 300 \\ \mathbf{5 0 0} \end{gathered}$ | $\begin{gathered} \mathrm{nA} \\ \max \end{gathered}$ |
|  |  | $\mathrm{V}_{\mathrm{CM}}=30 \mathrm{~V}$ | -50 | $\begin{aligned} & -100 \\ & -200 \end{aligned}$ | $\begin{aligned} & \mathrm{nA} \\ & \mathrm{~min} \end{aligned}$ |
| los | Input Offset Current | $\mathrm{V}_{\mathrm{CM}}=0 \mathrm{~V}$ | 1.2 | $\begin{gathered} 90 \\ 190 \end{gathered}$ | $\begin{gathered} \mathrm{nA} \\ \max \end{gathered}$ |
|  |  | $\mathrm{V}_{\mathrm{CM}}=30 \mathrm{~V}$ | 0.5 | $\begin{gathered} 65 \\ \mathbf{1 3 5} \end{gathered}$ | $\begin{gathered} \mathrm{nA} \\ \max \end{gathered}$ |
| RIN | Input Resistance | $\mathrm{OV} \leq \mathrm{V}_{\mathrm{CM}} \leq 30 \mathrm{~V}$ | 200 |  | M $\Omega$ |
| CMRR | Common Mode Rejection Ratio | $\mathrm{OV} \leq \mathrm{V}_{\text {CM }} \leq 30 \mathrm{~V}$ | 104 | $\begin{array}{r} 80 \\ \mathbf{7 8} \\ \hline \end{array}$ | $\begin{gathered} \mathrm{dB} \\ \mathrm{~min} \end{gathered}$ |
|  |  | $\mathrm{VV} \leq \mathrm{V}_{\mathrm{CM}} \leq 27 \mathrm{~V}$ | 115 | $\begin{aligned} & 90 \\ & \mathbf{8 8} \end{aligned}$ |  |
| PSRR | Power Supply Rejection Ratio | $2.2 \mathrm{~V} \leq \mathrm{V}^{+} \leq 30 \mathrm{~V}$ | 104 | $\begin{array}{r} 87 \\ \mathbf{8 4} \\ \hline \end{array}$ |  |
| $\mathrm{V}_{\text {CM }}$ | Input Common-Mode Voltage Range | CMRR > 80 dB | 30.1 |  | v |
|  |  |  | -0.1 |  | v |
| $A_{V}$ | Large Signal Voltage Gain | $\begin{aligned} & \mathrm{R}_{\mathrm{L}}=10 \mathrm{k} \Omega \\ & \mathrm{~V}_{\mathrm{O}}=28 \mathrm{~V}_{\mathrm{PP}} \\ & \hline \end{aligned}$ | 105 | $\begin{array}{r} 30 \\ \mathbf{2 0} \\ \hline \end{array}$ | $\begin{gathered} \mathrm{V} / \mathrm{mV} \\ \mathrm{~min} \\ \hline \end{gathered}$ |
| $\mathrm{V}_{\text {O }}$ | Output Swing | $\mathrm{R}_{\mathrm{L}}=10 \mathrm{k} \Omega$ | 0.16 | $\begin{gathered} 0.275 \\ \mathbf{0 . 3 7 5} \end{gathered}$ | $\checkmark$ max |
|  |  |  | 29.8 | $\begin{gathered} 29.75 \\ \mathbf{2 8 . 6 5} \end{gathered}$ | $\checkmark$ min |
| Isc | Output Short Circuit Current | Sourcing (Note 4) | 11.7 | $\begin{aligned} & 8.8 \\ & 6.5 \\ & \hline \end{aligned}$ | $\begin{aligned} & \mathrm{mA} \\ & \mathrm{~min} \\ & \hline \end{aligned}$ |
|  |  | Sinking (Note 4) | 11.5 | $\begin{aligned} & 8.2 \\ & 6.0 \\ & \hline \end{aligned}$ | $\begin{aligned} & \mathrm{mAA} \\ & \mathrm{~min} \end{aligned}$ |
| Is | Supply Current |  | 0.72 | $\begin{aligned} & 1.30 \\ & \mathbf{1 . 3 5} \\ & \hline \end{aligned}$ | $\begin{gathered} \mathrm{mA} \\ \max \end{gathered}$ |

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but specific performance is not guaranteed. For guaranteed specifications and the test conditions, see the Electrical Characteristics.
Note 2: Human body model, $1.5 \mathrm{k} \Omega$ in series with 100 pF .
Note 3: Applies to both single-supply and split-supply operation. Continuous short circuit operation at elevated ambient temperature can result in exceeding the maximum allowed junction temperature of $150^{\circ} \mathrm{C}$.
Note 4: The maximum power dissipation is a function of $T_{J(\max )}, \theta_{J A}$, and $T_{A}$. The maximum allowable power dissipation at any ambient temperature is $P_{D}=$ $\left(T_{J(\max )}-T_{A}\right) / \Theta_{J A}$. All numbers apply for packages soldered directly into a PC board.
Note 5: Typical Values represent the most likely parametric norm.
Note 6: All limits are guaranteed by testing or statistical analysis.


## Typical Performance Characteristics $T_{A}=25^{\circ} \mathrm{C}, \mathrm{R}_{\mathrm{L}}=1 \mathrm{M} \Omega$ unless otherwise specified (Continued)






TL/H/12842-25



TL/H/12842-26


TL/H/12842-14


Gain and Phase,
2.7V Supply


## Applications Information

## general information

Low supply current and wide bandwidth, greater than rail-torail input range, full rail-to-rail output, good capacitive load driving ability, wide supply voltage and low distortion all make the LM7301 ideal for many diverse applications.
The high common-mode rejection ratio and full rail-to-rail input range provides precision performance when operated in noninverting applications where the common-mode error is added directly to the other system errors.

## CAPACITIVE LOAD DRIVING

The LM7301 has the ability to drive large capacitive loads. For example, 1000 pF only reduces the phase margin to about 25 degrees.

## TRANSIENT RESPONSE

The LM7301 offers a very clean, well-behaved transient response. Figures 1 through 6 show the response when operated at gains of +1 and -1 when handling both small and large signals. The large phase margin, typically 70 to 80 degrees, assures clean and symmetrical response. In the large signal scope photos, Figures 1 and 4, the input signal is set to 4.8 V . Note that the output goes to within 100 mV of the supplies cleanly and without overshoot. In the small signal samples, the response is clean, with only slight overshoot when used as a follower. Figures 3 and 6 are the circuits used to make these photos.


TL/H/12842-16
FIGURE 1


TL/H/12842-17
FIGURE 2


TL/H/12842-18
FIGURE 3


FIGURE 4


TL/H/12842-20 FIGURE 5


FIGURE 6

## POWER DISSIPATION

Although the LM7301 has internal output current limiting, shorting the output to ground when operating on a +30 V power supply will cause the opamp to dissipate about 350 mW . This is a worst-case example. In the SO-8 package, this will cause a temperature rise of $58^{\circ} \mathrm{C}$. In the SOT23-5 package, the higher thermal resistance will cause a calculated rise of $113^{\circ} \mathrm{C}$. This can raise the junction temperature to above the absolute maximum temperature of $150^{\circ} \mathrm{C}$.
Operating from split supplies greatly reduces the power dissipated when the output is shorted. Operating on $\pm 15 \mathrm{~V}$ supplies can only cause a temperature rise of $29^{\circ} \mathrm{C}$ in the SO-8 and $57^{\circ} \mathrm{C}$ in the SOT23-5 package, assuming the short is to ground.

## SPICE Macromodel

A SPICE macromodel for this and many other National Semiconductor operational amplifiers is available, at no charge, from the NSC Customer Support Center at 800-272-9959 or on the World Wide Web at http://www.national.com/models.

## Applications Information

## WIDE SUPPLY RANGE

The high power-supply rejection ratio (PSRR) and commonmode rejection ratio (CMRR) provide precision performance when operated on battery or other unregulated supplies. This advantage is further enhanced by the very wide supply range (2.2V-30V, guaranteed) offered by the LM7301. In situations where highly variable or unregulated supplies are present, the excellent PSRR and wide supply range of the LM7301 benefit the system designer with continued precision performance, even in such adverse supply conditions.

## SPECIFIC ADVANTAGES OF SOT23-5 (TinyPak)

The obvious advantage of the SOT23-5, TinyPak, is that it can save board space, a critical aspect of any portable or miniaturized system design. The need to decrease overall system size is inherent in any handheld, portable, or lightweight system application.
Furthermore, the low profile can help in height limited designs, such as consumer hand-held remote controls, subnotebook computers, and PCMCIA cards.
An additional advantage of the tiny package is that it allows better system performance due to ease of package placement. Because the tiny package is so small, it can fit on the board right where the opamp needs to be placed for optimal performance, unconstrained by the usual space limitations. This optimal placement of the tiny package allows for many system enhancements, not easily achieved with the constraints of a larger package. For example, problems such as system noise due to undesired pickup of digital signals can be easily reduced or mitigated. This pick-up problem is often caused by long wires in the board layout going to or from an opamp. By placing the tiny package closer to the signal source and allowing the LM7301 output to drive the long wire, the signal becomes less sensitive to such pick-up. An overall reduction of system noise results.
Often times system designers try to save space by using dual or quad opamps in their board layouts. This causes a complicated board layout due to the requirement of routing several signals to and from the same place on the board. Using the tiny opamp eliminates this problem.
Additional space savings parts are available in tiny packages from National Semiconductor, including low power amplifiers, precision voltage references, and voltage regulators.

## LOW DISTORTION, HIGH OUTPUT DRIVE CAPABILITY

The LM7301 offers superior low-distortion performance, with a total-harmonic-distortion-plus-noise of $0.06 \%$ at $\mathrm{f}=10 \mathrm{kHz}$. The advantage offered by the LM7301 is its low distortion levels, even at high output current and low load resistance.

## Typical Applications

## HANDHELD REMOTE CONTROLS

The LM7301 offers outstanding specifications for applications requiring good speed/power trade-off. In applications such as remote control operation, where high bandwidth and low power consumption are needed. The LM7301 performance can easily meet these requirements.

## OPTICAL LINE ISOLATION FOR MODEMS

The combination of the low distortion and good load driving capabilities of the LM7301 make it an excellent choice for driving opto-coupler circuits to achieve line isolation for modems. This technique prevents telephone line noise from coupling onto the modem signal. Superior isolation is achieved by coupling the signal optically from the computer modem to the telephone lines; however, this also requires a low distortion at relatively high currents. Due to its low distortion at high output drive currents, the LM7301 fulfills this need, in this and in other telecom applications.

## REMOTE MICROPHONE IN <br> PERSONAL COMPUTERS

Remote microphones in Personal Computers often utilize a microphone at the top of the monitor which must drive a long cable in a high noise environment. One method often used to reduce the nose is to lower the signal impedance, which reduces the noise pickup. In this configuration, the amplifier usually requires $30 \mathrm{db}-40 \mathrm{db}$ of gain, at bandwidths higher than most low-power CMOS parts can achieve. The LM7301 offers the tiny package, higher bandwidths, and greater output drive capability than other rail-torail input/output parts can provide for this application.


Physical Dimensions inches (millimeters) unless otherwise noted


Physical Dimensions inches (millimeters) unless othervise noted


8-Pin Small Outline Package
Order Number LM7301IMX
NS Package Number M08A

## LIFE SUPPORT POLICY

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| :---: | :---: | :---: | :---: |

## CMOS Amplifiers and Comparators

- LMC272
- LMC6035/6
- LMC6572/4
- LMC6582/4
- LMC6681/2/4
- LMC6953
- LMC7215

Dual, Low Cost RR Output OpAmp
Dual/Quad Low Power 2.7V Single Supply Op Amp
Dual/Quad LV OpAmp in Tiny Package
Dual/Quad LV RR I/O OpAmp
Single/Dual/Quad LV RR I/O
OpAmp with Powerdown
PCI Local Bus Power Supervisor
Micro-Power, RR Comparator with Open-Drain/Push-Pull Outputs and TinyPak Package


| Absolute Maximum Ratings (Note 1 ) |  |
| :--- | ---: |
| If Military/Aerospace specified devices are required, |  |
| please contact the National Semiconductor Sales |  |
| Office/Distributors for availability and specifications. |  |
| ESD Tolerance (Note 2) | 2 kV |
| Differential Input Voltage | $\pm$ Supply Voltages |
| Voltage at Input/Output Pin | $(\mathrm{V}+)+0.3 \mathrm{~V},(\mathrm{~V}-)^{-}-0.3 \mathrm{~V}$ |
| Supply Voltage $(\mathrm{V}+-\mathrm{V}-)$ : | 16 V |
| Current at Input Pin (Note 10) | $\pm 5 \mathrm{~mA}$ |
| Current at Output Pin (Notes 3,7$)$ | $\pm 30 \mathrm{~mA}$ |
| Lead Temperature (soldering, 10 sec.) | $260^{\circ} \mathrm{C}$ |
| Storage Temp. Range | $-65^{\circ} \mathrm{C}$ to $+150^{\circ} \mathrm{C}$ |
| Junction Temperature (Note 4) | $150^{\circ} \mathrm{C}$ |

Operating Ratings (Note 1)

| Supply Voltage | $2.5 \mathrm{~V} \leq \mathrm{V}_{\mathrm{S}} \leq 15 \mathrm{~V}$ |
| :--- | ---: |
| Junction Temperature Range | $0^{\circ} \mathrm{C} \leq \mathrm{T}_{\mathrm{J}} \leq+70^{\circ} \mathrm{C}$ |
| $\quad$ LMC272C |  |
| Thermal Resistance $\left(\theta_{\mathrm{JA}}\right)$ | $115^{\circ} \mathrm{C} / \mathrm{W}$ |
| N Package, 8-pin Molded DIP | $177^{\circ} \mathrm{C} / \mathrm{W}$ |
| M Package, 8-pin Surface Mount | $235^{\circ} \mathrm{C} / \mathrm{W}$ |

2.7V DC Electrical Characteristics Unless otherwise specified, all limits guaranteed for $\mathrm{T}_{\mathrm{J}}=25^{\circ} \mathrm{C}, \mathrm{V}+=$ $2.7 \mathrm{~V}, \mathrm{~V}^{-}=0 \mathrm{~V}, \mathrm{~V}_{\mathrm{CM}}=\mathrm{V}_{\mathrm{O}}=\mathrm{V}^{+} / 2$, $\mathrm{R}_{\mathrm{L}}$ to ground, and $\mathrm{R}_{\mathrm{L}}>1 \mathrm{M} \Omega$. Boldface limits apply at the temperature extremes

| Symbol | Parameter | Conditions | $\begin{gathered} \text { Typ } \\ \text { (Note 5) } \end{gathered}$ | $\begin{aligned} & \text { LMC272C } \\ & \text { Limit } \\ & \text { (Note 6) } \\ & \hline \end{aligned}$ | Units |
| :---: | :---: | :---: | :---: | :---: | :---: |
| $\mathrm{V}_{\text {OS }}$ | Input Offset Voltage | $\mathrm{V}_{\mathrm{O}}=1.4 \mathrm{~V}, \mathrm{R}_{\mathrm{S}}=50, \mathrm{~V}_{\mathrm{CM}}=0 \mathrm{~V}, \mathrm{R}_{\mathrm{L}}=10 \mathrm{k}$ | 1.40 | $\begin{aligned} & 7 \\ & 9 \end{aligned}$ | $\begin{gathered} \mathrm{mV} \\ \max \end{gathered}$ |
| $\mathrm{TCV}_{\text {OS }}$ | Temp. Coefficient of Input Offset Voltage | $\mathrm{T}_{\mathrm{A}}=0^{\circ} \mathrm{C}$ to $70^{\circ} \mathrm{C}$ | 3.9 |  | $\mu \mathrm{V} /{ }^{\circ} \mathrm{C}$ |
| $\mathrm{I}_{\mathrm{B}}$ | Input Bias Current |  | 1 | 64 | pA <br> max |
| los | Input Offset Current |  | 0.5 | 32 | pA <br> max |
| CMRR | Common Mode Rejection Ratio | $\mathrm{V}_{\mathrm{CM}}=-0.2 \mathrm{~V}$ to 1.2 V | 77 | $\begin{aligned} & 65 \\ & 60 \end{aligned}$ | $\begin{gathered} \mathrm{dB} \\ \min \end{gathered}$ |
| PSRR | Power Supply Rejection Ratio | $\mathrm{V}+=2.7 \mathrm{~V}$ to $5 \mathrm{~V}, \mathrm{~V}_{\mathrm{O}}=1.4 \mathrm{~V}$ | 75 | $\begin{aligned} & 65 \\ & 60 \end{aligned}$ | $\begin{aligned} & \mathrm{dB} \\ & \mathrm{~min} \end{aligned}$ |
| $\mathrm{V}_{\mathrm{CM}}$ | Input Common-Mode Voltage Range | CMRR $\geq 50 \mathrm{~dB}$ | 1.7 | $\begin{aligned} & 1.5 \\ & \mathbf{1 . 2} \end{aligned}$ | $\begin{gathered} \mathrm{V} \\ \mathrm{~min} \end{gathered}$ |
|  |  |  | -0.3 | $\begin{array}{r} -0.2 \\ -0.2 \end{array}$ | $\begin{gathered} \mathrm{V} \\ \max \end{gathered}$ |
| $A_{V}$ | Large Signal Voltage Gain | $\mathrm{V}_{\mathrm{O}}=0.25 \mathrm{~V}$ to $2.45 \mathrm{~V}, \mathrm{R}_{\mathrm{L}}=10 \mathrm{k}$ | 88 |  | dB |
| $\mathrm{V}_{\mathrm{O}}$ | Output Swing | $\begin{aligned} & \mathrm{R}_{\mathrm{L}}=10 \mathrm{k} \Omega, \mathrm{~V}_{\mathrm{ID}}=100 \mathrm{mV} \\ & (\text { Note 11) } \end{aligned}$ | 2.64 | 2.55 | $\begin{gathered} \mathrm{V} \\ \min \end{gathered}$ |
|  |  | $\begin{aligned} & \mathrm{V}_{\mathrm{ID}}=-100 \mathrm{mV} \\ & \text { (Note 11) } \end{aligned}$ | 0 | $\begin{aligned} & 20 \\ & 25 \end{aligned}$ | mV max |
| Isc | Output Short Circuit Current | Sourcing, $\mathrm{V}_{\mathrm{ID}}=100 \mathrm{mV}$ (Note 11) | 3.7 |  | mA |
|  |  | Sinking, $\mathrm{V}_{\mathrm{ID}}=-100 \mathrm{mV}$ (Note 11) | 2.5 |  | mA |
| Is | Total Supply Current |  | 1.60 | $\begin{aligned} & 2.5 \\ & 3.0 \end{aligned}$ | mA <br> max |


| 2.7V AC Electrical Characteristics Unless otherwise specified, all limits guaranteed for $\mathrm{T}_{\mathrm{J}}=25^{\circ} \mathrm{C}, \mathrm{V}+=$ $2.7 \mathrm{~V}, \mathrm{~V}^{-}=0 \mathrm{~V}, \mathrm{~V}_{\mathrm{CM}}=\mathrm{V}_{\mathrm{O}}=\mathrm{V}^{+} / 2, \mathrm{R}_{\mathrm{L}}$ to ground and $\mathrm{R}_{\mathrm{L}}>1 \mathrm{M} \Omega$. Boldface limits apply at the temperature extremes |  |  |  |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: |
| Symbol | Parameter | Conditions | Typ (Note 5) | $\begin{aligned} & \text { LMC272C } \\ & \text { Limit } \\ & \text { (Note 6) } \\ & \hline \end{aligned}$ | Units |
| SR | Slew Rate (Note 8) | $\begin{aligned} & A_{V}=+1, R_{L}=10 \mathrm{k} \Omega \\ & \mathrm{VI}=1 \mathrm{~V}_{\mathrm{PP}}, \mathrm{C}_{\mathrm{L}}=20 \mathrm{pF} \\ & \text { (Note 12) } \end{aligned}$ | 1.7 |  | $\mathrm{V} / \mu \mathrm{s}$ |
| GBW | Unity Gain Frequency | $\begin{aligned} & \mathrm{VI}=10 \mathrm{mV} \mathrm{PP}, \mathrm{C}_{\mathrm{L}}=20 \mathrm{pF} \\ & \text { (Note 12) } \end{aligned}$ | 1.9 |  | MHz |
| $\phi_{\mathrm{m}}$ | Phase Margin | $\begin{aligned} & \mathrm{VI}=10 \mathrm{mV} \\ & \text { (Note 12) } \end{aligned}$ | 39 |  | Deg |
| $e_{n}$ | Input-Referred Voltage Noise | $\mathrm{f}=1 \mathrm{kHz}, \mathrm{R}_{\mathrm{S}}=20 \Omega$ | 27 |  | $\frac{\mathrm{nV}}{\sqrt{\mathrm{Hz}}}$ |
| $i_{n}$ | Input-Referred Current Noise | $\mathrm{f}=1 \mathrm{kHz}$ | 0.0015 |  | $\frac{\mathrm{pA}}{\sqrt{\mathrm{Hz}}}$ |
| $\mathrm{f}_{\text {max }}$ | Full Power Bandwidth | $\mathrm{V}_{\mathrm{S}}=10 \mathrm{~V}, \mathrm{C}_{\mathrm{L}}=20 \mathrm{pF}, \mathrm{R}_{\mathrm{L}}=20 \mathrm{k} \Omega$ | 120 |  | kHz |
|  | Amp-to-Amp Isolation | (Note 9) | 150 |  | dB |
| THD | Total Harmonic Distortion | $\begin{aligned} & \mathrm{A}_{\mathrm{V}}=+1, \mathrm{~V}_{\mathrm{IN}}=0.7 \mathrm{~V}_{\mathrm{PP}} \\ & \mathrm{f}=1 \mathrm{kHz} \end{aligned}$ | 0.035 |  | \% |

5V DC Electrical Characteristics Unless otherwise specified, all limits guaranteed for $\mathrm{T}_{\mathrm{J}}=25^{\circ} \mathrm{C}, \mathrm{V}+=$ $5 \mathrm{~V}, \mathrm{~V}^{-}=0 \mathrm{~V}, \mathrm{~V}_{\mathrm{CM}}=\mathrm{V}_{\mathrm{O}}=\mathrm{V}^{+} / 2, \mathrm{R}_{\mathrm{L}}$ to ground and $\mathrm{R}_{\mathrm{L}}>1 \mathrm{M} \Omega$. Boldface limits apply at the temperature extremes

| Symbol | Parameter | Conditions | $\begin{gathered} \text { Typ } \\ \text { (Note 5) } \end{gathered}$ | $\begin{gathered} \text { LMC272C } \\ \text { Limit } \\ \text { (Note 6) } \\ \hline \end{gathered}$ | Units |
| :---: | :---: | :---: | :---: | :---: | :---: |
| $\mathrm{V}_{\text {OS }}$ | Input Offset Voltage | $\begin{aligned} & \mathrm{V}_{\mathrm{O}}=1.4 \mathrm{~V}, \mathrm{R}_{\mathrm{S}}=50, \\ & \mathrm{R}_{\mathrm{L}}=10 \mathrm{k}, \mathrm{~V}_{\mathrm{CM}}=0 \mathrm{~V} \end{aligned}$ | 1.75 | $\begin{aligned} & 7 \\ & 9 \end{aligned}$ | $\begin{gathered} \mathrm{mV} \\ \max \end{gathered}$ |
| TCV ${ }_{\text {OS }}$ | Temp. Coefficient of Input Offset Voltage | $\mathrm{T}_{\mathrm{A}}=0^{\circ} \mathrm{C}$ to $70^{\circ} \mathrm{C}$ | 3.3 |  | $\mu \mathrm{V} /{ }^{\circ} \mathrm{C}$ |
| $\mathrm{I}_{\mathrm{B}}$ | Input Bias Current |  | 1 | 64 | pA <br> max |
| los | Input Offset Current |  | 0.5 | 32 | $\mathrm{pA}$ $\max$ |
| CMRR | Common Mode Rejection Ratio | $\mathrm{V}_{\mathrm{CM}}=-0.2 \mathrm{~V}$ to 3.5 V | 77 | $\begin{aligned} & 65 \\ & 60 \end{aligned}$ | $\begin{aligned} & \mathrm{dB} \\ & \mathrm{~min} \end{aligned}$ |
| PSRR | Power Supply Rejection Ratio | $\mathrm{V}+=5 \mathrm{~V}$ to $10 \mathrm{~V}, \mathrm{~V}_{\mathrm{O}}=1.4 \mathrm{~V}$ | 88 | $\begin{aligned} & 65 \\ & 60 \\ & \hline \end{aligned}$ | dB <br> min |
| $\mathrm{V}_{\mathrm{CM}}$ | Input Common-Mode Voltage Range | CMRR $\geq 50 \mathrm{~dB}$ | 4.2 | $\begin{gathered} 4 \\ 3.5 \\ \hline \end{gathered}$ | $\begin{gathered} \mathrm{V} \\ \mathrm{~min} \\ \hline \end{gathered}$ |
|  |  |  | -0.3 | $\begin{array}{r} -0.2 \\ -\mathbf{0 . 2} \end{array}$ | $\begin{gathered} \mathrm{V} \\ \max \end{gathered}$ |
| $A_{V}$ | Large Signal Voltage Gain | $\mathrm{V}_{\mathrm{O}}=0.25 \mathrm{~V}$ to $2 \mathrm{~V}, \mathrm{R}_{\mathrm{L}}=10 \mathrm{k}$ | 90 | $\begin{aligned} & 80 \\ & 72 \\ & \hline \end{aligned}$ | $\begin{gathered} \mathrm{dB} \\ \mathrm{~min} \end{gathered}$ |
| $\mathrm{V}_{0}$ | Output Swing | $\mathrm{R}_{\mathrm{L}}=10 \mathrm{k} \Omega, \mathrm{~V}_{\mathrm{ID}}=100 \mathrm{mV}$ <br> (Note 11) | 4.94 | $\begin{gathered} 4.85 \\ \mathbf{4 . 7 5} \end{gathered}$ | $\begin{gathered} \mathrm{V} \\ \mathrm{~min} \end{gathered}$ |
|  |  | $\begin{aligned} & \mathrm{V}_{\text {ID }}=-100 \mathrm{mV} \\ & \text { (Note 11) } \end{aligned}$ | 0 | $\begin{array}{r} 20 \\ \mathbf{2 5} \\ \hline \end{array}$ | $\begin{gathered} \mathrm{mV} \\ \max \end{gathered}$ |
| ISC | Output Short Circuit Current | Sourcing, $\mathrm{V}_{\mathrm{ID}}=100 \mathrm{mV}$ (Note 11) | 16 |  | mA |
|  |  | Sinking, $\mathrm{V}_{\mathrm{ID}}=-100 \mathrm{mV}$ (Note 11) | 16 |  | mA |
| Is |  |  | 1.95 | $\begin{aligned} & 3.2 \\ & 3.6 \end{aligned}$ | mA <br> max |


| 5V AC Electrical Characteristics Unless otherwise specified, all limits guaranteed for $\mathrm{T}_{\mathrm{J}}=25^{\circ} \mathrm{C}, \mathrm{V}+=$ $5 \mathrm{~V}, \mathrm{~V}^{-}=0 \mathrm{~V}, \mathrm{~V}_{\mathrm{CM}}=\mathrm{V}_{\mathrm{O}}=\mathrm{V}^{+} / 2, \mathrm{R}_{\mathrm{L}}$ to ground and $\mathrm{R}_{\mathrm{L}}>1 \mathrm{M} \Omega$. Boldface limits apply at the temperature extremes |  |  |  |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: |
| Symbol | Parameter | Conditions | Typ (Note 5) | $\begin{aligned} & \text { LMC272C } \\ & \text { Limit } \\ & \text { (Note 6) } \end{aligned}$ | Units |
| SR | Slew Rate (Note 8) | $\begin{aligned} & A_{V}=+1, R_{L}=10 \mathrm{k} \Omega \\ & \mathrm{VI}=1 \mathrm{~V}_{\mathrm{PP}}, \mathrm{C}_{\mathrm{L}}=20 \mathrm{pF} \\ & \text { (Note 12) } \end{aligned}$ | 2.5 |  | $\mathrm{V} / \mu \mathrm{s}$ |
|  |  | $\begin{aligned} & \mathrm{A}_{\mathrm{V}}=+1, \mathrm{R}_{\mathrm{L}}=10 \mathrm{k} \Omega, \\ & \mathrm{VI}=2.5 \mathrm{~V}_{\mathrm{PP}}, \mathrm{C}_{\mathrm{L}}=20 \mathrm{pF} \\ & (\text { Note 12) } \end{aligned}$ | 2.5 |  |  |
| GBW | Unity Gain Frequency | $\begin{aligned} & \mathrm{VI}=10 \mathrm{mV}, \mathrm{C}_{\mathrm{L}}=20 \mathrm{pF} \\ & \text { (Note 12) } \end{aligned}$ | 2.0 |  | MHz |
| $\phi_{\mathrm{m}}$ | Phase Margin | $\begin{aligned} & \mathrm{VI}=10 \mathrm{mV}, \mathrm{C}_{\mathrm{L}}=20 \mathrm{pF} \\ & \text { (Note 12) } \end{aligned}$ | 43 |  | Deg |
| $e_{n}$ | Input-Referred Voltage Noise | $\mathrm{f}=1 \mathrm{kHz}, \mathrm{R}_{\mathrm{S}}=20 \Omega$ | 25 |  | $\frac{n V}{\sqrt{\mathrm{~Hz}}}$ |
| $\mathrm{i}_{\mathrm{n}}$ | Input-Referred Current Noise | $\mathrm{f}=1 \mathrm{kHz}$ | 0.0015 |  | $\frac{\mathrm{pA}}{\sqrt{\mathrm{Hz}}}$ |
| $\mathrm{f}_{\text {max }}$ | Full Power Bandwidth | $\mathrm{V}_{\mathrm{S}}=10 \mathrm{~V}, \mathrm{C}_{\mathrm{L}}=20 \mathrm{pF}, \mathrm{R}_{\mathrm{L}}=20 \mathrm{k} \Omega$ | 120 |  | kHz |
|  | Amp-to-Amp Isolation | (Note 9) | 150 |  | dB |
| THD | Total Harmonic Distortion | $\begin{aligned} & A_{V}=+1, V_{I N}=2.5 V_{P P} \\ & f=1 \mathrm{kHz} \end{aligned}$ | 0.015 |  | \% |

10V DC Electrical Characteristics Unless otherwise specified, all limits guaranteed for $\mathrm{T}_{\mathrm{J}}=25^{\circ} \mathrm{C}, \mathrm{V}+=$ $10 \mathrm{~V}, \mathrm{~V}^{-}=0 \mathrm{~V}, \mathrm{~V}_{\mathrm{CM}}=\mathrm{V}_{\mathrm{O}}=\mathrm{V}^{+} / 2, \mathrm{R}_{\mathrm{L}}$ to ground and $\mathrm{R}_{\mathrm{L}}>1 \mathrm{M} \Omega$. Boldface limits apply at the temperature extremes

| Symbol | Parameter | Conditions | $\begin{gathered} \text { Typ } \\ \text { (Note 5) } \end{gathered}$ | $\begin{gathered} \text { LMC272C } \\ \text { Limit } \\ \text { (Note 6) } \\ \hline \end{gathered}$ | Units |
| :---: | :---: | :---: | :---: | :---: | :---: |
| $\mathrm{V}_{\text {OS }}$ | Input Offset Voltage | $\begin{aligned} & \mathrm{V}_{\mathrm{O}}=1.4 \mathrm{~V}, \mathrm{R}_{\mathrm{S}}=50, \\ & \mathrm{R}_{\mathrm{L}}=10 \mathrm{k}, \mathrm{~V}_{\mathrm{CM}}=0 \mathrm{~V} \end{aligned}$ | 2.1 | $\begin{aligned} & 7 \\ & 9 \end{aligned}$ | $\begin{gathered} \mathrm{mV} \\ \max \end{gathered}$ |
| TCV ${ }_{\text {OS }}$ | Temp. Coefficient of Input Offset Voltage | $\mathrm{T}_{\mathrm{A}}=0^{\circ} \mathrm{C}$ to $70^{\circ} \mathrm{C}$ | 3.6 |  | $\mu \mathrm{V} /{ }^{\circ} \mathrm{C}$ |
| $\mathrm{I}_{\mathrm{B}}$ | Input Bias Current |  | 1 | 64 | pA <br> max |
| los | Input Offset Current |  | 0.5 | 32 | pA <br> max |
| CMRR | Common Mode Rejection Ratio | $\mathrm{V}_{\mathrm{CM}}=-0.2 \mathrm{~V}$ to 8.5 V | 77 | $\begin{aligned} & 65 \\ & 60 \end{aligned}$ | $\begin{aligned} & \mathrm{dB} \\ & \mathrm{~min} \end{aligned}$ |
| PSRR | Power Supply Rejection Ratio | $\mathrm{V}+=5 \mathrm{~V}$ to $10 \mathrm{~V}, \mathrm{~V}_{\mathrm{O}}=1.4 \mathrm{~V}$ | 88 | $\begin{aligned} & 65 \\ & 60 \end{aligned}$ | dB <br> min |
| $\mathrm{V}_{\mathrm{CM}}$ | Input Common-Mode Voltage Range | CMRR $\geq 50 \mathrm{~dB}$ | 9.2 | $\begin{gathered} 9 \\ \mathbf{8 . 5} \\ \hline \end{gathered}$ | $\begin{gathered} \mathrm{V} \\ \mathrm{~min} \end{gathered}$ |
|  |  |  | -0.3 | $\begin{array}{r} -0.2 \\ -0.2 \end{array}$ | $\begin{gathered} \text { V } \\ \max \end{gathered}$ |
| $A_{V}$ | Large Signal Voltage Gain | $\mathrm{V}_{\mathrm{O}}=1 \mathrm{~V}$ to $6 \mathrm{~V}, \mathrm{R}_{\mathrm{L}}=10 \mathrm{k}$ | 95 | $\begin{aligned} & 85 \\ & 78 \end{aligned}$ | dB <br> min |
| $\mathrm{V}_{0}$ | Output Swing | $\begin{aligned} & \mathrm{R}_{\mathrm{L}}=10 \mathrm{k} \Omega, \mathrm{~V}_{\mathrm{ID}}=100 \mathrm{mV} \\ & \text { (Note 11) } \end{aligned}$ | 9.93 | $\begin{gathered} 9.85 \\ \mathbf{9 . 7 5} \\ \hline \end{gathered}$ | $\begin{gathered} \mathrm{V} \\ \mathrm{~min} \end{gathered}$ |
|  |  | $\begin{aligned} & \mathrm{V}_{I D}=-100 \mathrm{mV} \\ & \text { (Note 11) } \end{aligned}$ | 33 | $\begin{aligned} & 45 \\ & 50 \end{aligned}$ | $\begin{gathered} \mathrm{mV} \\ \max \end{gathered}$ |
| Isc | Output Short Circuit Current | Sourcing, $\mathrm{V}_{\mathrm{ID}}=100 \mathrm{mV}$ <br> (Note 11) | 55 |  | mA |
|  |  | Sinking, $\mathrm{V}_{\mathrm{ID}}=-100 \mathrm{mV}$ (Note 11) | 25 |  | mA |
| Is | Total Supply Current |  | 2.25 | $\begin{aligned} & 3.6 \\ & 4.0 \\ & \hline \end{aligned}$ | mA <br> max |


| 10V AC Electrical Characteristics Unless otherwise specified, all limits guaranteed for $\mathrm{T}_{\mathrm{J}}=25^{\circ} \mathrm{C}, \mathrm{V}+=$ $10 \mathrm{~V}, \mathrm{~V}^{-}=0 \mathrm{~V}, \mathrm{~V}_{\mathrm{CM}}=\mathrm{V}_{\mathrm{O}}=\mathrm{V}^{+} / 2, \mathrm{R}_{\mathrm{L}}$ to ground and $\mathrm{R}_{\mathrm{L}}>1 \mathrm{M} \Omega$. Boldface limits apply at the temperature extremes |  |  |  |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: |
| Symbol | Parameter | Conditions | Typ (Note 5) | $\begin{aligned} & \text { LMC272C } \\ & \text { Limit } \\ & \text { (Note 6) } \end{aligned}$ | Units |
| SR | Slew Rate (Note 8) | $\begin{aligned} & A_{V}=+1, R_{L}=10 \mathrm{k} \Omega \\ & \mathrm{VI}=1 \mathrm{VPP}, \mathrm{C}_{\mathrm{L}}=20 \mathrm{pF} \\ & \text { (Note 12) } \end{aligned}$ | 2.65 |  | $\mathrm{V} / \mu \mathrm{S}$ |
|  |  | $\begin{aligned} & \mathrm{A}_{\mathrm{V}}=+1, \mathrm{R}_{\mathrm{L}}=10 \mathrm{k} \Omega \\ & \mathrm{VI}=5.5 \mathrm{~V}_{\mathrm{PP}}, \mathrm{C}_{\mathrm{L}}=20 \mathrm{pF} \\ & (\text { Note 12) } \end{aligned}$ | 2.65 |  |  |
| GBW | Unity Gain Frequency | $\begin{aligned} & \mathrm{VI}=10 \mathrm{mV}, \mathrm{C}_{\mathrm{L}}=20 \mathrm{pF} \\ & \text { (Note 12) } \end{aligned}$ | 2.1 |  | MHz |
| $\phi_{\mathrm{m}}$ | Phase Margin | $\begin{aligned} & \mathrm{VI}=10 \mathrm{mV}, \mathrm{C}_{\mathrm{L}}=20 \mathrm{pF} \\ & \text { (Note 12) } \end{aligned}$ | 44 |  | Deg |
| $e_{n}$ | Input-Referred Voltage Noise | $\mathrm{f}=1 \mathrm{kHz}, R_{\mathrm{S}}=20 \Omega$ | 25 |  | $\frac{\mathrm{n} V}{\sqrt{\mathrm{~Hz}}}$ |
| $\mathrm{i}_{\mathrm{n}}$ | Input-Referred Current Noise | $\mathrm{f}=1 \mathrm{kHz}$ | 0.0015 |  | $\frac{\mathrm{pA}}{\sqrt{\mathrm{Hz}}}$ |
| $\mathrm{f}_{\text {max }}$ | Full Power Bandwidth | $\mathrm{C}_{\mathrm{L}}=20 \mathrm{pF}, \mathrm{R}_{\mathrm{L}}=20 \mathrm{k} \Omega$ | 120 |  | kHz |
|  | Amp-to-Amp Isolation | (Note 9) | 150 |  | dB |
| THD | Total Harmonic Distortion | $\begin{aligned} & A_{V}=+1, V_{I N}=5 V_{P P} \\ & f=1 \mathrm{kHz} \end{aligned}$ | 0.005 |  | \% |
| Note 4: The maximum power dissipation is a function of $T_{J(\max )}, \theta_{\mathrm{JA}}$, and $\mathrm{T}_{\mathrm{A}}$. The maximum allowable power dissipation at any ambient temperature is $\mathrm{P}_{\mathrm{D}}=$ $\left(T_{J(\max )}-T_{A}\right) / \theta_{J A}$. All numbers apply for packages soldered directly into a PC board. <br> Note 5: Typical Values represent the most likely parametric norm. <br> Note 6: All limits are guaranteed by testing or statistical analysis. <br> Note 7: Do not short circuit output to $\mathrm{V}+$, when $\mathrm{V}+$ is greater than 13 V or reliability will be adversely affected. <br> Note 8: Slew rate is the slower of the rising and falling slew rates. <br> Note 9: Input referred, $\mathrm{V}+=10 \mathrm{~V}$ and $\mathrm{R}_{\mathrm{L}}=100 \mathrm{k} \Omega$ connected to 5 V . Each amp excited in turn with 1 kHz to produce about $10 \mathrm{~V}_{\mathrm{PP}}$ output. <br> Note 10: Limiting input pin current is only necessary for input voltages that exceed absolute maximum input voltage ratings. <br> Note 11: $\mathrm{V}_{I D}$ is the differential voltage on the non-inverting input with respect to the inverting input. <br> Note 12: $\mathrm{V}_{1}$ is the input voltage. |  |  |  |  |  |




## Typical Performance Characteristics

$\left(V_{S}=+5 \mathrm{~V}\right.$, single supply, $T_{A}=25^{\circ} \mathrm{C}$, and $R_{L}$ to ground unless otherwise specified) (Continued)



## Typical Performance Characteristics

$\left(\mathrm{V}_{\mathrm{S}}=+5 \mathrm{~V}\right.$, single supply, $\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$, and $\mathrm{R}_{\mathrm{L}}$ to ground unless otherwise specified) (Continued)


TL/H/12867-36


TL/H/12867-35


## Application Information



## TL/H/12867-2

It is generally difficult to find already existing solutions in the market which are single supply and low noise. The circuit above is a low noise single supply preamp using the LMC272. It utilizes the feature of input common mode voltage range to ground to achieve zero-volt-in zero-volt-out performance and uses the RR output swing to achieve maximum dynamic range. By introducing a differential pair operating at high bias current as the front end, the equivalent input noise voltage, $e_{n}$, is reduced. The gain is $1+R 5 / R 6$
which is a 1000 in this case. There is an inherent trade off between noise voltage and power consumption, input bias current, and input noise current. Input equivalent noise current is inconsequential if the source impedance is small. R1 can be adjusted to vary bias current. To avoid saturation, R3 and R4 should be set such that Q1 and Q3 collector voltages do not exceed 0.5 V . Table I shows typical noise data for two different R1 settings:

TABLE I. Equivalent Input Noise Voltage, $\mathrm{e}_{\mathrm{n}}$, for Two Different Values of R1

| $\Omega$ | $\mathbf{m A}$ | $\mathbf{n V} / \sqrt{\mathbf{H z}}$ |  |  |
| :---: | :---: | :---: | :---: | :---: |
| $\mathbf{R 1}$ | $\mathbf{I}_{\mathbf{C}}(\mathbf{Q 1}, \mathbf{3})$ | $\mathbf{e}_{\mathbf{n}}(\mathbf{1 0 0} \mathbf{~ H z})$ | $\mathbf{e}_{\mathbf{n}}(\mathbf{1} \mathbf{~ k H z})$ | $\mathbf{e}_{\mathbf{n}}(\mathbf{1 0} \mathbf{~ k H z})$ |
| 270 | 1.85 | 3.2 | 2.0 | 1.7 |
| 1000 | 0.50 | 5.3 | 2.4 | 1.9 |

## Application Information (Continued)



TL/H/12867-3

Here is another application for the LMC272. This is a single supply notch filter set for 60 Hz using the component values shown, but the frequency can be changed using the equations below. The main feature of this circuit is its ability to adjust the filter selectivity $(Q)$ using RPOT. You can trade off notch depth for Q . Table II shows data for two different settings. The LMC272 lends itself nicely to general purpose applications like this because it is very well behaved and easy to use. This filter can operate from 2.7 V to 15 V supplies. Component value matching is important to achieve good results. Here R4 is used to set the input to within the common mode range of the device to allow maximum swing on the non-inverting input (pin 3). Since R1, R2, and R4 form a voltage divider at low frequencies, C4 is added to introduce a high frequency attenuation in conjunction with C1, and C3. R5 and R6 were picked to set the pass band gain to 0 dB .
$\mathrm{R}=\mathrm{R} 1=\mathrm{R} 2=2 \mathrm{R} 3$
$\mathrm{C}=\mathrm{C} 1=\mathrm{C} 3=\mathrm{C} 2 / 2$
$f($ notch $)=\frac{1}{2 \pi R C} ; C 4=\frac{R \cdot C}{R 4}, Q=\frac{f(\text { notch })}{B W}$
TABLE II. Filter Selectivity (Q) vs Notch Depth

|  | (dB) |
| :---: | :---: |
| $\mathbf{Q}$ | Notch Depth |
| 0.3 | 40 |
| 6 | 17 |

## Application Information (Continued)



TL/H/12867-4
$\mathrm{f}_{\mathrm{OSC}} \cong \frac{1}{2 \pi \sqrt{\mathrm{C} 1 \mathrm{C} 2 \mathrm{R1R2}}}$
f (range) $=6.4 \mathrm{kHz}$ to 30 kHz
Amplitude Adjustment (range) $=2.8 \mathrm{~V}$ PP to $8.6 \mathrm{~V}_{\mathrm{PP}}$

Physical Dimensions inches (millimeters) unless otherwise noted


8-Lead ( $0.150^{\prime \prime}$ Wide) Molded Small Outline Package, JEDEC
Order Number LMC272CM or LMC272CMX
NS Package Number M08A


## LIFE SUPPORT POLICY

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Absolute Maximum Ratings (Note 1) If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.
ESD Tolerance (Note 2)

| Human Body Model | 3000 V |
| :--- | ---: |
| Machine Model | 350 V |
| Differential Input Voltage | $\pm$ Supply Voltage |
| Supply Voltage $\left(\mathrm{V}^{+}-\mathrm{V}^{-}\right.$) | 16 V |
| Output Short Circuit to $\mathrm{V}^{+}$ | (Note 8) |
| Output Short Circuit to $\mathrm{V}^{-}$ | (Note 3) |
| Lead Temperature (soldering, 10 sec.) | $260^{\circ} \mathrm{C}$ |
| Current at Output Pin | $\pm 18 \mathrm{~mA}$ |
| Current at Input Pin | $\pm 5 \mathrm{~mA}$ |


| Current at Power Supply Pin | 35 mA |
| :--- | ---: |
| Storage Temperature Range | $-65^{\circ} \mathrm{C}$ to $+150^{\circ} \mathrm{C}$ |
| Junction Temperature (Note 4) | $150^{\circ} \mathrm{C}$ |
| Operating Ratings (Note 1) |  |
| Supply Voltage |  |
| Temperature Range | 2.0 V to 15.5 V |
| LMC6035I and LMC6036I | $-40^{\circ} \mathrm{C} \pm \mathrm{T}_{J} \pm+85^{\circ} \mathrm{C}$ |
| Thermal Resistance $\left(\theta_{\mathrm{JAA}}\right)$ |  |
| MSOP, 8-pin Mini Surface Mount | $230^{\circ} \mathrm{C} / \mathrm{W}$ |
| M Package, 8-pin Surface Mount | $175^{\circ} \mathrm{C} / \mathrm{W}$ |
| M Package, 14-pin Surface Mount | $127^{\circ} \mathrm{C} / \mathrm{W}$ |
|  |  |

DC Electrical Characteristics Unless otherwise specified, all limits guaranteed for $\mathrm{T}_{\mathrm{J}}=25^{\circ} \mathrm{C}, \mathrm{V}+=2.7 \mathrm{~V}$, $\mathrm{V}^{-}=0 \mathrm{~V}, \mathrm{~V}_{\mathrm{CM}}=1.0 \mathrm{~V}, \mathrm{~V}_{\mathrm{O}}=1.35 \mathrm{~V}$ and $\mathrm{R}_{\mathrm{L}}>1 \mathrm{M} \Omega$. Boldface limits apply at the temperature extremes.

| Symbol | Parameter | Conditions | Typ <br> (Note 5) | $\begin{gathered} \text { LMC6035I } \\ \text { LMC6036I } \\ \text { Limit (Note 6) } \\ \hline \end{gathered}$ | Units |
| :---: | :---: | :---: | :---: | :---: | :---: |
| $\mathrm{V}_{\text {OS }}$ | Input Offset Voltage |  | 0.5 | $\begin{aligned} & 5 \\ & 6 \end{aligned}$ | $\begin{gathered} m V \\ \max \end{gathered}$ |
| TCV ${ }_{\text {OS }}$ | Input Offset Voltage Average Drift |  | 2.3 |  | $\mu \mathrm{V} /{ }^{\circ} \mathrm{C}$ |
| IN | Input Current | (Note 11) | 0.02 | 90 | $\mathrm{pA}$ $\max$ |
| los | Input Offset Current | (Note 11) | 0.01 | 45 | pA <br> max |
| $\mathrm{R}_{\text {IN }}$ | Input Resistance |  | > 10 |  | Tera $\Omega$ |
| CMRR | Common Mode Rejection Ratio | $\begin{aligned} & 0.7 \mathrm{~V} \leq \mathrm{V}_{\mathrm{CM}} \leq 12.7 \mathrm{~V} \\ & \mathrm{~V}+=15 \mathrm{~V} \end{aligned}$ | 96 | $\begin{aligned} & 63 \\ & 60 \end{aligned}$ | $\begin{aligned} & \mathrm{dB} \\ & \mathrm{~min} \end{aligned}$ |
| + PSRR | Positive Power Supply Rejection Ratio | $\begin{aligned} & 5 \mathrm{~V} \leq \mathrm{V}^{+} \leq 15 \mathrm{~V}, \\ & \mathrm{~V}_{\mathrm{O}}=2.5 \mathrm{~V} \end{aligned}$ | 93 | $\begin{aligned} & 63 \\ & 60 \\ & \hline \end{aligned}$ | $\begin{aligned} & \mathrm{dB} \\ & \mathrm{~min} \end{aligned}$ |
| -PSRR | Negative Power Supply Rejection Ratio | $\begin{aligned} & 0 \mathrm{~V} \leq \mathrm{V}^{-} \leq-10 \mathrm{~V} \\ & \mathrm{~V}_{\mathrm{O}}=2.5 \mathrm{~V}, \mathrm{~V}^{+}=5 \mathrm{~V} \end{aligned}$ | 97 | $\begin{aligned} & 74 \\ & 70 \\ & \hline \end{aligned}$ | $\begin{gathered} \mathrm{dB} \\ \mathrm{~min} \end{gathered}$ |
| $\mathrm{V}_{\mathrm{CM}}$ | Input Common-Mode Voltage Range | $\begin{aligned} & \mathrm{V}^{+}=2.7 \mathrm{~V} \\ & \text { For CMRR } \geq 40 \mathrm{~dB} \end{aligned}$ | -0.1 | $\begin{aligned} & 0.3 \\ & 0.5 \end{aligned}$ | $\begin{gathered} \mathrm{V} \\ \max \end{gathered}$ |
|  |  |  | 2.3 | $\begin{aligned} & 2.0 \\ & 1.7 \end{aligned}$ | $\begin{gathered} \mathrm{V} \\ \mathrm{~min} \end{gathered}$ |
|  |  | $\begin{aligned} & \mathrm{V}^{+}=3 \mathrm{~V} \\ & \text { For CMRR } \geq 40 \mathrm{~dB} \end{aligned}$ | -0.3 | $\begin{aligned} & 0.1 \\ & 0.3 \end{aligned}$ | $\begin{gathered} \text { V } \\ \max \end{gathered}$ |
|  |  |  | 2.6 | $\begin{aligned} & 2.3 \\ & 2.0 \end{aligned}$ | $\begin{gathered} \mathrm{V} \\ \mathrm{~min} \end{gathered}$ |
|  |  | $\begin{aligned} & \mathrm{V}^{+}=5 \mathrm{~V} \\ & \text { For CMRR } \geq 50 \mathrm{~dB} \end{aligned}$ | -0.5 | $\begin{gathered} -0.2 \\ \mathbf{0 . 0} \end{gathered}$ | $\begin{gathered} \mathrm{V} \\ \max \end{gathered}$ |
|  |  |  | 4.5 | $\begin{aligned} & 4.2 \\ & 3.9 \end{aligned}$ | $\begin{gathered} \mathrm{V} \\ \mathrm{~min} \end{gathered}$ |
|  |  | $\begin{aligned} & \mathrm{V}^{+}=15 \mathrm{~V} \\ & \text { For CMRR } \geq 50 \mathrm{~dB} \end{aligned}$ | -0.5 | $\begin{gathered} -0.2 \\ \mathbf{0 . 0} \\ \hline \end{gathered}$ | $\begin{gathered} \mathrm{V} \\ \max \\ \hline \end{gathered}$ |
|  |  |  | 14.4 | $\begin{gathered} 14.0 \\ \mathbf{1 3 . 7} \end{gathered}$ | $\begin{gathered} \mathrm{V} \\ \mathrm{~min} \end{gathered}$ |



## AC Electrical Characteristics

Unless otherwise specified, all limits guaranteed for $T_{J}=25^{\circ} \mathrm{C}, \mathrm{V}^{+}=2.7 \mathrm{~V}, \mathrm{~V}^{-}=0 \mathrm{~V}, \mathrm{~V}_{\mathrm{CM}}=1.0 \mathrm{~V}, \mathrm{~V}_{\mathrm{O}}=1.35 \mathrm{~V}$ and $R_{L}>1 \mathrm{M} \Omega$. Boldface limits apply at the temperature extremes.

| Symbol | Parameter | Conditions | Typ (Note 5) | Units |
| :---: | :---: | :---: | :---: | :---: |
| SR | Slew Rate | (Note 9) | 1.5 | $\mathrm{V} / \mu \mathrm{s}$ |
| GBW | Gain Bandwidth Product | $\mathrm{V}^{+}=15 \mathrm{~V}$ | 1.4 | MHz |
| $\theta_{\mathrm{m}}$ | Phase Margin |  | 48 | - |
| $\mathrm{G}_{\mathrm{m}}$ | Gain Margin |  | 17 | dB |
|  | Amp-to-Amp Isolation | (Note 10) | 130 | dB |
| $e_{n}$ | Input-Referred Voltage Noise | $\begin{aligned} & f=1 \mathrm{kHz} \\ & \mathrm{~V}_{\mathrm{CM}}=1 \mathrm{~V} \end{aligned}$ | 27 | $\mathrm{nV} / \sqrt{\mathrm{Hz}}$ |
| $\mathrm{i}_{\mathrm{n}}$ | Input Referred Current Noise | $\mathrm{f}=1 \mathrm{kHz}$ | 0.2 | $\mathrm{fA} / \sqrt{\mathrm{Hz}}$ |
| THD | Total Harmonic Distortion | $\begin{aligned} & f=10 \mathrm{kHz}, \mathrm{~A}_{\mathrm{V}}=-10 \\ & \mathrm{R}_{\mathrm{L}}=2 \mathrm{k} \Omega, \mathrm{~V}_{\mathrm{O}}=8 \mathrm{~V} \mathrm{PP} \\ & \mathrm{~V}^{+}=10 \mathrm{~V} \end{aligned}$ | 0.01 | \% |

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but specific performance is not guaranteed. For guaranteed specifications and the test conditions, see the Electrical Characteristics. Note 2: Human body model, $1.5 \mathrm{k} \Omega$ in series with 100 pF .
Note 3: Applies to both single-supply and split-supply operation. Continuous short circuit operation at elevated ambient temperature can result in exceeding the maximum allowed junction temperature of $150^{\circ} \mathrm{C}$. Output currents in excess of 30 mA over long term may adversely affect reliabilty.
Note 4: The maximum power dissipation is a function of $T_{J(\max )}, \theta_{J A}$, and $T_{A}$. The maximum allowable power dissipation at any ambient temperature is $P_{D}=$
$\left(T_{J(\max )}-T_{A}\right) / \theta_{J A}$. All numbers apply for packages soldered directly onto a PC board with no air flow.
Note 5: Typical Values represent the most likely parametric norm or one sigma value.
Note 6: All limits are guaranteed by testing or statistical analysis.
Note 7: $\mathrm{V}^{+}=15 \mathrm{~V}, \mathrm{~V}_{\mathrm{CM}}=7.5 \mathrm{~V}$ and $\mathrm{R}_{\mathrm{L}}$ connected to 7.5 V . For Sourcing tests, $7.5 \mathrm{~V} \leq \mathrm{V}_{\mathrm{O}} \leq 11.5 \mathrm{~V}$. For Sinking tests, $3.5 \mathrm{~V} \leq \mathrm{V}_{\mathrm{O}} \leq 7.5 \mathrm{~V}$.
Note 8: Do not short circuit output to $\mathrm{V}^{+}$when $\mathrm{V}+$ is greater than 13 V or reliability will be adversely affected.
Note 9: $\mathrm{V}^{+}=15 \mathrm{~V}$. Connected as voltage follower with 10 V step input. Number specified is the slower of the positive and negative slew rates.
Note 10: Input referred, $\mathrm{V}^{+}=15 \mathrm{~V}$ and $\mathrm{R}_{\mathrm{L}}=100 \mathrm{k} \Omega$ connected to 7.5 V . Each amp excited in turn with 1 kHz to produce $\mathrm{V}_{\mathrm{O}}=12 \mathrm{~V}_{\mathrm{PP}}$.
Note 11: Guaranteed by design.





### 1.0 Application Notes

### 1.1 BACKGROUND

The LMC6035/6 is exceptionally well suited for low voltage applications. A desirable feature that the LMC6035/6 brings to low voltage applications is its output drive capability-a hallmark for National's CMOS amplifiers. The circuit of Figure 1 illustrates the drive capability of the LMC6035/6 at 3 V of supply. It is a differential output driver for a one-to-one audio transformer, like those used for isolating ground from the telephone lines. The transformer (T1) loads the op amps with about $600 \Omega$ of $A C$ load, at 1 kHz . Capacitor C1 functions to block DC from the low winding resistance of T1. Although the value of C 1 is relatively high, its load reactance $(\mathrm{Xc})$ is negligible compared to inductive reactance $\left(\mathrm{X}_{\mathrm{l}}\right)$ of T 1 .


## FIGURE 1. Differential Driver

The circuit in Figure 1 consists of one input signal and two output signals. U1A amplifies the input with an inverting gain of -2 , while the U1B amplifies the input with a noninverting gain of +2 . Since the two outputs are $180^{\circ}$ out of phase with each other, the gain across the differential output is 4 . As the differential output swings between the supply rails, one of the op amps sources the current to the load, while the other op amp sinks the current.
How good a CMOS op amp can sink or source a current is an important factor in determining its output swing capability. The output stage of the LMC6035/6-like many op amps-sources and sinks output current through two complementary transistors in series. This "totem pole" arrangement translates to a channel resistance ( $\mathrm{R}_{\text {dson }}$ ) at each supply rail which acts to limit the output swing. Most CMOS op amps are able to swing the outputs very close to the rails-except, however, under the difficult conditions of low supply voltage and heavy load. The LMC6035/6 exhibits exceptional output swing capability under these conditions.

The scope photos of Figures 2 and 3 represent measurements taken directly at the output (relative to GND) of U1A, in Figure 1. Figure 2 illustrates the output swing capability of the LMC6035, while Figure 3 provides a benchmark comparison. (The benchmark op amp is another low voltage $(3 \mathrm{~V})$ op amp manufactured by one of our reputable competitors.)


TL/H/12830-45
FIGURE 2. Output Swing Performance of the LMC6035 per the Circuit of Figure 1


Time ( $100 \mu \mathrm{~s} / \mathrm{div}$ )
TL/H/12830-46
FIGURE 3. Output Swing Performance of Benchmark Op Amp per the Circuit of Figure 1
Notice the superior drive capability of LMC6035 when compared with the benchmark measurement-even though the benchmark op amp uses twice the supply current.
Not only does the LMC6035/6 provide excellent output swing capability at low supply voltages, it also maintains high open loop gain (Avol) with heavy loads. To illustrate this, the LMC6035 and the benchmark op amp were compared for their distortion performance in the circuit of Figure 1. The graph of Figure 4 shows this comparison. The $y$-axis represents percent Total Harmonic Distortion (THD plus noise) across the loaded secondary of T1. The x-axis represents the input amplitude of a 1 kHz sine wave. (Note that T1 loses about $20 \%$ of the voltage to the voltage divider of $R_{L}(600 \Omega)$ and T1's winding resistances-a performance deficiency of the transformer.)

### 1.0 Application Notes

(Continued)


FIGURE 4. THD + Noise Performance of LMC6035 and "Benchmark" per Circuit of Figure 1
Figure 4 shows the superior distortion performance of LMC6035/6 over that of the benchmark op amp. The heavy loading of the circuit causes the Avol of the benchmark part to drop significantly which causes increased distortion.

### 1.2 APPLICATION CIRCUITS

1.2.1 Low-Pass Active Filter

A common application for low voltage systems would be active filters, in cordless and cellular phones for example. The ultra low input currents ( $\left(l_{\mathbb{N}}\right)$ of the LMC6035/6 makes it well suited for low power active filter applications, because it allows the use of higher resistor values and lower capacitor values. This reduces power consumption and space.
Figure 5 shows a low pass, active filter with a Butterworth (maximally flat) frequency response. Its topology is a Sallen and Key filter with unity gain. Note the normalized component values in parenthesis which are obtainable from standard filter design handbooks. These values provide a 1 Hz cutoff frequency, but they can be easily scaled for a desired cutoff frequency ( $\mathrm{f}_{\mathrm{c}}$ ). The bold component values of Figure 5 provide a cutoff frequency of 3 kHz . An example of the scaling procedure follows Figure 5.


TL/H/12830-48
FIGURE 5. 2-Pole, 3 kHz, Active, Sallen and Key, Lowpass Filter with Butterworth Response

### 1.2.1.1 Low-Pass Frequency Scaling Procedure

The actual component values represented in bold of Figure 5 were obtained with the following scaling procedure:
a) First determine the frequency scaling factor (FSF) for the desired cutoff frequency. Choosing $f_{c}$ at 3 kHz , provides the following FSF computation:
FSF $=2 \pi \times 3 \mathrm{kHz}$ (desired cutoff freq.) $=18.84 \times 10^{3}$
b) Then divide all of the normalized capacitor values by the FSF as follows:

C1' $=$ C(Normalized) $^{( } /$FSF
$C^{\prime}{ }^{\prime}=0.707 / 18.84 \times 10^{3}=37.93 \times 10^{-6}$
$\mathrm{C}^{\prime}=1.414 / 18.84 \times 10^{3}=75.05 \times 10^{-6}$
(C1' and C2': prior to impedance scaling)
c) Last, choose an impedance scaling factor (Z). This Z factor can be calculated from a standard value for C 2 . Then $Z$ can be used to determine the remaining component values as follows:
$\mathrm{Z}=\mathrm{C} 2^{\prime} / \mathrm{C}^{(\text {chosen })}=75.05 \times 10-6 / 6.8 \mathrm{nF}=8.4 \mathrm{k}$ $\mathrm{C} 1=\mathrm{C} 1$ ' $/ \mathrm{Z}=37.93 \times 10^{-6} / 8.4 \mathrm{k}=4.52 \mathrm{nF}$
(Standard capacitor value chosen for C 1 is 4.7 nF )
$\mathrm{R} 1=\mathrm{R} 1_{\text {(normalized) }} \times \mathrm{Z}=1 \Omega \times 8.4 \mathrm{k}=8.4 \mathrm{k} \Omega$
$\mathrm{R} 2=\mathrm{R} 2_{\text {(normalized) }} \times \mathrm{Z}=1 \Omega \times 8.4 \mathrm{k}=8.4 \mathrm{k} \Omega$
(Standard value chosen for R1 and R2 is $8.45 \mathrm{k} \Omega$ )

### 1.0 Application Notes (Continued)

### 1.2.2 High Pass Active Filter

The previous low-pass filter circuit of Figure 5 converts to a high-pass active filter per Figure 6.


## FILTER 6. 2 Pole, 300 Hz , Sallen and Key, High-Pass Filter

### 1.2.2.1 High-Pass Frequency Scaling Procedure

Choose a standard capacitor value and scale the impedances in the circuit according to the desired cutoff frequency $(300 \mathrm{~Hz})$ as follows:

$$
\begin{aligned}
& C=C 1=C 2 \\
& Z=1 \text { Farad/C (chosen) } \times 2 \pi \times \text { (desired cutoff freq.) }
\end{aligned}
$$

$$
=1 \mathrm{Farad} / 6.8 \mathrm{nF} \times 2 \pi \times 300 \mathrm{~Hz}=78.05 \mathrm{k}
$$

$\mathrm{R} 1=\mathrm{Z} \times \mathrm{R1}$ (normalized) $=78.05 \mathrm{k} \times(1 / 0.707)=110.4 \mathrm{k} \Omega$ (Standard value chosen for R1 is $\mathbf{1 1 0} \mathbf{k} \Omega$ )
$\mathrm{R} 2=\mathrm{Z} \times \mathrm{R}$ 2 $_{\text {(normalized) }}=78.05 \mathrm{k} \times(1 / 1.414)=55.2 \mathrm{k} \Omega$ (Standard value chosen for R1 is $54.9 \mathbf{k} \Omega$ )

### 1.2.3 Dual Amplifier Bandpass Filter

The dual amplifier bandpass (DABP) filter features the ability to independently adjust $\mathrm{f}_{\mathrm{C}}$ and Q . In most other bandpass topologies, the $f_{c}$ and $Q$ adjustments interact with each other. The DABP filter also offers both low sensitivity to component values and high Qs. The following application of Figure 7 , provides a 1 kHz center frequency and a Q of 100 .


TL/H/12830-50
FIGURE 7. 2 Pole, 1 kHz Active, Bandpass Filter

### 1.2.3.1 DABP Component Selection Procedure

Component selection for the DABP filter is performed as follows:
a) First choose a center frequency $\left(\mathrm{f}_{\mathrm{c}}\right)$. Figure 7 represents component values that were obtained from the following computation for a center frequency of 1 kHz .
$R 2=R 3=1 /\left(2 \pi f_{C} C\right)$
Given: $\mathrm{f}_{\mathrm{C}}=1 \mathrm{kHz}$ and $\mathrm{C}_{\text {(chosen) }}=\mathbf{6 . 8} \mathbf{~ n F}$
$\mathrm{R} 2=\mathrm{R} 3=1 /(2 \pi \times 3 \mathrm{kHz} \times 6.8 \mathrm{nF})=23.4 \mathrm{k} \Omega$
(Chosen standard value is $23.7 \mathrm{k} \Omega$ )
b) Then compute R 1 for a desired $Q\left(\mathrm{f}_{\mathrm{C}} / \mathrm{BW}\right)$ as follows:
$R 1=Q \times R 2$.
Choosing a $Q$ of 100 ,
$R 1=100 \times 23.7 \mathrm{k} \Omega=2.37 \mathrm{M} \Omega$.

## Application Notes (Continued)

### 1.3 PRINTED-CIRCUIT-BOARD LAYOUT FOR HIGH-IMPEDANCE WORK

It is generally recognized that any circuit which must operate with $<1000 \mathrm{pA}$ of leakage current requires special layout of the PC board. If one wishes to take advantage of the ultra-low bias current of the LMC6035/6, typically $<0.04$ pA , it is essential to have an excellent layout. Fortunately, the techniques for obtaining low leakages are quite simple. First, the user must not ignore the surface leakage of the PC board, even though it may at times appear acceptably low. Under conditions of high humidity, dust or contamination, the surface leakage will be appreciable.
To minimize the effect of any surface leakage, lay out a ring of foil completely surrounding the LMC6035 or LMC6036 inputs and the terminals of capacitors, diodes, conductors, resistors, relay terminals, etc. connected to the op amp's inputs. See Figure 8. To have a significant effect, guard rings should be placed on both the top and bottom of the PC board. This PC foil must then be connected to a voltage which is at the same voltage as the amplifier inputs, since no leakage current can flow between two points at the same potential. For example, a PC board trace-to-pad resistance of $10^{12} \Omega$, which is normally considered a very large resistance, could leak 5 pA if the trace were a 5 V bus adjacent to the pad of an input. This would cause a 100 times degradation from the amplifiers actual performance. However, if a guard ring is held within 5 mV of the inputs, then even a resistance of $1011 \Omega$ would cause only 0.05 pA of leakage current, or perhaps a minor (2:1) degradation of the amplifier's performance. See Figures 9a, 9b, 9c for typical connections of guard rings for standard op amp configurations. If both inputs are active and at high impedance, the guard can be tied to ground and still provide some protection; see Figure 9d.

(b) Non-Inverting Amplifier

(c) Follower

(d) Howland Current Pump

FIGURE 9. Guard Ring Connections

## Application Notes (Continued)

### 1.3.1 CAPACITIVE LOAD TOLERANCE

Like many other op amps, the LMC6035/6 may oscillate when its applied load appears capacitive. The threshold of oscillation varies both with load and circuit gain. The configuration most sensitive to oscillation is a unity-gain follower. See the Typical Performance Characteristics.
The load capacitance interacts with the op amp's output resistance to create an additional pole. If this pole frequency is sufficiently low, it will degrade the op amp's phase margin so that the amplifier is no longer stable at low gains. As shown in Figure 10a, the addition of a small resistor ( $50 \Omega-100 \Omega$ ) in series with the op amp's output, and a capacitor ( $5 \mathrm{pF}-10 \mathrm{pF}$ ) from inverting input to output pins, returns the phase margin to a safe value without interfering with lower-frequency circuit operation. Thus, larger values of capacitance can be tolerated without oscillation. Note that in all cases, the output will ring heavily when the load capacitance is near the threshold for oscillation.


Capacitive load driving capability is enhanced by using a pull up resistor to $\mathrm{V}^{+}$(Figure 10b). Typically a pull up resistor conducting $500 \mu \mathrm{~A}$ or more will significantly improve capacitive load responses. The value of the pull up resistor must be determined based on the current sinking capability of the amplifier with respect to the desired output swing. Open loop gain of the amplifier can also be affected by the pull up resistor (see Electrical Characteristics).


TL/H/12830-6
FIGURE 10b. Compensating for Large Capacitive Loads with a Pull Up Resistor

FIGURE 10a. Rx, Cx Improve Capacitive Load Tolerance

Physical Dimensions inches (millimeters) unless othervise noted


8-Lead ( $0.150^{\prime \prime}$ Wide) Molded
Small Outline Package, JEDEC
Order Number LMC6035IM or LMC6035IMX
NS Package Number M08A

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)


8-Lead ( $0.150^{\prime \prime}$ Wide) Molded
Mini Small Outline Package, JEDEC Order Number LMC6035IMM or LMC6035IMMX NS Package Number MA08D


## LMC6574 Quad/LMC6572 Dual Low Voltage (2.7V and 3V) Operational Amplifier

## General Description

Low voltage operation and low power dissipation make the LMC6574/2 ideal for battery-powered systems.
3 V amplifier performance is backed by 2.7 V guarantees to ensure operation throughout battery lifetime. These guarantees also enable analog circuits to operate from the same 3.3 V supply used for digital logic.

Battery life is maximized because each amplifier dissipates only micro-watts of power.
The LMC6574/2 does not sacrifice functionality for low voltage operation. The LMC6574/2 generates 120 dB of openloop gain just like a conventional amplifier, but the LMC6574/2 can do this from a 2.7 V supply.
These amplifiers are designed with features that optimize low voltage operation. The output voltage swings rail-to-rail to maximize signal-to-noise ratio and dynamic signal range. The common-mode input voltage range extends from 800 mV below the positive supply to 100 mV below ground. This device is built with National's advanced Double-Poly Silicon-Gate CMOS process.
LMC6572 is also available in MSOP package which is almost half the size of a SO-8 device.

## Connection Diagrams



TL/H/11934-1
Order Number LMC6572AIN, LMC6572BIN, LMC6572AIM, LMC6572BIM or LMC6572BIMM See NS Package Number N08E, M08A or MA08D

Features (Typical unless otherwise noted)
■ Guaranteed 2.7V and 3V Performance

- Rail-to-Rail Output Swing (within 5 mV of supply rail, $100 \mathrm{k} \Omega$ load)
- Ultra-Low Supply Current $40 \mu \mathrm{~A} /$ Amplifier
- Low Cost
- Ultra-Low Input Current

20 fA

- High Voltage Gain @ $\mathrm{V}_{\mathrm{S}}=2.7 \mathrm{~V}, \mathrm{R}_{\mathrm{L}}=100 \mathrm{k} \Omega 120 \mathrm{~dB}$
- Specified for $100 \mathrm{k} \Omega$ and $5 \mathrm{k} \Omega$ loads
- Available in MSOP Package


## Applications

- Transducer Amplifier
- Portable or Remote Equipment
- Battery-Operated Instruments
- Data Acquisition Systems
- Medical Instrumentation
- Improved Replacement for TLV2322 and TLV2324

| Package | Temperature Range <br> Industrial, $\mathbf{- 4 0} \mathbf{o}^{\circ} \mathbf{C}$ to $+\mathbf{8 5}{ }^{\circ} \mathbf{C}$ | NSC Drawing | Transport <br> Media |
| :--- | :--- | :---: | :---: |
| 8-Pin Molded DIP | LMC6572AIN, LMC6572BIN |  | Rail |
| 8-Pin Small Outline | LMC6572AIM, LMC6572BIM | M08A | Rail |
|  | LMC6572AIMX, LMC6572BIMX |  | Tape and Reel |
| 8-Pin Mini SO | LMC6572BIMM | MA08D | Rail |
|  | LMC6572BIMMX |  | Tape and Reel |
| 14-Pin Molded DIP | LMC6574AIN, LMC6574BIN | N14A | Rail |
| 14-Pin Small Outline | LMC6574AIM, LMC6574BIM |  | Rail |
|  | LMC6574AIMX, LMC6574BIMX |  | Tape and Reel |




| 2.7V AC Electrical Characteristics <br> Unless otherwise specified, all limits guaranteed for $\mathrm{T}_{\mathrm{J}}=25^{\circ} \mathrm{C}, \mathrm{V}^{+}=2.7 \mathrm{~V}, \mathrm{~V}^{-}=0 \mathrm{~V}, \mathrm{~V}_{\mathrm{CM}}=\mathrm{V}_{\mathrm{O}}=\mathrm{V}^{+} / 2$ and $\mathrm{R}_{\mathrm{L}}>1 \mathrm{M} \Omega$. <br> Boldface limits apply at the temperature extremes. |  |  |  |  |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| Symbol | Parameter | Conditions | Typ <br> (Note 5) | LMC6574AI <br> LMC6572AI <br> Limit <br> (Note 6) | LMC6574B <br> LMC6572B <br> Limit <br> (Note 6) | Units |
| SR | Slew Rate | $\mathrm{V}^{+}=2.7 \mathrm{~V} \text { and } 3 \mathrm{~V}$ <br> (Note 8) | 90 | $\begin{aligned} & 30 \\ & 10 \end{aligned}$ | $\begin{aligned} & 30 \\ & 10 \end{aligned}$ | $\mathrm{V} / \mathrm{ms}$ <br> Min |
| GBW | Gain-Bandwidth Product | $\mathrm{V}^{+}=3 \mathrm{~V}$ | 0.22 |  |  | MHz |
| $\phi_{\mathrm{m}}$ | Phase Margin |  | 60 |  |  | Deg |
| $\mathrm{G}_{\mathrm{m}}$ | Gain Margin |  | 12 |  |  | dB |
|  | Amp-to-Amp Isolation | (Note 9) | 120 |  |  | dB |
| $\mathrm{e}_{\mathrm{n}}$ | Input-Referred Voltage Noise | $\begin{aligned} & \mathrm{F}=1 \mathrm{kHz} \\ & \mathrm{~V}_{\mathrm{CM}}=1 \mathrm{~V} \end{aligned}$ | 45 |  |  | $\mathrm{nV} / \sqrt{\mathrm{Hz}}$ |
| $\mathrm{i}_{\mathrm{n}}$ | Input-Referred Current Noise | $\mathrm{F}=1 \mathrm{kHz}$ | 0.002 |  |  | $\mathrm{pA} / \sqrt{\mathrm{Hz}}$ |
| T.H.D. | Total Harmonic Distortion | $\begin{aligned} & \mathrm{F}=10 \mathrm{kHz}, \mathrm{~A}_{\mathrm{V}}=-2 \\ & \mathrm{R}_{\mathrm{L}}=10 \mathrm{k} \Omega, \mathrm{~V}_{\mathrm{O}}=1.0 \mathrm{~V} \mathrm{PP} \end{aligned}$ | 0.05 |  |  | \% |
| Note 4: The maximum power dissipation is a function of $T_{J(\operatorname{Max})}, \theta_{\mathrm{JA}}$, and $T_{A}$. The maximum allowable power dissipation at any ambient temperature is $P_{D}=\left(T_{J(\operatorname{Max})}-T_{A}\right) / \theta_{J A}$. All numbers apply for packages soldered directly into a PC board. <br> Note 5: Typical values represent the most likely parametric norm. <br> Note 6: All limits are guaranteed by testing or statistical analysis. <br> Note 7: $\mathrm{V}^{+}=3 \mathrm{~V}, \mathrm{~V}_{\mathrm{CM}}=1.5 \mathrm{~V}$ and $\mathrm{R}_{\mathrm{L}}$ connected to 1.5 V . For Sourcing tests, $1.5 \mathrm{~V} \leq \mathrm{V}_{\mathrm{O}} \leq 2.5 \mathrm{~V}$. For Sinking tests, $0.5 \mathrm{~V} \leq \mathrm{V}_{\mathrm{O}} \leq 1.5 \mathrm{~V}$. <br> Note 8: Connected as Voltage Follower with 1.0 V step input. Number specified is the slower of the positive and negative slew rates. <br> Note 9: Input referred, $\mathrm{V}^{+}=3 \mathrm{~V}$ and $\mathrm{R}_{\mathrm{L}}=100 \mathrm{k} \Omega$ connected to 1.5 V . Each amp excited in turn with 1 KHz to produce $\mathrm{V}_{\mathrm{O}}=2 \mathrm{~V}_{\mathrm{Pp}}$. |  |  |  |  |  |  |

Typical Performance Characteristics $\mathrm{v}_{\mathrm{S}}=+3 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$, Unless otherwise specified





Crosstalk Rejection vs Frequency




Positive PSRR vs


Input Voltage vs
Output Voltage ( $\mathbf{V}_{\mathbf{S}}= \pm \mathbf{1 . 5}$ )






## Typical Performance Characteristics (Continued) $\mathrm{V}_{\mathrm{S}}=+3 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$, Unless otherwise specified





## Applications Hints

### 1.0 LOW VOLTAGE AMPLIFIER TOPOLOGY

The LMC6574/2 incorporates a novel op-amp design topology that enables it to maintain rail-to-rail output swing even when driving a large load. Instead of relying on a push-pull unity gain output buffer stage, the output stage is taken directly from the internal integrator, which provides both low output impedance and large gain. Special feed-forward compensation design techniques are incorporated to maintain stability over a wider range of operating conditions than traditional micropower op-amps. These features make the LMC6574/2 both easier to design with, and provide higher speed than products typically found in this ultra-low power class.

### 2.0 COMPENSATING FOR INPUT CAPACITANCE

It is quite common to use large values of feedback resistance for amplifiers with ultra-low input current, like the LMC6574/2.

Although the LMC6574/2 is highly stable over a wide range of operating conditions, a large feedback resistor will react even with small values of capacitance at the input of the opamp to reduce phase margin. The capacitance at the input of the op-amp comes from transducers, photodiodes and circuit board parasitics.
The effect of input capacitance can be compensated for by adding a capacitor, $\mathrm{C}_{\mathrm{f}}$, around the feedback resistors (as in Figure 1 ) such that:

$$
\begin{gathered}
\frac{1}{2 \pi \mathrm{R}_{1} \mathrm{C}_{\mathrm{IN}}} \geq \frac{1}{2 \pi \mathrm{R}_{2} \mathrm{C}_{\mathrm{f}}} \\
\text { or } \\
\mathrm{R}_{1} \mathrm{C}_{\mathrm{IN}} \leq \mathrm{R}_{2} \mathrm{C}_{\mathrm{f}}
\end{gathered}
$$

Since it is often difficult to know the exact value of $\mathrm{C}_{\mathrm{IN}}, \mathrm{C}_{\mathrm{f}}$ can be experimentally adjusted so that the desired pulse response is achieved. Refer to the LMC660 and LMC662 for a more detailed discussion on compensating for input capacitance.
When high input impedances are demanded, guarding of the LMC6574/2 is suggested. Guarding input lines will not only reduce leakage, but lowers stray input capacitance as well. (See Printed-Circuit-Board Layout for High Impedance Work).


TL/H/11934-6
FIGURE 1. Cancelling the Effect of Input Capacitance 3.0 CAPACITIVE LOAD TOLERANCE

Direct capacitive loading will reduce the phase margin of many op-amps. A pole in the feedback loop is created by the combination of the op-amp's output impedance and the capacitive load. This pole induces phase lag at the unitygain crossover frequency of the amplifier resulting in either an oscillatory or underdamped pulse response. With a few external components, op amps can easily indirectly drive capacitive loads, as shown in Figure 2.


FIGURE 2. LMC6574/2 Noninverting Gain of 10 Amplifier, Compensated to Handle Capacitive Loads
In the circuit of Figure 2, R1 and C1 serve to counteract the loss of phase margin by feeding the high frequency component of the output signal back to the amplifier's inverting input, thereby preserving phase margin in the overall feedback loop.

## Applications Hints (Continued)

### 4.0 PRINTED-CIRCUIT-BOARD LAYOUT FOR HIGH-IMPEDANCE WORK

It is generally recognized that any circuit which must operate with less than 1000 pA of leakage current requires special layout of the PC board. When one wishes to take advantage of the ultra-low bias current of the LMC6574/2, typically less than 20 fA , it is essential to have an excellent layout. Fortunately, the techniques of obtaining low leakages are quite simple. First, the user must not ignore the surface leakage of the PC board, even though it may sometimes appear acceptably low, because under conditions of high humidity or dust or contamination, the surface leakage will be appreciable.
To minimize the effect of any surface leakage, lay out a ring of foil completely surrounding the LMC6574/2's inputs and the terminals of capacitors, diodes, conductors, resistors, relay terminals, etc. connected to the op-amp's inputs, as in Figure 3. To have a significant effect, guard rings should be placed on both the top and bottom of the PC board. This PC foil must then be connected to a voltage which is at the same voltage as the amplifier inputs, since no leakage current can flow between two points at the same potential. For example, a PC board trace-to-pad resistance of $10^{12} \Omega$, which is normally considered a very large resistance, could leak 5 pA if the trace were a 5 V bus adjacent to the pad of the input. This would cause a 250 times degradation from the LMC6574/2's actual performance. However, if a guard ring is held within 5 mV of the inputs, then even a resistance of $1011 \Omega$ would cause only 0.05 pA of leakage current. See Figures $4 a, 4 b, 4 c$ for typical connections of guard rings for standard op-amp configurations.


TL/H/11934-8
FIGURE 3. Example of Guard Ring in P.C. Board Layout

(a) Inverting Amplifier

(b) Non-Inverting Amplifier

(c) Follower

## FIGURE 4. Typical Connections of Guard Rings

The designer should be aware that when it is inappropriate to lay out a PC board for the sake of just a few circuits, there is another technique which is even better than a guard ring on a PC board: Don't insert the amplifier's input pin into the board at all, but bend it up in the air and use only air as an insulator. Air is an excellent insulator. In this case you may have to forego some of the advantages of PC board construction, but the advantages are sometimes well worth the effort of using point-to-point up-in-the-air wiring. See Figure 5.

(Input pins are lifted out of PC board and soldered directly to components. All other pins connected to PC board).

FIGURE 5. Air Wiring

## Applications Hints (Continued)

### 5.0 SPICE MACROMODEL

A spice macromodel is available for the LMC6574/2. This model includes accurate simulation of:

- input common-mode voltage range
- frequency and transient response
- GBW dependence on loading conditions
- quiescent and dynamic supply current
- output swing dependence on loading conditions
and many more characteristics as listed on the macromodel disk.
Contact your local National Semiconductor sales office to obtain an operational amplifier spice model library disk.


TL/H/11934-15
FIGURE 8. 1 Hz Square Wave Oscillator

## Typical Single-Supply Applications



FIGURE 6. Low-Power Two-Op-Amp Instrumentation Amplifier


FIGURE 7. Sample and Hold

$V_{\text {OUT }}=V_{1}+V_{2}-V_{3}-V_{4}$
TL/H/11934-16
FIGURE 9. Adder/Subtractor Circuit


FIGURE 10. Low Pass Filter

Physical Dimensions inches (millimeters) unless otherwise noted


Physical Dimensions inches (millimeters) unless otherwise noted (Continued)


8-Lead Mini-Small Outline Molded Package, JEDEC Order Number LMC6572BIMM or LMC6572BIMMX NS Package Number MA08D


8-Pin Molded Dual-In-Line Package Order Number LMC6572AIN or LMC6572BIN

NS Package Number N08E


National Semiconductor

## General Description

The LMC6582/4 is a high performance operational amplifier which can operate over a wide range of supply voltages with guaranteed specifications at $1.8 \mathrm{~V}, 2.2 \mathrm{~V}, 3 \mathrm{~V}, 5 \mathrm{~V}$, and 10 V .
The LMC6582/4 provides an input common-mode voltage range that exceeds both supplies. The rail-to-rail output swing of the amplifier assures maximum dynamic signal range. This rail-to-rail performance of the amplifier, combined with its high open-loop voltage gain makes it unique among rail-to-rail CMOS amplifiers. The LMC6582/4 is an excellent choice for circuits where the input common-mode voltage range is a concern.
The LMC6582/4 has been designed specifically to improve system performance in low voltage applications. Guaranteed operation down to 1.8 V means that this family of amplifiers can operate at the end of discharge (EOD) voltages of several popular batteries. The amplifier's 80 fA input current, 0.5 mV offset voltage, and 82 dB CMRR maintain accuracy in battery-powered systems.
For a single, dual or quad CMOS amplifier with similar specs and a powerdown mode, refer to the LMC6681/2/4 datasheet.

## Connection Diagrams



Top View


TL/H/12041-2
Top View
Ordering Information

| Package | Temperature Range <br> Industrial, $\mathbf{- 4 0 ^ { \circ }} \mathbf{C}$ to $+\mathbf{8 5}^{\circ} \mathbf{C}$ | NSC <br> Drawing | Transport <br> Media |
| :--- | :--- | :---: | :---: |
| 8-pin Molded DIP | LMC6582AIN, LMC6582BIN | N08E | Rails |
| 8-pin Small Outline | LMC6582AIM, LMC6582BIM <br> LMC6582AIMX, LMC6582BIMX | M08A <br> M08A | Rails <br> Tape and Reel |
| 14-pin Molded DIP | LMC6584AIN, LMC6584BIN | N14A | Rails |
| 14-pin Small Outline | LMC6584AIM, LMC6584BIM | M14A <br> LMC6584AIMX, LMC6584BIMX | Rails <br> Tape and Reel |

Absolute Maximum Ratings (Note 1)
If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.
ESD Tolerance (Note 2)
Differential Input Voltage
Voltage at Input/Output Pin
Supply Voltage ( $\mathrm{V}^{+}-\mathrm{V}^{-}$)
Current at Input Pin (Note 11)
Current at Output Pin (Note 3)
Current at Power Supply Pin
Lead Temp. (soldering, 10 sec .)
2 kV
$\pm$ Supply Voltage
$\left(\mathrm{V}^{+}\right)+0.3 \mathrm{~V},\left(\mathrm{~V}^{-}\right)-0.3 \mathrm{~V}$
12 V
$\pm 5 \mathrm{~mA}$
$\pm 30 \mathrm{~mA}$
35 mA
$260^{\circ} \mathrm{C}$
Storage Temperature Range $-65^{\circ} \mathrm{C}$ to $+150^{\circ} \mathrm{C}$
Junction Temperature (Note 4)

## 3V DC Electrical Characteristics

Unless otherwise specified, all limits guaranteed for $T_{J}=25^{\circ} \mathrm{C}, \mathrm{V}+=3.0 \mathrm{~V}, \mathrm{~V}^{-}=0 \mathrm{~V}, \mathrm{~V}_{\mathrm{CM}}=\mathrm{V}_{\mathrm{O}}=\mathrm{V}+/ 2$ and $\mathrm{R}_{\mathrm{L}}>1 \mathrm{M} \Omega$. Boldface limits apply at the temperature extremes.

| Symbol | Parameter | Conditions | Typ (Note 5) | LMC6582AI <br> LMC6584AI <br> Limit <br> (Note 6) | LMC6582BI <br> LMC6584BI <br> Limit <br> (Note 6) | Units |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| $\mathrm{V}_{\text {OS }}$ | Input Offset Voltage |  | 0.5 | $\begin{gathered} 1 \\ 2.5 \end{gathered}$ | $\begin{gathered} 3 \\ 4.5 \end{gathered}$ | mV max |
| TCV ${ }_{\text {OS }}$ | Input Offset Voltage <br> Average Drift |  | 1.5 |  |  | $\mu \mathrm{V} /{ }^{\circ} \mathrm{C}$ |
| $\mathrm{I}_{\mathrm{B}}$ | Input Current | (Note 12) | 0.08 | 20 | 20 | pA max |
| los | Input Offset Current | (Note 12) | 0.04 | 10 | 10 | pA max |
| $\mathrm{R}_{\text {IN }}$ | Input Resistance |  | $>1$ |  |  | Tera $\Omega$ |
| $\mathrm{C}_{\text {IN }}$ | Input Capacitance |  | 3 |  |  | pF |
| CMRR | Common Mode Rejection Ratio | (Note 13) | 82 | $\begin{aligned} & 70 \\ & 65 \end{aligned}$ | $\begin{aligned} & 65 \\ & 62 \end{aligned}$ | $\begin{gathered} \mathrm{dB} \\ \mathrm{~min} \end{gathered}$ |
| PSRR | Power Supply <br> Rejection Ratio | $\begin{aligned} & \pm 1.5 \mathrm{~V} \leq \mathrm{V}_{\mathrm{S}} \leq \pm 2.5 \mathrm{~V} \\ & \mathrm{~V}_{\mathrm{O}}=\mathrm{V}+/ 2=\mathrm{V}_{\mathrm{CM}} \end{aligned}$ | 82 | $\begin{aligned} & 70 \\ & 65 \end{aligned}$ | $\begin{aligned} & 65 \\ & \mathbf{6 2} \end{aligned}$ | $\begin{gathered} \mathrm{dB} \\ \mathrm{~min} \end{gathered}$ |
| $\mathrm{V}_{\mathrm{CM}}$ | Input Common Mode Voltage Range | CMRR > 50 dB | 3.23 | $\begin{aligned} & 3.18 \\ & \mathbf{3 . 0 0} \\ & \hline \end{aligned}$ | $\begin{aligned} & 3.18 \\ & \mathbf{3 . 0 0} \end{aligned}$ | $\begin{gathered} \mathrm{V} \\ \mathrm{~min} \end{gathered}$ |
|  |  |  | -0.3 | $\begin{aligned} & -0.18 \\ & \mathbf{0 . 0 0} \end{aligned}$ | $\begin{aligned} & -0.18 \\ & \mathbf{0 . 0 0} \end{aligned}$ | $\begin{gathered} \mathrm{V} \\ \max \end{gathered}$ |
| $A_{V}$ | Large Signal Voltage Gain | $R_{L}=600 \Omega$ (Notes 7, 12) | 70 | 10 | 10 | $\mathrm{V} / \mathrm{mV}$ |
|  |  | $\mathrm{R}_{\mathrm{L}}=10 \mathrm{k} \Omega$ (Notes 7, 12) | 1000 | 12 | 12 | $\mathrm{V} / \mathrm{mV}$ |

3V DC Electrical Characteristics (Continued)
Unless otherwise specified, all limits guaranteed for $T_{J}=25^{\circ} \mathrm{C}, \mathrm{V}^{+}=3.0 \mathrm{~V}, \mathrm{~V}^{-}=0 \mathrm{~V}, \mathrm{~V}_{\mathrm{CM}}=\mathrm{V}_{\mathrm{O}}=\mathrm{V}^{+} / 2$ and $\mathrm{R}_{\mathrm{L}}>1 \mathrm{M} \Omega$. Boldface limits apply at the temperature extremes.

| Symbol | Parameter | Conditions | Typ <br> (Note 5) | $\begin{aligned} & \text { LMC6582AI } \\ & \text { LMC6584AI } \\ & \text { Limit } \\ & \text { (Note 6) } \\ & \hline \end{aligned}$ | LMC6582BI <br> LMC6584BI Limit (Note 6) | Units |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| $\mathrm{V}_{0}$ | Output Swing | $\mathrm{R}_{\mathrm{L}}=600 \Omega$ to $\mathrm{V}+/ 2$ | 2.87 | $\begin{aligned} & 2.70 \\ & 2.58 \end{aligned}$ | $\begin{aligned} & 2.70 \\ & 2.58 \end{aligned}$ | $\begin{gathered} \mathrm{V} \\ \mathrm{~min} \end{gathered}$ |
|  |  |  | 0.15 | $\begin{gathered} 0.3 \\ \mathbf{0 . 4 2} \end{gathered}$ | $\begin{gathered} 0.3 \\ \mathbf{0 . 4 2} \end{gathered}$ | $\begin{gathered} V \\ \max \end{gathered}$ |
|  |  | $\mathrm{R}_{\mathrm{L}}=2 \mathrm{k} \Omega$ to $\mathrm{V}+/ 2$ | 2.95 | $\begin{gathered} 2.85 \\ \mathbf{2 . 7 9} \end{gathered}$ | $\begin{gathered} 2.85 \\ \mathbf{2 . 7 9} \end{gathered}$ | $\begin{gathered} \mathrm{V} \\ \mathrm{~min} \end{gathered}$ |
|  |  |  | 0.05 | $\begin{aligned} & 0.15 \\ & \mathbf{0 . 2 1} \end{aligned}$ | $\begin{aligned} & 0.15 \\ & \mathbf{0 . 2 1} \end{aligned}$ | $\begin{gathered} \mathrm{V} \\ \max \end{gathered}$ |
|  |  | $\mathrm{R}_{\mathrm{L}}=10 \mathrm{k} \Omega$ to $\mathrm{V}+/ 2$ | 2.99 | $\begin{array}{r} 2.94 \\ \mathbf{2 . 9 1} \end{array}$ | $\begin{array}{r} 2.94 \\ \mathbf{2 . 9 1} \\ \hline \end{array}$ | $\begin{gathered} V \\ \mathrm{~min} \end{gathered}$ |
|  |  |  | 0.01 | $\begin{aligned} & 0.04 \\ & \mathbf{0 . 0 5} \end{aligned}$ | $\begin{aligned} & 0.04 \\ & \mathbf{0 . 0 5} \end{aligned}$ | $\begin{gathered} \mathrm{V} \\ \max \\ \hline \end{gathered}$ |
| ISC | Output Short Circuit Current | Sourcing, $\mathrm{V}_{\mathrm{O}}=0 \mathrm{~V}$ | 20 | $\begin{aligned} & 9.0 \\ & 6.7 \end{aligned}$ | $\begin{aligned} & 9.0 \\ & 6.7 \end{aligned}$ | $\begin{aligned} & \mathrm{mA} \\ & \mathrm{~min} \end{aligned}$ |
|  |  | Sinking, $\mathrm{V}_{\mathrm{O}}=3 \mathrm{~V}$ | 12 | $\begin{aligned} & \hline 6.0 \\ & 4.5 \end{aligned}$ | $\begin{aligned} & \hline 6.0 \\ & 4.5 \end{aligned}$ | $\mathrm{mA}$ $\min$ |
| Is | Supply Current | Dual, LMC6582 $\mathrm{V}_{\mathrm{CM}}=1.5 \mathrm{~V}$ | 1.4 | $\begin{gathered} 2.26 \\ \mathbf{2 . 7 5} \end{gathered}$ | $\begin{aligned} & 2.26 \\ & \mathbf{2 . 7 5} \end{aligned}$ | mA <br> max |
|  |  | Quad, LMC6584 $\mathrm{V}_{\mathrm{CM}}=1.5 \mathrm{~V}$ | 2.8 | $\begin{gathered} 4.52 \\ \mathbf{5 . 4 2} \end{gathered}$ | $\begin{gathered} 4.52 \\ \mathbf{5 . 4 2} \end{gathered}$ | mA <br> max |

### 1.8 V and 2.2V DC Electrical Characteristics

Unless otherwise specified, all limits guaranteed for $\mathrm{T}_{\mathrm{J}}=25^{\circ} \mathrm{C}, \mathrm{V}^{+}=1.8 \mathrm{~V}$ and $2.2 \mathrm{~V}, \mathrm{~V}^{-}=0 \mathrm{~V}, \mathrm{~V}_{\mathrm{CM}}=\mathrm{V}_{\mathrm{O}}=\mathrm{V}+/ 2$ and $\mathrm{R}_{\mathrm{L}}>1 \mathrm{M} \Omega$. Boldface limits apply at the temperature extremes.

| Symbol | Parameter | Conditions | $\begin{gathered} \text { Typ } \\ \text { (Note 5) } \end{gathered}$ | LMC6582AI <br> LMC6584AI Limit (Note 6) | LMC6582BI <br> LMC6584BI Limit (Note 6) | Units |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| $\mathrm{V}_{\text {OS }}$ | Input Offset Voltage | $\mathrm{V}^{+}=1.8 \mathrm{~V}, \mathrm{~V}_{\mathrm{CM}}=1.5 \mathrm{~V}$ | 0.5 | 3 | 10 | $\mathrm{mV}$ <br> max |
|  |  | $\mathrm{V}^{+}=2.2 \mathrm{~V}, \mathrm{~V}_{\mathrm{CM}}=1.5 \mathrm{~V}$ | 0.5 | $\begin{gathered} 2 \\ 3.8 \end{gathered}$ | $\begin{gathered} 6 \\ 7.8 \end{gathered}$ | mV <br> max |
| TCV ${ }_{\text {os }}$ | Input Offset Voltage Average Drift | $\mathrm{V}^{+}=2.2 \mathrm{~V}$ | 1.5 |  |  | $\mu \mathrm{V} /{ }^{\circ} \mathrm{C}$ |
| $\mathrm{I}_{\mathrm{B}}$ | Input Current | $\mathrm{V}^{+}=2.2 \mathrm{~V}$ (Note 12) | 0.08 | 20 | 20 | pA max |
| l OS | Input Offset Current | $\mathrm{V}^{+}=2.2 \mathrm{~V}$ (Note 12) | 0.04 | 10 | 10 | pA max |
| CMRR | Common Mode Rejection Ratio | $\mathrm{V}^{+}=2.2 \mathrm{~V}$, (Note 13) | 82 | 60 | 60 | dB min |
|  |  | $\mathrm{V}^{+}=1.8 \mathrm{~V}$, (Note 13) | 82 | 50 | 50 | dB min |
| PSRR | Power Supply Rejection Ratio | $\begin{aligned} & \pm 1.1 \mathrm{~V} \leq \mathrm{V}_{\mathrm{S}} \leq \pm 5 \mathrm{~V} \\ & \mathrm{~V}_{\mathrm{O}}=\mathrm{V}+/ 2=\mathrm{V}_{\mathrm{CM}} \end{aligned}$ | 82 | $\begin{array}{r} 70 \\ 65 \\ \hline \end{array}$ | $\begin{aligned} & 65 \\ & 62 \end{aligned}$ | $\begin{aligned} & \mathrm{dB} \\ & \mathrm{~min} \\ & \hline \end{aligned}$ |
| $\mathrm{V}_{\mathrm{CM}}$ | Input Common Mode Voltage Range | $\begin{aligned} & \mathrm{V}^{+}=2.2 \mathrm{~V} \\ & \mathrm{CMRR}>40 \mathrm{~dB} \end{aligned}$ | 2.38 | 2.2 | 2.2 | $V$ min |
|  |  |  | -0.15 | 0.0 | 0.0 | $V$ max |
|  |  | $\begin{aligned} & \mathrm{V}^{+}=1.8 \mathrm{~V} \\ & \mathrm{CMRR}>40 \mathrm{~dB} \end{aligned}$ | 1.98 | 1.8 | 1.8 | $V_{\text {min }}$ |
|  |  |  | -0.10 | 0.0 | 0.0 | $\checkmark$ max |

### 1.8V and 2.2V DC Electrical Characteristics

Unless otherwise specified, all limits guaranteed for $\mathrm{T}_{\mathrm{J}}=25^{\circ} \mathrm{C}, \mathrm{V}+=1.8 \mathrm{~V}$ and $2.2 \mathrm{~V}, \mathrm{~V}^{-}=0 \mathrm{~V}, \mathrm{~V}_{\mathrm{CM}}=\mathrm{V}_{\mathrm{O}}=\mathrm{V}^{+} / 2$ and $\mathrm{R}_{\mathrm{L}}>$ $1 \mathrm{M} \Omega$. Boldface limits apply at the temperature extremes.

| Symbol | Parameter | Conditions | Typ (Note 5) | LMC6582AI <br> LMC6584AI <br> Limit <br> (Note 6) | LMC6582BI LMC6584BI Limit (Note 6) | Units |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| $\mathrm{V}_{0}$ | Output Swing | $\begin{aligned} & \mathrm{V}^{+}=2.2 \mathrm{~V} \\ & \mathrm{R}_{\mathrm{L}}=2 \mathrm{k} \Omega \text { to } \mathrm{V}+/ 2 \end{aligned}$ | 2.15 | $\begin{gathered} 2.0 \\ 1.88 \end{gathered}$ | $\begin{gathered} 2.0 \\ 1.88 \end{gathered}$ | $\begin{gathered} \mathrm{V} \\ \mathrm{~min} \end{gathered}$ |
|  |  |  | 0.05 | $\begin{gathered} 0.2 \\ \mathbf{0 . 3 2} \end{gathered}$ | $\begin{gathered} 0.2 \\ \mathbf{0 . 3 2} \end{gathered}$ | $\begin{gathered} \mathrm{V} \\ \max \end{gathered}$ |
|  |  | $\begin{aligned} & \mathrm{V}^{+}=1.8 \mathrm{~V} \\ & \mathrm{R}_{\mathrm{L}}=2 \mathrm{k} \Omega \text { to } \mathrm{V}+/ 2 \end{aligned}$ | 1.75 | $\begin{gathered} 1.6 \\ 1.44 \end{gathered}$ | $\begin{gathered} 1.6 \\ 1.44 \end{gathered}$ | $\begin{gathered} \mathrm{V} \\ \mathrm{~min} \end{gathered}$ |
|  |  |  | 0.05 | $\begin{gathered} 0.2 \\ \mathbf{0 . 3 6} \end{gathered}$ | $\begin{gathered} 0.2 \\ \mathbf{0 . 3 6} \end{gathered}$ | $\begin{gathered} \mathrm{V} \\ \max \end{gathered}$ |
| Is | Supply Current | Dual, LMC6582 $\mathrm{V}_{\mathrm{CM}}=1.5 \mathrm{~V}$ | 1.4 | $\begin{aligned} & 2.2 \\ & 2.7 \end{aligned}$ | $\begin{aligned} & 2.2 \\ & \mathbf{2 . 7} \end{aligned}$ | $\mathrm{mA}$ $\max$ |
|  |  | Quad, LMC6584 $\mathrm{V}_{\mathrm{CM}}=1.5 \mathrm{~V}$ | 2.8 | $\begin{aligned} & 4.4 \\ & 5.3 \end{aligned}$ | $\begin{aligned} & 4.4 \\ & 5.3 \end{aligned}$ | mA <br> max |

## 5V DC Electrical Characteristics

Unless otherwise specified, all limits guaranteed for $\mathrm{T}_{\mathrm{J}}=25^{\circ} \mathrm{C}, \mathrm{V}^{+}=5.0 \mathrm{~V}, \mathrm{~V}^{-}=0 \mathrm{~V}, \mathrm{~V}_{\mathrm{CM}}=\mathrm{V}_{\mathrm{O}}=\mathrm{V}^{+} / 2$ and $\mathrm{R}_{\mathrm{L}}>1 \mathrm{M} \Omega$.
Boldface limits apply at the temperature extremes.

| Symbol | Parameter | Conditions | Typ (Note 5) | LMC6582AI <br> LMC6584AI <br> Limit <br> (Note 6) | LMC6582BI <br> LMC6584BI Limit (Note 6) | Units |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| $\mathrm{V}_{\text {OS }}$ | Input Offset Voltage | $\mathrm{V}_{\mathrm{CM}}=1.5 \mathrm{~V}$ | 0.5 | $\begin{gathered} 1 \\ 2.5 \end{gathered}$ | $\begin{gathered} 3 \\ 4.5 \end{gathered}$ | $\mathrm{mV}$ $\max$ |
| TCV ${ }_{\text {OS }}$ | Input Offset Voltage Average Drift |  | 1.5 |  |  | $\mu \mathrm{V} /{ }^{\circ} \mathrm{C}$ |
| $\mathrm{I}_{\mathrm{B}}$ | Input Current | (Note 12) | 0.08 | 20 | 20 | pA max |
| los | Input Offset Current | (Note 12) | 0.04 | 10 | 10 | pA max |
| $\mathrm{R}_{\text {IN }}$ | Input Resistance |  | $>1$ |  |  | Tera $\Omega$ |
| $\mathrm{C}_{\text {IN }}$ | Input Capacitance |  | 3 |  |  | pF |
| CMRR | Common Mode Rejection Ratio | (Note 13) | 82 | $\begin{array}{r} 70 \\ \mathbf{6 5} \\ \hline \end{array}$ | $\begin{array}{r} 65 \\ \mathbf{6 2} \\ \hline \end{array}$ | $\begin{gathered} \mathrm{dB} \\ \mathrm{~min} \\ \hline \end{gathered}$ |
| PSRR | Power Supply <br> Rejection Ratio | $\begin{aligned} & \pm 1.5 \mathrm{~V} \leq \mathrm{V}_{\mathrm{S}} \leq \pm 2.5 \mathrm{~V}, \\ & \mathrm{~V}_{\mathrm{O}}=\mathrm{V}+/ 2=\mathrm{V}_{\mathrm{CM}} \end{aligned}$ | 82 | $\begin{array}{r} 70 \\ \mathbf{6 5} \\ \hline \end{array}$ | $\begin{aligned} & 65 \\ & 62 \end{aligned}$ | $\begin{gathered} \mathrm{dB} \\ \mathrm{~min} \\ \hline \end{gathered}$ |
| $\mathrm{V}_{\mathrm{CM}}$ | Input Common Mode Voltage Range | CMRR $>50 \mathrm{~dB}$ | 5.3 | $\begin{array}{r} 5.18 \\ \mathbf{5 . 0 0} \\ \hline \end{array}$ | $\begin{array}{r} 5.18 \\ \mathbf{5 . 0 0} \\ \hline \end{array}$ | $\begin{gathered} \mathrm{V} \\ \mathrm{~min} \end{gathered}$ |
|  |  |  | -0.3 | $\begin{aligned} & -0.18 \\ & \mathbf{0 . 0 0} \end{aligned}$ | $\begin{aligned} & -0.18 \\ & \mathbf{0 . 0 0} \end{aligned}$ | $\underset{\operatorname{lax}}{ }$ |
| $\mathrm{V}_{\mathrm{O}}$ | Output Swing | $R_{L}=2 \mathrm{k} \Omega$ to $\mathrm{V}^{+} / 2$ | 4.9 | $\begin{aligned} & 4.85 \\ & \mathbf{4 . 5 8} \end{aligned}$ | $\begin{aligned} & 4.85 \\ & \mathbf{4 . 5 8} \end{aligned}$ | $\begin{gathered} V \\ \mathrm{~min} \end{gathered}$ |
|  |  |  | 0.05 | $\begin{gathered} 0.2 \\ \mathbf{0 . 2 8} \end{gathered}$ | $\begin{gathered} 0.2 \\ \mathbf{0 . 2 8} \end{gathered}$ | $\begin{gathered} V \\ \max \end{gathered}$ |
| Is | Supply Current | Dual, LMC6582 $V_{C M}=1.5 \mathrm{~V}$ | 1.5 | $\begin{aligned} & 2.48 \\ & \mathbf{3 . 0 0} \\ & \hline \end{aligned}$ | $\begin{array}{r} 2.48 \\ \mathbf{3 . 0 0} \\ \hline \end{array}$ | $\begin{aligned} & \mathrm{mA} \\ & \max \end{aligned}$ |
|  |  | Quad, LMC6584 $\mathrm{V}_{\mathrm{CM}}=1.5 \mathrm{~V}$ | 3.0 | $\begin{aligned} & 4.96 \\ & 6.00 \end{aligned}$ | $\begin{aligned} & 4.96 \\ & 6.00 \end{aligned}$ | mA max |

## 10V DC Electrical Characteristics

Unless otherwise specified, all limits guaranteed for $\mathrm{T}_{\mathrm{J}}=25^{\circ} \mathrm{C}, \mathrm{V}^{+}=10.0 \mathrm{~V}, \mathrm{~V}^{-}=0 \mathrm{~V}, \mathrm{~V}_{\mathrm{CM}}=\mathrm{V}_{\mathrm{O}}=\mathrm{V}^{+} / 2$ and $\mathrm{R}_{\mathrm{L}}>1 \mathrm{M} \Omega$. Boldface limits apply at the temperature extremes.

| Symbol | Parameter | Conditions |  | $\begin{gathered} \text { Typ } \\ \text { (Note 5) } \end{gathered}$ | LMC6582AI <br> LMC6584AI <br> Limit <br> (Note 6) | LMC6582BI <br> LMC6584BI <br> Limit <br> (Note 6) | Units |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| $\mathrm{V}_{\text {OS }}$ | Input Offset Voltage | $\mathrm{V}_{\mathrm{CM}}=1.5 \mathrm{~V}$ |  | 0.5 | $\begin{aligned} & 1.5 \\ & 3.0 \end{aligned}$ | $\begin{aligned} & 3.5 \\ & 5.0 \end{aligned}$ | $\begin{gathered} m V \\ \max \end{gathered}$ |
| TCV ${ }_{\text {OS }}$ | Input Offset Voltage Average Drift |  |  | 1.5 |  |  | $\mu \mathrm{V} /{ }^{\circ} \mathrm{C}$ |
| $\mathrm{I}_{\mathrm{B}}$ | Input Current | (Note 12) |  | 0.08 | 20 | 20 | pA max |
| los | Input Offset Current | (Note 12) |  | 0.04 | 10 | 10 | pA max |
| $\mathrm{R}_{\mathrm{IN}}$ | Input Resistance |  |  | $>1$ |  |  | Tera $\Omega$ |
| $\mathrm{C}_{\text {IN }}$ | Input Capacitance |  |  | 3 |  |  | pF |
| CMRR | Common Mode Rejection Ratio | (Note 13) |  | 82 | $\begin{aligned} & 65 \\ & 62 \end{aligned}$ | $\begin{aligned} & 65 \\ & 62 \end{aligned}$ | $\begin{aligned} & \mathrm{dB} \\ & \mathrm{~min} \end{aligned}$ |
| PSRR | Power Supply Rejection Ratio | $\begin{aligned} & \pm 1.1 \mathrm{~V} \leq \mathrm{V}^{+} \leq \pm 5 \mathrm{~V} \\ & \mathrm{~V}_{\mathrm{O}}=\mathrm{V}+/ 2=\mathrm{V}_{\mathrm{CM}} \end{aligned}$ |  | 82 | $\begin{aligned} & 70 \\ & 65 \end{aligned}$ | $\begin{aligned} & 65 \\ & 62 \end{aligned}$ | $\begin{gathered} \mathrm{dB} \\ \mathrm{~min} \end{gathered}$ |
| $\mathrm{V}_{\mathrm{CM}}$ | Input Common Mode Voltage Range | CMRR $>50 \mathrm{~dB}$ |  | 10.30 | $\begin{gathered} 10.18 \\ \mathbf{1 0 . 0 0} \end{gathered}$ | $\begin{gathered} 10.18 \\ \mathbf{1 0 . 0 0} \end{gathered}$ | $\begin{gathered} \mathrm{V} \\ \mathrm{~min} \end{gathered}$ |
|  |  |  |  | -0.30 | $\begin{aligned} & -0.18 \\ & \mathbf{0 . 0 0} \end{aligned}$ | $\begin{aligned} & -0.18 \\ & \mathbf{0 . 0 0} \end{aligned}$ | $\begin{gathered} \mathrm{V} \\ \max \end{gathered}$ |
| $\mathrm{V}_{0}$ | Output Swing | $\mathrm{R}_{\mathrm{L}}=2 \mathrm{k} \Omega$ to $\mathrm{V}+/ 2$ |  | 9.93 | $\begin{gathered} 9.7 \\ \mathbf{9 . 5 8} \end{gathered}$ | $\begin{gathered} 9.7 \\ \mathbf{9 . 5 8} \end{gathered}$ | $\begin{gathered} \mathrm{V} \\ \mathrm{~min} \end{gathered}$ |
|  |  |  |  | 0.08 | $\begin{gathered} 0.3 \\ \mathbf{0 . 4 2} \end{gathered}$ | $\begin{gathered} 0.3 \\ \mathbf{0 . 4 2} \end{gathered}$ | $\underset{\max }{V}$ |
| $A_{V}$ | Large Signal Voltage Gain | $\mathrm{R}_{\mathrm{L}}=2 \mathrm{k} \Omega \text { to } \mathrm{V}+/ 2$ <br> (Note 12) | Sourcing | 89 | 25 | 25 | $\mathrm{V} / \mathrm{mV}$ |
|  |  |  | Sinking | 224 | 25 | 25 | $\mathrm{V} / \mathrm{mV}$ |
| Isc | Output Short Circuit Current | Sourcing, $\mathrm{V}_{\mathrm{O}}=0 \mathrm{~V}$ <br> (Note 14) |  | 65 | $\begin{aligned} & 30 \\ & 22 \end{aligned}$ | $\begin{aligned} & 30 \\ & 22 \end{aligned}$ | $\begin{aligned} & \mathrm{mA} \\ & \mathrm{~min} \end{aligned}$ |
|  |  | Sinking, $\mathrm{V}_{\mathrm{O}}=10 \mathrm{~V}$ <br> (Note 14) |  | 70 | $\begin{aligned} & 30 \\ & 22 \end{aligned}$ | $\begin{aligned} & 30 \\ & 22 \end{aligned}$ | $\begin{aligned} & \mathrm{mA} \\ & \mathrm{~min} \end{aligned}$ |
| Is | Supply Current | Dual, LMC6582$\mathrm{V}_{\mathrm{CM}}=1.5 \mathrm{~V}$ |  | 1.6 | $\begin{aligned} & 3.0 \\ & 3.6 \end{aligned}$ | $\begin{aligned} & 3.0 \\ & 3.6 \end{aligned}$ | mA <br> max |
|  |  | Quad, LMC6584$\mathrm{V}_{\mathrm{CM}}=1.5 \mathrm{~V}$ |  | 3.2 | $\begin{aligned} & 6.0 \\ & 7.2 \end{aligned}$ | $\begin{aligned} & 6.0 \\ & 7.2 \end{aligned}$ | $\begin{aligned} & \mathrm{mA} \\ & \max \\ & \hline \end{aligned}$ |

## AC Electrical Characteristics

Unless otherwise specified, all limits guaranteed for $T_{J}=25^{\circ} \mathrm{C}, \mathrm{V}^{+}=3 \mathrm{~V}, \mathrm{~V}^{-}=0 \mathrm{~V}, \mathrm{~V}_{\mathrm{CM}}=\mathrm{V}_{\mathrm{O}}=\mathrm{V}^{+} / 2$ and $\mathrm{R}_{\mathrm{L}}>1 \mathrm{M} \Omega$. Boldface limits apply at the temperature extremes.

| Symbol | Parameter | Conditions | $\begin{gathered} \text { Typ } \\ \text { (Note 5) } \end{gathered}$ | LMC6582AI <br> LMC6584AI <br> Limit <br> (Note 6) | LMC6582BI <br> LMC6584BI <br> Limit <br> (Note 6) | Units |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| SR | Slew Rate | (Note 8) | 1.2 | $\begin{gathered} 0.7 \\ \mathbf{0 . 5 5} \end{gathered}$ | $\begin{gathered} 0.7 \\ \mathbf{0 . 5 5} \end{gathered}$ | $\begin{gathered} \mathrm{V} / \mu \mathrm{s} \\ \mathrm{~min} \end{gathered}$ |
|  |  | $\mathrm{V}^{+}=10 \mathrm{~V}$, (Note 10) | 1.2 | $\begin{gathered} 0.7 \\ \mathbf{0 . 5 5} \end{gathered}$ | $\begin{gathered} 0.7 \\ \mathbf{0 . 5 5} \end{gathered}$ |  |
| GBW | Gain-Bandwidth Product |  | 1.2 |  |  | MHz |
| $\phi_{\mathrm{m}}$ | Phase Margin |  | 50 |  |  | Deg |
| $\mathrm{G}_{\mathrm{m}}$ | Gain Margin |  | 12 |  |  | dB |
|  | Amp-to-Amp Isolation | $\mathrm{V}^{+}=10 \mathrm{~V}$ (Note 9) | 130 |  |  | dB |
| $e_{n}$ | Input-Referred Voltage Noise | $\begin{aligned} & \mathrm{f}=1 \mathrm{kHz} \\ & \mathrm{~V}_{\mathrm{CM}}=0.5 \mathrm{~V} \end{aligned}$ | 30 |  |  | $\frac{n V}{\sqrt{H z}}$ |
| $\mathrm{i}_{\mathrm{n}}$ | Input-Referred Current Noise | $\mathrm{f}=1 \mathrm{kHz}$ | 0.5 |  |  | $\frac{f A}{\sqrt{H z}}$ |
| T.H.D. | Total Harmonic Distortion | $\begin{aligned} & f=1 \mathrm{kHz}, A_{V}=+1 \\ & R_{L}=10 \mathrm{k} \Omega, V_{O}=2 V_{p-p} \end{aligned}$ | 0.01 |  |  | \% |

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating ratings indicate conditions for which the device is intended to be functional, but specific performance is not guaranteed. For guaranteed specifications and the test conditions, see the electrical characteristics. Note 2: Human body model, $1.5 \mathrm{k} \Omega$ in series with 100 pF .
Note 3: Applies to both single-supply and split-supply operation. Continous short circuit operation at elevated ambient temperature can result in exceeding the maximum allowed junction temperature of $150^{\circ} \mathrm{C}$. Output current in excess of $\pm 30 \mathrm{~mA}$ over long term may adversely affect reliability.
Note 4: The maximum power dissipation is a function of $T_{J(\max )}, \theta_{J A}$, and $T_{A}$. The maximum allowable power dissipation at any ambient temperature is $P_{D}=$ $\left(T_{J(\max )}-T_{A}\right) / \theta_{J A}$. All numbers apply for packages soldered directly into a PC board.
Note 5: Typical Values represent the most likely parametric norm.
Note 6: All limits are guaranteed by testing or statistical analysis.
Note 7: $\mathrm{V}^{+}=3 \mathrm{~V}, \mathrm{~V}_{\mathrm{CM}}=0.5 \mathrm{~V}$. For sourcing and sinking, $0.5 \mathrm{~V} \leq \mathrm{V}_{\mathrm{O}} \leq 2.5 \mathrm{~V}$.
Note 8: $\mathrm{V}^{+}=3 \mathrm{~V}$. Connected as Voltage Follower with 2 V step input, and output is measured from 0.8 V to 2.2 V . Number specified is the slower of the positive or negative slew rates.
Note 9: Input referred, $\mathrm{V}^{+}=10 \mathrm{~V}$, and $\mathrm{R}_{\mathrm{L}}=100 \mathrm{k} \Omega$ connected to 5 V . Each amp excited in turn with 1 kHz to produce $\mathrm{V}_{\mathrm{O}}=2 \mathrm{~V}_{\mathrm{PP}}$.
Note 10: $\mathrm{V}^{+}=10 \mathrm{~V}$. Connected as voltage follower with 8 V step Input, and output is measured from 2 V to 8 V . Number specified is the slower of the positive or negative slew rates.
Note 11: Limiting input pin current is only necessary for input voltages that exceed absolute maximum input voltage ratings.
Note 12: Guaranteed limits are dictated by tester limitations and not device performance. Actual performance is reflected in the typical value
Note 13: $\mathrm{CMRR}^{+}$and CMRR ${ }^{-}$are tested, and the number indicated is the lower of the two values. For $\mathrm{CMRR}^{+}, \mathrm{V}^{+} / 2<\mathrm{V}_{\mathrm{CM}}<\mathrm{V}^{+}$for $1.8 \mathrm{~V}, 2.2 \mathrm{~V}, 3 \mathrm{~V}, 5 \mathrm{~V}$, and 10 V . For $\mathrm{CMRR}^{-}, 0<\mathrm{V}_{\mathrm{CM}}<\mathrm{V}^{+} / 2$ for $3 \mathrm{~V}, 5 \mathrm{~V}$ and 10 V . For 1.8 V and $2.2 \mathrm{~V}, 0.25<\mathrm{V}_{\mathrm{CM}}<\mathrm{V}^{+}-0.3$.
Note 14: $\mathrm{V}^{+}=10 \mathrm{~V}, \mathrm{~V}_{\mathrm{CM}}=0.5 \mathrm{~V}$. For Sourcing tests, $1 \mathrm{~V} \leq \mathrm{V}_{\mathrm{O}} \leq 5 \mathrm{~V}$. For Sinking tests, $5 \mathrm{~V} \leq \mathrm{V}_{\mathrm{O}} \leq 9 \mathrm{~V}$.

## Typical Performance Characteristics

$\mathrm{V}_{\mathrm{S}}{ }^{+}=3 \mathrm{~V}$, Single Supply, $\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$ unless otherwise specified.


Input Voltage Noise vs Common-Mode Voltage

$v_{C M}$, (v)

## Frequency Response vs Temperature


freouency, (kHz)



Vcm, (v)
Frequency Response vs $\mathrm{R}_{\mathrm{L}}$


Positive PSRR vs
Frequency


Sinking Current vs Output Voltage



Vcm, (v)
Input Voltage Noise vs Frequency



## Typical Performance Characteristics

$\mathrm{V}_{S^{+}}=3 \mathrm{~V}$, Single Supply, $\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$ unless otherwise specified. (Continued)


TL/H/12041-32

## Application Information

### 1.0 Input Common-Mode Voltage Range

The LMC6582/4 has a rail-to-rail input common-mode voltage range. Figure 1 shows an input voltage exceeding both supplies with no resulting phase inversion on the output.


TL/H/12041-3
FIGURE 1. An Input Signal Exceeds the LMC6582 Power Supply Voltages with No Output Phase Inversion
The absolute maximum input voltage at $\mathrm{V}^{+}=3 \mathrm{~V}$ is 300 mV beyond either supply rail at room temperature. Voltages greatly exceeding this absolute maximum rating, as in Figure 2, can cause excessive current to flow in or out of the input pins, possibly affecting reliability. The input current can be externally limited to $\pm 5 \mathrm{~mA}$, with an input resistor, as shown in Figure 3.


FIGURE 2. A $\pm$ 7.5V Input Signal Greatly Exceeds the 3V Supply, Causing No Phase Inversion Due to $\mathbf{R}_{\mathbf{I}}$


TL/H/12041-5
FIGURE 3. Input Current Protection for Voltages Exceeding the Supply Voltage

### 2.0 Rail-to-Rail Output

The approximated output resistance of the LMC6582 is $50 \Omega$ sourcing, and $50 \Omega$ sinking at $\mathrm{V}_{\mathrm{S}}=3 \mathrm{~V}$. The maximum output swing can be estimated as a function of load using the calculated output resistance.

### 3.0 Low Voltage Operation

The LMC6582/4 operates at supply voltages of 2.2 V and 1.8 V . These voltages represent the End of Discharge voltages of several popular batteries. The amplifier can operate from 1 Lead-Acid or Lithium Ion battery, or 2NiMH, NiCd, or Carbon-Zinc batteries. Nominal and End of Discharge of Voltage of several batteries are listed below.

| Battery Type | Nominal Voltage | End of Discharge <br> Voltage |
| :--- | :---: | :---: |
| NiMH | 1.2 V | 1 V |
| NiCd | 1.2 V | 1 V |
| Lead-Acid | 2 V | 1.8 V |
| Silver Oxide | 1.6 V | 1.3 V |
| Carbon-Zinc | 1.5 V | 1.1 V |
| Lithium | $2.6 \mathrm{~V}-3.6 \mathrm{~V}$ | $1.7 \mathrm{~V}-2.4 \mathrm{~V}$ |

At $\mathrm{V}_{\mathrm{S}}=2.2 \mathrm{~V}$, the LMC6582/4 has a rail-to-rail input com-mon-mode voltage range. Figure 4 shows an input voltage extending to both supplies and the resulting output.


TL/H/12041-6
FIGURE 4. The Input Common-Mode Voltage Range Extends to Both Supplies at $\mathbf{V}_{\mathbf{S}}=\mathbf{2 . 2 V}$
The amplifier is operational at $\mathrm{V}_{\mathrm{S}}=1.8 \mathrm{~V}$, with guaranteed input common-mode voltage range, output swing, and CMRR specs. Figure 5 shows the response of the LMC6582/4 at $\mathrm{V}_{\mathrm{S}}=1.8 \mathrm{~V}$.


FIGURE 5. Response of the LMC6582/4 at $\mathrm{V}_{\mathrm{S}}=1.8 \mathrm{~V}$

## Application Information (Continued)

Figure 6 shows an input voltage exceeding both supplies with no resulting phase inversion on the output.


FIGURE 6. An Input Voltage Signal Exceeds LMC6582/4 Power Supply Voltages of $\mathbf{V}_{\mathbf{S}}=1.8 \mathrm{~V}$ with No Output Phase Inversion

### 4.0 Capacitive Load Tolerance

The LMC6582/4 can typically drive a 100 pF load with $\mathrm{V}_{\mathrm{S}}=$ 10 V at unity gain without oscillating. The unity gain follower is the most sensitive configuration to capacitive load. Direct capacitive loading reduces the phase margin of op-amps. The combination of the op-amp's output impedance and the capacitive load induces phase lag. This results in either an underdamped pulse response or oscillation.
Capacitive load compensation can be accomplished using resistive isolation as shown in Figure 7. If there is a resistive component of the load in parallel to the capacitive component, the isolation resistor and the resistive load create a voltage divider at the output. This introduces a DC error at the output.


TL/H/12041-9
FIGURE 7. Resistive Isolation of a 350 pF Capacitive Load Figure 8 displays the pulse response of the LMC6582 circuit in Figure 7.


TL/H/12041-10
FIGURE 8. Pulse Response of the LMC6582 Circuit in Figure 7

Another circuit, shown in Figure 9, is also used to indirectly drive capacitive loads. This circuit is an improvement to the circuit shown Figure 7 because it provides DC accuracy as well as AC stability. R1 and C1 serve to counteract the loss of phase margin by feeding the high frequency component of the output signal back to the amplifiers inverting input, thereby preserving phase margin in the overall feedback loop. The values of R1 and C1 should be experimentally determined by the system designer for the desired pulse response. Increased capacitive drive is possible by increasing the value of the capacitor in the feedback loop.


TL/H/12041-11
FIGURE 9. The LMC6582 Compensated to Ensure DC Accuracy and AC Stability
The pulse response of the circuit shown in Figure 9 is shown in Figure 10.


TL/H/12041-12
FIGURE 10. Pulse Response of the LMC6582 Circuit Shown in Figure 9

## Application Information (Continued)

### 5.0 Printed-Circuit-Board Layout for High-Impedance Work

It is generally recognized that any circuit which must operate with less than 1000 pA of leakage current requires special layout of the PC board. When one wishes to take advantage of the ultra-low input current of the LMC6582/4, typically 80 fA , it is essential to have an excellent layout. Fortunately, the techniques of obtaining low leakages are quite simple. First, the user must not ignore the surface leakage of the PC board, even though it may sometimes appear acceptably low, because under conditions of high humidity or dust or contamination, the surface leakage will be appreciable.
To minimize the effect of any surface leakage, lay out a ring of foil completely surrounding the LMC6582/4's inputs and the terminals of capacitors, diodes, conductors, resistors, relay terminals, etc. connected to the op-amp's inputs, as in Figure 11. To have a significant effect, guard rings should be placed in both the top and bottom of the PC board. This PC foil must then be connected to a voltage which is at the same voltage as the amplifier inputs, since no leakage current can flow between two points at the same potential. For example, a PC board trace-to-pad resistance of $10^{12} \Omega$, which is normally considered a very large resistance, could leak 5 pA if the trace were a 5 V bus adjacent to the pad of the input. This would cause a 60 times degradation from the LMC6582/4's actual performance. However, if a guard ring is held within 5 mV of the inputs, then even a resistance of $10^{11} \Omega$ would cause only 0.05 pA of leakage current. See Figures 12a, 12b, and 12c for typical connections of guard rings for standard op-amp configurations.


TL/H/12041-14
FIGURE 11. Example of Guard Ring in PC Board Layout

(a) Inverting Amplifier


TL/H/12041-16
(b) Non-Inverting Amplifier

(c) Follower

FIGURE 12. Typical Connections of Guard Rings
The designer should be aware that when it is inappropriate to lay out a PC board for the sake of just a few circuits, there is another technique which is even better than a guard ring on a PC board: Don't insert the amplifier's input pin into the board at all, but bend it up in the air and use only air as an insulator. Air is an excellent insulator. In this case you may have to forego some of the advantages of PC board construction, but the advantages are sometimes well worth the effort of using point-to-point up-in-the-air wiring. See Figure 13.


FIGURE 13. Air Wiring

## Application Information (Continued)

### 6.0 Compensating for Input Capacitance

It is quite common to use large values of feedback resistance with amplifiers that have ultra-low input current, like the LMC6582/4. Large feedback resistors can react with small values of input capacitance due to transducers, photodiodes, and circuits board parasitics to reduce phase margins.


FIGURE 14. Canceling the Effect of Input Capacitance
The effect of input capacitance can be compensated for by adding a feedback capacitor. The feedback capacitor (as in Figure 14), $\mathrm{C}_{\mathrm{F}}$, is first estimated by:

$$
\begin{gathered}
\frac{1}{2 \pi R_{1} C_{I N}} \geq \frac{1}{2 \pi R_{2} C_{F}} \\
\text { or } \\
R_{1} C_{I N} \leq R_{2} C_{F}
\end{gathered}
$$

which typically provides significant overcompensation.
Printed circuit board stray capacitance may be larger or smaller than that of a breadboard, so the actual optimum value for $C_{F}$ may be different. The values of $C_{F}$ should be checked on the actual circuit. (Refer to the LMC660 quad CMOS amplifier data sheet for a more detailed discussion.)

### 7.0 Spice Macromodel

A Spice Macromodel is available for the LMC6582/4. The model includes a simulation of:

- Input common-mode voltage range
- Frequency and transient response
- GBW dependence on loading conditions
- Quiescent and dynamic supply current
- Output swing dependence on loading conditions and many more characteristics as listed on the macromodel disk.
Contact the National Semiconductor Customer Response Center at 1-800-272-9959 to obtain an operational amplifier spice model library disk.


## Applications

## Transducer Interface Circuits

A. PIEZOELECTRIC TRANSDUCERS


FIGURE 15. Transducer Interface Application
The LMC6582/4 can be used for processing of transducer signals as shown in the circuit below. The two $11 \mathrm{M} \Omega$ resistors provide a path for the DC currents to ground. Since the resistors are boot-strapped to the output, the AC input resistance of the LMC6582/4 is much higher.


TL/H/12041-22
FIGURE 16. LMC6582 Used for Signal Processing
An input current of 80 fA and a CMRR of 82 dB causes an insignifcant error offset voltage at the output. The rail-to-rail performance of the amplifier also provides the maximum dynamic range for the transducer signals.

## B. PHOTODIODE AMPLIFIERS



TL/H/12041-23
FIGURE 17. Photodiode Amplifier
Photocells can be used in light measuring instruments. An error voltage is produced at the output due to the input current and the offset voltage of the amplifier. The LMC6582/4 which can be operated off a single battery is an excellent choice for this application because of its 80 fA input current and 0.5 mV offset voltage.

## Applications (Continued)

## Low Voltage Peak Detector



## FIGURE 18. Low Voltage Peak Detector

The accuracy of the peak detector is dependent on the leakage currents of the diodes and the capacitor, and the non-idealities of the amplifier. The parameters of the amplifer which can limit the performance of this circuit are (a) Finite slew rate (b) Input current, and (c) Maximum output current of the amplifier.
The input current of the amplifier causes a slow discharge of the capacitor. This phenomenon is called "drooping". The LMC6582/4 has a typical input current of 80 fA . This would cause the capacitor to droop at a rate of $\mathrm{dv} / \mathrm{dt}=\mathrm{I}_{\mathrm{B}} / \mathrm{C}=$ $80 \mathrm{fA} / 100 \mathrm{pF}=0.8 \mathrm{mV} / \mathrm{s}$. Accuracy in the amplitude measurement is also maintained by an offset voltage of 0.5 mV , and an open-loop gain of 120 dB .

## Oscillators



TL/H/12041-27
FIGURE 19. 1 Hz Square-Wave Oscillator

For single supply 5 V operation, the output of the circuit will swing 0 V to 5 V . The voltage divider set by the resistors will cause the input at the non-inverting terminal of the op-amp to move $1 / 3(1.67 \mathrm{~V})$ of the supply voltage to $2 / 3(3.33 \mathrm{~V})$ of the supply voltage. This voltage behaves as the threshold voltage, and causes the capacitor to alternately charge and discharge.
R1 and C1 determine the time constant for the circuit. The frequency of oscillation, fosc is $\left(\frac{1}{2 \Delta t}\right)$, where $\Delta t$ is the time the amplifier input takes to move from 1.67 V to 3.33 V . The calculations are shown below.
$1.67=5\left(1-e-\frac{t_{1}}{\tau}\right)$
where $\tau=\mathrm{RC}=0.68$ seconds
$\rightarrow t_{1}=0.27$ seconds
and
$3.33=5\left(1-e-\frac{t_{1}}{\tau}\right)$
$\rightarrow t_{2}=0.74$ seconds
Then, $\mathrm{fOSC}=\left(\frac{1}{2 \Delta t}\right)$

$$
=\frac{1}{2(0.74-0.27)}
$$

$$
\sim 1 \mathrm{~Hz}
$$

## LMC6582/4 as a Comparator



TL/H/12041-28
FIGURE 20. Comparator with Hysteresis
Figure 20 shows the application of the LMC6582/4 as a comparator. The hysteresis is determined by the ratio of the two resistors. Since the supply current of the LMC6582/4 is less than 1 mA per amplifier, it can be used as a low power comparator, in applications where the quiescent current is an important parameter.
Typical propagation delays @ $\mathrm{V}_{\mathrm{S}}=3 \mathrm{~V}$ would be on the order of $\mathrm{t}_{\mathrm{PHL}}=6 \mu \mathrm{~s}$, and $\mathrm{t}_{\mathrm{PLH}}=5 \mu \mathrm{~s}$.

Applications (Continued)

## Filters



FIGURE 21. Wide-Band Band-Pass Filter
The filter shown in Figure 21 is used to process "voiceband" signals. The bandpass filter has a flatband gain of 40 dB . The two corner frequencies, $f_{1}$ and $f_{2}$, are calculated as:
$\mathrm{f}_{1}=\frac{1}{2 \pi \mathrm{R}_{1} \mathrm{C}_{1}}=\frac{1}{2 \pi(10 \mathrm{k} \Omega)(79 \mathrm{nF})}=200 \mathrm{~Hz}$
$\mathrm{f}_{2}=\frac{1}{2 \pi \mathrm{R}_{2} \mathrm{C}_{2}}=\frac{1}{2 \pi(1 \mathrm{M} \Omega)(40 \mathrm{pF})}=4 \mathrm{kHz}$
The LMC6582/4, with its rail-to-rail input common mode voltage range and high gain ( 120 dB typical, $R_{L}=10 \mathrm{k} \Omega$ ) is extremely well suited for such filter applications. The rail-torail input range allows for large input signals to be processed without distortion. The high gain means that the circuit can provide filtering and gain in one stage, instead of the typical two stage filter. This implies a reduction in cost, and a savings of space and power.
This is an illustration of a conceptual use of the LMC6582/4. The selectivity of the filter can be improved by increasing the order (number of poles) of the design.

## Sample-and-Hold Circuits



FIGURE 22. Sample-and-Hold Application

When the "switch" is closed during the sample interval, $\mathrm{C}_{\text {HOLD }}$ charges up to the value of the input signal. When the "switch" is open, CHOLD retains this value as it is buffered by the high input impedance of the LMC6582/4.
Errors in the "hold" voltage are caused by the input current of the amplifier, the leakage current of the CD4066, and the leakage current of the capacitor. While an input current of 80 fA minimizes the accumulation rate for error in the circuit, the LMC6582/4's CMRR of 82 dB allows excellent accuracy throughout the amplifier's rail-to-rail dynamic capture range.

## Battery Monitoring Circuit



TL/H/12041-33
FIGURE 23a. Circuit Used to Sense Charging.


FIGURE 23b. Circuit used to Sense Discharging
The LMC6582/4 has been optimized for performance at 3 V , and also has guaranteed specs at 1.8 V and 2.2 V . In portable applications, the $\mathrm{R}_{\text {Load }}$ represents the laptop/notebook, or any other computer which the battery is powering. A desired output voltage can be achieved by manipulating the ratios of the feedback resistors. During the charging cycle, the current flows out of the battery as shown. While during discharge, the current is in the reverse direction. Since the current can range from a few milliamperes to amperes, the amplifier will have to sense a signal below ground during the discharge cycle. At 3V, the LMC6582/4 can accept a signal up to 300 mV below ground. The common-mode voltage range of the LMC6582/4, which extends beyond both rails is thus a very useful feature in this application.
A typical offset voltage of 0.5 mV , and CMRR of 82 dB maintain accuracy in the circuit outputs while the rail-to-rail output performance allows for a maximum signal range.




Physical Dimensions inches (millimeters) (Continued)


14-Pin Molded Dual-In Line Package Order Number LMC6584AIN or LMC6584BIN

NS Package Number N14A

## LIFE SUPPORT POLICY

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Absolute Maximum Ratings (Note 1)
If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.
ESD Tolerance (Note 2)
Differential Input Voltage
Voltage at Input/Output Pin
Supply Voltage ( $\mathrm{V}^{+}-\mathrm{V}^{-}$)
Current at Input Pin (Note 11)
Current at Output Pin (Note 3) $\pm 30 \mathrm{~mA}$
Current at Power Supply Pin
Lead Temp. (soldering, 10 sec .)
(V)
$\left(V^{+}\right)+0.3 V,\left(V^{-}\right)-0.3 V$ 12 V
$\pm 5 \mathrm{~mA}$
$\pm 30 \mathrm{~mA}$
35 mA
$260^{\circ} \mathrm{C}$
Storage Temperature Range
$-65^{\circ} \mathrm{C}$ to $+150^{\circ} \mathrm{C}$
Junction Temperature (Note 4)

## 3V DC Electrical Characteristics

Unless otherwise specified, all limits guaranteed for $\mathrm{T}_{\mathrm{J}}=25^{\circ} \mathrm{C}, \mathrm{V}^{+}=3.0 \mathrm{~V}, \mathrm{~V}^{-}=0 \mathrm{~V}, \mathrm{~V}_{\mathrm{CM}}=\mathrm{V}_{\mathrm{O}}=\mathrm{V}^{+} / 2, \mathrm{~V}_{\mathrm{PD}}=0.6 \mathrm{~V}$ and $R_{L}>1 \mathrm{M} \Omega$. Boldface limits apply at the temperature extremes (Note 16).

| Symbol | Parameter | Conditions | $\begin{gathered} \text { Typ } \\ \text { (Note 5) } \end{gathered}$ | LMC6681AI <br> LMC6682AI <br> LMC6684AI <br> Limit <br> (Note 6) | LMC6681BI <br> LMC6682BI <br> LMC6684BI <br> Limit <br> (Note 6) | Units |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| $\mathrm{V}_{\text {OS }}$ | Input Offset Voltage |  | 0.5 | $\begin{gathered} 1 \\ 2.5 \end{gathered}$ | $\begin{gathered} 3 \\ 4.5 \end{gathered}$ | $\begin{gathered} \mathrm{mV} \\ \max \end{gathered}$ |
| TCV ${ }_{\text {OS }}$ | Input Offset Voltage Average Drift |  | 1.5 |  |  | $\mu \mathrm{V} /{ }^{\circ} \mathrm{C}$ |
| $\mathrm{I}_{\mathrm{B}}$ | Input Current | (Note 12) | 0.08 | 20 | 20 | pA max |
| los | Input Offset Current | (Note 12) | 0.04 | 10 | 10 | pA max |
| $\mathrm{R}_{\text {IN }}$ | Input Resistance |  | $>1$ |  |  | Tera $\Omega$ |
| $\mathrm{C}_{\text {IN }}$ | Input Capacitance |  | 3 |  |  | pF |
| CMRR | Common Mode Rejection Ratio | (Note 13) | 82 | $\begin{aligned} & 70 \\ & 65 \end{aligned}$ | $\begin{aligned} & 65 \\ & 62 \end{aligned}$ | $\begin{gathered} \mathrm{dB} \\ \mathrm{~min} \end{gathered}$ |
| PSRR | Power Supply <br> Rejection Ratio | $\begin{aligned} & \pm 1.5 \mathrm{~V} \leq \mathrm{V}_{\mathrm{S}} \leq \pm 2.5 \mathrm{~V} \\ & \mathrm{~V}_{\mathrm{O}}=\mathrm{V}+/ 2=\mathrm{V}_{\mathrm{CM}} \end{aligned}$ | 82 | $\begin{array}{r} 70 \\ 65 \\ \hline \end{array}$ | $\begin{array}{r} 65 \\ 62 \\ \hline \end{array}$ | $\begin{gathered} \mathrm{dB} \\ \mathrm{~min} \end{gathered}$ |
| $\mathrm{V}_{\mathrm{CM}}$ | Input Common Mode Voltage Range | CMRR > 50 dB | 3.23 | $\begin{aligned} & 3.18 \\ & \mathbf{3 . 0 0} \end{aligned}$ | $\begin{aligned} & 3.18 \\ & \mathbf{3 . 0 0} \end{aligned}$ | $\begin{gathered} \mathrm{V} \\ \mathrm{~min} \end{gathered}$ |
|  |  |  | -0.3 | $\begin{aligned} & -0.18 \\ & \mathbf{0 . 0 0} \end{aligned}$ | $\begin{aligned} & -0.18 \\ & 0.00 \end{aligned}$ | $\begin{gathered} \mathrm{V} \\ \max \end{gathered}$ |
| $A_{V}$ | Large Signal Voltage Gain | $\mathrm{R}_{\mathrm{L}}=600 \Omega$ (Notes 7, 12) | 70 | 10 | 10 | $\mathrm{V} / \mathrm{mV}$ |
|  |  | $R_{L}=10 \mathrm{k} \Omega$ (Notes 7, 12) | 1000 | 12 | 12 | $\mathrm{V} / \mathrm{mV}$ |


| 3V DC Electrical Characteristics (Continued) <br> Unless otherwise specified, all limits guaranteed for $\mathrm{T}_{\mathrm{J}}=25^{\circ} \mathrm{C}, \mathrm{V}^{+}=3.0 \mathrm{~V}, \mathrm{~V}^{-}=0 \mathrm{~V}, \mathrm{~V}_{\mathrm{CM}}=\mathrm{V}_{\mathrm{O}}=\mathrm{V}^{+} / 2, \mathrm{~V}_{\mathrm{PD}}=0.6 \mathrm{~V}$ and $R_{L}>1 \mathrm{M} \Omega$. Boldface limits apply at the temperature extremes (Note 16). |  |  |  |  |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| Symbol | Parameter | Conditions | Typ <br> (Note 5) | LMC6681AI <br> LMC6682AI <br> LMC6684AI <br> Limit <br> (Note 6) | LMC6681BI <br> LMC6682BI <br> LMC6684BI <br> Limit <br> (Note 6) | Units |
| $\mathrm{V}_{0}$ | Output Swing | $\mathrm{R}_{\mathrm{L}}=600 \Omega$ to $\mathrm{V}+/ 2$ | 2.87 | $\begin{aligned} & 2.70 \\ & \mathbf{2 . 5 8} \end{aligned}$ | $\begin{aligned} & 2.70 \\ & 2.58 \end{aligned}$ | $\begin{gathered} \mathrm{V} \\ \mathrm{~min} \end{gathered}$ |
|  |  |  | 0.15 | $\begin{gathered} 0.3 \\ \mathbf{0 . 4 2} \end{gathered}$ | $\begin{gathered} 0.3 \\ \mathbf{0 . 4 2} \end{gathered}$ | $\begin{gathered} \mathrm{V} \\ \max \end{gathered}$ |
|  |  | $R_{L}=2 \mathrm{k} \Omega$ to $\mathrm{V}+/ 2$ | 2.95 | $\begin{aligned} & 2.85 \\ & \mathbf{2 . 7 9} \end{aligned}$ | $\begin{gathered} 2.85 \\ \mathbf{2 . 7 9} \end{gathered}$ | $\begin{gathered} \mathrm{V} \\ \mathrm{~min} \end{gathered}$ |
|  |  |  | 0.05 | $\begin{gathered} 0.15 \\ \mathbf{0 . 2 1} \end{gathered}$ | $\begin{aligned} & 0.15 \\ & \mathbf{0 . 2 1} \end{aligned}$ | $\begin{gathered} \mathrm{V} \\ \max \end{gathered}$ |
|  |  | $\mathrm{R}_{\mathrm{L}}=10 \mathrm{k} \Omega$ to $\mathrm{V}+/ 2$ | 2.99 | $\begin{gathered} 2.94 \\ \mathbf{2 . 9 1} \end{gathered}$ | $\begin{gathered} 2.94 \\ \mathbf{2 . 9 1} \end{gathered}$ | $\begin{gathered} \mathrm{V} \\ \mathrm{~min} \end{gathered}$ |
|  |  |  | 0.01 | $\begin{aligned} & 0.04 \\ & 0.05 \end{aligned}$ | $\begin{gathered} 0.04 \\ 0.05 \end{gathered}$ | $\begin{gathered} \mathrm{V} \\ \max \end{gathered}$ |
| Isc | Output Short Circuit Current | Sourcing, $\mathrm{V}_{\mathrm{O}}=0 \mathrm{~V}$ | 20 | $\begin{aligned} & 9.0 \\ & 6.7 \\ & \hline \end{aligned}$ | $\begin{aligned} & 9.0 \\ & 6.7 \end{aligned}$ | $\begin{aligned} & \mathrm{mA} \\ & \mathrm{~min} \end{aligned}$ |
|  |  | Sinking, $\mathrm{V}_{\mathrm{O}}=3 \mathrm{~V}$ | 12 | $\begin{array}{r} 6.0 \\ \mathbf{4 . 5} \\ \hline \end{array}$ | $\begin{array}{r} 6.0 \\ 4.5 \\ \hline \end{array}$ | $\begin{aligned} & \mathrm{mA} \\ & \mathrm{~min} \end{aligned}$ |
| IS ON | Supply Current when Powered ON | Single, LMC6681 $\mathrm{V}_{\mathrm{CM}}=1.5 \mathrm{~V}$ | 0.7 | $\begin{aligned} & 1.13 \\ & \mathbf{1 . 3 6} \end{aligned}$ | $\begin{aligned} & 1.13 \\ & \mathbf{1 . 3 6} \\ & \hline \end{aligned}$ | mA <br> max |
|  |  | Dual, LMC6682 $\mathrm{V}_{\mathrm{CM}}=1.5 \mathrm{~V}$ | 1.4 | $\begin{gathered} 2.26 \\ \mathbf{2 . 7 5} \\ \hline \end{gathered}$ | $\begin{gathered} 2.26 \\ \mathbf{2 . 7 5} \end{gathered}$ | $\begin{aligned} & \mathrm{mA} \\ & \mathrm{max} \end{aligned}$ |
|  |  | Quad, LMC6684 $\mathrm{V}_{\mathrm{CM}}=1.5 \mathrm{~V}$ | 2.8 | $\begin{gathered} 4.52 \\ \mathbf{5 . 4 2} \\ \hline \end{gathered}$ | $\begin{gathered} 4.52 \\ \mathbf{5 . 4 2} \\ \hline \end{gathered}$ | $\begin{array}{r} \mathrm{mA} \\ \max \\ \hline \end{array}$ |
| IS OFF | Supply Current when Powered OFF | Single, LMC6681 $\mathrm{V}_{\mathrm{PD}}=2.3 \mathrm{~V}$ | 0.5 | $\begin{array}{r} 1.5 \\ \mathbf{2 . 1} \end{array}$ | $\begin{array}{r} 1.5 \\ \mathbf{2 . 1} \\ \hline \end{array}$ | $\begin{gathered} \mu \mathrm{A} \\ \max \end{gathered}$ |
|  |  | Dual, LMC6682 $V_{P D}=2.3 V$ | 0.5 | $\begin{array}{r} 1.5 \\ \mathbf{2 . 1} \\ \hline \end{array}$ | $\begin{array}{r} 1.5 \\ \mathbf{2 . 1} \\ \hline \end{array}$ | $\begin{gathered} \mu \mathrm{A} \\ \max \end{gathered}$ |
|  |  | Quad, LMC6684 $V_{P D}=2.3 V$ | 1.0 | $\begin{aligned} & 3.0 \\ & 4.2 \\ & \hline \end{aligned}$ | $\begin{array}{r} 3.0 \\ \mathbf{4 . 2} \\ \hline \end{array}$ | $\begin{gathered} \mu \mathrm{A} \\ \max \end{gathered}$ |
|  |  |  |  |  |  |  |




10V DC Electrical Characteristics
Unless otherwise specified, all limits guaranteed for $\mathrm{T}_{\mathrm{J}}=25^{\circ} \mathrm{C}, \mathrm{V}+=10.0 \mathrm{~V}, \mathrm{~V}^{-}=0 \mathrm{~V}, \mathrm{~V}_{\mathrm{CM}}=\mathrm{V}_{\mathrm{O}}=\mathrm{V}^{+} / 2, \mathrm{~V}_{\mathrm{PD}}=1.2 \mathrm{~V}$ and $R_{L}>1 \mathrm{M} \Omega$. Boldface limits apply at the temperature extremes (Note 16).

| Symbol | Parameter | Conditions |  | $\begin{gathered} \text { Typ } \\ \text { (Note 5) } \end{gathered}$ | LMC6681AI <br> LMC6682AI <br> LMC6684AI <br> Limit <br> (Note 6) | LMC6681BI <br> LMC6682BI <br> LMC6684BI <br> Limit <br> (Note 6) | Units |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| $\mathrm{V}_{\text {OS }}$ | Input Offset Voltage | $\mathrm{V}_{\mathrm{CM}}=1.5 \mathrm{~V}$ |  | 0.5 | $\begin{aligned} & 1.5 \\ & 3.0 \end{aligned}$ | $\begin{aligned} & 3.5 \\ & 5.0 \end{aligned}$ | $\mathrm{mV}$ $\max$ |
| TCV ${ }_{\text {OS }}$ | Input Offset Voltage Average Drift |  |  | 1.5 |  |  | $\mu \mathrm{V} /{ }^{\circ} \mathrm{C}$ |
| $\mathrm{I}_{\mathrm{B}}$ | Input Current | (Note 12) |  | 0.08 | 20 | 20 | pA max |
| los | Input Offset Current | (Note 12) |  | 0.04 | 10 | 10 | pA max |
| $\mathrm{R}_{\mathrm{IN}}$ | Input Resistance |  |  | $>1$ |  |  | Tera $\Omega$ |
| $\mathrm{C}_{\text {IN }}$ | Input Capacitance |  |  | 3 |  |  | pF |
| CMRR | Common Mode Rejection Ratio | (Note 13) |  | 82 | $\begin{array}{r} 65 \\ \mathbf{6 2} \\ \hline \end{array}$ | $\begin{array}{r} 65 \\ \mathbf{6 2} \\ \hline \end{array}$ | dB <br> min |
| PSRR | Positive Power Supply Rejection Ratio | $\begin{aligned} & \pm 1.1 \mathrm{~V} \leq \mathrm{V}_{\mathrm{S}} \leq \pm 5 \mathrm{~V} \\ & \mathrm{~V}_{\mathrm{O}}=\mathrm{V}+/ 2 \end{aligned}$ |  | 82 | $\begin{aligned} & 70 \\ & 65 \end{aligned}$ | $\begin{aligned} & 65 \\ & 62 \end{aligned}$ | $\begin{gathered} \mathrm{dB} \\ \mathrm{~min} \end{gathered}$ |
| $\mathrm{V}_{\mathrm{CM}}$ | Input Common Mode Voltage Range | CMRR > 50 dB |  | 10.30 | $\begin{gathered} 10.18 \\ \mathbf{1 0 . 0 0} \\ \hline \end{gathered}$ | $\begin{gathered} 10.18 \\ \mathbf{1 0 . 0 0} \end{gathered}$ | $\begin{gathered} \mathrm{V} \\ \mathrm{~min} \end{gathered}$ |
|  |  |  |  | -0.30 | $\begin{aligned} & -0.18 \\ & 0.00 \end{aligned}$ | $\begin{aligned} & -0.18 \\ & 0.00 \end{aligned}$ | $\underset{\max }{V}$ |
| $\mathrm{V}_{\mathrm{O}}$ | Output Swing | $\mathrm{R}_{\mathrm{L}}=2 \mathrm{k} \Omega$ to $\mathrm{V}+/ 2$ |  | 9.93 | $\begin{gathered} 9.7 \\ \mathbf{9 . 5 8} \end{gathered}$ | $\begin{gathered} 9.7 \\ \mathbf{9 . 5 8} \end{gathered}$ | $\begin{gathered} \mathrm{V} \\ \mathrm{~min} \end{gathered}$ |
|  |  |  |  | 0.08 | $\begin{gathered} 0.3 \\ \mathbf{0 . 4 2} \end{gathered}$ | $\begin{gathered} 0.3 \\ \mathbf{0 . 4 2} \end{gathered}$ | $\underset{\max }{V}$ |
| $A_{V}$ | Large Signal Voltage Gain | $\mathrm{R}_{\mathrm{L}}=2 \mathrm{k} \Omega \text { to } \mathrm{V}+/ 2$ <br> (Note 12) | Sourcing | 89 | 25 | 25 | $\mathrm{V} / \mathrm{mV}$ |
|  |  |  | Sinking | 224 | 25 | 25 | $\mathrm{V} / \mathrm{mV}$ |
| Isc | Output Short Circuit Current | Sourcing, $\mathrm{V}_{\mathrm{O}}=0 \mathrm{~V}$ <br> (Note 14) |  | 65 | $\begin{aligned} & 30 \\ & \mathbf{2 2} \\ & \hline \end{aligned}$ | $\begin{aligned} & 30 \\ & \mathbf{2 2} \\ & \hline \end{aligned}$ | mA min |
|  |  | Sinking, $\mathrm{V}_{\mathrm{O}}=10 \mathrm{~V}$ <br> (Note 14) |  | 70 | $\begin{array}{r} 30 \\ \mathbf{2 2} \\ \hline \end{array}$ | $\begin{array}{r} 30 \\ \mathbf{2 2} \\ \hline \end{array}$ | $\begin{aligned} & \mathrm{mA} \\ & \mathrm{~min} \\ & \hline \end{aligned}$ |
| IS ON | Supply Current when Powered ON | Single, LMC6681$\mathrm{V}_{\mathrm{CM}}=1.5 \mathrm{~V}$ |  | 0.9 | $\begin{array}{r} 1.50 \\ \mathbf{1 . 8} \\ \hline \end{array}$ | $\begin{array}{r} 1.50 \\ \mathbf{1 . 8} \\ \hline \end{array}$ | $\begin{array}{r} \mathrm{mA} \\ \mathrm{max} \\ \hline \end{array}$ |
|  |  | Dual, LMC6682$\mathrm{V}_{\mathrm{CM}}=1.5 \mathrm{~V}$ |  | 1.6 | $\begin{array}{r} 3.00 \\ \mathbf{3 . 6} \\ \hline \end{array}$ | $\begin{aligned} & 3.00 \\ & \mathbf{3 . 6} \\ & \hline \end{aligned}$ | $\begin{array}{r} \mathrm{mA} \\ \max \\ \hline \end{array}$ |
|  |  | Quad, LMC6684$\mathrm{V}_{\mathrm{CM}}=1.5 \mathrm{~V}$ |  | 3.2 | $\begin{aligned} & 6.00 \\ & \mathbf{7 . 2} \\ & \hline \end{aligned}$ | $\begin{aligned} & 6.00 \\ & \mathbf{7 . 2} \\ & \hline \end{aligned}$ | mA <br> max |
| IS OFF | Supply Current when Powered OFF | Single, LMC6681$V_{P D}=9.3 \mathrm{~V}$ |  | 0.5 | $\begin{aligned} & 5 \\ & 7 \\ & \hline \end{aligned}$ | $\begin{aligned} & 5 \\ & 7 \\ & \hline \end{aligned}$ | $\begin{gathered} \mu \mathrm{A} \\ \max \\ \hline \end{gathered}$ |
|  |  | Dual, LMC6682$V_{P D}=9.3 \mathrm{~V}$ |  | 0.5 | $\begin{array}{r} 5 \\ 7 \\ \hline \end{array}$ | $\begin{aligned} & 5 \\ & 7 \\ & \hline \end{aligned}$ | $\begin{gathered} \mu \mathrm{A} \\ \max \\ \hline \end{gathered}$ |
|  |  | Quad, LMC6684$V_{P D}=9.3 \mathrm{~V}$ |  | 1.0 | $\begin{array}{r} 10 \\ \mathbf{1 4} \\ \hline \end{array}$ | $\begin{array}{r} 10 \\ \mathbf{1 4} \\ \hline \end{array}$ | $\mu \mathrm{A}$ $\max$ |

Powerdown DC Threshold Characteristics
Boldface limits apply at the temperature extremes (Note 16).

| Symbol | Parameter | Conditions | LMC6681AI, LMC6681BI <br> LMC6682AI, LMC6682BI <br> LMC6684AI, LMC6684BI |  |  | Units |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  |  | Min | Typ | Max |  |
| $\mathrm{V}_{\mathrm{PD}, \mathrm{IL}}$ | Powerdown Voltage Input Low (Device Powered ON; Amplifier meets all specs in the datasheet tables) | $\begin{aligned} & \mathrm{V}^{+}=2.2 \mathrm{~V} \\ & \mathrm{~V}^{-}=0 \mathrm{~V} \end{aligned}$ |  |  | $\begin{gathered} 0.4 \\ \mathbf{0 . 2 5} \end{gathered}$ | V |
|  |  | $\begin{aligned} & \mathrm{V}^{+}=3 \mathrm{~V} \\ & \mathrm{~V}^{-}=0 \mathrm{~V} \end{aligned}$ |  |  | $\begin{gathered} 0.6 \\ \mathbf{0 . 4 5} \end{gathered}$ | V |
|  |  | $\begin{aligned} & \mathrm{V}^{+}=5 \mathrm{~V} \\ & \mathrm{~V}^{-}=0 \mathrm{~V} \end{aligned}$ |  |  | $\begin{gathered} 0.9 \\ \mathbf{0 . 7 5} \end{gathered}$ | V |
|  |  | $\begin{aligned} & \mathrm{V}^{+}=10 \mathrm{~V} \\ & \mathrm{~V}^{-}=0 \mathrm{~V} \end{aligned}$ |  |  | $\begin{gathered} 1.2 \\ \mathbf{1 . 0 5} \\ \hline \end{gathered}$ | V |
| $\mathrm{V}_{\mathrm{PD}, \mathrm{IH}}$ | Powerdown Voltage Input High (Device Powered OFF; Refer to DC Electrical Characteristics for Is OFF specs) | $\begin{aligned} & \mathrm{V}^{+}=2.2 \mathrm{~V} \\ & \mathrm{~V}^{-}=0 \mathrm{~V} \end{aligned}$ | $\begin{gathered} 1.5 \\ \mathbf{1 . 6 5} \end{gathered}$ |  |  | V |
|  |  | $\begin{aligned} & \mathrm{V}^{+}=3 \mathrm{~V} \\ & \mathrm{~V}^{-}=0 \mathrm{~V} \end{aligned}$ | $\begin{gathered} 2.3 \\ \mathbf{2 . 4 5} \end{gathered}$ |  |  | V |
|  |  | $\begin{aligned} & \mathrm{V}^{+}=5 \mathrm{~V} \\ & \mathrm{~V}^{-}=0 \mathrm{~V} \end{aligned}$ | $\begin{gathered} 4.3 \\ \mathbf{4 . 4 5} \end{gathered}$ |  |  | V |
|  |  | $\begin{aligned} & \mathrm{V}^{+}=10 \mathrm{~V} \\ & \mathrm{~V}^{-}=0 \mathrm{~V} \end{aligned}$ | $\begin{gathered} 9.3 \\ \mathbf{9 . 4 5} \end{gathered}$ |  |  | V |

## AC Electrical Characteristics

Unless otherwise specified, all limits guaranteed for $T_{J}=25^{\circ} \mathrm{C}, \mathrm{V}+=3 \mathrm{~V}, \mathrm{~V}^{-}=0 \mathrm{~V}, \mathrm{~V}_{\mathrm{CM}}=\mathrm{V}_{\mathrm{O}}=\mathrm{V}^{+} / 2, \mathrm{~V}_{\mathrm{PD}}=0.6 \mathrm{~V}$ and $\mathrm{R}_{\mathrm{L}}$ $>1 \mathrm{M} \Omega$. Boldface limits apply at the temperature extremes (Note 16).

| Symbol | Parameter | Conditions | $\begin{gathered} \text { Typ } \\ \text { (Note 5) } \end{gathered}$ | LMC6681AI <br> LMC6682AI <br> LMC6684AI <br> Limit <br> (Note 6) | LMC6681BI <br> LMC6682BI <br> LMC6684BI <br> Limit <br> (Note 6) | Units |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| ${ }^{\text {toN }}$ | Time Delay for Device to Power ON | (Note 15) | 50 | 200 | 200 | $\mu \mathrm{s}$ |
| $t_{\text {OFF }}$ | Time Delay for Device to Power OFF | (Note 15) | 0.5 | 2 | 2 | $\mu \mathrm{S}$ |
| SR | Slew Rate | (Note 8) | 1.2 | $\begin{gathered} 0.7 \\ \mathbf{0 . 5 5} \end{gathered}$ | $\begin{gathered} 0.7 \\ \mathbf{0 . 5 5} \end{gathered}$ | $\begin{gathered} \mathrm{V} / \mu \mathrm{s} \\ \mathrm{~min} \end{gathered}$ |
|  |  | $\mathrm{V}^{+}=10 \mathrm{~V}$, (Note 10) | 1.2 | $\begin{gathered} 0.7 \\ \mathbf{0 . 5 5} \end{gathered}$ | $\begin{gathered} 0.7 \\ \mathbf{0 . 5 5} \end{gathered}$ |  |
| GBW | Gain-Bandwidth Product |  | 1.2 |  |  | MHz |
| $\phi_{\mathrm{m}}$ | Phase Margin |  | 50 |  |  | Deg |
| $\mathrm{G}_{\mathrm{m}}$ | Gain Margin |  | 12 |  |  | dB |
|  | Amp-to-Amp Isolation | $\mathrm{V}+=10 \mathrm{~V}$ (Note 9) | 130 |  |  | dB |
| $e_{n}$ | Input-Referred Voltage Noise | $\begin{aligned} & f=1 \mathrm{kHz} \\ & V_{C M}=0.5 \mathrm{~V} \end{aligned}$ | 32 |  |  | $\frac{\mathrm{nV}}{\sqrt{\mathrm{Hz}}}$ |
| $\mathrm{i}_{\mathrm{n}}$ | Input-Referred Current Noise | $\mathrm{f}=1 \mathrm{kHz}$ | 0.5 |  |  | $\frac{\mathrm{fA}}{\sqrt{\mathrm{Hz}}}$ |
| T.H.D. | Total Harmonic Distortion | $\begin{aligned} & f=1 \mathrm{kHz}, \mathrm{~A}_{\mathrm{V}}=+1 \\ & \mathrm{R}_{\mathrm{L}}=10 \mathrm{k} \Omega, \mathrm{~V}_{\mathrm{O}}=2 \mathrm{~V}_{\mathrm{PP}} \end{aligned}$ | 0.01 |  |  | \% |

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating ratings indicate conditions for which the device is intended to be functional, but specific performance is not guaranteed. For guaranteed specifications and the test conditions, see the electrical characteristics. Note 2: Human body model, $1.5 \mathrm{k} \Omega$ in series with 100 pF .
Note 3: Applies to both single-supply and split-supply operation. Continous short circuit operation at elevated ambient temperature can result in exceeding the maximum allowed junction temperature of $150^{\circ} \mathrm{C}$. Output current in excess of $\pm 30 \mathrm{~mA}$ over long term may adversely affect reliability
Note 4: The maximum power dissipation is a function of $T_{J}(\max ), \theta_{J A}$, and $T_{A}$. The maximum allowable power dissipation at any ambient temperature is $P_{D}=$ $\left(T_{J(\max )}-T_{A}\right) / \theta_{J A}$. All numbers apply for packages soldered directly into a PC board.
Note 5: Typical Values represent the most likely parametric norm.
Note 6: All limits are guaranteed by testing or statistical analysis.
Note 7: $\mathrm{V}^{+}=3 \mathrm{~V}, \mathrm{~V}_{\mathrm{CM}}=0.5 \mathrm{~V}$. For sourcing and sinking, $0.5 \mathrm{~V} \leq \mathrm{V}_{\mathrm{O}} \leq 2.5 \mathrm{~V}$.
Note 8: $\mathrm{V}^{+}=3 \mathrm{~V}$. Connected as Voltage Follower with 2 V step input, and the output is measured from $15 \%-85 \%$. Number specified is the slower of the positive or negative slew rates.
Note 9: Input referred, $\mathrm{V}^{+}=10 \mathrm{~V}$, and $\mathrm{R}_{\mathrm{L}}=100 \mathrm{k} \Omega$ connected to 5 V . Each amp excited in turn with 1 kHz to produce $\mathrm{V}_{\mathrm{O}}=2 \mathrm{~V}_{\mathrm{PP}}$.
Note 10: $\mathrm{V}^{+}=10 \mathrm{~V}$. Connected as voltage follower with 8 V step Input, and output is measured from $15 \%-85 \%$. Number specified is the slower of the positive or negative slew rates.
Note 11: Limiting input pin current is only necessary for input voltages that exceed absolute maximum input voltage ratings.
Note 12: Guaranteed limits are dictated by tester limitations and not device performance. Actual performance is reflected in the typical value
Note 13: $\mathrm{CMRR}^{+}$and CMRR ${ }^{-}$are tested, and the number indicated is the lower of the two values. For CMRR,$+ \mathrm{V}^{+} / 2<\mathrm{V}_{\mathrm{CM}}<\mathrm{V}^{+}$for $1.8 \mathrm{~V}, 2.2 \mathrm{~V}, 3 \mathrm{~V}, 5 \mathrm{~V}$, and 10 V . For $\mathrm{CMRR}^{-}, 0<\mathrm{V}_{\mathrm{CM}}<\mathrm{V}^{+} / 2$ for $3 \mathrm{~V}, 5 \mathrm{~V}$ and 10 V . For 1.8 V and $2.2 \mathrm{~V}, 0.25<\mathrm{V}_{\mathrm{CM}}<\mathrm{V}^{+}-0.3$.
Note 14: $\mathrm{V}^{+}=10 \mathrm{~V}, \mathrm{~V}_{\mathrm{CM}}=0.5 \mathrm{~V}$. For Sourcing tests, $1 \mathrm{~V} \leq \mathrm{V}_{\mathrm{O}} \leq 5 \mathrm{~V}$. For Sinking tests, $5 \mathrm{~V} \leq \mathrm{V}_{\mathrm{O}} \leq 9 \mathrm{~V}$.
Note 15: The propogation delays are measured using an input waveform of $f=5 \mathrm{~Hz}$, and magnitude of 2.4 V . Refer to Section 6.3 and Figures 14,15 for a detailed explanation.
Note 16: The $\mathrm{V}_{\mathrm{PD}}$ (threshold low and threshold high) limits are guaranteed at room temperature and at temperature extremes. Room temperature limits are production tested. Limits at temperature extremes are guaranteed via correlation using temperature regression analysis methods. Refer to Section 6.2 for an overview of the threshold voltages.

## Typical Performance Characteristics

$\mathrm{V}_{\mathrm{S}}{ }^{+}=3 \mathrm{~V}$, Single Supply, $\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$ unless otherwise specified




Frequency Response vs Temperature



## Frequency Response

 vs $R_{L}$

$\mathrm{Vcm},(\mathrm{V})$




## Application Information

### 1.0 Input Common-Mode Voltage Range

The LMC6681/2/4 has a rail-to-rail input common-mode voltage range. Figure 1 shows an input voltage exceeding both supplies with no resulting phase inversion on the output.


TL/H/12042-5
FIGURE 1. An Input Signal Exceeds the LMC6681/2/4 Power Supply Voltages with No Output Phase Inversion

The absolute maximum input voltage at $\mathrm{V}^{+}=3 \mathrm{~V}$ is 300 mV beyond either supply rail at room temperature. Voltages greatly exceeding this absolute maximum rating, as in Figure 2, can cause excessive current to flow in or out of the input pins, possibly affecting reliability. The input current can be externally limited to $\pm 5 \mathrm{~mA}$, with an input resistor, as shown in Figure 3.


FIGURE 2. A $\pm 7.5 \mathrm{~V}$ Input Signal Greatly Exceeds the 3V Supply in Figure 3, Causing No Phase Inversion Due to $\mathbf{R}_{\mathbf{I}}$


TL/H/12042-7
FIGURE 3. Input Current Protection for Voltages Exceeding the Supply Voltage

### 2.0 Rail-to-Rail Output

The approximated output resistance of the LMC6681/2/4 is $50 \Omega$ sourcing, and $50 \Omega$ sinking at $V_{S}=3 \mathrm{~V}$. The maximum output swing can be estimated as a function of load using the calculated output resistance.

### 3.0 Low Voltage Operation

The LMC6682 operates at supply voltages of 2.2 V and 1.8 V . These voltages represent the End of Discharge voltages of several popular batteries. The amplifier can operate from 1 Lead-Acid or Lithium Ion battery, or 2NiMH, NiCd, or Carbon-Zinc batteries. Nominal and End of Discharge of Voltage of several batteries are listed below.

| Battery Type | Nominal Voltage | End of Discharge <br> Voltage |
| :--- | :---: | :---: |
| NiMH | 1.2 V | 1 V |
| NiCd | 1.2 V | 1 V |
| Lead-Acid | 2 V | 1.8 V |
| Silver Oxide | 1.6 V | 1.3 V |
| Carbon-Zinc | 1.5 V | 1.1 V |
| Lithium | $2.6 \mathrm{~V}-3.6 \mathrm{~V}$ | $1.7 \mathrm{~V}-2.4 \mathrm{~V}$ |

At $\mathrm{V}_{\mathrm{S}}=2.2 \mathrm{~V}$, the LMC6681/2/4 has a rail-to-rail input common-mode voltage range. Figure 4 shows an input voltage extending to both supplies and the resulting output.


FIGURE 4. The Input Common-Mode Voltage Range Extends to Both Supplies at $\mathbf{V}_{\mathbf{S}}=\mathbf{2 . 2 V}$
The amplifier is operational at $\mathrm{V}_{\mathrm{S}}=1.8 \mathrm{~V}$, with guaranteed input common-mode voltage range, output swing, and CMRR specs. Figure 5 shows the response of the LMC6681/2/4 at $\mathrm{V}_{\mathrm{S}}=1.8 \mathrm{~V}$.


FIGURE 5. Response of the LMC6681/2/4 at $V_{S}=1.8 \mathrm{~V}$

## Application Information (Continued)

Figure 6 shows an input voltage exceeding both supplies with no resulting phase inversion on the output.


FIGURE 6. An Input Voltage Signal Exceeds LMC6681/2/4 Power Supply Voltages of $\mathrm{V}_{\mathbf{S}}=1.8 \mathrm{~V}$ with No Output Phase Inversion

### 4.0 Capacitive Load Tolerance

The LMC6681/2/4 can typically drive a 100 pF load with $\mathrm{V}_{\mathrm{S}}$ $=10 \mathrm{~V}$ at unity gain without oscillating. The unity gain follower is the most sensitive configuration to capacitive load. Direct capacitive loading reduces the phase margin of opamps. The combination of the op-amp's output impedance and the capacitive load induces phase lag. This results in either an underdamped pulse response or oscillation.
Capacitive load compensation can be accomplished using resistive isolation as shown in Figure 7. If there is a resistive component of the load in parallel to the capacitive component, the isolation resistor and the resistive load create a voltage divider at the output. This introduces a DC error at the output.


TL/H/12042-11
FIGURE 7. Resistive Isolation of a $\mathbf{3 5 0} \mathbf{~ p F}$ Capacitive Load

Figure 8 displays the pulse response of the LMC6681 circuit in Figure 7.


Another circuit, shown in Figure 9, is also used to indirectly drive capacitive loads. This circuit is an improvement to the circuit shown Figure 7 because it provides DC accuracy as well as AC stability. R1 and C1 serve to counteract the loss of phase margin by feeding the high frequency component of the output signal back to the amplifiers inverting input, thereby preserving phase margin in the overall feedback loop. The values of R1 and C1 should be experimentally determined by the system designer for the desired pulse response. Increased capacitive drive is possible by increasing the value of the capacitor in the feedback loop.


FIGURE 9. The LMC6682 Compensated to Ensure DC Accuracy and AC Stability

The pulse response of the circuit shown in Figure 9 is shown in Figure 10.


TL/H/12042-14
FIGURE 10. Pulse Response of the LMC6682 Circuit Shown in Figure 9

## Application Hints

### 5.0 Printed-Circuit-Board Layout for High-Impedance Work

It is generally recognized that any circuit which must operate with less than 1000 pA of leakage current requires special layout of the PC board. When one wishes to take advantage of the ultra-low input current of the LMC6681/2/4, typically less than 80 fA , it is essential to have an excellent layout. Fortunately, the techniques of obtaining low leakages are quite simple. First, the user must not ignore the surface leakage of the PC board, even though it may sometimes appear acceptably low, because under conditions of high humidity or dust or contamination, the surface leakage will be appreciable.
To minimize the effect of any surface leakage, lay out a ring of foil completely surrounding the LMC6681/2/4's inputs and the terminals of capacitors, diodes, conductors, resistors, relay terminals, etc. connected to the op-amp's inputs, as in Figure 11. To have a significant effect, guard rings should be placed in both the top and bottom of the PC board. This PC foil must then be connected to a voltage which is at the same voltage as the amplifier inputs, since no leakage current can flow between two points at the same potential. For example, a PC board trace-to-pad resistance of $10^{12} \Omega$, which is normally considered a very large resistance, could leak 5 pA if the trace were a 5 V bus adjacent to the pad of the input. This would cause a 60 times degradation from the LMC6681/2/4's actual performance. However, if a guard ring is held within 5 mV of the inputs, then even a resistance of $10^{11} \Omega$ would cause only 0.05 pA of leakage current. See Figures 12a, 12b, and 12c for typical connections of guard rings for standard op-amp configurations.


FIGURE 11. Example of Guard Ring in PC Board Layout


TL/H/12042-19
(a) Inverting Amplifier

(b) Non-Inverting Amplifier

(c) Follower

FIGURE 12. Typical Connections of Guard Rings
The designer should be aware that when it is inappropriate to lay out a PC board for the sake of just a few circuits, there is another technique which is even better than a guard ring on a PC board: Don't insert the amplifier's input pin into the board at all, but bend it up in the air and use only air as an insulator. Air is an excellent insulator. In this case you may have to forego some of the advantages of PC board construction, but the advantages are sometimes well worth the effort of using point-to-point up-in-the-air wiring. See Figure 13.

(Input pins are lifted out of PC board and soldered directly to components. All other pins are connected to PC board.)

FIGURE 13. Air Wiring

## Application Hints (Continued)

### 6.0 Powerdown

### 6.1 PINOUT FOR THE LMC6681/LMC6682/LMC6684

For the LMC6681/2/4, the input, output, and power pins are the same as those used in the standard configuration. One of the other pins, pin 5 in the case of the LMC6681, is used to enable the powerdown mode. The connection diagrams for the LMC6681/2/4 are on the front page of the datasheet.
The LMC6684 has 2 powerdown options. Each of the powerdown pins disables two amplifiers. If both the powerdown pins are pulled high, all four amplifiers will be disabled. Referring to the connection diagrams on the front page of the datasheet, Pin 5 disables amplifiers B and C and Pin 13 disables amplifiers A and D.

### 6.2 EXPLANATION OF DATASHEET PARAMETERS

The LMC6681/2/4 is ON (meets all the datasheet specs) when the voltage applied to the powerdown pin, $\mathrm{V}_{\mathrm{PD}}$ is a logic low. The device is OFF when $V_{P D}$ is a logic high. These logic levels are indicated in the test conditions in the datasheet tables. Summarizing these numbers:

| Supply <br> Voltage | Logic High [V] |  | Logic Low [V] |  |
| :---: | :---: | :---: | :---: | :---: |
|  | at room | over temp | at room | over temp |
| 2.2 V | $V_{P D} \geq 1.5$ | $V_{P D} \geq 1.65$ | $V_{P D} \leq 0.4$ | $V_{P D} \leq 0.25$ |
| $3 V$ | $V_{P D} \geq 2.3$ | $V_{P D} \geq 2.45$ | $V_{P D} \leq 0.6$ | $V_{P D} \leq 0.45$ |
| 5 V | $V_{P D} \geq 4.3$ | $V_{P D} \geq 4.45$ | $V_{P D} \leq 0.9$ | $V_{P D} \leq 0.75$ |
| 10 V | $V_{P D} \geq 9.3$ | $V_{P D} \geq 9.45$ | $V_{P D} \leq 1.2$ | $V_{P D} \leq 1.05$ |

In applications where the powerdown pin is not connected externally, it is pulled to a logic low internally through a current source. The $\mathrm{t}_{\mathrm{ON}}$ and toff specs will essentially be the same for a $V_{P D}$ in the specified range. This means that the LMC6681/2/4 will typically be fully operational $50 \mu \mathrm{~s}$ after a logic low has been applied to the powerdown pin. Please note that the frequency of $V_{P D}$ in the test circuit below is 5 Hz .

### 6.3 TEST CIRCUIT TO MEASURE ton AND toff

The circuit used to measure the $t_{O N}$, and $t_{\text {OFF }}$ during the powerdown operation is a voltage follower with a load of $2 \mathrm{k} \Omega$ as shown in Figure 14.
When the input to the powerdown pin is low, the LMC6681/2/4 is on. Since the amplifier is connected in the voltage follower configuation, the output of the circuit is -1 V . When the powerdown pin is pulled high, the amplifier shuts down, and draws less than $1 \mu \mathrm{~A} /$ Amplifier. In this powerdown mode, the output pin has high impedance, and the output of the circuit is pulled to 0 V . toN is specified as the time between the $50 \%$ points of the trailing edges of the input waveform at the powerdown pin, and the waveform at the output pin. Similarly, the toff is specified as the time between the $50 \%$ points of the leading edges of the input waveform at the powerdown pin, and the waveform at the output pin.


TL/H/12042-16
FIGURE 14. Test Circuit for ton and toff Measurements



TL/H/12042-29
(b) toN Measurement

FIGURE 15

## Application Hints (Continued)

### 6.0 Powerdown (Continued)

## 6.4 ton $_{\text {and }}$ tofF

The ton (time delay for device to power on) the toff (time delay for device to power off) specs are guaranteed at a supply voltage of 3 V . The $\mathrm{t}_{\mathrm{ON}}$ and $\mathrm{t}_{\text {OFF }}$ spec are independent of the $\mathrm{V}_{\mathrm{PD}}$ applied in the specified range. Refer to the Powerdown DC Threshold Characteristics table for the values for a logic low and a logic high.
The guaranteed spec for toN is $200 \mu \mathrm{~s}$. This does not mean that the signal to the VPD pin can be as high as 5 kHz $(1 / 200 \mu \mathrm{~s})$. Note that the $\mathrm{V}_{\mathrm{PD}}$ frequency for the t ( and $t_{\text {OFF }}$ measurements is 5 Hz . The LMC6681/2/4 is ideal for DC type applications where the powerdown pin is controlled by low frequency signals.
When the LMC6681/2/4 is powered off, internal bias currents are shutoff. There is a inherent latency in the circuit, and the device has to power off for a certain period of time for the $\mathrm{t}_{\mathrm{ON}} \mathrm{spec}$ to apply. Refer to the figure below. tpD OFF refers to the time interval for which the device is in the powerdown mode. Consider the case when the device has been powered off for 5 ms , and then the powerdown pin is pulled to a logic low. From Figure 16, at room temperature, the device powers on after $500 \mu \mathrm{~s}$.


FIGURE 16. ton Delay Till Active-On after tpdoff in Powerdown Mode, $\mathbf{V}_{\mathbf{S}}=3 \mathbf{V}$

### 7.0 Compensating for Input Capacitance

It is quite common to use large values of feedback resistance with amplifiers that have ultra-low input current, like the LMC6681/2/4. Large feedback resistors can react with small values of input capacitance due to transducers, photodiodes, and circuits board parasitics to reduce phase margins.


TL/H/12042-15
FIGURE 17. Canceling the Effect of Input Capacitance
The effect of input capacitance can be compensated for by adding a feedback capacitor. The feedback capacitor (as in Figure 17), $\mathrm{C}_{\mathrm{F}}$, is first estimated by:

$$
\begin{gathered}
\frac{1}{2 \pi R_{1} C_{I N}} \geq \frac{1}{2 \pi R_{2} C_{F}} \\
\quad \text { or } \\
R_{1} C_{I N} \leq R_{2} C_{F}
\end{gathered}
$$

which typically provides significant overcompensation.
Printed circuit board stray capacitance may be larger or smaller than that of a breadboard, so the actual optimum value for $C_{F}$ may be different. The values of $C_{F}$ should be checked on the actual circuit. (Refer to the LMC660 quad CMOS amplifier data sheet for a more detailed discussion.)

### 8.0 Spice Macromodel

A Spice Macromodel is available for the LMC6681/2/4. The model includes a simulation of:

- Input common-mode voltage range
- Frequency and transient response
- GBW dependence on loading conditions
- Quiescent and dynamic supply current
- Output swing dependence on loading conditions
and many more characteristics as listed on the macromodel disk.
Contact the National Semiconductor Customer Response Center at 1-800-272-9959 to obtain an operational amplifier spice macromodel library disk.


## Applications

## Transducer Interface Circuits

## A. PIEZOELECTRIC TRANSDUCERS



FIGURE 18. Transducer Interface Application
The LMC6681 can be used for processing of transducer signals as shown in the circuit below. The two $11 \mathrm{M} \Omega$ resistors provide a path for the DC currents to ground. Since the resistors are bootstrapped to the output, the AC input resistance of the LMC6681 is much higher.


TL/H/12042-36
FIGURE 19. LMC6681 Used for Signal Processing
An input current of 80 fA and a CMRR of 82 dB causes an insignificant error offset voltage at the output. The rail-to-rail performance of the amplifier also provides the maximum dynamic range for the transducer signals.

## B. PHOTODIODE AMPLIFIERS



TL/H/12042-26 FIGURE 20. Photodiode Amplifier

Photocells can be used in light measuring instruments. An error offset voltage is produced at the output due to the input current and the offset voltage of the amplifier. The LMC6682, which can be operated off a single battery is an excellent choice for this application with its 80 fA input current and 0.5 mV offset voltage.

## Low Voltage Peak Detector



## FIGURE 21. Low Voltage Peak Detector

The accuracy of the peak detector is dependent on the leakage currents of the diodes and the capacitors, and the non-idealities of the amplifier. The parameters of the amplifier which can limit the performance of this circuit are (a) Finite slew rate, (b) Input current, and (c) Maximum output current of the amplifier.
The input current of the amplifier causes a slow discharge of the capacitor. This phenomenon is called "drooping". The LMC6682 has a typical input current of 80 fA . This would cause the capacitor to droop at a rate of $\mathrm{dV} / \mathrm{dt}=\mathrm{I}_{\mathrm{B}} / \mathrm{C}=$ $80 \mathrm{fA} / 100 \mathrm{pF}=0.8 \mathrm{mV} / \mathrm{s}$. Accuracy in the amplitude measurement is also maintained by an offset voltage of 0.5 mV , and an open-loop gain of 120 dB .

## Oscillators



TL/H/12042-30
FIGURE 22. 1 Hz Square—Wave Oscillator

## Applications (Continued)

For single supply 5 V operation, the output of the circuit will swing from 0 V to 5 V . The voltage divider set up $\mathrm{R}_{2}, \mathrm{R}_{3}$ and $R_{4}$ will cause the non-inverting input of the LMC6681/2/4 to move from $1.67 \mathrm{~V}(1 / 3$ of 5 V$)$ to $3.33 \mathrm{~V}(2 / 3$ of 5 V$)$. This voltage behaves as the threshold voltage.
$\mathrm{R}_{1}$ and $\mathrm{C}_{1}$ determine the time constant for the circuit. The frequency of oscillation, fOSc is $\left(\frac{1}{2 \Delta t}\right)$, where $\Delta \mathrm{t}$ is the time
the amplifier input takes to move from 1.67 V to 3.33 V . The calculations are shown below.

$$
\begin{aligned}
& 1.67=5\left(1-e-\frac{t_{1}}{\tau}\right) \\
& \text { where } \tau=\mathrm{RC}=0.68 \text { seconds } \\
& \rightarrow t_{1}=0.27 \text { seconds. } \\
& \text { and } \\
& 3.33=5\left(1-\mathrm{e}-\frac{\mathrm{t}_{2}}{\tau}\right) \\
& \rightarrow t_{2}=0.74 \text { seconds } \\
& \text { Then, } \mathrm{f} \text { OSC }=\left(\frac{1}{2 \Delta \mathrm{t}}\right) \\
& =\frac{1}{2(0.74-0.27)} \\
& \cong 1 \mathrm{~Hz}
\end{aligned}
$$

## LMC6681/2/4 as a Comparator



TL/H/12042-31

## FIGURE 23. Comparator with Hysteresis

Figure 23 shows the application of the LMC6681/2/4 as a comparator. The hysteresis is determined by the ratio of the two resistors. Since the supply current of the LMC6681/2/4 is less than 1 mA , it can be used as a low power comparator, in applications where the quiescent current is an important parameter. At $\mathrm{V}_{\mathrm{S}}=3 \mathrm{~V}$, typical propagation delays would be on the order of $\mathrm{t}_{\mathrm{PHL}}=6 \mu \mathrm{~s}$, and $\mathrm{t}_{\mathrm{PLH}}=5 \mu \mathrm{~s}$.

Filters


TL/H/12042-32
FIGURE 24. Wide-Band Band-Pass Filter
The filter shown in Figure 24 is used to process "voiceband" signals. The bandpass filter has a gain of 40 dB . The two corner frequencies, $f_{1}$ and $f_{2}$ are calculated as

$$
\begin{aligned}
& \mathrm{f}_{1}=\frac{1}{2 \pi \mathrm{R}_{1} \mathrm{C}_{1}}=\frac{1}{2 \pi(10 \mathrm{k} \Omega)(79 \mathrm{nF})}=200 \mathrm{~Hz} \\
& \mathrm{f}_{2}=\frac{1}{2 \pi \mathrm{R}_{2} \mathrm{C}_{2}}=\frac{1}{2 \pi(1 \mathrm{M} \Omega)(40 \mathrm{pF})}=4 \mathrm{kHz}
\end{aligned}
$$

The LMC6681/2/4, with its rail-to-rail input common-mode voltage range and high gain ( 120 dB typical, $R_{L}=10 \mathrm{k} \Omega$ ) is extremely well suited for such filter applications. The rail-torail input range allows for large input signals to be processed without distortion. The high gain means that the circuit can provide filtering and gain in one stage, instead of the typical two stage filter. This implies a reduction in cost, and savings of space and power.
This is an illustration of the conceptual use of the LMC6681/2/4. The selectivity of the filter can be improved by increasing the order (number of poles) of the design.

## Sample-and-Hold Circuits



FIGURE 25. Sample-and-Hold Application
When the "Switch" is closed during the Sample Interval, $\mathrm{C}_{\text {HOLD }}$ charges up to the value of the input signal when the "Switch" is open, CHOLD retains this value as it is buffered by the high input impedance of the LMC6681.

## Applications (Continued)

Errors in the "hold" voltage are caused by the input current of the amplifier, the leakage current of the CD4066, and the leakage current of the capacitor. While an input current of 80 fA minimizes the accumulation rate for error in this circuit, the LMC6681's CMRR of 82 dB allows excellent accuracy throughout the amplifier's rail-to-rail dynamic capture range.

## Battery Monitoring Circuit



FIGURE 26a. Circuit Used to Sense Charging


FIGURE 26b. Circuit Used to Sense Discharging

The LMC6681/2/4 has been optimized for performance at 3 V , and also has guaranteed specs at 1.8 V and 2.2 V . In portable applications, the R ROAD represents the laptop/ notebook, or any other computer which the battery is powering. A desired output voltage can be achieved by manipulating the ratios of the feedback resistors. During the charging cycle, the current flows out of the battery as shown. While during discharge, the current is in the reverse direction. Since the current can range from a few milliamperes to amperes, the amplifier will have to sense a signal below ground during the discharge cycle. At 3V, the LMC6681/2/4 can accept a signal up to 300 mV below ground. The commonmode voltage range of the LMC6681/2/4, which extends beyond both rails, is thus a very useful feature in this application.
A typical offset voltage of 0.5 mV , and CMRR of 82 dB maintain accuracy in the circuit output, while the rail-to-rail output performance allows for a maximum signal range.

## Physical Dimensions inches (millimeters)



8-Pin Small Outline Package
Order Number LMC6681AIM or LMC6681BIM
NS Package Number M08A


Physical Dimensions inches (millimeters) (Continued)


## 16-Pin Molded Dual-In-Line Package Order Number LMC6684AIN or LMC6684BIN <br> NS Package Number N16A

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| :---: | :---: | :---: | :---: | :---: | :---: | :---: |

## General Description

The LMC6953 is a voltage supervisory chip designed to meet PCI (Peripheral Component Interconnect) Specifications Revision 2.1. It monitors 5 V and 3.3 V power supplies. In cases of power-up, power-down, brown-out, power failure and manual reset interrupt, the LMC6953 provides an active low reset. $\overline{\text { RESET }}$ holds low for 100 ms after both 5 V and 3.3 V powers recover, or after manual reset signal returns to high state. The external capacitor on pin 8 adjusts the reset delay.
This part is ideal on PCI motherboards or add-in cards to ensure the integrity of the entire system when there is a fault condition. The active low reset sets the microprocessor or local device in a known state.

The LMC6953 has a built-in bandgap reference that accurately determines all the threshold voltages. The internal reset delay circuitry eliminates additional discrete components.

## Features

- Compliant to PCI specifications revision 2.1.

■ Under and over voltage detectors for 5 V and 3.3 V

- Power failure detection ( 5 V falling under 3.3 V by 300 mV max)
- Manual reset input pin

■ Guaranteed $\overline{\text { RESET }}$ assertion at $\mathrm{V}_{\mathrm{DD}}=1.5 \mathrm{~V}$

- Integrated reset delay circuitry
- Open drain output
- Adjustable reset delay
- Response time for over and under voltage detection

490 ns Max
■ Power failure response time 90 ns Max

- Requires minimal external components


## Applications

■ Desktop PCs

- PCI-Based Systems

■ Network servers

## Typical Application Circuits




Absolute Maximum Ratings (Note 1)
If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.
ESD Tolerance (Note 2)
Human Body Model 2 kV
Machine Model 200V
Voltage at Input Pin 7V
Supply Voltage 7V
Current at Output Pin 15 mA
Current at Power Supply Pin (Note 3) 10 mA

| Lead Temp. (Soldering, 10 sec . | $260^{\circ} \mathrm{C}$ |
| :---: | :---: |
| Storage Temperature Range | $-65^{\circ} \mathrm{C}$ to $+150^{\circ} \mathrm{C}$ |
| Junction Temperature | $150^{\circ} \mathrm{C}$ |
| Operating Ratings (Note 1) |  |
| Supply Voltage | 1.5 V to 6 V |
| Junction Temperature Range LMC6953C | $0^{\circ} \mathrm{C} \leq \mathrm{T}_{\mathrm{J}} \leq 70^{\circ} \mathrm{C}$ |
| Thermal Resistance ( $\theta_{\mathrm{JA}}$ ) M Package | $165^{\circ} \mathrm{C} / \mathrm{W}$ |

## DC Electrical Characteristics

Unless otherwise specified, all boldface limits guaranteed for $T_{J}=0^{\circ} \mathrm{C}$ to $70^{\circ} \mathrm{C}, \mathrm{V}_{\mathrm{DD}}=5 \mathrm{~V}, \mathrm{R}_{P U L L-U P}=4.7 \mathrm{k} \Omega$ and $\mathrm{C}_{E X T}=$ $0.01 \mu \mathrm{~F}$. Typical numbers are room temperature $\left(25^{\circ} \mathrm{C}\right)$ performance.

| Symbol | Parameter | Conditions | Min | Typ | Max | Units |
| :--- | :--- | :--- | :--- | :--- | :---: | :---: |
| $\mathrm{V}_{\mathrm{H} 5}$ | $\mathrm{~V}_{\mathrm{DD}}$ Over-Voltage Threshold | (Note 4) | $\mathbf{5 . 4 5}$ | 5.6 | $\mathbf{5 . 7 5}$ | V |
| $\mathrm{~V}_{\mathrm{L} 5}$ | $\mathrm{~V}_{\mathrm{DD}}$ Under-Voltage Threshold | (Note 4) | $\mathbf{4 . 2 5}$ | 4.4 | $\mathbf{4 . 5 5}$ | V |
| $\mathrm{~V}_{\mathrm{H} 3.3}$ | 3.3 V Over-Voltage Threshold | (Note 5) | $\mathbf{3 . 8}$ | 3.95 | $\mathbf{4 . 1}$ | V |
| $\mathrm{~V}_{\mathrm{L} 3.3}$ | 3.3 V Under-Voltage Threshold | (Note 5) | $\mathbf{2 . 5}$ | 2.65 | $\mathbf{2 . 8}$ | V |
| $\mathrm{~V}_{\mathrm{MR}}$ | Manual RESET Threshold |  |  | 2.5 | $\mathbf{2 . 8}$ | V |
| $\mathrm{~V}_{\mathrm{PF}}$ | Power Failure Differential Voltage <br> $(3.3 V$ Pin-5V Pin) | (Note 6) |  | 150 | $\mathbf{3 0 0}$ | mV |
| $\mathrm{R}_{\mathrm{IN}}$ | Input Resistance at 5V and 3.3V Pins |  |  | 35 |  | $\mathrm{k} \Omega$ |
| $\mathrm{V}_{\mathrm{OL}}$ | RESET Output Low | $\mathrm{V}_{\mathrm{DD}}=1.5 \mathrm{~V}$ to 6 V |  | 0.05 | $\mathbf{0 . 1}$ | V |
| $\mathrm{I}_{\mathrm{S}}$ | Supply Current | (Note 3) |  | 0.8 | $\mathbf{1 . 5}$ | mA |

## AC Electrical Characteristics

Unless otherwise specified, all boldface limits guaranteed for $T_{J}=0^{\circ} \mathrm{C}$ to $70^{\circ} \mathrm{C}, \mathrm{V}_{\mathrm{DD}}=5 \mathrm{~V}$, RPULL-UP $=4.7 \mathrm{k} \Omega$ and $\mathrm{C}_{\mathrm{EXT}}=$ $0.01 \mu \mathrm{~F}$. Typical numbers are room temperature $\left(25^{\circ} \mathrm{C}\right)$ performance.

| Symbol | Parameter | Conditions | Typ | LMC6953 <br> Limit | Units |
| :--- | :--- | :--- | :---: | :---: | :---: |
| $t_{D}$ | Over or Under Voltage Response Time | (Note 7) | 150 | $\mathbf{4 9 0}$ | ns <br> $\max$ |
| $t_{\text {PF }}$ | Power Failure Response Time | $($ Note 8$)$ | 40 | $\mathbf{9 0}$ | ns <br> $\max$ |
| $t_{\text {RESET }}$ | Reset Delay | $\mathrm{C}_{\mathrm{EXT}}=0.01 \mu \mathrm{~F}$ | 100 |  | ms |

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but specific performance is not guaranteed. For guaranteed specifications and the test conditions, see the Electrical Characteristics. Note 2: Human body model, $1.5 \mathrm{k} \Omega$ in series with 100 pF . Machine model. $200 \Omega$ in series with 100 pF .
Note 3: Supply current measured at pins 1, 2, and 3 . The $4.7 \mathrm{k} \Omega$ pull-up resistor on pin 7 is not tied to $V_{D D}$ in this measurement.
Note 4: PCI Specifications Revision 2.1, Section 4.2.1.1 and Section 4.3.2.
Note 5: PCI Specifications Revision 2.1, Section 4.2.2.1 and Section 4.3.2.
Note 6: PCI Specifications Revision 2.1 and Section 4.3.2.
Note 7: PCI Specifications Revision 2.1, Section 4.3.2. The response time is measured individually with $\pm 750 \mathrm{mV}$ of overdrive applied to pin 2 then $\pm 600 \mathrm{mV}$ of overdrive applied to pin 3 and taking the worst number of the four measurements.
Note 8: PCI Specifications Revision 2.1, Section 4.3.2. The power failure response time is measured with a signal changing from 5 V to 3 V applied to pin 2 and a 3.3V DC applied to pin 3.

## LMC6953 Timing Diagram



Note: $t_{\text {RESET }}, t_{D}$ and $t_{\text {PF }}$ are not to scale.

Typical Performance Characteristics Unless otherwise specified, $T_{A}=25^{\circ} \mathrm{C}$


TL/H/12846-4


TL/H/12846-9

TL/H/12846-6



TL/H/12846-5


TL/H/12846-7

Typical Performance Characteristics Unless otherwise specified, $T_{A}=25^{\circ} \mathrm{C}$ (Continued)


TL/H/12846-8


TL/H/12846-14


TL/H/12846-19


TL/H/12846-13

TL/H/12846-15
$I_{\text {OL }}$ vs R PULL-UP


Typical Performance Characteristics Unless otherwise speciifed, $\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$ (Continued)


TL/H/12846-11

## Block Diagram of the LMC6953



TL/H/12846-25
** All five comparators' positive power supplies are connected to $V_{D D}$

## Truth Table

| Power Failure | 5V Over-Voltage | 5V Under-Voltage | 3.3V Over-Voltage | 3.3V Under-Voltage | $\overline{M R}$ | RESET |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| Fail | X | X | X | X | High | Low |
| X | Fail | X | X | X | High | Low |
| X | X | Fail | X | X | High | Low |
| X | X | X | Fail | X | High | Low |
| X | X | X | X | Fail | High | Low |
| X | X | X | X | X | Low | Low |
| OK | OK | OK | OK | OK | High | High |

Pin Description

| Pin | Name | Function |
| :---: | :---: | :--- |
| 1 | $\mathrm{~V}_{\mathrm{DD}}$ | 5V input supply voltage. This pin supplies power to the internal comparators. It can be connected to a <br> capacitor acting as a back-up battery. Otherwise, it should be shorted to the 5 V pin. |
| 2 | 5 V | 5 V input supply voltage. This pin is not connected to the positive power supply of the internal comparators. It <br> provides input signal to the 5 V window comparators as well as the power failure comparator. |
| 3 | 3.3 V | 3.3 V input supply voltage. This pin provides input signal to the 3.3 V window comparators and the power failure <br> comparator. |
| 4 | $\overline{\mathrm{MR}}$ | Manual reset input pin. It takes 5 V CMOS logic low and triggers $\overline{\mathrm{RESET}}$. If not used, this pin should be <br> connected to $\mathrm{V}_{\mathrm{DD}}$. |
| 5 | PWR__GND | Ground. |
| 6 | GND | This pin should be grounded at all times. |
| 7 | $\overline{\text { RESET }}$ | Active low reset output. $\overline{R E S E T}$ holds low for 100 ms after both 5 V and 3.3 V powers recover, or after manual <br> reset signal returns to high state. |
| 8 | $\mathrm{C}_{\text {EXT }}$ | External capacitor pin. The value of $\mathrm{C}_{\text {EXT }}$ sets the reset delay. |

## Application Note

## HOW THE LMC6953 FUNCTIONS

The LMC6953 is a power supply supervisor with its performance specifications compliant to PCI Specifications Revision 2.1. The chip monitors power-up, power-down, brownout, power failure and manual reset interrupt situations.
During power-up, the LMC6953 holds RESET low for 100 ms after both 5 V and 3.3 V are within specified windows. It asserts reset in 490 ns when a brown-out is detected. Brown-out occurs when 5 V supply is above 5.75 V over-voltage or below 4.25 V under-voltage or when 3.3 V supply is above 4.1 V over-voltage or 2.5 V under-voltage. In case of power failure where the 5 V supply falls under 3.3 V supply by 300 mV maximum, reset is asserted in 90 ns . RESET also can be asserted by sending a 5 V CMOS logic low to the manual reset pin.
Each time $\overline{\text { RESET }}$ is asserted, it holds low for 100 ms after a fault condition is recovered. The 100 ms reset delay is generated by the $0.01 \mu \mathrm{~F} \mathrm{C}_{\text {EXT }}$ capacitor, and can be adjusted by changing the value of $\mathrm{C}_{\text {EXT }}$.
It is highly recommended to place lands on printed circuit boards for 120 pF capacitors between pin 2 and ground and also between pin 3 and ground. As power supplies may change abruptly, there can be very high frequency noise present and the capacitors can minimize the noise,

MINIMUM SUPPLY VOLTAGE FOR RESET ASSERTION
The LMC6953 guarantees $\mathrm{V}_{\mathrm{DD}}=1.5 \mathrm{~V}$ as the minimum supply voltage to achieve consistent RESET assertion. This ensures system stability in initialization state.


TL/H/12846-12
FIGURE 1. Output Voltage vs Supply Voltage
Figure 1 is measured by shorting pins 1,2 and 3 together when supply voltage is from 0 V to 3.3 V . Then pin 3 is connected with a constant $3.3 \mathrm{~V}_{\mathrm{DC}}$ and pins 1 and 2 are connected to a separate power supply that continues to vary from 3.3 V to 6 V .

## 5V AND VDD PINS

By having the 5 V and the $\mathrm{V}_{\mathrm{DD}}$ pins separately, a capacitor can be used as a back-up power supply in event of a sudden power supply failure. This circuit is shown in the application circuit section titled "On Motherboard With Capacitor as a Back-up Power Supply." Under normal condition, the diode is forward-biased and the capacitor is charged up to $V_{D D}-0.7 \mathrm{~V}$. If the power supply goes away, the diode becomes reverse-biased, isolating the 5 V and the $\mathrm{V}_{\mathrm{DD}}$ pins. The capacitor provides power to the internal comparators for a short duration for the LMC6953 to operate.

## $\mathrm{C}_{\text {EXt }}$ SETS RESET DELAY IN LINEAR FASHION

The LMC6953 has internal delay circuitry to generate the reset delay. By choosing different values of capacitor $\mathrm{C}_{\mathrm{EXT}}$, reset delay can be programmed to the desired length for the system to stabilize after a fault condition occurs.

## EVALUATING THE LMC6953

To Measure Over-Voltages and Under-Voltages.
Connect a 3.3V DC to the 3.3 V pin and a 5 V DC to the $\mathrm{V}_{\mathrm{DD}}$ and the 5 V pins ( $\mathrm{V}_{\mathrm{DD}}$ and 5 V pins are shorted). $\overline{\text { RESET }}$ output is high because voltages are within window. These voltages should be monitored. While keeping the 3.3 V constant, increase the 5V DC signal until a RESET low is detected. The point on the 5V DC signal at which RESET changes from high to low is the 5 V over-voltage. It is typically 5.6 V . To detect 5 V under-voltage, start the 5 V DC signal from 5 V and decrease it until a RESET low is detected. The point on the 5V DC signal at which RESET changes from high to low is the 5 V under-voltage. It is typically 4.4 V .
To find 3.3 V over-voltage and under-voltage, keep the 5 V $D C$ at 5 V and vary the 3.3 V DC signal until a $\overline{\text { RESET }}$ Iow is detected.

## To Measure Timing Specifications.

For evaluation purposes only, the $\mathrm{V}_{\mathrm{DD}}$ and the 5 V pins should have separate signals. It is easier to measure response time in this manner. The $\mathrm{V}_{\mathrm{DD}}$ pin is connected to a steady 5 V DC and the 5 V pin is connected to a pulse generator. To simulate the power supply voltages going out of window, a pulse generator with disable/enable feature and rise and fall time adjustment is recommended. To measure the RESET signal, a oscilloscope is recommended because of its ability to capture and store a signal.

## Application Note (Continued)

To measure the 5 V under-voltage response time on the LMC6953, set the pulse generator to trigger mode and program the amplitude to have a high value of 5 V and a low value of the 5 V under-voltage threshold measured previously with 50 mV overdrive. For example, if the measured 5 V under-voltage is 4.4 V , then a 50 mV overdrive on this signal is 4.35 V . The disable feature on the pulse generator should be on. Program the fall time of the pulse to be 30 ns and program the scope to trigger on the falling edge, with trigger level of 4.5 V . Set the scope to $200 \mathrm{~ns} /$ division. The probes should be connected to the 5 V pin and the RESET pin. Now enable the 5 V signal from the pulse generator and trigger the signal. Be aware that when the signal is enabled, there is high frequency noise present, and putting a 120 pF capacitor between the 5 V pin and ground suppresses some of the noise. Response time is measured by taking the 5 V under-voltage threshold on the 5 V signal to the point


TL/H/12846-21
FIGURE 2. 5V Under-Voltage Waveforms
where RESET goes low. Figure 2 shows a scope photo of 5 V under-voltage waveforms. It is taken with a signal going from 5 V to 4.25 V at the 5 V pin.
To measure the 100 ms RESET delay, change the scope to $50 \mathrm{~ms} /$ division and trigger the 5 V signal again. RESET should stay low for 100 ms after the 5 V is recovered and within window.
Other over-voltages and under-voltages can be measured by changing the pulse generator to different voltage steps. Putting a 120 pF capacitor between the 3.3 V pin and ground is recommended in evaluating 3.3 V signal.
To measure power-failure response time, set the pulse generator from 5 V to 3 V with fall time of the pulse 3 ns and connect it to the 5 V pin. $\overline{\text { RESET }}$ should go low within 90 ns of power failure. Figure 3 shows a scope photo of power failure waveforms. It is taken with a signal going from 5 V to 3 V at the 5 V pin.


Time ( $40 \mathrm{~ns} / \mathrm{div}$ )
TL/H/12846-22
FIGURE 3. Power Failure Waveforms




LIFE SUPPORT POLICY
NATIONAL'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF THE PRESIDENT OF NATIONAL SEMICONDUCTOR CORPORATION. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and whose failure to perform, when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.


| N |
| :--- | :--- |

## Ordering Information

| Package | Ordering <br> Information | NSC Drawing <br> Number | Package <br> Marking | Supplied As |
| :--- | :--- | :--- | :--- | :--- |
| 5-Pin SOT 23-5 | LMC7215IM5 | MA05A | C02B | 250 Tape and Reel <br> 5-Pin SOT 23-5 |
| LMC7225IM5 | MA05A | C03B | 250 Tape and Reel |  |
| 5-Pin SOT 23-5 | LMC7215IM5X | MA05A | C02B | 3k Tape and Reel |
| 5-Pin SOT 23-5 | LMC7225IM5X | MA05A | C03B | 3k Tape and Reel |
| 8-Pin SO-8 | LMC7215IM | M08A | LMC7215IM | Rails |
| 8-Pin SO-8 | LMC7225IM | M08A | LMC7225IM | Rails |
| 8-Pin SO-8 | LMC7215IMX | M08A | LMC7215IM | 2.5k Tape and Reel |
| 8-Pin SO-8 | LMC7225IMX | M08A | LMC7225IM | 2.5k Tape and Reel |

Absolute Maximum Ratings (Note 1)
If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.
ESD Tolerance (Note 2)
2 kV
Differential Input Voltage $\quad\left(\mathrm{V}_{\mathrm{CC}}\right)+0.3 \mathrm{~V}$ to $\left(-\mathrm{V}_{\mathrm{CC}}\right)-0.3 \mathrm{~V}$
Voltage at Input/Output Pin $\left(\mathrm{V}_{\mathrm{CC}}\right)+0.3 \mathrm{~V}$ to $\left(-\mathrm{V}_{\mathrm{CC}}\right)-0.3 \mathrm{~V}$
Supply Voltage ( $\mathrm{V}^{+}-\mathrm{V}^{-}$) 10 V
Current at Input Pin $\pm 5 \mathrm{~mA}$
Current at Output Pin (Note 3) $\pm 30 \mathrm{~mA}$
Current at Power Supply Pin 40 mA
Lead Temperature (soldering, 10 sec ) $260^{\circ} \mathrm{C}$

Storage Temperature Range
$-65^{\circ} \mathrm{C}$ to $+150^{\circ} \mathrm{C}$
Junction Temperature (Note 4) $150^{\circ} \mathrm{C}$

Operating Ratings (Note 1)

| Supply Voltage | $2 \mathrm{~V} \leq \mathrm{V}_{\mathrm{CC}} \leq 8 \mathrm{~V}$ |
| :--- | ---: |
| Junction Temperature Range |  |
| LMC7215IM, LMC7225IM | $-40^{\circ} \mathrm{C} \leq \mathrm{TJ} \leq+85^{\circ} \mathrm{C}$ |
| Thermal Resistance $\left(\theta_{\mathrm{JAA}}\right)$ |  |
| M Package, 8-Pin Surface Mount | $165^{\circ} \mathrm{C} / \mathrm{W}$ |
| SOT23-5 Package | $325^{\circ} \mathrm{C} / \mathrm{W}$ |

### 2.7V to 5V Electrical Characteristics

Unless otherwise specified, all limits guaranteed for $\mathrm{T}_{\mathrm{J}}=25^{\circ} \mathrm{C}, \mathrm{V}+=2.7 \mathrm{~V}$ to $5 \mathrm{~V}, \mathrm{~V}^{-}=0 \mathrm{~V}, \mathrm{~V}_{\mathrm{CM}}=\mathrm{V}_{\mathrm{O}}=\mathrm{V}+/ 2$. Boldface limits apply at the temperature extremes.

| Symbol | Parameter | Conditions | Typ <br> (Note 5) | $\begin{aligned} & \text { LMC7215 } \\ & \text { Limit } \\ & \text { (Note 6) } \end{aligned}$ | $\begin{aligned} & \text { LMC7225 } \\ & \text { Limit } \\ & \text { (Note 6) } \end{aligned}$ | Units |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| $\mathrm{V}_{\text {OS }}$ | Input Offset Voltage |  | 1 | $\begin{aligned} & 6 \\ & 8 \end{aligned}$ | $\begin{aligned} & 6 \\ & 8 \end{aligned}$ | $\begin{gathered} \mathrm{mV} \\ \max \end{gathered}$ |
| TCV ${ }_{\text {OS }}$ | Input Offset Voltage Average Drift |  | 2 |  |  | $\mu \mathrm{V} /{ }^{\circ} \mathrm{C}$ |
| $\mathrm{I}_{\mathrm{B}}$ | Input Current |  | 5 |  |  | fA |
| l OS | Input Offset Current |  | 1 |  |  | fA |
| CMRR | Common Mode Rejection Ratio | (Note 7) | 80 | 60 | 60 | $\begin{gathered} \mathrm{dB} \\ \mathrm{~min} \end{gathered}$ |
| PSRR | Power Supply <br> Rejection Ratio | $\mathrm{V}^{+}=2.2 \mathrm{~V}$ to 8 V | 90 | 60 | 60 | $\begin{gathered} \mathrm{dB} \\ \mathrm{~min} \end{gathered}$ |
| $A_{V}$ | Voltage Gain |  | 140 |  |  | dB |
| CMVR | Input Common-Mode Voltage Range | $\begin{aligned} & \mathrm{V}^{+}=2.7 \mathrm{~V} \\ & \mathrm{CMRR}>50 \mathrm{~dB} \end{aligned}$ | 3.0 | $\begin{aligned} & 2.9 \\ & 2.7 \end{aligned}$ | $\begin{aligned} & 2.9 \\ & 2.7 \end{aligned}$ | $\begin{gathered} \mathrm{V} \\ \mathrm{~min} \end{gathered}$ |
|  |  | $\begin{aligned} & \mathrm{V}^{+}=2.7 \mathrm{~V} \\ & \mathrm{CMRR}>50 \mathrm{~dB} \end{aligned}$ | -0.2 | $\begin{aligned} & 0.0 \\ & 0.2 \end{aligned}$ | $\begin{aligned} & 0.0 \\ & 0.2 \end{aligned}$ | $\begin{gathered} \text { V } \\ \max \end{gathered}$ |
|  |  | $\begin{aligned} & \mathrm{V}^{+}=5.0 \mathrm{~V} \\ & \mathrm{CMRR}>50 \mathrm{~dB} \end{aligned}$ | 5.3 | $\begin{aligned} & 5.2 \\ & 5.0 \end{aligned}$ | $\begin{aligned} & 5.2 \\ & 5.0 \end{aligned}$ | $\begin{gathered} \mathrm{V} \\ \mathrm{~min} \end{gathered}$ |
|  |  | $\begin{aligned} & \mathrm{V}^{+}=5.0 \mathrm{~V} \\ & \mathrm{CMRR}>50 \mathrm{~dB} \end{aligned}$ | -0.3 | $\begin{gathered} -0.2 \\ \mathbf{0 . 0} \\ \hline \end{gathered}$ | $\begin{gathered} -0.2 \\ \mathbf{0 . 0} \\ \hline \end{gathered}$ | $\begin{gathered} \text { V } \\ \max \end{gathered}$ |
| $\mathrm{V}_{\mathrm{OH}}$ | Output Voltage High | $\begin{aligned} & \mathrm{V}+=2.2 \mathrm{~V} \\ & \mathrm{l}_{\mathrm{OH}}=1.5 \mathrm{~mA} \end{aligned}$ | 2.05 | $\begin{aligned} & 1.8 \\ & \mathbf{1 . 7} \\ & \hline \end{aligned}$ | NA | $\begin{gathered} \mathrm{V} \\ \mathrm{~min} \end{gathered}$ |
|  |  | $\begin{aligned} & \mathrm{V}^{+}=2.7 \mathrm{~V} \\ & \mathrm{l}_{\mathrm{OH}}=2.0 \mathrm{~mA} \end{aligned}$ | 2.05 | $\begin{array}{r} 2.3 \\ \mathbf{2 . 2} \\ \hline \end{array}$ | NA | $\begin{gathered} \mathrm{V} \\ \mathrm{~min} \end{gathered}$ |
|  |  | $\begin{aligned} & \mathrm{V}^{+}=5.0 \mathrm{~V} \\ & \mathrm{l}_{\mathrm{OH}}=4.0 \mathrm{~mA} \end{aligned}$ | 4.8 | $\begin{array}{r} 4.6 \\ 4.5 \\ \hline \end{array}$ | NA | $\begin{gathered} \mathrm{V} \\ \mathrm{~min} \end{gathered}$ |


| 2.7V to 5V Electrical Characteristics (Continued) <br> Unless otherwise specified, all limits guaranteed for $\mathrm{T}_{\mathrm{J}}=25^{\circ} \mathrm{C}, \mathrm{V}^{+}=2.7 \mathrm{~V}$ to $5 \mathrm{~V}, \mathrm{~V}^{-}=0 \mathrm{~V}, \mathrm{~V}_{\mathrm{CM}}=\mathrm{V}_{\mathrm{O}}=\mathrm{V}+/ 2$. Boldface limits apply at the temperature extremes. (Continued) |  |  |  |  |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| Symbol | Parameter | Conditions | Typ <br> (Note 5) | $\begin{gathered} \text { LMC7215 } \\ \text { Limit } \\ \text { (Note 6) } \\ \hline \end{gathered}$ | $\begin{aligned} & \text { LMC7225 } \\ & \text { Limit } \\ & \text { (Note 6) } \\ & \hline \end{aligned}$ | Units |
| $\mathrm{V}_{\mathrm{OL}}$ | Output Voltage Low | $\begin{aligned} & \mathrm{V}^{+}=2.2 \mathrm{~V} \\ & \mathrm{I}_{\mathrm{OH}}=1.5 \mathrm{~mA} \end{aligned}$ | 0.17 | $\begin{aligned} & 0.4 \\ & 0.5 \end{aligned}$ | $\begin{aligned} & 0.4 \\ & 0.5 \end{aligned}$ | V <br> max |
|  |  | $\begin{aligned} & \mathrm{V}^{+}=2.7 \mathrm{~V} \\ & \mathrm{l}_{\mathrm{OH}}=2.0 \mathrm{~mA} \end{aligned}$ | 0.17 | $\begin{aligned} & 0.4 \\ & 0.5 \\ & \hline \end{aligned}$ | $\begin{aligned} & 0.4 \\ & 0.5 \end{aligned}$ | V max |
|  |  | $\begin{aligned} & \mathrm{V}^{+}=5.0 \mathrm{~V} \\ & \mathrm{l}_{\mathrm{OH}}=4.0 \mathrm{~mA} \end{aligned}$ | 0.2 | $\begin{aligned} & 0.4 \\ & \mathbf{0 . 5} \\ & \hline \end{aligned}$ | $\begin{aligned} & 0.4 \\ & \mathbf{0 . 5} \\ & \hline \end{aligned}$ | V <br> max |
| ISC+ | Output Short Circuit Current (Note 10) | $\mathrm{V}^{+}=2.7 \mathrm{~V}$, Sourcing | 15 |  | NA | mA |
|  |  | $\mathrm{V}^{+}=5.0 \mathrm{~V}$, Sourcing | 50 |  | NA | mA |
| Isc- | Output Short Circuit Current (Note 10) | $\mathrm{V}^{+}=2.7 \mathrm{~V}$, Sinking | 12 |  |  | mA |
|  |  | $\mathrm{V}^{+}=5.0 \mathrm{~V}$, Sinking | 30 |  |  | mA |
| LLeakage | Output Leakage Current | $\begin{aligned} & \mathrm{V}^{+}=2.2 \mathrm{~V} \\ & \mathrm{~V}_{\mathrm{IN}}^{+}=0.1 \mathrm{~V}, \mathrm{~V}_{\mathrm{IN}^{-}}=0 \mathrm{~V}, \\ & \mathrm{~V}_{\mathrm{OUT}}=15 \mathrm{~V} \\ & \hline \end{aligned}$ | 0.01 | NA | 500 | nA max |
| Is | Supply Current | $\begin{aligned} & \mathrm{V}^{+}=5.0 \mathrm{~V} \\ & \mathrm{~V}_{\mathrm{IN}}+=5 \mathrm{~V}, \mathrm{~V}_{\mathrm{IN}^{-}}=0 \mathrm{~V} \end{aligned}$ | 0.7 | $\begin{gathered} 1 \\ 1.2 \\ \hline \end{gathered}$ | $\begin{gathered} 1 \\ 1.2 \\ \hline \end{gathered}$ | $\begin{gathered} \mu \mathrm{A} \\ \max \end{gathered}$ |

## AC Electrical Characteristics

Unless otherwise specified, $\mathrm{T}_{\mathrm{J}}=25^{\circ} \mathrm{C}, \mathrm{V}^{+}=5 \mathrm{~V}, \mathrm{~V}^{-}=0 \mathrm{~V}, \mathrm{~V}_{\mathrm{CM}}=\mathrm{V}^{+} / 2$

| Symbol | Parameter | Conditions |  | $\begin{gathered} \text { LMC7215 } \\ \text { Typ } \\ \text { (Note 5) } \\ \hline \end{gathered}$ | LMC7225 Typ (Notes 5 and 8) | Units |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| $t_{\text {rise }}$ | Rise Time | Overdrive $=10 \mathrm{mV}$ (Note 8) |  | 1 | 12.2 | $\mu \mathrm{S}$ |
| $\mathrm{t}_{\text {fall }}$ | Fall Time | Overdrive $=10 \mathrm{mV}$ (Note 8) |  | 0.4 | 0.35 | $\mu \mathrm{s}$ |
| $t_{\text {PHL }}$ | Propagation Delay (High to Low) | (Note 9) | 10 mV | 24 | 24 | $\mu \mathrm{S}$ |
|  |  |  | 100 mV | 12 | 12 |  |
|  |  | $\mathrm{V}^{+}=2.7 \mathrm{~V}$ <br> (Note 9) | 10 mV | 17 | 17 | $\mu \mathrm{S}$ |
|  |  |  | 100 mV | 11 | 11 |  |
| $t_{\text {PLH }}$ | Propagation Delay (Low to High) | (Note 9) | 10 mV | 24 | 29 | $\mu \mathrm{S}$ |
|  |  |  | 100 mV | 12 | 17 |  |
|  |  | $\mathrm{V}^{+}=2.7 \mathrm{~V}$ <br> (Note 9) | 10 mV | 17 | 22 | $\mu \mathrm{S}$ |
|  |  |  | 100 mV | 11 | 16 |  |

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but specific performance is not guaranteed. For guaranteed specifications and the test conditions, see the Electrical Characteristics. Note 2: Human body model, $1.5 \mathrm{k} \Omega$ in series with 100 pF .
Note 3: Applies to both single-supply and split-supply operation. Continuous short circuit operation at elevated ambient temperature can result in exceeding the maximum allowed junction temperature of $150^{\circ} \mathrm{C}$.
Note 4: The maximum power dissipation is a function of $T_{J(\max )}, \theta_{J A}$, and $T_{A}$. The maximum allowable power dissipation at any ambient temperature is $P_{D}=\left(T_{J(\max )}-T_{A}\right) / \theta_{J A}$. All numbers apply for packages soldered directly into a PC board.
Note 5: Typical values represent the most likely parametric norm.
Note 6: All limits are guaranteed by testing or statistical analysis.
Note 7: CMRR measured at $\mathrm{V}_{\mathrm{CM}}=2.5 \mathrm{~V}$ and 2.5 V to 5 V when $\mathrm{V}_{\mathrm{S}}=5 \mathrm{~V}, \mathrm{~V}_{\mathrm{CM}}=0.2 \mathrm{~V}$ to 1.35 V and 1.35 V to 2.7 V when $\mathrm{V}_{\mathrm{S}}=2.7 \mathrm{~V}$. This eliminates units that have large $\mathrm{V}_{\mathrm{OS}}$ at the $\mathrm{V}_{\mathrm{CM}}$ extremes and low or opposite $\mathrm{V}_{\mathrm{OS}}$ at $\mathrm{V}_{\mathrm{CM}}=\mathrm{V}_{\mathrm{S}} / 2$.
Note 8: All measurements made at 10 kHz . A $100 \mathrm{k} \Omega$ pull-up resistor was used when measuring the LMC7225. $\mathrm{C}_{\mathrm{LOAD}}=50 \mathrm{pF}$ including the test jig and scope probe. The rise times of the LMC7225 are a function of the R-C time constant.
Note 9: Input step voltage for the propagation measurements is 100 mV .
Note 10: Do not short the output of the LMC7225 to voltages greater than 10 V or damage may occur.

Typical Performance Characteristics $\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$ unless otherwise specified



TL/H/12853-14

## Output Voltage vs

 Output Current LMC7215


TL/H/12853-12

## Output Voltage vs Output Current LMC7215



TL/H/12853-15

## Output Voltage vs

Output Current


Output Leakage Current vs Output Voltage LMC7225

TL/H/12853-20

## Application Information

## RESPONSE TIME

Depending upon the amount of overdrive, the delay will typically be between $10 \mu \mathrm{~s}$ to $200 \mu \mathrm{~s}$. The curve showing delay vs overdrive in the "Typical Characteristics" section shows the delay time when the input is preset with 100 mV across the inputs and then is driven the other way by 1 mV to 500 mV .
The transition from high to low or low to high is fast. Typically $1 \mu \mathrm{~s}$ rise and 400 ns fall.
With a small signal input, the comparators will provide a square wave output from sine wave inputs at frequencies as high as 25 kHz . Figure 1 shows a worst case example where a $\pm 5 \mathrm{mV}$ sine wave is applied to the input. Note that the output is delayed by almost $180^{\circ}$.


TL/H/12853-4
FIGURE 1

## NOISE

Most comparators have rather low gain. This allows the output to spend time between high and low when the input signal changes slowly. The result is the output may oscillate between high and low when the differential input is near zero.
The exceptionally high gain of these comparators, $10,000 \mathrm{~V} / \mathrm{mV}$, eliminates this problem. Less then $1 \mu \mathrm{~V}$ of change on the input will drive the output from one rail to the other rail.
If the input signal is noisy, the output cannot ignore the noise unless some hysteresis is provided by positive feedback.


FIGURE 2

## INPUT VOLTAGE RANGE

The LMC7215/25 have input voltage ranges that are larger than the supply voltage guarantees that signals from other parts of the system cannot overdrive the inputs. This allows sensing supply current by connecting one input directly to the $\mathrm{V}+$ line and the other to the other side of a current sense resistor. The same is true if the sense resistor is in the ground return line.
Sensing supply voltage is also easy by connecting one input directly to the supply.
The inputs of these comparators are protected by diodes to both supplies. This protects the inputs from both ESD as well as signals that greatly exceed the supply voltages. As a result, current will flow through these forward biased diodes whenever the input voltage is more than a few hundred millivolts larger than the supplies. Until this occurs, there is essentially no input current. As a result, placing a large resistor in series with any input that may be exposed to large voltages, will limit the input current but have no other noticeable effect.
If the input current is limited to less than 5 mA by a series resistor, (see Figure 2), a threshold or zero crossing detector, that works with inputs from as low as a few millivolts to as high as $5,000 \mathrm{~V}$, is made with only one resistor and the comparator.

## INPUTS

As mentioned above, these comparators have near zero input current. This allows very high resistance circuits to be used without any concern for matching input resistances. This also allows the use of very small capacitors in R-C type timing circuits. This reduces the cost of the capacitors and amount of board space used.

## CAPACITIVE LOADS

The high output current drive allows large capacitive loads with little effect. Capacitive loads as large as 10,000 pF have no effect upon delay and only slow the transition by about $3 \mu \mathrm{~s}$.

## OUTPUT CURRENT

Even though these comparators use less than $1 \mu \mathrm{~A}$ supply current, the outputs are able to drive very large currents.
The LMC7215 can source up to 50 mA when operated on a 5 V supply. Both the LMC7215 and LMC7225 can sink over 20 mA . (See the graph of Max IO vs $\mathrm{V}_{\text {Supply }}$ in the "Typical Characteristics" section.)
This large current handling ability allows driving heavy loads directly. LEDs, beepers and other loads can be driven easily.
The push-pull output stage of the LMC7215 is a very important feature. This keeps the total system power consumption to the absolute minimum. The only current consumed is the less than $1 \mu \mathrm{~A}$ supply current and the current going directly into the load. No power is wasted in a pull-up resistor when the output is low. The LMC7225 is only recommended where a level shifting function from one logic level to another is desired, where the LMC7225 is being used as a drop-in lower power replacement for an older comparator or in circuits where more than one output will be paralleled.

## Application Information (Continued)

## POWER DISSIPATION

The large output current ability makes it possible to exceed the maximum operating junction temperature of $85^{\circ} \mathrm{C}$ and possibly even the absolute maximum junction temperature of $150^{\circ} \mathrm{C}$.
The thermal resistance of the 8-pin surface mount package is $165^{\circ} \mathrm{C} / \mathrm{W}$. Shorting the output to ground with a 2.7 V supply will only result in about $5^{\circ} \mathrm{C}$ rise above ambient.
The thermal resistance of the much smaller SOT23-5 package is $325^{\circ} \mathrm{C} / \mathrm{W}$. With a 2.7 V supply, the raise is only $10.5^{\circ} \mathrm{C}$ but if the supply is 5 V and the short circuit current is 50 mA , this will cause a raise of $41^{\circ} \mathrm{C}$ in the $\mathrm{SO}-8$ and $81^{\circ} \mathrm{C}$ in the SOT23-5. This should be kept in mind if driving very low resistance loads.

## SHOOT-THROUGH

Shoot-through is a common occurrence on digital circuits and comparators where there is a push-pull output stage. This occurs when a signal is applied at the same time to both the N-channel and P-channel output transistors to turn one off and turn the other on. (See Figure 3.) If one of the output devices responds slightly faster than the other, the fast one can be turned on before the other has turned off. For a very short time, this allows supply current to flow directly through both output transistors. The result is a short spike of current drawn from the supply.


FIGURE 3


FIGURE 4. $\mathbf{R}_{\mathbf{S}}=100 \Omega$

The LMC7215 produces a small current spike of $300 \mu \mathrm{~A}$ peak for about 400 ns with 2.7 V supply and 1.8 mA peak for 400 ns with a 5 V supply. This spike only occurs when the output is going from high to low. It does not occur when going from low to high. Figures 4 and 5 show what this current pulse looks like on 2.7 V and 5 V supplies. The upper trace is the output voltage and the lower trace is the supply current as measured with the circuit in Figure 6.
If the power supply has a very high impedance, a bypass capacitor of $0.01 \mu \mathrm{~F}$ should be more than enough to minimize the effects of this small current pulse.


TL/H/12853-8
FIGURE 5. $\mathbf{R}_{\mathbf{S}}=10 \Omega$


TL/H/12853-9

## FIGURE 6

## LATCH-UP

In the past, most CMOS IC's were susceptible to a damaging phenomena known as latch-up. This occurred when an ESD current spike or other large signal was applied to any of the pins of an IC. The LMC7215 and LMC7225 both are designed to make them highly resistant to this type of damage. They have passed qualification tests with input currents on any lead up to 300 mA at temperatures up to $125^{\circ} \mathrm{C}$.

## SPICE MODELS

For a SPICE model of the LMC7215, LMC7225 and many other op-amps and comparators, contact the NSC Customer Response Center at 800-272-9959 or on the World Wide Web at http://www.national.com/models/index.html.

## SOT-23-5 Tape and Reel Specification

 REEL DIMENSIONS

| $\mathbf{8 m m}$ | $\mathbf{7 . 0 0}$ | $\mathbf{0 . 0 5 9}$ | $\mathbf{0 . 5 1 2}$ | $\mathbf{0 . 7 9 5}$ | $\mathbf{2 . 1 6 5}$ | $\mathbf{0 . 3 3 1 + 0 . 0 5 9 / - 0 . 0 0 0}$ | $\mathbf{0 . 5 6 7}$ | $\mathrm{W} 1+\mathbf{0 . 0 7 8 / - 0 . 0 3 9}$ |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  | 330.00 | $\mathbf{1 . 5 0}$ | $\mathbf{1 3 . 0 0}$ | $\mathbf{2 0 . 2 0}$ | $\mathbf{5 5 . 0 0}$ | $\mathbf{8 . 4 0 + 1 . 5 0 / - \mathbf { 0 . 0 0 }}$ | $\mathbf{1 4 . 4 0}$ | $\mathrm{~W} 1+\mathbf{2 . 0 0 / - 1 . 0 0}$ |
| Tape Size | A | B | C | D | N | W 1 | W 2 | W 3 |

## SOT-23-5 Tape and Reel Specification (Continued)

 tape format| Tape Section | \# Cavities | Cavity Status | Cover Tape Status |
| :---: | :---: | :---: | :---: |
| Leader (Start End) | 0 (min) | Empty | Sealed |
|  | 75 (min) | Empty | Sealed |
| Carrier | 3000 | Filled | Sealed |
|  | 250 | Filled | Sealed |
| Trailer (Hub End) | 125 (min) | Empty | Sealed |
|  | 0 (min) | Empty | Sealed |

TAPE DIMENSIONS


Physical Dimensions inches (millimeters) unless otherwise noted

*Suffix indicates number of units. See Ordering Information on first page.
5-Pin SOT Package
Order Number LMC7215IM5X, LMC7225IM5X, LMC7215IM5 or LMC7225IM5
NS Package Number MA05A
LMC7215/LMC7225 Micro-Power, Rail-to-Rail CMOS Comparators
${ }_{8}^{0}$

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)
Lit. \# 108496-001


8-Pin Small Outline Package
Order Number LMC7215IM, LMC7225IM, LMC7215IMX or LMC7225IMX
NS Package Number M08A

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# High Speed Amplifiers 

- CLC451 Single Supply, Low Power, High Output Programmable Buffer
- CLC452 Single Supply, LP, High Output CFB Amp
- CLC453 Programmable Gain Buffer of CLC452
- CLC5523 Low Power, Variable Gain Amplifier
- CLC5602 Dual CLC450
- CLC5612 Dual CLC451
- CLC5622 Dual CLC452
- CLC5623 Triple CLC452
- CLC5632 CLC5622 with internal Rf and Rg
- CLC5633 Triple CLC453


## Comlinear CLC451 <br> Single Supply, Low-Power, High Output, Programmable Buffer

## General Description

The Comlinear CLC451 is a low cost, high speed ( 85 MHz ) buffer that features user-programmable gains of $+2,+1$, and $-1 \mathrm{~V} / \mathrm{V}$. It has a new output stage that delivers high output drive current ( 100 mA ), but consumes minimal quiescent supply current ( 1.5 mA ) from a single 5 V supply. Its current feedback architecture, fabricated in an advanced complementary bipolar process, maintains consistent performance over a programmable range of gains and wide signal levels, and has a linear-phase response up to one half of the -3dB frequency. The CLC451's internal feedback network provides an excellent gain accuracy of 0.3\%

The CLC451 offers superior dynamic performance with a 85 MHz small-signal bandwidth, $260 \mathrm{~V} / \mu \mathrm{s}$ slew rate and 6.5 ns rise/fall times $\left(2 \mathrm{~V}_{\text {step }}\right)$. The combination of the small SOT23-5 package, low quiescent power, high output current drive, and high-speed performance make the CLC451 well suited for many batterypowered personal communication/computing systems.

The ability to drive low-impedance, highly capacitive loads, makes the CLC451 ideal for single ended cable applications. It also drives low impedance loads with minimum distortion. The CLC451 will drive a $100 \Omega$ load with only $-78 /-65 \mathrm{dBc}$ second/third harmonic distortion ( $\mathrm{A}_{\mathrm{v}}=+2, \mathrm{~V}_{\text {out }}=2 \mathrm{~V}_{\mathrm{pp}}, \mathrm{f}=1 \mathrm{MHz}$ ). With a $25 \Omega$ load, and the same conditions, it produces only $-55 /-60 \mathrm{dBc}$ second/third harmonic distortion. It is also optimized for driving high currents into single-ended transformers and coils.

When driving the input of high-resolution $A / D$ converters, the CLC451 provides excellent -66/-75dBc second/third harmonic distortion ( $\mathrm{A}_{\mathrm{V}}=+2, \mathrm{~V}_{\mathrm{out}}=2 \mathrm{~V}_{\mathrm{pp}}, \mathrm{f}=1 \mathrm{MHz}, \mathrm{R}_{\mathrm{L}}=1 \mathrm{k} \Omega$ ) and fast settling time.

## Features

- 100 mA output current
- 1.5 mA supply current
- 85 MHz bandwidth $\left(\mathrm{A}_{\mathrm{v}}=+2\right)$
- $-66 /-75 \mathrm{dBc}$ HD2/HD3 (1MHz)
- 25 ns settling to $0.05 \%$
- $260 \mathrm{~V} / \mathrm{\mu s}$ slew rate
- Stable for capacitive loads up to 1000 pF
- Single 5 V to $\pm 5 \mathrm{~V}$ supplies
- Available in Tiny SOT23-5 package


## Applications

- Coaxial cable driver
- Twisted pair driver
- Transformer/Coil Driver
- High capacitive load driver
- Video line driver
- Portable/battery-powered applications
- A/D driver


+5 V Electrical Characteristics ( $\mathrm{A}_{\mathrm{v}}=+2, \mathrm{R}_{\mathrm{L}}=100 \Omega, \mathrm{~V}_{\mathrm{s}}=+5 \mathrm{~V}^{1}, \mathrm{~V}_{\mathrm{cm}}=\mathrm{V}_{\mathrm{EE}}+\left(\mathrm{V}_{\mathrm{s}} / 2\right), \mathrm{R}_{\mathrm{L}}$ tied to $\mathrm{V}_{\mathrm{cm}}$, unless specified)

| PARAMETERS | CONDITIONS | TYP | MIN/MAX RATINGS |  |  | UNITS | NOTES |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| Ambient Temperature | CLC451AJ | $+25^{\circ} \mathrm{C}$ | $+25^{\circ} \mathrm{C}$ | 0 to $70^{\circ} \mathrm{C}$ | -40 to $85^{\circ} \mathrm{C}$ |  |  |
| FREQUENCY DOMAIN RESPONSE |  |  |  |  |  |  |  |
| -3dB bandwidth | $\mathrm{V}_{\mathrm{o}}=0.5 \mathrm{~V}_{\mathrm{pp}}$ | 85 | 70 | 58 | 55 | MHz | B |
|  | $\mathrm{V}_{\mathrm{o}}=2.0 \mathrm{~V}_{\mathrm{pp}}$ | 70 | 55 | 50 | 45 | MHz |  |
| -0.1 dB bandwidth | $\mathrm{V}_{0}=0.5 \mathrm{~V}_{\mathrm{pp}}$ | 20 | 15 | 13 | 13 | MHz |  |
| gain peaking | $<200 \mathrm{MHz}, \mathrm{V}_{\mathrm{o}}=0.5 \mathrm{~V}_{\mathrm{pp}}$ | 0 | 0.5 | 0.9 | 1.0 | dB | B |
| gain rolloff | $<30 \mathrm{MHz}, \mathrm{V}_{\mathrm{o}}=0.5 \mathrm{~V}_{\mathrm{pp}}$ | 0.2 | 0.5 | 0.7 | 0.7 | dB | B |
| linear phase deviation | $<30 \mathrm{MHz}, \mathrm{V}_{\mathrm{o}}=0.5 \mathrm{~V}_{\mathrm{pp}}$ | 0.1 | 0.4 | 0.5 | 0.5 | deg |  |
| TIME DOMAIN RESPONSE |  |  |  |  |  |  |  |
| rise and fall time | 2 V step | 6.5 | 9.0 | 9.7 | 10.5 | ns |  |
| settling time to 0.05\% | 1V step | 25 | - |  |  | ns |  |
| overshoot | 2 V step | 13 | 15 | 18 | 18 | \% |  |
| slew rate | 2 V step | 260 | 180 | 165 | 150 | V/us |  |
| DISTORTION AND NOISE RESPONSE |  |  |  |  |  |  | B |
| $2^{\text {nd }}$ harmonic distortion$3^{\text {rd }}$ harmonic distortion | $2 \mathrm{~V}_{\mathrm{pp}}, 1 \mathrm{MHz}$ | -78 | -72 | -70 | -70 | dBc |  |
|  | $2 \mathrm{~V}_{\mathrm{pp}}, 1 \mathrm{MHz} ; \mathrm{R}_{\mathrm{L}}=1 \mathrm{k} \Omega$ | -66 | -60 | -58 | -58 | dBc |  |
|  | $2 \mathrm{~V}_{\mathrm{pp}}, 5 \mathrm{MHz}$ | -60 | -54 | -52 | -52 | dBc |  |
|  | $2 \mathrm{~V}_{\mathrm{pp}}, 1 \mathrm{MHz}$ | -65 | -61 | -59 | -59 | dBc |  |
| $3^{\text {rd }}$ harmonic distortion | $2 \mathrm{~V}_{\mathrm{pp}}, 1 \mathrm{MHz} ; \mathrm{R}_{\mathrm{L}}=1 \mathrm{k} \Omega$ | -75 | -69 | -67 | -67 | dBc |  |
|  | $2 \mathrm{~V}_{\mathrm{pp}}, 5 \mathrm{MHz}$ | -52 | -48 | -46 | -46 | dBc | B |
| equivalent input noise |  | 3.0 | 3.7 | 4 | 4 | $\mathrm{nV} / \sqrt{ } \mathrm{Hz}$ |  |
| non-inverting current ( $\mathrm{i}_{\mathrm{bn}}$ ) | $>1 \mathrm{MHz}$ | 6.9 | 9 | 10 | 10 | $\mathrm{pA} / \sqrt{ } \mathrm{Hz}$ |  |
| inverting current ( $\mathrm{i}_{\mathrm{bi}}$ ) | $>1 \mathrm{MHz}$ | 8.5 | 11 | 12 | 12 | $\mathrm{pA} / \sqrt{ } \mathrm{Hz}$ |  |
| STATIC DC PERFORMANCE |  |  |  |  |  |  |  |
| input offset voltage |  | 8 | 30 | 35 | 35 | mV | A |
| average drift |  | 80 | - | - | - | $\mu \mathrm{V} /{ }^{\circ} \mathrm{C}$ |  |
| input bias current (non-inverting) |  | 3 | 14 | 17 | 18 | $\mu \mathrm{A}$ | A |
| average drift |  | 25 | - | - | - | $n A /{ }^{\circ} \mathrm{C}$ |  |
| gain accuracy |  | $\pm 0.3$ | $\pm 1.5$ | $\pm 2.0$ | $\pm 2.0$ | \% | A |
| internal resistors ( $\mathrm{R}_{\mathrm{f}}, \mathrm{R}_{\mathrm{g}}$ ) |  | 1000 | $\pm 20 \%$ | $\pm 26 \%$ | $\pm 30 \%$ | $\Omega$ |  |
| power supply rejection ratio | DC | 49 | 46 | 44 | 44 | dB | B |
| common-mode rejection ratio | DC | 51 | 48 | 46 | 46 | dB |  |
| supply current | $\mathrm{R}_{\mathrm{L}}=\infty$ | 1.5 | 1.7 | 1.8 | 1.8 | mA | A |
| MISCELLANEOUS PERFORMANCE |  |  |  |  |  |  |  |
| input resistance (non-inverting) |  | 0.5 | 0.37 | 0.33 | 0.33 | $\mathrm{M} \Omega$ |  |
| input capacitance (non-inverting) |  | 1.5 | 2.3 | 2.3 | 2.3 | pF |  |
| input voltage range, High |  | 4.2 | 4.1 | 4.0 | 4.0 | V |  |
| input voltage range, Low |  | 0.8 | 0.9 | 1.0 | 1.0 | V |  |
| output voltage range, High | $\mathrm{R}_{\mathrm{L}}=100 \Omega$ | 4.0 | 3.9 | 3.8 | 3.8 | V |  |
| output voltage range, Low | $R_{L}=100 \Omega$ | 1.0 | 1.1 | 1.2 | 1.2 | V |  |
| output voltage range, High | $\mathrm{R}_{\mathrm{L}}=\infty$ | 4.1 | 4.0 | 4.0 | 3.9 | V |  |
| output voltage range, Low | $\mathrm{R}_{\mathrm{L}}=\infty$ | 0.9 | 1.0 | 1.0 | 1.1 | V |  |
| output current |  | 100 | 80 | 65 | 40 | mA | C |
| output resistance, closed loop | DC | 400 | 600 | 600 | 600 | $\mathrm{m} \Omega$ |  |

$\mathrm{Min} / \mathrm{max}$ ratings are based on product characterization and simulation. Individual parameters are tested as noted. Outgoing quality levels are determined from tested parameters.

## Notes

A) J-level: spec is $100 \%$ tested at $+25^{\circ} \mathrm{C}$, sample tested at $+85^{\circ} \mathrm{C}$.
B) J-level: spec is sample tested at $+25^{\circ} \mathrm{C}$.
C) The short circuit current can exceed the maximum safe output current.

1) $V_{S}=V_{C C}-V_{E E}$

## Reliability Information

## Transistor Count

MTBF (based on limited test data)

Absolute Maximum Ratings
supply voltage ( $\left.\mathrm{V}_{\mathrm{CC}}-\mathrm{V}_{\mathrm{EE}}\right)$ output current (see note C) common-mode input voltage maximum junction temperature storage temperature range lead temperature (soldering 10 sec ) ESD rating (human body model)
$\pm 5 \mathrm{~V}$ Electrical Characteristics ( $\mathrm{A}_{\mathrm{V}}=+2, \mathrm{R}_{\mathrm{L}}=100 \Omega, \mathrm{~V}_{\mathrm{cc}}= \pm 5 \mathrm{~V}$, unless specified)

| PARAMETERS | CONDITIONS | TYP | GUARANTEED MIN/MAX |  |  | UNITS | NOTES |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| Ambient Temperature | CLC451AJ | $+25^{\circ} \mathrm{C}$ | $+25^{\circ} \mathrm{C}$ | 0 to $70^{\circ} \mathrm{C}$ | -40 to $85^{\circ} \mathrm{C}$ |  |  |
| FREQUENCY DOMAIN RESPONSE |  |  |  |  |  |  |  |
| -3dB bandwidth | $\mathrm{V}_{\mathrm{o}}=1.0 \mathrm{~V}_{\mathrm{pp}}$ | 100 | 80 | 68 | 65 | MHz |  |
|  | $\mathrm{V}_{\mathrm{o}}=4.0 \mathrm{~V}_{\mathrm{pp}}$ | 55 | 45 | 42 | 40 | MHz |  |
| -0.1 dB bandwidth | $\mathrm{V}_{0}=1.0 \mathrm{~V}_{\mathrm{pp}}$ | 20 | 15 | 13 | 13 | MHz |  |
| gain peaking | $<200 \mathrm{MHz}, \mathrm{V}_{0}=1.0 \mathrm{~V}_{\mathrm{pp}}$ | 0 | 0.5 | 0.9 | 1.0 | dB |  |
| gain rolloff | $<30 \mathrm{MHz}, \mathrm{V}_{\mathrm{o}}=1.0 \mathrm{~V}_{\mathrm{pp}}$ | 0.2 | 0.7 | 0.8 | 0.8 | dB |  |
| linear phase deviation | $<30 \mathrm{MHz}, \mathrm{V}_{0}=1.0 \mathrm{~V}_{\mathrm{pp}}$ | 0.1 | 0.3 | 0.4 | 0.4 | deg |  |
| differential gain | NTSC, $\mathrm{R}_{\mathrm{L}}=150 \Omega$ | 0.3 | - | - | - | \% |  |
| differential phase | NTSC, $\mathrm{R}_{\mathrm{L}}=150 \Omega$ | 0.3 | - | - | - | deg |  |
| TIME DOMAIN RESPONSE |  |  |  |  |  |  |  |
| rise and fall time | 2 V step | 5.0 | 6.5 | 7.0 | 7.7 | ns |  |
| settling time to $0.05 \%$ | 2 V step | 20 | - | - | - | ns |  |
| overshoot | 2 V step | 10 | 13 | 15 | 15 | \% |  |
| slew rate | 2 V step | 350 | 260 | 240 | 220 | V/ $\mu \mathrm{s}$ |  |
| DISTORTION AND NOISE RESPONSE |  |  |  |  |  |  |  |
| $2^{\text {nd }}$ harmonic distortion | $2 \mathrm{~V}_{\mathrm{pp}}, 1 \mathrm{MHz}$ | -72 | -66 | -64 | -64 | dBc |  |
|  | $2 \mathrm{~V}_{\mathrm{pp}}, 1 \mathrm{MHz} ; \mathrm{R}_{\mathrm{L}}=1 \mathrm{k} \Omega$ | -69 | -63 | -61 | -61 | dBc |  |
|  | $2 V_{p p}^{p p}, 5 \mathrm{MHz}$ | -66 | -60 | -58 | -58 | dBc |  |
| $3{ }^{\text {rd }}$ harmonic distortion | $2 \mathrm{~V}_{\mathrm{pp}}, 1 \mathrm{MHz}$ | -65 | -61 | -59 | -59 | dBc |  |
|  | $2 \mathrm{~V}_{\mathrm{pp}}, 1 \mathrm{MHz} ; \mathrm{R}_{\mathrm{L}}=1 \mathrm{k} \Omega$ | -73 | -67 | -65 | -65 | dBc |  |
| equivalent input noise | $2 \mathrm{~V}_{\mathrm{pp}}, 5 \mathrm{MHz}$ | -52 | -48 | -46 | -46 | dBc |  |
|  | $>1 \mathrm{MHz}$ | 3.0 | 3.7 | 4 | 4 | $\mathrm{nV} / \mathrm{VHz}$ |  |
| non-inverting current ( $\mathrm{i}_{\mathrm{bn}}$ ) | $>1 \mathrm{MHz}$ | 6.9 | 9 | 10 | 10 | $\mathrm{pA} / \sqrt{\mathrm{Hz}}$ |  |
| inverting current ( $\mathrm{ib}_{\mathrm{b}}$ ) | $>1 \mathrm{MHz}$ | 8.5 | 11 | 12 | 12 | $\mathrm{pA} / \mathrm{NHz}$ |  |
| STATIC DC PERFORMANCE |  |  |  |  |  |  |  |
| output offset voltage average drift |  | 3 80 | 30 | 35 - | 35 - | $\underset{\mu \mathrm{V} /{ }^{\circ} \mathrm{C}}{\mathrm{mV}}$ | B |
| input bias current (non-inverting) |  | 1 | 12 | 16 | 17 | $\mu \mathrm{A}$ | B |
| average drift |  | 40 | - | - | - | $n A /{ }^{\circ} \mathrm{C}$ |  |
| gain accuracy |  | $\pm 0.3$ | $\pm 1.5$ | $\pm 2.0$ | $\pm 2.0$ | \% |  |
| internal resistors ( $\mathrm{R}_{\mathrm{f}}, \mathrm{R}_{\mathrm{g}}$ ) |  | 1000 | $\pm 20 \%$ | $\pm 26 \%$ | $\pm 30 \%$ | $\Omega$ |  |
| power supply rejection ratio | DC | 51 | 48 | 46 | 46 | dB |  |
| common-mode rejection ratio | DC | 53 | 50 | 48 | 48 | dB |  |
| supply current | $\mathrm{R}_{\mathrm{L}}=\infty$ | 1.6 | 1.9 | 2.0 | 2.0 | mA | B |
| MISCELLANEOUS PERFORMAN |  |  |  |  |  |  |  |
| input resistance (non-inverting) |  | 0.7 | 0.50 | 0.45 | 0.45 | $\mathrm{M} \Omega$ |  |
| input capacitance (non-inverting) |  | 1.2 | 1.8 | 1.8 | 1.8 | pF |  |
| common-mode input range |  | $\pm 4.2$ | $\pm 4.1$ | $\pm 4.1$ | $\pm 4.0$ | V |  |
| output voltage range | $R_{L}=100 \Omega$ | $\pm 3.8$ | $\pm 3.6$ | $\pm 3.6$ | $\pm 3.5$ | V |  |
| output voltage range | $\mathrm{R}_{\mathrm{L}}=\infty$ | $\pm 4.0$ | $\pm 3.8$ | $\pm 3.8$ | $\pm 3.7$ | V |  |
| output current |  | 130 | 100 | 80 | 50 | mA | C |
| output resistance, closed loop | DC | 400 | 600 | 600 | 600 | $\mathrm{m} \Omega$ |  |

## Notes

B) J-level: spec is sample tested at $+25^{\circ} \mathrm{C}$.
C) The short circuit current can exceed the maximum safe output current.

## Package Thermal Resistance

| Package | $\boldsymbol{\theta}_{\text {JC }}$ | $\boldsymbol{\theta}_{\text {JA }}$ |
| :--- | :---: | :---: |
| Plastic (AJP) | $115^{\circ} \mathrm{C} / \mathrm{W}$ | $125^{\circ} \mathrm{C} / \mathrm{W}$ |
| Surface Mount (AJE) | $130^{\circ} \mathrm{C} / \mathrm{W}$ | $150^{\circ} \mathrm{C} / \mathrm{W}$ |
| Surface Mount (AJM5) | $140^{\circ} \mathrm{C} / \mathrm{W}$ | $210^{\circ} \mathrm{C} / \mathrm{W}$ |
| Dice (ALC) | $25^{\circ} \mathrm{C} / \mathrm{W}$ | - |

## Ordering Information

| Model | Temperature Range | Description |
| :--- | :---: | :--- |
| CLC451AJP | $-40^{\circ} \mathrm{C}$ to $+85^{\circ} \mathrm{C}$ | 8-pin PDIP |
| CLC451AJE | $-40^{\circ} \mathrm{C}$ to $+85^{\circ} \mathrm{C}$ | 8-pin SOIC |
| CLC451AJM5 | $-40^{\circ} \mathrm{C}$ to $+85^{\circ} \mathrm{C}$ | 5 -pin SOT |
| CLC451ALC | $-40^{\circ} \mathrm{C}$ to $+85^{\circ} \mathrm{C}$ | dice |

+5 V Typical Performance $\left(\mathrm{A}_{\mathrm{v}}=+2, \mathrm{R}_{\mathrm{L}}=100 \Omega, \mathrm{~V}_{\mathrm{s}}=+5 \mathrm{~V}^{1}, \mathrm{~V}_{\mathrm{cm}}=\mathrm{V}_{\mathrm{EE}}+\left(\mathrm{V}_{\mathrm{S}} / 2\right), \mathrm{R}_{\mathrm{L}}\right.$ tied to $\mathrm{V}_{\mathrm{cm}}$, unless specified)

+5 V Typical Performance $\left(\mathrm{A}_{\mathrm{v}}=+2, \mathrm{R}_{\mathrm{L}}=100 \Omega, \mathrm{v}_{\mathrm{s}}=+5 \mathrm{~V}^{1}, \mathrm{~V}_{\mathrm{cm}}=\mathrm{V}_{\mathrm{EE}}+\left(\mathrm{V}_{\mathrm{S}} / 2\right)\right.$, $\mathrm{R}_{\mathrm{L}}$ tied to $\mathrm{V}_{\mathrm{cm}}$, unless specified)




Time (10ns/div)



## $\pm 5 \mathrm{~V}$ Typical Performance ( $\mathrm{A}_{\mathrm{v}}=+2, \mathrm{R}_{\mathrm{L}}=100 \Omega, \mathrm{v}_{\mathrm{cc}}= \pm 5 \mathrm{~V}$, unless specified)






Frequency Response vs. $\mathrm{V}_{\mathrm{o}}\left(\mathrm{A}_{\mathrm{v}}=2\right)$


$\pm 5 \mathrm{~V}$ Typical Performance ( $\mathrm{A}_{\mathrm{v}}=+2, \mathrm{R}_{\mathrm{L}}=100 \Omega, \mathrm{~V}_{\mathrm{cc}}= \pm 5 \mathrm{~V}$, unless specified)


The CLC451 is a current feedback buffer built in an advanced complementary bipolar process. The CLC451 operates from a single 5 V supply or dual $\pm 5 \mathrm{~V}$ supplies. Operating from a single 5V supply, the CLC451 has the following features:

- Gains of $+1,-1$, and $2 \mathrm{~V} / \mathrm{V}$ are achievable without external resistors
- Provides 100 mA of output current while consuming only 7.5 mW of power
- Offers low $-66 /-75 \mathrm{dBc} 2 n \mathrm{~d}$ and 3rd harmonic distortion
- Provides $\mathrm{BW}>60 \mathrm{MHz}$ and 1 MHz distortion $<-55 \mathrm{dBc}$ at $\mathrm{V}_{\mathrm{o}}=2 \mathrm{~V}_{\mathrm{pp}}$
The CLC451 performance is further enhanced in $\pm 5 \mathrm{~V}$ supply applications as indicated in the $\pm 5 \mathrm{~V}$ Electrical Characteristics table and $\pm 5 \mathrm{~V}$ Typical Performance plots.

If gains other than $+1,-1$, or $+2 \mathrm{~V} / \mathrm{V}$ are required, then the CLC450 can be used. The CLC450 is a current feedback amplifier with near identical performance and allows for external feedback and gain setting resistors.

## Current Feedback Amplifiers

Some of the key features of current feedback technology are:

- Independence of AC bandwidth and voltage gain
- Inherently stable at unity gain
- Adjustable frequency response with feedback resistor
- High slew rate
- Fast settling

Current feedback operation can be described using a simple equation. The voltage gain for a non-inverting or inverting current feedback amplifier is approximated by Equation 1.

$$
\frac{V_{0}}{V_{i n}}=\frac{A_{V}}{1+\frac{R_{f}}{Z(j \omega)}}
$$

Equation 1
where:

- $A_{v}$ is the closed loop DC voltage gain
- $R_{f}$ is the feedback resistor
- Z $(\mathrm{j} \omega)$ is the CLC451's open loop transimpedance gain
- $\frac{Z(\mathrm{j} \omega)}{\mathrm{R}_{\mathrm{f}}}$ is the loop gain

The denominator of Equation 1 is approximately equal to 1 at low frequencies. Near the -3dB corner frequency, the interaction between $R_{f}$ and $Z(j \omega)$ dominates the circuit performance. The value of the feedback resistor has a large affect on the circuits performance. Increasing $R_{f}$ has the following affects:

```
- Decreases loop gain
- Decreases bandwidth
- Reduces gain peaking
- Lowers pulse response overshoot
- Affects frequency response phase linearity
```


## CLC451 Design Information

## Closed Loop Gain Selection

The CLC451 is a current feedback op amp with $R_{f}=R_{g}=1 \mathrm{k} \Omega$ on chip (in the package). Select from three closed loop gains without using any external gain or feedback resistors. Implement gains of $+2,+1$, and $-1 \mathrm{~V} / \mathrm{V}$ by connecting pins 2 and 3 as described in the chart below.

| Gain <br> $A_{V}$ | Input Connections |  |
| :---: | :---: | :---: |
|  | Non-Inverting (pin3) | Inverting (pin2) |
| $-1 \mathrm{~V} / \mathrm{V}$ | ground | input signal |
| $+1 \mathrm{~V} / \mathrm{V}$ | input signal | NC (open) |
| $+2 \mathrm{~V} / \mathrm{V}$ | input signal | ground |

The gain accuracy of the CLC451 is excellent and stable over temperature change. The internal gain setting resistors, $R_{f}$ and $R_{g}$ are diffused silicon resistors with a process variation of $\pm 20 \%$ and a temperature coefficient of $\sim 2000 \mathrm{ppm} /{ }^{\circ} \mathrm{C}$. Although their absolute values change with processing and temperature, their ratio ( $R_{f} / R_{g}$ ) remains constant. If an external resistor is used in series with $\mathrm{R}_{\mathrm{g}}$, gain accuracy over temperature will suffer.

Single Supply Operation ( $\mathrm{V}_{\mathrm{CC}}=+5 \mathrm{~V}, \mathrm{~V}_{\mathrm{EE}}=\mathrm{GND}$ ) The specifications given in the $\mathbf{+ 5 V}$ Electrical Characteristics table for single supply operation are measured with a common mode voltage $\left(\mathrm{V}_{\mathrm{cm}}\right)$ of $2.5 \mathrm{~V} . \mathrm{V}_{\mathrm{cm}}$ is the voltage around which the inputs are applied and the output voltages are specified.

Operating from a single +5 V supply, the Common Mode Input Range (CMIR) of the CLC451 is typically +0.8 V to +4.2 V . The typical output range with $\mathrm{R}_{\mathrm{L}}=100 \Omega$ is +1.0 V to +4.0 V .

For single supply DC coupled operation, keep input signal levels above 0.8 V DC. For input signals that drop below 0.8 V DC, AC coupling and level shifting the signal are recommended. The non-inverting and inverting configurations for both input conditions are illustrated in the following 2 sections.

## DC Coupled Single Supply Operation

Figures 1, 2, and 3 on the following page, show the recommended configurations for input signals that remain above 0.8 V DC.


Figure 1: $D C$ Coupled, $A_{v}=-1 V / V$ Configuration


Figure 2: DC Coupled, $\mathrm{A}_{\mathrm{v}}=+\mathbf{1 V} / \mathrm{V}$ Configuration


Figure 3: DC Coupled, $A_{v}=+2 \mathrm{~V} / \mathrm{V}$ Configuration

## AC Coupled Single Supply Operation

Figures 4,5 , and 6 show possible non-inverting and inverting configurations for input signals that go below 0.8 V DC.


Figure 4: AC Coupled, $\mathrm{A}_{\mathrm{v}}=-1 \mathrm{~V} / \mathrm{V}$ Configuration

The input is AC coupled to prevent the need for level shifting the input signal at the source. The resistive voltage divider biases the non-inverting input to $\mathrm{V}_{\mathrm{CC}} \div 2$ $=2.5 \mathrm{~V}$ (For $\left.\mathrm{V}_{\mathrm{CC}}=+5 \mathrm{~V}\right)$.


Figure 5: AC Coupled, $\mathrm{A}_{\mathrm{v}}=+1 \mathrm{~V} / \mathrm{V}$ Configuration


Figure 6: AC Coupled, $\mathrm{A}_{\mathrm{v}}=\boldsymbol{+ 2 V} / \mathrm{V}$ Configuration

## Dual Supply Operation

The CLC451 operates on dual supplies as well as single supplies. The non-inverting and inverting configurations are shown in Figures 7, 8 and 9.


Figure 7: Dual Supply, $\mathrm{A}_{\mathrm{v}}=-1 \mathrm{~V} / \mathrm{V}$ Configuration


Figure 8: Dual Supply, $\mathrm{A}_{\mathrm{v}}=\boldsymbol{+ 1 V} / \mathrm{V}$ Configuration


Figure 9: Dual Supply, $A_{v}=+2 \mathrm{~V} / \mathrm{V}$ Configuration

## Bandwidth vs. Output Amplitude

The bandwidth of the CLC451 is at a maximum for output voltages near $1 \mathrm{~V}_{\mathrm{pp}}$. The bandwidth decreases for smaller and larger output amplitudes. Refer to the
Frequency Response vs. $V_{o}$ plots.

## Load Termination

The CLC451 can source and sink near equal amounts of current. For optimum performance, the load should be tied to $\mathrm{V}_{\mathrm{cm}}$.

## Driving Cables and Capacitive Loads

When driving cables, double termination is used to prevent reflections. For capacitive load applications, a small series resistor at the output of the CLC451 will improve stability and settling performance. The Frequency Response vs. $C_{L}$ and Recommended $R_{s}$ vs. $C_{L}$ plots, in the typical performance section, give the recommended series resistance value for optimum flatness at various capacitive loads.

## Transmission Line Matching

One method for matching the characteristic impedance $\left(Z_{0}\right)$ of a transmission line or cable is to place the appropriate resistor at the input or output of the amplifier.

Figure 10 shows typical inverting and non-inverting circuit configurations for matching transmission lines.
Non-inverting gain applications:

- Connect pin 2 as indicated in the table in the Closed Loop Gain Selection section.
- Make $R_{1}, R_{2}, R_{6}$, and $R_{7}$ equal to $Z_{0}$.
- Use $R_{3}$ to isolate the amplifier from reactive loading caused by the transmission line, or by parasitics.
Inverting gain applications:
- Connect $\mathrm{R}_{3}$ directly to ground.
- Make the resistors $R_{4}, R_{6}$, and $R_{7}$ equal to $Z_{0}$.
- Make $\mathrm{R}_{5}$ II $\mathrm{R}_{\mathrm{g}}=\mathrm{Z}_{\mathrm{o}}$.

The input and output matching resistors attenuate the signal by a factor of 2 , therefore additional gain is needed. Use $\mathrm{C}_{6}$ to match the output transmission line over a greater frequency range. $\mathrm{C}_{6}$ compensates for the increase of the amplifier's output impedance with frequency.


Figure 10: Transmission Line Matching

## Power Dissipation

Follow these steps to determine the power consumption of the CLC451:

1. Calculate the quiescent (no-load) power:

$$
P_{\mathrm{amp}}=I_{\mathrm{CC}}\left(\mathrm{~V}_{\mathrm{CC}}-\mathrm{V}_{\mathrm{EE}}\right)
$$

2. Calculate the RMS power at the output stage: $P_{0}=\left(V_{C C}-V_{\text {load }}\right)\left(I_{\text {load }}\right)$, where $V_{\text {load }}$ and $I_{\text {load }}$ are the RMS voltage and current across the external load.
3. Calculate the total RMS power:

$$
P_{t}=P_{a m p}+P_{o}
$$

The maximum power that the DIP, SOIC, and SOT packages can dissipate at a given temperature is illustrated in Figure 11. The power derating curve for any CLC451 package can be derived by utilizing the following equation:
where $\quad \frac{\left(175^{\circ}-\mathrm{T}_{\mathrm{amb}}\right)}{\theta_{\mathrm{JA}}}$
$\mathrm{T}_{\mathrm{amb}}=$ Ambient temperature $\left({ }^{\circ} \mathrm{C}\right)$
$\theta_{\mathrm{JA}}=$ Thermal resistance, from junction to ambient, for a given package ( ${ }^{\circ} \mathrm{C} / \mathrm{W}$ )


Figure 11: Power Derating Curve

## Layout Considerations

A proper printed circuit layout is essential for achieving high frequency performance. Comlinear provides evaluation boards for the CLC451 (CLC730013-DIP, CLC730027-SOIC, CLC730068-SOT) and suggests their use as a guide for high frequency layout and as an aid for device testing and characterization.

General layout and supply bypassing play major roles in high frequency performance. Follow the steps below as a basis for high frequency layout:

■ Include $6.8 \mu \mathrm{~F}$ tantalum and $0.1 \mu \mathrm{~F}$ ceramic capacitors on both supplies.
$■$ Place the $6.8 \mu \mathrm{~F}$ capacitors within 0.75 inches of the power pins.

- Place the $0.1 \mu \mathrm{~F}$ capacitors less than 0.1 inches from the power pins.
- Remove the ground plane under and around the part, especially near the input and output pins to reduce parasitic capacitance.
■ Minimize all trace lengths to reduce series inductances.
- Use flush-mount printed circuit board pins for prototyping, never use high profile DIP sockets.


## Evaluation Board Information

Data sheets are available for the CLC730013/ CLC730027 and CLC730068 evaluation boards. The evaluation board data sheets provide:

- Evaluation board schematics
- Evaluation board layouts
- General information about the boards

The CLC730013/CLC730027 data sheet also contains tables of recommended components to evaluate several of Comlinear's high speed amplifiers. This table for the CLC451 is illustrated below. Refer to the evaluation board data sheet for schematics and further information.

## Components Needed to Evaluate the CLC451 on the Evaluation Board:

- $\mathrm{R}_{\text {in }}, \mathrm{R}_{\text {out }}$ - Typically $50 \Omega$ (Refer to the Basic Operation section of the evaluation board data sheet for details)

■ $R_{t}$ - Optional resistor for inverting gain configurations (Select $R_{t}$ to yield desired input impedance $\left.=R_{g} \| R_{t}\right)$

- $\mathrm{C}_{1}, \mathrm{C}_{2}-0.1 \mu \mathrm{~F}$ ceramic capacitors

■ $\mathrm{C}_{3}, \mathrm{C}_{4}-6.8 \mu \mathrm{~F}$ tantalum capacitors
Components not used:

- $\mathrm{C}_{5}, \mathrm{C}_{6}, \mathrm{C}_{7}, \mathrm{C}_{8}$
- $R_{1}$ thru $R_{8}$

The evaluation boards are designed to accommodate dual supplies. The boards can be modified to provide single supply operation. For best performance; 1) do not connect the unused supply, 2) ground the unused supply pin.

## Special Evaluation Board Considerations for the CLC451

To optimize off-isolation of the CLC451, cut the $R_{f}$ trace on both the CLC730013 and the CLC730027 evaluation boards. This cut minimizes capacitive feedthrough between the input and the output. Figure 12 shows where to cut both evaluation boards for improved off-isolation.


Figure 12: Evaluation Board Changes

## SPICE Models

SPICE models provide a means to evaluate amplifier designs. Free SPICE models are available for Comlinear's monolithic amplifiers that:

■ Support Berkeley SPICE 2G and its many derivatives

- Reproduce typical DC, AC, Transient, and Noise performance
- Support room temperature simulations

The readme file that accompanies the diskette lists released models, and provides a list of modeled parameters. The application note OA-18, Simulation SPICE Models for Comlinear's Op Amps, contains schematics and a reproduction of the readme file.

## Application Circuits

## Single Supply Cable Driver

The typical application shown on the front page shows the CLC451 driving 10 m of $75 \Omega$ coaxial cable. The CLC451 is set for a gain of $+2 \mathrm{~V} / \mathrm{V}$ to compensate for the divide-by-two voltage drop at $\mathrm{V}_{0}$.

## Twisted Pair Driver

The high output current and low distortion, of the CLC451, make it well suited for driving transformers. Figure 13 illustrates a typical twisted pair driver utilizing the CLC451 and a transformer. The transformer provides the signal and its inversion for the twisted pair.


Figure 13: Twisted Pair Driver
To match the line's characteristic impedance $\left(Z_{0}\right)$ set:

$$
\begin{aligned}
& \square R_{L}=Z_{o} \\
& -R_{m}=R_{e q}
\end{aligned}
$$

Where $R_{\text {eq }}$ is the transformed value of the load impedance, $\left(R_{L}\right)$, and is approximated by:

$$
R_{e q}=\frac{R_{L}}{n^{2}}
$$

Select the transformer so that it loads the line with a value close to $Z_{0}$, over the desired frequency range. The output impedance, $R_{0}$, of the CLC451 varies with frequency and can also affect the return loss. The return loss, shown below, takes into account an ideal transformer and the value of $R_{0}$.
Return Loss $(\mathrm{dB}) \approx-20 \log _{10}\left|n^{2} \cdot \frac{R_{0}}{Z_{0}}\right|$
The load current $\left(I_{L}\right)$ and voltage $\left(\mathrm{V}_{0}\right)$ are related to the CLC451's maximum output voltage and current by:

$$
\begin{aligned}
& \left|V_{0}\right| \leq n \cdot V_{\max } \\
& \left|I_{L}\right| \leq \frac{I_{\max }}{n}
\end{aligned}
$$

From the above current relationship, it is obvious that an amplifier with high output drive capability is required.

## Customer Design Applications Support

National Semiconductor is committed to design excellence. For sales, literature and technical support, call the National Semiconductor Customer Response Group at 1-800-272-9959 or fax 1-800-737-7018.

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## Comlinear CLC452 <br> Single Supply, Low-Power, High Output, Current Feedback Amplifier

## General Description

The Comlinear CLC452 has a new output stage that delivers high output drive current ( 100 mA ), but consumes minimal quiescent supply current ( 3.0 mA ) from a single 5 V supply. Its current feedback architecture, fabricated in an advanced complementary bipolar process, maintains consistent performance over a wide range of gains and signal levels, and has a linear-phase response up to one half of the -3 dB frequency.

The CLC452 offers superior dynamic performance with a 130 MHz small-signal bandwidth, $400 \mathrm{~V} / \mu \mathrm{s}$ slew rate and 4.5 ns rise/fall times $\left(2 \mathrm{~V}_{\text {step }}\right)$. The combination of low quiescent power, high output current drive, and high-speed performance make the CLC452 well suited for many battery-powered personal communication/computing systems.

The ability to drive low-impedance, highly capacitive loads, makes the CLC452 ideal for single ended cable applications. It also drives low impedance loads with minimum distortion. The CLC452 will drive a $100 \Omega$ load with only $-75 /-74 \mathrm{dBc}$ second/third harmonic distortion ( $\mathrm{A}_{\mathrm{v}}=+2, \mathrm{~V}_{\text {out }}=2 \mathrm{~V}_{\mathrm{pp}}, \mathrm{f}=1 \mathrm{MHz}$ ). With a $25 \Omega$ load, and the same conditions, it produces only $-65 /-77 \mathrm{dBc}$ second/third harmonic distortion. It is also optimized for driving high currents into single-ended transformers and coils.

When driving the input of high-resolution $A / D$ converters, the CLC452 provides excellent -78/-85dBc second/third harmonic distortion ( $\mathrm{A}_{\mathrm{v}}=+2, \mathrm{~V}_{\text {out }}=2 \mathrm{~V}_{\mathrm{pp}}, \mathrm{f}=1 \mathrm{MHz}, \mathrm{R}_{\mathrm{L}}=1 \mathrm{k} \Omega$ ) and fast settling time.

Available in SOT23-5, the CLC452 is ideal for applications where space is critical.

Features

- 100 mA output current
- 3.0 mA supply current
- 130 MHz bandwidth $\left(\mathrm{A}_{\mathrm{v}}=+2\right)$
- $-78 /-85 \mathrm{dBc}$ HD2/HD3 (1MHz)
- 25 ns settling to $0.05 \%$
- $400 \mathrm{~V} / \mathrm{\mu s}$ slew rate
- Stable for capacitive loads up to 1000 pF
- Single 5 V to $\pm 5 \mathrm{~V}$ supplies
- Available in Tiny SOT23-5 package


## Applications

- Coaxial cable driver
- Twisted pair driver
- Transformer/Coil Driver
- High capacitive load driver
- Video line driver
- Portable/battery-powered applications
- A/D driver



+5 V Electrical Characteristics ( $\mathrm{A}_{v}=+2, \mathrm{R}_{\mathrm{t}}=1 \mathrm{~K} \Omega, \mathrm{R}_{\mathrm{L}}=100 \Omega, \mathrm{~V}_{\mathrm{s}}=+5 \mathrm{~V}, \mathrm{~V}_{\mathrm{em}}=\mathrm{V}_{\mathrm{EE}}+\left(\mathrm{V}_{\mathrm{s}} 2\right), \mathrm{R}_{\mathrm{L}}$ tied to $\mathrm{V}_{\text {em }}$ unless specifiec $)$

$\mathrm{Min} / \mathrm{max}$ ratings are based on product characterization and simulation. Individual parameters are tested as noted. Outgoing quality levels are determined from tested parameters.


## Notes

A) J-level: spec is $100 \%$ tested at $+25^{\circ} \mathrm{C}$, sample tested at $+85^{\circ} \mathrm{C}$.
B) J-level: spec is sample tested at $+25^{\circ} \mathrm{C}$.
C) The short circuit current can exceed the maximum safe output current.

1) $V_{S}=V_{C C}-V_{E E}$

## Reliability Information

[^0]
## Absolute Maximum Ratings

supply voltage $\left(\mathrm{V}_{\mathrm{CC}}-\mathrm{V}_{\mathrm{EE}}\right)$ output current (see note C) common-mode input voltage maximum junction temperature storage temperature range lead temperature (soldering 10 sec ) ESD rating (human body model)

## 140 mA

$\mathrm{V}_{\mathrm{EE}}$ to $\mathrm{V}_{\mathrm{CC}}$
$+175^{\circ} \mathrm{C}$
$-65^{\circ} \mathrm{C}$ to $+150^{\circ} \mathrm{C}$
$+300^{\circ} \mathrm{C}$
$\pm 5 \mathrm{~V}$ Electrical Characteristics ( $\mathrm{A}_{\mathrm{v}}=+2, \mathrm{R}_{\mathrm{t}}=1 \mathrm{k} \Omega, \mathrm{R}_{\mathrm{L}}=100 \Omega, \mathrm{~V}_{\mathrm{cc}}= \pm 5 \mathrm{~V}$, unless speciifiec)

| PARAMETERS | CONDITIONS | TYP | GUARANTEED MIN/MAX |  |  | UNITS | NOTES |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| Ambient Temperature | CLC452AJ | $+25^{\circ} \mathrm{C}$ | $+25^{\circ} \mathrm{C}$ | 0 to $70^{\circ} \mathrm{C}$ | -40 to $85^{\circ} \mathrm{C}$ |  |  |
| FREQUENCY DOMAIN RESPONSE |  |  |  |  |  |  |  |
| -3dB bandwidth | $\mathrm{V}_{0}=1.0 \mathrm{~V}_{\mathrm{pp}}$ | 160 | 135 | 120 | 115 | MHz |  |
|  | $\mathrm{V}_{0}=4.0 \mathrm{~V}_{\mathrm{pp}}$ | 75 | 60 | 57 | 55 | MHz |  |
| -0.1 dB bandwidth | $\mathrm{V}_{0}=1.0 \mathrm{~V}_{\mathrm{pp}}$ | 30 | 25 | 25 | 20 | MHz |  |
| gain peaking | $<200 \mathrm{MHz}, \mathrm{V}_{\mathrm{o}}=1.0 \mathrm{~V}_{\mathrm{pp}}$ | 0 | 0.5 | 0.9 | 1.0 | dB |  |
| gain rolloff | $<30 \mathrm{MHz}, \mathrm{V}_{0}=1.0 \mathrm{~V}_{\mathrm{pp}}$ | 0.1 | 0.2 | 0.3 | 0.3 | dB |  |
| linear phase deviation | $<30 \mathrm{MHz}, \mathrm{V}_{0}=1.0 \mathrm{~V}_{\mathrm{pp}}$ | 0.1 | 0.2 | 0.3 | 0.3 | deg |  |
| differential gain | NTSC, $\mathrm{R}_{\mathrm{L}}=150 \Omega$ | 0.05 | - | - | - | \% |  |
| differential phase | NTSC, $\mathrm{R}_{\mathrm{L}}=150 \Omega$ | 0.08 | - | - | - | deg |  |
| TIME DOMAIN RESPONSE |  |  |  |  |  |  |  |
| rise and fall time | 2 V step | 3.2 | 4.2 | 4.5 | 5.0 | ns |  |
| settling time to $0.05 \%$ | 2 V step | 20 | - | - | - | ns |  |
| overshoot | 2 V step | 8 | 12 | 15 | 15 | \% |  |
| slew rate | 2 V step | 540 | 400 | 370 | 350 | V/ $\mu \mathrm{s}$ |  |
| DISTORTION AND NOISE RESPONSE |  |  |  |  |  |  |  |
| $2^{\text {nd }}$ harmonic distortion | $2 \mathrm{~V}_{\text {pp }}, 1 \mathrm{MHz}$ | -77 | -71 | -69 | -69 | dBc |  |
|  | $2 \mathrm{~V}_{\mathrm{pp}}, 1 \mathrm{MHz} ; \mathrm{R}_{\mathrm{L}}=1 \mathrm{k} \Omega$ | -78 | -72 | -70 | -70 | dBc |  |
|  | $2 \mathrm{~V}_{\mathrm{pp}}, 5 \mathrm{MHz}$ | -69 | -63 | -61 | -61 | dBc |  |
| $3{ }^{\text {rd }}$ harmonic distortion | $2 V_{\text {pp }}, 1 \mathrm{MHz}$ | -72 | -68 | -66 | -66 | dBc |  |
|  | $2 \mathrm{~V}_{\mathrm{pp}}, 1 \mathrm{MHz} ; \mathrm{R}_{\mathrm{L}}=1 \mathrm{k} \Omega$ | -90 | -80 | -78 | -78 | dBc |  |
| equivalent input noise | $2 \mathrm{~V}_{\mathrm{pp}}, 5 \mathrm{MHz}$ | -58 | -54 | -52 | -52 | dBc |  |
|  | $>1 \mathrm{MHz}$ | 2.8 | 3.8 | 3.8 | 3.8 | $\mathrm{nV} / \sqrt{ } \mathrm{Hz}$ |  |
| non-inverting current ( $\mathrm{i}_{\text {bn }}$ ) | $>1 \mathrm{MHz}$ | 7.5 | 10 | 11 | 11 | $\mathrm{pA} / \sqrt{ } \mathrm{Hz}$ |  |
| inverting current ( $\mathrm{i}_{\mathrm{bi}}$ ) | $>1 \mathrm{MHz}$ | 10.5 | 14 | 15 | 15 | $\mathrm{pA} / \mathrm{NHz}$ |  |
| STATIC DC PERFORMANCE |  |  |  |  |  |  |  |
| input offset voltage |  | 1 | 6 | 8 | 8 | mV | B |
| average drift |  | 10 | - | - | - | $\mu \mathrm{V} /{ }^{\circ} \mathrm{C}$ |  |
| input bias current (non-inverting) |  | 3 | 18 | 23 | 25 | $\mu \mathrm{A}$ | B |
| average drift |  | 40 | - | - | - | $n A /{ }^{\circ} \mathrm{C}$ |  |
| input bias current (inverting) |  | 9 | 19 | 21 | 22 | $\mu \mathrm{A}$ | B |
| average drift |  | 30 | - | - | - | $n A /{ }^{\circ} \mathrm{C}$ |  |
| power supply rejection ratio | DC | 54 | 51 | 49 | 49 | dB |  |
| common-mode rejection ratio | DC | 53 | 50 | 48 | 48 | dB |  |
| supply current | $\mathrm{R}_{\mathrm{L}}=\infty$ | 3.2 | 3.8 | 4.0 | 4.0 | mA | B |
| MISCELLANEOUS PERFORMAN |  |  |  |  |  |  |  |
| input resistance (non-inverting) |  | 0.52 | 0.35 | 0.30 | 0.30 | $\mathrm{M} \Omega$ |  |
| input capacitance (non-inverting) |  | 1.2 | 1.8 | 1.8 | 1.8 | pF |  |
| common-mode input range |  | $\pm 4.2$ | $\pm 4.1$ | $\pm 4.1$ | $\pm 4.0$ | V |  |
| output voltage range | $R_{L}=100 \Omega$ | $\pm 3.8$ | $\pm 3.6$ | $\pm 3.6$ | $\pm 3.5$ | V |  |
| output voltage range | $\mathrm{R}_{\mathrm{L}}=\infty$ | $\pm 4.0$ | $\pm 3.8$ | $\pm 3.8$ | $\pm 3.7$ | V |  |
| output current |  | 130 | 100 | 80 | 50 | mA | C |
| output resistance, closed loop | DC | 60 | 90 | 90 | 120 | $\mathrm{m} \Omega$ |  |

## Notes

B) J-level: spec is sample tested at $+25^{\circ} \mathrm{C}$.
C) The short circuit current can exceed the maximum safe output current.

## Package Thermal Resistance

| Package | $\boldsymbol{\theta}_{\text {JC }}$ | $\boldsymbol{\theta}_{\text {JA }}$ |
| :--- | :---: | :---: |
| Plastic (AJP) | $115^{\circ} \mathrm{C} / \mathrm{W}$ | $125^{\circ} \mathrm{C} / \mathrm{W}$ |
| Surface Mount (AJE) | $130^{\circ} \mathrm{C} / \mathrm{W}$ | $150^{\circ} \mathrm{C} / \mathrm{W}$ |
| Surface Mount (AJM5) | $140^{\circ} \mathrm{C} / \mathrm{W}$ | $210^{\circ} \mathrm{C} / \mathrm{W}$ |
| Dice (ALC) | $25^{\circ} \mathrm{C} / \mathrm{W}$ | - |

## Ordering Information

| Model | Temperature Range | Description |
| :--- | :---: | :--- |
| CLC452AJJ | $-40^{\circ} \mathrm{C}$ to $+85^{\circ} \mathrm{C}$ | 8-pin PDIP |
| CLC452AJE | $-40^{\circ} \mathrm{C}$ to $+85^{\circ} \mathrm{C}$ | 8-pin SOIC |
| CLC452AJM5 | $-40^{\circ} \mathrm{C}$ to $+85^{\circ} \mathrm{C}$ | 5 -pin SOT |
| CLC452ALC | $-40^{\circ} \mathrm{C}$ to $+85^{\circ} \mathrm{C}$ | dice |

+5 V Typical Performance $\left(\mathrm{A}_{\mathrm{v}}=+2, \mathrm{R}_{\mathrm{f}}=1 \mathrm{k} \Omega, \mathrm{R}_{\mathrm{L}}=100 \Omega, \mathrm{~V}_{\mathrm{s}}=+5 \mathrm{~V}^{1}, \mathrm{~V}_{\mathrm{cm}}=\mathrm{V}_{\mathrm{EE}}+\left(\mathrm{V}_{\mathrm{S}} / 2\right), \mathrm{R}_{\mathrm{L}}\right.$ tied to $\mathrm{V}_{\mathrm{cm}}$, unless specified)

+5 V Typical Performance ( $\mathrm{A}_{\mathrm{v}}=+2, \mathrm{R}_{\mathrm{f}}=1 \mathrm{k} \Omega, \mathrm{R}_{\mathrm{L}}=100 \Omega, \mathrm{~V}_{\mathrm{s}}=+5 \mathrm{~V}^{1}, \mathrm{~V}_{\mathrm{cm}}=\mathrm{V}_{\mathrm{EE}}+\left(\mathrm{V}_{\mathrm{s}} / 2\right), \mathrm{R}_{\mathrm{L}}$ tied to $\mathrm{V}_{\mathrm{cm}}$, unless specified)






## $\pm 5 \mathrm{~V}$ Tpical Performance $\left(A_{\mathrm{v}}=+2, R_{\mathrm{f}}=1 \mathrm{k} \Omega, R_{\mathrm{L}}=100 \Omega, \mathrm{~V}_{\mathrm{Cc}}= \pm 5 \mathrm{~V}\right.$, unless specified)






Frequency Response vs. $R_{L}$


## $\pm 5 \mathrm{~V}$ Typical Performance ( $\mathrm{A}_{\mathrm{v}}=+2, \mathrm{R}_{\mathrm{f}}=1 \mathrm{k} \Omega, \mathrm{R}_{\mathrm{L}}=100 \Omega, \mathrm{~V}_{\mathrm{cc}}= \pm 5 \mathrm{~V}$, unless specified)



The CLC452 is a current feedback amplifier built in an advanced complementary bipolar process. The CLC452 operates from a single 5 V supply or dual $\pm 5 \mathrm{~V}$ supplies. Operating from a single supply, the CLC452 has the following features:

> - Provides 100 mA of output current while consuming 15 mW of power
> - Offers low $-78 /-85 \mathrm{~dB} 2 \mathrm{nd}$ and 3 rd harmonic distortion
> - Provides $\mathrm{BW}>80 \mathrm{MHz}$ and 1 MHz distortion $<-70 \mathrm{dBc}$ at $\mathrm{V}_{\mathrm{o}}=2.0 \mathrm{~V}_{\mathrm{pp}}$

The CLC452 performance is further enhanced in $\pm 5 \mathrm{~V}$ supply applications as indicated in the $\pm 5 \mathrm{~V}$ Electrical Characteristics table and $\pm 5 \mathrm{~V}$ Typical Performance plots.

## Current Feedback Amplifiers

Some of the key features of current feedback technology are:

- Independence of AC bandwidth and voltage gain
- Inherently stable at unity gain
- Adjustable frequency response with feedback resistor
- High slew rate
- Fast settling

Current feedback operation can be described using a simple equation. The voltage gain for a non-inverting or inverting current feedback amplifier is approximated by Equation 1.

$$
\begin{equation*}
\frac{V_{0}}{V_{\text {in }}}=\frac{A_{v}}{1+\frac{R_{f}}{Z(j \omega)}} \tag{Equation 1}
\end{equation*}
$$

where:

- $A_{v}$ is the closed loop DC voltage gain
- $\mathrm{R}_{\mathrm{f}}$ is the feedback resistor
- Z(j $\omega$ ) is the CLC452's open loop transimpedance gain
$-\frac{Z(\mathrm{j} \omega)}{\mathrm{R}_{\mathrm{f}}}$ is the loop gain
The denominator of Equation 1 is approximately equal to 1 at low frequencies. Near the -3dB corner frequency, the interaction between $\mathrm{R}_{\mathrm{f}}$ and $\mathrm{Z}(\mathrm{j} \omega)$ dominates the circuit performance. The value of the feedback resistor has a large affect on the circuits performance. Increasing $R_{f}$ has the following affects:
- Decreases loop gain
- Decreases bandwidth
- Reduces gain peaking
- Lowers pulse response overshoot
- Affects frequency response phase linearity

Refer to the Feedback Resistor Selection section for more details on selecting a feedback resistor value.

## CLC452 Design Information

Single Supply Operation ( $\mathrm{V}_{\mathrm{CC}}=+5 \mathrm{~V}, \mathrm{~V}_{\mathrm{EE}}=\mathrm{GND}$ ) The specifications given in the $\mathbf{+ 5 V}$ Electrical Characteristics table for single supply operation are measured with a common mode voltage $\left(\mathrm{V}_{\mathrm{cm}}\right)$ of $2.5 \mathrm{~V} . \mathrm{V}_{\mathrm{cm}}$ is the voltage around which the inputs are applied and the output voltages are specified.

Operating from a single +5 V supply, the Common Mode Input Range (CMIR) of the CLC452 is typically +0.8 V to +4.2 V . The typical output range with $\mathrm{R}_{\mathrm{L}}=100 \Omega$ is +1.0 V to +4.0 V .

Figure 1: Non-Inverting Configuration

For single supply DC coupled operation, keep input signal levels above 0.8 V DC. For input signals that drop below 0.8 V DC, AC coupling and level shifting the signal are recommended. The non-inverting and inverting configurations for both input conditions are illustrated in the following 2 sections.

## DC Coupled Single Supply Operation

Figures 1 and 2 show the recommended non-inverting and inverting configurations for input signals that remain above 0.8 V DC.


Figure 2: Inverting Configuration

## AC Coupled Single Supply Operation

Figures 3 and 4 show possible non-inverting and inverting configurations for input signals that go below 0.8 V DC. The input is AC coupled to prevent the need for level shifting the input signal at the source. The resistive voltage divider biases the non-inverting input to $\mathrm{V}_{\mathrm{CC}} \div 2$ $=2.5 \mathrm{~V}$ (For $\mathrm{V}_{\mathrm{CC}}=+5 \mathrm{~V}$ ).

low frequency cutoff $=\frac{1}{2 \pi R_{\text {in }} C_{c}}$, where: $R_{\text {in }}=\frac{R}{2} \quad R \gg R_{\text {source }}$
Figure 3: AC Coupled Non-Inverting Configuration


Figure 4: AC Coupled Inverting Configuration

## Dual Supply Operation

The CLC452 operates on dual supplies as well as single supplies. The non-inverting and inverting configurations are shown in Figures 5 and 6.


Figure 5: Dual Supply Non-Inverting Configuration


Figure 6: Dual Supply Inverting Configuration

## Feedback Resistor Selection

The feedback resistor, $\mathrm{R}_{\mathrm{f}}$, affects the loop gain and frequency response of a current feedback amplifier. Optimum performance of the CLC452, at a gain of $+2 \mathrm{~V} / \mathrm{V}$, is achieved with $R_{f}$ equal to $1 \mathrm{k} \Omega$. The frequency response plots in the Typical Performance sections illustrate the recommended $\mathrm{R}_{\mathrm{f}}$ for several gains. These recommended values of $R_{f}$ provide the maximum bandwidth with minimal peaking. Within limits, $R_{f}$ can be adjusted to optimize the frequency response.

- Decrease $\mathrm{R}_{\mathrm{f}}$ to peak frequency response and extend bandwidth
- Increase $R_{f}$ to roll off frequency response and compress bandwidth

As a rule of thumb, if the recommended $R_{f}$ is doubled, then the bandwidth will be cut in half.

## Unity Gain Operation

The recommended $\mathrm{R}_{\mathrm{f}}$ for unity gain ( $+1 \mathrm{~V} / \mathrm{V}$ ) operation is $1 \mathrm{k} \Omega . \mathrm{R}_{\mathrm{g}}$ is left open. Parasitic capacitance at the inverting node may require a slight increase in $R_{f}$ to maintain a flat frequency response.

## Bandwidth vs. Output Amplitude

The bandwidth of the CLC452 is at a maximum for output voltages near $1 V_{p p}$. The bandwidth decreases for smaller and larger output amplitudes. Refer to the Frequency Response vs. $V_{o}$ plots.

## Load Termination

The CLC452 can source and sink near equal amounts of current. For optimum performance, the load should be tied to $\mathrm{V}_{\mathrm{cm}}$.

## Driving Cables and Capacitive Loads

When driving cables, double termination is used to prevent reflections. For capacitive load applications, a small series resistor at the output of the CLC452 will improve stability and settling performance. The Frequency Response vs. $C_{L}$ and Recommended $R_{s}$ vs. $C_{L}$ plots, in the typical performance section, give the recommended series resistance value for optimum flatness at various capacitive loads.

## Transmission Line Matching

One method for matching the characteristic impedance $\left(Z_{0}\right)$ of a transmission line or cable is to place the appropriate resistor at the input or output of the amplifier. Figure 7 shows typical inverting and non-inverting circuit configurations for matching transmission lines.


Figure 7: Transmission Line Matching
Non-inverting gain applications:

- Connect $R_{g}$ directly to ground.
- Make $\mathrm{R}_{1}, \mathrm{R}_{2}, \mathrm{R}_{6}$, and $\mathrm{R}_{7}$ equal to $\mathrm{Z}_{0}$.
- Use $R_{3}$ to isolate the amplifier from reactive loading caused by the transmission line, or by parasitics.

Inverting gain applications:

- Connect $\mathrm{R}_{3}$ directly to ground.
- Make the resistors $R_{4}, R_{6}$, and $R_{7}$ equal to $Z_{0}$.
- Make $\mathrm{R}_{5}$ II $\mathrm{R}_{\mathrm{g}}=\mathrm{Z}_{\mathrm{o}}$.

The input and output matching resistors attenuate the signal by a factor of 2 , therefore additional gain is needed. Use $\mathrm{C}_{6}$ to match the output transmission line over a greater frequency range. $\mathrm{C}_{6}$ compensates for the increase of the amplifier's output impedance with frequency.

## Power Dissipation

Follow these steps to determine the power consumption of the CLC452:

1. Calculate the quiescent (no-load) power: $P_{\mathrm{amp}}=\mathrm{I}_{\mathrm{CC}}\left(\mathrm{V}_{\mathrm{CC}}-\mathrm{V}_{\mathrm{EE}}\right)$
2. Calculate the RMS power at the output stage: $P_{\mathrm{O}}=\left(\mathrm{V}_{\mathrm{CC}}-\mathrm{V}_{\text {load }}\right)\left(\mathrm{I}_{\text {load }}\right)$, where $\mathrm{V}_{\text {load }}$ and $\mathrm{I}_{\text {load }}$ are the RMS voltage and current across the external load.
3. Calculate the total RMS power:
$P_{t}=P_{a m p}+P_{o}$
The maximum power that the DIP, SOIC, and SOT packages can dissipate at a given temperature is illustrated in Figure 8. The power derating curve for any CLC452 package can be derived by utilizing the following equation:

$$
\frac{\left(175^{\circ}-\mathrm{T}_{\mathrm{amb}}\right)}{\theta_{\mathrm{JA}}}
$$

where
$\mathrm{T}_{\mathrm{amb}}=$ Ambient temperature $\left({ }^{\circ} \mathrm{C}\right)$
$\theta_{\mathrm{JA}}=$ Thermal resistance, from junction to ambient, for a given package $\left({ }^{\circ} \mathrm{C} / \mathrm{W}\right)$


Figure 8: Power Derating Curves

## Layout Considerations

A proper printed circuit layout is essential for achieving high frequency performance. Comlinear provides evaluation boards for the CLC452 (730013-DIP, 730027SOIC, 730068-SOT) and suggests their use as a guide for high frequency layout and as an aid for device testing and characterization.

General layout and supply bypassing play major roles in high frequency performance. Follow the steps below as a basis for high frequency layout:

■ Include $6.8 \mu \mathrm{~F}$ tantalum and $0.1 \mu \mathrm{~F}$ ceramic capacitors on both supplies.

- Place the $6.8 \mu \mathrm{~F}$ capacitors within 0.75 inches of the power pins.
- Place the $0.1 \mu \mathrm{~F}$ capacitors less than 0.1 inches from the power pins.
- Remove the ground plane under and around the part, especially near the input and output pins to reduce parasitic capacitance.
- Minimize all trace lengths to reduce series inductances.
- Use flush-mount printed circuit board pins for prototyping, never use high profile DIP sockets.


## Evaluation Board Information

Data sheets are available for the CLC730013/ CLC730027 and CLC730068 evaluation boards. The evaluation board data sheets provide:

- Evaluation board schematics
- Evaluation board layouts
- General information about the boards

The CLC730013/CLC730027 data sheet also contains tables of recommended components to evaluate several of Comlinear's high speed amplifiers. This table for the CLC452 is illustrated below. Refer to the evaluation board data sheet for schematics and further information.

## Components Needed to Evaluate the CLC452 on the Evaluation Board:

- $\mathrm{R}_{\mathrm{f}}, \mathrm{R}_{\mathrm{g}}$ - Use this product data sheet to select values
- $\mathrm{R}_{\text {in }}, \mathrm{R}_{\text {out }}$ - Typically $50 \Omega$ (Refer to the Basic Operation section of the evaluation board data sheet for details)
$\square R_{t}$ - Optional resistor for inverting gain configurations (Select $R_{t}$ to yield desired input impedance
$\left.=R_{g} \| R_{t}\right)$
- $\mathrm{C}_{1}, \mathrm{C}_{2}-0.1 \mu \mathrm{~F}$ ceramic capacitors

■ $\mathrm{C}_{3}, \mathrm{C}_{4}-6.8 \mu \mathrm{~F}$ tantalum capacitors
Components not used:

- $\mathrm{C}_{5}, \mathrm{C}_{6}, \mathrm{C}_{7}, \mathrm{C}_{8}$
- $\mathrm{R}_{1}$ thru $\mathrm{R}_{8}$

The evaluation boards are designed to accommodate dual supplies. The boards can be modified to provide single supply operation. For best performance; 1) do not connect the unused supply, 2) ground the unused supply pin.

## SPICE Models

SPICE models provide a means to evaluate amplifier designs. Free SPICE models are available for Comlinear's monolithic amplifiers that:

- Support Berkeley SPICE 2G and its many derivatives
- Reproduce typical DC, AC, Transient, and Noise performance
- Support room temperature simulations

The readme file that accompanies the diskette lists released models, and provides a list of modeled parameters. The application note OA-18, Simulation SPICE Models for Comlinear's Op Amps, contains schematics and a reproduction of the readme file.

## Application Circuits

## Single Supply Cable Driver

The typical application shown on the front page shows the CLC452 driving 10 m of $75 \Omega$ coaxial cable. The CLC452 is set for a gain of $+2 \mathrm{~V} / \mathrm{V}$ to compensate for the divide-by-two voltage drop at $\mathrm{V}_{0}$.

## Single Supply Lowpass Filter

Figures 9 and 10 illustrate a lowpass filter and design equations. The circuit operates from a single supply of +5 V . The voltage divider biases the non-inverting input to 2.5 V . And the input is AC coupled to prevent the need for level shifting the input signal at the source. Use the design equations to determine $R_{1}, R_{2}, C_{1}$, and $C_{2}$ based on the desired $Q$ and corner frequency.


Figure 9: Lowpass Filter Topology

$$
\begin{aligned}
& \text { Gain }=K=1+\frac{R_{f}}{R_{g}} \\
& \text { Corner frequency }=\omega_{C}=\sqrt{\frac{1}{R_{1} R_{2} C_{1} C_{2}}} \\
& Q=\frac{1}{\sqrt{\frac{R_{2} C_{2}}{R_{1} C_{1}}}+\sqrt{\frac{R_{1} C_{2}}{R_{2} C_{1}}}+(1-K) \sqrt{\frac{R_{1} C_{1}}{R_{2} C_{2}}}} \\
& \text { For } R_{1}=R_{2}=R \text { and } C_{1}=C_{2}=C \\
& \omega_{C}=\frac{1}{R C} \\
& Q=\frac{1}{(3-K)}
\end{aligned}
$$

Figure 10: Design Equations
This example illustrates a lowpass filter with $Q=0.707$ and corner frequency $f_{c}=10 \mathrm{MHz}$. A Q of 0.707 was chosen to achieve a maximally flat, Butterworth response. Figure 11 indicates the filter response.


Figure 11: Lowpass Response

## Twisted Pair Driver

The high output current and low distortion, of the CLC452, make it well suited for driving transformers. Figure 12 illustrates a typical twisted pair driver utilizing the CLC452 and a transformer. The transformer provides the signal and its inversion for the twisted pair.


Figure 12: Twisted Pair Driver
To match the line's characteristic impedance $\left(Z_{0}\right)$ set:

$$
\begin{aligned}
& -\mathrm{R}_{\mathrm{L}}=\mathrm{Z}_{\mathrm{o}} \\
& -\mathrm{R}_{\mathrm{m}}=\mathrm{R}_{\mathrm{eq}}
\end{aligned}
$$

Where $R_{e q}$ is the transformed value of the load impedance, $\left(R_{L}\right)$, and is approximated by:

$$
R_{e q}=\frac{R_{L}}{n^{2}}
$$

Select the transformer so that it loads the line with a value close to $Z_{0}$, over the desired frequency range. The output impedance, $\mathrm{R}_{0}$, of the CLC452 varies with frequency and can also affect the return loss. The return loss, shown below, takes into account an ideal transformer and the value of $R_{0}$.
Return Loss $(d B) \approx-20 \log _{10}\left|n^{2} \cdot \frac{R_{0}}{Z_{0}}\right|$

The load current $\left(\mathrm{I}_{\mathrm{L}}\right)$ and voltage $\left(\mathrm{V}_{0}\right)$ are related to the CLC452's maximum output voltage and current by:

$$
\begin{aligned}
& \left|V_{0}\right| \leq n \cdot V_{\max } \\
& \left|I_{L}\right| \leq \frac{I_{\max }}{n}
\end{aligned}
$$

From the above current relationship, it is obvious that an amplifier with high output drive capability is required.

## Customer Design Applications Support

National Semiconductor is committed to design excellence. For sales, literature and technical support, call the National Semiconductor Customer Response Group at 1-800-272-9959 or fax 1-800-737-7018.

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## Comlinear CLC453 <br> Single Supply, Low-Power, High Output, Programmable Buffer

## General Description

The Comlinear CLC453 is a low cost, high speed (110MHz) buffer that features user-programmable gains of $+2,+1$, and $-1 \mathrm{~V} / \mathrm{V}$. It has a new output stage that delivers high output drive current ( 100 mA ), but consumes minimal quiescent supply current $(3.0 \mathrm{~mA})$ from a single 5 V supply. Its current feedback architecture, fabricated in an advanced complementary bipolar process, maintains consistent performance over a programmable range of gains and wide signal levels, and has a linear-phase response up to one half of the -3dB frequency. The CLC453's internal feedback network provides an excellent gain accuracy of $0.3 \%$

The CLC453 offers superior dynamic performance with a 110 MHz small-signal bandwidth, $370 \mathrm{~V} / \mu \mathrm{s}$ slew rate and 4.8 ns rise/fall times $\left(2 \mathrm{~V}_{\text {step }}\right)$. The combination of the small SOT23-5 package, low quiescent power, high output current drive, and high-speed performance make the CLC453 well suited for many batterypowered personal communication/computing systems.

The ability to drive low-impedance, highly capacitive loads, makes the CLC453 ideal for single ended cable applications. It also drives low impedance loads with minimum distortion. The CLC453 will drive a $100 \Omega$ load with only $-72 /-74 \mathrm{dBc}$ second/third harmonic distortion ( $\mathrm{A}_{\mathrm{v}}=+2, \mathrm{~V}_{\text {out }}=2 \mathrm{~V}_{\mathrm{pp}}, \mathrm{f}=1 \mathrm{MHz}$ ). With a $25 \Omega$ load, and the same conditions, it produces only $-65 /-77 \mathrm{dBc}$ second/third harmonic distortion. It is also optimized for driving high currents into single-ended transformers and coils.

When driving the input of high-resolution $A / D$ converters, the CLC453 provides excellent -65/-84dBc second/third harmonic distortion ( $\mathrm{A}_{\mathrm{v}}=+2, \mathrm{~V}_{\text {out }}=2 \mathrm{~V}_{\mathrm{pp}}, \mathrm{f}=1 \mathrm{MHz}, \mathrm{R}_{\mathrm{L}}=1 \mathrm{k} \Omega$ ) and fast settling time.

## Features

- 100 mA output current
- 3.0 mA supply current
- 110 MHz bandwidth $\left(\mathrm{A}_{\mathrm{v}}=+2\right)$
- $-65 /-84 \mathrm{dBc}$ HD2/HD3 ( 1 MHz )
- 25 ns settling to $0.05 \%$
- 370V/ $\mu \mathrm{s}$ slew rate
- Stable for capacitive loads up to 1000 pF
- Single 5 V to $\pm 5 \mathrm{~V}$ supplies
- Available in Tiny SOT23-5 package


## Applications

- Coaxial cable driver
- Twisted pair driver
- Transformer/Coil Driver
- High capacitive load driver
- Video line driver
- Portable/battery-powered applications
- A/D driver


+5 V Electrical Characteristics ( $\mathrm{A}_{\mathrm{v}}=+2, \mathrm{R}_{\mathrm{L}}=100 \Omega, \mathrm{~V}_{\mathrm{s}}=+5 \mathrm{~V}^{1}, \mathrm{~V}_{\mathrm{cm}}=\mathrm{V}_{\mathrm{EE}}+\left(\mathrm{V}_{\mathrm{s}} / 2\right), \mathrm{R}_{\mathrm{L}}$ tied to $\mathrm{V}_{\mathrm{cm}}$, unless specified)

| PARAMETERS | CONDITIONS | TYP | MIN/MAX RATINGS |  |  | UNITS | NOTES |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| Ambient Temperature | CLC453AJ | $+25^{\circ} \mathrm{C}$ | $+25^{\circ} \mathrm{C}$ | 0 to $70^{\circ} \mathrm{C}$ | -40 to $85^{\circ} \mathrm{C}$ |  |  |
| FREQUENCY DOMAIN RESPONSE |  |  |  |  |  |  |  |
| -3dB bandwidth | $\mathrm{V}_{\mathrm{o}}=0.5 \mathrm{~V}_{\mathrm{pp}}$ | 110 | 85 | 75 | 70 | MHz | B |
|  | $\mathrm{V}_{\mathrm{o}}=2.0 \mathrm{~V}_{\mathrm{pp}}$ | 90 | 75 | 72 | 70 | MHz |  |
| -0.1dB bandwidth | $\mathrm{V}_{\mathrm{o}}=0.5 \mathrm{~V}_{\mathrm{pp}}$ | 25 | 22 | 22 | 18 | MHz |  |
| gain peaking | $<200 \mathrm{MHz}, \mathrm{V}_{\mathrm{o}}=0.5 \mathrm{~V}_{\mathrm{pp}}$ | 0 | 0.5 | 0.9 | 1.0 | dB | B |
| gain rolloff | $<30 \mathrm{MHz}, \mathrm{V}_{\mathrm{o}}=0.5 \mathrm{~V}_{\mathrm{pp}}$ | 0.2 | 0.4 | 0.6 | 0.6 | dB | B |
| linear phase deviation | $<30 \mathrm{MHz}, \mathrm{V}_{\mathrm{o}}=0.5 \mathrm{~V}_{\mathrm{pp}}$ | 0.1 | 2 | 3 | 3 | deg |  |
| TIME DOMAIN RESPONSE |  |  |  |  |  |  |  |
| rise and fall time | 2 V step | 4.8 | 6.4 | 6.8 | 7.3 | ns |  |
| settling time to 0.05\% | 1V step | 25 | - | - |  | ns |  |
| overshoot | 2 V step | 9 | 13 | 16 | 16 | \% |  |
| slew rate | 2 V step | 370 | 280 | 250 | 240 | V/us |  |
| DISTORTION AND NOISE RESPONSE |  |  |  |  |  |  | B |
| $2^{\text {nd }}$ harmonic distortion$3^{\text {rd }}$ harmonic distortion | $2 \mathrm{~V}_{\mathrm{pp}}, 1 \mathrm{MHz}$ | -72 | -66 | -64 | -64 | dBc |  |
|  | $2 \mathrm{~V}_{\mathrm{pp}}, 1 \mathrm{MHz} ; \mathrm{R}_{\mathrm{L}}=1 \mathrm{k} \Omega$ | -65 | -59 | -57 | -57 | dBc |  |
|  | $2 \mathrm{~V}_{\mathrm{pp}}, 5 \mathrm{MHz}$ | -65 | -56 | -54 | -54 | dBc |  |
|  | $2 \mathrm{~V}_{\mathrm{pp}}, 1 \mathrm{MHz}$ | -74 | -70 | -68 | -68 | dBc |  |
| $3^{\text {rd }}$ harmonic distortion | $2 \mathrm{~V}_{\mathrm{pp}}, 1 \mathrm{MHz} ; \mathrm{R}_{\mathrm{L}}=1 \mathrm{k} \Omega$ | -84 | -76 | -74 | -74 | dBc |  |
|  | $2 \mathrm{~V}_{\mathrm{pp}}, 5 \mathrm{MHz}$ | -60 | -55 | -53 | -53 | dBc | B |
| equivalent input noise |  | 2.8 | 3.5 | 3.8 | 3.8 | $\mathrm{nV} / \sqrt{ } \mathrm{Hz}$ |  |
| non-inverting current ( $\mathrm{i}_{\mathrm{bn}}$ ) | $>1 \mathrm{MHz}$ | 7.5 | 10 | 11 | 11 | $\mathrm{pA} / \sqrt{ } \mathrm{Hz}$ |  |
| inverting current ( $\mathrm{i}_{\mathrm{b}}$ ) | $>1 \mathrm{MHz}$ | 10.5 | 14 | 15 | 15 | $\mathrm{pA} / \sqrt{ } \mathrm{Hz}$ |  |
| STATIC DC PERFORMANCE |  |  |  |  |  |  |  |
| input offset voltage average drift |  | 13 | 30 | 35 | 35 | mV | A |
|  |  | 80 | - | - | - | $\mu \mathrm{V} /{ }^{\circ} \mathrm{C}$ |  |
| input bias current (non-inverting) |  | 5 | 18 | 22 | 24 | $\mu \mathrm{A}$ | A |
| average drift |  | 30 | - | - | - | $n A /{ }^{\circ} \mathrm{C}$ |  |
| gain accuracy |  | $\pm 0.3$ | $\pm 1.5$ | $\pm 2.0$ | $\pm 2.0$ | \% | A |
| internal resistors ( $\mathrm{R}_{\mathrm{f}}, \mathrm{R}_{\mathrm{g}}$ ) |  | 1000 | $\pm 20 \%$ | $\pm 26 \%$ | $\pm 30 \%$ | $\Omega$ |  |
| power supply rejection ratio | DC | 48 | 45 | 43 | 43 | dB | B |
| common-mode rejection ratio | DC | 51 | 48 | 46 | 46 | dB |  |
| supply current | $\mathrm{R}_{\mathrm{L}}=\infty$ | 3.0 | 3.4 | 3.6 | 3.6 | mA | A |
| MISCELLANEOUS PERFORMANCE |  |  |  |  |  |  |  |
| input resistance (non-inverting) |  | 0.39 | 0.28 | 0.25 | 0.25 | $\mathrm{M} \Omega$ |  |
| input capacitance (non-inverting) |  | 1.5 | 2.3 | 2.3 | 2.3 | pF |  |
| input voltage range, High |  | 4.2 | 4.1 | 4.0 | 4.0 | V |  |
| input voltage range, Low |  | 0.8 | 0.9 | 1.0 | 1.0 | V |  |
| output voltage range, High | $\mathrm{R}_{\mathrm{L}}=100 \Omega$ | 4.0 | 3.9 | 3.8 | 3.8 | V |  |
| output voltage range, Low | $R_{L}=100 \Omega$ | 1.0 | 1.1 | 1.2 | 1.2 | V |  |
| output voltage range, High | $\mathrm{R}_{\mathrm{L}}=\infty$ | 4.1 | 4.0 | 4.0 | 3.9 | V |  |
| output voltage range, Low | $\mathrm{R}_{\mathrm{L}}=\infty$ | 0.9 | 1.0 | 1.0 | 1.1 | V |  |
| output current |  | 100 | 80 | 65 | 40 | mA | C |
| output resistance, closed loop | DC | 400 | 600 | 600 | 600 | $\mathrm{m} \Omega$ |  |

$\mathrm{Min} / \mathrm{max}$ ratings are based on product characterization and simulation. Individual parameters are tested as noted. Outgoing quality levels are determined from tested parameters.

## Notes

A) J-level: spec is $100 \%$ tested at $+25^{\circ} \mathrm{C}$, sample tested at $+85^{\circ} \mathrm{C}$.
B) J-level: spec is sample tested at $+25^{\circ} \mathrm{C}$.
C) The short circuit current can exceed the maximum safe output current.

1) $V_{S}=V_{C C}-V_{E E}$

## Reliability Information

[^1]Absolute Maximum Ratings
supply voltage $\left(\mathrm{V}_{\mathrm{CC}}-\mathrm{V}_{\mathrm{EE}}\right)$ output current (see note C) common-mode input voltage maximum junction temperature storage temperature range lead temperature (soldering 10 sec ) ESD rating (human body model)
$\pm 5 \mathrm{~V}$ Electrical Characteristics ( $\mathrm{A}_{\mathrm{V}}=+2, \mathrm{R}_{\mathrm{L}}=100 \Omega, \mathrm{v}_{\mathrm{cc}}= \pm 5 \mathrm{~V}$, unless specified)

| PARAMETERS | CONDITIONS | TYP | GUARANTEED MIN/MAX |  |  | UNITS | NOTES |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| Ambient Temperature | CLC453AJ | $+25^{\circ} \mathrm{C}$ | $+25^{\circ} \mathrm{C}$ | 0 to $70^{\circ} \mathrm{C}$ | -40 to $85^{\circ} \mathrm{C}$ |  |  |
| FREQUENCY DOMAIN RESPONSE |  |  |  |  |  |  |  |
| -3dB bandwidth | $\mathrm{V}_{\mathrm{o}}=1.0 \mathrm{~V}_{\mathrm{pp}}$ | 130 | 105 | 95 | 90 | MHz |  |
|  | $\mathrm{V}_{\mathrm{o}}=4.0 \mathrm{~V}_{\mathrm{pp}}$ | 70 | 55 | 52 | 50 | MHz |  |
| -0.1 dB bandwidth | $\mathrm{V}_{0}=1.0 \mathrm{~V}_{\mathrm{pp}}$ | 30 | 25 | 25 | 20 | MHz |  |
| gain peaking | $<200 \mathrm{MHz}, \mathrm{V}_{0}=1.0 \mathrm{~V}_{\mathrm{pp}}$ | 0 | 0.5 | 0.9 | 1.0 | dB |  |
| gain rolloff | $<30 \mathrm{MHz}, \mathrm{V}_{\mathrm{o}}=1.0 \mathrm{~V}_{\mathrm{pp}}$ | 0.2 | 0.7 | 0.8 | 0.8 | dB |  |
| linear phase deviation | $<30 \mathrm{MHz}, \mathrm{V}_{0}=1.0 \mathrm{~V}_{\mathrm{pp}}$ | 0.1 | 0.2 | 0.3 | 0.3 | deg |  |
| differential gain | NTSC, $\mathrm{R}_{\mathrm{L}}=150 \Omega$ | 0.3 | - | - | - | \% |  |
| differential phase | NTSC, $\mathrm{R}_{\mathrm{L}}=150 \Omega$ | 0.1 | - | - | - | deg |  |
| TIME DOMAIN RESPONSE |  |  |  |  |  |  |  |
| rise and fall time | 2 V step | 3.8 | 4.8 | 5.1 | 5.6 | ns |  |
| settling time to $0.05 \%$ | 2 V step | 20 | - | - | - | ns |  |
| overshoot | 2 V step | 6 | 10 | 13 | 13 | \% |  |
| slew rate | 2 V step | 460 | 340 | 315 | 300 | V/ $\mu \mathrm{s}$ |  |
| DISTORTION AND NOISE RESPONSE |  |  |  |  |  |  |  |
| $2^{\text {nd }}$ harmonic distortion | $2 \mathrm{~V}_{\mathrm{pp}}, 1 \mathrm{MHz}$ | -82 | -74 | -72 | -72 | dBc |  |
|  | $2 \mathrm{~V}_{\mathrm{pp}}, 1 \mathrm{MHz} ; \mathrm{R}_{\mathrm{L}}=1 \mathrm{k} \Omega$ | -69 | -63 | -61 | -61 | dBc |  |
|  | $2 V_{p p}^{p p}, 5 \mathrm{MHz}$ | -65 | -59 | -57 | -57 | dBc |  |
| $3{ }^{\text {rd }}$ harmonic distortion | $2 \mathrm{~V}_{\mathrm{pp}}, 1 \mathrm{MHz}$ | -73 | -69 | -67 | -67 | dBc |  |
|  | $2 \mathrm{~V}_{\mathrm{pp}}, 1 \mathrm{MHz} ; \mathrm{R}_{\mathrm{L}}=1 \mathrm{k} \Omega$ | -90 | -80 | -78 | -78 | dBc |  |
| equivalent input noise | $2 \mathrm{~V}_{\mathrm{pp}}, 5 \mathrm{MHz}$ | -60 | -56 | -54 | -54 | dBc |  |
|  | $>1 \mathrm{MHz}$ | 2.8 | 3.5 | 3.8 | 3.8 | $\mathrm{nV} / \sqrt{ } \mathrm{Hz}$ |  |
| non-inverting current ( $\mathrm{i}_{\text {bn }}$ ) | $>1 \mathrm{MHz}$ | 7.5 | 10 | 11 | 11 | $\mathrm{pA} / \sqrt{ } \mathrm{Hz}$ |  |
| inverting current ( $\mathrm{ib}_{\mathrm{b}}$ ) | $>1 \mathrm{MHz}$ | 10.5 | 14 | 15 | 15 | $\mathrm{pA} / \mathrm{NHz}$ |  |
| STATIC DC PERFORMANCE |  |  |  |  |  |  |  |
| output offset voltage average drift |  | 7 80 | 30 - | 35 - | 35 - | $\underset{\mu \mathrm{V} /{ }^{\circ} \mathrm{C}}{\mathrm{mV}}$ |  |
| input bias current (non-inverting) |  | 3 | 18 | 23 | 25 | $\mu \mathrm{A}$ | B |
| average drift |  | 40 | - | - | - | $n A /{ }^{\circ} \mathrm{C}$ |  |
| gain accuracy |  | $\pm 0.3$ | $\pm 1.5$ | $\pm 2.0$ | $\pm 2.0$ | \% |  |
| internal resistors ( $\mathrm{R}_{\mathrm{f}}, \mathrm{R}_{\mathrm{g}}$ ) |  | 1000 | $\pm 20 \%$ | $\pm 26 \%$ | $\pm 30 \%$ | $\Omega$ |  |
| power supply rejection ratio | DC | 50 | 47 | 45 | 45 | dB |  |
| common-mode rejection ratio | DC | 53 | 50 | 48 | 48 | dB |  |
| supply current | $\mathrm{R}_{\mathrm{L}}=\infty$ | 3.2 | 3.8 | 4.0 | 4.0 | mA | B |
| MISCELLANEOUS PERFORMAN |  |  |  |  |  |  |  |
| input resistance (non-inverting) |  | 0.52 | 0.35 | 0.30 | 0.30 | $\mathrm{M} \Omega$ |  |
| input capacitance (non-inverting) |  | 1.2 | 1.8 | 1.8 | 1.8 | pF |  |
| common-mode input range |  | $\pm 4.2$ | $\pm 4.1$ | $\pm 4.1$ | $\pm 4.0$ | V |  |
| output voltage range | $R_{L}=100 \Omega$ | $\pm 3.8$ | $\pm 3.6$ | $\pm 3.6$ | $\pm 3.5$ | V |  |
| output voltage range | $\mathrm{R}_{\mathrm{L}}=\infty$ | $\pm 4.0$ | $\pm 3.8$ | $\pm 3.8$ | $\pm 3.7$ | V |  |
| output current |  | 130 | 100 | 80 | 50 | mA | C |
| output resistance, closed loop | DC | 400 | 600 | 600 | 600 | $\mathrm{m} \Omega$ |  |

## Notes

B) J-level: spec is sample tested at $+25^{\circ} \mathrm{C}$.
C) The short circuit current can exceed the maximum safe output current.

## Package Thermal Resistance

| Package | $\boldsymbol{\theta}_{\text {JC }}$ | $\boldsymbol{\theta}_{\text {JA }}$ |
| :--- | :---: | :---: |
| Plastic (AJP) | $115^{\circ} \mathrm{C} / \mathrm{W}$ | $125^{\circ} \mathrm{C} / \mathrm{W}$ |
| Surface Mount (AJE) | $130^{\circ} \mathrm{C} / \mathrm{W}$ | $150^{\circ} \mathrm{C} / \mathrm{W}$ |
| Surface Mount (AJM5) | $140^{\circ} \mathrm{C} / \mathrm{W}$ | $210^{\circ} \mathrm{C} / \mathrm{W}$ |
| Dice (ALC) | $25^{\circ} \mathrm{C} / \mathrm{W}$ | - |

## Ordering Information

| Model | Temperature Range | Description |
| :--- | :---: | :--- |
| CLC453AJP | $-40^{\circ} \mathrm{C}$ to $+85^{\circ} \mathrm{C}$ | 8-pin PDIP |
| CLC453AJE | $-40^{\circ} \mathrm{C}$ to $+85^{\circ} \mathrm{C}$ | 8-pin SOIC |
| CLC43AJM5 | $-40^{\circ} \mathrm{C}$ to $+85^{\circ} \mathrm{C}$ | 5 -pin SOT |
| CLC453ALC | $-40^{\circ} \mathrm{C}$ to $+85^{\circ} \mathrm{C}$ | dice |

+5 V Typical Performance $\left(\mathrm{A}_{\mathrm{v}}=+2, \mathrm{R}_{\mathrm{L}}=100 \Omega, \mathrm{~V}_{\mathrm{s}}=+5 \mathrm{~V}^{1}, \mathrm{~V}_{\mathrm{cm}}=\mathrm{V}_{\mathrm{EE}}+\left(\mathrm{V}_{\mathrm{S}} / 2\right), \mathrm{R}_{\mathrm{L}}\right.$ tied to $\mathrm{V}_{\mathrm{cm}}$, unless specified)

+5 V Typical Performance $\left(\mathrm{A}_{\mathrm{v}}=+2, \mathrm{R}_{\mathrm{L}}=100 \Omega, \mathrm{v}_{\mathrm{s}}=+5 \mathrm{~V}^{1}, \mathrm{~V}_{\mathrm{cm}}=\mathrm{V}_{\mathrm{EE}}+\left(\mathrm{V}_{\mathrm{S}} / 2\right)\right.$, $\mathrm{R}_{\mathrm{L}}$ tied to $\mathrm{V}_{\mathrm{cm}}$, unless specified)





Time (10ns/div)
$\pm 5 \mathrm{~V}$ Typical Performance ( $\mathrm{A}_{\mathrm{v}}=+2, \mathrm{R}_{\mathrm{L}}=100 \Omega, \mathrm{v}_{\mathrm{cc}}= \pm 5 \mathrm{~V}$, unless specified)





Frequency Response vs. $\mathrm{V}_{\mathbf{o}}\left(\mathrm{A}_{\mathrm{v}}=2\right)$


Frequency Response vs. $C_{L}$

$\pm 5 \mathrm{~V}$ Typical Performance ( $\mathrm{A}_{\mathrm{v}}=+2, \mathrm{R}_{\mathrm{L}}=100 \Omega, \mathrm{v}_{\mathrm{Cc}}= \pm 5 \mathrm{~V}$, unless specified)







Time (10ns/div)

3rd Harmonic Distortion, $\mathrm{R}_{\mathrm{L}}=\mathbf{2 5 \Omega}$


Output Amplitude ( $\mathrm{V}_{\mathrm{pp}}$ )


Output Amplitude ( $\mathrm{V}_{\mathrm{pp}}$ )


Short Term Settling Time







The CLC453 is a current feedback buffer built in an advanced complementary bipolar process. The CLC453 operates from a single 5 V supply or dual $\pm 5 \mathrm{~V}$ supplies. Operating from a single 5V supply, the CLC453 has the following features:

- Gains of $+1,-1$, and $2 \mathrm{~V} / \mathrm{V}$ are achievable without external resistors
- Provides 100 mA of output current while consuming only 15 mW of power
- Offers low -65/-84dBc 2nd and 3rd harmonic distortion
- Provides $\mathrm{BW}>80 \mathrm{MHz}$ and 1 MHz distortion $<-70 \mathrm{dBc}$ at $\mathrm{V}_{\mathrm{o}}=2 \mathrm{~V}_{\mathrm{pp}}$
The CLC453 performance is further enhanced in $\pm 5 \mathrm{~V}$ supply applications as indicated in the $\pm 5 \mathrm{~V}$ Electrical Characteristics table and $\pm 5 \mathrm{~V}$ Typical Performance plots.

If gains other than $+1,-1$, or $+2 \mathrm{~V} / \mathrm{V}$ are required, then the CLC452 can be used. The CLC452 is a current feedback amplifier with near identical performance and allows for external feedback and gain setting resistors.

## Current Feedback Amplifiers

Some of the key features of current feedback technology are:

- Independence of AC bandwidth and voltage gain
- Inherently stable at unity gain
- Adjustable frequency response with feedback resistor
- High slew rate
- Fast settling

Current feedback operation can be described using a simple equation. The voltage gain for a non-inverting or inverting current feedback amplifier is approximated by Equation 1.

$$
\frac{V_{0}}{V_{i n}}=\frac{A_{V}}{1+\frac{R_{f}}{Z(j \omega)}}
$$

Equation 1
where:

- $A_{v}$ is the closed loop DC voltage gain
- $R_{f}$ is the feedback resistor
- Z $(\mathrm{j} \omega)$ is the CLC453's open loop transimpedance gain
- $\frac{Z(\mathrm{j} \omega)}{\mathrm{R}_{\mathrm{f}}}$ is the loop gain

The denominator of Equation 1 is approximately equal to 1 at low frequencies. Near the -3dB corner frequency, the interaction between $R_{f}$ and $Z(j \omega)$ dominates the circuit performance. The value of the feedback resistor has a large affect on the circuits performance. Increasing $R_{f}$ has the following affects:

```
- Decreases loop gain
- Decreases bandwidth
- Reduces gain peaking
- Lowers pulse response overshoot
- Affects frequency response phase linearity
```


## CLC453 Design Information

## Closed Loop Gain Selection

The CLC453 is a current feedback op amp with $R_{f}=R_{g}=1 \mathrm{k} \Omega$ on chip (in the package). Select from three closed loop gains without using any external gain or feedback resistors. Implement gains of $+2,+1$, and $-1 \mathrm{~V} / \mathrm{V}$ by connecting pins 2 and 3 as described in the chart below.

| Gain | Input Connections |  |
| :---: | :---: | :---: |
| $\mathrm{A}_{\mathrm{V}}$ | Non-Inverting (pin3) | Inverting (pin2) |
| $-1 \mathrm{~V} / \mathrm{V}$ | ground | input signal |
| $+1 \mathrm{~V} / \mathrm{V}$ | input signal | NC (open) |
| $+2 \mathrm{~V} / \mathrm{V}$ | input signal | ground |

The gain accuracy of the CLC453 is excellent and stable over temperature change. The internal gain setting resistors, $R_{f}$ and $R_{g}$ are diffused silicon resistors with a process variation of $\pm 20 \%$ and a temperature coefficient of $\sim 2000 \mathrm{ppm} /{ }^{\circ} \mathrm{C}$. Although their absolute values change with processing and temperature, their ratio ( $R_{f} / R_{g}$ ) remains constant. If an external resistor is used in series with $\mathrm{R}_{\mathrm{g}}$, gain accuracy over temperature will suffer.

Single Supply Operation ( $\mathrm{V}_{\mathrm{CC}}=+5 \mathrm{~V}, \mathrm{~V}_{\mathrm{EE}}=\mathrm{GND}$ ) The specifications given in the $\mathbf{+ 5 V}$ Electrical Characteristics table for single supply operation are measured with a common mode voltage $\left(\mathrm{V}_{\mathrm{cm}}\right)$ of $2.5 \mathrm{~V} . \mathrm{V}_{\mathrm{cm}}$ is the voltage around which the inputs are applied and the output voltages are specified.

Operating from a single +5 V supply, the Common Mode Input Range (CMIR) of the CLC453 is typically +0.8 V to +4.2 V . The typical output range with $\mathrm{R}_{\mathrm{L}}=100 \Omega$ is +1.0 V to +4.0 V .

For single supply DC coupled operation, keep input signal levels above 0.8 V DC. For input signals that drop below 0.8 V DC, AC coupling and level shifting the signal are recommended. The non-inverting and inverting configurations for both input conditions are illustrated in the following 2 sections.

## DC Coupled Single Supply Operation

Figures 1, 2, and 3 on the following page, show the recommended configurations for input signals that remain above 0.8 V DC.


Figure 1: $D C$ Coupled, $A_{v}=-1 \mathrm{~V} / \mathrm{V}$ Configuration


Figure 2: DC Coupled, $\mathrm{A}_{\mathrm{v}}=+\mathbf{1 V} / \mathrm{V}$ Configuration


Figure 3: DC Coupled, $A_{v}=+2 V / V$ Configuration

## AC Coupled Single Supply Operation

Figures 4,5 , and 6 show possible non-inverting and inverting configurations for input signals that go below 0.8 V DC.


Figure 4: AC Coupled, $A_{v}=-1 \mathrm{~V} / \mathrm{V}$ Configuration

The input is AC coupled to prevent the need for level shifting the input signal at the source. The resistive voltage divider biases the non-inverting input to $\mathrm{V}_{\mathrm{CC}} \div 2$ $=2.5 \mathrm{~V}$ (For $\left.\mathrm{V}_{\mathrm{CC}}=+5 \mathrm{~V}\right)$.


Figure 5: AC Coupled, $\mathrm{A}_{\mathrm{v}}=+1 \mathrm{~V} / \mathrm{V}$ Configuration


Figure 6: AC Coupled, $\mathrm{A}_{\mathrm{v}}=\boldsymbol{+ 2 V} / \mathrm{V}$ Configuration

## Dual Supply Operation

The CLC453 operates on dual supplies as well as single supplies. The non-inverting and inverting configurations are shown in Figures 7, 8 and 9.


Figure 7: Dual Supply, $\mathrm{A}_{\mathrm{v}}=-1 \mathrm{~V} / \mathrm{V}$ Configuration


Figure 8: Dual Supply, $A_{v}=+1 V / V$ Configuration


Figure 9: Dual Supply, $\mathrm{A}_{\mathrm{v}}=\mathbf{+ 2 V} / \mathrm{V}$ Configuration

## Bandwidth vs. Output Amplitude

The bandwidth of the CLC453 is at a maximum for output voltages near $1 \mathrm{~V}_{\mathrm{pp}}$. The bandwidth decreases for smaller and larger output amplitudes. Refer to the
Frequency Response vs. $V_{o}$ plots.

## Load Termination

The CLC453 can source and sink near equal amounts of current. For optimum performance, the load should be tied to $\mathrm{V}_{\mathrm{cm}}$.

## Driving Cables and Capacitive Loads

When driving cables, double termination is used to prevent reflections. For capacitive load applications, a small series resistor at the output of the CLC453 will improve stability and settling performance. The Frequency Response vs. $C_{L}$ and Recommended $\boldsymbol{R}_{\boldsymbol{s}}$ vs. $C_{L}$ plots, in the typical performance section, give the recommended series resistance value for optimum flatness at various capacitive loads.

## Transmission Line Matching

One method for matching the characteristic impedance $\left(Z_{0}\right)$ of a transmission line or cable is to place the appropriate resistor at the input or output of the amplifier.

Figure 10 shows typical inverting and non-inverting circuit configurations for matching transmission lines.
Non-inverting gain applications:

- Connect pin 2 as indicated in the table in the Closed Loop Gain Selection section.
- Make $R_{1}, R_{2}, R_{6}$, and $R_{7}$ equal to $Z_{0}$.
- Use $\mathrm{R}_{3}$ to isolate the amplifier from reactive loading caused by the transmission line, or by parasitics.
Inverting gain applications:
- Connect $\mathrm{R}_{3}$ directly to ground.
- Make the resistors $\mathrm{R}_{4}, \mathrm{R}_{6}$, and $\mathrm{R}_{7}$ equal to $\mathrm{Z}_{0}$.
- Make $\mathrm{R}_{5}$ II $\mathrm{R}_{\mathrm{g}}=\mathrm{Z}_{\mathrm{o}}$.

The input and output matching resistors attenuate the signal by a factor of 2 , therefore additional gain is needed. Use $\mathrm{C}_{6}$ to match the output transmission line over a greater frequency range. $\mathrm{C}_{6}$ compensates for the increase of the amplifier's output impedance with frequency.


Figure 10: Transmission Line Matching

## Power Dissipation

Follow these steps to determine the power consumption of the CLC453:

1. Calculate the quiescent (no-load) power:

$$
P_{\mathrm{amp}}=I_{\mathrm{CC}}\left(\mathrm{~V}_{\mathrm{CC}}-\mathrm{V}_{\mathrm{EE}}\right)
$$

2. Calculate the RMS power at the output stage: $P_{\mathrm{O}}=\left(\mathrm{V}_{\mathrm{CC}}-\mathrm{V}_{\text {load }}\right)\left(I_{\text {load }}\right)$, where $\mathrm{V}_{\text {load }}$ and $\mathrm{I}_{\text {load }}$ are the RMS voltage and current across the external load.
3. Calculate the total RMS power:

$$
P_{t}=P_{a m p}+P_{o}
$$

The maximum power that the DIP, SOIC, and SOT packages can dissipate at a given temperature is illustrated in Figure 11. The power derating curve for any CLC453 package can be derived by utilizing the following equation:
where $\quad \frac{\left(175^{\circ}-\mathrm{T}_{\mathrm{amb}}\right)}{\theta_{\mathrm{JA}}}$
$\mathrm{T}_{\mathrm{amb}}=$ Ambient temperature $\left({ }^{\circ} \mathrm{C}\right)$
$\theta_{\mathrm{JA}}=$ Thermal resistance, from junction to ambient, for a given package ( ${ }^{\circ} \mathrm{C} / \mathrm{W}$ )


Figure 11: Power Derating Curve

## Layout Considerations

A proper printed circuit layout is essential for achieving high frequency performance. Comlinear provides evaluation boards for the CLC453 (CLC730013-DIP, CLC730027-SOIC, CLC730068-SOT) and suggests their use as a guide for high frequency layout and as an aid for device testing and characterization.

General layout and supply bypassing play major roles in high frequency performance. Follow the steps below as a basis for high frequency layout:

■ Include $6.8 \mu \mathrm{~F}$ tantalum and $0.1 \mu \mathrm{~F}$ ceramic capacitors on both supplies.
$■$ Place the $6.8 \mu \mathrm{~F}$ capacitors within 0.75 inches of the power pins.

- Place the $0.1 \mu \mathrm{~F}$ capacitors less than 0.1 inches from the power pins.
- Remove the ground plane under and around the part, especially near the input and output pins to reduce parasitic capacitance.
■ Minimize all trace lengths to reduce series inductances.
- Use flush-mount printed circuit board pins for prototyping, never use high profile DIP sockets.


## Evaluation Board Information

Data sheets are available for the CLC730013/ CLC730027 and CLC730068 evaluation boards. The evaluation board data sheets provide:

■ Evaluation board schematics

- Evaluation board layouts
- General information about the boards

The CLC730013/CLC730027 data sheet also contains tables of recommended components to evaluate several of Comlinear's high speed amplifiers. This table for the CLC453 is illustrated below. Refer to the evaluation board data sheet for schematics and further information.

## Components Needed to Evaluate the CLC453 on the Evaluation Board:

- $\mathrm{R}_{\text {in }}, \mathrm{R}_{\text {out }}$ - Typically $50 \Omega$ (Refer to the Basic Operation section of the evaluation board data sheet for details)

■ $R_{t}$ - Optional resistor for inverting gain configurations (Select $R_{t}$ to yield desired input impedance $\left.=R_{g} \| R_{t}\right)$

- $\mathrm{C}_{1}, \mathrm{C}_{2}-0.1 \mu \mathrm{~F}$ ceramic capacitors

■ $\mathrm{C}_{3}, \mathrm{C}_{4}-6.8 \mu \mathrm{~F}$ tantalum capacitors
Components not used:

- $\mathrm{C}_{5}, \mathrm{C}_{6}, \mathrm{C}_{7}, \mathrm{C}_{8}$
- $R_{1}$ thru $R_{8}$

The evaluation boards are designed to accommodate dual supplies. The boards can be modified to provide single supply operation. For best performance; 1) do not connect the unused supply, 2) ground the unused supply pin.

## Special Evaluation Board Considerations for the CLC453

To optimize off-isolation of the CLC453, cut the $R_{f}$ trace on both the CLC730013 and the CLC730027 evaluation boards. This cut minimizes capacitive feedthrough between the input and the output. Figure 12 shows where to cut both evaluation boards for improved off-isolation.


Figure 12: Evaluation Board Changes

## SPICE Models

SPICE models provide a means to evaluate amplifier designs. Free SPICE models are available for Comlinear's monolithic amplifiers that:

■ Support Berkeley SPICE 2G and its many derivatives

- Reproduce typical DC, AC, Transient, and Noise performance
- Support room temperature simulations

The readme file that accompanies the diskette lists released models, and provides a list of modeled parameters. The application note OA-18, Simulation SPICE Models for Comlinear's Op Amps, contains schematics and a reproduction of the readme file.

## Application Circuits

## Single Supply Cable Driver

The typical application shown on the front page shows the CLC453 driving 10 m of $75 \Omega$ coaxial cable. The CLC453 is set for a gain of $+2 \mathrm{~V} / \mathrm{V}$ to compensate for the divide-by-two voltage drop at $\mathrm{V}_{0}$.

## Twisted Pair Driver

The high output current and low distortion, of the CLC453, make it well suited for driving transformers. Figure 13 illustrates a typical twisted pair driver utilizing the CLC453 and a transformer. The transformer provides the signal and its inversion for the twisted pair.


Figure 13: Twisted Pair Driver
To match the line's characteristic impedance $\left(Z_{0}\right)$ set:

$$
\begin{aligned}
& \square R_{L}=Z_{o} \\
& -R_{m}=R_{e q}
\end{aligned}
$$

Where $R_{\text {eq }}$ is the transformed value of the load impedance, $\left(R_{L}\right)$, and is approximated by:

$$
R_{e q}=\frac{R_{L}}{n^{2}}
$$

Select the transformer so that it loads the line with a value close to $Z_{0}$, over the desired frequency range. The output impedance, $R_{0}$, of the CLC453 varies with frequency and can also affect the return loss. The return loss, shown below, takes into account an ideal transformer and the value of $R_{0}$.
Return Loss $(\mathrm{dB}) \approx-20 \log _{10}\left|n^{2} \cdot \frac{R_{0}}{Z_{0}}\right|$
The load current $\left(I_{L}\right)$ and voltage $\left(\mathrm{V}_{0}\right)$ are related to the CLC453's maximum output voltage and current by:

$$
\begin{aligned}
& \left|V_{0}\right| \leq n \cdot V_{\max } \\
& \left|I_{L}\right| \leq \frac{I_{\max }}{n}
\end{aligned}
$$

From the above current relationship, it is obvious that an amplifier with high output drive capability is required.

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## Comlinear CLC5523

## Low-Power, Variable Gain Amplifier

## General Descriptions

The Comlinear CLC5523 is a low power, wideband, DC-coupled, voltage-controlled gain amplifier. It provides a voltage-controlled gain block coupled with a current feedback output amplifier. High impedance inputs and minimum dependence of bandwidth on gain make the CLC5523 easy to use in a wide range of applications. This amplifier is suitable as a continuous gain control element in a variety of electronic systems which benefit from a wide bandwidth of 250 MHz and high slew rate of $1800 \mathrm{~V} / \mathrm{\mu s}$, with only 135 mW of power dissipation.

Input impedances in the megaohm range on both the signal and gain control inputs simplify driving the CLC5523 in any application. The CLC5523 can be configured to use pin 3 as a low impedance input making it an ideal interface for current inputs. By using the CLC5523's inverting configuration in which $R_{G}$ is driven directly, inputs which exceed the device's input voltage range may be used.

The gain control input $\left(\mathrm{V}_{\mathrm{G}}\right)$, with a 0 to 2 V input range, and a linear-in-dB gain control, simplifies the implementation of AGC circuits. The gain control circuit can adjust the gain as fast as $4 \mathrm{~dB} / \mathrm{ns}$. Maximum gains from 2 to 100 are accurately and simply set by two external resistors while attenuation of up to 80 dB from this gain can be achieved.

The extremely high slew rate of $1800 \mathrm{~V} / \mu \mathrm{s}$ and wide bandwidth provides high speed rise and fall times of $2.0 n \mathrm{n}$, with settling time for a 2 volt step of only 22 ns to $0.2 \%$. In time domain applications where linear phase is important with gain adjust, the internal current mode circuitry maintains low deviation of delay over a wide gain adjust range.

## Features

- Low power: 135 mW
- 250MHz, -3dB bandwidth
- Slew rate $1800 \mathrm{~V} / \mathrm{\mu s}$
- Gain flatness $0.2 \mathrm{~dB} @ 75 \mathrm{MHz}$
- Rise \& fall times 2.0 ns
- Low input voltage noise $4 \mathrm{nV} / \sqrt{\mathrm{Hz}}$


## Applications

- Automatic gain control
- Voltage controlled filters
- Automatic signal leveling for A/D
- Amplitude modulation
- Variable gain transimpedance



CLC5523 Electrical Characteristics ( $\mathrm{V}_{\mathrm{Cc}}= \pm 5 \mathrm{~V}, \mathrm{R}_{\mathrm{f}}=1 \mathrm{k}, \mathrm{R}_{\mathrm{g}}=100 \Omega, \mathrm{R}_{\mathrm{L}}=100 \Omega, \mathrm{~V}_{\mathrm{G}}=2 \mathrm{~V}$; unless specified)

| PARAMETERS | CONDITIONS | TYP | MIN/MAX RATINGS |  | UNITS | NOTES |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| Ambient Temperature | CLC5523I | $+25^{\circ} \mathrm{C}$ | $25^{\circ} \mathrm{C}$ | -40 to $85^{\circ} \mathrm{C}$ |  |  |
| FREQUENCY DOMAIN RESPONSE |  |  |  |  |  |  |
| -3dB bandwidth | $\mathrm{V}_{\mathrm{o}}<0.5 \mathrm{~V}_{\mathrm{pp}}$ | 250 | 150 | 125 | MHz | B |
|  | $\mathrm{V}_{0}<4.0 \mathrm{~V}_{\mathrm{pp}}$ | 100 | 45 | 35 | MHz |  |
| peaking | DC to $200 \mathrm{MHz}\left(\mathrm{V}_{\mathrm{o}}=0.5 \mathrm{~V}_{\mathrm{pp}}\right)$ | 0 | 0.8 | 2.0 | dB | B |
| rolloff | DC to $75 \mathrm{MHz}\left(\mathrm{V}_{0}=0.5 \mathrm{~V}_{\mathrm{pp}}\right)$ | 0.2 | 1.0 | 1.2 | dB | B |
| linear phase deviation | DC to $75 \mathrm{MHz}\left(\mathrm{V}_{0}=0.5 \mathrm{~V}_{\mathrm{pp}}\right)$ | 0.6 | 1.5 | 3.0 | deg |  |
| gain control bandwidth | $\mathrm{V}_{\text {in }}=0.2 \mathrm{~V}_{\mathrm{DC}}, \mathrm{V}_{\mathrm{g}}=1 \mathrm{~V}_{\mathrm{DC}}$ | 95 | 70 | 60 | MHz |  |
| TIME DOMAIN RESPONSE |  |  |  |  |  |  |
| rise and fall time | 0.5 V step | 2.0 | 2.8 | 3.0 | ns |  |
| overshoot | 0.5 V step | 6.0 | 15 | 20 | \% |  |
| settling time to 0.2\% | 2 V step | 22 | 30 | 60 | ns |  |
| non-inverting slew rate | 4 V step | 700 | 450 | 400 | V/us |  |
| inverting slew rate | 4V step | 1800 | 1000 | 700 | V/us |  |
| gain control response rate |  | 4 |  |  | $\mathrm{dB} / \mathrm{nS}$ | 1 |
| DISTORTION AND NOISE RESPONSE |  |  |  |  |  |  |
| $2^{\text {nd }}$ harmonic distortion | $1 \mathrm{~V}_{\text {pp }}, 5 \mathrm{MHz}$ | -65 | - | - | dBc |  |
| $3^{\text {rd }}$ harmonic distortion | $1 \mathrm{~V}_{\mathrm{pp}}, 5 \mathrm{MHz}$ | -80 | - | - | dBc |  |
| $2^{\text {nd }}$ harmonic distortion | $1 \mathrm{~V}_{\mathrm{pp}}, 10 \mathrm{MHz}$ | -57 | -52 | -40 | dBc | B |
| $3^{\text {rd }}$ harmonic distortion | $1 \mathrm{~V}_{\mathrm{pp}}, 10 \mathrm{MHz}$ | -75 | -58 | -54 | dBc | B |
| input referred total noise | $\mathrm{V}_{\mathrm{g}}=2 \mathrm{~V}$ | 5 | 6 | 7 | $\mathrm{nV} / \mathrm{VHz}$ |  |
| input referred voltage noise |  | 4 | 5.5 | 5.5 | $\mathrm{nV} / \mathrm{VHz}$ |  |
| $\mathrm{R}_{\mathrm{g}}$ referred current noise |  | 36 | 50 | 60 | $\mathrm{pA} / \sqrt{ } \mathrm{Hz}$ |  |
| STATIC DC PERFORMANCE |  |  |  |  |  |  |
| output offset voltage |  | 50 | 120 | 150 | mV | A |
| $V_{\text {in }}$ signal input |  |  |  |  |  |  |
| input voltage range | $\mathrm{R}_{\mathrm{g}}$ open | $\pm 3.8$ | $\pm 3.6$ | $\pm 3.3$ | V |  |
| input bias current |  | 3.0 | 8.0 | 16 | $\mu \mathrm{A}$ | A |
| input resistance |  | 3.0 | 1.0 | 0.8 | $\mathrm{M} \Omega$ |  |
| input capacitance |  | 1.0 | 1.5 | 1.7 | pF |  |
| $\mathrm{I}_{\text {Rgmax }}$ | $0^{\circ}$ to $70^{\circ} \mathrm{C}$ | 7.0 | 5.0 | 4.0 | mA |  |
| $\mathrm{I}_{\text {Rgmax }}$ | $-40^{\circ}$ to $85^{\circ} \mathrm{C}$ | 7.0 | 5.0 | 2.5 | mA |  |
| signal ch. non-linearity | $\mathrm{V}_{\mathrm{o}}=2 \mathrm{~V}_{\mathrm{pp}}$ | 0.04 | 0.1 | 0.2 | \% | B |
| gain accuracy* |  | 0.3 | 0.5 | 0.9 | dB | A |
| $\mathrm{V}_{\mathrm{g}}$ gain input |  |  |  |  |  |  |
| input bias current |  | 0.5 | 2.0 | 4.0 | $\mu \mathrm{A}$ |  |
| input resistance |  | 10 | 2.0 | 2.0 | $\mathrm{M} \Omega$ |  |
| input capacitance |  | 1.0 | 1.5 | 1.5 | pF |  |
| ground pin current |  | 40 | 55 | 65 | $\mu \mathrm{A}$ |  |
| power supply rejection ratio | input-referred | 57 | 52 | 48 | dB | B |
| supply current | $\mathrm{R}_{\mathrm{L}}=\infty$ | 13.5 | 15 | 16 | mA | A |
| output voltage range | no load | $\pm 3.4$ | $\pm 3.3$ | $\pm 2.3$ | V |  |
| output voltage range | $\mathrm{R}_{\mathrm{L}}=100 \Omega$ | $\pm 3.0$ | $\pm 2.8$ | $\pm 2.3$ | V |  |
| output impedance |  | 0.1 | 0.15 | 0.15 | $\Omega$ |  |
| output current |  | 80 | 65 | 50 | mA |  |
| transistor count |  | 146 |  |  |  |  |

*maximum gain is defined as $R_{f} / R_{g}$
$\mathrm{Min} / \mathrm{max}$ ratings are based on product characterization and simulation. Individual parameters are tested as noted. Outgoing quality levels are determined from tested parameters.

## Notes

A) I-level: spec is $100 \%$ tested at $+25^{\circ} \mathrm{C}$, sample tested at $+85^{\circ} \mathrm{C}$.
B) I-level: spec is sample tested at $+25^{\circ} \mathrm{C}$.

1) See plot "Gain Control Settling Time".

## Absolute Maximum Ratings

| supply voltage | $\pm 7 \mathrm{~V}$ |
| :--- | ---: |
| output current | $\pm 96 \mathrm{~mA}$ |
| maximum junction temperature | $+175^{\circ} \mathrm{C}$ |
| storage temperature range | $-65^{\circ} \mathrm{C}$ to $+150^{\circ} \mathrm{C}$ |
| lead temperature (soldering 10 sec ) | $+300^{\circ} \mathrm{C}$ |
| ESD rating (human body model) | TBD |

## CLC5523 Typical Performance ( $\mathrm{V}_{\mathrm{G}}=+2 \mathrm{~V}, \mathrm{R}_{\mathrm{f}}=1 \mathrm{k} \Omega, \mathrm{R}_{\mathrm{g}}=100 \Omega, \mathrm{R}_{\mathrm{L}}=100 \Omega, \mathrm{~V}_{\mathrm{o}}=0.5 \mathrm{~V}_{\text {pp }}$; unless specified)



Frequency Response vs. $\mathbf{R}_{\mathrm{L}}$


Frequency Response vs. $\mathbf{R}_{\mathbf{g}}$


Frequency Response vs. $\mathbf{R}_{\boldsymbol{f}}$


Frequency (MHz)
Feed-Through Isolation $\left(\mathrm{V}_{\mathrm{G}}=\mathbf{0}, 2\right)$






## CLC5523 Typical Performance ( $\mathrm{V}_{\mathrm{G}}=+2 \mathrm{~V}, \mathrm{R}_{\mathrm{f}}=1 \mathrm{k} \Omega, \mathrm{R}_{\mathrm{g}}=100 \Omega, \mathrm{~A}_{\mathrm{vmax}}=10$; unless specified)



The key features of the CLC5523 are:

- Low Power
- Broad voltage controlled gain and attenuation range
- Bandwidth independent, resistor programmable gain range
- Broad signal and gain control bandwidths
- Frequency response may be adjusted with $R_{f}$
- High Impedance signal and gain control Inputs

The CLC5523 combines a closed loop input buffer, a voltage controlled variable gain cell and an output amplifier. The input buffer is a transconductance stage whose gain is set by the gain setting resistor, $\mathrm{R}_{\mathrm{g}}$. The output amplifier is a current feedback op amp and is configured as a transimpedance stage whose gain is set by, and equal to, the feedback resistor, $R_{f}$. The maximum gain, $A_{v m a x}$, of the CLC5523 is defined by the ratio; $R_{f} / R_{g}$. As the gain control input $\left(\mathrm{V}_{\mathrm{G}}\right)$ is adjusted over its 0 to 2 V range, the gain is adjusted over a range of 80 dB relative to the maximum set gain.

## Setting the CLC5523 Maximum Gain

$$
A_{v \max }=\frac{R_{f}}{R_{g}}
$$

Although the CLC5523 is specified at $A_{\text {vmax }}=10$, the recommended $A_{\text {vax }}$ varies between 2 and 100. Higher gains are possible but usually impractical due to output offsets, noise and distortion. When varying $\mathrm{A}_{\text {vmax }}$ several tradeoffs are made:
$\mathrm{R}_{\mathrm{g}}$ : determines the input voltage range
$R_{f}$ : determines overall bandwidth
The amount of current which the input buffer can source into $R_{g}$ is limited and is specified in the $\mathrm{I}_{\mathrm{R}_{\mathrm{g}} \max }$ spec. This sets the maximum input voltage:

$$
V_{\text {in }}(\max )=I_{R_{g} \max } \cdot R_{g}
$$

The effects of maximum input range on harmonic distortion are illustrated in the Input Harmonic Distortion plot. Variations in $R_{g}$ will also have an effect on the small signal bandwidth due to its loading of the input buffer and can be seen in Frequency Response vs. $R_{g}$. Changes in $R_{f}$ will have a more dramatic effect on the small signal bandwidth. The output amplifier of the CLC5523 is a current feedback amplifier(CFA) and its bandwidth is determined by $\mathrm{R}_{\mathrm{f}}$. As with any CFA, doubling the feedback resistor will roughly cut the bandwidth of the device in half (refer to the plot Frequency Response vs. $R_{f}$ ). For more information covering CFA's, there is a basic tutorial, OA-20, Current Feedback Myths Debunked or a more rigorous analysis, OA-13, Current Feedback Amplifier Loop Gain Analysis and Performance Enhancements.

## Using the CLC5523 in AGC Applications

In AGC applications, the control loop forces the CLC5523 to have a fixed output amplitude. The input amplitude will vary over a wide range and this can be the issue that limits dynamic range. At high input amplitudes, the distortion due to the input buffer driving $\mathrm{R}_{\mathrm{g}}$ may exceed that which is produced by the output amplifier driving the load. In the plot, Harmonic Distortion vs. Gain, second and third harmonic distortion are plotted over a gain range of nearly 40 dB for a fixed output amplitude of $100 \mathrm{mV} \mathrm{V}_{\mathrm{pp}}$ in the specified configuration, $\mathrm{R}_{\mathrm{f}}=1 \mathrm{k}$, $R_{g}=100 \Omega$. When the gain is adjusted to 0.1 (i.e. 40 dB down from $\mathrm{A}_{\mathrm{vmax}}$ ), the input amplitude would be $1 \mathrm{~V}_{\mathrm{pp}}$ and we can see the distortion is at its worst at this gain. If the output amplitude of the AGC were to be raised above 100 mV , the input amplitudes for gains 40 dB down from $\mathrm{A}_{\mathrm{vmax}}$ would be even higher and the distortion would degrade further. It is for this reason that we recommend lower output amplitudes if wide gain ranges are desired. Using a post-amp like the CLC404 or CLC409 would be the best way to preserve dynamic range and yield output amplitudes much higher than $100 \mathrm{mV} \mathrm{V}_{\mathrm{p}}$.

Another way of addressing distortion performance and its limitations on dynamic range, would be to raise the value of $\mathrm{R}_{\mathrm{g}}$. Just like any other high-speed amplifier, by increasing the load resistance, and therefore decreasing the demanded load current, the distortion performance will be improved in most cases. With an increased $R_{g}, R_{f}$ will also have to be increased to keep the same $A_{v m a x}$ and this will decrease the overall bandwidth.

## Gain Partitioning

If high levels of gain are needed, gain partitioning should be considered.


Figure 1: Gain Partitioning
The maximum gain range for this circuit is given by the following equation:
maximum gain $=\left(1+\frac{R_{2}}{R_{1}}\right) \cdot\left(\frac{R_{f}}{R_{g}}\right)$

The CLC425 is a low noise wideband voltage feedback amplifier. Setting R2 at $909 \Omega$ and R1 at $100 \Omega$ produces a gain of 20 dB . Setting $R_{f}$ at $1000 \Omega$ as recommended and $R_{g}$ at $50 \Omega$, produces a gain of 26 dB in the CLC5523. The total gain of this circuit is therefore approximately 46 dB . It is important to understand that when partitioning to obtain high levels of gain, very small signal levels will drive the amplifiers to full scale output. For example, with 46 dB of gain, a 20 mV signal at the input will drive the output of the CLC425 to 200 mV , the output of the CLC5523 to 4 V . Accordingly, the designer must carefully consider the contributions of each stage to the overall characteristics. Through gain partitioning the designer is provided with an opportunity to optimize the frequency response, noise, distortion, settling time, and loading effects of each amplifier to achieve improved overall performance.

## CLC5523 Gain Control Range and Minimum Gain

Before discussing Gain Control Range, it is important to understand the issues which limit it. The minimum gain of the CLC5523, theoretically, is zero, but in practical circuits is limited by the amount of feedthrough, here defined as the difference in output levels when $V_{G}=2 \mathrm{~V}$ and when $\mathrm{V}_{\mathrm{G}}=0 \mathrm{~V}$. Capacitive coupling through the board and package as well as coupling through the supplies will determine the amount of feedthrough. Even at DC, the input signal will not be completely rejected. At high frequencies feedthrough will get worse because of its capacitive nature. At low frequencies, the feedthrough will be 80 dB below the maximum gain, and therefore it can be said that the CLC5523 has an 80dB Gain Control Range.

## CLC5523 Gain Control Function

In the two plots, Gain vs. $V_{G}$, we can see the gain as a function of the control voltage. The first plot, sometimes referred to as the S-curve, is the linear (V/V) gain. This is a hyperbolic tangent relationship. The second gain curve plots the gain in dB and is linear over a wide range of gains. Because of this, the CLC5523 gain control is referred to as "linear-in-dB."

For applications where the CLC5523 will be used at the heart of a closed loop AGC circuit, the S-curve control characteristic provides a broad linear (in dB) control range with soft limiting at the highest gains where large changes in control voltage result in small changes in gain. For applications, requiring a fully linear (in dB ) control characteristic, use the CLC5523 at half gain and below $\left(\mathrm{V}_{\mathrm{G}} \leq 1 \mathrm{~V}\right)$.

## Avoiding Overdrive of the CLC5523 <br> Gain Control Input

There is an additional requirement for the CLC5523 Gain Control Input $\left(\mathrm{V}_{\mathrm{G}}\right)$ : $\mathrm{V}_{\mathrm{G}}$ must not exceed +2.5 V . The gain control circuitry may saturate and the gain may actually be reduced. In applications where $\mathrm{V}_{\mathrm{G}}$ is being driven from a DAC, this can easily be addressed in the software. If there is a linear loop driving $V_{G}$, such as an AGC loop,
other methods of limiting the input voltage should be implemented. One simple solution is to place a $2: 1$ resistive divider on the $\mathrm{V}_{\mathrm{G}}$ input. If the device driving this divider is operating off of $\pm 5 \mathrm{~V}$ supplies as well, its output will not exceed 5 V and through the divider $\mathrm{V}_{\mathrm{G}}$ can not exceed 2.5 V .

## Improving the CLC5523 Large Signal Performance

Figure 2 illustrates an inverting gain scheme for the CLC5523.


Figure 2: Inverting the CLC5523
The input signal is applied through the $\mathrm{R}_{\mathrm{g}}$ resistor. The $V_{\text {in }}$ pin should be grounded through a $25 \Omega$ resistor. The maximum gain range of this configuration is given in the following equation:

$$
A_{v \max }=-\left(\frac{R_{f}}{R_{g}}\right)
$$

The inverting slew rate of the CLC5523 is much higher than that of the non-inverting slew rate. This 2.5 X performance improvement comes about because in the non-inverting configuration, the slew rate of the overall amplifier is limited by the input buffer. In the inverting circuit, the input buffer remains at a fixed voltage and does not affect slew rate.

## Transmission Line Matching

One method for matching the characteristic impedance of a transmission line is to place the appropriate resistor at the input or output of the amplifier. Figure 3 shows a typical circuit configuration for matching transmission lines.


Figure 3: Transmission Line Matching
The resistors $R_{s}, R_{i}, R_{0}$, and $R_{T}$ are equal to the characteristic impedance, $Z_{0}$, of the transmission line or cable. Use $\mathrm{C}_{0}$ to match the output transmission line over a greater frequency range. It compensates for the increase of the op amp's output impedance with frequency.

## Minimizing Parasitic Effects on Small Signal Bandwidth

The best way to minimize parasitic effects is to use the small outline package and surface mount components. For designs utilizing through-hole components, specifically axial resistors, resistor self-capacitance should be considered. Example: the average magnitude of parasitic capacitance of RN55D 1\% metal film resistors is about 0.15 pF with variations of as much as 0.1 pF between lots. Given the CLC5523's extended bandwidth, these small parasitic reactance variations can cause measurable frequency response variations in the highest octave. We therefore recommend the use of surface mount resistors to minimize these parasitic reactance effects. If an axial component is preferred, we recommend PRP8351 resistors which are available from Precision Resistive Products, Inc., Highway 61 South, Mediapolis, Iowa.

## Small Signal Response at Low A vmax

When the maximum gain, as set by $R_{g}$ and $R_{f}$, is greater than or equal to $A_{\text {max }}=10$, little or no peaking should be observed in the amplifier response. When the gain range is set to less than $A_{v m a x}=10$, some peaking may be observed at higher frequencies. At gain ranges of $2 \leq \mathrm{A}_{\mathrm{vmax}} \leq 10$ peaking can be minimized by increasing $\mathrm{R}_{\mathrm{f}}$. At gain ranges of $\mathrm{A}_{\mathrm{vmax}}<2$ peaking reaches approximately 6 dB in the upper octave.

If peaking is observed with the recommended $R_{f}$ resistor, and a small increase in the $R_{f}$ resistor does not solve the problem, then investigate the possible causes and remedies listed below.

[^2]Keep these traces as short as possible

- Long traces between CLC5523 and $0.1 \mu \mathrm{~F}$ bypass capacitors
- Keep these traces less than 0.2 inches ( 5 mm )
- For the devices in the PDIP package, an additional 1000 pF monolithic capacitor should be placed less than $0.1^{\prime \prime}(3 \mathrm{~mm})$ from the pin
- Extra capacitance between the $\mathbf{R}_{\mathbf{g}}$ pin and ground ( $\mathrm{C}_{\mathrm{G}}$ )
- See the Printed Circuit Board Layout sub-section below for suggestions on reducing $\mathrm{C}_{\mathrm{G}}$
- Increase $\mathrm{R}_{\mathrm{f}}$ if peaking is still observed after reducing $\mathrm{C}_{\mathrm{G}}$
- Non-inverting input pin connected directly to ground
- Place a 50 to $200 \Omega$ resistor between the noninverting pin and ground


## Adjusting Offsets and DC Level Shifting

Offsets can be broken into two parts: an input-referred term and an output-referred term. These errors can be trimmed using the circuit in Figure 4. First set $\mathrm{V}_{\mathrm{G}}$ to OV and adjust the trim pot R4 to null the offset voltage at the output. This will eliminate the output stage offsets. Next set $\mathrm{V}_{\mathrm{G}}$ to 2 V and adjust the trim pot R1 to null the offset voltage at the output. This will eliminate the input stage offsets.


Figure 4: Offset Adjust Circuit

## Printed Circuit Board Layout

High frequency op amp performance is strongly dependent on proper layout, proper resistive termination and adequate power supply decoupling. The most important layout points to follow are:

- Use a ground plane
- Bypass each power supply pin with these capacitors:
- a high-quality $0.1 \mu \mathrm{~F}$ ceramic capacitor placed less than $0.2^{\prime \prime}(5 \mathrm{~mm})$ from the pin
- a $6.8 \mu \mathrm{~F}$ tantalum capacitor less than $2^{\prime \prime}(50 \mathrm{~mm})$ from the pin
- for the plastic DIP package, a high-quality 1000 pF ceramic capacitor placed less than 0.1 " ( 3 mm ) from the pin
Capacitively bypassing power pins to a good ground plane with a minimum of trace length (inductance) is necessary for any high speed device, but it is particularly important for the CLC5523.
- Establish wide, low impedance, power supply traces
- For the plastic DIP package, a $25 \Omega$ resistor should be connected from pin 4 to ground with a minimum length trace
- Minimize or eliminate sources of capacitance between the $R_{f}$ pin and the output pin. Avoid adjacent feedthrough vias between the $R_{f}$ and output leads since such a geometry may give rise to a significant source of capacitance.
- Minimize trace and lead lengths for components between the inverting and output pins
- Remove ground plane 0.1 " ( 3 mm ) from all input/output pads
- For prototyping, use flush-mount printed circuit board pins; never use high profile DIP sockets

To minimize high frequency distortion, other layout issues need be addressed:

- Short, equal length, low impedance power supply return paths from the load to the supplies
- avoid returning output ground currents near the input stage.


## Evaluation Boards

Evaluation boards are available for both the 8 -pin DIP and small outline package types. Evaluation kits that contain an evaluation board and CLC5523 samples can be obtained by calling National Semiconductor's Customer Service Center at 1-800-272-9959. The 8-pin DIP evaluation kit part number is CLC73065. The 8-pin small outline evaluation kit part number is CLC730066.

The DIP evaluation kit has been designed to utilize axial lead components. The small outline evaluation kit has been designed to utilize surface mount components.

The circuit diagram shown in Figure 5, applies to both the DIP and the small outline evaluation boards.


* $25 \Omega$ series resistor is not required on the small outline device and does not appear on the small outline board

Figure 5: Evaluation Board Schematic

Comlinear Layer1


Figure 6: DIP Evaluation Board (Top Layer)

Comlinear Layer2


Figure 7: DIP Evaluation Board (Bottom Layer)

Comlinear Layer1 Silk


Figure 8: Small Outline Evaluation Board (Top Layer)

Comlinear Layer2 Silk


Figure 9: Small Outline Evaluation Board (Bottom Layer)
(Not drawn to scale)

## Digital Gain Control

Digitally variable gain control can be easily realized by driving the CLC5523's gain control input with a digital-to-analog converter (DAC). Figure 10 illustrates such an application. This circuit employs National Semiconductor's eight-bit DAC0830, the LM351 JFET input op-amp, and the CLC5523 VGA. With $V_{\text {ref }}$ set to 2 V , the circuit provides up to 80 dB of gain control in 512 steps with up to $0.05 \%$ full scale resolution. The maximum gain of this circuit is 20 dB .


Figure 10: Digital Gain Control

## Automatic Gain Control (AGC) \#1

## Fast Response AGC Loop

The AGC circuit shown in Figure 11 will correct a 6 dB input amplitude step in 100 ns. The circuit includes a two op-amp precision rectifier amplitude detector (U1 and U 2 ), and an integrator (U3) to provide high loop gain at low frequencies. The output amplitude is set by R9.

Some notes on building fast AGC loops:
Precision rectifiers work best with large output signals. Accuracy is improved by blocking DC offsets, as shown in Figure 11.

Signal frequencies must not reach the gain control port of the CLC5523, or the output signal will be distorted (modulated by itself). A fast settling AGC needs additional filtering beyond the integrator stage to block signal frequencies. This is provided in Figure 11 by a simple R-C filter (R10 and C3); better distortion performance can be achieved with a more complex filter. These filters should be scaled with the input signal frequency. Loops with slower response time (longer integration time constants) may not need the R10 C3 filter.

Checking the loop stability can be done by monitoring the $\mathrm{V}_{\mathrm{g}}$ voltage while applying a step change in input signal amplitude. Changing the input signal amplitude can be easily done with either an arbitrary waveform generator or a fast multiplexer such as the CLC532.

## Automatic Gain Control (AGC) \#2

Figure 12 on the following page, illustrates an automatic gain control circuit that employs two CLC5523's. In this circuit, U1 receives the input signal and produces an output signal of constant amplitude. U2 is configured to provide negative feedback. U2 generates a rectified gain control signal that works against an adjustable bias level which may be set by the potentiometer and $R_{b} . \quad C_{i}$ integrates the bias and negative feedback. The resultant gain control signal is applied to the U1 gain control input $\mathrm{V}_{\mathrm{g}}$. The bias adjustment allows the U 1 output to be set at an arbitrary level less than the maximum output specification of the amplifier. Rectification is accomplished in U2 by driving both the amplifier input and the gain control input with the U1 output signal. The voltage divider that is formed by $\mathrm{R} 1, \mathrm{R} 2$ and the $\mathrm{V}_{\mathrm{g}}$ input (pin 1) resistance, sets the rectifier gain.


Figure 11: Automatic Gain Control Circuit \#1


Figure 12: Automatic Gain Control Circuit \#2

## Customer Design Applications Support

National Semiconductor is committed to design excellence. For sales, literature and technical support, call the National Semiconductor Customer Response Group at 1-800-272-9959 or fax 1-800-737-7018.

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## Comlinear CLC5602 Dual, High Output, Video Amplifier

## General Description

The Comlinear CLC5602 has a new output stage that delivers high output drive current ( 130 mA ), but consumes minimal quiescent supply current ( 1.6 mA ) from a single 5 V supply. Its current feedback architecture, fabricated in an advanced complementary bipolar process, maintains consistent performance over a wide range of gains and signal levels, and has a linear-phase response up to one half of the -3 dB frequency.

The CLC5602 offers superior dynamic performance with a 135 MHz small-signal bandwidth, $300 \mathrm{~V} / \mu \mathrm{s}$ slew rate and 5.7 ns rise/fall times $\left(2 \mathrm{~V}_{\text {step }}\right)$. The combination of low quiescent power, high output current drive, and high-speed performance make the CLC5602 well suited for many battery-powered personal communication/computing systems.

The ability to drive low-impedance, highly capacitive loads, makes the CLC5602 ideal for single ended cable applications. It also drives low impedance loads with minimum distortion. The CLC5602 will drive a $100 \Omega$ load with only $-86 /-85 \mathrm{dBc}$ second/third harmonic distortion ( $\mathrm{A}_{\mathrm{v}}=+2, \mathrm{~V}_{\text {out }}=2 \mathrm{~V}_{\mathrm{pp}}, \mathrm{f}=1 \mathrm{MHz}$ ). With a $25 \Omega$ load, and the same conditions, it produces only -86/ -72 dBc second/third harmonic distortion. It is also optimized for driving high currents into single-ended transformers and coils.

When driving the input of high-resolution $A / D$ converters, the CLC5602 provides excellent -87/-95dBc second/third harmonic distortion ( $\mathrm{A}_{\mathrm{V}}=+2, \mathrm{~V}_{\mathrm{out}}=2 \mathrm{~V}_{\mathrm{pp}}, \mathrm{f}=1 \mathrm{MHz}, \mathrm{R}_{\mathrm{L}}=1 \mathrm{k} \Omega$ ) and fast settling time.

The CLC5602 offers 0.1 dB gain flatness to 20 MHz and differential gain and phase errors of $0.06 \%$ and $0.02^{\circ}$. These features are ideal for professional and consumer video applications.

## Features

- 130 mA output current

■ $0.06 \%, 0.02^{\circ}$ differntial gain, phase
■ 1.6 mA supply current

- 135 MHz bandwidth $\left(\mathrm{A}_{\mathrm{v}}=+2\right)$

■ -87/-95dBc HD2/HD3 (1MHz)

- 15ns settling to $0.05 \%$

■ 300V/ $\mu$ s slew rate
■ Stable for capacitive loads up to 1000pf

- Single 5 V to $\pm 5 \mathrm{~V}$ supplies


## Applications

- Video line driver
- Coaxial cable driver
- Twisted pair driver
- Transformer/Coil Driver
- High capacitive load driver
- Portable/battery-powered applications
- A/D driver




## Comlinear CLC5612 <br> Dual, High Output, Video Programmable Gain Buffer

## General Description

The Comlinear CLC5612 has a new output stage that delivers high output drive current ( 130 mA ), but consumes minimal quiescent supply current ( 1.6 mA ) from a single 5 V supply. Its current feedback architecture, fabricated in an advanced complementary bipolar process, maintains consistent performance over a wide range of gains and signal levels, and has a linear-phase response up to one half of the -3 dB frequency.

The CLC5612 offers superior dynamic performance with a 90 MHz small-signal bandwidth, $290 \mathrm{~V} / \mu \mathrm{s}$ slew rate and 6.2 ns rise/fall times $\left(2 \mathrm{~V}_{\text {step }}\right)$. The combination of low quiescent power, high output current drive, and high-speed performance make the CLC5612 well suited for many battery-powered personal communication/computing systems.

The ability to drive low-impedance, highly capacitive loads, makes the CLC5612 ideal for single ended cable applications. It also drives low impedance loads with minimum distortion. The CLC5612 will drive a $100 \Omega$ load with only $-74 /-86 \mathrm{dBc}$ second/third harmonic distortion ( $\mathrm{A}_{\mathrm{v}}=+2, \mathrm{~V}_{\text {out }}=2 \mathrm{~V}_{\mathrm{pp}}, \mathrm{f}=1 \mathrm{MHz}$ ). With a $25 \Omega$ load, and the same conditions, it produces only $-70 /$ -67 dBc second/third harmonic distortion. It is also optimized for driving high currents into single-ended transformers and coils.

When driving the input of high-resolution $A / D$ converters, the CLC5612 provides excellent -87/-93dBc second/third harmonic distortion ( $\mathrm{A}_{\mathrm{V}}=+2, \mathrm{~V}_{\mathrm{out}}=2 \mathrm{~V}_{\mathrm{pp}}, \mathrm{f}=1 \mathrm{MHz}, \mathrm{R}_{\mathrm{L}}=1 \mathrm{k} \Omega$ ) and fast settling time.

The CLC5612 offers 0.1 dB gain flatness to 17 MHz and differential gain and phase errors of $0.15 \%$ and $0.02^{\circ}$. These features are ideal for professional and consumer video applications.

## Features

- 130mA output current

■ $0.15 \%, 0.02^{\circ}$ differntial gain, phase
■ 1.6 mA supply current
■ 90MHz bandwidth $\left(\mathrm{A}_{\mathrm{v}}=+2\right)$
■ -87/-93dBc HD2/HD3 (1MHz)

- 17 ns settling to $0.05 \%$
- 290V/ $\mu$ s slew rate

■ Stable for capacitive loads up to 1000pf

- Single 5 V to $\pm 5 \mathrm{~V}$ supplies


## Applications

- Video line driver
- Coaxial cable driver
- Twisted pair driver
- Transformer/Coil Driver
- High capacitive load driver

■ Portable/battery-powered applications

- A/D driver



## Typical Application Single Supply Cable Driver



NOTE: Channel 2 not shown

Pinout DIP \& SOIC



## Comlinear CLC5622 Dual, High Output, Video Amplifier

## General Description

The Comlinear CLC5622 has a new output stage that delivers high output drive current ( 130 mA ), but consumes minimal quiescent supply current ( 3.2 mA ) from a single 5 V supply. Its current feedback architecture, fabricated in an advanced complementary bipolar process, maintains consistent performance over a wide range of gains and signal levels, and has a linear-phase response up to one half of the -3 dB frequency.

The CLC5622 offers superior dynamic performance with a 160 MHz small-signal bandwidth, $370 \mathrm{~V} / \mu \mathrm{s}$ slew rate and 4.4 ns rise/fall times $\left(2 \mathrm{~V}_{\text {step }}\right)$. The combination of low quiescent power, high output current drive, and high-speed performance make the CLC5622 well suited for many battery-powered personal communication/computing systems.

The ability to drive low-impedance, highly capacitive loads, makes the CLC5622 ideal for single ended cable applications. It also drives low impedance loads with minimum distortion. The CLC5622 will drive a $100 \Omega$ load with only $-95 /-95 d B c$ second/third harmonic distortion ( $\mathrm{A}_{\mathrm{v}}=+2, \mathrm{~V}_{\text {out }}=2 \mathrm{~V}_{\mathrm{pp}}, \mathrm{f}=1 \mathrm{MHz}$ ). With a $25 \Omega$ load, and the same conditions, it produces only -72 / -77 dBc second/third harmonic distortion. It is also optimized for driving high currents into single-ended transformers and coils.

When driving the input of high-resolution $A / D$ converters, the CLC5622 provides excellent -90/-97dBc second/third harmonic distortion ( $\mathrm{A}_{\mathrm{V}}=+2, \mathrm{~V}_{\mathrm{out}}=2 \mathrm{~V}_{\mathrm{pp}}, \mathrm{f}=1 \mathrm{MHz}, \mathrm{R}_{\mathrm{L}}=1 \mathrm{k} \Omega$ ) and fast settling time.

The CLC5622 offers 0.1 dB gain flatness to 30 MHz and differential gain and phase errors of $0.05 \%$ and $0.03^{\circ}$. These features are ideal for professional and consumer video applications.

## Features

- 130 mA output current

■ $0.05 \%, 0.03^{\circ}$ differntial gain, phase
■ 3.2 mA supply current

- 160MHz bandwidth $\left(\mathrm{A}_{\mathrm{v}}=+2\right)$

■ -90/-97dBc HD2/HD3 (1MHz)

- 18ns settling to $0.05 \%$
- 370V/ $\mu$ s slew rate

■ Stable for capacitive loads up to 1000pf

- Single 5 V to $\pm 5 \mathrm{~V}$ supplies


## Applications

- Video line driver
- Coaxial cable driver
- Twisted pair driver
- Transformer/Coil Driver
- High capacitive load driver
- Portable/battery-powered applications
- A/D driver




## Comlinear CLC5623 <br> Triple, High Output, Video Amplifier

## General Description

The Comlinear CLC5623 has a new output stage that delivers high output drive current ( 130 mA ), but consumes minimal quiescent supply current ( 3.2 mA ) from a single 5 V supply. Its current feedback architecture, fabricated in an advanced complementary bipolar process, maintains consistent performance over a wide range of gains and signal levels, and has a linear-phase response up to one half of the -3 dB frequency.

The CLC5623 offers superior dynamic performance with a 160 MHz small-signal bandwidth, $370 \mathrm{~V} / \mu \mathrm{s}$ slew rate and 4.4 ns rise/fall times $\left(2 \mathrm{~V}_{\text {step }}\right)$. The combination of low quiescent power, high output current drive, and high-speed performance make the CLC5623 well suited for many battery-powered personal communication/computing systems.

The ability to drive low-impedance, highly capacitive loads, makes the CLC5623 ideal for single ended cable applications. It also drives low impedance loads with minimum distortion. The CLC5623 will drive a $100 \Omega$ load with only $-95 /-95 d B c$ second/third harmonic distortion ( $\mathrm{A}_{\mathrm{v}}=+2, \mathrm{~V}_{\text {out }}=2 \mathrm{~V}_{\mathrm{pp}}, \mathrm{f}=1 \mathrm{MHz}$ ). With a $25 \Omega$ load, and the same conditions, it produces only -72 / -77 dBc second/third harmonic distortion. It is also optimized for driving high currents into single-ended transformers and coils.

When driving the input of high-resolution $A / D$ converters, the CLC5623 provides excellent -90/-97dBc second/third harmonic distortion ( $\mathrm{A}_{\mathrm{V}}=+2, \mathrm{~V}_{\mathrm{out}}=2 \mathrm{~V}_{\mathrm{pp}}, \mathrm{f}=1 \mathrm{MHz}, \mathrm{R}_{\mathrm{L}}=1 \mathrm{k} \Omega$ ) and fast settling time.

The CLC5623 offers 0.1 dB gain flatness to 30 MHz and differential gain and phase errors of $0.05 \%$ and $0.03^{\circ}$. These features are ideal for professional and consumer video applications.

## Features

- 130 mA output current

■ $0.05 \%, 0.03^{\circ}$ differntial gain, phase
■ 3.2 mA supply current

- 160MHz bandwidth $\left(\mathrm{A}_{\mathrm{v}}=+2\right)$

■ -90/-97dBc HD2/HD3 (1MHz)

- 18ns settling to $0.05 \%$
- 370V/ $\mu$ s slew rate

■ Stable for capacitive loads up to 1000pf

- Single 5 V to $\pm 5 \mathrm{~V}$ supplies


## Applications

- Video line driver
- Coaxial cable driver
- Twisted pair driver
- Transformer/Coil Driver
- High capacitive load driver
- Portable/battery-powered applications
- A/D driver




## Comlinear CLC5632

## Dual, High Output, Video Programmable Gain Buffer

## General Description

The Comlinear CLC5632 has a new output stage that delivers high output drive current ( 130 mA ), but consumes minimal quiescent supply current ( 3.2 mA ) from a single 5 V supply. Its current feedback architecture, fabricated in an advanced complementary bipolar process, maintains consistent performance over a wide range of gains and signal levels, and has a linear-phase response up to one half of the -3 dB frequency.

The CLC5632 offers superior dynamic performance with a 130 MHz small-signal bandwidth, $410 \mathrm{~V} / \mathrm{ms}$ slew rate and 5.0 ns rise/fall times $\left(2 \mathrm{~V}_{\text {step }}\right)$. The combination of low quiescent power, high output current drive, and high-speed performance make the CLC5632 well suited for many battery-powered personal communication/computing systems.

The ability to drive low-impedance, highly capacitive loads, makes the CLC5632 ideal for single ended cable applications. It also drives low impedance loads with minimum distortion. The CLC5632 will drive a $100 \Omega$ load with only $-82 /-69 \mathrm{dBc}$ second/third harmonic distortion ( $A_{v}=+2, \mathrm{~V}_{\text {out }}=2 \mathrm{~V}_{\mathrm{pp}}, \mathrm{f}=1 \mathrm{MHz}$ ). With a $25 \Omega$ load, and the same conditions, it produces only -71/ -73 dBc second/third harmonic distortion. It is also optimized for driving high currents into single-ended transformers and coils.

When driving the input of high-resolution $A / D$ converters, the CLC5632 provides excellent -86/-96dBc second/third harmonic distortion ( $\mathrm{A}_{\mathrm{V}}=+2, \mathrm{~V}_{\mathrm{out}}=2 \mathrm{~V}_{\mathrm{pp}}, \mathrm{f}=1 \mathrm{MHz}, \mathrm{R}_{\mathrm{L}}=1 \mathrm{k} \Omega$ ) and fast settling time.

The CLC5632 offers 0.1 dB gain flatness to 30 MHz and differential gain and phase errors of $0.08 \%$ and $0.02^{\circ}$. These features are ideal for professional and consumer video applications.

## Features

- 130mA output current
- $0.08 \%, 0.02^{\circ}$ differntial gain, phase
- 3.2 mA supply current
- 130 MHz bandwidth $\left(\mathrm{A}_{\mathrm{v}}=+2\right)$
- -86/-96dBc HD2/HD3 (1MHz)
- 17 ns settling to $0.05 \%$
- $410 \mathrm{~V} / \mathrm{\mu s}$ slew rate
- Stable for capacitive loads up to 1000pf
- Single 5 V to $\pm 5 \mathrm{~V}$ supplies


## Applications

- Video line driver
- Coaxial cable driver
- Twisted pair driver
- Transformer/Coil Driver
- High capacitive load driver
- Portable/battery-powered applications
- A/D driver



## Typical Application Single Supply Cable Driver



NOTE: Channel 2 not shown

Pinout DIP \& SOIC



## Comlinear CLC5633 <br> Triple, High Output, Video Programmable Gain Buffer

## General Description

The Comlinear CLC5633 has a new output stage that delivers high output drive current ( 130 mA ), but consumes minimal quiescent supply current ( 3.2 mA ) from a single 5 V supply. Its current feedback architecture, fabricated in an advanced complementary bipolar process, maintains consistent performance over a wide range of gains and signal levels, and has a linear-phase response up to one half of the -3 dB frequency.

The CLC5633 offers superior dynamic performance with a 130 MHz small-signal bandwidth, $410 \mathrm{~V} / \mathrm{ms}$ slew rate and 5.0 ns rise/fall times $\left(2 \mathrm{~V}_{\text {step }}\right)$. The combination of low quiescent power, high output current drive, and high-speed performance make the CLC5633 well suited for many battery-powered personal communication/computing systems.

The ability to drive low-impedance, highly capacitive loads, makes the CLC5633 ideal for single ended cable applications. It also drives low impedance loads with minimum distortion. The CLC5633 will drive a $100 \Omega$ load with only $-82 /-69 \mathrm{dBc}$ second/third harmonic distortion ( $A_{v}=+2, \mathrm{~V}_{\text {out }}=2 \mathrm{~V}_{\mathrm{pp}}, \mathrm{f}=1 \mathrm{MHz}$ ). With a $25 \Omega$ load, and the same conditions, it produces only -71/ -73 dBc second/third harmonic distortion. It is also optimized for driving high currents into single-ended transformers and coils.

When driving the input of high-resolution $A / D$ converters, the CLC5633 provides excellent -86/-96dBc second/third harmonic distortion ( $\mathrm{A}_{\mathrm{V}}=+2, \mathrm{~V}_{\mathrm{out}}=2 \mathrm{~V}_{\mathrm{pp}}, \mathrm{f}=1 \mathrm{MHz}, \mathrm{R}_{\mathrm{L}}=1 \mathrm{k} \Omega$ ) and fast settling time.

The CLC5633 offers 0.1 dB gain flatness to 30 MHz and differential gain and phase errors of $0.08 \%$ and $0.02^{\circ}$. These features are ideal for professional and consumer video applications.

## Features

- 130mA output current
- $0.08 \%, 0.02^{\circ}$ differntial gain, phase
- 3.2 mA supply current
- 130 MHz bandwidth $\left(\mathrm{A}_{\mathrm{v}}=+2\right)$
- -86/-96dBc HD2/HD3 (1MHz)
- 17 ns settling to $0.05 \%$
- $410 \mathrm{~V} / \mathrm{\mu s}$ slew rate
- Stable for capacitive loads up to 1000pf
- Single 5 V to $\pm 5 \mathrm{~V}$ supplies


## Applications

- Video line driver
- Coaxial cable driver
- Twisted pair driver
- Transformer/Coil Driver
- High capacitive load driver
- Portable/battery-powered applications
- A/D driver




## LVDS and Channel Link

- DS90C401
- DS90C402
- DS90CR213/4
- DS90CR283/4
- DS90LV017

Dual, 5V, LVDS Driver
Dual, 5V, LVDS Receiver
21bit, 5V, 66MHz, 1.386 Gbps Channel Link

21bit, $5 \mathrm{~V}, 66 \mathrm{MHz}, 1.386 \mathrm{Gbps}$ Channel Link

LVDS Single, High Speed
Differential Driver



Electrical Characteristics (Notes 2 and 3)
Over supply voltage and operating temperature ranges, unless otherwise specified.

| Symbol | Parameter | Conditions |  | Pin | Min | Typ | Max | Units |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| $\mathrm{V}_{\text {OD1 }}$ | Differential Output Voltage | $R_{L}=100 \Omega$(Figure 1) |  | Dout-, <br> $\mathrm{D}_{\text {OUT }+}$ | 250 | 340 | 450 | mV |
| $\Delta \mathrm{V}_{\text {OD } 1}$ | Change in Magnitude of $\mathrm{V}_{\mathrm{OD} 1}$ for Complementary Output States |  |  |  | 4 | 35 | \|mV| |
| $\mathrm{V}_{\text {os }}$ | Offset Voltage |  |  | 1.125 | 1.25 | 1.375 | V |
| $\Delta \mathrm{V}_{\text {OS }}$ | Change in Magnitude of $\mathrm{V}_{\text {Os }}$ for Complementary Output States |  |  |  | 5 | 25 | \|mV| |
| $\mathrm{V}_{\mathrm{OH}}$ | Output Voltage High | $\mathrm{R}_{\mathrm{L}}=100 \Omega$ |  |  |  | 1.41 | 1.60 | V |
| $\mathrm{V}_{\text {OL }}$ | Output Voltage Low |  |  | 0.90 | 1.07 |  | V |
| $\mathrm{V}_{\mathrm{IH}}$ | Input Voltage High |  |  |  | $\mathrm{DIN}^{\text {I }}$ | 2.0 |  | $\mathrm{V}_{\mathrm{cc}}$ | V |
| $\mathrm{V}_{\mathrm{IL}}$ | Input Voltage Low |  |  |  |  | GND |  | 0.8 | V |
| $I_{1}$ | Input Current | $\mathrm{V}_{\mathrm{IN}}=\mathrm{V}_{\mathrm{CC}}, \mathrm{GND}, 2.5 \mathrm{~V}$, or 0.4V |  |  |  | -10 | $\pm 1$ | +10 | $\mu \mathrm{A}$ |
| $\mathrm{V}_{\mathrm{CL}}$ | Input Clamp Voltage | $\mathrm{I}_{\mathrm{CL}}=-18 \mathrm{~mA}$ |  |  |  | -1.5 | -0.8 |  | V |
| $\mathrm{l}_{\text {os }}$ | Output Short Circuit Current | $\mathrm{V}_{\text {OUT }}=0 \mathrm{~V}$ (Note 8) |  | $\begin{aligned} & \hline \mathrm{D}_{\text {OUT },}, \\ & \mathrm{D}_{\text {OUT }+} \end{aligned}$ |  | -3.5 | -5.0 | mA |
| $\mathrm{I}_{\mathrm{cc}}$ | No Load Supply Current Drivers Enabled | $\mathrm{D}_{\text {IN }}=\mathrm{V}_{\mathrm{CC}}$ or GND | DS90C401T | $\mathrm{V}_{\mathrm{cc}}$ |  | 1.7 | 3.0 | mA |
|  |  | $\mathrm{D}_{\text {IN }}=2.5 \mathrm{~V}$ or 0.4 V |  |  |  | 3.5 | 5.5 | mA |
| $\overline{I_{\text {ccL }}}$ | Loaded Supply Current Drivers Enabled | $\begin{aligned} & \hline \mathrm{R}_{\mathrm{L}}=100 \Omega \text { All Channels } \\ & \mathrm{V}_{\text {IN }}=\mathrm{V}_{\mathrm{CC}} \text { or GND (all } \\ & \text { inputs) } \\ & \hline \end{aligned}$ | DS90C401T |  |  | 8 | 14.0 | mA |

Switching Characteristics (Notes 3, 4, 5, 6, and 9)
$\mathrm{V}_{\mathrm{CC}}=+5.0 \mathrm{~V} \pm 10 \%, \mathrm{~T}_{\mathrm{A}}=-40^{\circ} \mathrm{C}$ to $+85^{\circ} \mathrm{C}$ DS90C401T

| Symbol | Parameter | Conditions | Min | Typ | Max | Units |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| $\mathrm{t}_{\text {PHLD }}$ | Differential Propagation Delay High to Low | $R_{L}=100 \Omega, C_{L}=5 \mathrm{pF}$ <br> (Figures 2, 3) | 0.5 | 2.0 | 3.5 | ns |
| $\overline{t_{\text {PLHD }}}$ | Differential Propagation Delay Low to High |  | 0.5 | 2.1 | 3.5 | ns |
| $t_{\text {SKD }}$ <br> $\left\|t_{\text {PHLD }}-t_{\text {PLHD }}\right\|$ | Differential Skew |  | 0 | 80 | 900 | ps |
| $\mathrm{t}_{\text {SK1 }}$ | Channel to Channel Skew | (Note 4) | 0 | 0.3 | 1.0 | ns |
| $\mathrm{t}_{\text {SK2 }}$ | Chip to Chip Skew | (Note 5) |  |  | 3.0 | ns |
| $\mathrm{t}_{\text {TLH }}$ | Rise Time | $\mathrm{R}_{\mathrm{L}}=100 \Omega, \mathrm{C}_{\mathrm{L}}=5 \mathrm{pF}$ <br> (Figures 2, 3) |  | 0.35 | 2.0 | ns |
| $\mathrm{t}_{\text {THL }}$ | Fall Time |  |  | 0.35 | 2.0 | ns |

## Parameter Measurement Information



FIGURE 1. Driver $V_{\text {OD }}$ and $V_{\text {Os }}$ Test Circuit


DS100013-4

FIGURE 2. Driver Propagation Delay and Transition Time Test Circuit


FIGURE 3. Driver Propagation Delay and Transition Time Waveforms

## Typical Application



DS100013-9
FIGURE 4. Point-to-Point Application

## Applications Information

LVDS drivers and receivers are intended to be primarily used in an uncomplicated point-to-point configuration as is shown in Figure 4. This configuration provides a clean signaling environment for the quick edge rates of the drivers. The receiver is connected to the driver through a balanced media which may be a standard twisted pair cable, a parallel pair cable, or simply PCB traces. Typically, the characteristic impedance of the media is in the range of $100 \Omega$. A termination resistor of $100 \Omega$ should be selected to match the media, and is located as close to the receiver input pins as possible. The termination resistor converts the current sourced by the driver into a voltage that is detected by the receiver. Other configurations are possible such as a multi-receiver configuration, but the effects of a mid-stream connector(s), cable stub(s), and other impedance discontinuities as well as ground shifting, noise margin limits, and total termination loading must be taken into account.
The DS90C401 differential line driver is a balanced current source design. A current mode driver, generally speaking has a high output impedance and supplies a constant current for a range of loads (a voltage mode driver on the other hand supplies a constant voltage for a range of loads). Current is switched through the load in one direction to produce a logic state and in the other direction to produce the other logic state. The typical output current is mere 3.4 mA , a minimum of 2.5 mA , and a maximum of 4.5 mA . The current mode requires (as discussed above) that a resistive termination be employed to terminate the signal and to complete
the loop as shown in Figure 4. AC or unterminated configurations are not allowed. The 3.4 mA loop current will develop a differential voltage of 340 mV across the $100 \Omega$ termination resistor which the receiver detects with a 240 mV minimum differential noise margin neglecting resistive line losses (driven signal minus receiver threshold ( $340 \mathrm{mV}-100 \mathrm{mV}=$ 240 mV )). The signal is centered around +1.2 V (Driver Off set, $\mathrm{V}_{\mathrm{OS}}$ ) with respect to ground as shown in Figure 5. Note that the steady-state voltage ( $\mathrm{V}_{\mathrm{SS}}$ ) peak-to-peak swing is twice the differential voltage ( $\mathrm{V}_{\mathrm{OD}}$ ) and is typically 680 mV .
The current mode driver provides substantial benefits over voltage mode drivers, such as an RS-422 driver. Its quiescent current remains relatively flat versus switching frequency. Whereas the RS-422 voltage mode driver increases exponentially in most case between $20 \mathrm{MHz}-50 \mathrm{MHz}$. This is due to the overlap current that flows between the rails of the device when the internal gates switch. Whereas the current mode driver switches a fixed current between its output without any substantial overlap current. This is similar to some ECL and PECL devices, but without the heavy static $\mathrm{I}_{\mathrm{Cc}}$ requirements of the ECL/PECL designs. LVDS requires $80 \%$ less current than similar PECL devices. AC specifications for the driver are a tenfold improvement over other existing RS-422 drivers.
The TRI-STATE function allows the driver outputs to be disabled, thus obtaining an even lower power state when the transmission of data is not required.
The footprint of the DS90C401 is the same as the industry standard 26LS31 Quad Differential (RS-422) Driver.


DS100013-10
FIGURE 5. Driver Output Levels

## Pin Descriptions

TABLE 1. Device Pin Descriptions

| Pin No. | Name | Description |
| :--- | :---: | :--- |
| 4,8 | $\mathrm{D}_{\text {IN }}$ | TTL/CMOS driver input pins |
| 3,7 | $\mathrm{D}_{\text {OUT+ }+}$ | Non-inverting driver output pin, |
| 2,6 | $\mathrm{D}_{\text {OUT- }}$ | Inverting driver output pin, |
| 5 | GND | Ground pin |
| 1 | $\mathrm{~V}_{\mathrm{CC}}$ | Positive power supply pin, +5.0 V <br> $\pm 10$ |

## Ordering Information

| Operating <br> Temperature | Package Type/ <br> Number | Order Number |
| :---: | :---: | :---: |
| $-40^{\circ} \mathrm{C}$ to $+85^{\circ} \mathrm{C}$ | SOP/M08A | DS90C 401 TM |

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" specifies conditions of device operation.
Note 2: Current into device pins is defined as positive. Current out of device pins is defined as negative. All voltages are referenced to ground except: $\mathrm{V}_{\mathrm{OD} 1}$ and $\Delta \mathrm{V}_{\mathrm{OD} 1}$ -
Note 3: All typicals are given for: $\mathrm{V}_{\mathrm{CC}}=+5.0 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=+25^{\circ} \mathrm{C}$.
Note 4: Channel to Channel Skew is defined as the difference between the propagation delay of the channel and the other channels in the same chip with an event on the inputs.
Note 5: Chip to Chip Skew is defined as the difference between the minimum and maximum specified differential propagation delays.
Note 6: Generator waveform for all tests unless otherwise specified: $f=1 \mathrm{MHz}, Z_{O}=50 \Omega, t_{r} \leq 6 \mathrm{~ns}$, and $\mathrm{t}_{\mathrm{f}} \leq 6 \mathrm{~ns}$
Note 7: ESD Ratings: HBM ( $1.5 \mathrm{k} \Omega, 100 \mathrm{pF}) \geq 3,500 \mathrm{~V}$
EIAJ $(0 \Omega, 200 \mathrm{pF}) \geq 250 \mathrm{~V}$
Note 8: Output short circuit current ( $\mathrm{l}_{\mathrm{OS}}$ ) is specified as magnitude only, minus sign indicates direction only
Note 9: $C_{L}$ includes probe and jig capacitance.

## Truth Table

| INPUT/OUTPUT |  |  |
| :---: | :---: | :---: |
| $\mathrm{D}_{\text {IN }}$ | $\mathrm{D}_{\text {OUT }}{ }^{+}$ | $\mathbf{D}_{\text {OUT }^{-}}$ |
| L | L | H |
| H | H | L |
| $2>\&>.8$ | X | X |

$\mathrm{H}=$ Logic high level
L = Logic low level
X = Indeterminant state

## Typical Performance Characteristics

Power Supply Current
vs Power Supply Voltage


Power Supply Current vs Temperature


Typical Performance Characteristics (Continued)


## Output TRI-STATE Current <br> vs Power Supply Voltage



Power Supply Current vs Temperature


Output Short Circuit Current vs Power Supply Voltage


DS100013-16


## Typical Performance Characteristics (Continued)

Output Voltage High vs


## Output Voltage Low vs

Power Supply Voltage


Offset Voltage vs
Power Supply Voltage


Output Voltage High vs Ambient Temperature


Output Voltage Low vs Ambient Temperature


Offset Voltage vs
Ambient Temperature


Typical Performance Characteristics (Continued)



Power Supply Current vs Frequency



Differential Skew vs


## Typical Performance Characteristics (Continued)




Physical Dimensions inches (millimeters)


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| Absolute Maximum Ratings (Note 1) | Maximum Junction Temperature (DS90C402T) |  | $+150^{\circ} \mathrm{C}$ |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: |
| If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications. | $\begin{aligned} & \text { ESD Rating } \\ & (\mathrm{HBM} 1.5 \mathrm{k} \Omega, 100 \mathrm{pF}) \end{aligned}$ |  | $\geq 3,500 \mathrm{~V}$ (Note 4) |  |  |
| Supply Voltage ( $\mathrm{V}_{\mathrm{CC}}$ ) -0.3 V to +6 V | Recommended Operating Conditions |  |  |  |  |
| Input Voltage ( $\mathrm{R}_{\mathbf{I N +},}, \mathrm{R}_{\mathrm{IN}-}$ ) $\quad-0.3 \mathrm{~V}$ to ( $\left.\mathrm{V}_{\mathrm{CC}}+0.3 \mathrm{~V}\right)$ |  |  |  |  |  |
| Output Voltage ( $\mathrm{R}_{\text {OUT }}$ ) $\quad-0.3 \mathrm{~V}$ to ( $\left.\mathrm{V}_{\mathrm{CC}}+0.3 \mathrm{~V}\right)$ |  |  |  |  |  |
| Maximum Package Power Dissipation @ $+25^{\circ} \mathrm{C}$ |  | Min | Typ | Max | Units |
| M Package 1025 mW | Supply Voltage ( $\mathrm{V}_{\mathrm{cc}}$ ) | +4.5 | +5.0 | +5.5 | V |
| Derate M Package $\quad 8.2 \mathrm{~mW} /{ }^{\circ} \mathrm{C}$ above $+25^{\circ} \mathrm{C}$ | Receiver Input Voltage | GND |  | 2.4 | v |
| Storage Temperature Range $\quad-65^{\circ} \mathrm{C}$ to $+150^{\circ} \mathrm{C}$ | Operating Free Air Temp | ure (T) |  |  |  |
| Lead Temperature Range <br> Soldering (4 sec.) <br> $+260^{\circ} \mathrm{C}$ | DS90C402T | -40 | +25 | +85 | C |

## Electrical Characteristics (Note 2)

Over Supply Voltage and Operating Temperature ranges, unless otherwise specified.

| Symbol | Parameter | Conditions |  | Pin | Min | Typ | Max | Units |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| $\mathrm{V}_{\text {TH }}$ | Differential Input High Threshold | $\mathrm{V}_{\mathrm{CM}}=+1.2 \mathrm{~V}$ |  | $\begin{aligned} & \mathrm{R}_{\mathrm{IN}+}, \\ & \mathrm{R}_{\mathrm{IN}-} \end{aligned}$ |  |  | +100 | mV |
| $\mathrm{V}_{\text {TL }}$ | Differential Input Low Threshold |  |  | -100 |  |  | mV |
| $\mathrm{I}_{\mathrm{IN}}$ | Input Current | $\mathrm{V}_{\text {IN }}=+2.4 \mathrm{~V}$ | $\mathrm{V}_{\mathrm{CC}}=5.5 \mathrm{~V}$ |  | -10 | $\pm 1$ | +10 | $\mu \mathrm{A}$ |
|  |  | $\mathrm{V}_{\mathrm{IN}}=0 \mathrm{~V}$ |  |  | -10 | $\pm 1$ | +10 | $\mu \mathrm{A}$ |
| $\mathrm{V}_{\mathrm{OH}}$ | Output High Voltage | $\mathrm{I}_{\mathrm{OH}}=-0.4 \mathrm{~mA}, \mathrm{~V}_{\mathrm{ID}}=+200 \mathrm{mV}$ |  |  | $\mathrm{R}_{\text {OUT }}$ | 3.8 | 4.9 |  | V |
|  |  | $\mathrm{I}_{\mathrm{OH}}=-0.4 \mathrm{~mA}$, Input terminated | DS90C402T | 3.8 |  | 4.9 |  | V |
|  |  | Inputs Open |  |  |  |  |  |  |
|  |  | Inputs Shorted |  |  |  |  |  |  |
| $\mathrm{V}_{\mathrm{OL}}$ | Output Low Voltage | $\mathrm{I}_{\mathrm{OL}}=2 \mathrm{~mA}, \mathrm{~V}_{\mathrm{ID}}=-200 \mathrm{mV}$ |  |  |  | 0.07 | 0.3 | V |
| $\mathrm{I}_{\mathrm{OS}}$ | Output Short Circuit Current | $\mathrm{V}_{\text {OUT }}=0 \mathrm{~V}$ (Note 8) |  | -15 |  | -60 | -100 | mA |
| $\mathrm{I}_{\mathrm{Cc}}$ | No Load Supply Current <br> Receivers Enabled | Inputs Open | DS90C402T | $\mathrm{V}_{\mathrm{cc}}$ |  | 3.5 | 10 | mA |
|  |  |  |  |  |  | 3.5 | 11 | mA |
|  |  | Inputs Open |  |  |  | 3.7 | 11 | mA |

Switching Characteristics (Notes 3, 4, 5, 6, and 9)
$\mathrm{V}_{\mathrm{CC}}=+5.0 \mathrm{~V} \pm 10 \%, \mathrm{~T}_{\mathrm{A}}=-40^{\circ} \mathrm{C}$ to $+85^{\circ} \mathrm{C}$ DS90C402T

| Symbol | Parameter | Conditions | Min | Typ | Max | Units |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| $\mathrm{t}_{\text {PHLD }}$ | Differential Propagation Delay High to Low | $\begin{aligned} & \mathrm{C}_{\mathrm{L}}=5 \mathrm{pF} \\ & \mathrm{~V}_{\mathrm{ID}}=200 \mathrm{mV} \\ & (\text { Figures 1, 2) } \end{aligned}$ | 1.0 | 3.40 | 6.0 | ns |
| $\mathrm{t}_{\text {PLHD }}$ | Differential Propagation Delay Low to High |  | 1.0 | 3.48 | 6.0 | ns |
| $\mathrm{t}_{\text {SKD }}$ | Differential Skew \|t ${ }_{\text {PHLD }}-t_{\text {PLHD }} \mid$ |  | 0 | 0.08 | 1.2 | ns |
| $\mathrm{t}_{\text {SK1 }}$ | Channel to Channel Skew | (Note 5) | 0 | 0.6 | 1.5 | ns |
| $\mathrm{t}_{\text {SK2 }}$ | Chip to Chip Skew | (Note 6) |  |  | 5.0 | ns |
| $\mathrm{t}_{\text {TLH }}$ | Rise Time | (Figures 1, 2) |  | 0.5 | 2.5 | ns |
| $\mathrm{t}_{\text {THL }}$ | Fall Time |  |  | 0.5 | 2.5 | ns |

## Parameter Measurement Information



FIGURE 1. Receiver Propagation Delay and Transition Time Test Circuit


DS100006-4
(Receiver Propagation Delay and Transition Time Test Circuit

DS100006-5
FIGURE 2. Receiver Propagation Delay and Transition Time Waveforms

## Typical Application



## FIGURE 3. Point-to-Point Application

## Applications Information

LVDS drivers and receivers are intended to be primarily used in an uncomplicated point-to-point configuration as is shown in Figure 3. This configuration provides a clean signaling environment for the quick edge rates of the drivers. The receiver is connected to the driver through a balanced media which may be a standard twisted pair cable, a parallel pair cable, or simply PCB traces. Typically the characteristic impedance of the media is in the range of $100 \Omega$. A termination resistor of $100 \Omega$ should be selected to match the media, and is located as close to the receiver input pins as possible. The termination resistor converts the current sourced by the driver into a voltage that is detected by the receiver. Other configurations are possible such as a multi-receiver configuration, but the effects of a mid-stream connector(s), cable stub(s), and other impedance discontinuities as well as ground shifting, noise margin limits, and total termination loading must be taken into account.
The DS90C402 differential line receiver is capable of detecting signals as low as 100 mV , over a $\pm 1 \mathrm{~V}$ common mode range centered around +1.2 V . This is related to the driver offset voltage which is typically +1.2 V . The driven signal is centered around this voltage and may shift $\pm 1 \mathrm{~V}$ around this center point. The $\pm 1 \mathrm{~V}$ shifting may be the result of a ground potential difference between the driver's ground reference and the receiver's ground reference, the common mode ef-
fects of coupled noise, or a combination of the two. Both receiver input pins should honor their specified operating input voltage range of 0 V to +2.4 V (measured from each pin to ground), exceeding these limits may turn on the ESD protection circuitry which will clamp the bus voltages.
The receiver also supports a failsafe feature which provides a stable (known state) high output voltage for any of the following conditions:

1. Open Input Pins. The DS90C402 is a quad receiver device, and if an application requires only 1 , 2 or 3 receivers, the unused channel(s) inputs should be left OPEN. Do not tie unused receiver inputs to ground or other voltages. The internal circuitry will guarantee a high, stable output state.
2. Terminated Input. If the driver is in a TRI-STATE ${ }^{\oplus}$ condition, or if the driver is in a power-off condition, or if the driver is even disconnected (cable unplugged), the receiver output will again be in a high state, even with the end of cable $100 \Omega$ termination resistor across the input pins.
3. Shorted Inputs. If a cable fault condition occurs that shorts the twisted pair conductors together, thus resulting in a $0 V$ differential input voltage to the receiver, the receiver output will remain in a high state.
The footprint of the DS90C402 is the same as the industry standard 26LS32 Quad Differential (RS-422) Receiver.

## Pin Descriptions

| Pin <br> No. | Name | Description |
| :--- | :---: | :--- |
| 2,6 | $\mathrm{R}_{\text {OUT }}$ | Receiver output pin |
| 3,7 | $\mathrm{R}_{\mathrm{IN}^{+}}$ | Positive receiver input pin |
| 4,8 | $\mathrm{R}_{\mathrm{IN}^{-}}$ | Negative receiver input pin |
| 5 | $\mathrm{GND}^{\text {Ground pin }}$ |  |
| 1 | $\mathrm{~V}_{\mathrm{CC}}$ | Positive power supply pin, <br> $+5 \mathrm{~V} \pm 10 \%$ |

## Ordering Information

| Operating <br> Temperature | Package Type/ <br> Number | Order Number |
| :---: | :---: | :---: |
| $-40^{\circ} \mathrm{C}$ to $+85^{\circ} \mathrm{C}$ | SOP/M08A | DS90C402TM |

RECEIVE MODE

| $\mathbf{R}_{\mathbf{I N +}+}-\mathbf{R}_{\mathbf{I N -}}$ | $\mathbf{R}_{\text {OUT }}$ |
| :---: | :---: |
| $>+100 \mathrm{mV}$ | H |
| $<-100 \mathrm{mV}$ | L |
| $100 \mathrm{mV}>\&>-100 \mathrm{mV}$ | X |

$\mathrm{H}=$ Logic High Level
$\mathrm{L}=$ Logic Low level
$\mathrm{X}=$ Indeterminant State

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" specifies conditions of device operation.
Note 2: Current into device pins is defined as positive. Current out of device pins is defined as negative. All voltages are referenced to ground unless otherwise specified.
Note 3: All typicals are given for: $\mathrm{V}_{\mathrm{CC}}=+5.0 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=+25^{\circ} \mathrm{C}$.
Note 4: Generator waveform for all tests unless otherwise specified: $f=1 \mathrm{MHz}, Z_{O}=50 \Omega$, $t_{r}$ and $t_{f}(0 \%-100 \%) \leq 1 \mathrm{~ns}$ for $R_{I N}$ and $t_{r}$ and $t_{f} \leq 6 \mathrm{~ns}$ for $E N$ or $E N *$.
Note 5: Channel to Channel Skew is defined as the difference between the propagation delay of one channel and that of the others on the same chip with an event on the inputs.
Note 6: Chip to Chip Skew is defined as the difference between the minimum and maximum specified differential propagation delays.
Note 7: ESD Rating:
HBM ( $1.5 \mathrm{k} \Omega, 100 \mathrm{pF}$ ) $\geq 3,500 \mathrm{~V}$
EIAJ $(0 \Omega, 200 \mathrm{pF}) \geq 250 \mathrm{~V}$
Note 8: Output short circuit current ( $\mathrm{l}_{\mathrm{OS}}$ ) is specified as magnitude only, minus sign indicates direction only. Only one output should be shorted at a time, do not exceed maximum junction temperature specification.
Note 9: $C_{L}$ includes probe and jig capacitance.

## Typical Performance Characteristics



Output High Voltage vs Ambient Temperature


## Typical Performance Characteristics (Continued)

Output Low Voltage vs
Power Supply Voltage


DS100006-11

## Output Short Circuit Current vs Power Supply Voltage




Output Low Voltage vs Ambient Temperature


Output Short Circuit Current vs Ambient Temperature



## Typical Performance Characteristics (Continued)



Transition Time vs
Power Supply Voltage


Differential Skew vs
Ambient Temperature


Transition Time vs
Ambient Temperature

Physical Dimensions inches (millimeters)


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## Pin Diagrams



Typical Application



## Electrical Characteristics

Over recommended operating supply and temperature ranges unless otherwise specified.

| Symbol | Parameter | Conditions |  | Min | Typ | Max | Units |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| CMOS/TTL DC SPECIFICATIONS |  |  |  |  |  |  |  |
| $\mathrm{V}_{\mathrm{IH}}$ | High Level Input Voltage |  |  | 2.0 |  | $\mathrm{V}_{\mathrm{CC}}$ | V |
| $\mathrm{V}_{\text {IL }}$ | Low Level Input Voltage |  |  | GND |  | 0.8 | V |
| $\mathrm{V}_{\mathrm{OH}}$ | High Level Output Voltage | $\mathrm{I}_{\mathrm{OH}}=-0.4 \mathrm{~mA}$ |  | 3.8 | 4.9 |  | V |
| $\mathrm{V}_{\mathrm{OL}}$ | Low Level Output Voltage | $\mathrm{I}_{\mathrm{OL}}=2 \mathrm{~mA}$ |  |  | 0.1 | 0.3 | V |
| $\mathrm{V}_{\mathrm{CL}}$ | Input Clamp Voltage | $\mathrm{I}_{\mathrm{CL}}=-18 \mathrm{~mA}$ |  |  | -0.79 | -1.5 | V |
| $\mathrm{I}_{\mathrm{IN}}$ | Input Current | $\mathrm{V}_{\mathrm{IN}}=\mathrm{V}_{\mathrm{CC}}$, GND, 2.5 V or | .4V |  | $\pm 5.1$ | $\pm 10$ | $\mu \mathrm{A}$ |
| los | Output Short Circuit Current | $\mathrm{V}_{\text {OUT }}=0 \mathrm{~V}$ |  |  |  | -120 | mA |
| LVDS DRIVER DC SPECIFICATIONS |  |  |  |  |  |  |  |
| $\mathrm{V}_{\text {OD }}$ | Differential Output Voltage | $\mathrm{R}_{\mathrm{L}}=100 \Omega$ |  | 250 | 290 | 450 | mV |
| $\Delta \mathrm{V}_{\text {OD }}$ | Change in $\mathrm{V}_{\mathrm{OD}}$ between Complimentary Output States |  |  |  |  | 35 | mV |
| $\mathrm{V}_{\text {OS }}$ | Offset Voltage |  |  | 1.1 | 1.25 | 1.375 | V |
| $\Delta \mathrm{V}_{\text {OS }}$ | Change in Magnitude of $\mathrm{V}_{\mathrm{OS}}$ between Complimentary Output States |  |  |  |  | 35 | mV |
| $\mathrm{I}_{\mathrm{OS}}$ | Output Short Circuit Current | $\mathrm{V}_{\text {OUT }}=0 \mathrm{~V}, \mathrm{R}_{\mathrm{L}}=100 \Omega$ |  |  | -2.9 | -5 | mA |
| $\mathrm{I}_{\mathrm{Oz}}$ | Output TRI-STATE ${ }^{\oplus}$ Current | $\overline{\text { Powerdown }}=0 \mathrm{~V}, \mathrm{~V}_{\text {OUT }}=$ | V or $\mathrm{V}_{\mathrm{Cc}}$ |  | $\pm 1$ | $\pm 10$ | $\mu \mathrm{A}$ |
| LVDS RECEIVER DC SPECIFICATIONS |  |  |  |  |  |  |  |
| $\mathrm{V}_{\text {TH }}$ | Differential Input High Threshold | $\mathrm{V}_{\mathrm{CM}}=+1.2 \mathrm{~V}$ |  |  |  | +100 | mV |
| $\mathrm{V}_{\text {TL }}$ | Differential Input Low Threshold |  |  | -100 |  |  | mV |
| $\mathrm{I}_{\mathrm{N}}$ | Input Current | $\mathrm{V}_{\mathrm{IN}}=+2.4 \mathrm{~V}, \mathrm{~V}_{\mathrm{CC}}=5.0 \mathrm{~V}$ |  |  |  | $\pm 10$ | $\mu \mathrm{A}$ |
|  |  | $\mathrm{V}_{\mathrm{IN}}=0 \mathrm{~V}, \mathrm{~V}_{\mathrm{CC}}=5.0 \mathrm{~V}$ |  |  |  | $\pm 10$ | $\mu \mathrm{A}$ |
| TRANSMITTER SUPPLY CURRENT |  |  |  |  |  |  |  |
| $\mathrm{I}_{\text {cctw }}$ | Transmitter Supply Current Worst Case | $\mathrm{R}_{\mathrm{L}}=100 \Omega, \mathrm{C}_{\mathrm{L}}=5 \mathrm{pF},$ <br> Worst Case Pattern <br> (Figure 1 and Figure 2 ) | $\mathrm{f}=32.5 \mathrm{MHz}$ |  | 49 | 63 | mA |
|  |  |  | $\mathrm{f}=37.5 \mathrm{MHz}$ |  | 51 | 64 | mA |
|  |  |  | $\mathrm{f}=66 \mathrm{MHz}$ |  | 70 | 84 | mA |
| $\mathrm{I}_{\text {CCTZ }}$ | Transmitter Supply Current Power Down | $\overline{\bar{P} o w e r d o w n}=\text { Low }$ <br> Driver Outputs in TRI-STATE under Powerdown Mode |  |  | 1 | 10 | $\mu \mathrm{A}$ |

Electrical Characteristics (Continued)
Over recommended operating supply and temperature ranges unless otherwise specified.

| Symbol | Parameter | Conditions |  | Min | Typ | Max | Units |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| RECEIVER SUPPLY CURRENT |  |  |  |  |  |  |  |
| $\mathrm{I}_{\text {CCRW }}$ | Receiver Supply Current Worst Case | $\mathrm{C}_{\mathrm{L}}=8 \mathrm{pF},$ <br> Worst Case Pattern <br> (Figure 1 and Figure 3 ) | $\mathrm{f}=32.5 \mathrm{MHz}$ |  | 64 | 77 | mA |
|  |  |  | $\mathrm{f}=37.5 \mathrm{MHz}$ |  | 70 | 85 | mA |
|  |  |  | $\mathrm{f}=66 \mathrm{MHz}$ |  | 110 | 140 | mA |
| $\mathrm{I}_{\text {CCRZ }}$ | Receiver Supply Current Power Down | $\overline{\text { Powerdown }=\text { Low }}$ <br> Receiver Outputs in Previ Power Down Mode. | us State during |  | 1 | 10 | $\mu \mathrm{A}$ |

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the device
should be operated at these limits. The tables of "Electrical Characteristics" specify conditions for device operation.
Note 2: Typical values are given for $\mathrm{V}_{\mathrm{CC}}=5.0 \mathrm{~V}$ and $\mathrm{T}_{\mathrm{A}}=+25^{\circ} \mathrm{C}$.
Note 3: Current into device pins is defined as positive. Current out of device pins is defined as negative. Voltages are referenced to ground unless otherwise speci-
fied (except $\mathrm{V}_{\mathrm{OD}}$ and $\Delta \mathrm{V}_{\mathrm{OD}}$ ).
Note 4: ESD Rating: HBM ( $1.5 \mathrm{k} \Omega, 100 \mathrm{pF}$ )
PLL VCC $\geq 1000 \mathrm{~V}$
All Other Pins $\geq 2000 \mathrm{~V}$
EIAJ $(0 \Omega, 200 \mathrm{pF}) \geq 150 \mathrm{~V}$
Note 5: $\mathrm{V}_{\mathrm{OS}}$ previously referred as $\mathrm{V}_{\mathrm{CM}}$.

## Transmitter Switching Characteristics

Over recommended operating supply and temperature ranges unless otherwise specified

| Symbol | Parameter |  | Min | Typ | Max | Units |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| LLHT | LVDS Low-to-High Transition Time (Figure 2 ) |  |  | 0.75 | 1.5 | ns |
| LHLT | LVDS High-to-Low Transition Time (Figure 2) |  |  | 0.75 | 1.5 | ns |
| TCIT | TxCLK IN Transition Time (Figure 4 ) |  |  |  | 8 | ns |
| TCCS | TxOUT Channel-to-Channel Skew (Note 6) (Figure 5) |  |  |  | 350 | ps |
| TPPos0 | Transmitter Output Pulse Position for Bit 0 (Figure 16 ) | $\mathrm{f}=66 \mathrm{MHz}$ | -0.30 | 0 | 0.30 | ns |
| TPPos1 | Transmitter Output Pulse Position for Bit 1 |  | 1.70 | (1/7)Tclk | 2.50 | ns |
| TPPos2 | Transmitter Output Pulse Position for Bit 2 |  | 3.60 | (2/7)Tclk | 4.50 | ns |
| TPPos3 | Transmitter Output Pulse Position for Bit 3 |  | 5.90 | (3/7)Tclk | 6.75 | ns |
| TPPos4 | Transmitter Output Pulse Position for Bit 4 |  | 8.30 | (4/7)Tclk | 9.00 | ns |
| TPPos5 | Transmitter Output Pulse Position for Bit 5 |  | 10.40 | (5/7)Tclk | 11.10 | ns |
| TPPos6 | Transmitter Output Pulse Position for Bit 6 |  | 12.70 | (6/7)Tclk | 13.40 | ns |
| TCIP | TxCLK IN Period (Figure 6) |  | 15 | T | 50 | ns |
| TCIH | TxCLK IN High Time (Figure 6 ) |  | 0.35T | 0.5T | 0.65T | ns |
| TCIL | TxCLK IN Low Time (Figure 6 ) |  | 0.35T | 0.5 T | 0.65 T | ns |
| TSTC | TxIN Setup to TxCLK IN (Figure 6) |  | 5 | 3.5 |  | ns |
| THTC | TxIN Hold to TxCLK IN (Figure 6) |  | 2.5 | 1.5 |  | ns |
| TCCD | TxCLK IN to TxCLK OUT Delay @ $5^{\circ} \mathrm{C}, \mathrm{V}_{\mathrm{CC}}=5.0 \mathrm{~V}$ (Figure 8 ) |  | 3.5 |  | 8.5 | ns |
| TPLLS | Transmitter Phase Lock Loop Set (Figure 10) |  |  |  | 10 | ms |
| TPDD | Transmitter Powerdown Delay (Figure 14 ) |  |  |  | 100 | ns |

Note 6: This limit based on bench characterization.

## Receiver Switching Characteristics

Over recommended operating supply and temperature ranges unless otherwise specified

| Symbol | Parameter | Min | Typ | Max | Units |
| :--- | :--- | :---: | :---: | :---: | :---: |
| CLHT | CMOS/TTL Low-to-High Transition Time (Figure 3 ) |  | 2.5 | 4.0 | ns |
| CHLT | CMOS TTL High-to-Low Transition Time (Figure 3) |  | 2.0 | 4.0 | ns |
| RSKM | RxIN Skew Margin (Note 7) $\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}($ Figure 17) | $\mathrm{f}=40 \mathrm{MHz}$ | 700 |  |  |
|  |  | $\mathrm{f}=66 \mathrm{MHz}$ | 600 |  | ps |

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| Receiver Switching Characteristics (Continued) <br> Over recommended operating supply and temperature ranges unless otherwise specified |  |  |  |  |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| Symbol | Parameter |  | Min | Typ | Max | Units |
| RCOP | RxCLK OUT Period (Figure 7) |  | 15 | T | 50 | ns |
| RCOH | RxCLK OUT High Time (Figure 7) | $\mathrm{f}=40 \mathrm{MHz}$ | 6 |  |  | ns |
|  |  | $\mathrm{f}=66 \mathrm{MHz}$ | 4.3 | 5 |  | ns |
| RCOL | RxCLK OUT Low Time (Figure 7) | $\mathrm{f}=40 \mathrm{MHz}$ | 10.5 |  |  | ns |
|  |  | $\mathrm{f}=66 \mathrm{MHz}$ | 7.0 | 9 |  | ns |
| RSRC | RxOUT Setup to RxCLK OUT (Figure 7) | $\mathrm{f}=40 \mathrm{MHz}$ | 4.5 |  |  | ns |
|  |  | $\mathrm{f}=66 \mathrm{MHz}$ | 2.5 | 4.2 |  | ns |
| RHRC | RxOUT Hold to RxCLK OUT (Figure 7 ) | $\mathrm{f}=40 \mathrm{MHz}$ | 6.5 |  |  | ns |
|  |  | $\mathrm{f}=66 \mathrm{MHz}$ | 4 | 5.2 |  | ns |
| RCCD | RxCLK IN to RxCLK OUT Delay @ $5^{\circ} \mathrm{C}$, $\mathrm{V}_{\mathrm{CC}}=5.0 \mathrm{~V}$ (Figure 9) |  | 6.4 |  | 10.7 | ns |
| RPLLS | Receiver Phase Lock Loop Set (Figure 11) |  |  |  | 10 | ms |
| RPDD | Receiver Powerdown Delay (Figure 15 ) |  |  |  | 1 | $\mu \mathrm{s}$ |

Note 7: Receiver Skew Margin is defined as the valid data sampling region at the receiver inputs. This margin takes into account for transmitter output skew (TCCS) and the setup and hold time (internal data sampling window), allowing LVDS cable skew dependent on type/length and source clock (TxCLK IN) jitter.
RSKM $\geq$ cable skew (type, length) + source clock jitter (cycle to cycle)

## AC Timing Diagrams



FIGURE 1. "Worst Case" Test Pattern


Vdiff $=($ TxOUT +$)-(T \times O U T-)$


FIGURE 2. DS90CR213 (Transmitter) LVDS Output Load and Transition Times


FIGURE 3. DS90CR214 (Receiver) CMOS/TTL Output Load and Transition Times

## AC Timing Diagrams (Continued)



FIGURE 4. DS90CR213 (Transmitter) Input Clock Transition Time


DS012888-7

DS012888-8
Note 8: Measurements at $\mathrm{V}_{\text {diff }}=0 \mathrm{~V}$
Note 9: TCSS measured between earliest and latest LVDS edges.
Note 10: TxCLK Differential Low $\rightarrow$ High Edge
FIGURE 5. DS90CR213 (Transmitter) Channel-to-Channel Skew


DS012888-9
FIGURE 6. DS90CR213 (Transmitter) Setup/Hold and High/Low Times


FIGURE 7. DS90CR214 (Receiver) Setup/Hold and High/Low Times

## AC Timing Diagrams (Continued)



FIGURE 8. DS90CR213 (Transmitter) Clock In to Clock Out Delay


FIGURE 9. DS90CR214 (Receiver) Clock In to Clock Out Delay


DS012888-13
FIGURE 10. DS90CR213 (Transmitter) Phase Lock Loop Set Time


FIGURE 11. DS90CR214 (Receiver) Phase Lock Loop Set Time

## AC Timing Diagrams (Continued)



FIGURE 12. Seven Bits of LVDS in Once Clock Cycle


FIGURE 13. 21 Parallel TTL Data Inputs Mapped to LVDS Outputs (DS90CR283)


FIGURE 14. Transmitter Powerdown Delay


RxOUT


AC Timing Diagrams (Continued)


DS012888-19
FIGURE 16. Transmitter LVDS Output Pulse Position Measurement


Ideal Strobe Position
SW—Setup and Hold Time (Internal Data Sampling Window)
TCCS—Transmitter Output Skew
RSKM $\geq$ Cable Skew (Type, Length) + Source Clock Jitter (Cycle to Cycle)
Cable Skew-Typically $10 \mathrm{ps}-40 \mathrm{ps}$ per foot
FIGURE 17. Receiver LVDS Input Skew Margin

## DS90CR213 Pin Description—Channel Link Transmitter

| Pin Name | I/O | No. |  |
| :--- | :---: | :---: | :--- |
| TxIN | I | 21 | TTL level inputs. |
| TxOUT + | O | 3 | Positive LVDS differential data output. |
| TxOUT- | O | 3 | Negative LVDS differential data output. |
| TxCLK IN | I | 1 | TTL level clock input. The rising edge acts as data strobe. |
| TxCLK OUT + | O | 1 | Positive LVDS differential clock output. |
| TxCLK OUT- | O | 1 | Negative LVDS differential clock output. |
| PWR DOWN | I | 1 | TTL level input. Assertion (low input) TRI-STATES the outputs, ensuring low current at power <br> down. |
| $V_{\text {CC }}$ | I | 4 | Power supply pins for TTL inputs. |
| GND | I | 5 | Ground pins for TTL inputs. |

## DS90CR213 Pin Description—Channel Link Transmitter (Continued)

| Pin Name | I/O | No. |  | Description |
| :--- | :---: | :---: | :--- | :--- |
| PLL $\mathrm{V}_{\mathrm{CC}}$ | I | 1 | Power supply pin for PLL. |  |
| PLL GND | I | 2 | Ground pins for PLL. |  |
| LVDS $\mathrm{V}_{\mathrm{CC}}$ | 1 | 1 | Power supply pin for LVDS outputs. |  |
| LVDS GND | I | 3 | Ground pins for LVDS outputs. |  |

DS90CR214 Pin Description—Channel Link Receiver

| Pin Name | 1/0 | No. | Description |
| :---: | :---: | :---: | :---: |
| Rxin+ | 1 | 3 | Positive LVDS differential data inputs. |
| RxiN- | 1 | 3 | Negative LVDS differential data inputs. |
| RxOUT | 0 | 21 | TTL level outputs. |
| RxCLK IN+ | 1 | 1 | Positive LVDS differential clock input. |
| RxCLK IN- | 1 | 1 | Negative LVDS differential clock input. |
| RxCLK OUT | O | 1 | TTL level clock output. The rising edge acts as data strobe. |
| $\overline{\text { PWR DOWN }}$ | 1 | 1 | TTL level input. Locks the previous receiver output state. |
| $\mathrm{V}_{\mathrm{cc}}$ | 1 | 4 | Power supply pins for TTL outputs. |
| GND | 1 | 5 | Ground pins for TTL outputs. |
| PLL V ${ }_{\text {cc }}$ | 1 | 1 | Power supply for PLL. |
| PLL GND | 1 | 2 | Ground pin for PLL. |
| LVDS V ${ }_{\text {cc }}$ | 1 | 1 | Power supply pin for LVDS inputs. |
| LVDS GND | 1 | 3 | Ground pins for LVDS inputs. |

## Applications Information

The Channel Link devices are intended to be used in a wide variety of data transmission applications. Depending upon the application the interconnecting media may vary. For example, for lower data rate (clock rate) and shorter cable lengths ( $<2 \mathrm{~m}$ ), the media electrical performance is less critical. For higher speed/long distance applications the media's performance becomes more critical. Certain cable constructions provide tighter skew (matched electrical length between the conductors and pairs). Twin-coax for example, has been demonstrated at distances as great as 5 meters and with the maximum data transfer of $1.38 \mathrm{Gbit} / \mathrm{s}$. Additional applications information can be found in the following National Interface Application Notes:

| AN $=$ \#\#\#\# | Topic |
| :--- | :--- |
| AN-1041 | Introduction to Channel Link |
| AN-1035 | PCB Design Guidelines for LVDS and <br> Link Devices |
| AN-806 | Transmission Line Theory |
| AN-905 | Transmission Line Calculations and |
|  | Differential Impedance |
| AN-916 | Cable Information |

CABLES: A cable interface between the transmitter and receiver needs to support the differential LVDS pairs. The 21-bit CHANNEL LINK chipset (DS90CR213/214) requires four pairs of signal wires and the 28 -bit CHANNEL LINK chipset (DS90CR283/284) requires five pairs of signal wires. The ideal cable/connector interface would have a constant $100 \Omega$ differential impedance throughout the path. It is also
recommended that cable skew remain below 350 ps (@ 66 MHz clock rate) to maintain a sufficient data sampling window at the receiver.
In addition to the four or five cable pairs that carry data and clock, it is recommended to provide at least one additional conductor (or pair) which connects ground between the transmitter and receiver. This low impedance ground provides a common mode return path for the two devices. Some of the more commonly used cable types for point-to-point applications include flat ribbon, flex, twisted pair and Twin-Coax. All are available in a variety of configurations and options. Flat ribbon cable, flex and twisted pair generally perform well in short point-to-point applications while Twin-Coax is good for short and long applications. When using ribbon cable, it is recommended to place a ground line between each differential pair to act as a barrier to noise coupling between adjacent pairs. For Twin-Coax cable applications, it is recommended to utilize a shield on each cable pair. All extended point-to-point applications should also employ an overall shield surrounding all cable pairs regardless of the cable type. This overall shield results in improved transmission parameters such as faster attainable speeds, longer distances between transmitter and receiver and reduced problems associated with EMS or EMI.
The high-speed transport of LVDS signals has been demonstrated on several types of cables with excellent results. However, the best overall performance has been seen when using Twin-Coax cable. Twin-Coax has very low cable skew and EMI due to its construction and double shielding. All of the design considerations discussed here and listed in the supplemental application notes provide the subsystem communications designer with many useful guidelines. It is rec-

## Applications Information (Continued)

ommended that the designer assess the tradeoffs of each application thoroughly to arrive at a reliable and economical cable solution.
BOARD LAYOUT: To obtain the maximum benefit from the noise and EMI reductions of LVDS, attention should be paid to the layout of differential lines. Lines of a differential pair should always be adjacent to eliminate noise interference from other signals and take full advantage of the noise canceling of the differential signals. The board designer should also try to maintain equal length on signal traces for a given differential pair. As with any high speed design, the impedance discontinuities should be limited (reduce the numbers of vias and no 90 degree angles on traces). Any discontinuities which do occur on one signal line should be mirrored in the other line of the differential pair. Care should be taken to ensure that the differential trace impedance match the differential impedance of the selected physical media (this impedance should also match the value of the termination resistor that is connected across the differential pair at the receiver's input). Finally, the location of the CHANNEL LINK TxOUT/ RxIN pins should be as close as possible to the board edge so as to eliminate excessive pcb runs. All of these considerations will limit reflections and crosstalk which adversely effect high frequency performance and EMI.
UNUSED INPUTS: All unused inputs at the TxIN inputs of the transmitter must be tied to ground. All unused outputs at the RxOUT outputs of the receiver must then be left floating.

TERMINATION: Use of current mode drivers requires a terminating resistor across the receiver inputs. The CHANNEL LINK chipset will normally require a single $100 \Omega$ resistor between the true and complement lines on each differential pair of the receiver input. The actual value of the termination resistor should be selected to match the differential mode characteristic impedance ( $90 \Omega$ to $120 \Omega$ typical) of the cable. Figure 18 shows an example. No additional pull-up or pull-down resistors are necessary as with some other differential technologies such as PECL. Surface mount resistors are recommended to avoid the additional inductance that accompanies leaded resistors. These resistors should be placed as close as possible to the receiver input pins to reduce stubs and effectively terminate the differential lines.
DECOUPLING CAPACITORS: Bypassing capacitors are needed to reduce the impact of switching noise which could limit performance. For a conservative approach three parallel-connected decoupling capacitors (Multi-Layered Ceramic type in surface mount form factor) between each $\mathrm{V}_{\mathrm{CC}}$ and the ground plane(s) are recommended. The three capacitor values are $0.1 \mu \mathrm{~F}, 0.01 \mu \mathrm{~F}$ and $0.001 \mu \mathrm{~F}$. An example is shown in Figure 19. The designer should employ wide traces for power and ground and ensure each capacitor has its own via to the ground plane. If board space is limiting the number of bypass capacitors, the PLL $V_{C C}$ should receive the most filtering/bypassing. Next would be the LVDS $\mathrm{V}_{\mathrm{CC}}$ pins and finally the logic $\mathrm{V}_{\mathrm{CC}}$ pins.


FIGURE 18. LVDS Serialized Link Termination


FIGURE 19. CHANNEL LINK Decoupling Configuration

CLOCK JITTER: The CHANNEL LINK devices employ a PLL to generate and recover the clock transmitted across the LVDS interface. The width of each bit in the serialized LVDS data stream is one-seventh the clock period. For example, a 66 MHz clock has a period of 15 ns which results in a data bit
width of 2.16 ns . Differential skew ( $\Delta \mathrm{t}$ within one differential pair), interconnect skew ( $\Delta$ t of one differential pair to another) and clock jitter will all reduce the available window for sampling the LVDS serial data streams. Care must be taken to ensure that the clock input to the transmitter be a clean low noise signal. Individual bypassing of each $\mathrm{V}_{\mathrm{CC}}$ to ground will minimize the noise passed on to the PLL, thus creating a low jitter LVDS clock. These measures provide more margin for channel-to-channel skew and interconnect skew as a part of the overall jitter/skew budget.
COMMON MODE vs. DIFFERENTIAL MODE NOISE MARGIN: The typical signal swing for LVDS is 300 mV centered at +1.2 V . The CHANNEL LINK receiver supports a 100 mV threshold therefore providing approximately 200 mV of differential noise margin. Common mode protection is of more importance to the system's operation due to the differential data transmission. LVDS supports an input voltage range of Ground to +2.4 V . This allows for a $\pm 1.0 \mathrm{~V}$ shifting of the center point due to ground potential differences and common mode noise.

## Applications Information (Continued)

POWER SEQUENCING AND POWERDOWN MODE: Outputs of the CHANNEL LINK transmitter remain in TRI-STATE until the power supply reaches 3 V . Clock and data outputs will begin to toggle 10 ms after $\mathrm{V}_{\mathrm{cc}}$ has reached 4.5 V and the Powerdown pin is above 2V. Either device may be placed into a powerdown mode at any time by asserting the Powerdown pin (active low). Total power dissipation for each device will decrease to $5 \mu \mathrm{~W}$ (typical).

The CHANNEL LINK chipset is designed to protect itself from accidental loss of power to either the transmitter or receiver. If power to the transmit board is lost, the receiver clocks (input and output) stop. The data outputs (RxOUT) retain the states they were in when the clocks stopped. When the receiver board loses power, the receiver inputs are shorted to $\mathrm{V}_{\mathrm{CC}}$ through an internal diode. Current is limited ( 5 mA per input) by the fixed current mode drivers, thus avoiding the potential for latchup when powering the device.


DS012888-26
FIGURE 20. Single-Ended and Differential Waveforms
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Pin Diagrams


Typical Application


| Absolute Maximum Ratings (Note 1) |  | DS90CR283 |  |  |  | 1.63W |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ |  | DS90CR284 |  |  |  | 1.61 W |
|  |  | Package Derating: |  |  |  |  |
| Distributors for availability and specifications. |  | DS90CR283 |  | $12.5 \mathrm{~mW} /{ }^{\circ} \mathrm{C}$ above $+25^{\circ} \mathrm{C}$ |  |  |
| Supply Voltage ( $\mathrm{V}_{\mathrm{CC}}$ ) | -0.3 V to +6 V | DS90CR284 |  | 12.4 m | / ${ }^{\circ} \mathrm{C}$ | e $+25^{\circ} \mathrm{C}$ |
| CMOS/TTL Input Voltage | -0.3 V to $\left(\mathrm{V}_{\mathrm{Cc}}+0.3 \mathrm{~V}\right)$ | This device does not meet 2000V ESD rating (Note 4) |  |  |  |  |
| CMOS/TTL Ouput Voltage | -0.3 V to $\left(\mathrm{V}_{\mathrm{Cc}}+0.3 \mathrm{~V}\right)$ | Recommended Operating |  |  |  |  |
| LVDS Receiver Input Voltage | -0.3 V to $\left(\mathrm{V}_{\mathrm{Cc}}+0.3 \mathrm{~V}\right)$ |  |  |  |  |  |
| LVDS Driver Output Voltage | -0.3 V to $\left(\mathrm{V}_{\mathrm{cc}}+0.3 \mathrm{~V}\right)$ | Conditions |  |  |  |  |
| LVDS Output Short Circuit |  |  | Min | Nom | Max | Units |
| Duration <br> Junction Temperature | Continuous $+150^{\circ} \mathrm{C}$ | Supply Voltage ( $\mathrm{V}_{\mathrm{CC}}$ ) | 4.75 | 5.0 | 5.25 | V |
| Junction Temperature | $+150^{\circ} \mathrm{C}$ | Operating Free Air |  |  |  |  |
| Storage Temperature Range | $-65^{\circ} \mathrm{C}$ to $+150^{\circ} \mathrm{C}$ | Temperature ( $\mathrm{T}_{\mathrm{A}}$ ) | -10 | +25 | +70 | ${ }^{\circ} \mathrm{C}$ |
| Lead Temperature (Soldering, 4 sec .) | $+260^{\circ} \mathrm{C}$ | Receiver Input Range | 0 |  | 2.4 | V |
| Maximum Package Power Dissipation @+25 ${ }^{\circ} \mathrm{C}$ MTD56(TSSOP) Package: |  | Supply Noise Voltage $\left(\mathrm{V}_{\mathrm{cc}}\right)$ |  |  |  | $\mathrm{mV} \mathrm{P}-\mathrm{P}$ |

## Electrical Characteristics

Over recommended operating supply and temperature ranges unless otherwise specified

| Symbol | Parameter | Conditions |  | Min | Typ | Max | Units |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| CMOS/TTL DC SPECIFICATIONS |  |  |  |  |  |  |  |
| $\mathrm{V}_{\mathrm{IH}}$ | High Level Input Voltage |  |  | 2.0 |  | $\mathrm{V}_{\mathrm{Cc}}$ | V |
| $\mathrm{V}_{\text {IL }}$ | Low Level Input Voltage |  |  | GND |  | 0.8 | V |
| $\mathrm{V}_{\mathrm{OH}}$ | High Level Output Voltage | $\mathrm{I}_{\mathrm{OH}}=-0.4 \mathrm{~mA}$ |  | 3.8 | 4.9 |  | V |
| $\mathrm{V}_{\mathrm{OL}}$ | Low Level Output Voltage | $\mathrm{I}_{\mathrm{OL}}=2 \mathrm{~mA}$ |  |  | 0.1 | 0.3 | V |
| $\mathrm{V}_{\mathrm{CL}}$ | Input Clamp Voltage | $\mathrm{I}_{\mathrm{CL}}=-18 \mathrm{~mA}$ |  |  | -0.79 | -1.5 | V |
| $\mathrm{I}_{\mathrm{IN}}$ | Input Current | $\mathrm{V}_{\mathrm{IN}}=\mathrm{V}_{\mathrm{CC}}$, GND, 2.5 V or | 0.4V |  | $\pm 5.1$ | $\pm 10$ | $\mu \mathrm{A}$ |
| $\mathrm{l}_{\mathrm{OS}}$ | Output Short Circuit Current | $\mathrm{V}_{\text {OUT }}=0 \mathrm{~V}$ |  |  |  | -120 | mA |
| LVDS DRIVER DC SPECIFICATIONS |  |  |  |  |  |  |  |
| $\mathrm{V}_{\text {OD }}$ | Differential Output Voltage | $\mathrm{R}_{\mathrm{L}}=100 \Omega$ |  | 250 | 290 | 450 | mV |
| $\Delta \mathrm{V}_{\mathrm{OD}}$ | Change in $\mathrm{V}_{\mathrm{OD}}$ between Complementary Output States |  |  |  |  | 35 | mV |
| $\mathrm{V}_{\text {OS }}$ | Offset Voltage |  |  | 1.1 | 1.25 | 1.375 | V |
| $\Delta \mathrm{V}_{\text {OS }}$ | Change in Magnitude of $\mathrm{V}_{\text {OS }}$ between Complementary Output States |  |  |  |  | 35 | mV |
| $\mathrm{I}_{\mathrm{Os}}$ | Output Short Circuit Current | $\mathrm{V}_{\text {OUT }}=\mathrm{OV}, \mathrm{R}_{\mathrm{L}}=100 \Omega$ |  |  | -2.9 | -5 | mA |
| $\mathrm{I}_{\mathrm{Oz}}$ | Output TRI-STATE® ${ }^{\text {® }}$ Current | $\overline{\text { Power Down }}=0 \mathrm{~V}, \mathrm{~V}_{\text {Out }}$ | OV or $\mathrm{V}_{\mathrm{cc}}$ |  | $\pm 1$ | $\pm 10$ | $\mu \mathrm{A}$ |
| LVDS RECEIVER DC SPECIFICATIONS |  |  |  |  |  |  |  |
| $\mathrm{V}_{\text {TH }}$ | Differential Input High Threshold | $\mathrm{V}_{\mathrm{CM}}=+1.2 \mathrm{~V}$ |  |  |  | +100 | mV |
| $\mathrm{V}_{\mathrm{TL}}$ | Differential Input Low Threshold |  |  | -100 |  |  | mV |
| $\mathrm{I}_{\mathrm{IN}}$ | Input Current | $\mathrm{V}_{\mathrm{IN}}=+2.4 \mathrm{~V}, \mathrm{~V}_{\mathrm{CC}}=5.0 \mathrm{~V}$ |  |  |  | $\pm 10$ | $\mu \mathrm{A}$ |
|  |  | $\mathrm{V}_{\mathrm{IN}}=0 \mathrm{~V}, \mathrm{~V}_{\mathrm{CC}}=5.0 \mathrm{~V}$ |  |  |  | $\pm 10$ | $\mu \mathrm{A}$ |
| TRANSMITTER SUPPLY CURRENT |  |  |  |  |  |  |  |
| $\mathrm{I}_{\text {cctw }}$ | Transmitter Supply Current, Worst Case | $\mathrm{R}_{\mathrm{L}}=100 \Omega, \mathrm{C}_{\mathrm{L}}=5 \mathrm{pF},$ <br> Worst Case Pattern (Figures 1, 2) | $\mathrm{f}=32.5 \mathrm{MHz}$ |  | 49 | 63 | mA |
|  |  |  | $\mathrm{f}=37.5 \mathrm{MHz}$ |  | 51 | 64 | mA |
|  |  |  | $\mathrm{f}=66 \mathrm{MHz}$ |  | 70 | 84 | mA |
| $\mathrm{I}_{\text {CCTz }}$ | Transmitter Supply Current, Power Down | Power Down $=$ Low Driver Outputs in TRI-ST under Power Down Mode |  |  | 1 | 10 | $\mu \mathrm{A}$ |

## Electrical Characteristics <br> (Continued)

Over recommended operating supply and temperature ranges unless otherwise specified

| Symbol | Parameter | Conditions |  | Min | Typ | Max | Units |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| RECEIVER SUPPLY CURRENT |  |  |  |  |  |  |  |
| $\mathrm{I}_{\text {CCRW }}$ | Receiver Supply Current, Worst Case | $\mathrm{C}_{\mathrm{L}}=8 \mathrm{pF},$ <br> Worst Case Pattern <br> (Figures 1, 3) | $\mathrm{f}=32.5 \mathrm{MHz}$ |  | 64 | 77 | mA |
|  |  |  | $\mathrm{f}=37.5 \mathrm{MHz}$ |  | 70 | 85 | mA |
|  |  |  | $\mathrm{f}=66 \mathrm{MHz}$ |  | 110 | 140 | mA |
| $\mathrm{I}_{\text {CCRZ }}$ | Receiver Supply Current, Power Down | Power Down = Low Receiver Outputs in during Power Down | us State |  | 1 | 10 | $\mu \mathrm{A}$ |

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the device should be operated at these limits. The tables of "Electrical Characteristics" specify conditions for device operation.
Note 2: Typical values are given for $\mathrm{V}_{\mathrm{CC}}=5.0 \mathrm{~V}$ and $\mathrm{T}_{\mathrm{A}}=+25^{\circ} \mathrm{C}$.
Note 3: Current into device pins is defined as positive. Current out of device pins is defined as negative. Voltages are referenced to ground unless otherwise speci-
fied (except $V_{O D}$ and $\Delta V_{O D}$ ).
Note 4: ESD Rating: HBM ( $1.5 \mathrm{k} \Omega, 100 \mathrm{pF}$ )
PLL VCC $\geq 1000 \mathrm{~V}$
All other pins $\geq 2000 \mathrm{~V}$
EIAJ $(0 \Omega, 200 \mathrm{pF}) \geq 150 \mathrm{~V}$
Note 5: $\mathrm{V}_{\mathrm{OS}}$ previously referred as $\mathrm{V}_{\mathrm{CM}}$.

## Transmitter Switching Characteristics

Over recommended operating supply and temperature ranges unless otherwise specified

| Symbol | Parameter |  | Min | Typ | Max | Units |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| LLHT | LVDS Low-to-High Transition Time (Figure 2) |  |  | 0.75 | 1.5 | ns |
| LHLT | LVDS High-to-Low Transition Time (Figure 2) |  |  | 0.75 | 1.5 | ns |
| TCIT | TxCLK IN Transition Time (Figure 4) |  |  |  | 8 | ns |
| TCCS | TxOUT Channel-to-Channel Skew (Note 6) (Figure 5) |  |  |  | 350 | ps |
| TPPos0 | Transmitter Output Pulse Position for Bit 0 (Figure 16) | $\mathrm{f}=66 \mathrm{MHz}$ | -0.30 | 0 | 0.30 | ns |
| TPPos1 | Transmitter Output Pulse Position for Bit 1 |  | 1.70 | (1/7) $\mathrm{T}_{\text {clk }}$ | 2.50 | ns |
| TPPos2 | Transmitter Output Pulse Position for Bit 2 |  | 3.60 | (2/7) $\mathrm{T}_{\text {clk }}$ | 4.50 | ns |
| TPPos3 | Transmitter Output Pulse Position for Bit 3 |  | 5.90 | $(3 / 7) \mathrm{T}_{\mathrm{clk}}$ | 6.75 | ns |
| TPPos4 | Transmitter Output Pulse Position for Bit 4 |  | 8.30 | (4/7) $\mathrm{T}_{\text {clk }}$ | 9.00 | ns |
| TPPos5 | Transmitter Output Pulse Position for Bit 5 |  | 10.40 | (5/7) $\mathrm{T}_{\text {clk }}$ | 11.10 | ns |
| TPPos6 | Transmitter Output Pulse Position for Bit 6 |  | 12.70 | (6/7) $\mathrm{T}_{\text {clk }}$ | 13.40 |  |
| TCIP | TxCLK IN Period (Figure 6) |  | 15 | T | 50 | ns |
| TCIH | TxCLK IN High Time (Figure 6) |  | 0.35T | 0.5 T | 0.65T | ns |
| TCIL | TxCLK IN Low Time (Figure 6) |  | 0.35T | 0.5 T | 0.65T | ns |
| TSTC | TxIN Setup to TxCLK IN (Figure 6) |  | 5 | 3.5 |  | ns |
| THTC | TxIN Hold to TxCLK IN (Figure 6) |  | 2.5 | 1.5 |  | ns |
| TCCD | TxCLK IN to TxCLK OUT Delay @ $25^{\circ} \mathrm{C}$, $\mathrm{V}_{\mathrm{CC}}=5.0 \mathrm{~V}$ (Figure 8) |  | 3.5 |  | 8.5 | ns |
| TPLLS | Transmitter Phase Lock Loop Set (Figure 10) |  |  |  | 10 | ms |
| TPDD | Transmitter Power Down Delay (Figure 14) |  |  |  | 100 | ns |

Note 6: This limit based on bench characterization

## Receiver Switching Characteristics

Over recommended operating supply and temperature ranges unless otherwise specified

| Symbol | Parameter |  | Min | Typ | Max | Units |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| CLHT | CMOS/TTL Low-to-High Transition Time (Figure 3) |  |  | 2.5 | 4.0 | ns |
| CHLT | CMOS/TTL High-to-Low Transition Time (Figure 3) |  |  | 2.0 | 4.0 | ns |
| RSKM | RxIN Skew Margin (Note 7),$\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C} \text { (Figure 17) }$ | $\mathrm{f}=40 \mathrm{MHz}$ | 700 |  |  | ps |
|  |  | $\mathrm{f}=66 \mathrm{MHz}$ | 600 |  |  | ps |
| RCOP | RxCLK OUT Period (Figure 7) |  | 15 | T | 50 | ns |
| RCOH | RxCLK OUT High Time (Figure 7) | $\mathrm{f}=40 \mathrm{MHz}$ | 6 |  |  | ns |
|  |  | $\mathrm{f}=66 \mathrm{MHz}$ | 4.3 | 5 |  | ns |
| RCOL | RxCLK OUT Low Time (Figure 7) | $\mathrm{f}=40 \mathrm{MHz}$ | 10.5 |  |  | ns |
|  |  | $\mathrm{f}=66 \mathrm{MHz}$ | 7.0 | 9 |  | ns |
| RSRC | RxOUT Setup to RxCLK OUT (Figure 7) | $\mathrm{f}=40 \mathrm{MHz}$ | 4.5 |  |  | ns |
|  |  | $\mathrm{f}=66 \mathrm{MHz}$ | 2.5 | 4.2 |  | ns |
| RHRC | RxOUT Hold to RxCLK OUT (Figure 7) | $\mathrm{f}=40 \mathrm{MHz}$ | 6.5 |  |  | ns |
|  |  | $\mathrm{f}=66 \mathrm{MHz}$ | 4 | 5.2 |  | ns |
| RCCD | RxCLK IN to RxCLK OUT Delay @ $25^{\circ} \mathrm{C}$, $\mathrm{V}_{\mathrm{CC}}=5.0 \mathrm{~V}$ (Figure 9) |  | 6.4 |  | 10.7 | ns |
| RPLLS | Receiver Phase Lock Loop Set (Figure 11) |  |  |  | 10 | ms |
| RPDD | Receiver Power Down Delay (Figure 11) |  |  |  | 1 | $\mu \mathrm{s}$ |

Note 7: Receiver Skew Margin is defined as the valid data sampling region at the receiver inputs. This margin takes into account transmitter output skew (TCCS) and the setup and hold time (internal data sampling window), allowing for LVDS cable skew dependent on type/length and source clock (TxCLK IN) jitter
RSKM $\geq$ cable skew (type, length) + source clock jitter (cycle to cycle)

## AC Timing Diagrams




FIGURE 2. DS90CR283 (Transmitter) LVDS Output Load and Transition Timing

## AC Timing Diagrams (Continued)



FIGURE 3. DS90CR284 (Receiver) CMOS/TTL Output Load and Transition Timing


FIGURE 4. DS90CR283 (Transmitter) Input Clock Transition Time
DS012889-7


DS012889-8
Note 8: Measurements at $V_{\text {diff }}=0 \mathrm{~V}$
Note 9: TCCS measured between earliest and latest initial LVDS edges.
Note 10: TxCLK OUT Differential Low $\rightarrow$ High Edge
FIGURE 5. DS90CR283 (Transmitter) Channel-to-Channel Skew


FIGURE 6. DS90CR283 (Transmitter) Setup/Hold and High/Low Times

## AC Timing Diagrams (Continued)



FIGURE 7. DS90CR284 (Receiver) Setup/Hold and High/Low Times


FIGURE 8. DS90CR283 (Transmitter) Clock In to Clock Out Delay


FIGURE 9. DS90CR284 (Receiver) Clock In to Clock Out Delay

FIGURE 10. DS90CR283 (Transmitter) Phase Lock Loop Set Time

## AC Timing Diagrams (Continued)



FIGURE 11. DS90CR284 (Receiver) Phase Lock Loop Set Time


FIGURE 12. Seven Bits of LVDS in One Clock Cycle


DS012889-16
FIGURE 13. 28 Parallel TTL Data Inputs Mapped to LVDS Outputs (DS90CR283)


FIGURE 14. Transmitter Powerdown Delay

## AC Timing Diagrams (Continued)



DS012889-18


FIGURE 16. Transmitter LVDS Output Pulse Position Measurement


SW-Setup and Hold Time (Internal data sampling window)
TCCS-Transmitter Output Skew
RSKM $\geq$ Cable Skew (type, length) + Source Clock Jitter (cycle to cycle)
Cable Skew-typically 10 ps-40 ps per foot.
FIGURE 17. Receiver LVDS Input Skew Margin

DS90CR283 Pin Description—Channel Link Transmitter

| Pin Name | I/O | No. | Description |
| :--- | :---: | :---: | :--- |
| TxIN | I | 28 | TTL Level inputs |
| TxOUT + | O | 4 | Positive LVDS differential data output |
| TxOUT- | O | 4 | Negative LVDS differential data output |
| TxCLK IN | I | 1 | TTL level clock input. The rising edge acts as data strobe |
| TxCLK OUT + | O | 1 | Positive LVDS differential clock output |
| TxCLK OUT- | O | 1 | Negative LVDS differential clock output |
| PWR DOWN | I | 1 | TTL level input. Assertion (low input) TRI-STATES the outputs, ensuring low current at power <br> down |
| $\mathrm{V}_{\mathrm{CC}}$ | I | 4 | Power supply pins for TTL inputs |
| GND | I | 5 | Ground pins for TTL inputs |
| PLL $V_{\text {CC }}$ | 1 | 1 | Power supply pin for PLL |
| PLL GND | 1 | 2 | Ground pins for PLL |
| LVDS $V_{\text {CC }}$ | I | 1 | Power supply pin for LVDS outputs |
| LVDS GND | I | 3 | Ground pins for LVDS outputs |

DS90CR284 Pin Description—Channel Link Receiver

| Pin Name | I/O | No. | Description |
| :---: | :---: | :---: | :---: |
| Rxin + | 1 | 4 | Positive LVDS differential data inputs |
| RxiN- | 1 | 4 | Negative LVDS differential data inputs |
| RxOUT | 0 | 28 | TTL level outputs |
| RxCLK IN+ | I | 1 | Positive LVDS differential clock input |
| RxCLK IN- | 1 | 1 | Negative LVDS differential clock input |
| RxCLK OUT | 0 | 1 | TTL level clock output. The rising edge acts as data strobe |
| PWR DOWN | 1 | 1 | TTL level input. Assertion (low input) maintains the receiver outputs in the previous state |
| $\mathrm{V}_{\mathrm{cc}}$ | 1 | 4 | Power supply pins for TTL outputs |
| GND | 1 | 5 | Ground pins for TTL outputs |
| PLL V ${ }_{\text {cc }}$ | 1 | 1 | Power supply for PLL |
| PLL GND | I | 2 | Ground pin for PLL |
| LVDS $\mathrm{V}_{\mathrm{cc}}$ | 1 | 1 | Power supply pin for LVDS inputs |
| LVDS GND | 1 | 3 | Ground pins for LVDS inputs |

## Applications Information

The Channel Link devices are intended to be used in a wide variety of data transmission applications. Depending upon the application the interconnecting media may vary. For example, for lower data rate (clock rate) and shorter cable lengths $(<2 m)$, the media electrical performance is less critical. For higher speed/long distance applications the media's performance becomes more critical. Certain cable constructions provide tighter skew (matched electrical length between the conductors and pairs). Twin-coax for example, has been demonstrated at distances as great as 5 meters and with the maximum data transfer of $1.848 \mathrm{Gbit} / \mathrm{s}$. Additional applications information can be found in the following Na tional Interface Application Notes:

| AN $=$ \#\#\#\# | Topic |
| :--- | :--- |
| AN-1041 | Introduction to Channel Link |
| AN-1035 | PCB Design Guidelines for LVDS and <br>  <br> Link Devices |
| AN-806 | Transmission Line Theory |


| AN $=$ \#\#\#\# | Topic |
| :--- | :--- |
| AN-905 | Transmission Line Calculations and <br> Differential Impedance <br> Cable Information |
| AN-916 | Can |

CABLES: A cable interface between the transmitter and receiver needs to support the differential LVDS pairs. The 21-bit CHANNEL LINK chipset (DS90CR213/214) requires four pairs of signal wires and the 28 -bit CHANNEL LINK chipset (DS90CR283/284) requires five pairs of signal wires. The ideal cable/connector interface would have a constant $100 \Omega$ differential impedance throughout the path. It is also recommended that cable skew remain below 350 ps (@ 66 MHz clock rate) to maintain a sufficient data sampling window at the receiver.
In addition to the four or five cable pairs that carry data and clock, it is recommended to provide at least one additional conductor (or pair) which connects ground between the transmitter and receiver. This low impedance ground provides a common mode return path for the two devices. Some of the more commonly used cable types for point-to-point ap-

## Applications Information (Continued)

plications include flat ribbon, flex, twisted pair and Twin-Coax. All are available in a variety of configurations and options. Flat ribbon cable, flex and twisted pair generally perform well in short point-to-point applications while Twin-Coax is good for short and long applications. When using ribbon cable, it is recommended to place a ground line between each differential pair to act as a barrier to noise coupling between adjacent pairs. For Twin-Coax cable applications, it is recommended to utilize a shield on each cable pair. All extended point-to-point applications should also employ an overall shield surrounding all cable pairs regardless of the cable type. This overall shield results in improved transmission parameters such as faster attainable speeds, longer distances between transmitter and receiver and reduced problems associated with EMS or EMI.
The high-speed transport of LVDS signals has been demonstrated on several types of cables with excellent results. However, the best overall performance has been seen when using Twin-Coax cable. Twin-Coax has very low cable skew and EMI due to its construction and double shielding. All of the design considerations discussed here and listed in the supplemental application notes provide the subsystem communications designer with many useful guidelines. It is recommended that the designer assess the tradeoffs of each application thoroughly to arrive at a reliable and economical cable solution.
BOARD LAYOUT: To obtain the maximum benefit from the noise and EMI reductions of LVDS, attention should be paid to the layout of differential lines. Lines of a differential pair should always be adjacent to eliminate noise interference from other signals and take full advantage of the noise canceling of the differential signals. The board designer should also try to maintain equal length on signal traces for a given differential pair. As with any high speed design, the impedance discontinuities should be limited (reduce the numbers of vias and no 90 degree angles on traces). Any discontinuities which do occur on one signal line should be mirrored in the other line of the differential pair. Care should be taken to
ensure that the differential trace impedance match the differential impedance of the selected physical media (this impedance should also match the value of the termination resistor that is connected across the differential pair at the receiver's input). Finally, the location of the CHANNEL LINK TxOUT/ RxIN pins should be as close as possible to the board edge so as to eliminate excessive pcb runs. All of these considerations will limit reflections and crosstalk which adversely effect high frequency performance and EMI.
UNUSED INPUTS: All unused inputs at the TxIN inputs of the transmitter must be tied to ground. All unused outputs at the RxOUT outputs of the receiver must then be left floating.
TERMINATION: Use of current mode drivers requires a terminating resistor across the receiver inputs. The CHANNEL LINK chipset will normally require a single $100 \Omega$ resistor between the true and complement lines on each differential pair of the receiver input. The actual value of the termination resistor should be selected to match the differential mode characteristic impedance ( $90 \Omega$ to $120 \Omega$ typical) of the cable. Figure 18 shows an example. No additional pull-up or pull-down resistors are necessary as with some other differential technologies such as PECL. Surface mount resistors are recommended to avoid the additional inductance that accompanies leaded resistors. These resistors should be placed as close as possible to the receiver input pins to reduce stubs and effectively terminate the differential lines.
DECOUPLING CAPACITORS: Bypassing capacitors are needed to reduce the impact of switching noise which could limit performance. For a conservative approach three parallel-connected decoupling capacitors (Multi-Layered Ceramic type in surface mount form factor) between each $\mathrm{V}_{\mathrm{CC}}$ and the ground plane(s) are recommended. The three capacitor values are $0.1 \mu \mathrm{~F}, 0.01 \mu \mathrm{~F}$ and $0.001 \mu \mathrm{~F}$. An example is shown in Figure 19. The designer should employ wide traces for power and ground and ensure each capacitor has its own via to the ground plane. If board space is limiting the number of bypass capacitors, the PLL $V_{C c}$ should receive the most filtering/bypassing. Next would be the LVDS $\mathrm{V}_{\mathrm{CC}}$ pins and finally the logic $\mathrm{V}_{\mathrm{CC}}$ pins.


FIGURE 18. LVDS Serialized Link Termination

## Applications Information (Continued)



FIGURE 19. CHANNEL LINK Decoupling Configuration
CLOCK JITTER: The CHANNEL LINK devices employ a PLL to generate and recover the clock transmitted across the LVDS interface. The width of each bit in the serialized LVDS data stream is one-seventh the clock period. For example, a 66 MHz clock has a period of 15 ns which results in a data bit width of 2.16 ns . Differential skew ( $\Delta \mathrm{t}$ within one differential pair), interconnect skew ( $\Delta \mathrm{t}$ of one differential pair to another) and clock jitter will all reduce the available window for sampling the LVDS serial data streams. Care must be taken to ensure that the clock input to the transmitter be a clean low noise signal. Individual bypassing of each $\mathrm{V}_{\mathrm{CC}}$ to ground will minimize the noise passed on to the PLL, thus creating a
low jitter LVDS clock. These measures provide more margin for channel-to-channel skew and interconnect skew as a part of the overall jitter/skew budget.
COMMON MODE vs. DIFFERENTIAL MODE NOISE MARGIN: The typical signal swing for LVDS is 300 mV centered at +1.2 V . The CHANNEL LINK receiver supports a 100 mV threshold therefore providing approximately 200 mV of differential noise margin. Common mode protection is of more importance to the system's operation due to the differential data transmission. LVDS supports an input voltage range of Ground to +2.4 V . This allows for a $\pm 1.0 \mathrm{~V}$ shifting of the center point due to ground potential differences and common mode noise.
POWER SEQUENCING AND POWERDOWN MODE: Outputs of the CHANNEL LINK transmitter remain in TRI-STATE until the power supply reaches 3V. Clock and data outputs will begin to toggle 10 ms after $\mathrm{V}_{\mathrm{Cc}}$ has reached 4.5 V and the Powerdown pin is above 2V. Either device may be placed into a powerdown mode at any time by asserting the Powerdown pin (active low). Total power dissipation for each device will decrease to $5 \mu \mathrm{~W}$ (typical).
The CHANNEL LINK chipset is designed to protect itself from accidental loss of power to either the transmitter or receiver. If power to the transmit board is lost, the receiver clocks (input and output) stop. The data outputs (RxOUT) retain the states they were in when the clocks stopped. When the receiver board loses power, the receiver inputs are shorted to $\mathrm{V}_{\mathrm{CC}}$ through an internal diode. Current is limited ( 5 mA per input) by the fixed current mode drivers, thus avoiding the potential for latchup when powering the device.


DS012889-26
FIGURE 20. Single-Ended and Differential Waveforms
$\qquad$ THIS PAGE IS IGNORED IN THE DATABOOK


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Absolute Maximum Ratings (Note 2)
If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

| Supply Voltage ( $\mathrm{V}_{\mathrm{cc}}$ ) | -0.3 V to +6 V |
| :--- | ---: |
| Input Voltage (DI) | -0.3 V to V |
| Voltage (DO $\pm$ | -0.3 V to $(\mathrm{V}$ (cc $+0.3 \mathrm{~V})$ |

Maximum Package Power Dissipation @ $+25^{\circ} \mathrm{C}$
M Package 1190 mW

Derate M Package $\quad 9.5 \mathrm{~mW} / /^{\circ} \mathrm{C}$ above $+25^{\circ} \mathrm{C}$
Storage Temperature Range $-65^{\circ} \mathrm{C}$ to $+150^{\circ} \mathrm{C}$

| Lead Temperature Range |  |
| :--- | ---: |
| $\quad$ Soldering (4 Sec.) | $+260^{\circ} \mathrm{C}$ |
| ESD Rating |  |
| $\quad(\mathrm{HBM} 1.5 \mathrm{k} \Omega, 100 \mathrm{pF})($ Note 5$)$ | $\geq 4.5 \mathrm{kV}$ |

## Recommended Operating Conditions

|  | Min | Typ | Max | Units |
| :--- | :---: | :---: | :---: | :---: |
| Supply Voltage $\left(\mathrm{V}_{\mathrm{CC}}\right)$ | 3.0 | 3.3 | 3.6 | V |
| Temperature $\left(\mathrm{T}_{\mathrm{A}}\right)$ | 0 | 25 | 70 | ${ }^{\circ} \mathrm{C}$ |

Electrical Characteristics (Notes 3, 4, and 8)
Over Supply Voltage and Operating Temperature ranges, unless otherwise specified

| Symbol | Parameter | Conditions |  | Pin | Min | Typ | Max | Units |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| DIFFERENTIAL DRIVER CHARACTERISTICS |  |  |  |  |  |  |  |  |
| $\mathrm{V}_{\text {OD }}$ | Output Differential Voltage | $\mathrm{R}_{\mathrm{L}}=100 \Omega$ <br> (Figure 1) |  | $\begin{aligned} & \text { DO+, } \\ & \text { DO- } \end{aligned}$ | 250 | 340 | 450 | mV |
| $\Delta \mathrm{V}_{\text {OD }}$ | $\mathrm{V}_{\text {OD }}$ Magnitude Change |  |  | 0 | 10 | 35 | mV |
| $\mathrm{V}_{\mathrm{OH}}$ | Output High Voltage |  |  |  | 1.43 | 1.6 | V |
| $\mathrm{V}_{\text {OL }}$ | Output Low Voltage |  |  | 0.9 | 1.09 |  | V |
| $\mathrm{V}_{\text {OS }}$ | Offset Voltage |  |  | 0.9 | 1.25 | 1.6 | V |
| $\Delta \mathrm{V}_{\text {OS }}$ | Offset Magnitude Change |  |  | 0 | 5 | 25 | mV |
| $\mathrm{l}_{\text {OzD }}$ | TRI-STATE® Leakage | $\mathrm{V}_{\mathrm{O}}=\mathrm{V}_{\mathrm{CC}}$ or GND |  |  | 0 | $\pm 1$ | $\pm 10$ | $\mu \mathrm{A}$ |
| $\mathrm{l}_{\text {OXD }}$ | Power-off Leakage | $\mathrm{V}_{\mathrm{O}}=\mathrm{V}_{\mathrm{CC}}$ or GND |  |  | 0 | $\pm 1$ | $\pm 10$ | $\mu \mathrm{A}$ |
| $\mathrm{l}_{\text {OSD }}$ | Output Short Circuit Current |  |  |  |  | -4 | -6 | mA |
| $\mathrm{V}_{\mathrm{IH}}$ | Input High Voltage |  |  |  | DI | 2.0 |  | $\mathrm{V}_{\mathrm{CC}}$ | V |
| $\mathrm{V}_{\text {IL }}$ | Input Low Voltage |  |  |  |  | GND |  | 0.8 | V |
| $\mathrm{I}_{\mathrm{IH}}$ | Input High Current | $\begin{aligned} & \mathrm{V}_{\mathrm{IN}}=5.5 \mathrm{~V}, 3.3 \mathrm{~V}, \text { or } 2.4 \mathrm{~V} \\ & \mathrm{~V}_{\mathrm{IN}}=\mathrm{GND} \text { or } 0.5 \mathrm{~V} \end{aligned}$ |  |  |  |  | $\pm 1$ | $\pm 10$ | $\mu \mathrm{A}$ |
| $\mathrm{I}_{\text {IL }}$ | Input Low Current |  |  |  |  | $\pm 1$ | $\pm 10$ | $\mu \mathrm{A}$ |
| $\mathrm{V}_{\mathrm{CL}}$ | Input Clamp Voltage | $\mathrm{I}_{\mathrm{CL}}=-18 \mathrm{~mA}$ |  |  |  | -1.5 | -0.8 |  | V |
| $\mathrm{I}_{\mathrm{cc}}$ | Power Supply Current | No Load | $\begin{aligned} & \mathrm{V}_{\text {IN }}=\mathrm{V}_{\mathrm{CC}} \text { or } \\ & \text { GND } \end{aligned}$ |  | $\mathrm{V}_{\mathrm{cc}}$ |  | 1 | 4 | mA |
|  |  | $\mathrm{R}_{\mathrm{L}}=100 \Omega$ |  |  |  | 1 | 7 | mA |

## Switching Characteristics (Note 6)

Over Supply Voltage and Operating Temperature Ranges, unless otherwise specified.

| Symbol | Parameter | Conditions | Min | Typ | Max | Units |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| DIFFERENTIAL DRIVER CHARACTERISTICS |  |  |  |  |  |  |
| $\mathrm{t}_{\text {PHLD }}$ | Differential Propagation Delay High to Low | $\mathrm{R}_{\mathrm{L}}=100 \Omega, \mathrm{C}_{\mathrm{L}}=5 \mathrm{pF}$ <br> (Figures 2, 3) | 1.5 | 3.4 | 6 | ns |
| $\mathrm{t}_{\text {PLHD }}$ | Differential Propagation Delay Low to High |  | 1.5 | 3.5 | 6 | ns |
| $\mathrm{t}_{\text {SKD }}$ | Differential Skew, \|t ${ }_{\text {PHLD }}-\mathrm{t}_{\text {PLHD }} \mid$ |  | 0 | 0.1 | 1.9 | ns |
| $\mathrm{t}_{\text {TLH }}$ | Transition Low to High Time |  | 0 | 1 | 3 | ns |
| $\mathrm{t}_{\text {THL }}$ | Transition High to Low Time |  | 0 | 1 | 3 | ns |

Note 2: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" specifies conditions of device operation.
Note 3: Current into device pins is defined as positive. Current out of device pins is defined as negative. All voltages are referenced to ground except $V_{O D}$
Note 4: All typicals are given for: $\mathrm{V}_{\mathrm{CC}}=+3.3 \mathrm{~V}$ and $\mathrm{T}_{\mathrm{A}}=+25^{\circ} \mathrm{C}$.
Note 5: ESD Rating: HBM $(1.5 \mathrm{k} \Omega, 100 \mathrm{pF}) \geq 4.5 \mathrm{kV}$
Note 6: $C_{L}$ includes probe and fixture capacitance.
Note 7: Generator waveform for all tests unless otherwise specified: $\mathrm{f}=1 \mathrm{MHz}, \mathrm{Zo}=50 \Omega$, $\mathrm{tr} \leq 6 \mathrm{~ns}, \mathrm{tf} \leq 6 \mathrm{~ns}(10 \%-90 \%)$.
Note 8: The DS90LV017 is a current mode device and only function with datasheet specification when a resistive load is applied to the drivers outputs.

## Parameter Measurement Information



FIGURE 1. Differential Driver DC Test Circuit


DS012900-3

DS012900-4
FIGURE 2. Differential Driver Propagation Delay and Transition Time Test Circuit


FIGURE 3. Differential Driver Propagation Delay and Transition Time Waveforms

## Application Information

Truth Table

| Input/Output |  |  |
| :---: | :---: | :---: |
| DI | DO+ | DO- |
| L | L | H |
| H | H | L |
| $2>$ DI $>0.8$ | X | X |

$H=$ Logic high level
$L$ = Logic low level
X = indeterminant

TABLE 1. Device Pin Descriptions

| Pin \# | Name | Description |
| :---: | :--- | :--- |
| 1 | DI | TTL/CMOS driver input pins |
| 8 | DO+ | Noninverting driver output pin |
| 7 | DO- | Inverting driver output pin |
| 3 | GND | Ground pin |
| 2 | V $_{\text {CC }}$ | Positive power supply pin, +3.3 V <br> $\pm 0.3 \mathrm{~V}$ |

Physical Dimensions inches (millimeters)


Order Number DS90LV017M
NS Package Number M08A

## LIFE SUPPORT POLICY

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## Power Management

- Low Dropout Regulators
- Switch-Capacitor Converters and Controller
- Step-Down DC/DC Converters
- Boost/Flyback DC/DC Converters


## Low Dropout Regulators

- LP2981 Micropower, SOT, 100mA, Ultra LDO
- LP2982 Micropower, SOT, 50mA, Ultra LDO
- LP2986 Micropower, 200mA, Ultra LDO Fixed or Adjustable Voltage Regulator


Absolute Maximum Ratings (Note 1)
If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.
Storage Temperature Range $\quad-65^{\circ} \mathrm{C}$ to $+150^{\circ} \mathrm{C}$
Operating Junction Temperature Range $-40^{\circ} \mathrm{C}$ to $+125^{\circ} \mathrm{C}$
Lead Temperature (Soldering, 5 sec .)
ESD Rating (Note 2)
$260^{\circ} \mathrm{C}$ 2 kV
Power Dissipation (Note 3)
Internally Limited

| Input Supply Voltage (Survival) | -0.3 V to +16 V |
| :--- | ---: |
| Input Supply Voltage (Operating) | 2.1 V to +16 V |
| Shutdown Input Voltage (Survival) | -0.3 V to +16 V |
| Output Voltage (Survival, Note 4) | -0.3 V to +9 V | Short Circuit Protected Input-Output Voltage (Survival, Note 5) $\quad-0.3 \mathrm{~V}$ to +16 V

Electrical Characteristics Limits in standard typeface are for $T_{J}=25^{\circ} \mathrm{C}$, and limits in boldface type apply over the fulloperating temperature range. Unless otherwise specified: $\mathrm{V}_{I \mathrm{~N}}=\mathrm{V}_{\mathrm{O}(\mathrm{NOM})}+1 \mathrm{~V}, \mathrm{C}_{\mathrm{IN}}=1 \mu \mathrm{~F}, \mathrm{I}_{\mathrm{L}}=1 \mathrm{~mA}, \mathrm{C}_{\mathrm{OUT}}=4.7 \mu \mathrm{~F}$, $\mathrm{V}_{\text {ON/OFF }}=2 \mathrm{~V}$.

| Symbol | Parameter | Conditions | Typ | $\begin{aligned} & \text { LP2981AI-XX } \\ & \text { (Note 6) } \\ & \hline \end{aligned}$ |  | $\begin{aligned} & \text { LP2981I-XX } \\ & \text { (Note 6) } \\ & \hline \end{aligned}$ |  | Units |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  |  |  | Min | Max | Min | Max |  |
| $\mathrm{V}_{\mathrm{O}}$ | Output Voltage <br> (5.0V Versions) | $\mathrm{V}_{\text {IN }}=\mathrm{V}_{\mathrm{O}(\mathrm{NOM})}+1 \mathrm{~V}$ | 5.0 | 4.962 | 5.038 | 4.937 | 5.063 | V |
|  |  | $1 \mathrm{~mA}<\mathrm{I}_{\mathrm{L}}<100 \mathrm{~mA}$ | 5.0 | $\begin{gathered} 4.950 \\ \mathbf{4 . 8 7 5} \end{gathered}$ | $\begin{gathered} 5.050 \\ \mathbf{5 . 1 2 5} \end{gathered}$ | $\begin{gathered} 4.900 \\ \mathbf{4 . 8 2 5} \end{gathered}$ | $\begin{gathered} 5.100 \\ \mathbf{5 . 1 7 5} \end{gathered}$ |  |
|  | Output Voltage (3.3V Versions) | $\mathrm{V}_{\text {IN }}=\mathrm{V}_{\mathrm{O}(\mathrm{NOM})}+1 \mathrm{~V}$ | 3.3 | 3.275 | 3.325 | 3.259 | 3.341 |  |
|  |  | $1 \mathrm{~mA}<\mathrm{I}_{\mathrm{L}}<100 \mathrm{~mA}$ | 3.3 | $\begin{gathered} 3.267 \\ \mathbf{3 . 2 1 7} \end{gathered}$ | $\begin{gathered} 3.333 \\ \mathbf{3 . 3 8 3} \end{gathered}$ | $\begin{gathered} 3.234 \\ \mathbf{3 . 1 8 4} \end{gathered}$ | $\begin{gathered} 3.366 \\ \mathbf{3 . 4 1 6} \end{gathered}$ |  |
|  | Output Voltage <br> (3.0V Versions) | $\mathrm{V}_{\text {IN }}=\mathrm{V}_{\mathrm{O}(\mathrm{NOM})}+1 \mathrm{~V}$ | 3.0 | 2.977 | 3.023 | 2.962 | 3.038 |  |
|  |  | $1 \mathrm{~mA}<\mathrm{I}_{\mathrm{L}}<100 \mathrm{~mA}$ | 3.0 | $\begin{gathered} 2.970 \\ \mathbf{2 . 9 2 5} \end{gathered}$ | $\begin{gathered} 3.030 \\ \mathbf{3 . 0 7 5} \\ \hline \end{gathered}$ | $\begin{gathered} 2.940 \\ \mathbf{2 . 8 9 5} \end{gathered}$ | $\begin{gathered} 3.060 \\ \mathbf{3 . 1 0 5} \end{gathered}$ |  |
| $\frac{\Delta \mathrm{V}_{\mathrm{O}}}{\Delta \mathrm{~V}_{\mathrm{IN}}}$ | Output Voltage Line Regulation | $\begin{gathered} \mathrm{V}_{\mathrm{O}(\mathrm{NOM})}+1 \mathrm{~V} \\ \leq \mathrm{V}_{\text {IN }} \leq 16 \mathrm{~V} \end{gathered}$ | 0.007 |  | $\begin{gathered} 0.014 \\ \mathbf{0 . 0 3 2} \end{gathered}$ |  | $\begin{gathered} 0.014 \\ \mathbf{0 . 0 3 2} \end{gathered}$ | \%/V |
| $\mathrm{V}_{\text {IN }}-\mathrm{V}_{\mathrm{O}}$ | Dropout Voltage (Note 7) | $\mathrm{I}_{\mathrm{L}}=0$ | 1 |  | $\begin{aligned} & 3 \\ & 5 \end{aligned}$ |  | $\begin{aligned} & 3 \\ & 5 \end{aligned}$ | mV |
|  |  | $\mathrm{I}_{\mathrm{L}}=1 \mathrm{~mA}$ | 7 |  | $\begin{array}{r} 10 \\ \mathbf{1 5} \\ \hline \end{array}$ |  | $\begin{array}{r} 10 \\ \mathbf{1 5} \\ \hline \end{array}$ |  |
|  |  | $\mathrm{I}_{\mathrm{L}}=25 \mathrm{~mA}$ | 70 |  | $\begin{aligned} & 100 \\ & \mathbf{1 5 0} \end{aligned}$ |  | $\begin{aligned} & 100 \\ & \mathbf{1 5 0} \end{aligned}$ |  |
|  |  | $\mathrm{I}_{\mathrm{L}}=100 \mathrm{~mA}$ | 200 |  | $\begin{array}{r} 250 \\ \mathbf{3 7 5} \\ \hline \end{array}$ |  | $\begin{array}{r} 250 \\ \mathbf{3 7 5} \\ \hline \end{array}$ |  |
| $\mathrm{I}_{\mathrm{GND}}$ | Ground Pin Current | $\mathrm{I}_{\mathrm{L}}=0$ | 65 |  | $\begin{gathered} 95 \\ 125 \end{gathered}$ |  | $\begin{gathered} 95 \\ 125 \end{gathered}$ | $\mu \mathrm{A}$ |
|  |  | $\mathrm{I}_{\mathrm{L}}=1 \mathrm{~mA}$ | 80 |  | $\begin{aligned} & 110 \\ & 170 \end{aligned}$ |  | $\begin{aligned} & 110 \\ & 170 \end{aligned}$ |  |
|  |  | $\mathrm{I}_{\mathrm{L}}=25 \mathrm{~mA}$ | 200 |  | $\begin{aligned} & 300 \\ & \mathbf{5 5 0} \end{aligned}$ |  | $\begin{gathered} 300 \\ \mathbf{5 5 0} \end{gathered}$ |  |
|  |  | $\mathrm{I}_{\mathrm{L}}=100 \mathrm{~mA}$ | 600 |  | $\begin{gathered} 800 \\ \mathbf{1 5 0 0} \end{gathered}$ |  | $\begin{gathered} 800 \\ \mathbf{1 5 0 0} \end{gathered}$ |  |
|  |  | $\mathrm{V}_{\text {ON/OFF }}<0.3 \mathrm{~V}$ | 0.01 |  | 0.8 |  | 0.8 |  |
|  |  | $\mathrm{V}_{\text {ON/OFF }}<0.15 \mathrm{~V}$ | 0.05 |  | 2 |  | 2 |  |
| $\mathrm{V}_{\text {ON/OFF }}$ | ON/OFF Input Voltage (Note 8) | High = O/P ON | 1.4 | 2.0 |  | 2.0 |  | V |
|  |  | Low = O/P OFF | 0.50 |  | 0.15 |  | 0.15 |  |
| ION/OFF | ON/OFF Input Current | $\mathrm{V}_{\text {ON/OFF }}=0$ | 0.01 |  | -1 |  | -1 | $\mu \mathrm{A}$ |
|  |  | $\mathrm{V}_{\text {ON/OFF }}=5 \mathrm{~V}$ | 5 |  | 15 |  | 15 |  |


| Electrical Characteristics Limits in standard typeface are for $\mathrm{T}_{J}=25^{\circ} \mathrm{C}$, and limits in boldface type apply over the fulloperating temperature range. Unlessotherwise specified: $\mathrm{V}_{\mathrm{IN}}=\mathrm{V}_{\mathrm{O}(\mathrm{NOM})}+1 \mathrm{~V}, \mathrm{C}_{\mathrm{IN}}=1 \mu \mathrm{~F}, \mathrm{I}_{\mathrm{L}}=1 \mathrm{~mA}, \mathrm{C}_{\mathrm{OUT}}=4.7 \mu \mathrm{~F}$, $\mathrm{V}_{\text {ON/OFF }}=2 \mathrm{~V}$. (Continued) |  |  |  |  |  |  |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| Symbol | Parameter | Conditions | Typ | $\begin{aligned} & \text { LP2981AI-XX } \\ & \text { (Note 6) } \\ & \hline \end{aligned}$ |  | $\begin{aligned} & \text { LP2981I-XX } \\ & \text { (Note 6) } \\ & \hline \end{aligned}$ |  | Units |
|  |  |  |  | Min | Max | Min | Max |  |
| $\mathrm{l}_{\mathrm{O}}(\mathrm{PK})$ | Peak Output Current | $\mathrm{V}_{\text {OUT }} \geq \mathrm{V}_{\text {O(NOM }}-5 \%$ | 400 | 150 |  | 150 |  | mA |
| $e_{n}$ | Output Noise Voltage (RMS) | $\begin{aligned} & \mathrm{BW}=300 \mathrm{~Hz}-50 \mathrm{kHz}, \\ & \mathrm{C}_{\mathrm{OUT}}=10 \mu \mathrm{~F} \end{aligned}$ | 160 |  |  |  |  | $\mu \mathrm{V}$ |
| $\frac{\Delta \mathrm{V}_{\mathrm{OUT}}}{\Delta \mathrm{~V}_{\mathrm{IN}}}$ | Ripple Rejection | $\begin{aligned} & f=1 \mathrm{kHz} \\ & \text { Cout }_{\text {OU }}=10 \mu \mathrm{~F} \end{aligned}$ | 63 |  |  |  |  | dB |
| $\mathrm{IO}(\mathrm{MAX})$ | Short Circuit Current | $\mathrm{R}_{\mathrm{L}}=0$ (Steady State) (Note 9) | 150 |  |  |  |  | mA |

Note 1: Absolute maximum ratings indicate limits beyond which damage to the component may occur. Electrical specifications do not apply when operating the device outside of its rated operating conditions.
Note 2: The ESD rating of pins 3 and 4 is 1 kV .
Note 3: The maximum allowable power dissipation is a function of the maximum junction temperature, $\mathrm{T}_{J(\mathrm{MAX})}$, the junction-to-ambient thermal resistance, $\theta_{\mathrm{JA}}$, and the ambient temperature, $\mathrm{T}_{\mathrm{A}}$. The maximum allowable power dissipation at any ambient temperature is calculated using

$$
P(M A X)=\frac{T_{J(M A X)}-T_{A}}{\theta_{J A}}
$$

The value of $\theta_{\mathrm{JA}}$ for the SOT-23 package is $300^{\circ} \mathrm{C} / \mathrm{W}$. Exceeding the maximum allowable power dissipation will cause excessive die temperature, and the regulator will go into thermal shutdown.

Note 4: If used in a dual-supply system where the regulator load is returned to a negative supply, the LP2981 output must be diode-clamped to ground.
Note 5: The output PNP structure contains a diode between the $\mathrm{V}_{I N}$ and $\mathrm{V}_{\text {OUT }}$ terminals that is normally reverse-biased. Reversing the polarity from $\mathrm{V}_{\mathrm{IN}}$ to $\mathrm{V}_{\text {OUT }}$ will turn on this diode (see Application Hints).

Note 6: Limits are $100 \%$ production tested at $25^{\circ} \mathrm{C}$. Limits over the operating temperature range are guaranteed through correlation using Statistical Quality Control SQC) methods. The limits are used to calculate National's Averaging Outgoing Level (AOQL)
Note 7: Dropout voltage is defined as the input to output differential at which the output voltage drops 100 mV below the value measured with a 1 V differential. Note 8: The ON/OFF inputs must be properly driven to prevent misoperation. For details, refer to Application Hints.
Note 9: See Typical Performance Characteristics curves

## Basic Application Circuit


*ON/ $\overline{\mathrm{OFF}}$ input must be actively terminated. Tie to $\mathrm{V}_{\mathrm{IN}}$ if this function is not to be used.
**Minimum Output Capacitance is shown to insure stability over full load current range. More capacitance provides superior dynamic performance and additiona stability margin (see Application Hints).
***Do not make connections to this pin.

## Ordering Information

TABLE I. Package Marking and Order Information

| Output <br> Voltage <br> (V) | Grade | Order <br> Information | Package <br> Marking | Supplied as: |
| :---: | :---: | :---: | :---: | :---: |
| 5.0 | A | LP2981AIM5X-5.0 | L03A | 3k Units on Tape and Reel |
| 5.0 | A | LP2981AIM5-5.0 | L03A | 250 Units on Tape and Reel |
| 5.0 | STD | LP2981IM5X-5.0 | L03B | $3 k$ Units on Tape and Reel |
| 5.0 | STD | LP2981IM5-5.0 | L03B | 250 Units on Tape and Reel |
| 3.3 | A | LP2981AIM5X-3.3 | L04A | $3 k$ Units on Tape and Reel |
| 3.3 | A | LP2981AIM5-3.3 | L04A | 250 Units on Tape and Reel |
| 3.3 | STD | LP2981IM5X-3.3 | L04B | $3 k$ Units on Tape and Reel |
| 3.3 | STD | LP2981IM5-3.3 | L04B | 250 Units on Tape and Reel |
| 3.0 | A | LP2981AIM5X-3.0 | L05A | $3 k$ Units on Tape and Reel |
| 3.0 | A | LP2981AIM5-3.0 | L05A | 250 Units on Tape and Reel |
| 3.0 | STD | LP2981IM5X-3.0 | L05B | 3k Units on Tape and Reel |
| 3.0 | STD | LP2981IM5-3.0 | L05B | 250 Units on Tape and Reel |

## Connection Diagram



See NS Package Number MA05A

## Typical Performance Characteristics

Unless otherwise specified: $\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}, \mathrm{V}_{\mathrm{IN}}=\mathrm{V}_{\mathrm{O}(\mathrm{NOM})}+1 \mathrm{~V}, \mathrm{C}_{\mathrm{OUT}}=4.7 \mu \mathrm{~F}, \mathrm{C}_{\mathrm{IN}}=1 \mu \mathrm{~F}$ all voltage options, ON/OFF pin tied to $\mathrm{V}_{\mathrm{IN}}$.


TL/H/12506-6


TL/H/12506-8


TL/H/12506-10


TL/H/12506-7

Dropout Characteristics


TL/H/12506-9


TL/H/12506-11

Typical Performance Characteristics (Continued)
Unless otherwise specified: $\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}, \mathrm{V}_{\mathrm{IN}}=\mathrm{V}_{\mathrm{O}(\mathrm{NOM})}+1 \mathrm{~V}, \mathrm{C}_{\mathrm{OUT}}=4.7 \mu \mathrm{~F}, \mathrm{C}_{\mathrm{IN}}=1 \mu \mathrm{~F}$ all voltage options, ON/OFF pin tied to $\mathrm{V}_{\mathrm{IN}}$.


TL/H/12506-14


TL/H/12506-16



TL/H/12506-15

## Input Current vs $\mathrm{V}_{\mathrm{IN}}$



TL/H/12506-17



## Typical Performance Characteristics (Continued)

Unless otherwise specified: $\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}, \mathrm{V}_{\mathrm{IN}}=\mathrm{V}_{\mathrm{O}(\mathrm{NOM})}+1 \mathrm{~V}, \mathrm{C}_{\mathrm{OUT}}=4.7 \mu \mathrm{~F}, \mathrm{C}_{\mathrm{IN}}=1 \mu \mathrm{~F}$ all voltage options, ON/OFF pin tied to $\mathrm{V}_{\mathrm{IN}}$.


TL/H/12506-30


TL/H/12506-32
Turn-On Waveform

$20 \mu \mathrm{~s} / \mathrm{div} \rightarrow$
TL/H/12506-34


TL/H/12506-31


Turn-Off Waveform

$10 \mathrm{~ms} / \mathrm{div} \longrightarrow$
TL/H/12506-35

## Typical Performance

## Characteristics (Continued)

## Unless otherwise specified:

$\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}, \mathrm{V}_{\mathrm{IN}}=\mathrm{V}_{\mathrm{O}(\mathrm{NOM})}+1 \mathrm{~V}, \mathrm{COUT}=4.7 \mu \mathrm{~F}$,
$\mathrm{C}_{\mathrm{IN}}=1 \mu \mathrm{~F}$, all voltage options, ON/OFF pin tied to $\mathrm{V}_{\text {IN }}$.

| ON/OFF Pin Current vs |
| :--- |
| VON/OFF |
| $\left.\begin{array}{\|l\|l\|l\|l\|l\|l\|l\|l\|l\|}\hline & & & & & & \\ \hline\end{array}\right)$ |
|  |

TL/H/12506-36


## Application Hints

## EXTERNAL CAPACITORS

Like any low-dropout regulator, the external capacitors used with the LP2981 must be carefully selected to assure regulator loop stability.
INPUT CAPACITOR: An input capacitor whose value is $\geq 1 \mu \mathrm{~F}$ is required with the LP2981 (amount of capacitance can be increased without limit).
This capacitor must be located a distance of not more than $0.5^{\prime \prime}$ from the input pin of the LP2981 and returned to a clean analog ground. Any good quality ceramic or tantalum can be used for this capacitor.

OUTPUT CAPACITOR: The output capacitor must meet both the requirement for minimum amount of capacitance and E.S.R. (equivalent series resistance) value. Curves are provided which show the allowable ESR range as a function of load current for various output voltages and capacitor values (refer to Figures 1-4).
IMPORTANT: The output capacitor must maintain its ESR in the stable region over the full operating temperature range to assure stability. Also, capacitor tolerance and variation with temperature must be considered to assure the minimum amount of capacitance is provided at all times.
This capacitor should be located not more than $0.5^{\prime \prime}$ from the output pin of the LP2981 and returned to a clean analog ground.

## CAPACITOR CHARACTERISTICS

TANTALUM: Tantalum capacitors offer the best value for size, cost, and electrical performance. Most good quality tantalums can be used with the LP2981, but check the manufacturer's data sheet to be sure the ESR is in range.
It is important to remember that ESR increases at lower temperatures and a capacitor that is near the upper limit for stability at room temperature can cause instability when it gets cold.
In applications which must operate at very low temperatures, it may be necessary to parallel the output tantalum capacitor with a ceramic capacitor to prevent the ESR from going up too high (see next section for important information on ceramic capacitors).
CERAMIC: Ceramic capacitors are typically larger and more costly than tantalum for a given capacitance, however they have a much lower ESR (and they do not exhibit the low temperature increase seen in tantalum and aluminum electrolytics).
It should be warned that the ESR of a ceramic can be low enough to go below the minimum stable value for the LP2981. A $2.2 \mu \mathrm{~F}$ ceramic was measured and found to have an ESR of about $15 \mathrm{~m} \Omega$, which is low enough to cause oscillations.
This means that in many cases, large value ( $\geq 1 \mu \mathrm{~F}$ ) ceramics should not be used on the LP2981 output (the limiting value of ceramic capacitance which can be used will be dictated by the ESR).
If ceramic capacitors are used on the output, they should be used in parallel with a tantalum that provides most of the output capacitance. Remember that when a tantalum and ceramic are put in parallel, the effective ESR seen by the LP2981 output is the parallel value resulting from the ESR of each capacitor.
ALUMINUM: Because of large physical size, aluminum electrolytics are not typically used with the LP2981. They must meet the same ESR requirements over the operating temperature range, more difficult because of their steep increase at cold temperature.
An aluminum electrolytic can exhibit an ESR increase of as much as 50 X when going from $20^{\circ} \mathrm{C}$ to $-40^{\circ} \mathrm{C}$. Also, some aluminum electrolytics are not operational below $-25^{\circ} \mathrm{C}$ because the electrolyte can freeze.

## Application Hints (Continued)



TL/H/12506-40
FIGURE 3. $3 \mathrm{~V} / 3.3 \mu \mathrm{~F}$ ESR Curves


FIGURE 2. 5V/10 $\mu$ F ESR Curves


FIGURE 4. 3V/10 $\mu$ F ESR Curves

## Application Hints (Continued)

## reverse current path

The power transistor used in the LP2981 has an inherent diode connected between the regulator input and output (see below).


TL/H/12506-41
If the output is forced above the input by more than a $\vee_{B E}$, this diode will become forward biased and current will flow from the $\mathrm{V}_{\text {OUT }}$ terminal to $\mathrm{V}_{\text {IN }}$
This current must be limited to $<100 \mathrm{~mA}$ to prevent damage to the part.
The internal diode can also be turned on by abruptly stepping the input voltage to a value below the output voltage. To prevent regulator mis-operation, a Schottky diode should be used in any application where input/output voltage conditions can cause the internal diode to be turned on (see below).

TL/H/12506-43
As shown, the Schottky diode is connected in parallel with the internal parasitic diode and prevents it from being turned on by limiting the voltage drop across it to about 0.3 V .


## ON/OFF INPUT OPERATION

The LP2981 is shut off by pulling the ON/OFF input low, and turned on by driving the input high. If this feature is not to be used, the ON/OFF input should be tied to $\mathrm{V}_{\text {IN }}$ to keep the regulator on at all times (the ON/OFF input must not be left floating).
To ensure proper operation, the signal source used to drive the ON/OFF input must be able to swing above and below the specified turn-on/turn-off voltage thresholds which guarantee an ON or OFF state (see Electrical Characteristics).
The ON/OFF signal may come from either a totem-pole output, or an open-collector output with pull-up resistor to the LP2981 input voltage or another logic supply. The high-level voltage may exceed the LP2981 input voltage, but must remain within the Absolute Maximum Ratings for the ON/OFF pin.
It is also important that the turn-on/turn-off voltage signals applied to the ON/OFF input have a slew rate which is greater than $40 \mathrm{mV} / \mu \mathrm{s}$.
Important: the regulator shutdown function will operate incorrectly if a slow-moving signal is applied to the ON/OFF input.



LAND PATTERN RECOMMENDATION


5-Lead Small Outline Package (M5)
NS Package Number MA05A
For Order Numbers, refer to Table I in the "Order Information" section of this document.

## LIFE SUPPORT POLICY

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1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and whose failure to perform, when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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| :---: | :---: | :---: | :---: |



## Basic Application Circuit



TL/H/12679-2
*ON/ $\overline{\mathrm{FFF}}$ input must be actively terminated. Tie to $\mathrm{V}_{\text {IN }}$ if this function is not to be used.
${ }^{* *}$ Minimum capacitance is shown to insure stability over full load current range. More capacitance provides superior dynamic performance (see Application Hints). ***See Application Hints.

## Ordering Information

TABLE I. Package Marking and Ordering Information

| Output Voltage (V) |  |  |  |  |  | Grade | Order Information | Package Marking | Supplied As: |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| 5.0 | A | LP2982AIM5X-5.0 | L18A | 3k Units on Tape and Reel |  |  |  |  |  |
| 5.0 | A | LP2982AIM5-5.0 | L18A | 250 Units on Tape and Reel |  |  |  |  |  |
| 5.0 | STD | LP2982IM5X-5.0 | L18B | 3k Units on Tape and Reel |  |  |  |  |  |
| 5.0 | STD | LP2982IM5-5.0 | L18B | 250 Units on Tape and Reel |  |  |  |  |  |
| 3.3 | A | LP2982AIM5X-3.3 | L19A | 3k Units on Tape and Reel |  |  |  |  |  |
| 3.3 | A | LP2982AIM5-3.3 | L19A | 250 Units on Tape and Reel |  |  |  |  |  |
| 3.3 | STD | LP2982IM5X-3.3 | L19B | 3k Units on Tape and Reel |  |  |  |  |  |
| 3.3 | STD | LP2982IM5-3.3 | L19B | 250 Units on Tape and Reel |  |  |  |  |  |
| 3.0 | A | LP2982AIM5X-3.0 | L20A | 3k Units on Tape and Reel |  |  |  |  |  |
| 3.0 | A | LP2982AIM5-3.0 | L20A | 250 Units on Tape and Reel |  |  |  |  |  |
| 3.0 | STD | LP2982IM5X-3.0 | L20B | 3k Units on Tape and Reel |  |  |  |  |  |
| 3.0 | STD | LP2982IM5-3.0 | L20B | 250 Units on Tape and Reel |  |  |  |  |  |



| Electrical Characteristics Limits in standard typeface are for $\mathrm{T}_{\mathrm{J}}=25^{\circ} \mathrm{C}$, and limits in boldface type apply over the full operating temperature range. Unless otherwise specified: $\mathrm{V}_{\mathrm{IN}}=\mathrm{V}_{\mathrm{O}(\mathrm{NOM})}+1 \mathrm{~V}, \mathrm{~L}_{\mathrm{L}}=1 \mathrm{~mA}, \mathrm{C}_{\mathrm{IN}}=1 \mu \mathrm{~F}, \mathrm{C}_{\mathrm{OUT}}=4.7 \mu \mathrm{~F}$, $\mathrm{V}_{\text {ON/OFF }}=2 \mathrm{~V}$. (Continued) |  |  |  |  |  |  |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| Symbol | Parameter | Conditions | Typ | $\begin{aligned} & \text { LP2982AI-X.X } \\ & \text { (Note 6) } \end{aligned}$ |  | $\begin{aligned} & \text { LP2982I-X.X } \\ & \text { (Note 6) } \end{aligned}$ |  | Units |
|  |  |  |  | Min | Max | Min | Max |  |
| $\mathrm{l}_{\mathrm{O}}(\mathrm{PK})$ | Peak Output Current | $\mathrm{V}_{\text {OUT }} \geq \mathrm{V}_{\text {O(NOM })}-5 \%$ | 150 | 100 |  | 100 |  | mA |
| $\mathrm{V}_{1 \mathrm{~N}^{-}} \mathrm{V}_{\mathrm{O}}$ | Dropout Voltage | $\mathrm{L}_{\mathrm{L}}=80 \mathrm{~mA}$ | 180 |  | $\begin{aligned} & 225 \\ & 325 \end{aligned}$ |  | $\begin{gathered} 225 \\ \mathbf{3 2 5} \end{gathered}$ | mV |
| IGND | Ground Pin Current | $\mathrm{L}_{\mathrm{L}}=80 \mathrm{~mA}$ | 525 |  | $\begin{gathered} 750 \\ \mathbf{1 4 0 0} \end{gathered}$ |  | $\begin{gathered} 750 \\ \mathbf{1 4 0 0} \end{gathered}$ | $\mu \mathrm{A}$ |
| $e_{n}$ | Output Noise <br> Voltage (RMS) | $\begin{aligned} & \mathrm{BW}=300 \mathrm{~Hz}-50 \mathrm{kHz}, \\ & \mathrm{C}_{\text {OUT }}=10 \mu \mathrm{~F} \\ & \mathrm{C}_{\text {BYPASS }}=0.01 \mu \mathrm{~F} \end{aligned}$ | 30 |  |  |  |  | $\mu \mathrm{V}$ |
| $\frac{\Delta \mathrm{V}_{\mathrm{OUT}}}{\Delta \mathrm{~V}_{\mathrm{IN}}}$ | Ripple Rejection | $\begin{aligned} & f=1 \mathrm{kHz} \\ & \mathrm{C}_{\text {OUT }}=10 \mu \mathrm{~F} \end{aligned}$ | 45 |  |  |  |  | dB |
| IO(MAX) | Short Circuit Current | $R_{L}=0$ (Steady State) <br> (Note 9) | 150 |  |  |  |  | mA |
| The value of $\theta_{\mathrm{JA}}$ for the SOT-23 package is $300^{\circ} \mathrm{C} / \mathrm{W}$. Exceeding the maximum allowable power dissipation will cause excessive die temperature, and the regulator will go into thermal shutdown. <br> Note 4: If used in a dual-supply system where the regulator load is returned to a negative supply, the LP2982 output must be diode-clamped to ground. <br> Note 5: The output PNP structure contains a diode between the $\mathrm{V}_{I N}$ and $\mathrm{V}_{\text {OUT }}$ terminals that is normally reverse-biased. Reversing the polarity from $\mathrm{V}_{I N}$ to $\mathrm{V}_{\text {OUT }}$ will turn on this diode. <br> Note 6: Limits are $100 \%$ production tested at $25^{\circ} \mathrm{C}$. Limits over the operating temperature range are guaranteed through correlation using Statistical Quality Control (SQC) methods. The limits are used to calculate National's Averaging Outgoing Level (AOQL). <br> Note 7: Dropout voltage is defined as the input to output differential at which the output voltage drops 100 mV below the value measured with a $1 V$ differential. <br> Note 8: The ON/OFF inputs must be properly driven to prevent possible misoperation. For details, refer to Application Hints. <br> Note 9: See Typical Performance Characteristics curves. |  |  |  |  |  |  |  |  |

## Typical Performance Characteristics

Unless otherwise specified: $\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}, \mathrm{V}_{\mathrm{IN}}=\mathrm{V}_{\mathrm{O}(\mathrm{NOM})}+1 \mathrm{~V}, \mathrm{C}_{\mathrm{OUT}}=4.7 \mu \mathrm{~F}, \mathrm{C}_{\mathrm{IN}}=1 \mu \mathrm{~F}$, all voltage options, ON/OFF pin tied to $\mathrm{V}_{\mathrm{IN}}$.


TL/H/12679-4

TL/H/12679-6


TL/H/12679-8


TL/H/12679-5


TL/H/12679-7

Typical Performance Characteristics (Continued)
Unless otherwise specified: $\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}, \mathrm{V}_{\mathrm{IN}}=\mathrm{V}_{\mathrm{O}(\mathrm{NOM})}+1 \mathrm{~V}, \mathrm{C}_{\mathrm{OUT}}=4.7 \mu \mathrm{~F}, \mathrm{C}_{\mathrm{IN}}=1 \mu \mathrm{~F}$, all voltage options, ON/OFF pin tied to $\mathrm{V}_{\mathrm{IN}}$.


TL/H/12679-10


TL/H/12679-12


TL/H/12679-14


TL/H/12679-11





## Typical Performance Characteristics (Continued)

Unless otherwise specified: $\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}, \mathrm{V}_{\mathrm{IN}}=\mathrm{V}_{\mathrm{O}(\mathrm{NOM})}+1 \mathrm{~V}, \mathrm{C}_{\mathrm{OUT}}=4.7 \mu \mathrm{~F}, \mathrm{C}_{\mathrm{IN}}=1 \mu \mathrm{~F}$, all voltage options, ON/OFF pin tied to $\mathrm{V}_{\mathrm{IN}}$.


TL/H/12679-42


TL/H/12679-30

$20 \mu \mathrm{~s} / \mathrm{div} \rightarrow$
TL/H/12679-32


TL/H/12679-29


$10 \mathrm{~ms} / \mathrm{div} \longrightarrow$

TL/H/12679-33

## Typical Performance

## Characteristics (Continued)

Unless otherwise specified:
$\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}, \mathrm{V}_{\mathrm{IN}}=\mathrm{V}_{\mathrm{O}(\mathrm{NOM})}+1 \mathrm{~V}$, COUT $=4.7 \mu \mathrm{~F}$,
$\mathrm{C}_{\mathrm{IN}}=1 \mu \mathrm{~F}$, all voltage options, ON/OFF pin tied to $\mathrm{V}_{\text {IN }}$.

$$
\begin{aligned}
& \text { ON/OFF Pin Current vs } \\
& \text { VON/OFF } \\
& \begin{array}{|l|l|l|l|l|l|l|l|}
\hline & & & & & & & \\
\hline
\end{array} \\
& \hline
\end{aligned}
$$



## Application Hints

## EXTERNAL CAPACITORS

Like any low-dropout regulator, the external capacitors used with the LP2982 must be carefully selected to assure regulator loop stability.
INPUT CAPACITOR: An input capacitor whose value is $\geq 1 \mu \mathrm{~F}$ is required with the LP2982 (amount of capacitance can be increased without limit).
This capacitor must be located a distance of not more than $0.5^{\prime \prime}$ from the input pin of the LP2982 and returned to a clean analog ground. Any good quality ceramic or tantalum can be used for this capacitor.
OUTPUT CAPACITOR: The output capacitor must meet both the requirement for minimum amount of capacitance and E.S.R. (equivalent series resistance) value. Curves are provided which show the allowable ESR range as a function of load current for various output voltages and capacitor values (refer to Figures 1, 2 ).

IMPORTANT: The output capacitor must maintain its ESR in the stable region over the full operating temperature to assure stability. Also, capacitor tolerance and variation with temperature must be considered to assure the minimum amount of capacitance is provided at all times.
This capacitor should be located not more than $0.5^{\prime \prime}$ from the output pin of the LP2982 and returned to a clean analog ground.
LOW-CURRENT OPERATION: In applications where the load current is $<1 \mathrm{~mA}$, special consideration must be given to the output capacitor.
Circuitry inside the LP2982 is specially designed to reduce operating (quiescent) current at light loads down to about $65 \mu \mathrm{~A}$.
The mode of operation which yields this very low quiescent current also means that the output capacitor ESR is critical. For optimum stability and minimum output noise, it is recommended that a $10 \Omega$ resistor be placed in series with the output capacitor in any applications where $\mathrm{I}_{\mathrm{L}}<1 \mathrm{~mA}$.

## CAPACITOR CHARACTERISTICS

TANTALUM: Tantalum capacitors offer the best value for considerations of size, cost, and electrical performance. Most good quality tantalums can be used with the LP2982, but check the manufacturer's data sheet to be sure the ESR is in range.
It is important to remember that ESR increases sharply at lower temperatures ( $<10^{\circ} \mathrm{C}$ ) and a capacitor that is near the upper limit for stability at room temperature can cause instability when it gets cold.
In applications which must operate at very low temperatures, it may be necessary to parallel the output tantalum capacitor with a ceramic capacitor to prevent the ESR from going up too high (see next section for important information on ceramic capacitors).
CERAMIC: Ceramic capacitors are typically larger and more costly than tantalum for a given capacitance, however they have a much lower ESR (and they do not exhibit the low temperature increase seen in tantalum and aluminum electrolytics).
It should be warned that the ESR of a ceramic can be low enough to go below the minimum stable value for the LP2982. A good $2.2 \mu \mathrm{~F}$ ceramic was measured and found to have an ESR of about $15 \mathrm{~m} \Omega$, which is low enough to cause oscillations.
This means that in many cases, large value ( $\geq 1 \mu \mathrm{~F}$ ) ceramics should not be used on the LP2982 output (the limiting value of ceramic capacitance which can be used will be dictated by the ESR).
If ceramic capacitors are used on the output, they should be used in parallel with a tantalum that provides most of the output capacitance. Remember that when a tantalum and ceramic are put in parallel, the effective ESR seen by the LP2982 output is the parallel value resulting from the ESR of each capacitor.

ALUMINUM: Because of large physical size, aluminum electrolytics are not typically used with the LP2982. They must meet the same ESR requirements over the operating temperature range, which is more difficult because of their large increase in ESR at cold temperature.
An aluminum electrolytic can exhibit an ESR increase of as much as 50 X when going from $20^{\circ} \mathrm{C}$ to $-40^{\circ} \mathrm{C}$. Also, some aluminum electrolytics are not operational below $-25^{\circ} \mathrm{C}$ because the electrolyte can freeze.

## Application Hints (Continued)



TL/H/12679-43
FIGURE 1. $5 \mathrm{~V} / 2.2 \mu \mathrm{~F}$ ESR Curves


TL/H/12679-44
FIGURE 2. $3 V / 4.7 \mu \mathrm{~F}$ ESR Curves

## BYPASS CAPACITOR

The $0.01 \mu \mathrm{~F}$ capacitor connected to the bypass pin to reduce noise must have very low leakage.
The current flowing out of the bypass pin comes from the bandgap reference, which is used to set the output voltage.
This capacitor leakage current causes the output voltage to decline by an amount proportional to the current. Typical values are $-0.015 \% / \mathrm{nA} @-40^{\circ} \mathrm{C},-0.021 \% / \mathrm{nA} @ 25^{\circ} \mathrm{C}$, and $-0.035 \% / n A @+125^{\circ} \mathrm{C}$.
This data is valid up to a maximum leakage current of about 500 nA , beyond which the bandgap is so severly loaded that it can not function.
Care must be taken to ensure that the capacitor selected will not have excessive leakage current over the operating temperature range of the application.
A high quality ceramic capacitor which uses either NPO or COG type dielectric material will typically have very low leakage. Small surface mount polypropolene or polycarbonate film capacitors also have extremely low leakage, but are slightly larger than ceramics.

## REVERSE CURRENT PATH

The power transistor used in the LP2982 has an inherent diode connected between the regulator input and output (see below).


TL/H/12679-39
If the output is forced above the input by more than a $\mathrm{V}_{\mathrm{BE}}$, this diode will become forward biased and current will flow from the $\mathrm{V}_{\text {OUT }}$ terminal to $\mathrm{V}_{\text {IN }}$. This current must be limited to $<100 \mathrm{~mA}$ to prevent damage to the part.
The internal diode can also be turned on by abruptly stepping the input voltage to a value below the output voltage. To prevent regulator mis-operation, a Schottky diode should be used in any application where input/output voltage conditions can cause the internal diode to be turned on (see below).


TL/H/12679-40
As shown, the Schottky diode is connected in parallel with the internal parasitic diode and prevents it from being turned on by limiting the voltage drop across it to about 0.3 V .

## ON/OFF INPUT OPERATION

The LP2982 is shut off by pulling the ON/OFF input low, and turned on by driving the input high. If this feature is not to be used, the ON/OFF input should be tied to $\mathrm{V}_{\text {IN }}$ to keep the regulator on at all times (the ON/OFF input must not be left floating).
To ensure proper operation, the signal source used to drive the ON/OFF input must be able to swing above and below the specified turn-on/turn-off voltage thresholds which guarantee an ON or OFF state (see Electrical Characteristics).
The ON/OFF signal may come from either a totem-pole output, or an open-collector output with pull-up resistor to the LP2982 input voltage or another logic supply. The high-level voltage may exceed the LP2982 input voltage, but must remain within the Absolute Maximum Ratings for the ON/OFF pin.
It is also important that the turn-on/turn-off voltage signals applied to the ON/OFF input have a slew rate which is greater than $40 \mathrm{mV} / \mu \mathrm{s}$.
Important: the regulator shutdown function will operate incorrectly if a slow-moving signal is applied to the ON/OFF input.

Physical Dimensions inches (millimeters) unless otherwise noted


LAND PATTERN RECOMMENDATION


5-Lead Small Outline Package (M5)
NS Package Number MA05A
For Order Numbers, refer to Table I in the "Order Information" section of this document.

## LIFE SUPPORT POLICY

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2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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## Connection Diagram and Ordering Information

Surface Mount Packages:
Mini SO-8 Package Type MM: See NS Package Drawing Number MUA08A SO-8 Package Type M: See NS Package Drawing Number M08A

Top View
For ordering information, refer to Table 1 of this document.

## Basic Application Circuits



* Minimum capacitance shown to assure stability, but may be increased without limit. Larger output capacitor provides improved dynamic response.
** Shutdown input must be actively terminated. Tie to $V_{I N}$ if not used.


## Basic Application Circuits (Continued)



* Minimum capacitance shown to assure stability, but may be increased without limit. Larger output capacitor provides improved dynamic response.
** Shutdown input must be actively terminated. Tie to $V_{I N}$ if not used.


## Ordering Information

TABLE 1. Package Marking and Ordering Information

| Output Voltage | Grade | Order Information | Package Marking | Supplied as: |
| :---: | :---: | :---: | :---: | :---: |
| 5 | A | LP2986AIMMX-5.0 | L41A | 3.5k Units on Tape and Reel |
| 5 | A | LP2986AIMM-5.0 | L41A | 250 Units on Tape and Reel |
| 5 | STD | LP2986IMMX-5.0 | L41B | 3.5k Units on Tape and Reel |
| 5 | STD | LP2986IMM-5.0 | L41B | 250 Units on Tape and Reel |
| 3.3 | A | LP2986AIMMX-3.3 | L40A | 3.5k Units on Tape and Reel |
| 3.3 | A | LP2986AIMM-3.3 | L40A | 250 Units on Tape and Reel |
| 3.3 | STD | LP2986IMMX-3.3 | L40B | 3.5k Units on Tape and Reel |
| 3.3 | STD | LP2986IMM-3.3 | L40B | 250 Units on Tape and Reel |
| 3.0 | A | LP2986AIMMX-3.0 | L39A | 3.5k Units on Tape and Reel |
| 3.0 | A | LP2986AIMM-3.0 | L39A | 250 Units on Tape and Reel |
| 3.0 | STD | LP2986IMMX-3.0 | L39B | 3.5k Units on Tape and Reel |
| 3.0 | STD | LP2986IMM-3.0 | L39B | 250 Units on Tape and Reel |
| 5 | A | LP2986AIMX-5.0 | 2986AIM5.0 | 2.5k Units on Tape and Reel |
| 5 | A | LP2986AIM-5.0 | 2986AIM5.0 | Shipped in Anti-Static Rails |
| 5 | STD | LP2986IMX-5.0 | 2986IM5.0 | 2.5k Units on Tape and Reel |
| 5 | STD | LP2986IM-5.0 | 2986IM5.0 | Shipped in Anti-Static Rails |
| 3.3 | A | LP2986AIMX-3.3 | 2986AIM3.3 | 2.5k Units on Tape and Reel |
| 3.3 | A | LP2986AIM-3.3 | 2986AIM3.3 | Shipped in Anti-Static Rails |
| 3.3 | STD | LP2986IMX-3.3 | 2986IM3.3 | 2.5k Units on Tape and Reel |
| 3.3 | STD | LP2986IM-3.3 | 2986IM3.3 | Shipped in Anti-Static Rails |
| 3.0 | A | LP2986AIMX-3.0 | 2986AIM3.0 | 2.5k Units on Tape and Reel |
| 3.0 | A | LP2986AIM-3.0 | 2986AIM3.0 | Shipped in Anti-Static Rails |
| 3.0 | STD | LP2986IMX-3.0 | 2986IM3.0 | 2.5k Units on Tape and Reel |
| 3.0 | STD | LP2986IM-3.0 | 2986IM3.0 | Shipped in Anti-Static Rails |

$\left.\begin{array}{llr}\text { Absolute Maximum Ratings (Note 1) }\end{array} \quad \begin{array}{c}\text { Input Supply Voltage } \\ \text { (Operating) }\end{array}\right)$

## Electrical Characteristics

Limits in standard typeface are for $\mathrm{T}_{J}=25^{\circ} \mathrm{C}$, and limits in boldface type apply over the full operating temperature range. Unless otherwise specified: $\mathrm{V}_{\mathrm{IN}}=\mathrm{V}_{\mathrm{O}}(\mathrm{NOM})+1 \mathrm{~V}, \mathrm{I}_{\mathrm{L}}=1 \mathrm{~mA}, \mathrm{C}_{\text {OUT }}=4.7 \mu \mathrm{~F}, \mathrm{C}_{\mathrm{IN}}=2.2 \mu \mathrm{~F}, \mathrm{~V}_{\mathrm{S} / \mathrm{D}}=2 \mathrm{~V}$.

| Symbol | Parameter | Conditions | Typical | LM2986AI-X.X <br> (Note 6) |  | $\begin{aligned} & \text { LM2986I-X.X } \\ & \text { (Note 6) } \end{aligned}$ |  | Units |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  |  |  | Min | Max | Min | Max |  |
| $\mathrm{V}_{\mathrm{O}}$ | Output Voltage (5.0V Versions) |  | 5.0 | 4.975 | 5.025 | 4.950 | 5.050 | V |
|  |  | $0.1 \mathrm{~mA}<\mathrm{I}_{\mathrm{L}}<200 \mathrm{~mA}$ | 5.0 | 4.960 | 5.040 | 4.920 | 5.080 |  |
|  |  |  |  | 4.910 | 5.090 | 4.860 | 5.140 |  |
|  | Output Voltage (3.3V Versions) |  | 3.3 | 3.283 | 3.317 | 3.267 | 3.333 |  |
|  |  | $0.1 \mathrm{~mA}<\mathrm{I}_{\mathrm{L}}<200 \mathrm{~mA}$ | 3.3 | 3.274 | 3.326 | 3.247 | 3.353 |  |
|  |  |  |  | 3.241 | 3.359 | 3.208 | 3.392 |  |
|  | Output Voltage <br> (3.0V Versions) |  | 3.0 | 2.985 | 3.015 | 2.970 | 3.030 |  |
|  |  | $0.1 \mathrm{~mA}<\mathrm{I}_{\mathrm{L}}<200 \mathrm{~mA}$ | 3.0 | 2.976 | 3.024 | 2.952 | 3.048 |  |
|  |  |  |  | 2.946 | 3.054 | 2.916 | 3.084 |  |
| $\frac{V_{0}}{\Delta V_{I N}}$ | Output Voltage Line Regulation | $\begin{aligned} & \mathrm{V}_{\mathrm{O}}(\mathrm{NOM})+1 \mathrm{~V} \leq \mathrm{V}_{\mathrm{IN}} \leq \\ & 16 \mathrm{~V} \end{aligned}$ | 0.007 |  | 0.014 |  | 0.014 | \%/V |
|  |  |  |  |  | 0.032 |  | 0.032 |  |
| $\mathrm{V}_{\text {IN }}-\mathrm{V}_{\mathrm{O}}$ | Dropout Voltage (Note 7) | $\mathrm{I}_{\mathrm{L}}=100 \mu \mathrm{~A}$ | 1 |  | 2.0 |  | 2.0 | mV |
|  |  |  |  |  | 3.5 |  | 3.5 |  |
|  |  | $\mathrm{I}_{\mathrm{L}}=75 \mathrm{~mA}$ | 90 |  | 120 |  | 120 |  |
|  |  |  |  |  | 170 |  | 170 |  |
|  |  | $\mathrm{I}_{\mathrm{L}}=200 \mathrm{~mA}$ | 180 |  | 230 |  | 230 |  |
|  |  |  |  |  | 350 |  | 350 |  |
| $\mathrm{I}_{\text {GND }}$ | Ground Pin Current | $\mathrm{I}_{\mathrm{L}}=100 \mu \mathrm{~A}$ | 100 |  | 120 |  | 120 | $\mu \mathrm{A}$ |
|  |  |  |  |  | 150 |  | 150 |  |
|  |  | $\mathrm{I}_{\mathrm{L}}=75 \mathrm{~mA}$ | 500 |  | 800 |  | 800 |  |
|  |  |  |  |  | 1400 |  | 1400 |  |
|  |  | $\mathrm{I}_{\mathrm{L}}=200 \mathrm{~mA}$ | 1 |  | 2.1 |  | 2.1 | mA |
|  |  |  |  |  | 3.7 |  | 3.7 |  |
|  |  | $\mathrm{V}_{\text {S/D }}<0.3 \mathrm{~V}$ | 0.05 |  | 1.5 |  | 1.5 | $\mu \mathrm{A}$ |
| $\mathrm{I}_{\mathrm{O}}(\mathrm{PK})$ | Peak Output Current | $\mathrm{V}_{\text {OUT }} \geq \mathrm{V}_{\text {O }}(\mathrm{NOM})-5 \%$ | 400 | 250 |  | 250 |  | mA |
| $\mathrm{I}_{0}(\mathrm{MAX})$ | Short Circuit Current | $\mathrm{R}_{\mathrm{L}}=0$ (Steady State) <br> (Note 11) | 400 |  |  |  |  |  |
| $\mathrm{e}_{\mathrm{n}}$ | Output Noise Voltage (RMS) | $\begin{aligned} & \mathrm{BW}=300 \mathrm{~Hz} \text { to } 50 \\ & \mathrm{kHz}, \mathrm{C}_{\text {OUT }}=10 \mu \mathrm{~F} \\ & \hline \end{aligned}$ | 160 |  |  |  |  | $\mu \mathrm{V}$ (RMS) |
| $\frac{\Delta \mathrm{V}_{\mathrm{OUT}}}{\Delta \mathrm{~V}_{\mathrm{IN}}}$ | Ripple Rejection | $\mathrm{f}=1 \mathrm{kHz}, \mathrm{C}_{\text {OUT }}=10 \mu \mathrm{~F}$ | 65 |  |  |  |  | dB |

## Electrical Characteristics <br> (Continued)

Limits in standard typeface are for $\mathrm{T}_{J}=25^{\circ} \mathrm{C}$, and limits in boldface type apply over the full operating temperature range. Unless otherwise specified: $\mathrm{V}_{I N}=\mathrm{V}_{\mathrm{O}}(\mathrm{NOM})+1 \mathrm{~V}, \mathrm{I}_{\mathrm{L}}=1 \mathrm{~mA}, \mathrm{C}_{\text {OUT }}=4.7 \mu \mathrm{~F}, \mathrm{C}_{\mathbb{I N}}=2.2 \mu \mathrm{~F}, \mathrm{~V}_{\mathrm{S} / \mathrm{D}}=2 \mathrm{~V}$.

| Symbol | Parameter | Conditions | Typical | $\begin{aligned} & \text { LM2986AI-X.X } \\ & \text { (Note 6) } \\ & \hline \end{aligned}$ |  | $\begin{aligned} & \text { LM2986I-X.X } \\ & \text { (Note 6) } \\ & \hline \end{aligned}$ |  | Units |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  |  |  | Min | Max | Min | Max |  |
| $\frac{\Delta V_{\text {OUT }}}{\Delta T}$ | Output Voltage <br> Temperature Coefficient | (Note 9) | 20 |  |  |  |  | ppm/ ${ }^{\circ} \mathrm{C}$ |
| FEEDBACK PIN |  |  |  |  |  |  |  |  |
| $\mathrm{V}_{\mathrm{FB}}$ | Feedback Pin Voltage |  | 1.23 | 1.21 | 1.25 | 1.20 | 1.26 | V |
|  |  |  |  | 1.20 | 1.26 | 1.19 | 1.27 |  |
|  |  | (Note 10) | 1.23 | 1.19 | 1.28 | 1.18 | 1.29 |  |
| $\frac{\Delta V_{F B}}{\Delta T}$ | FB Pin Voltage Temperature Coefficient | (Note 9) | 20 |  |  |  |  | ppm/ ${ }^{\circ} \mathrm{C}$ |
| $\mathrm{I}_{\text {FB }}$ | Feedback Pin Bias Current | $\mathrm{I}_{\mathrm{L}}=200 \mathrm{~mA}$ | 150 |  | 330 |  | 330 | nA |
|  |  |  |  |  | 760 |  | 760 |  |
| $\frac{I_{F B}}{\Delta T}$ | FB Pin Bias Current Temperature Coefficient | (Note 9) | 0.1 |  |  |  |  | $n A /{ }^{\circ} \mathrm{C}$ |

## SHUTDOWN INPUT

| $\mathrm{V}_{\mathrm{S} / \mathrm{D}}$ | S/D Input Voltage (Note 8) | $\mathrm{V}_{\mathrm{H}}=\mathrm{O} / \mathrm{P}$ ON | 1.4 | 2.0 |  | 2.0 |  | V |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | $V_{L}=$ O/P OFF | 0.55 |  | 0.18 |  | 0.18 |  |
| $\mathrm{I}_{\mathrm{S} / \mathrm{D}}$ | S/D Input Current | $\mathrm{V}_{\text {S/D }}=0$ | 0 |  | -1 |  | -1 | $\mu \mathrm{A}$ |
|  |  | $\mathrm{V}_{\mathrm{S} / \mathrm{D}}=5 \mathrm{~V}$ | 5 |  | 15 |  | 15 |  |

## ERROR COMPARATOR

| $\mathrm{I}_{\mathrm{OH}}$ | Output "HIGH" Leakage | $\mathrm{V}_{\mathrm{OH}}=16 \mathrm{~V}$ | 0.01 |  | 1 |  | 1 | $\mu \mathrm{A}$ |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  |  |  |  | 2 |  | 2 |  |
| $\mathrm{V}_{\text {OL }}$ | Output "LOW" Voltage | $\begin{aligned} & \mathrm{V}_{\mathrm{IN}}=\mathrm{V}_{\mathrm{O}}(\mathrm{NOM})-0.5 \mathrm{~V}, \\ & \mathrm{I}_{\mathrm{O}}(\mathrm{COMP})=300 \mu \mathrm{~A} \end{aligned}$ | 150 |  | 220 |  | 220 | mV |
|  |  |  |  |  | 350 |  | 350 |  |
| $\begin{aligned} & \mathrm{V}_{\text {THR }} \\ & (\mathrm{MAX}) \end{aligned}$ | Upper Threshold Voltage |  | -4.6 | -5.5 | -3.5 | -5.5 | -3.5 | \% $\mathrm{V}_{\text {OUT }}$ |
|  |  |  |  | -7.7 | -2.5 | -7.7 | -2.5 |  |
| $\mathrm{V}_{\text {THR }}$ <br> (MIN) | Lower Threshold Voltage |  | -6.6 | -8.9 | -4.9 | -8.9 | -4.9 |  |
|  |  |  |  | -13.0 | -3.3 | -13.0 | -3.3 |  |
| HYST | Hysteresis |  | 2.0 |  |  |  |  |  |

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the component may occur. Electrical specifications do not apply when operating the device outside of its rated operating conditions.
Note 2: The ESD rating of the Feedback pin is 500 V and the Tap pin is 1.5 kV
Note 3: The maximum allowable power dissipation is a function of the maximum junction temperature, $T_{J}(M A X)$, the junction-to-ambient thermal resistance, $\theta_{J}-A$, and the ambient temperature, $\mathrm{T}_{\mathrm{A}}$. The maximum allowable power dissipation at any ambient temperature is calculated using

$$
P(M A X)=\frac{T_{J}(M A X)-T_{A}}{\theta_{J-A}}
$$

The value of $\theta_{J-A}$ for the SO-8 (M) package is $160^{\circ} \mathrm{C} / \mathrm{W}$, and the mini SO-8 (MM) package is $200^{\circ} \mathrm{C} / \mathrm{W}$. Exceeding the maximum allowable power dissipation will cause excessive die temperature, and the regulator will go into thermal shutdown.
Note 4: If used in a dual-supply system where the regulator load is returned to a negative supply, the LM2986 output must be diode-clamped to ground.
Note 5: The output PNP structure contains a diode between the $\mathrm{V}_{\mathbb{I N}}$ and $\mathrm{V}_{\mathrm{OUT}}$ terminals that is normally reverse-biased. Forcing the output above the input will turn on this diode and may induce a latch-up mode which can damage the part (see Application Hints).
Note 6: Limits are $100 \%$ production tested at $25^{\circ}$ C. Limits over the operating temperature range are guaranteed through correlation using Statistical Quality Control (SQC) methods. The limits are used to calculate National's Average Outgoing Quality Level (AOQL).
Note 7: Dropout voltage is defined as the input to output differential at which the output voltage drops 100 mV below the value measured with a 1 V differential.
Note 8: To prevent mis-operation, the Shutdown input must be driven by a signal that swings above $\mathrm{V}_{\mathrm{H}}$ and below $\mathrm{V}_{\mathrm{L}}$ with a slew rate not less than $40 \mathrm{mV} / \mu \mathrm{s}$ (see Application Hints)
Note 9: Temperature coefficient is defined as the maximum (worst-case) change divided by the total temperature range.
Note 10: $\mathrm{V}_{\mathrm{FB}} \leq \mathrm{V}_{\mathrm{OUT}} \leq\left(\mathrm{V}_{\mathrm{IN}}-1\right), 2.5 \mathrm{~V} \leq \mathrm{V}_{\mathrm{IN}} \leq 16 \mathrm{~V}, 100 \mu \mathrm{~A} \leq \mathrm{I}_{\mathrm{L}} \leq 200 \mathrm{~mA}, \mathrm{~T}_{\mathrm{J}} \leq 125^{\circ} \mathrm{C}$.
Note 11: See Typical Performance Characteristics curves.

Typical Performance Characteristics Unless othervise speciied: $\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}, \mathrm{C}_{\mathrm{out}}=4.7 \mu \mathrm{~F}$, $\mathrm{C}_{\mathbb{N}}=2.2 \mu \mathrm{~F}, \mathrm{~S} / \mathrm{D}$ is tied to $\mathrm{V}_{\mathbb{N}}, \mathrm{V}_{\mathbb{I N}}=\mathrm{V}_{\mathrm{O}}(\mathrm{NOM})+1 \mathrm{~V}, \mathrm{~L}_{\mathrm{L}}=1 \mathrm{~mA}$.


Dropout Voltage vs Load Current


Ground Pin Current vs Temperature and Load


Dropout Voltage vs Temperature


## Dropout Characteristics



DS012935-13
Ground Pin Current vs Load Current


Typical Performance Characteristics Unless otherwise speciified: $T_{A}=25^{\circ} \mathrm{C}, \mathrm{C}_{\text {out }}=4.7 \mathrm{\mu F}$, $\mathrm{C}_{\mathrm{IN}}=2.2 \mu \mathrm{~F}, \mathrm{~S} / \mathrm{D}$ is tied to $\mathrm{V}_{\mathrm{IN}}, \mathrm{V}_{\mathrm{IN}}=\mathrm{V}_{\mathrm{O}}(\mathrm{NOM})+1 \mathrm{~V}, \mathrm{I}_{\mathrm{L}}=1 \mathrm{~mA}$. (Continued)

$50 \mu \mathrm{~s} / \mathrm{Div}$
DS012935-16

$50 \mu \mathrm{~s} / \mathrm{Div}$


Load Transient Response

$50 \mu \mathrm{~s} / \mathrm{Div}$
DS012935-17
Line Transient Response

$20 \mu \mathrm{~s} / \mathrm{Div}$ DS012935-20

Typical Performance Characteristics Unless otherwise specified: $\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}, \mathrm{C}_{\mathrm{out}}=4.7 \mu \mathrm{~F}$, $\mathrm{C}_{\mathrm{IN}}=2.2 \mu \mathrm{~F}, \mathrm{~S} / \mathrm{D}$ is tied to $\mathrm{V}_{\mathrm{IN}}, \mathrm{V}_{\mathrm{IN}}=\mathrm{V}_{\mathrm{O}}(\mathrm{NOM})+1 \mathrm{~V}, \mathrm{I}_{\mathrm{L}}=1 \mathrm{~mA}$. (Continued)


## Short Circuit Current



Short Circuit Current vs Output
Voltage


Turn-Off Waveform


Short Circuit Current


Instantaneous Short Circuit Current vs Temperature


Typical Performance Characteristics Unless otherwise specified: $\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}, \mathrm{C}_{\text {out }}=4.7 \mu \mathrm{~F}$, $\mathrm{C}_{\mathrm{IN}}=2.2 \mu \mathrm{~F}, \mathrm{~S} / \mathrm{D}$ is tied to $\mathrm{V}_{\mathrm{IN}}, \mathrm{V}_{\mathrm{IN}}=\mathrm{V}_{\mathrm{O}}(\mathrm{NOM})+1 \mathrm{~V}, \mathrm{I}_{\mathrm{L}}=1 \mathrm{~mA}$. (Continued)


Feedback Bias Current vs Temperature


DS012935-30

Feedback Bias Current vs Load


Shutdown Pin Current vs Shutdown Pin Voltage


Input to Output Leakage vs
Temperature


Typical Performance Characteristics Unless otherwise specified: $\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}, \mathrm{C}_{\text {out }}=4.7 \mu \mathrm{~F}$, $\mathrm{C}_{\mathbb{I N}}=2.2 \mu \mathrm{~F}, \mathrm{~S} / \mathrm{D}$ is tied to $\mathrm{V}_{\mathrm{IN}^{\prime}}, \mathrm{V}_{\mathbb{I N}}=\mathrm{V}_{\mathrm{O}}(\mathrm{NOM})+1 \mathrm{~V}, \mathrm{I}_{\mathrm{L}}=1 \mathrm{~mA}$. (Continued)



## Application Hints

## EXTERNAL CAPACITORS

Like any low-dropout regulator, external capacitors are required to assure stability. These capacitors must be correctly selected for proper performance.
INPUT CAPACITOR: An input capacitor ( $\geq 2.2 \mu \mathrm{~F}$ ) is required between the LP2986 input and ground (amount of capacitance may be increased without limit).
This capacitor must be located a distance of not more than 0.5 " from the input pin and returned to a clean analog ground. Any good quality ceramic or tantalum may be used for this capacitor.
OUTPUT CAPACITOR: The output capacitor must meet the requirement for minimum amount of capacitance and also have an appropriate E.S.R. (equivalent series resistance) value.

Curves are provided which show the allowable ESR range as a function of load current for various output voltages and capacitor values (see ESR curves below).

## ESR Curves For 5V Output



ESR Curves For 2.5V Output


IMPORTANT: The output capacitor must maintain its ESR in the stable region over the full operating temperature range of the application to assure stability.
The minimum required amount of output capacitance is $4.7 \mu \mathrm{~F}$. Output capacitor size can be increased without limit. It is important to remember that capacitor tolerance and variation with temperature must be taken into consideration
when selecting an output capacitor so that the minimum required amount of output capacitance is provided over the full operating temperature range. A good Tantalum capacitor will show very little variation with temperature, but a ceramic may not be as good (see next section).

## CAPACITOR CHARACTERISTICS

TANTALUM: The best choice for size, cost, and performance are solid tantalum capacitors. Available from many sources, their typical ESR is very close to the ideal value required on the output of many LDO regulators.
Tantalums also have good temperature stability: a $4.7 \mu \mathrm{~F}$ was tested and showed only a $10 \%$ decline in capacitance as the temperature was decreased from $+125^{\circ} \mathrm{C}$ to $-40^{\circ} \mathrm{C}$. The ESR increased only about 2:1 over the same range of temperature.
However, it should be noted that the increasing ESR at lower temperatures present in all tantalums can cause oscillations when marginal quality capacitors are used (where the ESR of the capacitor is near the upper limit of the stability range at room temperature).
CERAMIC: For a given amount of a capacitance, ceramics are usually larger and more costly than tantalums.
Be warned that the ESR of a ceramic capacitor can be low enough to cause instability: a $2.2 \mu \mathrm{~F}$ ceramic was measured and found to have an ESR of about $15 \mathrm{~m} \Omega$.
If a ceramic capacitor is to be used on the LP2986 output, a $1 \Omega$ resistor should be placed in series with the capacitor to provide a minimum ESR for the regulator.
Another disadvantage of ceramic capacitors is that their capacitance varies a lot with temperature:
Large ceramic capacitors are typically manufactured with the Z5U temperature characteristic, which results in the capacitance dropping by a $50 \%$ as the temperature goes from $25^{\circ} \mathrm{C}$ to $80^{\circ} \mathrm{C}$.
This means you have to buy a capacitor with twice the minimum $\mathrm{C}_{\text {Out }}$ to assure stable operation up to $80^{\circ} \mathrm{C}$.
ALUMINUM: The large physical size of aluminum electrolytics makes them unattractive for use with the LP2986. Their ESR characteristics are also not well suited to the requirements of LDO regulators.
The ESR of an aluminum electrolytic is higher than a tantalum, and it also varies greatly with temperature.
A typical aluminum electrolytic can exhibit an ESR increase of 50 X when going from $20^{\circ} \mathrm{C}$ to $-40^{\circ} \mathrm{C}$. Also, some aluminum electrolytics can not be used below $-25^{\circ} \mathrm{C}$ because the electrolyte will freeze.

## USING AN EXTERNAL RESISTIVE DIVIDER

The LP2986 output voltage can be programmed using an external resistive divider (see Basic Application Circuits).
The resistor connected between the Feedback pin and ground should be 51.1 k . The value for the other resistor (R1) connected between the Feedback pin and the regulated output is found using the formula:

$$
\mathrm{V}_{\text {OUT }}=1.23 \times(1+\mathrm{R} 1 / 51.1 \mathrm{k})
$$

It should be noted that the $25 \mu \mathrm{~A}$ of current flowing through the external divider is approximately equal to the current saved by not connecting the internal divider, which means the quiescent current is not increased by using external resistors.

## Application Hints (Continued)

A lead compensation capacitor $\left(\mathrm{C}_{\mathrm{F}}\right)$ must also be used to place a zero in the loop response at about 50 kHz . The value for $\mathrm{C}_{\mathrm{F}}$ can be found using:

$$
C_{F}=1 /(2 \pi \times R 1 \times 50 k)
$$

A good quality capacitor must be used for $\mathrm{C}_{\mathrm{F}}$ to ensure that the value is accurate and does not change significantly over temperature. Mica or ceramic capacitors can be used, assuming a tolerance of $\pm 20 \%$ or better is selected.
If a ceramic is used, select one with a temperature coefficient of NPO, COG, Y5P, or X7R. Capacitor types Z5U, Y5V, and $\mathrm{Z4V}$ can not be used because their value varies more that $50 \%$ over the $-25^{\circ} \mathrm{C}$ to $+85^{\circ} \mathrm{C}$ temperature range.

## SHUTDOWN INPUT OPERATION

The LP2986 is shut off by driving the Shutdown input low, and turned on by pulling it high. If this feature is not to be used, the Shutdown input should be tied to $\mathrm{V}_{\mathrm{IN}}$ to keep the regulator output on at all times.
To assure proper operation, the signal source used to drive the Shutdown input must be able to swing above and below the specified turn-on/turn-off voltage thresholds listed as $\mathrm{V}_{\mathrm{H}}$ and $\mathrm{V}_{\mathrm{L}}$, respectively (see Electrical Characteristics).

It is also important that the turn-on (and turn-off) voltage signals applied to the Shutdown input have a slew rate which is not less than $40 \mathrm{mV} / \mu \mathrm{s}$.
CAUTION: the regulator output state can not be guaranteed if a slow-moving AC (or DC) signal is applied that is in the range between $\mathrm{V}_{\mathrm{H}}$ and $\mathrm{V}_{\mathrm{L}}$.

## REVERSE INPUT-OUTPUT VOLTAGE

The PNP power transistor used as the pass element in the LP2986 has an inherent diode connected between the regulator output and input.
During normal operation (where the input voltage is higher than the output) this diode is reverse-biased.
However, if the output is pulled above the input, this diode will turn ON and current will flow into the regulator output.
In such cases, a parasitic SCR can latch which will allow a high current to flow into $\mathrm{V}_{\mathrm{IN}}$ (and out the ground pin), which can damage the part
In any application where the output may be pulled above the input, an external Schottky diode must be connected from $\mathrm{V}_{\text {IN }}$ to $\mathrm{V}_{\text {OUT }}$ (cathode on $\mathrm{V}_{\text {IN }}$, anode on $\mathrm{V}_{\text {OUT }}$ ), to limit the reverse voltage across the LP2986 to 0.3V (see Absolute Maximum Ratings).

Physical Dimensions inches (millimeters)


Physical Dimensions inches (millimeters) (Continued)


8-Lead (0.150" Wide) Molded Small Outline Package, JEDEC NS Package Number M08A

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# Switch-Capacitor Converters and Controllers 

- LM2660/1 Switched Capacitor Voltage Converter
- LM3460 Precision Controller for GTLp and GTL Bus Termination




## Test Circuits



FIGURE 1. LM2660 and LM2661 Test Circuits
Typical Performance Characteristics (Circuit of Figure 1)


Output Source
Resistance vs Supply
Voltage



## Efficiency vs Load

 Current

Output Voltage Drop vs Load Current


Typical Performance Characteristics (Circuit of Figure 1) (Continued)


Oscillator Frequency
vs Supply Voltage vs Supply Voltage
( $\mathrm{FC}=\mathrm{V}_{+}$)


Output Voltage vs
Oscillator Frequency


Oscillator Frequency vs Supply Voltage (FC = Open)



Oscillator Frequency vs Temperature ( $\mathrm{FC}=\mathrm{V}+$ )



## Connection Diagrams

## 8-Lead SO (M) or Mini SO (MM)



Top View
Order Number LM2660M, LM2661M, LM2660MM or LM2661MM See NS Package Number M08A and MUA08A

## Ordering Information

| Order Number | Package Number | Package Marking | Supplied As |
| :--- | :--- | :--- | :--- |
| LM2660M | M08A | Datecode | Rail (95 units/rail) |
|  |  | LM26 |  |
| LM2660MX | M08A | Datecode | Tape and Reel (2500 units/rail) |
|  |  | LM26 |  |
| LM2660MM | MUA08A | S01A (Note 8) | Tape and Reel (250 units/rail) |
| LM2660MMX | MUA08A | S01A (Note 8) | Tape and Reel (3500 units/rail) |
| LM2661M | M08A | Datecode | Rail (95 units/rail) |
|  |  | LM26 |  |
| LM2661MX | M08A | Datecode | Tape and Reel (2500 units/rail) |
|  |  | LM26 |  |
| LM2661MM | MUA08A | S02A (Note 8) | Tape and Reel (250 units/rail) |
| LM2661MMX | MUA08A | Tape and Reel (3500 units/rail) |  |

Note 8: The first letter " S " identifies the part as a switched capacitor converter. The next two numbers are the device number: " 01 " for a LM 2660 device, and " 02 " for a LM2661 device. The fourth letter "A" indicates the grade. Only one grade is available. Larger quantity reels are available upon request.

## Pin Description

| Pin | Name | Function |  |
| :---: | :---: | :---: | :---: |
|  |  | Voltage Inverter | Voltage Doubler |
| 1 | $\begin{gathered} \text { FC } \\ (\text { LM2660) } \end{gathered}$ | Frequency control for internal oscillator: $\begin{aligned} & \mathrm{FC}=o \mathrm{open}, \mathrm{f}_{\mathrm{Osc}}=10 \mathrm{kHz}(\mathrm{typ}) ; \\ & \mathrm{FC}=\mathrm{V}+, \mathrm{f}_{\mathrm{OSC}}=80 \mathrm{kHz}(\mathrm{typ}) ; \end{aligned}$ <br> FC has no effect when OSC pin is driven externally. | Same as inverter. |
| 1 | $\begin{gathered} \hline \text { SD } \\ \text { (LM2661) } \end{gathered}$ | Shutdown control pin, tie this pin to the ground in normal operation, and to $\mathrm{V}+$ for shutdown. | Same as inverter. |
| 2 | CAP+ | Connect this pin to the positive terminal of charge-pump capacitor. | Same as inverter. |
| 3 | GND | Power supply ground input. | Power supply positive voltage input. |
| 4 | CAP- | Connect this pin to the negative terminal of charge-pump capacitor. | Same as inverter. |
| 5 | OUT | Negative voltage output. | Power supply ground input. |
| 6 | LV | Low-voltage operation input. Tie LV to GND when input voltage is less than 3.5 V . Above 3.5 V , LV can be connected to GND or left open. When driving OSC with an external clock, LV must be connected to GND. | LV must be tied to OUT. |
| 7 | OSC | Oscillator control input. OSC is connected to an internal 15 pF capacitor. An external capacitor can be connected to slow the oscillator. Also, an external clock can be used to drive OSC. | Same as inverter except that OSC cannot be driven by an external clock. |
| 8 | V+ | Power supply positive voltage input. | Positive voltage output. |

## Circuit Description

The LM2660/LM2661 contains four large CMOS switches which are switched in a sequence to invert the input supply voltage. Energy transfer and storage are provided by external capacitors. Figure 2 illustrates the voltage conversion scheme. When $\mathrm{S}_{1}$ and $\mathrm{S}_{3}$ are closed, $\mathrm{C}_{1}$ charges to the supply voltage $V+$. During this time interval switches $S_{2}$ and $S_{4}$ are open. In the second time interval, $\mathrm{S}_{1}$ and $\mathrm{S}_{3}$ are open and $\mathrm{S}_{2}$ and $\mathrm{S}_{4}$ are closed, $\mathrm{C}_{1}$ is charging $\mathrm{C}_{2}$. After a number of cycles, the voltage across $C_{2}$ will be pumped to $V+$. Since the anode of $\mathrm{C}_{2}$ is connected to ground, the output at the cathode of $\mathrm{C}_{2}$ equals $-(\mathrm{V}+)$ assuming no load on $\mathrm{C}_{2}$, no loss in the switches, and no ESR in the capacitors. In reality, the charge transfer efficiency depends on the switching frequency, the on-resistance of the switches, and the ESR of the capacitors.


DS012911-21
FIGURE 2. Voltage Inverting Principle

## Application Information

## SIMPLE NEGATIVE VOLTAGE CONVERTER

The main application of LM2660/LM2661 is to generate a negative supply voltage. The voltage inverter circuit uses only two external capacitors as shown in the Basic Application Circuits. The range of the input supply voltage is 1.5 V to 5.5 V . For a supply voltage less than 3.5 V , the LV pin must be connected to ground to bypass the internal regulator circuitry. This gives the best performance in low voltage applications. If the supply voltage is greater than 3.5 V , LV may be connected to ground or left open. The choice of leaving LV open simplifies the direct substitution of the LM2660/ LM2661 for the LMC7660 Switched Capacitor Voltage Converter.

The output characteristics of this circuit can be approximated by an ideal voltage source in series with a resistor. The voltage source equals $-\left(V_{+}\right)$. The output resistance $R_{\text {out }}$ is a function of the ON resistance of the internal MOS switches, the oscillator frequency, and the capacitance and ESR of $\mathrm{C}_{1}$ and $C_{2}$. A good approximation is:

$$
R_{\text {out }} \cong 2 R_{S W}+\frac{2}{f_{\text {osc }} \times C_{1}}+4 E S R_{C 1}+E S R_{C 2}
$$

where $R_{S W}$ is the sum of the $O N$ resistance of the internal MOS switches shown in Figure 2.
High value, low ESR capacitors will reduce the output resistance. Instead of increasing the capacitance, the oscillator frequency can be increased to reduce the $2 /\left(\mathrm{f}_{\text {osc }} \times \mathrm{C}_{1}\right)$ term. Once this term is trivial compared with $\mathrm{R}_{\mathrm{Sw}}$ and ESRs, further increasing in oscillator frequency and capacitance will become ineffective.

## Application Information (Continued)

The peak-to-peak output voltage ripple is determined by the oscillator frequency, and the capacitance and ESR of the output capacitor $\mathrm{C}_{2}$ :

$$
V_{\text {ripple }}=\frac{L_{L}}{f_{\text {osc }} \times C_{2}}+2 \times I_{L} \times E S R_{C 2}
$$

Again, using a low ESR capacitor will result in lower ripple.

## POSITIVE VOLTAGE DOUBLER

The LM2660/LM2661 can operate as a positive voltage doubler (as shown in the Basic Application Circuits). The doubling function is achieved by reversing some of the connections to the device. The input voltage is applied to the GND pin with an allowable voltage from 2.5 V to 5.5 V . The $\mathrm{V}+$ pin is used as the output. The LV pin and OUT pin must be connected to ground. The OSC pin can not be driven by an external clock in this operation mode. The unloaded output voltage is twice of the input voltage and is not reduced by the diode $\mathrm{D}_{1}$ 's forward drop.
The Schottky diode $D_{1}$ is only needed for start-up. The internal oscillator circuit uses the $\mathrm{V}+\mathrm{pin}$ and the LV pin (connected to ground in the voltage doubler circuit) as its power rails. Voltage across $\mathrm{V}+$ and LV must be larger than 1.5 V to insure the operation of the oscillator. During start-up, $D_{1}$ is used to charge up the voltage at $\mathrm{V}+$ pin to start the oscillator; also, it protects the device from turning-on its own parasitic diode and potentially latching-up. Therefore, the Schottky diode $D_{1}$ should have enough current carrying capability to charge the output capacitor at start-up, as well as a low forward voltage to prevent the internal parasitic diode from turning-on. A Schottky diode like 1N5817 can be used for most applications. If the input voltage ramp is less than $10 \mathrm{~V} /$ ms , a smaller Schottky diode like MBR0520LT1 can be used to reduce the circuit size.

## SPLIT V+ IN HALF

Another interesting application shown in the Basic Application Circuits is using the LM2660/LM2661 as a precision voltage divider. Since the off-voltage across each switch equals $\mathrm{V}_{\text {IN }} / 2$, the input voltage can be raised to +11 V .

## CHANGING OSCILLATOR FREQUENCY

For the LM2660, the internal oscillator frequency can be selected using the Frequency Control (FC) pin. When FC is open, the oscillator frequency is 10 kHz ; when FC is connected to $\mathrm{V}_{+}$, the frequency increases to 80 kHz . A higher oscillator frequency allows smaller capacitors to be used for equivalent output resistance and ripple, but increases the typical supply current from 0.12 mA to 1 mA .
The oscillator frequency can be lowered by adding an external capacitor between OSC and GND. (See Typical Performance Characteristics.) Also, in the inverter mode, an external clock that swings within 100 mV of $\mathrm{V}+$ and GND can be used to drive OSC. Any CMOS logic gate is suitable for driving OSC. LV must be grounded when driving OSC. The maximum external clock frequency is limited to 150 kHz .
The switching frequency of the converter (also called the charge pump frequency) is half of the oscillator frequency. Note: OSC cannot be driven by an external clock in the voltage-doubling mode.

TABLE 1. LM2660 Oscillator Frequency Selection

| FC | OSC | Oscillator |
| :--- | :--- | :--- |
| Open | Open | 10 kHz |
| V+ | Open | 80 kHz |
| Open or $\mathrm{V}_{+}$ | External Capacitor | See Typical |
|  |  | Performance |
| N/A |  | Characteristics |
|  | External Clock | External Clock |
|  | (inverter mode only) | Frequency |

TABLE 2. LM2661 Oscillator Frequency Selection

| OSC | Oscillator |
| :--- | :--- |
| Open | 80 kHz |
| External Capacitor | See Typical Performance |
|  | Characteristics |
| External Clock | External Clock Frequency |
| (inverter mode only) |  |

## SHUTDOWN MODE

For the LM2661, a shutdown (SD) pin is available to disable the device and reduce the quiescent current to $0.5 \mu \mathrm{~A}$. Applying a voltage greater than 2 V to the SD pin will bring the device into shutdown mode. While in normal operating mode, the SD pin is connected to ground.

## CAPACITOR SELECTION

As discussed in the Simple Negative Voltage Converter section, the output resistance and ripple voltage are dependent on the capacitance and ESR values of the external capacitors. The output voltage drop is the load current times the output resistance, and the power efficiency is

$$
\eta=\frac{P_{\text {out }}}{P_{\text {in }}}=\frac{I_{L}{ }^{2} R_{L}}{I_{L}{ }^{2} R_{L}+I_{L}{ }^{2} R_{\text {out }}+I_{Q}(V+)}
$$

Where $I_{Q}\left(V_{+}\right)$is the quiescent power loss of the IC device, and $I_{L}{ }^{2} R_{\text {OUT }}$ is the conversion loss associated with the switch on-resistance, the two external capacitors and their ESRs.
Since the switching current charging and discharging $\mathrm{C}_{1}$ is approximately twice as the output current, the effect of the ESR of the pumping capacitor $\mathrm{C}_{1}$ is multiplied by four in the output resistance. The output capacitor $\mathrm{C}_{2}$ is charging and discharging at a current approximately equal to the output current, therefore, its ESR only counts once in the output resistance. However, the ESR of $\mathrm{C}_{2}$ directly affects the output voltage ripple. Therefore, low ESR capacitors (Table 3) are recommended for both capacitors to maximize efficiency, reduce the output voltage drop and voltage ripple. For convenience, $\mathrm{C}_{1}$ and $\mathrm{C}_{2}$ are usually chosen to be the same.
The output resistance varies with the oscillator frequency and the capacitors. In Figure 3, the output resistance vs. oscillator frequency curves are drawn for three different tantalum capacitors. At very low frequency range, capacitance plays the most important role in determining the output resis tance. Once the frequency is increased to some point (such as 20 kHz for the $150 \mu \mathrm{~F}$ capacitors), the output resistance is dominated by the ON resistance of the internal switches and the ESRs of the external capacitors. A low value, smaller

## Application Information <br> (Continued)

size capacitor usually has a higher ESR compared with a bigger size capacitor of the same type. For lower ESR, use ceramic capacitors.


FIGURE 3. Output Source Resistance vs Oscillator Frequency
TABLE 3. Low ESR Capacitor Manufacturers

| Manufacturer | Phone | FAX | Capacitor Type |
| :--- | :---: | :---: | :--- |
| Nichicon Corp. | $(708)-843-7500$ | $(708)-843-2798$ | PL, PF series, through-hole aluminum electrolytic |
| AVX Corp. | $(803)-448-9411$ | $(803)-448-1943$ | TPS series, surface-mount tantalum |
| Sprague | $(207)-324-4140$ | $(207)-324-7223$ | 593D, 594D, 595D series, surface-mount tantalum |
| Sanyo | $(619)-661-6835$ | $(619)-661-1055$ | OS-CON series, through-hole aluminum electrolytic |

## Other Applications

## PARALLELING DEVICES

Any number of LM2660s (or LM2661s) can be paralleled to reduce the output resistance. Each device must have its own pumping capacitor $\mathrm{C}_{1}$, while only one output capacitor $\mathrm{C}_{\text {out }}$ is needed as shown in Figure 4. The composite output resistance is:

$$
R_{\text {out }}=\frac{R_{\text {out }} \text { of each LM2660 (or LM2661) }}{\text { Number of Devices }}
$$



DS012911-22
FIGURE 4. Lowering Output Resistance by Paralleling Devices

## Other Applications (Continued)

## CASCADING DEVICES

Cascading the LM2660s (or LM2661s) is an easy way to produce a greater negative voltage (as shown in Figure 5). If n is the integer representing the number of devices cascaded, the unloaded output voltage $\mathrm{V}_{\text {out }}$ is $\left(-\mathrm{n} \mathrm{V}_{\text {in }}\right)$. The effective output resistance is equal to the weighted sum of each individual device:

$$
R_{\text {out }}=n R_{\text {out }}^{-1} 1+\frac{n}{2} R_{\text {out }_{-} 2}+\ldots+R_{\text {out }} n
$$

A three-stage cascade circuit shown in Figure 6 generates $-3 \mathrm{~V}_{\mathrm{in}}$, from $\mathrm{V}_{\text {in }}$.
Cascading is also possible when devices are operating in doubling mode. In Figure 7 , two devices are cascaded to generate $3 \mathrm{~V}_{\text {in }}$. An example of using the circuit in Figure 6 or Figure 7 is generating +15 V or -15 V from a +5 V input.
Note that, the number of $n$ is practically limited since the increasing of $n$ significantly reduces the efficiency and increases the output resistance and output voltage ripple.


DS012911-23
FIGURE 5. Increasing Output Voltage by Cascading Devices


FIGURE 6. Generating $-3 V_{\text {in }}$ from $+V_{\text {in }}$


DS012911-25
FIGURE 7. Generating $+3 \mathrm{~V}_{\text {in }}$ from $+\mathrm{V}_{\text {in }}$

Other Applications (Continued)
REGULATING $V_{\text {out }}$
It is possible to regulate the output of the LM2660/LM2661 by use of a low dropout regulator (such as LP2951). The whole converter is depicted in Figure 8. This converter can give a regulated output from -1.5 V to -5.5 V by choosing the proper resistor ratio:

$$
V_{\text {out }}=V_{\text {ref }}\left(1+\frac{R_{1}}{R_{2}}\right)
$$

where, $V_{\text {ref }}=1.235 \mathrm{~V}$
The error flag on pin 5 of the LP2951 goes low when the regulated output at pin 4 drops by about 5\%. The LP2951 can be shutdown by taking pin 3 high.


FIGURE 8. Combining LM2660/LM2661 with LP2951 to Make a Negative Adjustable Regulator
Also, as shown in Figure 9 by operating LM2660/LM2661 in voltage doubling mode and adding a linear regulator (such as LP2981) at the output, we can get +5 V output from an input as low as +3 V .


FIGURE 9. Generating +5 V from +3 V Input Voltage

Physical Dimensions inches (millimeters)


Physical Dimensions inches (millimeters) (Continued)


8-Lead Mini SO (MM)
Order Number LM2660MM or LM2661MM
NS Package Number MUA08A

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## Typical Applications



FIGURE 1. 1.5V Typical Application (See Application Information Section)


FIGURE 2. 1.2V Typical Application (See Application Information Section)

| Absolute Maximum Ratings (Note 1) |  |
| :---: | :---: |
| If Military/Aerospace specified dev please contact the National Sem Office/Distributors for availability an | ces are required, iconductor Sales specifications. |
| Input Voltage ( $\mathrm{V}_{\text {IN }}$ ) | 20 V |
| Output Current | 20 mA |
| Junction Temperature | $150^{\circ} \mathrm{C}$ |
| Storage Temperature | $-65^{\circ} \mathrm{C}$ to $+150^{\circ} \mathrm{C}$ |
| Lead Temperature |  |
| Vapor Phase ( 60 sec .) <br> Infrared ( 15 sec .) | $\begin{aligned} & +25^{\circ} \mathrm{C} \\ & +220^{\circ} \mathrm{C} \end{aligned}$ |
| Power Dissipation ( $\left.\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\right)($ (Note 2) | 300 mW |

ESD Susceptibility (Note 3)
Human Body Model
1500 V
See AN-450 "Surface Mounting Methods and Their Effect on Product Reliability" for methods on soldering surfacemount devices.

Operating Ratings (Notes 1and 2)

$$
\text { Ambient Temperature Range } \quad 0^{\circ} \mathrm{C} \leq \mathrm{T}_{\mathrm{A}} \leq+70^{\circ} \mathrm{C}
$$

Output Current
1 mA

## LM3460-1.5

Electrical Characteristics Specifications with standard type face are for $\mathrm{T}_{J}=25^{\circ} \mathrm{C}$, and those with boldface type apply over full Operating Temperature Range. Unless otherwise specified, ( + ) IN $=\mathrm{V}_{\text {REG }}, \mathrm{V}_{\text {OUT }}=200 \mathrm{mV}$

| Symbol | Parameter | Conditions | Typical (Note 4) | $\begin{aligned} & \text { LM3460-1.5 } \\ & \text { Limit (Note 5) } \end{aligned}$ | Units |
| :---: | :---: | :---: | :---: | :---: | :---: |
| $\mathrm{V}_{\text {REG }}$ | Regulated Voltage | lout $=1 \mathrm{~mA}$ | 1.5 | $\begin{aligned} & 1.515 / 1.530 \\ & 1.485 / 1.470 \end{aligned}$ | $\begin{aligned} & V(\max ) \\ & V(\min ) \end{aligned}$ |
|  | Regulated Voltage Tolerance | lout $=1 \mathrm{~mA}$ |  | $\pm 1 / \pm 2$ | \% (max) |
| $\mathrm{I}_{\mathrm{q}}$ | Quiescent Current | lout $=1 \mathrm{~mA}$ | 85 | 125/150 | $\mu \mathrm{A}$ (max) |
| $\mathrm{G}_{\mathrm{m}}$ | Transconductance $\Delta \mathrm{l}_{\text {OUT }} / \Delta \mathrm{V}_{\text {REG }}$ | $\begin{aligned} & 20 \mu \mathrm{~A} \leq \mathrm{I}_{\text {OUT }} \leq 1 \mathrm{~mA} \\ & \mathrm{~V}_{\text {OUT }}=500 \mathrm{mV} \end{aligned}$ | 3.3 | 1/0.5 | $\mathrm{mA} / \mathrm{mV}$ (min) |
| $\mathrm{V}_{\text {SAT }}$ | Output Saturation Voltage (Note 6) | $\begin{aligned} & \mathrm{V}_{\mathrm{IN}}=\mathrm{V}_{\mathrm{REG}}+100 \mathrm{mV} \\ & \mathrm{I}_{\mathrm{OUT}}=1 \mathrm{~mA} \end{aligned}$ | 0.8 | 0.95 | $V$ (max) |
| $I_{L}$ | Output Leakage Current | $\begin{aligned} & \mathrm{V}_{\text {IN }}=\mathrm{V}_{\text {REG }}-100 \mathrm{mV} \\ & \mathrm{~V}_{\text {OUT }}=0 \mathrm{~V} \end{aligned}$ | 0.1 | 0.5/1.0 | $\mu \mathrm{A}$ (max) |
| $\mathrm{R}_{\mathrm{F}}$ | Internal Feedback Resistor (See Functional Diagram) |  | 7.1 | $\begin{aligned} & 8.9 \\ & 5.3 \\ & \hline \end{aligned}$ | $k \Omega$ (max) <br> $k \Omega$ (min) |
| $E_{n}$ | Output Noise Voltage | lout $=1 \mathrm{~mA}, 10 \mathrm{~Hz} \leq \mathrm{f} \leq 10 \mathrm{kHz}$ | 50 |  | $\mu \mathrm{V}$ (rms) |

## LM3460-1.2

Electrical Characteristics Specifications with standard type face are for $T_{J}=25^{\circ} \mathrm{C}$, and those with boldface type apply over full Operating Temperature Range. Unless otherwise specified, ( + ) $\mathrm{IN}=\mathrm{V}_{\text {REG }}, \mathrm{V}_{\text {OUT }}=200 \mathrm{mV}$

| Symbol | Parameter | Conditions | Typical (Note 4) | $\begin{aligned} & \text { LM3460-1.2 } \\ & \text { Limit (Note 5) } \end{aligned}$ | Units |
| :---: | :---: | :---: | :---: | :---: | :---: |
| $\mathrm{V}_{\text {REG }}$ | Regulated Voltage | $\mathrm{I}_{\text {OUT }}=1 \mathrm{~mA}$ | 1.220 | $\begin{aligned} & 1.232 / 1.244 \\ & 1.208 / 1.196 \end{aligned}$ | $\begin{aligned} & V(\max ) \\ & V(\min ) \end{aligned}$ |
|  | Regulated Voltage Tolerance | l OUT $=1 \mathrm{~mA}$ |  | $\pm 1 / \pm 2$ | \% (max) |
| $\mathrm{I}_{\mathrm{q}}$ | Quiescent Current | IOUT $=1 \mathrm{~mA}$ | 85 | 125/150 | $\mu \mathrm{A}$ (max) |
| $\mathrm{G}_{\mathrm{m}}$ | Transconductance $\Delta$ lout $/ \Delta V_{\text {REG }}$ | $\begin{aligned} & 20 \mu \mathrm{~A} \leq \mathrm{I} \text { OUT } \leq 1 \mathrm{~mA} \\ & \mathrm{~V}_{\text {OUT }}=200 \mathrm{mV} \end{aligned}$ | 3.3 | 1/0.5 | $\mathrm{mA} / \mathrm{mV}$ (min) |
| $\mathrm{V}_{\text {SAT }}$ | Output Saturation Voltage (Note 6) | $\begin{aligned} & \mathrm{V}_{\mathrm{IN}}=\mathrm{V}_{\mathrm{REG}}+100 \mathrm{mV} \\ & \mathrm{I}_{\mathrm{OUT}}=1 \mathrm{~mA} \end{aligned}$ | 0.8 | 0.95 | $V$ (max) |
| $I_{L}$ | Output Leakage Current | $\begin{aligned} & \mathrm{V}_{\mathrm{IN}}=\mathrm{V}_{\text {REG }}-100 \mathrm{mV} \\ & \mathrm{~V}_{\text {OUT }}=0 \mathrm{~V} \end{aligned}$ | 0.1 | 0.5/1.0 | $\mu \mathrm{A}$ (max) |
| $\mathrm{R}_{\mathrm{F}}$ | Internal Feedback Resistor (See Functional Diagram) |  | 10 | $\begin{gathered} 12.5 \\ 7.5 \\ \hline \end{gathered}$ | $k \Omega$ (max) $k \Omega$ (min) |
| $E_{n}$ | Output Noise Voltage | IOUT $=1 \mathrm{~mA}, 10 \mathrm{~Hz} \leq \mathrm{f} \leq 10 \mathrm{kHz}$ | 50 |  | $\mu \mathrm{V}$ (rms) |

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but do not guarantee specific performance limits. For guaranteed specifications and test conditions, see the Electrical Characteristics. The guaranteed specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions.
Note 2: The maximum power dissipation must be derated at elevated temperatures and is dictated by $T_{J m a x}$ (maximum junction termperature), $\theta_{J A}$ (junction to ambient thermal resistance), and $T_{A}$ (ambient temperature). The maximum allowable power dissipation at any temperature is ( $P_{D \operatorname{Dax}}=\left(T_{J m a x}-T_{A}\right) / \theta_{J A}$ or the number given in the Absolute Maximum Ratings, whichever is lower. The typical thermal resistance ( $\theta_{J A}$ ) when soldered to a printed circuit board is approximately $330^{\circ} \mathrm{C} / \mathrm{W}$.
Note 3: The human body model is a 100 pF capacitor discharged through a $1.5 \mathrm{k} \Omega$ resistor into each pin.
Note 4: Typical numbers are at $25^{\circ} \mathrm{C}$ and represent the most likely parametric norm.
Note 5: Limits are $100 \%$ production tested at $25^{\circ} \mathrm{C}$. Limits over the operating temperature range are guaranteed through correlation using Statistical Quality Control (SQC) methods. The limits are used to calculate National's Average Outgoing Quality Level (AOQL).
Note 6: $\mathrm{V}_{\text {SAT }}=\mathrm{V}_{\text {REG }}-\mathrm{V}_{\text {OUT }}$, when the voltage at the $I \mathrm{~N}$ pin is forced 100 mV above the nominal regulating voltage $\left(\mathrm{V}_{\text {REG }}\right)$.

## Product Description

The LM3460 is a shunt regulator designed for use as a precision control element in a feedback loop. The regulated output voltage is sensed between the IN pin and GROUND pin of the LM3460.
The output of the LM3460 sources current whenever the voltage at the IN pin reaches the regulated voltage.
This current is used to cut off the drive to the external pass transistor, which provides the negative feedback to force the output voltage to be the same value as $V_{\text {REG }}$.
If the voltage on the IN pin is forced above the $\mathrm{V}_{\text {REG }}$ voltage, the maximum voltage applied to the IN pin should not exceed 20V. In addition, an external resistor may be required on the OUT pin to limit the maximum current to 20 mA .

## Compensation

The inverting input of the error amplifier is brought out to simplify closed-loop compensation. Typically, compensation is provided by a single capacitor connected from the COMPENSATION pin to the OUT pin of the LM3460.
Applying a load pulse to the output of the regulator circuit and observing the output voltage response is a good method of verifying the stability of the control loop.
If excessive ringing on the output waveform is observed, this usually indicates marginal stability resulting from insufficient phase margin.

## Test Circuit

The test circuit shown in Figure 3 can be used to measure various LM3460 parameters. Test conditions are set by forcing the appropriate voltage at the VOUT Set test point and selecting the appropriate $R_{L}$ or IOUT as specified in the Electrical Characteristics section. Use a DVM at the "measure" test points to read the data.


TL/H/12603-9
FIGURE 3. Test Circuit
Vout Set Note: OV to 500 mV for LM3460-1.5
OV to 200 mV for LM3460-1.2

## Setting the Output Voltage

If a regulated output voltage is desired which is not available as a standard voltage, the output voltage may be adjusted by using an external resistive divider (see Figure 4):


TL/H/12603-10

$$
\begin{aligned}
\mathrm{V}_{\mathrm{OUT}} & =1.22+\left(\frac{1.22}{R_{\mathrm{A}}}\right) \mathrm{R}_{\mathrm{B}} \\
\mathrm{R}_{\mathrm{B}} & =\frac{\left(\mathrm{V}_{\mathrm{OUT}}-1.22\right) \mathrm{R}_{\mathrm{A}}}{1.22}
\end{aligned}
$$

## FOR BEST RESULTS: SELECT $R_{A}<500 \Omega$.

FIGURE 4. Setting the Output Voltage
The simplest way to calculate the resistor values is to assume a value for $R_{A}$ and then solve the equation shown for $\mathrm{R}_{\mathrm{B}}$.
To assure best output voltage accuracy, the value selected for $\mathrm{R}_{\mathrm{A}}$ should be $<500 \Omega$, and $1 \%$ tolerance resistors should be used.
As the ohmic value of $R_{A}$ is increased, the internal resistive divider inside the LM3460 will cause the output voltage to deviate from the value predicted by the formula shown.

## App Circuit Technical Information

Figure 1 and Figure 2 (shown on page 2 of this document) highlight two applications of the LM3460. This section provides details of circuit function.

### 1.5V/7A TYPICAL APPLICATION

Figure 1 shows the schematic of a wide-bandwidth linear regulator which provides a regulated 1.5 V output at up to 7 A of load current from a $3 \mathrm{~V}-3.6 \mathrm{~V}$ input.
The pass element of the regulator (which supplies the load current) is made up of a three-transistor complimentary Darlington composed of Q2, Q3, and Q4. The bias current flowing through R1 will drive the pass element ON, until such time as Q1 pulls down and takes the drive away from the base of Q2.

The circuit regulates the output to 1.5 V using the LM3460 precision controller, which sources current from its output whenever the voltage at the IN pin reaches 1.5 V .
When the LM3460 sources current from its output, it turns on Q1 (stealing the base drive for Q2) which reduces the current from the 1.5 V regulated output. In this way, a negative feedback loop is established which locks the output at 1.5 V .

C1 and C2 are used for compensation, and should be ceramic capacitors.
C4 is required for regulator stability, and both C3 and C4 affect transient response. Circuit performance should be carefully evaluated if substitutions are made for these two components.

## PERFORMANCE DATA

All data taken at $20^{\circ} \mathrm{C}$ ambient:
LOAD/LINE REGULATION: The output voltage changed $<0.1 \mathrm{mV}$ as the load was increased from $0-7 \mathrm{~A}$, and the input voltage was varied from $3.0 \mathrm{~V}-3.6 \mathrm{~V}$.
DROPOUT VOLTAGE: The dropout voltage (which is defined as the minimum input-output voltage differential required to maintain a regulated output) was measured at 7A and found to be 1.4 V . This means that a minimum input voltage of 2.9 V is required to keep the 1.5 V output in regulation.
TRANSIENT RESPONSE: Transient response was tested using a $0.2 \Omega$ power resistor connected to the output using a mechanical contact to provide a 0-7A load current step. When the load was applied, the change in output voltage was seen to be $<5 \mathrm{mV}$ with a total recovery time of about $30 \mu \mathrm{~s}$ (see Figure 5).


FIGURE 5. Output Transient Response

## App Circuit Technical Information (Continued)

## heatsinking/COMPONENT SELECTION

HEATSINKING: As with any linear regulator, the power dissipated in the pass transistor (Q4) is approximately:

$$
\mathrm{P}=\left(\mathrm{V}_{\text {IN }}-\mathrm{V}_{\text {OUT }}\right) \times \mathrm{I}_{\text {LOAD }}
$$

Q4 must be provided with adequate heatsinking so that the junction temperature never exceeds $150^{\circ} \mathrm{C}$.
Figure 6 shows the maximum allowable values of thermal resistance (from heatsink-to-ambient) that must be provided for various values of load current.


TL/H/12306-12

## FIGURE 6. Q4 Heatsink Requirements

 for Circuit Shown in Figure 1These values are calculated assuming a maximum ambient temperature of $50^{\circ} \mathrm{C}, 3.3 \mathrm{~V}$ input, and a TO-220 power transistor mounted using thermal grease and a mica insulator.
A given thermal resistance can be obtained by using different combinations of heatsink and airflow (refer to heatsink manufacturers data sheets).
The design tradeoff here is that heatsinks which are smaller, lighter, and cheaper require more airflow to get the desired value of thermal resistance.
TRANSIENT RESPONSE: If the regulator is to respond quickly to changes in load current demand, the input and output capacitors must be selected carefully.
The output capacitor C4 is most critical, as it must supply current to the load in the time it takes the regulator loop to sense the output voltage change and turn on the pass transistor. A Sanyo Oscon type (or equivalent) will give the best performance here.
The input capacitor C3 is also important, as it provides an energy reservoir from which the regulator sources current to force the output back up to the nominal value. A good, low ESR electrolytic such as a Panasonic HFQ type is a good choice for C3.

LAYOUT TIPS: In order to optimize performance, parasitic inductance due to connecting traces must be minimized. All paths shown as heavy lines on the schematic must be made by traces which are as wide and short as possible (component placement should be optimized for minimum lead length).
POWER TRANSISTOR AND DRIVER: The power transistor used at Q4 must have very good current gain at 7A, and wide bandwidth (high $\mathrm{f}_{\mathrm{T}}$ ) for this circuit to work as specified. The D44H8 is an excellent choice for cost and performance. The current gain of Q4 dictates the power dissipation in its driver (Q3) which must supply the base current to Q4. If the gain of Q4 is lowered, Q3 must source more current into its base (and the power dissipation in Q3 goes up proportionally).
The D44H8 has a guaranteed minimum gain of 40 @ 4A, with typical gain much higher. Assuming the gain of Q4 is about $30 \%$ lower at 7 A , it will still be $>28$. Therefore, to support 7A of load current, Q3 must supply 250 mA to the base of Q4 (worst case).
The power dissipation in Q3 (assuming 3.3 V input) will never exceed approximately 250 mW , which is easily handled by the 2N3906 in a TO-92 case (which has a thermal resistance of about $180^{\circ} \mathrm{C} / \mathrm{W}$ ), but could be a problem for a very small surface mount device.
If substitutions are made for Q3 or Q4, careful attention must be paid to the current gain as well as the $f_{T}$.
TRANSISTOR BANDWIDTH: Fast transient response requires that the regulator be able to respond quickly to any change in output voltage (which will occur if the current drawn by the load suddenly changes).
All of the transistors specified in the schematic are very wide-band devices (have high $\mathrm{f}_{\mathrm{T}}$ values) which is necessary for fast response. If substitutions are made for any of the transistors, this specification must be considered.

### 1.2V/7A TYPICAL APPLICATION

The 1.2V @ 7A design shown in Figure 2 is very similar in function to the design shown in Figure 1. Most of the circuit descriptions previously detailed for that circuit apply unchanged to Figure 2, and will not be repeated.
Detailed information will be presented in the areas which differ between the two circuits.

## HEATSINKING

The 1.2 V design needs a little more heatsinking because the lower output voltage means more power dissipation in Q4 at any value of load current.
Figure 7 shows the maximum allowable values of thermal resistance (from heatsink-to-ambient) that must be provided for various values of load current.

## App Circuit Technical Information (Continued)



TL/H/12603-13

## FIGURE 7. Q4 Heatsink Requirements

 for Circuit Shown in Figure 2
## Q1 DRIVE CIRCUITRY

In the circuit shown in Figure 1, the output of U1 drives the base of Q1 with current when the voltage at $V_{\text {OUT }}$ reaches the regulation point. As Q1 turns ON, it steals drive from Q2 which holds the loop in regulation.
The circuit of Figure 2 uses a different drive configuration for Q1, required because of the lower voltage across U1.
With only 1.2 V across U1, the OUT pin of the LM3460 can not swing up high enough in voltage to turn on the $\mathrm{V}_{\mathrm{BE}}$ of Q1.

In the circuit of Figure 2, drive for Q1 is provided by R7, but only when U1 sources current: The operation of the drive scheme is as follows
If the voltage at $\mathrm{V}_{\text {OUT }}$ is below 1.2 V , no current flows from the OUT pin of U1. Q1 is held OFF as the current flowing down through R7 goes through D1 and R5 to ground.
IMPORTANT: Diode D1 is a 1N4001 because its $\mathrm{V}_{\mathrm{F}}$ must be much less than the $\mathrm{V}_{\mathrm{BE}}$ of Q 1 (a signal diode like 1N4148 will not work here).
When U1 is not sourcing current, the voltage at the OUT pin (and the cathode of D1) will be held at about 50 mV by the R7/D1/R5 divider. The current flowing to ground through these components is about $110 \mu \mathrm{~A}$.
Because D1 is a 1A power diode, the $\mathrm{V}_{\mathrm{F}}$ across D1 at this small value of current will be much less than the $V_{B E}$ needed to turn ON Q1 (so Q1 is held off by D1).
When U1 begins to source current (to cut off the pass transistor and regulate $\mathrm{V}_{\text {OUT }}$ ) it forces the voltage at the cathode of D1 to rise.
This action causes the current that was flowing through D1 to flow into the base of Q1, turning it ON and taking drive away from the base of Q2.
This action provides the negative feedback required to regulate $\mathrm{V}_{\text {OUT }}$ and allows the LM3460 to operate with only 1.2 V of total supply voltage across the device.


Physical Dimensions inches (millimeters) unless otherwise noted


LAND PATTERN RECOMMENDATION

mA05A (REV D)
5-Lead Small Outline Package (M5)
Ordering Number, See Page 1 of this Document NS Package Number MA05A

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## Step-Down DC/DC Converters

- LM2594 0.5A, 150kHz Simple Switcher ${ }^{\text {TM }}$ Converter
- LM2595 1A Version of LM2594
- LM2596 3A Version of LM2594
- LM2597 0.5A, 150kHz, Simple Switcher ${ }^{\text {TM }}$ Converter with Features
- LM2598 1A Version of LM2597
- LM2599 3A Version of LM2597
- LM2650 Synchronous Step-Down DC/DC Converter
- LM2825 Integrated Power Supply (IPS): 1A DC/DC Converter in 24DIL Package



## Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.
Maximum Supply Voltage
45 V
$\overline{\text { ON} / O F F ~ P i n ~ I n p u t ~ V o l t a g e ~} \quad-0.3 \leq \mathrm{V} \leq+25 \mathrm{~V}$
Feedback Pin Voltage $\quad-0.3 \leq \mathrm{V} \leq+25 \mathrm{~V}$
Output Voltage to Ground (Steady State) -1V
Power Dissipation Internally limited
Storage Temperature Range $\quad-65^{\circ} \mathrm{C}$ to $+150^{\circ} \mathrm{C}$
ESD Susceptibility
Human Body Model (Note 2) 2 kV

| Lead Temperature |  |
| :--- | :--- |
| M8 Package | $+215^{\circ} \mathrm{C}$ |
| $\quad$ Vapor Phase (60 sec.) | $+220^{\circ} \mathrm{C}$ |
| $\quad$ Infrared (15 sec.) | $+260^{\circ} \mathrm{C}$ |
| N Package (Soldering, 10 sec.) | $+150^{\circ} \mathrm{C}$ |
| Maximum Junction Temperature |  |
| Operating Conditions |  |


| Temperature Range | $-40^{\circ} \mathrm{C} \leq \mathrm{T}_{\mathrm{J}}+125^{\circ} \mathrm{C}$ |
| :--- | ---: |
| Supply Voltage | 4.5 V to 40 V |

## LM2594-3.3

Electrical Characteristics Specifications with standard type face are for $\mathrm{T}_{J}=25^{\circ} \mathrm{C}$, and those with boldface type apply over full Operating Temperature Range

| Symbol | Parameter | Conditions | LM2594-3.3 |  | Units (Limits) |
| :---: | :---: | :---: | :---: | :---: | :---: |
|  |  |  | Type <br> (Note 3) | Limit (Note 4) |  |
| SYSTEM PARAMETERS (Note 5) Test Circuit Figure 2 |  |  |  |  |  |
| $\mathrm{V}_{\text {OUT }}$ | Output Voltage | $4.75 \mathrm{~V} \leq \mathrm{V}_{\text {IN }} \leq 40 \mathrm{~V}, 0.1 \mathrm{~A} \leq \mathrm{I}_{\text {LOAD }} \leq 0.5 \mathrm{~A}$ | 3.3 | $\begin{aligned} & 3.168 / \mathbf{3 . 1 3 5} \\ & 3.432 / \mathbf{3 . 4 6 5} \end{aligned}$ | $V(\min )$ <br> V(max) |
| $\eta$ | Efficiency | $\mathrm{V}_{\mathrm{IN}}=12 \mathrm{~V}, \mathrm{I}_{\text {LOAD }}=0.5 \mathrm{~A}$ | 80 |  | \% |

LM2594-5.0
Electrical Characteristics Specifications with standard type face are for $\mathrm{T}_{\mathrm{J}}=25^{\circ} \mathrm{C}$, and those with boldface type apply over full Operating Temperature Range

| Symbol | Parameter | Conditions | LM2594-5.0 |  | Units (Limits) |
| :---: | :---: | :---: | :---: | :---: | :---: |
|  |  |  | Type (Note 3) | Limit (Note 4) |  |
| SYSTEM PARAMETERS (Note 5) Test Circuit Figure 2 |  |  |  |  |  |
| V OUT | Output Voltage | $7 \mathrm{~V} \leq \mathrm{V}_{\text {IN }} \leq 40 \mathrm{~V}, 0.1 \mathrm{~A} \leq \mathrm{I}_{\text {LOAD }} \leq 0.5 \mathrm{~A}$ | 5.0 | $\begin{aligned} & 4.800 / 4.750 \\ & 5.200 / 5.250 \end{aligned}$ | $V(\min )$ <br> V (max) |
| $\eta$ | Efficiency | $\mathrm{V}_{\mathrm{IN}}=12 \mathrm{~V}, \mathrm{I}_{\text {LOAD }}=0.5 \mathrm{~A}$ | 82 |  | \% |
| LM2594-12 <br> Electrical Characteristics Speecifications with standard type face are for $\mathrm{T}_{\mathrm{J}}=25^{\circ} \mathrm{C}$, and those with boldface type apply over full Operating Temperature Range |  |  |  |  |  |
|  |  |  |  | 59-12 |  |
| Symbol | Parameter | Conditions | Type (Note 3) | Limit (Note 4) | (Limits) |
| SYSTEM PARAMETERS (Note 5) Test Circuit Figure 2 |  |  |  |  |  |
| V OUT | Output Voltage | $15 \mathrm{~V} \leq \mathrm{V}_{\text {IN }} \leq 40 \mathrm{~V}, 0.1 \mathrm{~A} \leq \mathrm{I}_{\text {LOAD }} \leq 0.5 \mathrm{~A}$ | 12.0 | $\begin{aligned} & 11.52 / \mathbf{1 1 . 4 0} \\ & 12.48 / \mathbf{1 2 . 6 0} \end{aligned}$ | $V(\min )$ <br> V (max) |
| $\eta$ | Efficiency | $\mathrm{V}_{\mathrm{IN}}=12 \mathrm{~V}, \mathrm{I}_{\text {LOAD }}=0.5 \mathrm{~A}$ | 88 |  | \% |


| Electrical Characteristics Specifications with standard type face are for $\mathrm{T}_{\mathrm{J}}=25^{\circ} \mathrm{C}$, and those with boldface type apply over full Operating Temperature Range |  |  |  |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: |
|  |  |  |  | 94-ADJ |  |
| Symbol | Parameter | Conditions | Type (Note 3) | Limit (Note 4) | (Limits) |
| SYSTEM PARAMETERS (Note 5) Test Circuit Figure 2 |  |  |  |  |  |
| $\mathrm{V}_{\text {FB }}$ | Feedback Voltage | $4.5 \mathrm{~V} \leq \mathrm{V}_{\mathrm{IN}} \leq 40 \mathrm{~V}, 0.1 \mathrm{~A} \leq \mathrm{I}_{\mathrm{LOAD}} \leq 0.5 \mathrm{~A}$ <br> $\mathrm{V}_{\text {OUT }}$ programmed for 3 V . Circuit of Figure 2 | 1.230 | $\begin{aligned} & 1.193 / \mathbf{1 . 1 8 0} \\ & 1.267 / \mathbf{1 . 2 8 0} \end{aligned}$ | $\begin{aligned} & V \\ & \mathrm{~V}(\min ) \\ & \mathrm{V}(\max ) \end{aligned}$ |
| $\eta$ | Efficiency | $\mathrm{V}_{\mathrm{IN}}=12 \mathrm{~V}, \mathrm{I}$ LOAD $=0.5 \mathrm{~A}$ | 80 |  | \% |

## All Output Voltage Versions

Electrical Characteristics Specifications with standard type face are for $\mathrm{T}_{J}=25^{\circ} \mathrm{C}$, and those with boldface type apply over full Operating Temperature Range. Unless otherwise specified, $\mathrm{V}_{\mathrm{IN}}=12 \mathrm{~V}$ for the $3.3 \mathrm{~V}, 5 \mathrm{~V}$, and Adjustable version and $\mathrm{V}_{\mathrm{IN}}=24 \mathrm{~V}$ for the 12 V version. ILOAD $=100 \mathrm{~mA}$

| Symbol | Parameter | Conditions | LM2594-XX |  | Units |
| :---: | :---: | :---: | :---: | :---: | :---: |
|  |  |  | Limit <br> (Note 4) | (Limits) |  |

## DEVICE PARAMETERS

| $\mathrm{I}_{\mathrm{b}}$ | Feedback Bias Current | Adjustable Version Only, VFB $=1.3 \mathrm{~V}$ | 10 | 50/100 | nA |
| :---: | :---: | :---: | :---: | :---: | :---: |
| $\mathrm{f}_{\mathrm{O}}$ | Oscillator Frequency | (Note 6) | 150 | $\begin{aligned} & 127 / \mathbf{1 1 0} \\ & 173 / 173 \end{aligned}$ | $\begin{gathered} \mathrm{kHz} \\ \mathrm{kHz}(\min ) \\ \mathrm{kHz}(\max ) \\ \hline \end{gathered}$ |
| $\mathrm{V}_{\text {SAT }}$ | Saturation Voltage | IOUT $=0.5 \mathrm{~A}($ Notes 7 and 8$)$ | 0.9 | 1.1/1.2 | $\begin{gathered} \mathrm{V} \\ \mathrm{~V}(\max ) \end{gathered}$ |
| DC | Max Duty Cycle (ON) <br> Min Duty Cycle (OFF) | (Note 8) <br> (Note 9) | $\begin{gathered} 100 \\ 0 \end{gathered}$ |  | \% |
| $\mathrm{I}_{\mathrm{CL}}$ | Current Limit | Peak Current, (Notes 7 and 8) | 0.8 | $\begin{gathered} 0.65 / 0.58 \\ 1.3 / 1.4 \end{gathered}$ |  |
| $\mathrm{I}_{\mathrm{L}}$ | Output Leakage Current | $\begin{array}{ll} (\text { Notes 7, 9, and 10) } & \text { Output }=0 \mathrm{~V} \\ & \text { Output }=-1 \mathrm{~V} \end{array}$ | 2 | $\begin{aligned} & 50 \\ & 15 \end{aligned}$ | $\begin{gathered} \mu \mathrm{A}(\max ) \\ \mathrm{mA} \\ \mathrm{~mA}(\max ) \end{gathered}$ |
| $\mathrm{I}_{\mathrm{Q}}$ | Quiescent Current | (Note 9) | 5 | 10 | $\begin{gathered} \mathrm{mA} \\ \mathrm{~mA}(\max ) \end{gathered}$ |
| ISTBY | Standby Quiescent Current | ON/OFF pin $=5 \mathrm{~V}$ (OFF) $\quad$ (Note 10) | 85 | 200/250 | $\mu \mathrm{A}$ $\mu \mathrm{A}$ (max) |
| $\theta_{\mathrm{JA}}$ | Thermal Resistance | N Package, Junction to Ambient (Note 11) M Package, Junction to Ambient (Note 11) | $\begin{gathered} 95 \\ 150 \end{gathered}$ |  | ${ }^{\circ} \mathrm{C} / \mathrm{W}$ |

ON/OFF CONTROL Test Circuit Figure 2

| $\begin{aligned} & \mathrm{V}_{\mathrm{IH}} \\ & \mathrm{~V}_{\mathrm{IL}} \end{aligned}$ | $\overline{\mathrm{ON}}$ /OFF Pin Logic Input Threshold Voltage | Low (Regulator ON) <br> High (Regulator OFF) | 1.3 | $\begin{aligned} & 0.6 \\ & 2.0 \end{aligned}$ |  |
| :---: | :---: | :---: | :---: | :---: | :---: |
| ${ }^{\mathrm{H}}$ | $\overline{O N} / O F F$ Pin Input Current | $\mathrm{V}_{\text {LOGIC }}=2.5 \mathrm{~V}$ (Regulator OFF) | 5 | 15 | $\begin{gathered} \mu \mathrm{A} \\ \mu \mathrm{~A}(\max ) \end{gathered}$ |
| $\mathrm{I}_{\mathrm{L}}$ |  | $\mathrm{V}_{\text {LOGIC }}=0.5 \mathrm{~V}$ (Regulator ON) | 0.02 | 5 | $\begin{gathered} \mu \mathrm{A} \\ \mu \mathrm{~A}(\mathrm{max}) \end{gathered}$ |

## Electrical Characteristics (Continued)

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but do not guarantee specific performance limits. For guaranteed specifications and test conditions, see the Electrical Characteristics.
Note 2: The human body model is a 100 pF capacitor discharged through a 1.5 k resistor into each pin.
Note 3: Typical numbers are at $25^{\circ} \mathrm{C}$ and represent the most likely norm.
Note 4: All limits guaranteed at room temperature (standard type face) and at temperature extremes (bold type face). All room temperature limits are $100 \%$ production tested. All limits at temperature extremes are guaranteed via correlation using standard Statistical Quality Control (SQC) methods. All limits are used to calculate Average Outgoing Quality Level (AOQL).
Note 5: External components such as the catch diode, inductor, input and output capacitors, and voltage programming resistors can affect switching regulator system performance. When the LM2594 is used as shown in the Figure 2 test circuit, system performance will be as shown in system parameters section of Electrical Characteristics.
Note 6: The switching frequency is reduced when the second stage current limit is activated. The amount of reduction is determined by the severity of current overload.
Note 7: No diode, inductor or capacitor connected to output pin.
Note 8: Feedback pin removed from output and connected to OV to force the output transistor switch ON.
Note 9: Feedback pin removed from output and connected to 12 V for the $3.3 \mathrm{~V}, 5 \mathrm{~V}$, and the ADJ. version, and 15 V for the 12 V version, to force the output transistor switch OFF.
Note 10: $\mathrm{V}_{\mathrm{IN}}=40 \mathrm{~V}$.
Note 11: Junction to ambient thermal resistance with approximately 1 square inch of printed circuit board copper surrounding the leads. Additional copper area will lower thermal resistance further. See application hints in this data sheet and the thermal model in Switchers Made Simple software.
Typical Performance Characteristics (Circuit of Figure 2)


## Typical Performance Characteristics (Circuit of Figure 2) (Continued)



TL/H/12439-10


Standby
Quiescent Current


TL/H/12439-11
$\overline{\mathrm{ON}} /$ OFF Pin
Current (Sinking)

TL/H/12439-14


TL/H/12439-16

Typical Performance Characteristics (Circuit of Figure 2)

Continuous Mode Switching Waveforms
$\mathrm{V}_{\text {IN }}=20 \mathrm{~V}, \mathrm{~V}_{\text {OUT }}=5 \mathrm{~V}$, I LOAD $=400 \mathrm{~mA}$
$L=100 \mu \mathrm{H}$, C OUT $=120 \mu \mathrm{~F}$, C OUT $E S R=140 \mathrm{~m} \Omega$


Load Transient Response for Continuous Mode
$\mathrm{V}_{\mathbf{I N}}=20 \mathrm{~V}, \mathrm{~V}_{\text {OUT }}=5 \mathrm{~V}$, $\mathrm{I}_{\text {LOAD }}=200 \mathrm{~mA}$ to 500 mA
$\mathrm{L}=100 \mu \mathrm{H}$, C OUT $=120 \mu \mathrm{~F}$, C OUT ESR $=140 \mathrm{~m} \Omega$


A: Output Voltage, $50 \mathrm{mV} /$ div. (AC)
B: 200 mA to 500 mA Load Pulse
Horizontal Time Base: $50 \mu \mathrm{~s} / \mathrm{div}$.

Discontinuous Mode Switching Waveforms
$\mathrm{V}_{\text {IN }}=\mathbf{2 0 V}, \mathrm{V}_{\text {OUT }}=\mathbf{5 V}$, I LOAD $=200 \mathrm{~mA}$
L $=\mathbf{3 3} \mu \mathrm{H}$, C $_{\text {OUT }}=220 \mu \mathrm{~F}$, C OUT ESR $=60 \mathrm{~m} \Omega$


Load Transient Response for Discontinuous Mode $\mathrm{V}_{\mathrm{IN}}=20 \mathrm{~V}, \mathrm{~V}_{\text {OUT }}=5 \mathrm{~V}, \mathrm{I}_{\text {LOAD }}=100 \mathrm{~mA}$ to 200 mA L = $\mathbf{3 3} \mu \mathrm{H}$, C OUT $=\mathbf{2 2 0} \mu \mathrm{F}$, C $_{\text {OUT }}$ ESR $=60 \mathrm{~m} \Omega$


A: Output Voltage, $50 \mathrm{mV} /$ div. ( AC )
B: 100 mA to 200 mA Load Pulse
Horizontal Time Base: $200 \mu \mathrm{~s} / \mathrm{div}$.

## Block Diagram



FIGURE 1

## Test Circuit and Layout Guidelines



TL/H/12439-22

$$
\begin{gathered}
\mathrm{C}_{\mathrm{IN}}-68 \mu \mathrm{~F}, 35 \mathrm{~V} \text {, Aluminum Electrolytic } \\
\text { Nichicon "PL Series" } \\
\mathrm{C}_{\mathrm{OUT}}-120 \mu \mathrm{~F}, 25 \mathrm{~V} \text { Aluminum Electrolytic, } \\
\\
\quad \text { Nichicon "PL Series" } \\
\mathrm{D} 1 \quad-1 \mathrm{~A}, 40 \mathrm{~V} \text { Schottky Rectifier, 1N5819 } \\
\mathrm{L} 1 \quad-100 \mu \mathrm{H}, \mathrm{~L} 20
\end{gathered}
$$

Adjustable Output Voltage Versions
$\mathrm{C}_{\mathrm{FF}}$
$V_{\text {OUT }}=V_{\text {REF }}\left(1+\frac{R_{2}}{R_{1}}\right) \quad$ where $V_{\text {REF }}=1.23 V$

$$
R_{2}=R_{1}\left(\frac{V_{\text {OUT }}}{V_{\text {REF }}}-1\right) \quad \begin{aligned}
& \text { Select } R_{1} \text { to be approximately } 1 \mathrm{k} \Omega, \\
& \text { use a } 1 \% \text { resistor for best stability. }
\end{aligned}
$$

TL/H/12439-23
$\mathrm{C}_{\mathrm{IN}}-68 \mu \mathrm{~F}, 35 \mathrm{~V}$, Aluminum Electrolytic Nichicon "PL Series"

Cout - $120 \mu \mathrm{~F}, 25 \mathrm{~V}$ Aluminum Electrolytic, Nichicon "PL Series"
D1 - 1A, 40V Schottky Rectifier, 1N5819
L1 $-100 \mu \mathrm{H}$, L20
$R_{1}-1 \mathrm{k} \Omega, 1 \%$
CFF - See Application Information Section

## FIGURE 2. Standard Test Circuits and Layout Guides

As in any switching regulator, layout is very important. Rapidly switching currents associated with wiring inductance can generate voltage transients which can cause problems. For minimal inductance and ground loops, the wires indicated by heavy lines should be wide printed circuit traces and should be kept as short as possible. For best results, external components should be located as close to the switcher IC as possible using ground plane construction or single point grounding.

If open core inductors are used, special care must be taken as to the location and positioning of this type of inductor. Allowing the inductor flux to intersect sensitive feedback, IC groundpath and $\mathrm{C}_{\text {OUT }}$ wiring can cause problems. When using the adjustable version, special care must be taken as to the location of the feedback resistors and the associated wiring. Physically locate both resistors near the $I C$, and route the wiring away from the inductor, especially an open core type of inductor. (See application section for more information.)

| LM2594 Series Buck Regulator Design Procedure (Fixed Output) |  |
| :---: | :---: |
| PR | EXAMPLE (Fixed Output Voltage Version) |
| Given: <br> $\mathrm{V}_{\text {OUT }}=$ Regulated Output Voltage (3.3V, 5 V or 12 V ) <br> $\mathrm{V}_{\text {IN }}(\max )=$ Maximum DC Input Voltage <br> $l_{\text {LOAD }}(\max )=$ Maximum Load Current <br> 1. Inductor Selection (L1) <br> A. Select the correct inductor value selection guide from Figures 5, 6, or 7 . (Output voltages of $3.3 \mathrm{~V}, 5 \mathrm{~V}$, or 12 V respectively.) For all other voltages, see the design procedure for the adjustable version. <br> B. From the inductor value selection guide, identify the inductance region intersected by the Maximum Input Voltage line and the Maximum Load Current line. Each region is identified by an inductance value and an inductor code (LXX). <br> C. Select an appropriate inductor from the four manufacturer's part numbers listed in Figure 9. | Given |
|  |  |
|  |  |
|  | LOAD(max) |
|  | Inductor Selectio |
|  | A. Use the inductor selection guide for the 5 V version shown in Figure 6. |
|  | B. From the inductor value selection guide shown in Figure 6 , the inductance region intersected by the 12 V hori- |
|  | zontal line and the 0.4 A vertical line is $100 \mu \mathrm{H}$, and the inductor code is L20. |
|  | inductance value required is $100 \mu \mathrm{H}$. From the Figure 9 , go to the L20 line and choose an induct number from any of the four manufacturers |
|  | shown. (In most instance, both through hole and surface mount inductors are available.) |
| 2. Output Capacitor Selection (COUT) <br> A. In the majority of applications, low ESR (Equivalent Series Resistance) electrolytic capacitors between $82 \mu \mathrm{~F}$ and $220 \mu \mathrm{~F}$ and low ESR solid tantalum capacitors between $15 \mu \mathrm{~F}$ and $100 \mu \mathrm{~F}$ provide the best results. This capacitor should be located close to the IC using short capacitor leads and short copper traces. Do not use capacitors larger than $220 \mu \mathrm{~F}$. | 2. Output Capacitor Selection |
|  | A. See section on output capacitors in application information section. |
|  | B. From the quick design component selection table shown in Figure 3, locate the 5V output voltage section. In the load current column, choose the load current line that is closest to the current needed in your application, for this example, use the 0.5 A line. In the maximum input |
| For additional information, see section on output capacitors in application information section. | voltage column, select the line that covers the input voltage needed in your application, in this example, use the |
| B. To simplify the capacitor selection procedure, refer to the quick design component selection table shown in Figure 3. This table contains different input voltages, output voltages, and load currents, and lists various inductors and output capacitors that will provide the best design solutions. | 15 V line. Continuing on this line are recommended inductors and capacitors that will provide the best overall performance. |
|  | The capacitor list contains both through hole electrolytic and surface mount tantalum capacitors from four different capacitor manufacturers. It is recommended that |
| C. The capacitor voltage rating for electrolytic capacitors should be at least 1.5 times greater than the output voltage, and often much higher voltage ratings are needed to satisfy the low ESR requirements for low output ripple voltage. | both the manufacturers and the manufacturer's series that are listed in the table be used. |
|  | In this example aluminum electrolytic capacitors from several different manufacturers are available with the range of ESR numbers needed. |
| D. For computer aided design software, see Switchers Made Simple ${ }^{\circledR}$ version 4.1 or later. | $120 \mu \mathrm{~F}$ 25V Panasonic HFQ Serie <br> $120 \mu \mathrm{~F}$ 25V Nichicon PL Series |
| 3. C | or a 5 V output, a capacitor voltage rating at least |
| A. The catch diode current rating must be at least 1.3 times greater than the maximum load current. Also, if the power supply design must withstand a continuous output short, the diode should have a current rating equal to the maximum current limit of the LM2594. The most stressful condition for this diode is an overload or shorted output condition. | 7.5 V or more is needed. But, in this example, even a low ESR, switching grade, $120 \mu \mathrm{~F} 10 \mathrm{~V}$ aluminum electrolytic capacitor would exhibit approximately $400 \mathrm{~m} \Omega$ of ESR (see the curve in Figure 14 for the ESR vs voltage rating). This amount of ESR would result in relatively high output ripple voltage. To reduce the ripple to $1 \%$ of the output voltage, or less, a capacitor with a higher voltage |
| B. The reverse voltage rating of the diode should be at least 1.25 times the maximum input voltage. | rating (lower ESR) should be selected. A 16 V or 25 V capacitor will reduce the ripple voltage by approximately half. |
| C. This diode must be fast (short reverse recovery time) and must be located close to the LM2594 using short | 3. Catch Diode Selection (D1) |
| leads and short printed circuit traces. Because of their fast switching speed and low forward voltage drop, Schottky diodes provide the best performance and efficiency, and should be the first choice, especially in low output voltage applications. Ultra-fast recovery, or High- | A. Refer to the table shown in Figure 12. In this example, a $1 \mathrm{~A}, 20 \mathrm{~V}, 1 \mathrm{~N} 5817$ Schottky diode will provide the best performance, and will not be overstressed even for a shorted output. |
|  |  |

LM2594 Series Buck Regulator Design Procedure (Fixed Output) (Continued)

PROCEDURE (Fixed Output Voltage Version)
Efficiency rectifiers also provide good results. Ultra-fast recovery diodes typically have reverse recovery times of 50 ns or less. Rectifiers such as the 1N4001 series are much too slow and should not be used.
4. Input Capacitor ( $\mathrm{C}_{\mathrm{IN}}$ )

A low ESR aluminum or tantalum bypass capacitor is needed between the input pin and ground to prevent large voltage transients from appearing at the input. In addition, the RMS current rating of the input capacitor should be selected to be at least $1 / 2$ the DC load current. The capacitor manufacturers data sheet must be checked to assure that this current rating is not exceeded. The curve shown in Figure 13 shows typical RMS current ratings for several different aluminum electrolytic capacitor values.
This capacitor should be located close to the IC using short leads and the voltage rating should be approximately 1.5 times the maximum input voltage.
If solid tantalum input capacitors are used, it is recomended that they be surge current tested by the manufacturer.
Use caution when using ceramic capacitors for input bypassing, because it may cause severe ringing at the $\mathrm{V}_{\mathrm{IN}}$ pin.
For additional information, see section on input capacitors in Application Information section.

## EXAMPLE (Fixed Output Voltage Version)

4. Input Capacitor ( $\mathrm{C}_{\mathrm{IN}}$ )

The important parameters for the Input capacitor are the input voltage rating and the RMS current rating. With a nominal input voltage of 12 V , an aluminum electrolytic capacitor with a voltage rating greater than 18V (1.5 $\times$
$\mathrm{V}_{\mathrm{IN}}$ ) would be needed. The next higher capacitor voltage rating is 25 V .
The RMS current rating requirement for the input capacitor in a buck regulator is approximately $1 / 2$ the DC load current. In this example, with a 400 mA load, a capacitor with a RMS current rating of at least 200 mA is needed. The curves shown in Figure 13 can be used to select an appropriate input capacitor. From the curves, locate the 25 V line and note which capacitor values have RMS current ratings greater than 200 mA . Either a $47 \mu \mathrm{~F}$ or $68 \mu \mathrm{~F}, 25 \mathrm{~V}$ capacitor could be used.
For a through hole design, a $68 \mu \mathrm{~F} / 25 \mathrm{~V}$ electrolytic capacitor (Panasonic HFQ series or Nichicon PL series or equivalent) would be adequate. other types or other manufacturers capacitors can be used provided the RMS ripple current ratings are adequate.
For surface mount designs, solid tantalum capacitors are recommended. The TPS series available from AVX, and the 593D series from Sprague are both surge current tested.

| Conditions |  |  | Inductor |  | Output Capacitor |  |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  |  | Through Hole | Surface Mount |  |
| Output Voltage (V) | Load Current (A) | Max Input Voltage (V) |  |  | Inductance ( $\mu \mathrm{H}$ ) | Inductor (\#) | Panasonic HFQ Series ( $\mu \mathrm{F} / \mathrm{V}$ ) | Nichicon PL Series ( $\mu \mathrm{F} / \mathrm{V}$ ) | AVX TPS Series ( $\mu \mathrm{F} / \mathrm{V}$ ) | Sprague 595D Series ( $\mu \mathrm{F} / \mathrm{V}$ ) |
| 3.3 | 0.5 | 5 | 33 | L14 | 220/16 | 220/16 | 100/16 | 100/6.3 |
|  |  | 7 | 47 | L13 | 120/25 | 120/25 | 100/16 | 100/6.3 |
|  |  | 10 | 68 | L21 | 120/25 | 120/25 | 100/16 | 100/6.3 |
|  |  | 40 | 100 | L20 | 120/35 | 120/35 | 100/16 | 100/6.3 |
|  | 0.2 | 6 | 68 | L4 | 120/25 | 120/25 | 100/16 | 100/6.3 |
|  |  | 10 | 150 | L10 | 120/16 | 120/16 | 100/16 | 100/6.3 |
|  |  | 40 | 220 | L9 | 120/16 | 120/16 | 100/16 | 100/6.3 |
| 5 | 0.5 | 8 | 47 | L13 | 180/16 | 180/16 | 100/16 | 33/25 |
|  |  | 10 | 68 | L21 | 180/16 | 180/16 | 100/16 | 33/25 |
|  |  | 15 | 100 | L20 | 120/25 | 120/25 | 100/16 | 33/25 |
|  |  | 40 | 150 | L19 | 120/25 | 120/25 | 100/16 | 33/25 |
|  | 0.2 | 9 | 150 | L10 | 82/16 | 82/16 | 100/16 | 33/25 |
|  |  | 20 | 220 | L9 | 120/16 | 120/16 | 100/16 | 33/25 |
|  |  | 40 | 330 | L8 | 120/16 | 120/16 | 100/16 | 33/25 |
| 12 | 0.5 | 15 | 68 | L21 | 82/25 | 82/25 | 100/16 | 15/25 |
|  |  | 18 | 150 | L19 | 82/25 | 82/25 | 100/16 | 15/25 |
|  |  | 30 | 220 | L27 | 82/25 | 82/25 | 100/16 | 15/25 |
|  |  | 40 | 330 | L26 | 82/25 | 82/25 | 100/16 | 15/25 |
|  | 0.2 | 15 | 100 | L11 | 82/25 | 82/25 | 100/16 | 15/25 |
|  |  | 20 | 220 | L9 | 82/25 | 82/25 | 100/16 | 15/25 |
|  |  | 40 | 330 | L17 | 82/25 | 82/25 | 100/16 | 15/25 |

FIGURE 3. LM2594 Fixed Voltage Quick Design Component Selection Table


Procedure continued on next page.
A. See section on COUT in Application Information section.
hown in Figure 4, locate the output voltage column. From that column, locate the cation. In output capacitor section, select a capacitor from the list mur hour yypes from four derent capacior manufacturers. It is ufacturers series that are listed in the table be used.
In this example, through hole aluminum electrolytic capacitors from several different manufacturers are available.
$120 \mu \mathrm{~F} \quad 50 \mathrm{~V}$ Nichicon PL Series
Example continued on next page.

|  |  |
| :---: | :---: |
| PROCEDURE (Adjustable Output Voltage Version) | EXAMPLE (Adjustable Output Voltage Version) |
| 4. Feedforward Capacitor ( $\mathbf{C F F}_{\text {FF }}$ ) (See Figure 2) <br> For output voltages greater than approximately 10 V , an additional capacitor is required. The compensation capacitor is typically between 50 pF and 10 nF , and is wired in parallel with the output voltage setting resistor, $\mathrm{R}_{2}$. It provides additional stability for high output voltages, low input-output voltages, and/or very low ESR output capacitors, such as solid tantalum capacitors. $C_{F F}=\frac{1}{31 \times 10^{3} \times R_{2}}$ | C. For a 20 V output, a capacitor rating of at least 30 V or more is needed. In this example, either a 35 V or 50 V capacitor would work. A 50 V rating was chosen because it has a lower ESR which provides a lower output ripple voltage. <br> Other manufacturers or other types of capacitors may also be used, provided the capacitor specifications (especially the 100 kHz ESR) closely match the types listed in the table. Refer to the capacitor manufacturers data sheet for this information. <br> 4. Feedforward Capacitor ( $\mathrm{C}_{\mathrm{FF}}$ ) <br> The table shown in Figure 4 contains feed forward capacitor values for various output voltages. In this example, a 1 nF capacitor is needed. |
| 5. Catch Diode Selection (D1) <br> A. The catch diode current rating must be at least 1.3 times greater than the maximum load current. Also, if the power supply design must withstand a continuous output short, the diode should have a current rating equal to the maximum current limit of the LM2594. The most stressful condition for this diode is an overload or shorted output condition. | 5. Catch Diode Selection (D1) |
|  | A. Refer to the table shown in Figure 12. Schottky diodes provide the best performance, and in this example a 1A, $40 \mathrm{~V}, 1$ N5819 Schottky diode would be a good choice. The 1A diode rating is more than adequate and will not be overstressed even for a shorted output. <br> 6. Input Capacitor ( $\mathrm{C}_{\mathbf{I N}}$ ) <br> The important parameters for the Input capacitor are the |
| B. The reverse voltage rating of the diode should be at least 1.25 times the maximum input voltage. | ut voltage rating and the RMS current rating. With a minal input voltage of 28 V , an aluminum electrolytic |
| C. This diode must be fast (short reverse recovery time) and must be located close to the LM2594 using short leads and short printed circuit traces. Because of their fast switching speed and low forward voltage drop, Schottky diodes provide the best performance and efficiency, and should be the first choice, especially in low | aluminum electrolytic capacitor with a voltage rating greater than $42 \mathrm{~V}\left(1.5 \times \mathrm{V}_{\mathrm{IN}}\right)$ would be needed. Since the the next higher capacitor voltage rating is 50 V , a 50 V capacitor should be used. The capacitor voltage rating of ( $1.5 \times \mathrm{V}_{\mathrm{IN}}$ ) is a conservative guideline, and can be modified somewhat if desired. |
| output voltage applications. Ultra-fast recovery, or HighEfficiency rectifiers are also a good choice, but some types with an abrupt turn-off characteristic may cause instability or EMI problems. Ultra-fast recovery diodes typically have reverse recovery times of 50 ns or less. | The RMS current rating requirement for the input capacitor of a buck regulator is approximately $1 / 2$ the DC load current. In this example, with a 400 mA load, a capacitor with a RMS current rating of at least 200 mA is needed. <br> The curves shown in Figure 13 can be used to select an |
| Rectifiers such as the 1 N4001 series are much too slow and should not be used. | appropriate input capacitor. From the curves, locate the 50 V line and note which capacitor values have RMS cur- |
| 6. Input Capacitor ( $\mathrm{C}_{\mathbf{I N}}$ ) <br> A low ESR aluminum or tantalum bypass capacitor is | rent ratings greater than 200 mA . A $47 \mu \mathrm{~F} / 50 \mathrm{~V}$ low ESR electrolytic capacitor capacitor is needed. |
| needed between the input pin and ground to prevent large voltage transients from appearing at the input. In addition, the RMS current rating of the input capacitor should be selected to be at least $1 / 2$ the DC load current. The capacitor manufacturers data sheet must be | For a through hole design, a $47 \mu \mathrm{~F} / 50 \mathrm{~V}$ electrolytic capacitor (Panasonic HFQ series or Nichicon PL series or equivalent) would be adequate. Other types or other manufacturers capacitors can be used provided the RMS ripple current ratings are adequate. |
| checked to assure that this current rating is not exceeded. The curve shown in Figure 13 shows typical RMS current ratings for several different aluminum electrolytic capacitor values. | For surface mount designs, solid tantalum capacitors are recommended. The TPS series available from AVX, and the 593D series from Sprague are both surge current tested. |
| This capacitor should be located close to the IC using short leads and the voltage rating should be approximately 1.5 times the maximum input voltage. | To further simplify the buck regulator design procedure, Na tional Semiconductor is making available computer design software to be used with the Simple Switcher line ot switch- |
| If solid tantalum input capacitors are used, it is recomended that they be surge current tested by the manufacturer. | ing regulators. Switchers Made Simple (version 4.1 or later) is available on a $31 / 2^{\prime \prime}$ diskette for IBM compatible computers. |
| Use caution when using ceramic capacitors for input bypassing, because it may cause severe ringing at the $\mathrm{V}_{\mathrm{IN}}$ pin. |  |
| For additional information, see section on input capacitors in application information section. |  |


| LM2594 Series Buck Regulator Design Procedure (Adjustable Output) (Continued) |  |  |  |  |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  | Through Hole Output Capacitor |  |  | Surface Mount Output Capacitor |  |  |
| Voltage <br> (V) | Panasonic HFQ Series ( $\mu \mathrm{F} / \mathrm{V}$ ) | $\begin{gathered} \text { Nichicon PL } \\ \text { Series } \\ (\mu \mathrm{F} / \mathrm{V}) \\ \hline \end{gathered}$ | Feedforward Capacitor | AVX TPS <br> Series <br> ( $\mu \mathrm{F} / \mathrm{V}$ ) | Sprague 595D Series ( $\mu \mathrm{F} / \mathrm{V}$ ) | Feedforward Capacitor |
| 1.2 | 220/25 | 220/25 | 0 | 220/10 | 220/10 | 0 |
| 4 | 180/25 | 180/25 | 4.7 nF | 100/10 | 120/10 | 4.7 nF |
| 6 | 82/25 | 82/25 | 4.7 nF | 100/10 | 120/10 | 4.7 nF |
| 9 | 82/25 | 82/25 | 3.3 nF | 100/16 | 100/16 | 3.3 nF |
| 12 | 82/25 | 82/25 | 2.2 nF | 100/16 | 100/16 | 2.2 nF |
| 15 | 82/25 | 82/25 | 1.5 nF | 68/20 | 100/20 | 1.5 nF |
| 24 | 82/50 | 120/50 | 1 nF | 10/35 | 15/35 | 220 pF |
| 28 | 82/50 | 120/50 | 820 pF | 10/35 | 15/35 | 220 pF |

FIGURE 4. Output Capacitor and Feedforward Capacitor Selection Table

## LM2594 Series Buck Regulator Design Procedure

INDUCTOR VALUE SELECTION GUIDES (For Continuous Mode Operation)



LM2594 Series Buck Regulator Design Procedure (Continued)

| VR | 1A Diodes |  |  |  |
| :---: | :---: | :---: | :---: | :---: |
|  | Surface Mount |  | Through Hole |  |
|  | Schottky | Ultra Fast Recovery | Schottky | Ultra Fast Recovery |
| 20 V |  | All of these diodes are rated to at least 50V. | 1N5817 | All of these diodes are rated to at least 50V. |
|  |  |  | SR102 |  |
| 30V | MBRS130 |  | 1N5818 |  |
|  |  |  | SR103 |  |
|  |  |  | 11DQ03 |  |
| 40V | MBRS140 | MURS120 <br> 10BF10 | 1N5819 | MUR120 <br> HER101 <br> 11DF1 |
|  | 10BQ040 |  | SR104 |  |
|  | 10MQ040 |  | 11DQ04 |  |
| $\begin{aligned} & 50 \mathrm{~V} \\ & \text { or } \\ & \text { more } \end{aligned}$ | MBRS160 |  | SR105 |  |
|  | 10BQ050 |  | MBR150 |  |
|  | 10MQ060 |  | 11DQ05 |  |

FIGURE 12. Diode Selection Table

## Application Information

## PIN FUNCTIONS

$+\mathrm{V}_{\mathrm{IN}}$-This is the positive input supply for the IC switching regulator. A suitable input bypass capacitor must be present at this pin to minimize voltage transients and to supply the switching currents needed by the regulator.
Ground-Circuit ground.
Output-Internal switch. The voltage at this pin switches between ( $+\mathrm{V}_{\text {IN }}-\mathrm{V}_{\mathrm{SAT}}$ ) and approximately -0.5 V , with a duty cycle of $\mathrm{V}_{\mathrm{OUT}} / \mathrm{V}_{\text {IN }}$. To minimize coupling to sensitive circuitry, the PC board copper area connected to this pin should be kept to a minimum.
Feedback-Senses the regulated output voltage to complete the feedback loop.
$\overline{\text { ON}}$ /OFF—Allows the switching regulator circuit to be shut down using logic level signals thus dropping the total input supply current to approximately $80 \mu \mathrm{~A}$. Pulling this pin below a threshold voltage of approximately 1.3 V turns the regulator on, and pulling this pin above 1.3 V (up to a maximum of 25 V ) shuts the regulator down. If this shutdown feature is not needed, the ON/OFF pin can be wired to the ground pin or it can be left open, in either case the regulator will be in the ON condition.

## EXTERNAL COMPONENTS

$\mathbf{C}_{\mathrm{IN}}$-A low ESR aluminum or tantalum bypass capacitor is needed between the input pin and ground pin. It must be located near the regulator using short leads. This capacitor prevents large voltage transients from appearing at the input, and provides the instantaneous current needed each time the switch turns on.
The important parameters for the Input capacitor are the voltage rating and the RMS current rating. Because of the relatively high RMS currents flowing in a buck regulator's
nput capacitor, this capacitor should be chosen for its RMS current rating rather than its capacitance or voltage ratings, although the capacitance value and voltage rating are directly related to the RMS current rating.
The RMS current rating of a capacitor could be viewed as a capacitor's power rating. The RMS current flowing through the capacitors internal ESR produces power which causes the internal temperature of the capacitor to rise. The RMS current rating of a capacitor is determined by the amount of current required to raise the internal temperature approximately $10^{\circ} \mathrm{C}$ above an ambient temperature of $105^{\circ} \mathrm{C}$. The ability of the capacitor to dissipate this heat to the surrounding air will determine the amount of current the capacitor can safely sustain. Capacitors that are physically large and have a large surface area will typically have higher RMS current ratings. For a given capacitor value, a higher voltage electrolytic capacitor will be physically larger than a lower voltage capacitor, and thus be able to dissipate more heat to the surrounding air, and therefore will have a higher RMS current rating.
The consequences of operating an electrolytic capacitor above the RMS current rating is a shortened operating life. The higher temperature speeds up the evaporation of the capacitor's electrolyte, resulting in eventual failure.
Selecting an input capacitor requires consulting the manufacturers data sheet for maximum allowable RMS ripple current. For a maximum ambient temperature of $40^{\circ} \mathrm{C}$, a general guideline would be to select a capacitor with a ripple current rating of approximately $50 \%$ of the DC load current. For ambient temperatures up to $70^{\circ} \mathrm{C}$, a current rating of $75 \%$ of the DC load current would be a good choice for a conservative design. The capacitor voltage rating must be at least 1.25 times greater than the maximum input voltage, and often a much higher voltage capacitor is needed to satisfy the RMS current requirements.
A graph shown in Figure 13 shows the relationship between an electrolytic capacitor value, its voltage rating, and the RMS current it is rated for. These curves were obtained from the Nichicon "PL" series of Iow ESR, high reliability electrolytic capacitors designed for switching regulator applications. Other capacitor manufacturers offer similar types of capacitors, but always check the capacitor data sheet.
"Standard" electrolytic capacitors typically have much higher ESR numbers, lower RMS current ratings and typically have a shorter operating lifetime.
Because of their small size and excellent performance, surface mount solid tantalum capacitors are often used for input bypassing, but several precautions must be observed. A small percentage of solid tantalum capacitors can short if the inrush current rating is exceeded. This can happen at turn on when the input voltage is suddenly applied, and of course, higher input voltages produce higher inrush currents. Several capacitor manufacturers do a $100 \%$ surge current testing on their products to minimize this potential problem. If high turn on currents are expected, it may be necessary to limit this current by adding either some resistance or inductance before the tantalum capacitor, or select a higher voltage capacitor. As with aluminum electrolytic capacitors, the RMS ripple current rating must be sized to the load current.

## Application Information (Continued)



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FIGURE 13. RMS Current Ratings for Low ESR Electrolytic Capacitors (Typical)

## OUTPUT CAPACITOR

Cout-An output capacitor is required to filter the output and provide regulator loop stability. Low impedance or low ESR Electrolytic or solid tantalum capacitors designed for switching regulator applications must be used. When selecting an output capacitor, the important capacitor parameters are; the 100 kHz Equivalent Series Resistance (ESR), the RMS ripple current rating, voltage rating, and capacitance value. For the output capacitor, the ESR value is the most important parameter.
The output capacitor requires an ESR value that has an upper and lower limit. For low output ripple voltage, a low ESR value is needed. This value is determined by the maximum allowable output ripple voltage, typically $1 \%$ to $2 \%$ of the output voltage. But if the selected capacitor's ESR is extremely low, there is a possibility of an unstable feedback loop, resulting in an oscillation at the output. Using the capacitors listed in the tables, or similar types, will provide design solutions under all conditions.
If very low output ripple voltage (less than 15 mV ) is required, refer to the section on Output Voltage Ripple and Transients for a post ripple filter.
An aluminum electrolytic capacitor's ESR value is related to the capacitance value and its voltage rating. In most cases, Higher voltage electrolytic capacitors have lower ESR values (see Figure 14). Often, capacitors with much higher voltage ratings may be needed to provide the low ESR values required for low output ripple voltage.
The output capacitor for many different switcher designs often can be satisfied with only three or four different capacitor values and several different voltage ratings. See the quick design component selection tables in Figures 3 and 4 for typical capacitor values, voltage ratings, and manufacturers capacitor types.
Electrolytic capacitors are not recommended for temperatures below $-25^{\circ} \mathrm{C}$. The ESR rises dramatically at cold temperatures and typically rises 3 X @ $-25^{\circ} \mathrm{C}$ and as much as 10 X at $-40^{\circ} \mathrm{C}$. See curve shown in Figure 15.
Solid tantalum capacitors have a much better ESR spec for cold temperatures and are recommended for temperatures below $-25^{\circ} \mathrm{C}$.


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FIGURE 14. Capacitor ESR vs Capacitor Voltage Rating (Typical Low ESR Electrolytic Capacitor)

## CATCH DIODE

Buck regulators require a diode to provide a return path for the inductor current when the switch turns off. This must be a fast diode and must be located close to the LM2594 using short leads and short printed circuit traces.
Because of their very fast switching speed and low forward voltage drop, Schottky diodes provide the best performance, especially in low output voltage applications ( 5 V and lower). Ultra-fast recovery, or High-Efficiency rectifiers are also a good choice, but some types with an abrupt turnoff characteristic may cause instability or EMI problems. Ultrafast recovery diodes typically have reverse recovery times of 50 ns or less. Rectifiers such as the 1N4001 series are much too slow and should not be used.


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FIGURE 15. Capacitor ESR Change vs Temperature

## INDUCTOR SELECTION

All switching regulators have two basic modes of operation; continuous and discontinuous. The difference between the two types relates to the inductor current, whether it is flowing continuously, or if it drops to zero for a period of time in the normal switching cycle. Each mode has distinctively different operating characteristics, which can affect the regulators performance and requirements. Most switcher designs will operate in the discontinuous mode when the load current is low.
The LM2594 (or any of the Simple Switcher family) can be used for both continuous or discontinuous modes of operation.

## Application Information (Continued)

In many cases the preferred mode of operation is the continuous mode. It offers greater output power, lower peak switch, inductor and diode currents, and can have lower output ripple voltage. But it does require larger inductor values to keep the inductor current flowing continuously, especially at low output load currents and/or high input voltages.
To simplify the inductor selection process, an inductor selection guide (nomograph) was designed (see Figures 5 through 8). This guide assumes that the regulator is operating in the continuous mode, and selects an inductor that will allow a peak-to-peak inductor ripple current to be a certain percentage of the maximum design load current. This peak-to-peak inductor ripple current percentage is not fixed, but is allowed to change as different design load currents are selected. (See Figure 16.)


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FIGURE 16. ( $\Delta_{\text {IND }}$ ) Peak-to-Peak Inductor Ripple Current (as a Percentage of the Load Current) vs Load Current

By allowing the percentage of inductor ripple current to increase for low load currents, the inductor value and size can be kept relatively low.
When operating in the continuous mode, the inductor current waveform ranges from a triangular to a sawtooth type of waveform (depending on the input voltage), with the average value of this current waveform equal to the DC output load current.
Inductors are available in different styles such as pot core, toroid, E-core, bobbin core, etc., as well as different core materials, such as ferrites and powdered iron. The least expensive, the bobbin, rod or stick core, consists of wire wrapped on a ferrite bobbin. This type of construction makes for a inexpensive inductor, but since the magnetic flux is not completely contained within the core, it generates more Electro-Magnetic Interference (EMI). This magnetic flux can induce voltages into nearby printed circuit traces, thus causing problems with both the switching regulator operation and nearby sensitive circuitry, and can give incorrect scope readings because of induced voltages in the scope probe. Also see section on Open Core Inductors.
The inductors listed in the selection chart include ferrite E-core construction for Schott, ferrite bobbin core for Renco and Coilcraft, and powdered iron toroid for Pulse Engineering.

Exceeding an inductor's maximum current rating may cause the inductor to overheat because of the copper wire losses, or the core may saturate. If the inductor begins to saturate, the inductance decreases rapidly and the inductor begins to look mainly resistive (the DC resistance of the winding). This can cause the switch current to rise very rapidly and force the switch into a cycle-by-cycle current limit, thus reducing the DC output load current. This can also result in overheating of the inductor and/or the LM2594. Different inductor types have different saturation characteristics, and this should be kept in mind when selecting an inductor.
The inductor manufacturers data sheets include current and energy limits to avoid inductor saturation.

## DISCONTINUOUS MODE OPERATION

The selection guide chooses inductor values suitable for continuous mode operation, but for low current applications and/or high input voltages, a discontinuous mode design may be a better choice. It would use an inductor that would be physically smaller, and would need only one half to one third the inductance value needed for a continuous mode design. The peak switch and inductor currents will be higher in a discontinuous design, but at these low load currents ( 200 mA and below), the maximum switch current will still be less than the switch current limit.
Discontinuous operation can have voltage waveforms that are considerable different than a continuous design. The output pin (switch) waveform can have some damped sinusoidal ringing present. (See photo titled; Discontinuous Mode Switching Waveforms) This ringing is normal for discontinuous operation, and is not caused by feedback loop instabilities. In discontinuous operation, there is a period of time where neither the switch or the diode are conducting, and the inductor current has dropped to zero. During this time, a small amount of energy can circulate between the inductor and the switch/diode parasitic capacitance causing this characteristic ringing. Normally this ringing is not a problem, unless the amplitude becomes great enough to exceed the input voltage, and even then, there is very little energy present to cause damage.
Different inductor types and/or core materials produce different amounts of this characteristic ringing. Ferrite core inductors have very little core loss and therefore produce the most ringing. The higher core loss of powdered iron inductors produce less ringing. If desired, a series RC could be placed in parallel with the inductor to dampen the ringing. The computer aided design software Switchers Made Simple (version 4.1) will provide all component values for continuous and discontinuous modes of operation.


FIGURE 17. Post Ripple Filter Waveform

## Application Information (Continued)

## output voltage ripple and transients

The output voltage of a switching power supply operating in the continuous mode will contain a sawtooth ripple voltage at the switcher frequency, and may also contain short voltage spikes at the peaks of the sawtooth waveform.
The output ripple voltage is a function of the inductor sawtooth ripple current and the ESR of the output capacitor. A typical output ripple voltage can range from approximately $0.5 \%$ to $3 \%$ of the output voltage. To obtain low ripple voltage, the ESR of the output capacitor must be low, however, caution must be exercised when using extremely low ESR capacitors because they can affect the loop stability, resulting in oscillation problems. If very low output ripple voltage is needed (less than 15 mV ), a post ripple filter is recommended. (See Figure 2.) The inductance required is typically between $1 \mu \mathrm{H}$ and $5 \mu \mathrm{H}$, with low DC resistance, to maintain good load regulation. A low ESR output filter capacitor is also required to assure good dynamic load response and ripple reduction. The ESR of this capacitor may be as low as desired, because it is out of the regulator feedback loop. The photo shown in Figure 17 shows a typical output ripple voltage, with and without a post ripple filter.
When observing output ripple with a scope, it is essential that a short, low inductance scope probe ground connection be used. Most scope probe manufacturers provide a special probe terminator which is soldered onto the regulator board, preferable at the output capacitor. This provides a very short scope ground thus eliminating the problems associated with the 3 inch ground lead normally provided with the probe, and provides a much cleaner and more accurate picture of the ripple voltage waveform.

The voltage spikes are caused by the fast switching action of the output switch and the diode, and the parasitic inductance of the output filter capacitor, and its associated wiring. To minimize these voltage spikes, the output capacitor should be designed for switching regulator applications, and the lead lengths must be kept very short. Wiring inductance, stray capacitance, as well as the scope probe used to evaluate these transients, all contribute to the amplitude of these spikes.
When a switching regulator is operating in the continuous mode, the inductor current waveform ranges from a triangular to a sawtooth type of waveform (depending on the input voltage). For a given input and output voltage, the peak-topeak amplitude of this inductor current waveform remains constant. As the load current increases or decreases, the entire sawtooth current waveform also rises and falls. The average value (or the center) of this current waveform is equal to the DC load current.
If the load current drops to a low enough level, the bottom of the sawtooth current waveform will reach zero, and the switcher will smoothly change from a continuous to a discontinuous mode of operation. Most switcher designs (irregardless how large the inductor value is) will be forced to run discontinuous if the output is lightly loaded. This is a perfectly acceptable mode of operation.


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## IGURE 18. Peak-to-Peak Inductor

 Ripple Current vs Load CurrentIn a switching regulator design, knowing the value of the peak-to-peak inductor ripple current ( $\Delta l_{\mathrm{IND}}$ ) can be useful for determining a number of other circuit parameters. Parameters such as, peak inductor or peak switch current minimum load current before the circuit becomes discontinuous, output ripple voltage and output capacitor ESR can all be calculated from the peak-to-peak $\Delta l_{\mathrm{IND}}$. When the inductor nomographs shown in Figures 5 through 8 are used to select an inductor value, the peak-to-peak inductor ripple current can immediately be determined. The curve shown in Figure 18 shows the range of ( $\Delta l_{\mathrm{IND}}$ ) that can be expected for different load currents. The curve also shows how the peak-to-peak inductor ripple current ( $\Delta_{\text {I }}$ IND ) changes as you go from the lower border to the upper border (for a given load current) within an inductance region. The upper border represents a higher input voltage, while the lower border represents a lower input voltage (see Inductor Selection Guides).
These curves are only correct for continuous mode operation, and only if the inductor selection guides are used to select the inductor value
Consider the following example:
$\mathrm{V}_{\text {OUT }}=5 \mathrm{~V}$, maximum load current of 300 mA
$\mathrm{V}_{\mathrm{IN}}=15 \mathrm{~V}$, nominal, varying between 11 V and 20 V .
The selection guide in Figure 6 shows that the vertical line for a 0.3 A load current, and the horizontal line for the 15 V input voltage intersect approximately midway between the upper and lower borders of the $150 \mu \mathrm{H}$ inductance region. A $150 \mu \mathrm{H}$ inductor will allow a peak-to-peak inductor current ( $\Delta l_{\mathrm{IND}}$ ) to flow that will be a percentage of the maximum load current. Referring to Figure 18, follow the 0.3A line approximately midway into the inductance region, and read the peak-to-peak inductor ripple current ( $\Delta \mathrm{I}_{\mathrm{IND}}$ ) on the left hand axis (approximately $150 \mathrm{~mA} \mathrm{p}-\mathrm{p}$ ).
As the input voltage increases to 20 V , it approaches the upper border of the inductance region, and the inductor ripple current increases. Referring to the curve in Figure 18, it can be seen that for a load current of 0.3 A , the peak-topeak inductor ripple current ( $\Delta l_{\mathrm{IND}}$ ) is 150 mA with 15 V in, and can range from 175 mA at the upper border ( 20 V in) to 120 mA at the lower border (11V in).

## Application Information (Continued)

Once the $\Delta l_{I N D}$ value is known, the following formulas can be used to calculate additional information about the switching regulator circuit.

1. Peak Inductor or peak switch current

$$
=\left(\mathrm{I}_{\mathrm{LOAD}}+\frac{\Delta l_{\mathrm{IND}}}{2}\right)=\left(0.3 \mathrm{~A}+\frac{0.150}{2}\right)=0.375 \mathrm{~A}
$$

2. Minimum load current before the circuit becomes discontinuous

$$
=\frac{\Delta l_{\mathrm{IND}}}{2}=\frac{0.150}{2}=0.075 \mathrm{~A}
$$

3. Output Ripple Voltage $=\left(\Delta I_{\text {IND }}\right) \times\left(E S R\right.$ of $\left.C_{\text {OUT }}\right)$ $=0.150 \mathrm{~A} \times 0.240 \Omega=36 \mathrm{mV} \mathrm{p}-\mathrm{p}$
4. $\stackrel{\text { Or }}{\mathrm{ESR}}$ of $\mathrm{C}_{\text {OUT }}=\frac{\text { Output Ripple Voltage }\left(\Delta \mathrm{V}_{\text {OUT }}\right)}{\Delta \mathrm{I}_{\text {IND }}}$

$$
=\frac{0.036 \mathrm{~V}}{0.150 \mathrm{~A}}=0.240 \Omega
$$

## OPEN CORE INDUCTORS

Another possible source of increased output ripple voltage or unstable operation is from an open core inductor. Ferrite bobbin or stick inductors have magnetic lines of flux flowing through the air from one end of the bobbin to the other end. These magnetic lines of flux will induce a voltage into any wire or PC board copper trace that comes within the inductor's magnetic field. The strength of the magnetic field, the orientation and location of the PC copper trace to the magnetic field, and the distance between the copper trace and the inductor, determine the amount of voltage generated in the copper trace. Another way of looking at this inductive coupling is to consider the PC board copper trace as one turn of a transformer (secondary) with the inductor winding as the primary. Many millivolts can be generated in a copper trace located near an open core inductor which can cause stability problems or high output ripple voltage problems.
If unstable operation is seen, and an open core inductor is used, it's possible that the location of the inductor with respect to other PC traces may be the problem. To determine if this is the problem, temporarily raise the inductor away from the board by several inches and then check circuit operation. If the circuit now operates correctly, then the magnetic flux from the open core inductor is causing the problem. Substituting a closed core inductor such as a torroid or E-core will correct the problem, or re-arranging the PC layout may be necessary. Magnetic flux cutting the IC device ground trace, feedback trace, or the positive or negative traces of the output capacitor should be minimized.
Sometimes, locating a trace directly beneath a bobbin inductor will provide good results, provided it is exactly in the center of the inductor (because the induced voltages cancel themselves out), but if it is off center one direction or the other, then problems could arise. If flux problems are present, even the direction of the inductor winding can make a difference in some circuits.
This discussion on open core inductors is not to frighten the user, but to alert the user on what kind of problems to watch out for when using them. Open core bobbin or "stick" inductors are an inexpensive, simple way of making a compact efficient inductor, and they are used by the millions in many different applications.

## THERMAL CONSIDERATIONS

The LM2594 is available in two packages, an 8-pin through hole DIP (N) and an 8-pin surface mount SO-8 (M). Both packages are molded plastic with a copper lead frame. When the package is soldered to the PC board, the copper and the board are the heat sink for the LM2594 and the other heat producing components.
For best thermal performance, wide copper traces should be used and all ground and unused pins should be soldered to generous amounts of printed circuit board copper, such as a ground plane (one exception to this is the output (switch) pin, which should not have large areas of copper). Large areas of copper provide the best transfer of heat (lower thermal resistance) to the surrounding air, and even dou-ble-sided or multilayer boards provide a better heat path to the surrounding air. Unless power levels are small, sockets are not recommended because of the added thermal resistance it adds and the resultant higher junction temperatures.
Package thermal resistance and junction temperature rise numbers are all approximate, and there are many factors that will affect the junction temperature. Some of these factors include board size, shape, thickness, position, location, and even board temperature. Other factors are, trace width, printed circuit copper area, copper thickness, single- or dou-ble-sided, multilayer board, and the amount of solder on the board. The effectiveness of the PC board to dissipate heat also depends on the size, quantity and spacing of other components on the board. Furthermore, some of these components such as the catch diode will add heat to the PC board and the heat can vary as the input voltage changes. For the inductor, depending on the physical size, type of core material and the DC resistance, it could either act as a heat sink taking heat away from the board, or it could add heat to the board.


TL/H/12439-35

| Circuit Data for Temperature Rise Curve (DIP-8) |  |
| :--- | :--- |
| Capacitors | Through hole electrolytic |
| Inductor | Through hole, Schott, $100 \mu \mathrm{H}$ |
| Diode | Through hole, 1A 40V, Schottky |
| PC board | 4 square inches single sided 2 oz. copper <br> $\left(0.0028^{\prime \prime}\right)$ |

FIGURE 19. Junction Temperature Rise, DIP-8

## Application Information (Continued)



TL/H/12439-34

| Circuit Data for Temperature Rise Curve (Surface Mount) |  |
| :--- | :--- |
| Capacitors | Surface mount tantalum, molded "D" size |
| Inductor | Surface mount, Coilcraft DO33, 100 $\mu \mathrm{H}$ |
| Diode | Surface mount, 1A 40V, Schottky |
| PC board | 4 square inches single sided 2 oz. copper <br> $(0.0028 ")$ |

## FIGURE 20. Junction Temperature Rise, SO-8

The curves shown in Figures 19 and 20 show the LM2594 junction temperature rise above ambient temperature with a 500 mA load for various input and output voltages. This data was taken with the circuit operating as a buck switcher with all components mounted on a PC board to simulate the junction temperature under actual operating conditions. This curve is typical, and can be used for a quick check on the maximum junction temperature for various conditions, but keep in mind that there are many factors that can affect the junction temperature.


TL/H/12439-36
FIGURE 21. Delayed Startup


TL/H/12439-37
FIGURE 22. Undervoltage Lockout for Buck Regulator

## DELAYED STARTUP

The circuit in Figure 21 uses the the $\overline{\mathrm{ON}}$ /OFF pin to provide a time delay between the time the input voltage is applied and the time the output voltage comes up (only the circuitry pertaining to the delayed start up is shown). As the input voltage rises, the charging of capacitor C1 pulls the $\overline{O N} / O F F$ pin high, keeping the regulator off. Once the input voltage reaches its final value and the capacitor stops charging, and resistor $R_{2}$ pulls the $\overline{O N} / O F F$ pin low, thus allowing the circuit to start switching. Resistor $\mathrm{R}_{1}$ is included to limit the maximum voltage applied to the $\overline{O N} / O F F$ pin (maximum of 25 V ), reduces power supply noise sensitivity, and also limits the capacitor, C1, discharge current. When high input ripple voltage exists, avoid long delay time, because this ripple can be coupled into the $\overline{O N} / O F F$ pin and cause problems.

This delayed startup feature is useful in situations where the input power source is limited in the amount of current it can deliver. It allows the input voltage to rise to a higher voltage before the regulator starts operating. Buck regulators require less input current at higher input voltages.

## UNDERVOLTAGE LOCKOUT

Some applications require the regulator to remain off until the input voltage reaches a predetermined voltage. An undervoltage lockout feature applied to a buck regulator is shown in Figure 22, while Figures 23 and 24 applies the same feature to an inverting circuit. The circuit in Figure 23 features a constant threshold voltage for turn on and turn off (zener voltage plus approximately one volt). If hysteresis is needed, the circuit in Figure 24 has a turn ON voltage which is different than the turn OFF voltage. The amount of hysteresis is approximately equal to the value of the output voltage. If zener voltages greater than 25 V are used, an additional $47 \mathrm{k} \Omega$ resistor is needed from the ON/OFF pin to the ground pin to stay within the 25 V maximum limit of the $\overline{\mathrm{ON}} / \mathrm{OFF}$ pin.

## INVERTING REGULATOR

The circuit in Figure 25 converts a positive input voltage to a negative output voltage with a common ground. The circuit operates by bootstrapping the regulators ground pin to the negative output voltage, then grounding the feedback pin, the regulator senses the inverted output voltage and regulates it.


TL/H/12439-38
This circuit has an ON/OFF threshold of approximately 13 V .
FIGURE 23. Undervoltage Lockout for Inverting Regulator

## Application Information (Continued)



FIGURE 24. Undervoltage Lockout with Hysteresis for Inverting Regulator


Cout - $22 \mu \mathrm{~F} / 20 \mathrm{~V}$ Tant. Sprague 595D
TL/H/12439-40
$39 \mu \mathrm{~F} / 16 \mathrm{~V}$ Elec. Panasonic HFQ
FIGURE 25. Inverting - 5V Regulator with Delayed Startup

This example uses the LM2594-5 to generate a -5 V output, but other output voltages are possible by selecting other output voltage versions, including the adjustable version. Since this regulator topology can produce an output voltage that is either greater than or less than the input voltage, the maximum output current greatly depends on both the input and output voltage. The curve shown in Figure 26 provides a guide as to the amount of output load current possible for the different input and output voltage conditions.
The maximum voltage appearing across the regulator is the absolute sum of the input and output voltage, and this must be limited to a maximum of 40 V . For example, when converting +20 V to -12 V , the regulator would see 32 V between the input pin and ground pin. The LM2594 has a maximum input voltage spec of 40 V .
Additional diodes are required in this regulator configuration. Diode D1 is used to isolate input voltage ripple or noise from coupling through the $\mathrm{C}_{\mathrm{IN}}$ capacitor to the output, under light or no load conditions. Also, this diode isolation changes the topology to closley resemble a buck configuration thus providing good closed loop stability. A Schottky diode is recommended for low input voltages, (because of its lower voltage drop) but for higher input voltages, a fast recovery diode could be used.
Without diode D3, when the input voltage is first applied, the charging current of $\mathrm{C}_{\mathrm{IN}}$ can pull the output positive by several volts for a short period of time. Adding D3 prevents the output from going positive by more than a diode voltage.


TL/H/12439-41
FIGURE 26. Inverting Regulator Typical Load Current
Because of differences in the operation of the inverting regulator, the standard design procedure is not used to select the inductor value. In the majority of designs, a $100 \mu \mathrm{H}, 1 \mathrm{~A}$ inductor is the best choice. Capacitor selection can also be narrowed down to just a few values. Using the values shown in Figure 25 will provide good results in the majority of inverting designs.
This type of inverting regulator can require relatively large amounts of input current when starting up, even with light loads. Input currents as high as the LM2594 current limit (approx 0.8 A ) are needed for at least 2 ms or more, until the output reaches its nominal output voltage. The actual time depends on the output voltage and the size of the output capacitor. Input power sources that are current limited or

## Application Information (Continued)

sources that can not deliver these currents without getting loaded down, may not work correctly. Because of the relatively high startup currents required by the inverting topology, the delayed startup feature ( $\mathrm{C} 1, \mathrm{R}_{1}$ and $\mathrm{R}_{2}$ ) shown in Figure 25 is recommended. By delaying the regulator startup, the input capacitor is allowed to charge up to a higher voltage before the switcher begins operating. A portion of the high input current needed for startup is now supplied by the input capacitor $\left(\mathrm{C}_{\mathrm{IN}}\right)$. For severe start up conditions, the input capacitor can be made much larger than normal.

## INVERTING REGULATOR SHUTDOWN METHODS

To use the ON/OFF pin in a standard buck configuration is simple, pull it below 1.3 V (@25 ${ }^{\circ} \mathrm{C}$, referenced to ground) to turn regulator ON , pull it above 1.3 V to shut the regulator OFF. With the inverting configuration, some level shifting is required, because the ground pin of the regulator is no longer at ground, but is now setting at the negative output voltage level. Two different shutdown methods for inverting regulators are shown in Figures 27 and 28.


TL/H/12439-42
FIGURE 27. Inverting Regulator Ground Referenced Shutdown


TL/H/12439-43
FIGURE 28. Inverting Regulator Ground Referenced Shutdown using Opto Device

Application Information (Continued)
TYPICAL SURFACE MOUNT PC BOARD LAYOUT, FIXED OUTPUT (2X SIZE)


TL/H/12439-44
$\mathrm{C}_{\mathrm{IN}}-10 \mu \mathrm{~F}, 35 \mathrm{~V}$, Solid Tantalum AVX, "TPS series"

Cout - $100 \mu \mathrm{~F}, 10 \mathrm{~V}$ Solid Tantalum AVX, "TPS series"
D1 $-1 \mathrm{~A}, 40 \mathrm{~V}$ Schottky Rectifier, surface mount
L1 $\quad-100 \mu \mathrm{H}, \mathrm{L} 20$, Coilcraft DO33

TYPICAL SURFACE MOUNT PC BOARD LAYOUT, ADJUSTABLE OUTPUT (2X SIZE)

$\mathrm{C}_{\mathrm{IN}}-10 \mu \mathrm{~F}, 35 \mathrm{~V}$, Solid Tantalum AVX, "TPS series"
Cout - $100 \mu \mathrm{~F}, 10 \mathrm{~V}$ Solid Tantalum AVX, "TPS series"
D1 $-1 \mathrm{~A}, 40 \mathrm{~V}$ Schottky Rectifier, surface mount
L1 - $100 \mu \mathrm{H}, \mathrm{L} 20$, Coilcraft DO33
R1 $-1 \mathrm{k} \Omega, 1 \%$
$\mathrm{R}_{2}$ - Use formula in Design Procedure
$\mathrm{C}_{\mathrm{FF}}$ - See Figure 4.
FIGURE 29. PC Board Layout

## Physical Dimensions inches (millimeters) unless otherwise noted



8-Lead ( 0.150 " Wide) Molded Small Outline Package, Order Number LM2594M-3.3, LM2594M-5.0, LM2594M-12 or LM2594M-ADJ JEDEC

NS Package Number M08A
LM2594 SIMPLE SWITCHER Power Converter 150 kHz 0.5A Step-Down Voltage Regulator
Physical Dimensions inches (millimeters) unless otherwise noted (Continued)

8-Lead ( $0.300^{\prime \prime}$ Wide) Molded Dual-In-Line Package, Order Number LM2594N-3.3, LM2594N-5.0, LM2594N-12 or LM2594N-ADJ NS Package Number N08E

## LIFE SUPPORT POLICY

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1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and whose failure to perform, when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.



## Connection Diagrams and Ordering Information

Bent and Staggered Leads, Through Hole Package 5-Lead TO-220 (T)

Surface Mount Package


TL/H/12565-2
Order Number LM2595T-3.3, LM2595T-5.0, LM2595T-12 or LM2595T-ADJ See NS Package Number T05D

5-Lead TO-263 (S)


TL/H/12565-3
Order Number LM2595S-3.3, LM2595S-5.0, LM2595S-12 or LM2595S-ADJ See NS Package Number TS5B

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## Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.
Maximum Supply Voltage
45 V
$\overline{O N} /$ OFF Pin Input Voltage $\quad-0.3 \leq \mathrm{V} \leq+25 \mathrm{~V}$
Feedback Pin Voltage $\quad-0.3 \leq \mathrm{V} \leq+25 \mathrm{~V}$
Output Voltage to Ground (Steady State) -1V
Power Dissipation Internally limited
Storage Temperature Range $\quad-65^{\circ} \mathrm{C}$ to $+150^{\circ} \mathrm{C}$
ESD Susceptibility
Human Body Model (Note 2)

## LM2595-3.3

Electrical Characteristics Specifications with standard type face are for $T_{J}=25^{\circ} \mathrm{C}$, and those with boldface type apply over full Operating Temperature Range

| Symbol | Parameter | Conditions | LM2595-3.3 |  | Units <br> (Limits) |
| :---: | :---: | :---: | :---: | :---: | :---: |
|  |  |  | Typ (Note 3) | Limit (Note 4) |  |
| SYSTEM PARAMETERS (Note 5) Test Circuit Figure 2 |  |  |  |  |  |
| $\mathrm{V}_{\text {OUT }}$ | Output Voltage | $4.75 \mathrm{~V} \leq \mathrm{V}_{\mathrm{IN}} \leq 40 \mathrm{~V}, 0.1 \mathrm{~A} \leq \mathrm{I}_{\text {LOAD }} \leq 1 \mathrm{~A}$ | 3.3 | $\begin{aligned} & 3.168 / \mathbf{3 . 1 3 5} \\ & 3.432 / \mathbf{3 . 4 6 5} \end{aligned}$ | $V$ $V(\min )$ $V(\max )$ |
| $\eta$ | Efficiency | $\mathrm{V}_{\mathrm{IN}}=12 \mathrm{~V}, \mathrm{I}_{\text {LOAD }}=1 \mathrm{~A}$ | 78 |  | \% |

LM2595-5.0
Electrical Characteristics Specifications with standard type face are for $\mathrm{T}_{\mathrm{J}}=25^{\circ} \mathrm{C}$, and those with boldface type apply over full Operating Temperature Range

| Symbol | Parameter | Conditions | LM2595-5.0 |  | Units (Limits) |
| :---: | :---: | :---: | :---: | :---: | :---: |
|  |  |  | Typ <br> (Note 3) | Limit (Note 4) |  |
| SYSTEM PARAMETERS (Note 5) Test Circuit Figure 2 |  |  |  |  |  |
| V OUT | Output Voltage | $7 \mathrm{~V} \leq \mathrm{V}_{\text {IN }} \leq 40 \mathrm{~V}, 0.1 \mathrm{~A} \leq \mathrm{I}_{\text {LOAD }} \leq 1 \mathrm{~A}$ | 5.0 | $\begin{aligned} & 4.800 / 4.750 \\ & 5.200 / 5.250 \end{aligned}$ |  |
| $\eta$ | Efficiency | $\mathrm{V}_{\text {IN }}=12 \mathrm{~V}, \mathrm{I}_{\text {LOAD }}=1 \mathrm{~A}$ | 82 |  | \% |
| LM2595-12 <br> Electrical Characteristics Specifications with standard type face are for $\mathrm{T}_{\mathrm{J}}=25^{\circ} \mathrm{C}$, and those with boldface type apply over full Operating Temperature Range |  |  |  |  |  |
|  |  |  |  | 95-12 |  |
| Symbol | Parameter | Conditions | Typ (Note 3) | Limit (Note 4) | (Limits) |
| SYSTEM PARAMETERS (Note 5) Test Circuit Figure 2 |  |  |  |  |  |
| V OUT | Output Voltage | $15 \mathrm{~V} \leq \mathrm{V}_{\mathrm{IN}} \leq 40 \mathrm{~V}, 0.1 \mathrm{~A} \leq \mathrm{I}_{\text {LOAD }} \leq 1 \mathrm{~A}$ | 12.0 | $\begin{aligned} & 11.52 / \mathbf{1 1 . 4 0} \\ & 12.48 / \mathbf{1 2 . 6 0} \end{aligned}$ | $\begin{gathered} V \\ \mathrm{~V}(\min ) \\ \mathrm{V}(\max ) \end{gathered}$ |
| $\eta$ | Efficiency | $\mathrm{V}_{\mathrm{IN}}=25 \mathrm{~V}, \mathrm{l}_{\text {LOAD }}=1 \mathrm{~A}$ | 90 |  | \% |



## Electrical Characteristics (Continued)

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but do not guarantee specific performance limits. For guaranteed specifications and test conditions, see the Electrical Characteristics.
Note 2: The human body model is a 100 pF capacitor discharged through a 1.5 k resistor into each pin.
Note 3: Typical numbers are at $25^{\circ} \mathrm{C}$ and represent the most likely norm.
Note 4: All limits guaranteed at room temperature (standard type face) and at temperature extremes (bold type face). All room temperature limits are $100 \%$ production tested. All limits at temperature extremes are guaranteed via correlation using standard Statistical Quality Control (SQC) methods. All limits are used to calculate Average Outgoing Quality Level (AOQL).
Note 5: External components such as the catch diode, inductor, input and output capacitors, and voltage programming resistors can affect switching regulator system performance. When the LM2595 is used as shown in the Figure 2 test circuit, system performance will be as shown in system parameters section of Electrical Characteristics.
Note 6: The switching frequency is reduced when the second stage current limit is activated. The amount of reduction is determined by the severity of current overload.
Note 7: No diode, inductor or capacitor connected to output pin.
Note 8: Feedback pin removed from output and connected to OV to force the output transistor switch ON.
Note 9: Feedback pin removed from output and connected to 12 V for the $3.3 \mathrm{~V}, 5 \mathrm{~V}$, and the ADJ. version, and 15 V for the 12 V version, to force the output transistor switch OFF.
Note 10: $\mathrm{V}_{\mathrm{IN}}=40 \mathrm{~V}$.
Note 11: Junction to ambient thermal resistance (no external heat sink) for the TO-220 package mounted vertically, with the leads soldered to a printed circuit board with ( 1 oz .) copper area of approximately $1 \mathrm{in}^{2}$.
Note 12: Junction to ambient thermal resistance with the TO-263 package tab soldered to a single printed circuit board with $0.5 \mathrm{in}^{2}$ of ( 1 oz .) copper area.
Note 13: Junction to ambient thermal resistance with the TO-263 package tab soldered to a single sided printed circuit board with $2.5 \mathrm{in}^{2}$ of ( 1 oz .) copper area. Note 14: Junction to ambient thermal resistance with the TO-263 package tab soldered to a double sided printed circuit board with 3 in ${ }^{2}$ of ( 1 oz .) copper area on the LM2595S side of the board, and approximately $16 \mathrm{in}^{2}$ of copper on the other side of the p-c board. See Application Information in this data sheet and the thermal model in Switchers Made Simple ${ }^{\circledR}$ version 4.2 software.

Typical Performance Characteristics (Circuit of Figure 2)





## Typical Performance Characteristics (Circuit of Figure 2) (Continued)



Shutdown
Quiescent Current



TL/H/12565-6



TL/H/12565-10

Typical Performance Characteristics (Circuit of Figure 2)

Continuous Mode Switching Waveforms
$\mathrm{V}_{\text {IN }}=20 \mathrm{~V}, \mathrm{~V}_{\text {OUT }}=5 \mathrm{~V}$, ILOAD $=1 \mathrm{~A}$
L $=68 \mu \mathrm{H}$, C OUT $=120 \mu \mathrm{~F}$, C OUT ESR $=100 \mathrm{~m} \Omega$


Load Transient Response for Continuous Mode
$\mathrm{V}_{\text {IN }}=20 \mathrm{~V}, \mathrm{~V}_{\text {OUT }}=\mathbf{5 V}$, $\mathrm{I}_{\text {LOAD }}=250 \mathrm{~mA}$ to 750 mA
$\mathrm{L}=68 \mu \mathrm{H}, \mathrm{C}_{\text {OUT }}=120 \mu \mathrm{~F}, \mathrm{C}_{\text {OUT }} \mathrm{ESR}=100 \mathrm{~m} \Omega$


Discontinuous Mode Switching Waveforms
$\mathrm{V}_{\text {IN }}=\mathbf{2 0 V}, \mathrm{V}_{\text {OUT }}=5 \mathrm{~V}, \mathrm{I}_{\text {LOAD }}=\mathbf{6 0 0} \mathrm{mA}$ L $=22 \mu \mathrm{H}$, C OUt $=220 \mu \mathrm{~F}$, C OUt $\mathrm{ESR}=50 \mathrm{~m} \Omega$


A: Output Pin Voltage, 10V/div. B: Inductor Current 0.5A/div.
C: Output Ripple Voltage, $50 \mathrm{mV} /$ div. Horizontal Time Base: $2 \mu \mathrm{~s} / \mathrm{div}$.

Load Transient Response for Discontinuous Mode $\mathrm{V}_{\mathrm{IN}}=20 \mathrm{~V}, \mathrm{~V}_{\text {OUT }}=5 \mathrm{~V}, \mathrm{I}_{\text {LOAD }}=250 \mathrm{~mA}$ to 750 mA $\mathbf{L}=22 \mu \mathrm{H}, \mathrm{C}_{\text {OUT }}=220 \mu \mathrm{~F}, \mathrm{C}_{\text {OUT }} \mathrm{ESR}=50 \mathrm{~m} \Omega$


## Block Diagram



FIGURE 1

## Test Circuit and Layout Guidelines



TL/H/12565-22
$\mathrm{C}_{\mathrm{IN}}-120 \mu \mathrm{~F}, 50 \mathrm{~V}$, Aluminum Electrolytic Nichicon "PL Series"
Cout - $120 \mu \mathrm{~F}, 25 \mathrm{~V}$ Aluminum Electrolytic, Nichicon "PL Series"
D1 - 3A, 40V Schottky Rectifier, 1N5822
L1 $\quad-100 \mu \mathrm{H}$, L29


## FIGURE 2. Standard Test Circuits and Layout Guides

As in any switching regulator, layout is very important. Rapidly switching currents associated with wiring inductance can generate voltage transients which can cause problems. For minimal inductance and ground loops, the wires indicated by heavy lines should be wide printed circuit traces and should be kept as short as possible. For best results, external components should be located as close to the switcher IC as possible using ground plane construction or single point grounding.

If open core inductors are used, special care must be taken as to the location and positioning of this type of inductor. Allowing the inductor flux to intersect sensitive feedback, IC groundpath and $\mathrm{C}_{\text {OUT }}$ wiring can cause problems. When using the adjustable version, special care must be taken as to the location of the feedback resistors and the associated wiring. Physically locate both resistors near the IC, and route the wiring away from the inductor, especially an open core type of inductor. (See application section for more information.)

| LM2595 Series Buck Regulator Design Procedure (Fixed Output) |  |
| :---: | :---: |
| PROCEDURE (Fixed Output Voltage Version) | EXAMPLE (Fixed Output Voltage Version) |
| Given: <br> $\mathrm{V}_{\text {OUT }}=$ Regulated Output Voltage (3.3V, 5 V or 12 V ) <br> $\mathrm{V}_{\mathrm{IN}}(\max )=$ Maximum DC Input Voltage <br> LLOAD (max) $=$ Maximum Load Current <br> 1. Inductor Selection (L1) <br> A. Select the correct inductor value selection guide from Figures 5, 6, or 7 . (Output voltages of $3.3 \mathrm{~V}, 5 \mathrm{~V}$, or 12 V respectively.) For all other voltages, see the design procedure for the adjustable version. <br> B. From the inductor value selection guide, identify the inductance region intersected by the Maximum Input Voltage line and the Maximum Load Current line. Each region is identified by an inductance value and an inductor code (LXX). <br> C. Select an appropriate inductor from the four manufacturer's part numbers listed in Figure 9. <br> 2. Output Capacitor Selection (COUT) <br> A. In the majority of applications, low ESR (Equivalent Series Resistance) electrolytic capacitors between $47 \mu \mathrm{~F}$ and $330 \mu \mathrm{~F}$ and low ESR solid tantalum capacitors between $56 \mu \mathrm{~F}$ and $270 \mu \mathrm{~F}$ provide the best results. This capacitor should be located close to the IC using short capacitor leads and short copper traces. Do not use capacitors larger than $330 \mu \mathrm{~F}$. <br> For additional information, see section on output capacitors in application information section. <br> B. To simplify the capacitor selection procedure, refer to the quick design component selection table shown in Figure 3. This table contains different input voltages, output voltages, and load currents, and lists various inductors and output capacitors that will provide the best design solutions. <br> C. The capacitor voltage rating for electrolytic capacitors should be at least 1.5 times greater than the output voltage, and often much higher voltage ratings are needed to satisfy the low ESR requirements for low output ripple voltage. <br> D. For computer aided design software, see Switchers Made Simple ${ }^{\circledR}$ version 4.2 or later. <br> 3. Catch Diode Selection (D1) <br> A. The catch diode current rating must be at least 1.3 times greater than the maximum load current. Also, if the power supply design must withstand a continuous output short, the diode should have a current rating equal to the maximum current limit of the LM2595. The most stressful condition for this diode is an overload or shorted output condition. <br> B. The reverse voltage rating of the diode should be at least 1.25 times the maximum input voltage. <br> C. This diode must be fast (short reverse recovery time) and must be located close to the LM2595 using short leads and short printed circuit traces. Because of their fast switching speed and low forward voltage drop, Schottky diodes provide the best performance and efficiency, and should be the first choice, especially in low output voltage applications. Ultra-fast recovery, or HighProcedure continued on next page. | Given: $\begin{aligned} & \mathrm{V}_{\text {OUT }}=5 \mathrm{~V} \\ & \mathrm{~V}_{\text {IN }}(\max )=12 \mathrm{~V} \\ & \mathrm{I}_{\text {LOAD }}(\max )=1 \mathrm{~A} \end{aligned}$ <br> 1. Inductor Selection (L1) <br> A. Use the inductor selection guide for the 5 V version shown in Figure 6. <br> B. From the inductor value selection guide shown in Figure 6 , the inductance region intersected by the 12 V horizontal line and the 1 A vertical line is $68 \mu \mathrm{H}$, and the inductor code is L30. <br> C. The inductance value required is $68 \mu \mathrm{H}$. From the table in Figure 9, go to the L30 line and choose an inductor part number from any of the four manufacturers shown. (In most instance, both through hole and surface mount inductors are available.) <br> 2. Output Capacitor Selection (COUT) <br> A. See section on output capacitors in application information section. <br> B. From the quick design component selection table shown in Figure 3, locate the 5V output voltage section. In the load current column, choose the load current line that is closest to the current needed in your application, for this example, use the 1 A line. In the maximum input voltage column, select the line that covers the input voltage needed in your application, in this example, use the 15 V line. Continuing on this line are recommended inductors and capacitors that will provide the best overall performance. <br> The capacitor list contains both through hole electrolytic and surface mount tantalum capacitors from four different capacitor manufacturers. It is recommended that both the manufacturers and the manufacturer's series that are listed in the table be used. <br> In this example aluminum electrolytic capacitors from several different manufacturers are available with the range of ESR numbers needed. <br> $220 \mu \mathrm{~F}$ 25V Panasonic HFQ Series <br> $220 \mu \mathrm{~F}$ 25V Nichicon PL Series <br> C. For a 5 V output, a capacitor voltage rating at least 7.5 V or more is needed. But, in this example, even a low ESR, switching grade, $220 \mu \mathrm{~F} 10 \mathrm{~V}$ aluminum electrolytic capacitor would exhibit approximately $225 \mathrm{~m} \Omega$ of ESR (see the curve in Figure 14 for the ESR vs voltage rating). This amount of ESR would result in relatively high output ripple voltage. To reduce the ripple to $1 \%$ of the output voltage, or less, a capacitor with a higher voltage rating (lower ESR) should be selected. A 16 V or 25 V capacitor will reduce the ripple voltage by approximately half. <br> 3. Catch Diode Selection (D1) <br> A. Refer to the table shown in Figure 12. In this example, a 3A, 20V, 1 N5820 Schottky diode will provide the best performance, and will not be overstressed even for a shorted output. |


| PROCEDURE (Fixed Output Voltage Version) |  |  |  |  | EXAMPLE (Fixed Output Voltage Version) |  |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| Effici <br> recov <br> 50 ns <br> much <br> 4. Inpu <br> A low <br> need <br> large <br> capa <br> leads <br> capa <br> load <br> must <br> exce <br> RMS <br> trolytic <br> For <br> should <br> volta <br> pacit <br> capa <br> be 2 <br> mend <br> factu <br> Use <br> passi <br> pin. <br> For <br> paci |  | also provid <br> ically have <br> tifiers such should not <br> In) <br> um or tant e input pin ents from a e located the RMS e selected capacitor assure th ve shown in s for severa alues. <br> ectrolytic, th mately 1.5 ust be exer (see Applic talum capa ximum input be surge cu <br> using ceram may cause <br> ormation, ation Infor | good results. erse recovery the 1N5400 used. <br> $m$ bypass ca ground pin to earing at the in to the IC us ent rating of be at least $1 /$ nufacturers da his current rat Figure 13 show different alumin <br> capacitor volta es the maxim ed if solid tan Information r voltage ratin oltage and it t tested by th <br> capacitors for vere ringing <br> section on tion section. | tra-fast imes of ies are <br> citor is prevent <br> ut. This <br> g short <br> e input <br> the DC <br> sheet <br> is not <br> typical <br> m elec- <br> e rating <br> m input <br> lum ca- <br> n input <br> should <br> recom- <br> manu- <br> put bythe $\mathrm{V}_{\text {IN }}$ <br> put ca- | 4. Input Cap <br> The import input volta nominal i capacitor $\mathrm{V}_{\text {IN }}$ ) would rating is 2 <br> The RMS tor in a bu current. In a RMS cu curves sh propriate 25 V line a rent rating $220 \mu \mathrm{~F}$, 2 <br> For a thr capacitor or equival manufactu RMS rippla For surfa can be us to the cap formation TPS serie from Spra | or ( $\mathrm{C}_{\mathrm{IN}}$ ) <br> parameters ating and th voltage of a voltage rat needed. The <br> nt rating req egulator is example, w rating of at in Figure 13 capacitor. ote which cap eater than apacitor cou hole desig asonic HFQ would be a capacitors rent ratings mount desig but caution r surge cur input capac vailable from are both sur | he Input ca MS current an alumin greater th thigher ca <br> ment for th oximately <br> 1A load, a 500 mA be used to $m$ the curv tor values mA . Either e used. <br> $220 \mu \mathrm{~F} / 2$ ies or Nich ate. other be used adequate. solid tantal be exercis rating (see in this da $X$, and the urrent test | citor are the ing. With a electrolytic 18V (1.5 $\times$ citor voltage <br> put capacihe DC load pacitor with needed. The lect an aplocate the RMS cur$180 \mu \mathrm{~F}$ or <br> electrolytic PL series es or other ovided the <br> capacitors with regard plication Insheet). The 93D series |
| Conditions |  |  | Inductor |  | Output Capacitor |  |  |  |
|  |  |  | Through Hole Electrolytic | Surface Mount Tantalum |  |
| Output Voltage (V) | Load Current (A) | Max Input Voltage (V) |  |  | Inductance ( $\mu \mathrm{H}$ ) | Inductor (\#) | Panasonic HFQ Series ( $\mu \mathrm{F} / \mathrm{V}$ ) | Nichicon PL Series ( $\mu \mathrm{F} / \mathrm{V}$ ) | AVX TPS Series ( $\mu \mathrm{F} / \mathrm{V}$ ) | ```Sprague 595D Series ( }\mu\textrm{F}/\textrm{V}``` |
| 3.3 | 1 | 5 | 22 | L24 | 330/16 | 330/16 | 220/10 | 330/10 |
|  |  | 7 | 33 | L23 | 270/25 | 270/25 | 220/10 | 270/10 |
|  |  | 10 | 47 | L31 | 220/25 | 220/35 | 220/10 | 220/10 |
|  |  | 40 | 68 | L30 | 180/35 | 220/35 | 220/10 | 180/10 |
|  | 0.5 | 6 | 47 | L13 | 220/25 | 220/16 | 220/10 | 220/10 |
|  |  | 10 | 68 | L21 | 150/35 | 150/25 | 100/16 | 150/16 |
|  |  | 40 | 100 | L20 | 150/35 | 82/35 | 100/16 | 100/20 |
| 5 | 1 | 8 | 33 | L28 | 330/16 | 330/16 | 220/10 | 270/10 |
|  |  | 10 | 47 | L31 | 220/25 | 220/25 | 220/10 | 220/10 |
|  |  | 15 | 68 | L30 | 180/35 | 180/35 | 220/10 | 150/16 |
|  |  | 40 | 100 | L29 | 180/35 | 120/35 | 100/16 | 120/16 |
|  | 0.5 | 9 | 68 | L21 | 180/16 | 180/16 | 220/10 | 150/16 |
|  |  | 20 | 150 | L19 | 120/25 | 1200/25 | 100/16 | 100/20 |
|  |  | 40 | 150 | L19 | 100/25 | 100/25 | 68/20 | 68/25 |
| 12 | 1 | 15 | 47 | L31 | 220/25 | 220/25 | 68/20 | 120/20 |
|  |  | 18 | 68 | L30 | 180/35 | 120/25 | 68/20 | 120/20 |
|  |  | 30 | 150 | L36 | 82/25 | 82/25 | 68/20 | 100/20 |
|  |  | 40 | 220 | L35 | 82/25 | 82/25 | 68/20 | 68/25 |
|  | 0.5 | 15 | 68 | L21 | 180/25 | 180/25 | 68/20 | 120/20 |
|  |  | 20 | 150 | L19 | 82/25 | 82/25 | 68/20 | 100/20 |
|  |  | 40 | 330 | L26 | 56/25 | 56/25 | 68/20 | 68/25 |

FIGURE 3. LM2595 Fixed Voltage Quick Design Component Selection Table

| LM2595 Series Buck Regulator Design Procedure (Adjustable Output) |  |
| :---: | :---: |
| PROCEDURE (Adjustable Output Voltage Version) | EXAMPLE (Adjustable Output Voltage Version) |
| Given: <br> $\mathrm{V}_{\text {OUT }}=$ Regulated Output Voltage <br> $\mathrm{V}_{\mathrm{IN}}(\max )=$ Maximum Input Voltage <br> $\mathrm{I}_{\text {LOAD }}(\mathrm{max})=$ Maximum Load Current <br> $\mathrm{F}=$ Switching Frequency (Fixed at a nominal 150 kHz ). <br> 1. Programming Output Voltage (Selecting $R_{1}$ and $R_{2}$, as shown in Figure 2) <br> Use the following formula to select the appropriate resistor values. $\mathrm{V}_{\text {OUT }}=\mathrm{V}_{\text {REF }}\left(1+\frac{\mathrm{R}_{2}}{\mathrm{R}_{1}}\right) \text { where } \mathrm{V}_{\text {REF }}=1.23 \mathrm{~V}$ <br> Select a value for $R_{1}$ between $240 \Omega$ and $1.5 \mathrm{k} \Omega$. The lower resistor values minimize noise pickup in the sensitive feedback pin. (For the lowest temperature coefficient and the best stability with time, use $1 \%$ metal film resistors.) $\mathrm{R}_{2}=\mathrm{R}_{1}\left(\frac{\mathrm{~V}_{\mathrm{OUT}}}{\mathrm{~V}_{\mathrm{REF}}}-1\right)$ | Given: |
|  | $\mathrm{V}_{\text {OUT }}=20 \mathrm{~V}$ |
|  | $\mathrm{V}_{\mathrm{IN}}($ max $)=$ |
|  | $l_{\text {LOAD }}(\max )=1 \mathrm{~A}$ |
|  | $\mathrm{F}=$ Switching Freq |
|  | 1. Programming Output Voltage (Selecting $R_{1}$ and $R_{2}$, as shown in Figure 2) |
|  | Select $R_{1}$ to be $1 \mathrm{k} \Omega, 1 \%$. Solve for $\mathrm{R}_{2}$. |
|  | $R_{2}=R_{1}\left(\frac{V_{\mathrm{OUT}}}{\mathrm{~V}_{\mathrm{REF}}}-1\right)=1 \mathrm{k}\left(\frac{20 \mathrm{~V}}{1.23 \mathrm{~V}}-1\right)$ |
|  | $R_{2}=1 \mathrm{k}(16.26-1)=15.26 \mathrm{k}$, closest $1 \%$ value is $15.4 \mathrm{k} \Omega$. |
|  |  |
|  |  |
| 2. Inductor Selection (L1) <br> A. Calculate the inductor Volt - microsecond constant $\mathrm{E} \bullet \mathrm{T}(\mathrm{V} \bullet \mu \mathrm{s})$, from the following formula: | 2. Inductor Selection (L1) |
|  | A. Calculate the inductor Volt - microsecond constant ( $\mathrm{E} \bullet \mathrm{T}$ ), |
| $E \cdot T=\left(V_{\text {IN }}-V_{\text {OUT }}-V_{S A T}\right) \cdot \frac{V_{\text {OUT }}+V_{D}}{V_{I N}-V_{S A T}+V_{D}} \cdot \frac{1000}{150 \mathrm{kHz}}(\mathrm{~V} \cdot \mu \mathrm{~S})$ | $=(28-20-1) \cdot \frac{20+0.5}{28-1+0.5} \cdot \frac{1000}{150}(\mathrm{~V} \cdot \mu \mathrm{~s})$ |
| where $\mathrm{V}_{\text {SAT }}=$ internal switch saturation voltage $=1 \mathrm{~V}$ and $V_{D}=$ diode forward voltage drop $=0.5 \mathrm{~V}$ | $\frac{20.5}{27.5} \bullet 6.67(\mathrm{~V} \bullet \mu \mathrm{~s})=34.8(\mathrm{~V} \bullet \mu \mathrm{~s})$ |
| B. Use the E - T value from the previous formula and | B. $\mathrm{E} \bullet \mathrm{T}=34.8(\mathrm{~V} \bullet$ |
| match it with Inductor V | C. $\mathrm{I}_{\text {LOAD }}(\max )=1 \mathrm{~A}$ |
| C. on the horizontal axis, select the maximum load current. | D. From the inductor value selection guide shown in Figure 8 , the inductance region intersected by the 35 (V • $\mu$ s) horizontal line and the 1 A vertical line is $100 \mu \mathrm{H}$, and |
|  | the inductor code is L29. |
| value and the Maximum Load Current value. Each region is identified by an inductance value and an inductor code (LXX). | E. From the table in Figure 9, locate line L29, and select an inductor part number from the list of manufacturers part numbers. |
| E. Select an appropriate inductor from the four manufacturer's part numbers listed in Figure 9. |  |
| 3. Output Capacitor Selection (COUT) | 3. Output Capacitor Selection ( $\mathrm{C}_{\mathrm{OU}}$ |
| A. In the majority of applications, low ESR electrolytic or solid tantalum capacitors between $47 \mu \mathrm{~F}$ and $330 \mu \mathrm{~F}$ | A. See section on COUT in Application Information section. |
| provide the best results. This capacitor should be located close to the IC using short capacitor leads and short copper traces. Do not use capacitors larger than $330 \mu \mathrm{~F}$. For additional information, see section on output capacitors in application information section. | B. From the quick design table shown in Figure 4, locate the output voltage column. From that column, locate the output voltage closest to the output voltage in your application. In this example, select the 24 V line. Under the output capacitor section, select a capacitor from the list |
| B. To simplify the capacitor selection procedure, refer to the quick design table shown in Figure 4. This table contains different output voltages, and lists various output capacitors that will provide the best design solutions. | of through hole electrolytic or surface mount tantalum types from four different capacitor manufacturers. It is recommended that both the manufacturers and the manufacturers series that are listed in the table be used. |
| C. The capacitor voltage rating should be at least 1.5 times greater than the output voltage, and often much higher voltage ratings are needed to satisfy the low ESR requirements needed for low output ripple voltage. | In this example, through hole aluminum electrolytic capacitors from several different manufacturers are available. <br> $82 \mu \mathrm{~F}, 35 \mathrm{~V}$ Panasonic HFQ Series |
|  | $82 \mu \mathrm{~F}, 35 \mathrm{~V}$ Nichicon PL Series |
|  | Example continued on next page. |

Procedure continued on next page.

## LM2595 Series Buck Regulator Design Procedure (Adjustable Output)

| PROCEDURE (Adjustable Output Voltage Version) |
| :--- |
| 4. Feedforward Capacitor (C $C_{\text {FF }}$ ) (See Figure 2) |
| For output voltages greater than approximately 10V, an |
| additional capacitor is required. The compensation ca- | additional capacitor is required. The compensation capacitor is typically between 50 pF and 10 nF , and is wired in parallel with the output voltage setting resistor, $\mathrm{R}_{2}$. It provides additional stability for high output voltages, low input-output voltages, and/or very low ESR output capacitors, such as solid tantalum capacitors

$$
C_{F F}=\frac{1}{31 \times 10^{3} \times R_{2}}
$$

This capacitor type can be ceramic, plastic, silver mica, etc. (Because of the unstable characteristics of ceramic capacitors made with Z5U material, they are not recommended.)
5. Catch Diode Selection (D1)
A. The catch diode current rating must be at least 1.3 times greater than the maximum load current. Also, if the power supply design must withstand a continuous output short, the diode should have a current rating equal to the maximum current limit of the LM2595. The most stressful condition for this diode is an overload or shorted output condition.
B. The reverse voltage rating of the diode should be at least 1.25 times the maximum input voltage.
C. This diode must be fast (short reverse recovery time) and must be located close to the LM2595 using short leads and short printed circuit traces. Because of their fast switching speed and low forward voltage drop, Schottky diodes provide the best performance and efficiency, and should be the first choice, especially in low output voltage applications. Ultra-fast recovery, or HighEfficiency rectifiers are also a good choice, but some types with an abrupt turn-off characteristic may cause instability or EMI problems. Ultra-fast recovery diodes typically have reverse recovery times of 50 ns or less. Rectifiers such as the 1N4001 series are much too slow and should not be used.
6. Input Capacitor ( $\mathrm{C}_{\mathrm{IN}}$ )

A low ESR aluminum or tantalum bypass capacitor is needed between the input pin and ground to prevent large voltage transients from appearing at the input. In addition, the RMS current rating of the input capacitor should be selected to be at least $1 / 2$ the DC load current. The capacitor manufacturers data sheet must be checked to assure that this current rating is not exceeded. The curve shown in Figure 13 shows typical RMS current ratings for several different aluminum electrolytic capacitor values.

This capacitor should be located close to the IC using short leads and the voltage rating should be approximately 1.5 times the maximum input voltage.
If solid tantalum input capacitors are used, it is recomended that they be surge current tested by the manufacturer.
Use caution when using a high dielectric constant ceramic capacitor for input bypassing, because it may cause severe ringing at the $\mathrm{V}_{\mathrm{IN}}$ pin.
For additional information, see section on input capacitors in application information section.
C. For a 20 V output, a capacitor rating of at least 30 V or more is needed. In this example, either a 35 V or 50 V capacitor would work. A 35 V rating was chosen, although a 50 V rating could also be used if a lower output ripple voltage is needed.
Other manufacturers or other types of capacitors may also be used, provided the capacitor specifications (especially the 100 kHz ESR) closely match the types listed in the table. Refer to the capacitor manufacturers data sheet for this information.
4. Feedforward Capacitor ( $\mathrm{C}_{\mathrm{FF}}$ )

The table shown in Figure 4 contains feed forward capacitor values for various output voltages. In this example, a 1 nF capacitor is needed.
5. Catch Diode Selection (D1)
A. Refer to the table shown in Figure 12. Schottky diodes provide the best performance, and in this example a 3A, 40V, 1N5822 Schottky diode would be a good choice. The 3A diode rating is more than adequate and will not be overstressed even for a shorted output.
6. Input Capacitor ( $\mathrm{C}_{\mathrm{IN}}$ )

The important parameters for the Input capacitor are the input voltage rating and the RMS current rating. With a nominal input voltage of 28 V , an aluminum electrolytic aluminum electrolytic capacitor with a voltage rating greater than 42V $\left(1.5 \times \mathrm{V}_{\mathrm{IN}}\right)$ would be needed. Since the the next higher capacitor voltage rating is 50 V , a 50 V capacitor should be used. The capacitor voltage rating of ( $1.5 \times \mathrm{V}_{\mathrm{IN}}$ ) is a conservative guideline, and can be modified somewhat if desired.
The RMS current rating requirement for the input capacitor of a buck regulator is approximately $1 / 2$ the DC load current. In this example, with a 1 A load, a capacitor with a RMS current rating of at least 500 mA is needed.
The curves shown in Figure 13 can be used to select an appropriate input capacitor. From the curves, locate the 50 V line and note which capacitor values have RMS current ratings greater than 500 mA . Either a $100 \mu \mathrm{~F}$ or $120 \mu \mathrm{~F}, 50 \mathrm{~V}$ capacitor could be used.
For a through hole design, a $120 \mu \mathrm{~F} / 50 \mathrm{~V}$ electrolytic capacitor (Panasonic HFQ series or Nichicon PL series or equivalent) would be adequate. Other types or other manufacturers capacitors can be used provided the RMS ripple current ratings are adequate.
For surface mount designs, solid tantalum capacitors can be used, but caution must be exercised with regard to the capacitor surge current rting (see Application Information or input capacitors in this data sheet). The TPS series available from AVX, and the 593D series from Sprague are both surge current tested.
To further simplify the buck regulator design procedure, National Semiconductor is making available computer design software to be used with the Simple Switcher line ot switching regulators. Switchers Made Simple (version 4.2 or later) is available on a $31 / 2^{\prime \prime}$ diskette for IBM compatible computers.

| LM2595 Series Buck Regulator Design Procedure (Adjustable Output) (Continued) |  |  |  |  |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| Output Voltage (V) | Through Hole Electrolytic Output Capacitor |  |  | Surface Mount Tantalum Output Capacitor |  |  |
|  | Panasonic HFQ Series ( $\mu \mathrm{F} / \mathrm{V}$ ) | Nichicon PL Series ( $\mu \mathrm{F} / \mathrm{V}$ ) | Feedforward Capacitor | AVX TPS <br> Series <br> ( $\mu \mathrm{F} / \mathrm{V}$ ) | Sprague 595D Series ( $\mu \mathrm{F} / \mathrm{V}$ ) | Feedforward Capacitor |
| 1.2 | 330/50 | 330/50 | 0 | 330/6.3 | 330/6.3 | 0 |
| 4 | 220/25 | 220/25 | 4.7 nF | 220/10 | 220/10 | 4.7 nF |
| 6 | 220/25 | 220/25 | 3.3 nF | 220/10 | 220/10 | 3.3 nF |
| 9 | 180/25 | 180/25 | 1.5 nF | 100/16 | 180/16 | 1.5 nF |
| 12 | 120/25 | 120/25 | 1.5 nF | 68/20 | 120/20 | 1.5 nF |
| 15 | 120/25 | 120/25 | 1.5 nF | 68/20 | 100/20 | 1.5 nF |
| 24 | 82/35 | 82/35 | 1 nF | 33/25 | 33/35 | 220 pF |
| 28 | 82/50 | 82/50 | 1 nF | 10/35 | 33/35 | 220 pF |

FIGURE 4. Output Capacitor and Feedforward Capacitor Selection Table

## LM2595 Series Buck Regulator Design Procedure

INDUCTOR VALUE SELECTION GUIDES (For Continuous Mode Operation)


| LM2595 Series Buck Regulator Design Procedure (Continued) |  |  |  |  |  |  |  |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  | Inductance ( $\mu \mathrm{H}$ ) | Current <br> (A) | Schott |  | Renco |  | Pulse Engineering |  | Coilcraft <br> Surface Mount |
|  |  |  | Through Hole | Surface Mount | Through Hole | Surface Mount | Through Hole | Surface Mount |  |
| L4 | 68 | 0.32 | 67143940 | 67144310 | RL-1284-68-43 | RL1500-68 | PE-53804 | PE-53804-S | DO1608-68 |
| L5 | 47 | 0.37 | 67148310 | 67148420 | RL-1284-47-43 | RL1500-47 | PE-53805 | PE-53805-S | DO1608-473 |
| L6 | 33 | 0.44 | 67148320 | 67148430 | RL-1284-33-43 | RL1500-33 | PE-53806 | PE-53806-S | DO1608-333 |
| L9 | 220 | 0.32 | 67143960 | 67144330 | RL-5470-3 | RL1500-220 | PE-53809 | PE-53809-S | DO3308-224 |
| L10 | 150 | 0.39 | 67143970 | 67144340 | RL-5470-4 | RL1500-150 | PE-53810 | PE-53810-S | DO3308-154 |
| L11 | 100 | 0.48 | 67143980 | 67144350 | RL-5470-5 | RL1500-100 | PE-53811 | PE-53811-S | DO3308-104 |
| L12 | 68 | 0.58 | 67143990 | 67144360 | RL-5470-6 | RL1500-68 | PE-53812 | PE-53812-S | DO3308-683 |
| L13 | 47 | 0.70 | 67144000 | 67144380 | RL-5470-7 | RL1500-47 | PE-53813 | PE-53813-S | DO3308-473 |
| L14 | 33 | 0.83 | 67148340 | 67148450 | RL-1284-33-43 | RL1500-33 | PE-53814 | PE-53814-S | DO3308-333 |
| L15 | 22 | 0.99 | 67148350 | 67148460 | RL-1284-22-43 | RL1500-22 | PE-53815 | PE-53815-S | DO3308-223 |
| L16 | 15 | 1.24 | 67148360 | 67148470 | RL-1284-15-43 | RL1500-15 | PE-53816 | PE-53816-S | DO3308-153 |
| L17 | 330 | 0.42 | 67144030 | 67144410 | RL-5471-1 | RL1500-330 | PE-53817 | PE-53817-S | DO3316-334 |
| L18 | 220 | 0.55 | 67144040 | 67144420 | RL-5471-2 | RL1500-220 | PE-53818 | PE-53818-S | DO3316-224 |
| L19 | 150 | 0.66 | 67144050 | 67144430 | RL-5471-3 | RL1500-150 | PE-53819 | PE-53819-S | DO3316-154 |
| L20 | 100 | 0.82 | 67144060 | 67144440 | RL-5471-4 | RL1500-100 | PE-53820 | PE-53820-S | DO3316-104 |
| L21 | 68 | 0.99 | 67144070 | 67144450 | RL-5471-5 | RL1500-68 | PE-53821 | PE-53821-S | DO3316-683 |
| L22 | 47 | 1.17 | 67144080 | 67144460 | RL-5471-6 | - | PE-53822 | PE-53822-S | DO3316-473 |
| L23 | 33 | 1.40 | 67144090 | 67144470 | RL-5471-7 | - | PE-53823 | PE-53823-S | DO3316-333 |
| L24 | 22 | 1.70 | 67148370 | 67144480 | RL-1283-22-43 | - | PE-53824 | PE-53824-S | DO3316-223 |
| L26 | 330 | 0.80 | 67144100 | 67144480 | RL-5471-1 | - | PE-53826 | PE-53826-S | DO5022P-334 |
| L27 | 220 | 1.00 | 67144110 | 67144490 | RL-5471-2 | - | PE-53827 | PE-53827-S | DO5022P-224 |
| L28 | 150 | 1.20 | 67144120 | 67144500 | RL-5471-3 | - | PE-53828 | PE-53828-S | DO5022P-154 |
| L29 | 100 | 1.47 | 67144130 | 67144510 | RL-5471-4 | - | PE-53829 | PE-53829-S | DO5022P-104 |
| L30 | 68 | 1.78 | 67144140 | 67144520 | RL-5471-5 | - | PE-53830 | PE-53830-S | DO5022P-683 |
| L35 | 47 | 2.15 | 67144170 | - | RL-5473-1 | - | PE-53935 | PE-53935-S | - |

FIGURE 9. Inductor Manufacturers Part Numbers

## LM2595 Series Buck Regulator Design Procedure (Continued)

| Coilcraft Inc. | Phone | $(800) 322-2645$ |
| :--- | :--- | :--- |
|  | FAX | $(708) 639-1469$ |
| Coilcraft Inc., Europe | Phone | +111236730595 |
|  | FAX | +441236730627 |
| Pulse Engineering Inc. | Phone | $(619) 674-8100$ |
|  | FAX | $(619) 674-8262$ |
| Pulse Engineering Inc., <br> Europe | Phone | +3539324107 |
|  | FAX | +3539324459 |
| Renco Electronics Inc. | Phone | $(800) 645-5828$ |
|  | FAX | $(516) 586-5562$ |
| Schott Corp. | Phone | $(612) 475-1173$ |
|  | FAX | $(612) 475-1786$ |


| Nichicon Corp. | Phone | (708) 843-7500 |
| :--- | :--- | :--- |
|  | FAX | $(708) 843-2798$ |
| Panasonic | Phone | $(714) 373-7857$ |
|  | FAX | $(714) 373-7102$ |
| AVX Corp. | Phone | $(803) 448-9411$ |
|  | FAX | $(803) 448-1943$ |
| Sprague/Vishay | Phone | $(207) 324-4140$ |
|  | FAX | $(207) 324-7223$ |

FIGURE 11. Capacitor Manufacturers Phone Numbers

FIGURE 10. Inductor Manufacturers Phone Numbers

| VR | 1A Diodes |  |  |  | 3A Diodes |  |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  | Surface Mount |  | Through Hole |  | Surface Mount |  | Through Hole |  |
|  | Schottky | Ultra Fast <br> Recovery | Schottky | Ultra Fast Recovery | Schottky | Ultra Fast <br> Recovery | Schottky | Ultra Fast <br> Recovery |
| 20 V | SK12 | All of these diodes are rated to at least 50 V . | 1N5817 | All of these diodes are rated to at least 50 V . |  | All of these diodes are rated to at least 50V. | 1N5820 | All of <br> these <br> diodes are rated to at least 50 V . |
|  |  |  | SR102 |  | SK32 |  | SR302 |  |
|  |  |  |  |  |  |  | MBR320 |  |
| 30V | SK13 |  | 1N5818 |  |  |  | 1N5821 |  |
|  | MBRS130 |  | SR103 |  | SK33 |  | MBR330 |  |
|  |  |  | 11DQ03 |  |  |  | 31DQ03 |  |
| 40V | SK14 |  |  |  |  |  | 1N5822 |  |
|  | MBRS140 |  | 1N5819 |  | SK34 |  | SR304 |  |
|  | 10BQ040 |  | SR104 |  | MBRS340 |  | MBR340 |  |
|  | 10MQ040 | MURS12010BF10 | 11DQ04 | MUR120 | 30WQ04 | MURS320 <br> 30WF10 | 31DQ04 |  |
| 50 V <br> or <br> More | MBRS160 |  | SR105 |  | SK35 |  | SR305 |  |
|  | 10BQ050 |  | MBR150 |  | MBR360 |  | MBR350 |  |
|  | 10MQ060 |  | 11DQ05 |  | 30WQ05 |  | 31DQ05 |  |

FIGURE 12. Diode Selection Table

## Application Information

## PIN FUNCTIONS

$+\mathbf{V}_{\text {IN }}$-This is the positive input supply for the IC switching regulator. A suitable input bypass capacitor must be present at this pin to minimize voltage transients and to supply the switching currents needed by the regulator.

## Ground-Circuit ground.

Output-Internal switch. The voltage at this pin switches between ( $+\mathrm{V}_{\mathbb{I N}}-\mathrm{V}_{\mathrm{SAT}}$ ) and approximately -0.5 V , with a duty cycle of approximately $\mathrm{V}_{\text {OUT }} / \mathrm{V}_{\text {IN }}$. To minimize coupling to sensitive circuitry, the PC board copper area connected to this pin should be kept to a minimum.
Feedback-Senses the regulated output voltage to complete the feedback loop.
$\overline{\mathbf{O N}} / \mathbf{O F F}$ —Allows the switching regulator circuit to be shut down using logic level signals thus dropping the total input supply current to approximately $85 \mu \mathrm{~A}$. Pulling this pin below a threshold voltage of approximately 1.3 V turns the regulator on, and pulling this pin above 1.3 V (up to a maximum of 25 V ) shuts the regulator down. If this shutdown feature is not needed, the ON/OFF pin can be wired to the ground pin or it can be left open, in either case the regulator will be in the ON condition.

## EXTERNAL COMPONENTS

$\mathrm{C}_{\text {IN }}$-A low ESR aluminum or tantalum bypass capacitor is needed between the input pin and ground pin. It must be located near the regulator using short leads. This capacitor prevents large voltage transients from appearing at the input, and provides the instantaneous current needed each time the switch turns on.

The important parameters for the Input capacitor are the voltage rating and the RMS current rating. Because of the relatively high RMS currents flowing in a buck regulator's input capacitor, this capacitor should be chosen for its RMS current rating rather than its capacitance or voltage ratings, although the capacitance value and voltage rating are directly related to the RMS current rating.
The RMS current rating of a capacitor could be viewed as a capacitor's power rating. The RMS current flowing through the capacitors internal ESR produces power which causes the internal temperature of the capacitor to rise. The RMS current rating of a capacitor is determined by the amount of current required to raise the internal temperature approximately $10^{\circ} \mathrm{C}$ above an ambient temperature of $105^{\circ} \mathrm{C}$. The ability of the capacitor to dissipate this heat to the surrounding air will determine the amount of current the capacitor can safely sustain. Capacitors that are physically large and have a large surface area will typically have higher RMS current ratings. For a given capacitor value, a higher voltage electrolytic capacitor will be physically larger than a lower voltage capacitor, and thus be able to dissipate more heat to the surrounding air, and therefore will have a higher RMS current rating.

The consequences of operating an electrolytic capacitor above the RMS current rating is a shortened operating life. The higher temperature speeds up the evaporation of the capacitor's electrolyte, resulting in eventual failure.
Selecting an input capacitor requires consulting the manufacturers data sheet for maximum allowable RMS ripple current. For a maximum ambient temperature of $40^{\circ} \mathrm{C}$, a general guideline would be to select a capacitor with a ripple current rating of approximately $50 \%$ of the DC load current. For ambient temperatures up to $70^{\circ} \mathrm{C}$, a current rating of $75 \%$ of the DC load current would be a good choice for a conservative design. The capacitor voltage rating must be at least 1.25 times greater than the maximum input voltage, and often a much higher voltage capacitor is needed to satisfy the RMS current requirements.
A graph shown in Figure 13 shows the relationship between an electrolytic capacitor value, its voltage rating, and the RMS current it is rated for. These curves were obtained from the Nichicon "PL" series of low ESR, high reliability electrolytic capacitors designed for switching regulator applications. Other capacitor manufacturers offer similar types of capacitors, but always check the capacitor data sheet.
"Standard" electrolytic capacitors typically have much higher ESR numbers, lower RMS current ratings and typically have a shorter operating lifetime.
Because of their small size and excellent performance, surface mount solid tantalum capacitors are often used for input bypassing, but several precautions must be observed. A small percentage of solid tantalum capacitors can short if the inrush current rating is exceeded. This can happen at turn on when the input voltage is suddenly applied, and of course, higher input voltages produce higher inrush currents. Several capacitor manufacturers do a $100 \%$ surge current testing on their products to minimize this potential problem. If high turn on currents are expected, it may be necessary to limit this current by adding either some resistance or inductance before the tantalum capacitor, or select a higher voltage capacitor. As with aluminum electrolytic capacitors, the RMS ripple current rating must be sized to the load current.

## FEEDFORWARD CAPACITOR

(Adjustable Output Voltage Version)
$\mathrm{C}_{\mathrm{FF}}-\mathrm{A}$ Feedforward Capacitor $\mathrm{C}_{\mathrm{FF}}$, shown across R2 in Figure 2 is used when the output voltage is greater than 10 V or when COUT has a very low ESR. This capacitor adds lead compensation to the feedback loop and increases the phase margin for better loop stability. For CFF selection, see the design procedure section.

## Application Information (Continued)



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## FIGURE 13. RMS Current Ratings for Low ESR Electrolytic Capacitors (Typical)

## OUTPUT CAPACITOR

CoUT-An output capacitor is required to filter the output and provide regulator loop stability. Low impedance or low ESR Electrolytic or solid tantalum capacitors designed for switching regulator applications must be used. When selecting an output capacitor, the important capacitor parameters are; the 100 kHz Equivalent Series Resistance (ESR), the RMS ripple current rating, voltage rating, and capacitance value. For the output capacitor, the ESR value is the most important parameter.
The output capacitor requires an ESR value that has an upper and lower limit. For low output ripple voltage, a low ESR value is needed. This value is determined by the maximum allowable output ripple voltage, typically $1 \%$ to $2 \%$ of the output voltage. But if the selected capacitor's ESR is extremely low, there is a possibility of an unstable feedback loop, resulting in an oscillation at the output. Using the capacitors listed in the tables, or similar types, will provide design solutions under all conditions.
If very low output ripple voltage (less than 15 mV ) is required, refer to the section on Output Voltage Ripple and Transients for a post ripple filter.
An aluminum electrolytic capacitor's ESR value is related to the capacitance value and its voltage rating. In most cases, higher voltage electrolytic capacitors have lower ESR values (see Figure 14). Often, capacitors with much higher voltage ratings may be needed to provide the low ESR values required for low output ripple voltage.
The output capacitor for many different switcher designs often can be satisfied with only three or four different capacitor values and several different voltage ratings. See the quick design component selection tables in Figures 3 and 4 for typical capacitor values, voltage ratings, and manufacturers capacitor types.
Electrolytic capacitors are not recommended for temperatures below $-25^{\circ} \mathrm{C}$. The ESR rises dramatically at cold temperatures and typically rises 3 X @ $-25^{\circ} \mathrm{C}$ and as much as 10 X at $-40^{\circ} \mathrm{C}$. See curve shown in Figure 15.
Solid tantalum capacitors have a much better ESR spec for cold temperatures and are recommended for temperatures below $-25^{\circ} \mathrm{C}$.


TL/H/12565-29
FIGURE 14. Capacitor ESR vs Capacitor Voltage Rating (Typical Low ESR Electrolytic Capacitor)

## CATCH DIODE

Buck regulators require a diode to provide a return path for the inductor current when the switch turns off. This must be a fast diode and must be located close to the LM2595 using short leads and short printed circuit traces.
Because of their very fast switching speed and low forward voltage drop, Schottky diodes provide the best performance, especially in low output voltage applications ( 5 V and lower). Ultra-fast recovery, or High-Efficiency rectifiers are also a good choice, but some types with an abrupt turnoff characteristic may cause instability or EMI problems. Ultrafast recovery diodes typically have reverse recovery times of 50 ns or less. Rectifiers such as the 1N5400 series are much too slow and should not be used.


TL/H/12565-30
FIGURE 15. Capacitor ESR Change vs Temperature

## INDUCTOR SELECTION

All switching regulators have two basic modes of operation; continuous and discontinuous. The difference between the two types relates to the inductor current, whether it is flowing continuously, or if it drops to zero for a period of time in the normal switching cycle. Each mode has distinctively different operating characteristics, which can affect the regulators performance and requirements. Most switcher designs will operate in the discontinuous mode when the load current is low.
The LM2595 (or any of the Simple Switcher family) can be used for both continuous or discontinuous modes of operation.

## Application Information (Continued)

In many cases the preferred mode of operation is the continuous mode. It offers greater output power, lower peak switch, inductor and diode currents, and can have lower output ripple voltage. But it does require larger inductor values to keep the inductor current flowing continuously, especially at low output load currents and/or high input voltages.
To simplify the inductor selection process, an inductor selection guide (nomograph) was designed (see Figures 5 through 8). This guide assumes that the regulator is operating in the continuous mode, and selects an inductor that will allow a peak-to-peak inductor ripple current to be a certain percentage of the maximum design load current. This peak-to-peak inductor ripple current percentage is not fixed, but is allowed to change as different design load currents are selected. (See Figure 16.)


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FIGURE 16. ( $\Delta \|_{\text {IND }}$ ) Peak-to-Peak Inductor Ripple Current (as a Percentage of the Load Current) vs Load Current

By allowing the percentage of inductor ripple current to increase for low load currents, the inductor value and size can be kept relatively low.
When operating in the continuous mode, the inductor current waveform ranges from a triangular to a sawtooth type of waveform (depending on the input voltage), with the average value of this current waveform equal to the DC output load current.
Inductors are available in different styles such as pot core, toroid, E-core, bobbin core, etc., as well as different core materials, such as ferrites and powdered iron. The least expensive, the bobbin, rod or stick core, consists of wire wound on a ferrite bobbin. This type of construction makes for an inexpensive inductor, but since the magnetic flux is not completely contained within the core, it generates more Electro-Magnetic Interference (EMI). This magnetic flux can induce voltages into nearby printed circuit traces, thus causing problems with both the switching regulator operation and nearby sensitive circuitry, and can give incorrect scope readings because of induced voltages in the scope probe. Also see section on Open Core Inductors.
When multiple switching regulators are located on the same PC board, open core magnetics can cause interference between two or more of the regulator circuits, especially at high currents. A torroid or E-core inductor (closed magnetic structure) should be used in these situations.
The inductors listed in the selection chart include ferrite E-core construction for Schott, ferrite bobbin core for Renco and Coilcraft, and powdered iron toroid for Pulse Engineering.

Exceeding an inductor's maximum current rating may cause the inductor to overheat because of the copper wire losses, or the core may saturate. If the inductor begins to saturate, the inductance decreases rapidly and the inductor begins to look mainly resistive (the DC resistance of the winding). This can cause the switch current to rise very rapidly and force the switch into a cycle-by-cycle current limit, thus reducing the DC output load current. This can also result in overheating of the inductor and/or the LM2595. Different inductor types have different saturation characteristics, and this should be kept in mind when selecting an inductor.
The inductor manufacturer's data sheets include current and energy limits to avoid inductor saturation.

## DISCONTINUOUS MODE OPERATION

The selection guide chooses inductor values suitable for continuous mode operation, but for low current applications and/or high input voltages, a discontinuous mode design may be a better choice. It would use an inductor that would be physically smaller, and would need only one half to one third the inductance value needed for a continuous mode design. The peak switch and inductor currents will be higher in a discontinuous design, but at these low load currents ( 400 mA and below), the maximum switch current will still be less than the switch current limit.
Discontinuous operation can have voltage waveforms that are considerable different than a continuous design. The output pin (switch) waveform can have some damped sinusoidal ringing present. (See Figure 1 photo titled; Discontinuous Mode Switching Waveforms) This ringing is normal for discontinuous operation, and is not caused by feedback loop instabilities. In discontinuous operation, there is a period of time where neither the switch or the diode are conducting, and the inductor current has dropped to zero. During this time, a small amount of energy can circulate between the inductor and the switch/diode parasitic capacitance causing this characteristic ringing. Normally this ringing is not a problem, unless the amplitude becomes great enough to exceed the input voltage, and even then, there is very little energy present to cause damage.
Different inductor types and/or core materials produce different amounts of this characteristic ringing. Ferrite core inductors have very little core loss and therefore produce the most ringing. The higher core loss of powdered iron inductors produce less ringing. If desired, a series RC could be placed in parallel with the inductor to dampen the ringing. The computer aided design software Switchers Made Simple (version 4.2) will provide all component values for continuous and discontinuous modes of operation.


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FIGURE 17. Post Ripple Filter Waveform

## Application Information (Continued)

## OUTPUT VOLTAGE RIPPLE AND TRANSIENTS

The output voltage of a switching power supply operating in the continuous mode will contain a sawtooth ripple voltage at the switcher frequency, and may also contain short voltage spikes at the peaks of the sawtooth waveform.
The output ripple voltage is a function of the inductor sawtooth ripple current and the ESR of the output capacitor. A typical output ripple voltage can range from approximately $0.5 \%$ to $3 \%$ of the output voltage. To obtain low ripple voltage, the ESR of the output capacitor must be low, however, caution must be exercised when using extremely low ESR capacitors because they can affect the loop stability, resulting in oscillation problems. If very low output ripple voltage is needed (less than 20 mV ), a post ripple filter is recommended. (See Figure 2.) The inductance required is typically between $1 \mu \mathrm{H}$ and $5 \mu \mathrm{H}$, with low DC resistance, to maintain good load regulation. A low ESR output filter capacitor is also required to assure good dynamic load response and ripple reduction. The ESR of this capacitor may be as low as desired, because it is out of the regulator feedback loop. The photo shown in Figure 17 shows a typical output ripple voltage, with and without a post ripple filter.
When observing output ripple with a scope, it is essential that a short, low inductance scope probe ground connection be used. Most scope probe manufacturers provide a special probe terminator which is soldered onto the regulator board, preferable at the output capacitor. This provides a very short scope ground thus eliminating the problems associated with the 3 inch ground lead normally provided with the probe, and provides a much cleaner and more accurate picture of the ripple voltage waveform.
The voltage spikes are caused by the fast switching action of the output switch and the diode, and the parasitic inductance of the output filter capacitor, and its associated wiring. To minimize these voltage spikes, the output capacitor should be designed for switching regulator applications, and the lead lengths must be kept very short. Wiring inductance, stray capacitance, as well as the scope probe used to evaluate these transients, all contribute to the amplitude of these spikes.
When a switching regulator is operating in the continuous mode, the inductor current waveform ranges from a triangular to a sawtooth type of waveform (depending on the input voltage). For a given input and output voltage, the peak-topeak amplitude of this inductor current waveform remains constant. As the load current increases or decreases, the entire sawtooth current waveform also rises and falls. The average value (or the center) of this current waveform is equal to the DC load current.
If the load current drops to a low enough level, the bottom of the sawtooth current waveform will reach zero, and the switcher will smoothly change from a continuous to a discontinuous mode of operation. Most switcher designs (irregardless how large the inductor value is) will be forced to run discontinuous if the output is lightly loaded. This is a perfectly acceptable mode of operation.


TL/H/12565-33
FIGURE 18. Peak-to-Peak Inductor Ripple Current vs Load Current

In a switching regulator design, knowing the value of the peak-to-peak inductor ripple current ( $\Delta \mathrm{I}_{\mathrm{IND}}$ ) can be useful for determining a number of other circuit parameters. Parameters such as, peak inductor or peak switch current, minimum load current before the circuit becomes discontinuous, output ripple voltage and output capacitor ESR can all be calculated from the peak-to-peak $\Delta I_{\text {IND }}$. When the inductor nomographs shown in Figures 5 through 8 are used to select an inductor value, the peak-to-peak inductor ripple current can immediately be determined. The curve shown in Figure 18 shows the range of ( $\Delta \mathrm{I}_{\mathrm{IND}}$ ) that can be expected for different load currents. The curve also shows how the peak-to-peak inductor ripple current ( $\Delta l_{\mathrm{IND}}$ ) changes as you go from the lower border to the upper border (for a given load current) within an inductance region. The upper border represents a higher input voltage, while the lower border represents a lower input voltage (see Inductor Selection Guides).
These curves are only correct for continuous mode operation, and only if the inductor selection guides are used to select the inductor value
Consider the following example:
$\mathrm{V}_{\text {OUT }}=5 \mathrm{~V}$, maximum load current of 800 mA
$\mathrm{V}_{\mathrm{IN}}=12 \mathrm{~V}$, nominal, varying between 10 V and 14 V .
The selection guide in Figure 6 shows that the vertical line for a 0.8 A load current, and the horizontal line for the 12 V input voltage intersect approximately midway between the upper and lower borders of the $68 \mu \mathrm{H}$ inductance region. A $68 \mu \mathrm{H}$ inductor will allow a peak-to-peak inductor current ( $\Delta l_{I N D}$ ) to flow that will be a percentage of the maximum load current. Referring to Figure 18, follow the 0.8A line approximately midway into the inductance region, and read the peak-to-peak inductor ripple current ( $\Delta \mathrm{I}_{\mathrm{IND}}$ ) on the left hand axis (approximately $300 \mathrm{~mA} \mathrm{p}-\mathrm{p}$ ).
As the input voltage increases to 14 V , it approaches the upper border of the inductance region, and the inductor ripple current increases. Referring to the curve in Figure 18, it can be seen that for a load current of 0.8 A , the peak-topeak inductor ripple current ( $\Delta \mathrm{I}_{\mathrm{IND}}$ ) is 300 mA with 12 V in, and can range from 340 mA at the upper border ( 14 V in) to 225 mA at the lower border ( 10 V in ).

## Application Information (Continued)

Once the $\Delta_{\text {IND }}$ value is known, the following formulas can be used to calculate additional information about the switching regulator circuit.

1. Peak Inductor or peak switch current

$$
=\left(\mathrm{I}_{\mathrm{LOAD}}+\frac{\Delta \mathrm{I}_{\mathrm{IND}}}{2}\right)=\left(0.8 \mathrm{~A}+\frac{0.30}{2}\right)=0.95 \mathrm{~A}
$$

2. Minimum load current before the circuit becomes discontinuous
$=\frac{\Delta l_{\text {IND }}}{2}=\frac{0.3}{2}=0.15 \mathrm{~A}$
3. Output Ripple Voltage $=\left(\Delta I_{I N D}\right) \times\left(E S R\right.$ of $\left.C_{O U T}\right)$ $=0.30 \mathrm{~A} \times 0.16 \Omega=48 \mathrm{mV} \mathrm{p}-\mathrm{p}$
or


$$
=\frac{0.048 \mathrm{~V}}{0.30 \mathrm{~A}}=0.16 \Omega
$$

## OPEN CORE INDUCTORS

Another possible source of increased output ripple voltage or unstable operation is from an open core inductor. Ferrite bobbin or stick inductors have magnetic lines of flux flowing through the air from one end of the bobbin to the other end. These magnetic lines of flux will induce a voltage into any wire or PC board copper trace that comes within the inductor's magnetic field. The strength of the magnetic field, the orientation and location of the PC copper trace to the magnetic field, and the distance between the copper trace and the inductor, determine the amount of voltage generated in the copper trace. Another way of looking at this inductive coupling is to consider the PC board copper trace as one turn of a transformer (secondary) with the inductor winding as the primary. Many millivolts can be generated in a copper trace located near an open core inductor which can cause stability problems or high output ripple voltage problems.
If unstable operation is seen, and an open core inductor is used, it's possible that the location of the inductor with respect to other PC traces may be the problem. To determine if this is the problem, temporarily raise the inductor away from the board by several inches and then check circuit operation. If the circuit now operates correctly, then the magnetic flux from the open core inductor is causing the problem. Substituting a closed core inductor such as a torroid or E-core will correct the problem, or re-arranging the PC layout may be necessary. Magnetic flux cutting the IC device ground trace, feedback trace, or the positive or negative traces of the output capacitor should be minimized.
Sometimes, locating a trace directly beneath a bobbin inductor will provide good results, provided it is exactly in the center of the inductor (because the induced voltages cancel themselves out), but if it is off center one direction or the other, then problems could arise. If flux problems are present, even the direction of the inductor winding can make a difference in some circuits.
This discussion on open core inductors is not to frighten the user, but to alert the user on what kind of problems to watch out for when using them. Open core bobbin or "stick" inductors are an inexpensive, simple way of making a compact efficient inductor, and they are used by the millions in many different applications.

## THERMAL CONSIDERATIONS

The LM2595 is available in two packages, a 5-pin TO-220 ( T ) and a 5 -pin surface mount TO-263 (S).
The TO-220 package can be used without a heat sink for ambient temperatures up to approximately $50^{\circ} \mathrm{C}$ (depending on the output voltage and load current). The curves in Figure 19 show the LM2595T junction temperature rises above ambient temperature for different input and output voltages. The data tor these curves was taken with the LM2595T (TO220 package) operating as a switching regutator in an ambient temperature of $25^{\circ} \mathrm{C}$ (still air). These temperature rise numbers are all approximate and there are many factors that can affect these temperatures. Higher ambient temperatures require some heat sinking, either to the PC board or a small external heat sink.
The TO-263 surface mount package tab is designed to be soldered to the copper on a printed circuit board. The copper and the board are the heat sink for this package and the other heat producing components, such as the catch diode and inductor. The PC board copper area that the package is soldered to should be at least $0.4 \mathrm{in}^{2}$, and ideally should have 2 or more square inches of 2 oz . ( 0.0028 in ) copper. Additional copper area improves the thermal characteristics, but with copper areas greater than approximately $3 \mathrm{in}^{2}$, only small improvements in heat dissipation are realized. If further thermal improvements are needed, double sided or multilayer PC-board with large copper areas are recommended.
The curves shown in Figure 20 show the LM2595S (TO-263 package) junction temperature rise above ambient temperature with a 1A load for various input and output voltages. This data was taken with the circuit operating as a buck switching regulator with all components mounted on a PC board to simulate the junction temperature under actual operating conditions. This curve can be used for a quick check for the approximate junction temperature for various conditions, but be aware that there are many factors that can affect the junction temperature.
For the best thermal performance, wide copper traces and generous amounts of printed circuit board copper should be used in the board layout. (One exception to this is the output (switch) pin, which should not have large areas of copper.) Large areas of copper provide the best transfer of heat (lower thermal resistance) to the surrounding air, and moving air lowers the thermal resistance even further.
Package thermal resistance and junction temperature rise numbers are all approximate, and there are many factors that will affect these numbers. Some of these factors include board size, shape, thickness, position, location, and even board temperature. Other factors are, trace width, total printed circuit copper area, copper thickness, single- or dou-ble-sided, multilayer board and the amount of solder on the board. The effectiveness of the PC board to dissipate heat also depends on the size, quantity and spacing of other components on the board, as well as whether the surrounding air is still or moving. Furthermore, some of these components such as the catch diode will add heat to the PC board and the heat can vary as the input voltage changes. For the inductor, depending on the physical size, type of core material and the DC resistance, it could either act as a heat sink taking heat away from the board, or it could add heat to the board.

## Application Information (Continued)



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| Circuit Data for Temperature Rise Curve <br> TO-220 Package (T) |  |
| :--- | :--- |
| Capacitors | Through hole electrolytic |
| Inductor | Through hole, Schott, 68 $\mu \mathrm{H}$ |
| Diode | Through hole, 3A 40V, Schottky |
| PC board | 3 square inches single sided 2 oz. copper <br> $\left(0.0028^{\prime \prime}\right)$ |

FIGURE 19. Junction Temperature Rise, TO-220


TL/H/12565-35

| Circuit Data for Temperature Rise Curve <br> TO-263 Package (S) |  |
| :--- | :--- |
| Capacitors | Surface mount tantalum, molded "D" size |
| Inductor | Surface mount, Schottky, 68 $\mu \mathrm{H}$ |
| Diode | Surface mount, 3A 40V, Schottky |
| PC board | 3 square inches single sided 2 oz. copper <br> $(0.0028 ")$ |

FIGURE 20. Junction Temperature Rise, TO-263


TL/H/12565-36
FIGURE 21. Delayed Startup


FIGURE 22. UndervoItage Lockout for Buck Regulator

## DELAYED STARTUP

The circuit in Figure 21 uses the the $\overline{O N} / O F F$ pin to provide a time delay between the time the input voltage is applied and the time the output voltage comes up (only the circuitry pertaining to the delayed start up is shown). As the input voltage rises, the charging of capacitor C1 pulls the $\overline{\mathrm{ON}} /$ OFF pin high, keeping the regulator off. Once the input voltage reaches its final value and the capacitor stops charging, and resistor $R_{2}$ pulls the $\overline{\mathrm{ON}}$ /OFF pin low, thus allowing the circuit to start switching. Resistor $R_{1}$ is included to limit the maximum voltage applied to the ON/OFF pin (maximum of 25 V ), reduces power supply noise sensitivity, and also limits the capacitor, C1, discharge current. When high input ripple voltage exists, avoid long delay time, because this ripple can be coupled into the ON/OFF pin and cause problems.
This delayed startup feature is useful in situations where the input power source is limited in the amount of current it can deliver. It allows the input voltage to rise to a higher voltage before the regulator starts operating. Buck regulators require less input current at higher input voltages.

## UNDERVOLTAGE LOCKOUT

Some applications require the regulator to remain off until the input voltage reaches a predetermined voltage. An undervoltage lockout feature applied to a buck regulator is shown in Figure 22, while Figures 23 and 24 applies the same feature to an inverting circuit. The circuit in Figure 23 features a constant threshold voltage for turn on and turn off (zener voltage plus approximately one volt). If hysteresis is needed, the circuit in Figure 24 has a turn ON voltage which is different than the turn OFF voltage. The amount of hysteresis is approximately equal to the value of the output voltage. If zener voltages greater than 25 V are used, an additional $47 \mathrm{k} \Omega$ resistor is needed from the $\overline{\mathrm{ON}} / \mathrm{OFF}$ pin to the ground pin to stay within the 25 V maximum limit of the ON/OFF pin.

## Application Information (Continued)

## INVERTING REGULATOR

The circuit in Figure 25 converts a positive input voltage to a negative output voltage with a common ground. The circuit operates by bootstrapping the regulator's ground pin to the negative output voltage, then grounding the feedback pin, the regulator senses the inverted output voltage and regulates it.


This circuit has an ON/OFF threshold of approximately 13 V .
FIGURE 23. Undervoltage Lockout for Inverting Regulator
This example uses the LM2595-5.0 to generate a -5 V output, but other output voltages are possible by selecting other output voltage versions, including the adjustable version.

Since this regulator topology can produce an output voltage that is either greater than or less than the input voltage, the maximum output current greatly depends on both the input and output voltage. The curve shown in Figure 26 provides a guide as to the amount of output load current possible for the different input and output voltage conditions.
The maximum voltage appearing across the regulator is the absolute sum of the input and output voltage, and this must be limited to a maximum of 40 V . For example, when converting +20 V to -12 V , the regulator would see 32 V between the input pin and ground pin. The LM2595 has a maximum input voltage spec of 40 V .
Additional diodes are required in this regulator configuration. Diode D1 is used to isolate input voltage ripple or noise from coupling through the $\mathrm{C}_{\mathrm{IN}}$ capacitor to the output, under light or no load conditions. Also, this diode isolation changes the topology to closley resemble a buck configuration thus providing good closed loop stability. A Schottky diode is recommended for low input voltages, (because of its lower voltage drop) but for higher input voltages, a fast recovery diode could be used.
Without diode D3, when the input voltage is first applied, the charging current of $\mathrm{C}_{\mathrm{IN}}$ can pull the output positive by several volts for a short period of time. Adding D3 prevents the output from going positive by more than a diode voltage.


FIGURE 24. Undervoltage Lockout with Hysteresis for Inverting Regulator


COUT - $22 \mu \mathrm{~F} / 20 \mathrm{~V}$ Tant. Sprague 595D

FIGURE 25. Inverting - 5V Regulator with Delayed Startup

## Application Information (Continued)



TL/H/12565-41
FIGURE 26. Inverting Regulator Typical Load Current
Because of differences in the operation of the inverting regulator, the standard design procedure is not used to select the inductor value. In the majority of designs, a $68 \mu \mathrm{H}, 1.5 \mathrm{~A}$ inductor is the best choice. Capacitor selection can also be narrowed down to just a few values. Using the values shown in Figure 25 will provide good results in the majority of inverting designs.
This type of inverting regulator can require relatively large amounts of input current when starting up, even with light
loads. Input currents as high as the LM2595 current limit (approx 1.5 A ) are needed for at least 2 ms or more, until the output reaches its nominal output voltage. The actual time depends on the output voltage and the size of the output capacitor. Input power sources that are current limited or sources that can not deliver these currents without getting loaded down, may not work correctly. Because of the relatively high startup currents required by the inverting topology, the delayed startup feature ( $C 1, R_{1}$ and $R_{2}$ ) shown in Figure 25 is recommended. By delaying the regulator startup, the input capacitor is allowed to charge up to a higher voltage before the switcher begins operating. A portion of the high input current needed for startup is now supplied by the input capacitor $\left(\mathrm{C}_{\mid \mathrm{N}}\right)$. For severe start up conditions, the input capacitor can be made much larger than normal.

## NVERTING REGULATOR SHUTDOWN METHODS

To use the $\overline{O N} /$ OFF pin in a standard buck configuration is simple, pull it below 1.3 V (@25 ${ }^{\circ} \mathrm{C}$, referenced to ground) to turn regulator ON , pull it above 1.3 V to shut the regulator OFF. With the inverting configuration, some level shifting is required, because the ground pin of the regulator is no longer at ground, but is now setting at the negative output voltage level. Two different shutdown methods for inverting regulators are shown in Figures 27 and 28.


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FIGURE 27. Inverting Regulator Ground Referenced Shutdown


TL/H/12565-43
FIGURE 28. Inverting Regulator Ground Referenced Shutdown using Opto Device

Application Information (Continued)
TYPICAL THROUGH HOLE PC BOARD LAYOUT, FIXED OUTPUT ( 2 X SIZE)



Physical Dimensions inches (millimeters)


5-Lead TO-220 (T)
Order Number LM2595T-3.3, LM2595T-5.0,
LM2595T-12 or LM2595T-ADJ
NS Package Number T05D



## Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.
Maximum Supply Voltage
45 V
$\overline{\text { ON/OFF Pin Input Voltage }} \quad-0.3 \leq \mathrm{V} \leq+25 \mathrm{~V}$
Feedback Pin Voltage $\quad-0.3 \leq \mathrm{V} \leq+25 \mathrm{~V}$
Output Voltage to Ground (Steady State) -1V
Power Dissipation Internally limited
Storage Temperature Range $\quad-65^{\circ} \mathrm{C}$ to $+150^{\circ} \mathrm{C}$
ESD Susceptibility
Human Body Model (Note 2) 2 kV


Temperature Range $\quad-40^{\circ} \mathrm{C} \leq \mathrm{T}_{\mathrm{J}}+125^{\circ} \mathrm{C}$
Supply Voltage 4.5 V to 40 V

## LM2596-3.3

Electrical Characteristics Specifications with standard type face are for $\mathrm{T}_{J}=25^{\circ} \mathrm{C}$, and those with boldface type apply over full Operating Temperature Range

| Symbol | Parameter | Conditions | LM2596-3.3 |  | Units <br> (Limits) |
| :---: | :---: | :---: | :---: | :---: | :---: |
|  |  |  | Typ <br> (Note 3) | $\begin{aligned} & \text { Limit } \\ & \text { (Note 4) } \end{aligned}$ |  |
| SYSTEM PARAMETERS (Note 5) Test Circuit Figure 2 |  |  |  |  |  |
| $\mathrm{V}_{\text {OUT }}$ | Output Voltage | $4.75 \mathrm{~V} \leq \mathrm{V}_{\text {IN }} \leq 40 \mathrm{~V}, 0.2 \mathrm{~A} \leq \mathrm{I}_{\text {LOAD }} \leq 3 \mathrm{~A}$ | 3.3 | $\begin{aligned} & 3.168 / \mathbf{3 . 1 3 5} \\ & 3.432 / \mathbf{3 . 4 6 5} \end{aligned}$ | $V$ $V(\min )$ $V(\max )$ |
| $\eta$ | Efficiency | $\mathrm{V}_{\mathrm{IN}}=12 \mathrm{~V}, \mathrm{l}_{\text {LOAD }}=3 \mathrm{~A}$ | 73 |  | \% |

LM2596-5.0
Electrical Characteristics Specifications with standard type face are for $\mathrm{T}_{\mathrm{J}}=25^{\circ} \mathrm{C}$, and those with boldface type apply over full Operating Temperature Range

| Symbol | Parameter | Conditions | LM2596-5.0 |  | Units (Limits) |
| :---: | :---: | :---: | :---: | :---: | :---: |
|  |  |  | Typ <br> (Note 3) | Limit (Note 4) |  |
| SYSTEM PARAMETERS (Note 5) Test Circuit Figure 2 |  |  |  |  |  |
| V OUT | Output Voltage | $7 \mathrm{~V} \leq \mathrm{V}_{\text {IN }} \leq 40 \mathrm{~V}, 0.2 \mathrm{~A} \leq \mathrm{I}_{\text {LOAD }} \leq 3 \mathrm{~A}$ | 5.0 | $\begin{aligned} & 4.800 / 4.750 \\ & 5.200 / 5.250 \end{aligned}$ |  |
| $\eta$ | Efficiency | $\mathrm{V}_{\mathrm{IN}}=12 \mathrm{~V}, \mathrm{I}_{\text {LOAD }}=3 \mathrm{~A}$ | 80 |  | \% |
| LM2596-12 <br> Electrical Characteristics Specifications with standard type face are for $\mathrm{T}_{\mathrm{J}}=25^{\circ} \mathrm{C}$, and those with boldface type apply over full Operating Temperature Range |  |  |  |  |  |
|  |  |  |  | 96-12 |  |
| Symbol | Parameter | Conditions | Typ (Note 3) | Limit (Note 4) | (Limits) |
| SYSTEM PARAMETERS (Note 5) Test Circuit Figure 2 |  |  |  |  |  |
| V OUT | Output Voltage | $15 \mathrm{~V} \leq \mathrm{V}_{\mathrm{IN}} \leq 40 \mathrm{~V}, 0.2 \mathrm{~A} \leq \mathrm{I}_{\text {LOAD }} \leq 3 \mathrm{~A}$ | 12.0 | $\begin{aligned} & 11.52 / \mathbf{1 1 . 4 0} \\ & 12.48 / \mathbf{1 2 . 6 0} \end{aligned}$ | $\begin{gathered} V \\ \mathrm{~V}(\min ) \\ \mathrm{V}(\max ) \end{gathered}$ |
| $\eta$ | Efficiency | $\mathrm{V}_{\mathrm{IN}}=12 \mathrm{~V}, \mathrm{I}_{\text {LOAD }}=3 \mathrm{~A}$ | 90 |  | \% |



## Electrical Characteristics (Continued)

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but do not guarantee specific performance limits. For guaranteed specifications and test conditions, see the Electrical Characteristics.
Note 2: The human body model is a 100 pF capacitor discharged through a 1.5 k resistor into each pin.
Note 3: Typical numbers are at $25^{\circ} \mathrm{C}$ and represent the most likely norm.
Note 4: All limits guaranteed at room temperature (standard type face) and at temperature extremes (bold type face). All room temperature limits are $100 \%$ production tested. All limits at temperature extremes are guaranteed via correlation using standard Statistical Quality Control (SQC) methods. All limits are used to calculate Average Outgoing Quality Level (AOQL).
Note 5: External components such as the catch diode, inductor, input and output capacitors, and voltage programming resistors can affect switching regulator system performance. When the LM2596 is used as shown in the Figure 2 test circuit, system performance will be as shown in system parameters section of Electrical Characteristics.
Note 6: The switching frequency is reduced when the second stage current limit is activated. The amount of reduction is determined by the severity of current overload.
Note 7: No diode, inductor or capacitor connected to output pin.
Note 8: Feedback pin removed from output and connected to OV to force the output transistor switch ON.
Note 9: Feedback pin removed from output and connected to 12 V for the $3.3 \mathrm{~V}, 5 \mathrm{~V}$, and the ADJ. version, and 15 V for the 12 V version, to force the output transistor switch OFF.
Note 10: $\mathrm{V}_{\mathrm{IN}}=40 \mathrm{~V}$.
Note 11: Junction to ambient thermal resistance (no external heat sink) for the TO-220 package mounted vertically, with the leads soldered to a printed circuit board with ( 1 oz .) copper area of approximately $1 \mathrm{in}^{2}$.
Note 12: Junction to ambient thermal resistance with the TO-263 package tab soldered to a single printed circuit board with $0.5 \mathrm{in}^{2}$ of ( 1 oz .) copper area.
Note 13: Junction to ambient thermal resistance with the TO-263 package tab soldered to a single sided printed circuit board with 2.5 in ${ }^{2}$ of ( 1 oz .) copper area. Note 14: Junction to ambient thermal resistance with the TO-263 package tab soldered to a double sided printed circuit board with 3 in ${ }^{2}$ of ( 1 oz .) copper area on the LM2596S side of the board, and approximately $16 \mathrm{in}^{2}$ of copper on the other side of the p-c board. See Application Information in this data sheet and the thermal model in Switchers Made Simple ${ }^{\circledR}$ version 4.3 software.

Typical Performance Characteristics (Circuit of Figure 2)


TL/H/12583-4
Switch Saturation Voltage



TL/H/12583-5



TL/H/12583-6


## Typical Performance Characteristics (Circuit of Figure 2) (Continued)



TL/H/12583-10

Shutdown
Quiescent Current


TL/H/12583-11
$\overline{\text { ON/OFF Pin }}$ Current (Sinking)


Minimum Operating Supply Voltage


TL/H/12583-12



TL/H/12583-16

Typical Performance Characteristics (Circuit of Figure 2)

Continuous Mode Switching Waveforms
$\mathrm{V}_{\text {IN }}=20 \mathrm{~V}, \mathrm{~V}_{\text {OUT }}=5 \mathrm{~V}$, ILOAD $=2 \mathrm{~A}$
L $=\mathbf{3 2} \mu \mathrm{H}$, C OUT $=\mathbf{2 2 0} \mu \mathrm{F}$, C OUT ESR $=\mathbf{5 0} \mathrm{m} \Omega$


Load Transient Response for Continuous Mode $\mathrm{V}_{\mathrm{IN}}=20 \mathrm{~V}, \mathrm{~V}_{\text {OUT }}=5 \mathrm{~V}$, $\mathrm{I}_{\text {LOAD }}=500 \mathrm{~mA}$ to 2 A L $=32 \mu \mathrm{H}$, C $_{\text {OUT }}=220 \mu \mathrm{~F}$, C $_{\text {OUT }} \mathrm{ESR}=50 \mathrm{~m} \Omega$


Discontinuous Mode Switching Waveforms $\mathrm{V}_{\text {IN }}=\mathbf{2 0 V}, \mathrm{V}_{\text {OUT }}=5 \mathrm{~V}$, I LOAD $=500 \mathrm{~mA}$ L $=10 \mu \mathrm{H}$, C OUT $=330 \mu \mathrm{~F}$, C $_{\text {OUT }} \mathrm{ESR}=45 \mathrm{~m} \Omega$


A: Output Pin Voltage, $10 \mathrm{~V} /$ div.
B: Inductor Current $0.5 \mathrm{~A} /$ div.
C: Output Ripple Voltage, $100 \mathrm{mV} /$ div. Horizontal Time Base: $2 \mu \mathrm{~s} / \mathrm{div}$.

Load Transient Response for Discontinuous Mode
$\mathrm{V}_{\text {IN }}=20 \mathrm{~V}, \mathrm{~V}_{\text {OUT }}=5 \mathrm{~V}$, $\mathrm{I}_{\text {LOAD }}=500 \mathrm{~mA}$ to 2 A
$\mathrm{L}=10 \mu \mathrm{H}$, C $_{\text {OUT }}=\mathbf{3 3 0} \mu \mathrm{F}$, C $_{\text {OUT }} \mathrm{ESR}=\mathbf{4 5} \mathrm{m} \Omega$


Horizontal Time Base: $200 \mu \mathrm{~s} / \mathrm{div}$.

Block Diagram


FIGURE 1

## Test Circuit and Layout Guidelines

$\mathrm{C}_{\mathrm{IN}}-470 \mu \mathrm{~F}, 50 \mathrm{~V}$, Aluminum Electrolytic
Nichicon "PL Series"
$\mathrm{C}_{\mathrm{OUT}}-220 \mu \mathrm{~F}, 25 \mathrm{~V}$ Aluminum Electrolytic,
Nichicon "PL Series"
D1 $-5 \mathrm{~A}, 40 \mathrm{~V}$ Schottky Rectifier, 1N5825
L1 $-68 \mu \mathrm{H}, \mathrm{L} 38$


FIGURE 2. Standard Test Circuits and Layout Guides

As in any switching regulator, layout is very important. Rapidly switching currents associated with wiring inductance can generate voltage transients which can cause problems. For minimal inductance and ground loops, the wires indicated by heavy lines should be wide printed circuit traces and should be kept as short as possible. For best results, external components should be located as close to the switcher IC as possible using ground plane construction or single point grounding.

If open core inductors are used, special care must be taken as to the location and positioning of this type of inductor. Allowing the inductor flux to intersect sensitive feedback, IC groundpath and COUT wiring can cause problems. When using the adjustable version, special care must be taken as to the location of the feedback resistors and the associated wiring. Physically locate both resistors near the IC, and route the wiring away from the inductor, especially an open core type of inductor. (See application section for more information.)

| LM2596 Series Buck Regulator Design Procedure (Fixed Output) |  |
| :---: | :---: |
| PROCEDURE (Fixed Output Voltage Version) | EXAMPLE (Fixed Output Voltage Version) |
| Given: <br> $\mathrm{V}_{\text {OUT }}=$ Regulated Output Voltage (3.3V, 5 V or 12 V ) <br> $\mathrm{V}_{\mathrm{IN}}(\max )=$ Maximum DC Input Voltage <br> LLOAD (max) $=$ Maximum Load Current <br> 1. Inductor Selection (L1) <br> A. Select the correct inductor value selection guide from Figures 5, 6, or 7 . (Output voltages of $3.3 \mathrm{~V}, 5 \mathrm{~V}$, or 12 V respectively.) For all other voltages, see the design procedure for the adjustable version. <br> B. From the inductor value selection guide, identify the inductance region intersected by the Maximum Input Voltage line and the Maximum Load Current line. Each region is identified by an inductance value and an inductor code (LXX). <br> C. Select an appropriate inductor from the four manufacturer's part numbers listed in Figure 9. <br> 2. Output Capacitor Selection (COUT) <br> A. In the majority of applications, low ESR (Equivalent Series Resistance) electrolytic capacitors between $82 \mu \mathrm{~F}$ and $820 \mu \mathrm{~F}$ and low ESR solid tantalum capacitors between $10 \mu \mathrm{~F}$ and $470 \mu \mathrm{~F}$ provide the best results. This capacitor should be located close to the IC using short capacitor leads and short copper traces. Do not use capacitors larger than $820 \mu \mathrm{~F}$. <br> For additional information, see section on output capacitors in application information section. <br> B. To simplify the capacitor selection procedure, refer to the quick design component selection table shown in Figure 3. This table contains different input voltages, output voltages, and load currents, and lists various inductors and output capacitors that will provide the best design solutions. <br> C. The capacitor voltage rating for electrolytic capacitors should be at least 1.5 times greater than the output voltage, and often much higher voltage ratings are needed to satisfy the low ESR requirements for low output ripple voltage. <br> D. For computer aided design software, see Switchers Made Simple ${ }^{\circledR}$ version 4.3 or later. <br> 3. Catch Diode Selection (D1) <br> A. The catch diode current rating must be at least 1.3 times greater than the maximum load current. Also, if the power supply design must withstand a continuous output short, the diode should have a current rating equal to the maximum current limit of the LM2596. The most stressful condition for this diode is an overload or shorted output condition. <br> B. The reverse voltage rating of the diode should be at least 1.25 times the maximum input voltage. <br> C. This diode must be fast (short reverse recovery time) and must be located close to the LM2596 using short leads and short printed circuit traces. Because of their fast switching speed and low forward voltage drop, Schottky diodes provide the best performance and efficiency, and should be the first choice, especially in low output voltage applications. Ultra-fast recovery, or HighProcedure continued on next page. | Given: $\begin{aligned} & \mathrm{V}_{\text {OUT }}=5 \mathrm{~V} \\ & \mathrm{~V}_{\text {IN }}(\max )=12 \mathrm{~V} \\ & \mathrm{I}_{\text {LOAD }}(\max )=3 \mathrm{~A} \end{aligned}$ <br> 1. Inductor Selection (L1) <br> A. Use the inductor selection guide for the 5 V version shown in Figure 6. <br> B. From the inductor value selection guide shown in Figure 6 , the inductance region intersected by the 12 V horizontal line and the 3 A vertical line is $33 \mu \mathrm{H}$, and the inductor code is L40. <br> C. The inductance value required is $33 \mu \mathrm{H}$. From the table in Figure 9, go to the L40 line and choose an inductor part number from any of the four manufacturers shown. (In most instance, both through hole and surface mount inductors are available.) <br> 2. Output Capacitor Selection (COUT) <br> A. See section on output capacitors in application information section. <br> B. From the quick design component selection table shown in Figure 3, locate the 5V output voltage section. In the load current column, choose the load current line that is closest to the current needed in your application, for this example, use the 3A line. In the maximum input voltage column, select the line that covers the input voltage needed in your application, in this example, use the 15 V line. Continuing on this line are recommended inductors and capacitors that will provide the best overall performance. <br> The capacitor list contains both through hole electrolytic and surface mount tantalum capacitors from four different capacitor manufacturers. It is recommended that both the manufacturers and the manufacturer's series that are listed in the table be used. <br> In this example aluminum electrolytic capacitors from several different manufacturers are available with the range of ESR numbers needed. <br> $330 \mu \mathrm{~F}$ 35V Panasonic HFQ Series <br> $330 \mu \mathrm{~F}$ 35V Nichicon PL Series <br> C. For a 5 V output, a capacitor voltage rating at least 7.5 V or more is needed. But even a low ESR, switching grade, $220 \mu \mathrm{~F} 10 \mathrm{~V}$ aluminum electrolytic capacitor would exhibit approximately $225 \mathrm{~m} \Omega$ of ESR (see the curve in Figure 14 for the ESR vs voltage rating). This amount of ESR would result in relatively high output ripple voltage. To reduce the ripple to $1 \%$ of the output voltage, or less, a capacitor with a higher value or with a higher voltage rating (lower ESR) should be selected. A 16 V or 25 V capacitor will reduce the ripple voltage by approximately half. <br> 3. Catch Diode Selection (D1) <br> A. Refer to the table shown in Figure 12. In this example, a $5 \mathrm{~A}, 20 \mathrm{~V}$, 1N5823 Schottky diode will provide the best performance, and will not be overstressed even for a shorted output. |


| PROCEDURE (Fixed Output Voltage Version) |  |  |  |  | EXAMPLE (Fixed Output Voltage Version) |  |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| Effici recov 50 ns much <br> 4. Inpu <br> A low need large capa leads. capa load must exce RMS trolytic <br> For should volta pacit capa be 2 mend factu Use passi pin. For pacit | ncy rectifie ry diodes or less. R too slow and Capacitor ESR alum d between oltage tra tor should In additio tor should urrent. Th <br> be checke ded. The current ratin capacitor aluminum be approxi e. Caution s are use tor). The ta imes the d that the <br> aution when <br> g , becaus <br> dditional i rs in App | also provi <br> pically have tifiers such should not <br> (1) <br> um or tan he input pin ients from e located the RMS e selected capacitor o assure th ve shown s for sever values. <br> lectrolytic, th mately 1.5 ust be exer (see Applic talum capa ximum inpu be surge cu <br> using ceram it may caus <br> ormation, ation Infor | good results. erse recovery the 1N5400 used. <br> m bypass ca ground pin aring at the to the IC u ent rating of be at least ufacturers d is current ra igure 13 sho fferent alumi <br> apacitor volt es the maxim d if solid $\tan$ Information voltage rati oltage and it ht tested by <br> capacitors for vere ringing <br> section on tion section | tra-fast mes of ies are <br> citor is prevent <br> ut. This <br> g short <br> e input <br> the DC <br> sheet <br> is not <br> typical <br> m elec- <br> rating <br> m input <br> um ca- <br> n input <br> should <br> recom- <br> manu- <br> put bythe $\mathrm{V}_{\text {IN }}$ <br> put ca- | 4. Input Cap <br> The import input volta nominal in capacitor $V_{\text {IN }}$ ) would rating is 2 <br> The RMS tor in a buck current. In a RMS c curves sh propriate 35 V line and rent rating could be For a thr capacitor or equival manufactu RMS ripp For surfa can be us to the cap formation TPS serie from Spra | ( $\mathrm{C}_{\mathrm{IN}}$ ) <br> parameters rating and the voltage of a voltage r needed. The <br> nt rating re egulator is example, w rating of in Figure 13 capacitor. te which cap ater than <br> hole desig asonic HFQ would be a capacitors rent ratings ount desig ut caution r surge cur input capac ailable from are both su | he Input cap MS curren an alumin greater th higher ca <br> ment for th ximately 3A load, 1.5A be used to the curv tor values A $680 \mu \mathrm{~F}$ <br> $680 \mu \mathrm{~F} / 3$ es or Nich ate. other be used adequate. olid tantal be exercis ating (see in this data $X$, and th urrent test | citor are the ting. With a electrolytic 18V (1.5 $\times$ itor voltage <br> nput capacihe DC load pacitor with needed. The elect an aplocate the RMS curV capacitor <br> electrolytic n PL series es or other provided the <br> capacitors with regard plication Insheet). The 593D series |
| Conditions |  |  | Inductor |  | Output Capacitor |  |  |  |
|  |  |  | Through Hole Electrolytic | Surface Mount Tantalum |  |
| Output Voltage (V) | Load Current (A) | Max Input Voltage (V) |  |  | Inductance <br> ( $\mu \mathrm{H}$ ) | Inductor (\#) | Panasonic HFQ Series ( $\mu \mathrm{F} / \mathrm{V}$ ) | Nichicon PL Series ( $\mu \mathrm{F} / \mathrm{V}$ ) | AVX TPS Series ( $\mu \mathrm{F} / \mathrm{V}$ ) | $\begin{gathered} \text { Sprague } \\ \text { 595D Series } \\ (\mu \mathrm{F} / \mathrm{V}) \\ \hline \end{gathered}$ |
| 3.3 | 3 | 5 | 22 | L41 | 470/25 | 560/16 | 330/6.3 | 390/6.3 |
|  |  | 7 | 22 | L41 | 560/35 | 560/35 | 330/6.3 | 390/6.3 |
|  |  | 10 | 22 | L41 | 680/35 | 680/35 | 330/6.3 | 390/6.3 |
|  |  | 40 | 33 | L40 | 560/35 | 470/35 | 330/6.3 | 390/6.3 |
|  | 2 | 6 | 22 | L33 | 470/25 | 470/35 | 330/6.3 | 390/6.3 |
|  |  | 10 | 33 | L32 | 330/35 | 330/35 | 330/6.3 | 390/6.3 |
|  |  | 40 | 47 | L39 | 330/35 | 270/50 | 220/10 | 330/10 |
| 5 | 3 | 8 | 22 | L41 | 470/25 | 560/16 | 220/10 | 330/10 |
|  |  | 10 | 22 | L41 | 560/25 | 560/25 | 220/10 | 330/10 |
|  |  | 15 | 33 | L40 | 330/35 | 330/35 | 220/10 | 330/10 |
|  |  | 40 | 47 | L39 | 330/35 | 270/35 | 220/10 | 330/10 |
|  | 2 | 9 | 22 | L33 | 470/25 | 560/16 | 220/10 | 330/10 |
|  |  | 20 | 68 | L38 | 180/35 | 180/35 | 100/10 | 270/10 |
|  |  | 40 | 68 | L38 | 180/35 | 180/35 | 100/10 | 270/10 |
| 12 | 3 | 15 | 22 | L41 | 470/25 | 470/25 | 100/16 | 180/16 |
|  |  | 18 | 33 | L40 | 330/25 | 330/25 | 100/16 | 180/16 |
|  |  | 30 | 68 | L44 | 180/25 | 180/25 | 100/16 | 120/20 |
|  |  | 40 | 68 | L44 | 180/35 | 180/35 | 100/16 | 120/20 |
|  | 2 | 15 | 33 | L32 | 330/25 | 330/25 | 100/16 | 180/16 |
|  |  | 20 | 68 | L38 | 180/25 | 180/25 | 100/16 | 120/20 |
|  |  | 40 | 150 | L42 | 82/25 | 82/25 | 68/20 | 68/25 |



## LM2596 Series Buck Regulator Design Procedure (Adjustable Output)

| PROCEDURE (Adjustable Output Voltage Version) |
| :--- |
| 4. Feedforward Capacitor (C $\mathrm{C}_{\mathrm{FF}}$ ) (See Figure 2) |
| For output voltages greater than approximately 10V, an |
| additional capacitor is required. The compensation ca- | additional capacitor is required. The compensation capacitor is typically between 100 pF and 33 nF , and is wired in parallel with the output voltage setting resistor, $\mathrm{R}_{2}$. It provides additional stability for high output voltages, low input-output voltages, and/or very low ESR output capacitors, such as solid tantalum capacitors.

$$
C_{F F}=\frac{1}{31 \times 10^{3} \times R_{2}}
$$

This capacitor type can be ceramic, plastic, silver mica, etc. (Because of the unstable characteristics of ceramic capacitors made with Z5U material, they are not recommended.)
5. Catch Diode Selection (D1)
A. The catch diode current rating must be at least 1.3 times greater than the maximum load current. Also, if the power supply design must withstand a continuous output short, the diode should have a current rating equal to the maximum current limit of the LM2596. The most stressful condition for this diode is an overload or shorted output condition.
B. The reverse voltage rating of the diode should be at least 1.25 times the maximum input voltage.
C. This diode must be fast (short reverse recovery time) and must be located close to the LM2596 using short leads and short printed circuit traces. Because of their fast switching speed and low forward voltage drop, Schottky diodes provide the best performance and efficiency, and should be the first choice, especially in low output voltage applications. Ultra-fast recovery, or HighEfficiency rectifiers are also a good choice, but some types with an abrupt turn-off characteristic may cause instability or EMI problems. Ultra-fast recovery diodes typically have reverse recovery times of 50 ns or less. Rectifiers such as the 1N4001 series are much too slow and should not be used.
6. Input Capacitor ( $\mathrm{C}_{\mathrm{IN}}$ )

A low ESR aluminum or tantalum bypass capacitor is needed between the input pin and ground to prevent large voltage transients from appearing at the input. In addition, the RMS current rating of the input capacitor should be selected to be at least $1 / 2$ the DC load current. The capacitor manufacturers data sheet must be checked to assure that this current rating is not exceeded. The curve shown in Figure 13 shows typical RMS current ratings for several different aluminum electrolytic capacitor values.
This capacitor should be located close to the IC using short leads and the voltage rating should be approximately 1.5 times the maximum input voltage.
If solid tantalum input capacitors are used, it is recomended that they be surge current tested by the manufacturer.
Use caution when using a high dielectric constant ceramic capacitor for input bypassing, because it may cause severe ringing at the $\mathrm{V}_{\mathrm{IN}}$ pin.
For additional information, see section on input capacitors in application information section.
C. For a 20 V output, a capacitor rating of at least 30 V or more is needed. In this example, either a 35 V or 50 V capacitor would work. A 35 V rating was chosen, although a 50 V rating could also be used if a lower output ripple voltage is needed.
Other manufacturers or other types of capacitors may also be used, provided the capacitor specifications (especially the 100 kHz ESR) closely match the types listed in the table. Refer to the capacitor manufacturers data sheet for this information.
4. Feedforward Capacitor ( $\mathrm{C}_{\mathrm{FF}}$ )

The table shown in Figure 4 contains feed forward capacitor values for various output voltages. In this example, a 560 pF capacitor is needed.
5. Catch Diode Selection (D1)
A. Refer to the table shown in Figure 12. Schottky diodes provide the best performance, and in this example a 5A, 40V, 1N5825 Schottky diode would be a good choice. The 5A diode rating is more than adequate and will not be overstressed even for a shorted output.
6. Input Capacitor ( $\mathrm{C}_{\mathrm{IN}}$ )

The important parameters for the Input capacitor are the input voltage rating and the RMS current rating. With a nominal input voltage of 28 V , an aluminum electrolytic aluminum electrolytic capacitor with a voltage rating greater than 42V $\left(1.5 \times \mathrm{V}_{\mathrm{IN}}\right)$ would be needed. Since the the next higher capacitor voltage rating is 50 V , a 50 V capacitor should be used. The capacitor voltage rating of ( $1.5 \times \mathrm{V}_{\mathrm{IN}}$ ) is a conservative guideline, and can be modified somewhat if desired.
The RMS current rating requirement for the input capacitor of a buck regulator is approximately $1 / 2$ the DC load current. In this example, with a 3A load, a capacitor with a RMS current rating of at least 1.5 A is needed.
The curves shown in Figure 13 can be used to select an appropriate input capacitor. From the curves, locate the 50 V line and note which capacitor values have RMS current ratings greater than 1.5 A . Either a $470 \mu \mathrm{~F}$ or $680 \mu \mathrm{~F}, 50 \mathrm{~V}$ capacitor could be used.
For a through hole design, a $680 \mu \mathrm{~F} / 50 \mathrm{~V}$ electrolytic capacitor (Panasonic HFQ series or Nichicon PL series or equivalent) would be adequate. Other types or other manufacturers capacitors can be used provided the RMS ripple current ratings are adequate.
For surface mount designs, solid tantalum capacitors can be used, but caution must be exercised with regard to the capacitor surge current rting (see Application Information or input capacitors in this data sheet). The TPS series available from AVX, and the 593D series from Sprague are both surge current tested.
To further simplify the buck regulator design procedure, National Semiconductor is making available computer design software to be used with the Simple Switcher line ot switching regulators. Switchers Made Simple (version 4.3 or later) is available on a $31 / 2^{\prime \prime}$ diskette for IBM compatible computers.

| LM2596 Series Buck Regulator Design Procedure (Adjustable Output) <br> (Continued) |  |  |  |  |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  | Through Hole Output Capacitor |  |  | Surface Mount Output Capacitor |  |  |
| Voltage <br> (V) | Panasonic HFQ Series ( $\mu \mathrm{F} / \mathrm{V}$ ) | Nichicon PL <br> Series ( $\mu \mathrm{F} / \mathrm{V}$ ) | Feedforward Capacitor | AVX TPS <br> Series ( $\mu \mathrm{F} / \mathrm{V}$ ) | Sprague 595D Series ( $\mu \mathrm{F} / \mathrm{V}$ ) | Feedforward Capacitor |
| 2 | 820/35 | 820/35 | 33 nF | 330/6.3 | 470/4 | 33 nF |
| 4 | 560/35 | 470/35 | 10 nF | 330/6.3 | 390/6.3 | 10 nF |
| 6 | 470/25 | 470/25 | 3.3 nF | 220/10 | 330/10 | 3.3 nF |
| 9 | 330/25 | 330/25 | 1.5 nF | 100/16 | 180/16 | 1.5 nF |
| 12 | 330/25 | 330/25 | 1 nF | 100/16 | 180/16 | 1 nF |
| 15 | 220/35 | 220/35 | 680 pF | 68/20 | 120/20 | 680 pF |
| 24 | 220/35 | 150/35 | 560 pF | 33/25 | 33/25 | 220 pF |
| 28 | 100/50 | 100/50 | 390 pF | 10/35 | 15/50 | 220 pF |

FIGURE 4. Output Capacitor and Feedforward Capacitor Selection Table

## LM2596 Series Buck Regulator Design Procedure

INDUCTOR VALUE SELECTION GUIDES (For Continuous Mode Operation)


FIGURE 5. LM2596-3.3


TL/H/12583-26


FIGURE 6. LM2596-5.0


FIGURE 8. LM2596-ADJ

|  | Inductance ( $\mu \mathrm{H}$ ) | Current <br> (A) | Schott |  | Renco |  | Pulse Engineering |  | Coilcraft <br> Surface Mount |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  |  | Through Hole | Surface Mount | Through Hole | Surface Mount | Through Hole | Surface Mount |  |
| L15 | 22 | 0.99 | 67148350 | 67148460 | RL-1284-22-43 | RL1500-22 | PE-53815 | PE-53815-S | DO3308-223 |
| L21 | 68 | 0.99 | 67144070 | 67144450 | RL-5471-5 | RL1500-68 | PE-53821 | PE-53821-S | DO3316-683 |
| L22 | 47 | 1.17 | 67144080 | 67144460 | RL-5471-6 | - | PE-53822 | PE-53822-S | DO3316-473 |
| L23 | 33 | 1.40 | 67144090 | 67144470 | RL-5471-7 | - | PE-53823 | PE-53823-S | DO3316-333 |
| L24 | 22 | 1.70 | 67148370 | 67148480 | RL-1283-22-43 | - | PE-53824 | PE-53825-S | DO3316-223 |
| L25 | 15 | 2.10 | 67148380 | 67148490 | RL-1283-15-43 | - | PE-53825 | PE-53824-S | DO3316-153 |
| L26 | 330 | 0.80 | 67144100 | 67144480 | RL-5471-1 | - | PE-53826 | PE-53826-S | DO5022P-334 |
| L27 | 220 | 1.00 | 67144110 | 67144490 | RL-5471-2 | - | PE-53827 | PE-53827-S | DO5022P-224 |
| L28 | 150 | 1.20 | 67144120 | 67144500 | RL-5471-3 | - | PE-53828 | PE-53828-S | DO5022P-154 |
| L29 | 100 | 1.47 | 67144130 | 67144510 | RL-5471-4 | - | PE-53829 | PE-53829-S | DO5022P-104 |
| L30 | 68 | 1.78 | 67144140 | 67144520 | RL-5471-5 | - | PE-53830 | PE-53830-S | DO5022P-683 |
| L31 | 47 | 2.20 | 67144150 | 67144530 | RL-5471-6 | - | PE-53831 | PE-53831-S | DO5022P-473 |
| L32 | 33 | 2.50 | 67144160 | 67144540 | RL-5471-7 | - | PE-53932 | PE-53932-S | DO5022P-333 |
| L33 | 22 | 3.10 | 67148390 | 67148500 | RL-1283-22-43 | - | PE-53933 | PE-53933-S | DO5022P-223 |
| L34 | 15 | 3.40 | 67148400 | 67148790 | RL-1283-15-43 | - | PE-53934 | PE-53934-S | DO5022P-153 |
| L35 | 220 | 1.70 | 67144170 | - | RL-5473-1 | - | PE-53935 | PE-53935-S | - |
| L36 | 150 | 2.10 | 67144180 | - | RL-5473-4 | - | PE-54036 | PE-54036-S | - |
| L37 | 100 | 2.50 | 67144190 | - | RL-5472-1 | - | PE-54037 | PE-54037-S | - |
| L38 | 68 | 3.10 | 67144200 | - | RL-5472-2 | - | PE-54038 | PE-54038-S | - |
| L39 | 47 | 3.50 | 67144210 | - | RL-5472-3 | - | PE-54039 | PE-54039-S | - |
| L40 | 33 | 3.50 | 67144220 | 67148290 | RL-5472-4 | - | PE-54040 | PE-54040-S | - |
| L41 | 22 | 3.50 | 67144230 | 67148300 | RL-5472-5 | - | PE-54041 | PE-54041-S | - |
| L42 | 150 | 2.70 | 67148410 | - | RL-5473-4 | - | PE-54042 | PE-54042-S | - |
| L43 | 100 | 3.40 | 67144240 | - | RL-5473-2 | - | PE-54043 |  | - |
| L44 | 68 | 3.40 | 67144250 | - | RL-5473-3 | - | PE-54044 |  | - |
| FIGURE 9. Inductor Manufacturers Part Numbers |  |  |  |  |  |  |  |  |  |

## LM2596 Series Buck Regulator Design Procedure (Continued)

| Coilcraft Inc. | Phone | $(800) 322-2645$ |
| :--- | :--- | :--- |
|  | FAX | $(708) 639-1469$ |
| Coilcraft Inc., Europe | Phone | +111236730595 |
|  | FAX | +441236730627 |
| Pulse Engineering Inc. | Phone | $(619) 674-8100$ |
|  | FAX | $(619) 674-8262$ |
| Pulse Engineering Inc., <br> Europe | Phone | +3539324107 |
|  | FAX | +3539324459 |
| Renco Electronics Inc. | Phone | $(800) 645-5828$ |
|  | FAX | $(516) 586-5562$ |
| Schott Corp. | Phone | $(612) 475-1173$ |
|  | FAX | $(612) 475-1786$ |


| Nichicon Corp. | Phone | (708) 843-7500 |
| :--- | :--- | :--- |
|  | FAX | $(708) 843-2798$ |
| Panasonic | Phone | $(714) 373-7857$ |
|  | FAX | $(714) 373-7102$ |
| AVX Corp. | Phone | $(803) 448-9411$ |
|  | FAX | $(803) 448-1943$ |
| Sprague/Vishay | Phone | $(207) 324-4140$ |
|  | FAX | $(207) 324-7223$ |

FIGURE 11. Capacitor Manufacturers Phone Numbers

FIGURE 10. Inductor Manufacturers Phone Numbers


FIGURE 12. Diode Selection Table

## Application Information

## PIN FUNCTIONS

$+\mathbf{V}_{\text {IN }}$-This is the positive input supply for the IC switching regulator. A suitable input bypass capacitor must be present at this pin to minimize voltage transients and to supply the switching currents needed by the regulator.

## Ground-Circuit ground.

Output-Internal switch. The voltage at this pin switches between ( $+\mathrm{V}_{\mathrm{IN}}-\mathrm{V}_{\mathrm{SAT}}$ ) and approximately -0.5 V , with a duty cycle of approximately $\mathrm{V}_{\mathrm{OUT}} / \mathrm{V}_{\text {IN }}$. To minimize coupling to sensitive circuitry, the PC board copper area connected to this pin should be kept to a minimum.
Feedback-Senses the regulated output voltage to complete the feedback loop.
$\overline{\mathbf{O N}} / \mathbf{O F F}$ —Allows the switching regulator circuit to be shut down using logic level signals thus dropping the total input supply current to approximately $80 \mu \mathrm{~A}$. Pulling this pin below a threshold voltage of approximately 1.3 V turns the regulator on, and pulling this pin above 1.3 V (up to a maximum of 25 V ) shuts the regulator down. If this shutdown feature is not needed, the ON/OFF pin can be wired to the ground pin or it can be left open, in either case the regulator will be in the ON condition.

## EXTERNAL COMPONENTS

INPUT CAPACITOR
$\mathbf{C}_{\text {IN }}$-A low ESR aluminum or tantalum bypass capacitor is needed between the input pin and ground pin. It must be located near the regulator using short leads. This capacitor prevents large voltage transients from appearing at the input, and provides the instantaneous current needed each time the switch turns on.
The important parameters for the Input capacitor are the voltage rating and the RMS current rating. Because of the relatively high RMS currents flowing in a buck regulator's input capacitor, this capacitor should be chosen for its RMS current rating rather than its capacitance or voltage ratings, although the capacitance value and voltage rating are directly related to the RMS current rating.
The RMS current rating of a capacitor could be viewed as a capacitor's power rating. The RMS current flowing through the capacitors internal ESR produces power which causes the internal temperature of the capacitor to rise. The RMS current rating of a capacitor is determined by the amount of current required to raise the internal temperature approximately $10^{\circ} \mathrm{C}$ above an ambient temperature of $105^{\circ} \mathrm{C}$. The ability of the capacitor to dissipate this heat to the surrounding air will determine the amount of current the capacitor can safely sustain. Capacitors that are physically large and have a large surface area will typically have higher RMS current ratings. For a given capacitor value, a higher voltage electrolytic capacitor will be physically larger than a lower
voltage capacitor, and thus be able to dissipate more heat to the surrounding air, and therefore will have a higher RMS current rating.
The consequences of operating an electrolytic capacitor above the RMS current rating is a shortened operating life. The higher temperature speeds up the evaporation of the capacitor's electrolyte, resulting in eventual failure.
Selecting an input capacitor requires consulting the manufacturers data sheet for maximum allowable RMS ripple current. For a maximum ambient temperature of $40^{\circ} \mathrm{C}$, a general guideline would be to select a capacitor with a ripple current rating of approximately $50 \%$ of the DC load current. For ambient temperatures up to $70^{\circ} \mathrm{C}$, a current rating of $75 \%$ of the DC load current would be a good choice for a conservative design. The capacitor voltage rating must be at least 1.25 times greater than the maximum input voltage, and often a much higher voltage capacitor is needed to satisfy the RMS current requirements.
A graph shown in Figure 13 shows the relationship between an electrolytic capacitor value, its voltage rating, and the RMS current it is rated for. These curves were obtained from the Nichicon "PL" series of low ESR, high reliability electrolytic capacitors designed for switching regulator applications. Other capacitor manufacturers offer similar types of capacitors, but always check the capacitor data sheet.
"Standard" electrolytic capacitors typically have much higher ESR numbers, lower RMS current ratings and typically have a shorter operating lifetime.
Because of their small size and excellent performance, surface mount solid tantalum capacitors are often used for input bypassing, but several precautions must be observed. A small percentage of solid tantalum capacitors can short if the inrush current rating is exceeded. This can happen at turn on when the input voltage is suddenly applied, and of course, higher input voltages produce higher inrush currents. Several capacitor manufacturers do a $100 \%$ surge current testing on their products to minimize this potential problem. If high turn on currents are expected, it may be necessary to limit this current by adding either some resistance or inductance before the tantalum capacitor, or select a higher voltage capacitor. As with aluminum electrolytic capacitors, the RMS ripple current rating must be sized to the load current.

## FEEDFORWARD CAPACITOR

## (Adjustable Output Voltage Version)

$\mathrm{C}_{\mathrm{FF}}$-A Feedforward Capacitor $\mathrm{C}_{\mathrm{FF}}$, shown across R2 in Figure 2 is used when the ouput voltage is greater than 10 V or when Cout $_{\text {O }}$ has a very low ESR. This capacitor adds lead compensation to the feedback loop and increases the phase margin for better loop stability. For CFF selection, see the design procedure section.

## Application Information (Continued)



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## FIGURE 13. RMS Current Ratings for Low ESR Electrolytic Capacitors (Typical)

## OUTPUT CAPACITOR

Cout-An output capacitor is required to filter the output and provide regulator loop stability. Low impedance or low ESR Electrolytic or solid tantalum capacitors designed for switching regulator applications must be used. When selecting an output capacitor, the important capacitor parameters are; the 100 kHz Equivalent Series Resistance (ESR), the RMS ripple current rating, voltage rating, and capacitance value. For the output capacitor, the ESR value is the most important parameter.
The output capacitor requires an ESR value that has an upper and lower limit. For low output ripple voltage, a low ESR value is needed. This value is determined by the maximum allowable output ripple voltage, typically $1 \%$ to $2 \%$ of the output voltage. But if the selected capacitor's ESR is extremely low, there is a possibility of an unstable feedback loop, resulting in an oscillation at the output. Using the capacitors listed in the tables, or similar types, will provide design solutions under all conditions.
If very low output ripple voltage (less than 15 mV ) is required, refer to the section on Output Voltage Ripple and Transients for a post ripple filter.
An aluminum electrolytic capacitor's ESR value is related to the capacitance value and its voltage rating. In most cases, higher voltage electrolytic capacitors have lower ESR values (see Figure 14). Often, capacitors with much higher voltage ratings may be needed to provide the low ESR values required for low output ripple voltage.
The output capacitor for many different switcher designs often can be satisfied with only three or four different capacitor values and several different voltage ratings. See the quick design component selection tables in Figures 3 and 4 for typical capacitor values, voltage ratings, and manufacturers capacitor types.
Electrolytic capacitors are not recommended for temperatures below $-25^{\circ} \mathrm{C}$. The ESR rises dramatically at cold temperatures and typically rises 3 X @ $-25^{\circ} \mathrm{C}$ and as much as 10 X at $-40^{\circ} \mathrm{C}$. See curve shown in Figure 15.
Solid tantalum capacitors have a much better ESR spec for cold temperatures and are recommended for temperatures below $-25^{\circ} \mathrm{C}$.


TL/H/12583-29
FIGURE 14. Capacitor ESR vs Capacitor Voltage Rating (Typical Low ESR Electrolytic Capacitor)

## CATCH DIODE

Buck regulators require a diode to provide a return path for the inductor current when the switch turns off. This must be a fast diode and must be located close to the LM2596 using short leads and short printed circuit traces.
Because of their very fast switching speed and low forward voltage drop, Schottky diodes provide the best performance, especially in low output voltage applications ( 5 V and lower). Ultra-fast recovery, or High-Efficiency rectifiers are also a good choice, but some types with an abrupt turnoff characteristic may cause instability or EMI problems. Ultrafast recovery diodes typically have reverse recovery times of 50 ns or less. Rectifiers such as the 1N5400 series are much too slow and should not be used.


TL/H/12583-30
FIGURE 15. Capacitor ESR Change vs Temperature

## INDUCTOR SELECTION

All switching regulators have two basic modes of operation; continuous and discontinuous. The difference between the two types relates to the inductor current, whether it is flowing continuously, or if it drops to zero for a period of time in the normal switching cycle. Each mode has distinctively different operating characteristics, which can affect the regulators performance and requirements. Most switcher designs will operate in the discontinuous mode when the load current is low.
The LM2596 (or any of the Simple Switcher family) can be used for both continuous or discontinuous modes of operation.

## Application Information (Continued)

In many cases the preferred mode of operation is the continuous mode. It offers greater output power, lower peak switch, inductor and diode currents, and can have lower output ripple voltage. But it does require larger inductor values to keep the inductor current flowing continuously, especially at low output load currents and/or high input voltages.
To simplify the inductor selection process, an inductor selection guide (nomograph) was designed (see Figures 5 through 8). This guide assumes that the regulator is operating in the continuous mode, and selects an inductor that will allow a peak-to-peak inductor ripple current to be a certain percentage of the maximum design load current. This peak-to-peak inductor ripple current percentage is not fixed, but is allowed to change as different design load currents are selected. (See Figure 16.)


TL/H/12583-31
FIGURE 16. ( $\Delta \|_{\text {IND }}$ ) Peak-to-Peak Inductor Ripple Current (as a Percentage of the Load Current) vs Load Current

By allowing the percentage of inductor ripple current to increase for low load currents, the inductor value and size can be kept relatively low.
When operating in the continuous mode, the inductor current waveform ranges from a triangular to a sawtooth type of waveform (depending on the input voltage), with the average value of this current waveform equal to the DC output load current.
Inductors are available in different styles such as pot core, toroid, E-core, bobbin core, etc., as well as different core materials, such as ferrites and powdered iron. The least expensive, the bobbin, rod or stick core, consists of wire wound on a ferrite bobbin. This type of construction makes for an inexpensive inductor, but since the magnetic flux is not completely contained within the core, it generates more Electro-Magnetic Interference (EMI). This magnetic flux can induce voltages into nearby printed circuit traces, thus causing problems with both the switching regulator operation and nearby sensitive circuitry, and can give incorrect scope readings because of induced voltages in the scope probe. Also see section on Open Core Inductors.
When multiple switching regulators are located on the same PC board, open core magnetics can cause interference between two or more of the regulator circuits, especially at high currents. A torroid or E-core inductor (closed magnetic structure) should be used in these situations.
The inductors listed in the selection chart include ferrite E-core construction for Schott, ferrite bobbin core for Renco and Coilcraft, and powdered iron toroid for Pulse Engineering.

Exceeding an inductor's maximum current rating may cause the inductor to overheat because of the copper wire losses, or the core may saturate. If the inductor begins to saturate, the inductance decreases rapidly and the inductor begins to look mainly resistive (the DC resistance of the winding). This can cause the switch current to rise very rapidly and force the switch into a cycle-by-cycle current limit, thus reducing the DC output load current. This can also result in overheating of the inductor and/or the LM2596. Different inductor types have different saturation characteristics, and this should be kept in mind when selecting an inductor.
The inductor manufacturer's data sheets include current and energy limits to avoid inductor saturation.

## DISCONTINUOUS MODE OPERATION

The selection guide chooses inductor values suitable for continuous mode operation, but for low current applications and/or high input voltages, a discontinuous mode design may be a better choice. It would use an inductor that would be physically smaller, and would need only one half to one third the inductance value needed for a continuous mode design. The peak switch and inductor currents will be higher in a discontinuous design, but at these low load currents (1A and below), the maximum switch current will still be less than the switch current limit.
Discontinuous operation can have voltage waveforms that are considerable different than a continuous design. The output pin (switch) waveform can have some damped sinusoidal ringing present. (See Figure 1 photo titled; Discontinuous Mode Switching Waveforms) This ringing is normal for discontinuous operation, and is not caused by feedback loop instabilities. In discontinuous operation, there is a period of time where neither the switch or the diode are conducting, and the inductor current has dropped to zero. During this time, a small amount of energy can circulate between the inductor and the switch/diode parasitic capacitance causing this characteristic ringing. Normally this ringing is not a problem, unless the amplitude becomes great enough to exceed the input voltage, and even then, there is very little energy present to cause damage.
Different inductor types and/or core materials produce different amounts of this characteristic ringing. Ferrite core inductors have very little core loss and therefore produce the most ringing. The higher core loss of powdered iron inductors produce less ringing. If desired, a series RC could be placed in parallel with the inductor to dampen the ringing. The computer aided design software Switchers Made Simple (version 4.3) will provide all component values for continuous and discontinuous modes of operation.


TL/H/12583-32
FIGURE 17. Post Ripple Filter Waveform

## Application Information (Continued)

## OUTPUT VOLTAGE RIPPLE AND TRANSIENTS

The output voltage of a switching power supply operating in the continuous mode will contain a sawtooth ripple voltage at the switcher frequency, and may also contain short voltage spikes at the peaks of the sawtooth waveform.
The output ripple voltage is a function of the inductor sawtooth ripple current and the ESR of the output capacitor. A typical output ripple voltage can range from approximately $0.5 \%$ to $3 \%$ of the output voltage. To obtain low ripple voltage, the ESR of the output capacitor must be low, however, caution must be exercised when using extremely low ESR capacitors because they can affect the loop stability, resulting in oscillation problems. If very low output ripple voltage is needed (less than 20 mV ), a post ripple filter is recommended. (See Figure 2.) The inductance required is typically between $1 \mu \mathrm{H}$ and $5 \mu \mathrm{H}$, with low DC resistance, to maintain good load regulation. A low ESR output filter capacitor is also required to assure good dynamic load response and ripple reduction. The ESR of this capacitor may be as low as desired, because it is out of the regulator feedback loop. The photo shown in Figure 17 shows a typical output ripple voltage, with and without a post ripple filter.
When observing output ripple with a scope, it is essential that a short, low inductance scope probe ground connection be used. Most scope probe manufacturers provide a special probe terminator which is soldered onto the regulator board, preferable at the output capacitor. This provides a very short scope ground thus eliminating the problems associated with the 3 inch ground lead normally provided with the probe, and provides a much cleaner and more accurate picture of the ripple voltage waveform.
The voltage spikes are caused by the fast switching action of the output switch and the diode, and the parasitic inductance of the output filter capacitor, and its associated wiring. To minimize these voltage spikes, the output capacitor should be designed for switching regulator applications, and the lead lengths must be kept very short. Wiring inductance, stray capacitance, as well as the scope probe used to evaluate these transients, all contribute to the amplitude of these spikes.
When a switching regulator is operating in the continuous mode, the inductor current waveform ranges from a triangular to a sawtooth type of waveform (depending on the input voltage). For a given input and output voltage, the peak-topeak amplitude of this inductor current waveform remains constant. As the load current increases or decreases, the entire sawtooth current waveform also rises and falls. The average value (or the center) of this current waveform is equal to the DC load current.
If the load current drops to a low enough level, the bottom of the sawtooth current waveform will reach zero, and the switcher will smoothly change from a continuous to a discontinuous mode of operation. Most switcher designs (irregardless how large the inductor value is) will be forced to run discontinuous if the output is lightly loaded. This is a perfectly acceptable mode of operation.


FIGURE 18. Peak-to-Peak Inductor Ripple Current vs Load Current

In a switching regulator design, knowing the value of the peak-to-peak inductor ripple current ( $\Delta \mathrm{I}_{\mathrm{IND}}$ ) can be useful for determining a number of other circuit parameters. Parameters such as, peak inductor or peak switch current, minimum load current before the circuit becomes discontinuous, output ripple voltage and output capacitor ESR can all be calculated from the peak-to-peak $\Delta I_{I N D}$. When the inductor nomographs shown in Figures 5 through 8 are used to select an inductor value, the peak-to-peak inductor ripple current can immediately be determined. The curve shown in Figure 18 shows the range of ( $\Delta I_{I N D}$ ) that can be expected for different load currents. The curve also shows how the peak-to-peak inductor ripple current ( $\Delta_{l_{\mathrm{IND}}}$ ) changes as you go from the lower border to the upper border (for a given load current) within an inductance region. The upper border represents a higher input voltage, while the lower border represents a lower input voltage (see Inductor Selection Guides).
These curves are only correct for continuous mode operation, and only if the inductor selection guides are used to select the inductor value

## Consider the following example:

$\mathrm{V}_{\text {OUT }}=5 \mathrm{~V}$, maximum load current of 2.5 A
$\mathrm{V}_{\mathrm{IN}}=12 \mathrm{~V}$, nominal, varying between 10 V and 16 V .
The selection guide in Figure 6 shows that the vertical line for a 2.5A load current, and the horizontal line for the 12 V input voltage intersect approximately midway between the upper and lower borders of the $33 \mu \mathrm{H}$ inductance region. A $33 \mu \mathrm{H}$ inductor will allow a peak-to-peak inductor current ( $\Delta l_{\mathrm{IND}}$ ) to flow that will be a percentage of the maximum load current. Referring to Figure 18, follow the 2.5A line approximately midway into the inductance region, and read the peak-to-peak inductor ripple current ( $\Delta l_{\mathrm{IND}}$ ) on the left hand axis (approximately $620 \mathrm{~mA} p-\mathrm{p}$ ).
As the input voltage increases to 16 V , it approaches the upper border of the inductance region, and the inductor ripple current increases. Referring to the curve in Figure 18, it can be seen that for a load current of 2.5 A , the peak-topeak inductor ripple current ( $\Delta l_{\mathrm{IND}}$ ) is 620 mA with 12 V in, and can range from 740 mA at the upper border ( 16 V in) to 500 mA at the lower border ( 10 V in).

## Application Information (Continued)

Once the $\Delta_{\text {IND }}$ value is known, the following formulas can be used to calculate additional information about the switching regulator circuit.

1. Peak Inductor or peak switch current

$$
=\left(\mathrm{I}_{\mathrm{LOAD}}+\frac{\Delta \mathrm{l}_{\mathrm{IND}}}{2}\right)=\left(2.5 \mathrm{~A}+\frac{0.62}{2}\right)=2.81 \mathrm{~A}
$$

2. Minimum load current before the circuit becomes discontinuous

$$
=\frac{\Delta l_{\mathrm{IND}}}{2}=\frac{0.62}{2}=0.31 \mathrm{~A}
$$

3. Output Ripple Voltage $=\left(\Delta I_{\text {IND }}\right) \times\left(\right.$ ESR of $\left.\mathrm{C}_{\text {OUT }}\right)$

$$
=0.62 \mathrm{~A} \times 0.1 \Omega=62 \mathrm{mV} \text { p-p }
$$

or


## OPEN CORE INDUCTORS

Another possible source of increased output ripple voltage or unstable operation is from an open core inductor. Ferrite bobbin or stick inductors have magnetic lines of flux flowing through the air from one end of the bobbin to the other end. These magnetic lines of flux will induce a voltage into any wire or PC board copper trace that comes within the inductor's magnetic field. The strength of the magnetic field, the orientation and location of the PC copper trace to the magnetic field, and the distance between the copper trace and the inductor, determine the amount of voltage generated in the copper trace. Another way of looking at this inductive coupling is to consider the PC board copper trace as one turn of a transformer (secondary) with the inductor winding as the primary. Many millivolts can be generated in a copper trace located near an open core inductor which can cause stability problems or high output ripple voltage problems.
If unstable operation is seen, and an open core inductor is used, it's possible that the location of the inductor with respect to other PC traces may be the problem. To determine if this is the problem, temporarily raise the inductor away from the board by several inches and then check circuit operation. If the circuit now operates correctly, then the magnetic flux from the open core inductor is causing the problem. Substituting a closed core inductor such as a torroid or E-core will correct the problem, or re-arranging the PC layout may be necessary. Magnetic flux cutting the IC device ground trace, feedback trace, or the positive or negative traces of the output capacitor should be minimized.
Sometimes, locating a trace directly beneath a bobbin inductor will provide good results, provided it is exactly in the center of the inductor (because the induced voltages cancel themselves out), but if it is off center one direction or the other, then problems could arise. If flux problems are present, even the direction of the inductor winding can make a difference in some circuits.
This discussion on open core inductors is not to frighten the user, but to alert the user on what kind of problems to watch out for when using them. Open core bobbin or "stick" inductors are an inexpensive, simple way of making a compact efficient inductor, and they are used by the millions in many different applications.

## THERMAL CONSIDERATIONS

The LM2596 is available in two packages, a 5 -pin TO-220 (T) and a 5-pin surface mount TO-263 (S).

The TO-220 package needs a heat sink under most conditions. The size of the heatsink depends on the input voltage, the output voltage, the load current and the ambient temperature. The curves in Figure 19 show the LM2596T junction temperature rises above ambient temperature for a 3 A load and different input and output voltages. The data for these curves was taken with the LM2596T (TO-220 package) operating as a buck switching regulator in an ambient temperature of $25^{\circ} \mathrm{C}$ (still air). These temperature rise numbers are all approximate and there are many factors that can affect these temperatures. Higher ambient temperatures require more heat sinking.
The TO-263 surface mount package tab is designed to be soldered to the copper on a printed circuit board. The copper and the board are the heat sink for this package and the other heat producing components, such as the catch diode and inductor. The PC board copper area that the package is soldered to should be at least $0.4 \mathrm{in}^{2}$, and ideally should have 2 or more square inches of 2 oz . ( 0.0028 ) in) copper. Additional copper area improves the thermal characteristics, but with copper areas greater than approximately 6 in 2 , only small improvements in heat dissipation are realized. If further thermal improvements are needed, double sided, multilayer PC board with large copper areas and/or airflow are recommended.
The curves shown in Figure 20 show the LM2596S (TO-263 package) junction temperature rise above ambient temperature with a 2A load for various input and output voltages. This data was taken with the circuit operating as a buck switching regulator with all components mounted on a PC board to simulate the junction temperature under actual operating conditions. This curve can be used for a quick check for the approximate junction temperature for various conditions, but be aware that there are many factors that can affect the junction temperature. When load currents higher than 2A are used, double sided or multilayer PC boards with large copper areas and/or airflow might be needed, especially for high ambient temperatures and high output voltages.
For the best thermal performance, wide copper traces and generous amounts of printed circuit board copper should be used in the board layout. (One exception to this is the output (switch) pin, which should not have large areas of copper.) Large areas of copper provide the best transfer of heat (lower thermal resistance) to the surrounding air, and moving air lowers the thermal resistance even further.
Package thermal resistance and junction temperature rise numbers are all approximate, and there are many factors that will affect these numbers. Some of these factors include board size, shape, thickness, position, location, and even board temperature. Other factors are, trace width, total printed circuit copper area, copper thickness, single- or dou-ble-sided, multilayer board and the amount of solder on the board. The effectiveness of the PC board to dissipate heat also depends on the size, quantity and spacing of other components on the board, as well as whether the surrounding air is still or moving. Furthermore, some of these components such as the catch diode will add heat to the PC board and the heat can vary as the input voltage changes. For the inductor, depending on the physical size, type of core material and the DC resistance, it could either act as a heat sink taking heat away from the board, or it could add heat to the board.

## Application Information (Continued)



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| Circuit Data for Temperature Rise Curve <br> TO-220 Package (T) |  |
| :--- | :--- |
| Capacitors | Through hole electrolytic |
| Inductor | Through hole, Renco |
| Diode | Through hole, 5A 40V, Schottky |
| PC board | 3 square inches single sided 2 oz. copper <br> $\left(0.0028^{\prime \prime}\right)$ |

FIGURE 19. Junction Temperature Rise, TO-220


TL/H/12583-35

| Circuit Data for Temperature Rise Curve <br> TO-263 Package (S) |  |
| :--- | :--- |
| Capacitors | Surface mount tantalum, molded "D" size |
| Inductor | Surface mount, Pulse Engineering, $68 \mu \mathrm{H}$ |
| Diode | Surface mount, 5A 40V, Schottky |
| PC board | 9 square inches single sided 2 oz. copper <br> $(0.0028 ")$ |

FIGURE 20. Junction Temperature Rise, TO-263


TL/H/12583-36
FIGURE 21. Delayed Startup


FIGURE 22. Undervoltage Lockout for Buck Regulator

## DELAYED STARTUP

The circuit in Figure 21 uses the the $\overline{O N} / O F F$ pin to provide a time delay between the time the input voltage is applied and the time the output voltage comes up (only the circuitry pertaining to the delayed start up is shown). As the input voltage rises, the charging of capacitor C1 pulls the $\overline{\mathrm{ON}} / \mathrm{OFF}$ pin high, keeping the regulator off. Once the input voltage reaches its final value and the capacitor stops charging, and resistor $R_{2}$ pulls the $\overline{O N}$ /OFF pin low, thus allowing the circuit to start switching. Resistor $R_{1}$ is included to limit the maximum voltage applied to the $\overline{O N} / O F F$ pin (maximum of 25 V ), reduces power supply noise sensitivity, and also limits the capacitor, C1, discharge current. When high input ripple voltage exists, avoid long delay time, because this ripple can be coupled into the ON/OFF pin and cause problems.
This delayed startup feature is useful in situations where the input power source is limited in the amount of current it can deliver. It allows the input voltage to rise to a higher voltage before the regulator starts operating. Buck regulators require less input current at higher input voltages.

## UNDERVOLTAGE LOCKOUT

Some applications require the regulator to remain off until the input voltage reaches a predetermined voltage. An undervoltage lockout feature applied to a buck regulator is shown in Figure 22, while Figures 23 and 24 applies the same feature to an inverting circuit. The circuit in Figure 23 features a constant threshold voltage for turn on and turn off (zener voltage plus approximately one volt). If hysteresis is needed, the circuit in Figure 24 has a turn ON voltage which is different than the turn OFF voltage. The amount of hysteresis is approximately equal to the value of the output voltage. If zener voltages greater than 25 V are used, an additional $47 \mathrm{k} \Omega$ resistor is needed from the $\overline{\mathrm{ON}} / \mathrm{OFF}$ pin to the ground pin to stay within the 25 V maximum limit of the ON/OFF pin.

## Application Information (Continued) <br> INVERTING REGULATOR

The circuit in Figure 25 converts a positive input voltage to a negative output voltage with a common ground. The circuit operates by bootstrapping the regulator's ground pin to the negative output voltage, then grounding the feedback pin, the regulator senses the inverted output voltage and regulates it.


This circuit has an ON/OFF threshold of approximately 13 V . FIGURE 23. Undervoltage Lockout for Inverting Regulator

$$
\log \log \log
$$

This example uses the LM2596-5.0 to generate a -5 V output, but other output voltages are possible by selecting other output voltage versions, including the adjustable version. Since this regulator topology can produce an output voltage that is either greater than or less than the input voltage, the maximum output current greatly depends on both the input and output voltage. The curve shown in Figure 26 provides a guide as to the amount of output load current possible for the different input and output voltage conditions.
The maximum voltage appearing across the regulator is the absolute sum of the input and output voltage, and this must be limited to a maximum of 40 V . For example, when converting +20 V to -12 V , the regulator would see 32 V between the input pin and ground pin. The LM2596 has a maximum input voltage spec of 40 V .
Additional diodes are required in this regulator configuration. Diode D1 is used to isolate input voltage ripple or noise from coupling through the $\mathrm{C}_{\mathrm{IN}}$ capacitor to the output, under light or no load conditions. Also, this diode isolation changes the topology to closley resemble a buck configuration thus providing good closed loop stability. A Schottky diode is recommended for low input voltages, (because of its lower voltage drop) but for higher input voltages, a fast recovery diode could be used.
Without diode D3, when the input voltage is first applied, the charging current of $\mathrm{C}_{\mathrm{IN}}$ can pull the output positive by several volts for a short period of time. Adding D3 prevents the output from going positive by more than a diode voltage.


TL/H/12583-39
FIGURE 24. Undervoltage Lockout with Hysteresis for Inverting Regulator

$220 \mu$ F/25V Elec. Panasonic HFQ
FIGURE 25. Inverting - 5V Regulator with Delayed Startup

## Application Information (Continued)



TL/H/12583-41
FIGURE 26. Inverting Regulator Typical Load Current
Because of differences in the operation of the inverting regulator, the standard design procedure is not used to select the inductor value. In the majority of designs, a $33 \mu \mathrm{H}, 3.5 \mathrm{~A}$ inductor is the best choice. Capacitor selection can also be narrowed down to just a few values. Using the values shown in Figure 25 will provide good results in the majority of inverting designs.
This type of inverting regulator can require relatively large amounts of input current when starting up, even with light
loads. Input currents as high as the LM2596 current limit (approx 4.5A) are needed for at least 2 ms or more, until the output reaches its nominal output voltage. The actual time depends on the output voltage and the size of the output capacitor. Input power sources that are current limited or sources that can not deliver these currents without getting loaded down, may not work correctly. Because of the relatively high startup currents required by the inverting topology, the delayed startup feature ( $\mathrm{C} 1, \mathrm{R}_{1}$ and $\mathrm{R}_{2}$ ) shown in Figure 25 is recommended. By delaying the regulator startup, the input capacitor is allowed to charge up to a higher voltage before the switcher begins operating. A portion of the high input current needed for startup is now supplied by the input capacitor $\left(\mathrm{C}_{\mathrm{IN}}\right)$. For severe start up conditions, the input capacitor can be made much larger than normal.

## INVERTING REGULATOR SHUTDOWN METHODS

To use the $\overline{\mathrm{ON}} /$ OFF pin in a standard buck configuration is simple, pull it below 1.3 V (@ $25^{\circ} \mathrm{C}$, referenced to ground) to turn regulator ON , pull it above 1.3 V to shut the regulator OFF. With the inverting configuration, some level shifting is required, because the ground pin of the regulator is no longer at ground, but is now setting at the negative output voltage level. Two different shutdown methods for inverting regulators are shown in Figures 27 and 28.


TL/H/12583-42
FIGURE 27. Inverting Regulator Ground Referenced Shutdown


TL/H/12583-43
FIGURE 28. Inverting Regulator Ground Referenced Shutdown using Opto Device

Application Information (Continued)
TYPICAL THROUGH HOLE PC BOARD LAYOUT, FIXED OUTPUT (1X SIZE), DOUBLE SIDED

$\mathrm{C}_{\text {IN }}-470 \mu \mathrm{~F}, 50 \mathrm{~V}$, Aluminum Electrolytic Panasonic, "HFQ Series"
COUT - $330 \mu \mathrm{~F}, 35 \mathrm{~V}$, Aluminum Electrolytic Panasonic, "HFQ Series"
D1 -5A, 40V Schottky Rectifier, 1N5825
L1 $-47 \mu \mathrm{H}$, L39, Renco, Through Hole
Thermalloy Heat Sink \#7020
TYPICAL THROUGH HOLE PC BOARD LAYOUT, ADJUSTABLE OUTPUT (1X SIZE), DOUBLE SIDED

Copper Side


Component Side


[^4]FIGURE 29. PC Board Layout


Physical Dimensions inches (millimeters)


5-Lead TO-220 (T)
Order Number LM2596T-3.3, LM2596T-5.0,
LM2596T-12 or LM2596T-ADJ
NS Package Number T05D


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| Qnational Semiconductor |  |
| :---: | :---: |
| LM2597 |  |
| SIMPLE SWITCHER ${ }^{\circledR}$ Power Converter 150 kHz 0.5A Step-Down Voltage Regulator, with Features |  |
| General Description |  |
| The LM2597 series of regulators are monoliticic integrated circuits that provide all the active functions for a step-down (buck) switching regulator, capable of driving a 0.5 A load with excellent line and load regulation. These devices are | by current. Self protection features include a two stage curent limit for the output switch and an over temperature shutdown for complete protection under fault conditions. |
|  | Features |
| 俍 |  |
| This series of switching reguiates is similar to the LM2594 | - $\pm 40$ max overs Ifine and load conditions |
| series, added. | - Guaranteed 0.5A output current |
| ming |  |
|  | - 150 kHz fixed frequency intemal oscillator |
|  | - |
|  |  |
| 1259 |  |
| 150 KHzz thus allowing smaller sized filter compon | - Bias Supply Pin (Vss) for internal circuitry improves effi- |
| what would be needed w with lower freauency switching regu- | ciency at high inut |
| lators. Because of its high efficiency, the copper traces on | - Low power standiby mode, la typically |
| rruit board are normaly the only heat sinking | - Highe Eficiency |
| A tandard series of inductors (bothtrough hole and sur- - Thermal shutdown and current linit protection |  |
|  |  |
|  |  |
| feature gsupplies. |  |
| Other features include a guaranted $44 \%$ \% Olerance on out. |  |
| put voltage under all conditions of input voltage and output oad conditions, and $\pm 15 \%$ on the oscillator frequency. Ex- |  |

## Typical Application (Fixed Output Voltage Versions)



[^5]
## Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required please contact the National Semiconductor Sales Office/Distributors for availability and specifications.
Maximum Supply Voltage ( $\mathrm{V}_{\mathrm{IN}}$ ) 45V
$\overline{\mathrm{SD}} / \mathrm{SS}$ Pin Input Voltage (Note 2) 6V

Delay Pin Voltage (Note 2) 1.5V
Flag Pin Voltage $\quad-0.3 \leq \mathrm{V} \leq 45 \mathrm{~V}$
Bias Supply Voltage ( $\mathrm{V}_{\mathrm{BS}}$ ) $\quad-0.3 \leq \mathrm{V} \leq 30 \mathrm{~V}$
Feedback Pin Voltage $\quad-0.3 \leq \mathrm{V} \leq+25 \mathrm{~V}$
Output Voltage to Ground (Steady State) -1V
Power Dissipation Internally limited
Storage Temperature Range $\quad-65^{\circ} \mathrm{C}$ to $+150^{\circ} \mathrm{C}$
ESD Susceptibility
Human Body Model (Note 3) 2 kV

| Lead Temperature |  |
| :--- | :--- |
| M8 Package |  |
| $\quad$ Vapor Phase $(60$ sec.) | $+215^{\circ} \mathrm{C}$ |
| $\quad$ Infrared (15 sec.) | $+220^{\circ} \mathrm{C}$ |
| N Package (Soldering, 10 sec.) | $+260^{\circ} \mathrm{C}$ |
| Maximum Junction Temperature | $+150^{\circ} \mathrm{C}$ |

Operating Conditions
Temperature Range $\quad-40^{\circ} \mathrm{C} \leq \mathrm{T}_{\mathrm{J}}+125^{\circ} \mathrm{C}$

Supply Voltage 4.5 V to 40 V

## LM2597-3.3

Electrical Characteristics Specifications with standard type face are for $\mathrm{T}_{\mathrm{J}}=25^{\circ} \mathrm{C}$, and those with boldface type apply over full Operating Temperature Range.

| Symbol | Parameter | Conditions | LM2597-3.3 |  | Units(Limits) |
| :---: | :---: | :---: | :---: | :---: | :---: |
|  |  |  | Typ <br> (Note 4) | Limit (Note 5) |  |
| SYSTEM PARAMETERS (Note 6) Test Circuit Figure 12 |  |  |  |  |  |
| $\mathrm{V}_{\text {OUT }}$ | Output Voltage | $4.75 \mathrm{~V} \leq \mathrm{V}_{\text {IN }} \leq 40 \mathrm{~V}, 0.1 \mathrm{~A} \leq \mathrm{I}_{\text {LOAD }} \leq 0.5 \mathrm{~A}$ | 3.3 | $\begin{aligned} & 3.168 / \mathbf{3 . 1 3 5} \\ & 3.432 / \mathbf{3 . 4 6 5} \end{aligned}$ | V (min) <br> $V$ (max) |
| $\eta$ | Efficiency | $\mathrm{V}_{\mathrm{IN}}=12 \mathrm{~V}, \mathrm{I}_{\text {LOAD }}=0.5 \mathrm{~A}$ | 80 |  | \% |

LM2597-5.0
Electrical Characteristics Specifications with standard type face are for $\mathrm{T}_{\mathrm{J}}=25^{\circ} \mathrm{C}$, and those with boldface type apply over full Operating Temperature Range.

| Symbol | Parameter | Conditions | LM2597-5.0 |  | Units(Limits) |
| :---: | :---: | :---: | :---: | :---: | :---: |
|  |  |  | $\begin{gathered} \text { Typ } \\ \text { (Note 4) } \end{gathered}$ | Limit (Note 5) |  |
| SYSTEM PARAMETERS (Note 6) Test Circuit Figure 12 |  |  |  |  |  |
| $\mathrm{V}_{\text {OUT }}$ | Output Voltage | $7 \mathrm{~V} \leq \mathrm{V}_{\text {IN }} \leq 40 \mathrm{~V}, 0.1 \mathrm{~A} \leq \mathrm{I}_{\text {LOAD }} \leq 0.5 \mathrm{~A}$ | 5 | $\begin{aligned} & 4.800 / 4.750 \\ & 5.200 / 5.250 \end{aligned}$ |  |
| $\eta$ | Efficiency | $\mathrm{V}_{\mathrm{IN}}=12 \mathrm{~V}, \mathrm{I}_{\text {LOAD }}=0.5 \mathrm{~A}$ | 82 |  | \% |

LM2597-12
Electrical Characteristics Specifications with standard type face are for $\mathrm{T}_{\mathrm{J}}=25^{\circ} \mathrm{C}$, and those with boldface type apply over full Operating Temperature Range.

| Symbol | Parameter | Conditions | LM2597-12 |  | Units (Limits) |
| :---: | :---: | :---: | :---: | :---: | :---: |
|  |  |  | Typ <br> (Note 4) | Limit (Note 5) |  |
| SYSTEM PARAMETERS (Note 6) Test Circuit Figure 12 |  |  |  |  |  |
| V OUT | Output Voltage | $15 \mathrm{~V} \leq \mathrm{V}_{\text {IN }} \leq 40 \mathrm{~V}, 0.1 \mathrm{~A} \leq \mathrm{I}_{\text {LOAD }} \leq 0.5 \mathrm{~A}$ | 12 | $\begin{aligned} & 11.52 / \mathbf{1 1 . 4 0} \\ & 12.48 / \mathbf{1 2 . 6 0} \end{aligned}$ |  |
| $\eta$ | Efficiency | $\mathrm{V}_{\mathrm{IN}}=25 \mathrm{~V}, \mathrm{I}_{\text {LOAD }}=0.5 \mathrm{~A}$ | 88 |  | \% |


| Electrical Characteristics Specifications with standard type face are for $\mathrm{T}_{\mathrm{J}}=25^{\circ} \mathrm{C}$, and those with boldface type apply over full Operating Temperature Range. |  |  |  |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: |
|  |  |  |  | 997-ADJ |  |
| Symbol | Parameter | Conditions | $\begin{gathered} \text { Typ } \\ \text { (Note 4) } \end{gathered}$ | $\begin{aligned} & \text { Limit } \\ & \text { (Note 5) } \end{aligned}$ | (Limits) |
| SYSTEM PARAMETERS (Note 6) Test Circuit Figure 12 |  |  |  |  |  |
| $\mathrm{V}_{\text {FB }}$ | Feedback Voltage | $\begin{aligned} & 4.5 \mathrm{~V} \leq \mathrm{V}_{\mathrm{IN}} \leq 40 \mathrm{~V}, 0.1 \mathrm{~A} \leq \mathrm{I}_{\mathrm{LOAD}} \leq 0.5 \mathrm{~A} \\ & \mathrm{~V}_{\text {OUT }} \text { programmed for } 3 \mathrm{~V} \text {. Circuit of Figure } 12 . \end{aligned}$ | 1.230 | $\begin{aligned} & 1.193 / \mathbf{1 . 1 8 0} \\ & 1.267 / \mathbf{1 . 2 8 0} \end{aligned}$ | $\begin{gathered} \mathrm{V} \\ \mathrm{~V}(\min ) \\ \mathrm{V}(\max ) \end{gathered}$ |
| $\eta$ | Efficiency | $\mathrm{V}_{\text {IN }}=12 \mathrm{~V}, \mathrm{~V}_{\text {OUT }}=3 \mathrm{~V}, \mathrm{I}$ LOAD $=0.5 \mathrm{~A}$ | 80 |  | \% |

## All Output Voltage Versions

Electrical Characteristics Specifications with standard type face are for $T_{J}=25^{\circ} \mathrm{C}$, and those with boldface type apply over full Operating Temperature Range. Unless otherwise specified, $\mathrm{V}_{\mathrm{IN}}=12 \mathrm{~V}$ for the $3.3 \mathrm{~V}, 5 \mathrm{~V}$, and Adjustable version and $\mathrm{V}_{\mathrm{IN}}=24 \mathrm{~V}$ for the 12 V version. $\mathrm{I}_{\text {LOAD }}=100 \mathrm{~mA}$

| Symbol | Parameter | Conditions | LM2597-XX |  | Units <br> (Limits) |
| :---: | :---: | :---: | :---: | :---: | :---: |
|  |  |  | Typ (Note 4) | Limit (Note 5) |  |
| DEVICE PARAMETERS |  |  |  |  |  |
| $\mathrm{Ib}^{\text {b }}$ | Feedback Bias Current | Adjustable Version Only, $\mathrm{V}_{\mathrm{FB}}=1.235 \mathrm{~V}$ | 10 | 50/100 | nA |
| $\mathrm{fo}_{0}$ | Oscillator Frequency | (Note 7) | 150 | $\begin{array}{r} 127 / \mathbf{1 1 0} \\ 173 / 173 \\ \hline \end{array}$ | $\begin{gathered} \mathrm{kHz} \\ \mathrm{kHz}(\min ) \\ \mathrm{kHz}(\max ) \end{gathered}$ |
| $\mathrm{V}_{\text {SAT }}$ | Saturation Voltage | IOUT $=0.5 \mathrm{~A}($ Notes 8 and 9$)$ | 0.9 | 1.1/1.2 | $\stackrel{V}{V(\max )}$ |
| DC | Max Duty Cycle (ON) Min Duty Cycle (OFF) | (Note 9) (Note 10) | $\begin{gathered} 100 \\ 0 \end{gathered}$ |  | \% |
| ${ }^{\text {ICL }}$ | Current Limit | Peak Current, (Notes 8 and 9) | 0.8 | $\begin{gathered} 0.65 / \mathbf{0 . 5 8} \\ 1.3 / \mathbf{1 . 4} \\ \hline \end{gathered}$ | $\begin{gathered} A \\ A(\min ) \\ A(\max ) \\ \hline \end{gathered}$ |
| $\mathrm{I}_{\mathrm{L}}$ | Output Leakage Current | $\begin{array}{ll} (\text { Notes } 8,10 \text { and 11) } & \text { Output }=0 \mathrm{~V} \\ & \text { Output }=-1 \mathrm{~V} \end{array}$ | 2 | $\begin{aligned} & 50 \\ & 15 \end{aligned}$ | $\begin{gathered} \mu \mathrm{A}(\max ) \\ \mathrm{mA} \\ \mathrm{~mA}(\max ) \end{gathered}$ |
| $\mathrm{I}_{\mathrm{Q}}$ | Operating Quiescent Current | $\overline{\mathrm{SD}} / \mathrm{SS}$ Pin Open, $\mathrm{V}_{\mathrm{BS}}$ Pin Open (Note 10) | 5 | 10 | $\begin{gathered} \mathrm{mA} \\ \mathrm{~mA}(\mathrm{max}) \\ \hline \end{gathered}$ |
| IstBy | Standby Quiescent Current | $\overline{\mathrm{SD}} / \mathrm{SS}$ pin $=0 \mathrm{~V} \quad$ (Note 10) | 85 | 200/250 | $\begin{gathered} \mu \mathrm{A} \\ \mu \mathrm{~A}(\mathrm{max}) \\ \hline \end{gathered}$ |
| $\theta_{\text {JA }}$ | Thermal Resistance | N Package, Junction to Ambient (Note 12) M Package, Junction to Ambient (Note 12) | $\begin{gathered} 95 \\ 150 \end{gathered}$ |  | ${ }^{\circ} \mathrm{C} / \mathrm{W}$ |

## All Output Voltage Versions (Continued)

Electrical Characteristics Specifications with standard type face are for $\mathrm{T}_{\mathrm{J}}=25^{\circ} \mathrm{C}$, and those with boldface type apply over full Operating Temperature Range. Unless otherwise specified, $\mathrm{V}_{\mathrm{IN}}=12 \mathrm{~V}$ for the $3.3 \mathrm{~V}, 5 \mathrm{~V}$, and Adjustable version and $\mathrm{V}_{\mathrm{IN}}=24 \mathrm{~V}$ for the 12 V version. $\mathrm{I}_{\text {LOAD }}=100 \mathrm{~mA}$

| Symbol | Parameter | Conditions | LM2597-XX |  | Units (Limits) |
| :---: | :---: | :---: | :---: | :---: | :---: |
|  |  |  | Typ (Note 4) | Limit (Note 5) |  |
| SHUTDOWN/SOFT-START CONTROL Test Circuit of Figure 12 |  |  |  |  |  |
| $V_{S D}$ | Shutdown Threshold Voltage | Low, (Shutdown Mode) High, (Soft-start Mode) | 1.3 | $\begin{gathered} 0.6 \\ 2 \end{gathered}$ |  |
| $\mathrm{V}_{\text {SS }}$ | Soft-start Voltage | $\mathrm{V}_{\text {OUT }}=20 \%$ of Nominal Output Voltage <br> $\mathrm{V}_{\text {OUT }}=100 \%$ of Nominal Output Voltage | $\begin{aligned} & 2 \\ & 3 \end{aligned}$ |  | V |
| $I_{\text {SD }}$ | Shutdown Current | $\mathrm{V}_{\text {SHUTDOWN }}=0.5 \mathrm{~V}$ | 5 | 10 | $\begin{gathered} \mu \mathrm{A} \\ \mu \mathrm{~A}(\max ) \end{gathered}$ |
| Iss | Soft-start Current | $\mathrm{V}_{\text {Soft-start }}=2.5 \mathrm{~V}$ | 1.6 | 5 | $\begin{gathered} \mu \mathrm{A} \\ \mu \mathrm{~A}(\mathrm{max}) \end{gathered}$ |
| FLAG/DELAY CONTROL Test Circuit of Figure 12 |  |  |  |  |  |
|  | Regulator Dropout Detector Threshold Voltage | Low (Flag ON) | 96 | $\begin{aligned} & 92 \\ & 98 \end{aligned}$ |  |
| VF ${ }_{\text {SAT }}$ | Flag Output Saturation Voltage | $\begin{aligned} & I_{S I N K}=3 \mathrm{~mA} \\ & \mathrm{~V}_{\mathrm{DELAY}}=0.5 \mathrm{~V} \end{aligned}$ | 0.3 | 0.7/1.0 | $\begin{gathered} \mathrm{V} \\ \mathrm{~V}(\max ) \end{gathered}$ |
| $\mathrm{IF}_{\mathrm{L}}$ | Flag Output Leakage Current | $\mathrm{V}_{\mathrm{FLAG}}=40 \mathrm{~V}$ | 0.3 |  | $\mu \mathrm{A}$ |
|  | Delay Pin Threshold Voltage | Low (Flag ON) <br> High (Flag OFF) and $\mathrm{V}_{\text {OUT }}$ Regulated | 1.25 | $\begin{aligned} & 1.21 \\ & 1.29 \end{aligned}$ | $\begin{gathered} \mathrm{V} \\ \mathrm{~V}(\min ) \\ \mathrm{V}(\max ) \end{gathered}$ |
|  | Delay Pin Source Current | $\mathrm{V}_{\text {DELAY }}=0.5 \mathrm{~V}$ | 3 | 6 | $\begin{gathered} \mu \mathrm{A} \\ \mu \mathrm{~A}(\mathrm{max}) \\ \hline \end{gathered}$ |
|  | Delay Pin Saturation | Low (Flag ON) | 55 | 350/400 | $\begin{gathered} \mathrm{mV} \\ \mathrm{mV}(\max ) \end{gathered}$ |
| BIAS SUPPLY |  |  |  |  |  |
| $\mathrm{I}_{\mathrm{BS}}$ | Bias Supply Pin Current (OFF) | $\mathrm{V}_{\mathrm{BS}}=2 \mathrm{~V} \quad$ (Note 10) | 120 | 400 | $\begin{gathered} \mu \mathrm{A} \\ \mu \mathrm{~A}(\mathrm{max}) \end{gathered}$ |
|  | Bias Supply Pin Current (ON) | $\mathrm{V}_{\mathrm{BS}}=4.4 \mathrm{~V} \quad($ Note 10) | 4 | 10 | $\begin{gathered} \mathrm{mA} \\ \mathrm{~mA}(\mathrm{max}) \\ \hline \end{gathered}$ |
| $\mathrm{I}_{\mathrm{Q}}$ | Operating Quiescent Current | $\mathrm{V}_{\mathrm{BS}}=4.4 \mathrm{~V} \quad$ (Note 10) | 1 | 2 | mA |

## Electrical Characteristics (Continued)

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but do not guarantee specific performance limits. For guaranteed specifications and test conditions, see the Electrical Characteristics
Note 2: Voltage internally clamped. If clamp voltage is exceeded, limit current to a maximum of 1 mA .
Note 3: The human body model is a 100 pF capacitor discharged through a 1.5 k resistor into each pin.
Note 4: Typical numbers are at $25^{\circ} \mathrm{C}$ and represent the most likely norm.
Note 5: All limits guaranteed at room temperature (standard type face) and at temperature extremes (bold type face). All room temperature limits are 100\% production tested. All limits at temperature extremes are guaranteed via correlation using standard Statistical Quality Control (SQC) methods. All limits are used to calculate Average Outgoing Quality Level (AOQL).
Note 6: External components such as the catch diode, inductor, input and output capacitors can affect switching regulator system performance. When the LM2597 is used as shown in the Figure 12 test circuit, system performance will be as shown in system parameters section of Electrical Characteristics.
Note 7: The switching frequency is reduced when the second stage current limit is activated. The amount of reduction is determined by the severity of current overload.
Note 8: No diode, inductor or capacitor connected to output pin
Note 9: Feedback pin removed from output and connected to 0 V to force the output transistor switch ON.
Note 10: Feedback pin removed from output and connected to 12 V for the $3.3 \mathrm{~V}, 5 \mathrm{~V}$, and the ADJ. version, and 15 V for the 12 V version, to force the output transistor switch OFF.
Note 11: $\mathrm{V}_{\mathrm{IN}}=40 \mathrm{~V}$.
Note 12: Junction to ambient thermal resistance with approximately 1 square inch of printed circuit board copper surrounding the leads. Additional copper area will lower thermal resistance further. See application hints in this data sheet and the thermal model in Switchers Made Simple ${ }^{\circledR}$ software
Typical Performance Characteristics (Circuit of Figure 12)

Normalized
Output Voltage


Switch Saturation
Voltage


Line Regulation


TL/H/12440-3

Switch Current Limit


Efficiency


Typical Performance Characteristics (Circuit of Figure 12 ) (Continued)






Typical Performance Characteristics (Circuit of Figure 12)

Continuous Mode Switching Waveforms
$\mathrm{V}_{\mathrm{IN}}=\mathbf{2 0 V}, \mathrm{V}_{\text {OUT }}=5 \mathrm{~V}, \mathrm{I}_{\text {LOAD }}=400 \mathrm{~mA}$ $L=100 \mu \mathrm{H}$, C OUT $=120 \mu \mathrm{~F}$, C OUT ESR $=140 \mathrm{~m} \Omega$


Load Transient Response for Continuous Mode
$\mathrm{V}_{\text {IN }}=20 \mathrm{~V}, \mathrm{~V}_{\text {OUT }}=5 \mathrm{~V}$, ILOAD $=200 \mathrm{~mA}$ to 500 mA $L=100 \mu \mathrm{H}$, C OUT $=120 \mu \mathrm{~F}$, C OUT ESR $=140 \mathrm{~m} \Omega$


A: Output Voltage, $50 \mathrm{mV} /$ div. (AC)
B: 200 mA to 500 mA Load Pulse
Horizontal Time Base: $50 \mu \mathrm{~s} / \mathrm{div}$.

Discontinuous Mode Switching Waveforms $\mathrm{V}_{\text {IN }}=20 \mathrm{~V}, \mathrm{~V}_{\text {OUT }}=5 \mathrm{~V}$, $\mathrm{I}_{\text {LOAD }}=200 \mathrm{~mA}$
$\mathbf{L}=33 \mu \mathrm{H}$, C OUT $=220 \mu \mathrm{~F}$, C $_{\text {OUT }} \mathrm{ESR}=60 \mathrm{~m} \Omega$


A: Output Pin Voltage, 10V/div.
B: Inductor Current 0.2A/div.
C: Output Ripple Voltage, $20 \mathrm{mV} /$ div, Horizontal Time Base: $2 \mu \mathrm{~s} /$ div.

Load Transient Response for Discontinuous Mode $\mathrm{V}_{\text {IN }}=20 \mathrm{~V}, \mathrm{~V}_{\text {OUT }}=5 \mathrm{~V}$, ILOAD $=100 \mathrm{~mA}$ to 200 mA $\mathrm{L}=\mathbf{3 3} \mu \mathrm{H}$, C OUT $=\mathbf{2 2 0} \mu \mathrm{F}, \mathrm{C}_{\text {OUT }} \mathrm{ESR}=60 \mathrm{~m} \Omega$


A: Output Voltage, $50 \mathrm{mV} /$ div. (AC)
B: 100 mA to 200 mA Load Pulse
Horizontal Time Base: $200 \mu \mathrm{~s} / \mathrm{div}$.

Connection Diagrams and Order Information


Order Number LM2597N-3.3, LM2597N-5.0, LM2597N-12 or LM2597N-ADJ
See NS Package Number N08E


Top View
Order Number LM2597M-3.3, LM2597M-5.0, LM2597M-12 or LM2597M-ADJ
See NS Package Number M08A

| LM2597 Series Buck Regulator Design Procedure (Fixed Output) |  |
| :---: | :---: |
| PROCEDURE (Fixed Output Voltage Version) | EXAMPLE (Fixed Output Voltage Version) |
| Given: <br> $\mathrm{V}_{\text {OUT }}=$ Regulated Output Voltage (3.3V, 5 V or 12 V ) <br> $\mathrm{V}_{\mathrm{IN}}(\max )=$ Maximum DC Input Voltage <br> LLOAD (max) $=$ Maximum Load Current <br> 1. Inductor Selection (L1) <br> A. Select the correct inductor value selection guide from Figures 3, 4, or 5 . (Output voltages of $3.3 \mathrm{~V}, 5 \mathrm{~V}$, or 12 V respectively.) For all other voltages, see the design procedure for the adjustable version. <br> B. From the inductor value selection guide, identify the inductance region intersected by the Maximum Input Voltage line and the Maximum Load Current line. Each region is identified by an inductance value and an inductor code (LXX). <br> C. Select an appropriate inductor from the four manufacturer's part numbers listed in Figure 7. <br> 2. Output Capacitor Selection (COUT) <br> A. In the majority of applications, low ESR (Equivalent Series Resistance) electrolytic capacitors between $82 \mu \mathrm{~F}$ and $220 \mu \mathrm{~F}$ and low ESR solid tantalum capacitors between $15 \mu \mathrm{~F}$ and $100 \mu \mathrm{~F}$ provide the best results. This capacitor should be located close to the IC using short capacitor leads and short copper traces. Do not use capacitors larger than $220 \mu \mathrm{~F}$. <br> For additional information, see section on output capacitors in application information section. <br> B. To simplify the capacitor selection procedure, refer to the quick design component selection table shown in Figure 1. This table contains different input voltages, output voltages, and load currents, and lists various inductors and output capacitors that will provide the best design solutions. <br> C. The capacitor voltage rating for electrolytic capacitors should be at least 1.5 times greater than the output voltage, and often much higher voltage ratings are needed to satisfy the low ESR requirements for low output ripple voltage. <br> D. For computer aided design software, see Switchers Made Simple ${ }^{\circledR}$ (version 4.1 or later). <br> 3. Catch Diode Selection (D1) <br> A. The catch diode current rating must be at least 1.3 times greater than the maximum load current. Also, if the power supply design must withstand a continuous output short, the diode should have a current rating equal to the maximum current limit of the LM2597. The most stressful condition for this diode is an overload or shorted output condition. <br> B. The reverse voltage rating of the diode should be at least 1.25 times the maximum input voltage. <br> C. This diode must be fast (short reverse recovery time) and must be located close to the LM2597 using short leads and short printed circuit traces. Because of their fast switching speed and low forward voltage drop, Schottky diodes provide the best performance and efficiency, and should be the first choice, especially in low output voltage applications. Ultra-fast recovery, or HighProcedure continued on next page. | Given: $\begin{aligned} & \mathrm{V}_{\text {OUT }}=5 \mathrm{~V} \\ & \mathrm{~V}_{\text {IN }}(\max )=12 \mathrm{~V} \\ & \mathrm{I}_{\text {LOAD }}(\max )=0.4 \mathrm{~A} \end{aligned}$ <br> 1. Inductor Selection (L1) <br> A. Use the inductor selection guide for the 5 V version shown in Figure 4. <br> B. From the inductor value selection guide shown in Figure 4, the inductance region intersected by the 12 V horizontal line and the 0.4A vertical line is $100 \mu \mathrm{H}$, and the inductor code is L20. <br> C. The inductance value required is $100 \mu \mathrm{H}$. From the table in Figure 7, go to the L20 line and choose an inductor part number from any of the four manufacturers shown. (In most instance, both through hole and surface mount inductors are available.) <br> 2. Output Capacitor Selection (COUT) <br> A. See section on output capacitors in application information section. <br> B. From the quick design component selection table shown in Figure 1, locate the 5V output voltage section. In the load current column, choose the load current line that is closest to the current needed in your application, for this example, use the 0.5A line. In the maximum input voltage column, select the line that covers the input voltage needed in your application, in this example, use the 15 V line. Continuing on this line are recommended inductors and capacitors that will provide the best overall performance. <br> The capacitor list contains both through hole electrolytic and surface mount tantalum capacitors from four different capacitor manufacturers. It is recommended that both the manufacturers and the manufacturer's series that are listed in the table be used. <br> In this example aluminum electrolytic capacitors from several different manufacturers are available with the range of ESR numbers needed. <br> $120 \mu \mathrm{~F} 25 \mathrm{~V}$ Panasonic HFQ Series <br> $120 \mu \mathrm{~F}$ 25V Nichicon PL Series <br> C. For a 5 V output, a capacitor voltage rating at least 7.5 V or more is needed. But, in this example, even a low ESR, switching grade, $120 \mu \mathrm{~F} 10 \mathrm{~V}$ aluminum electrolytic capacitor would exhibit approximately $400 \mathrm{~m} \Omega$ of ESR (see the curve in Figure 16 for the ESR vs voltage rating). This amount of ESR would result in relatively high output ripple voltage. To reduce the ripple to $1 \%$ of the output voltage, or less, a capacitor with a higher voltage rating (lower ESR) should be selected. A 16 V or 25 V capacitor will reduce the ripple voltage by approximately half. <br> 3. Catch Diode Selection (D1) <br> A. Refer to the table shown in Figure 10. In this example, a 1A, 20V, 1 N5817 Schottky diode will provide the best performance, and will not be overstressed even for a shorted output. |

LM2597 Series Buck Regulator Design Procedure (Fixed Output) (Continued)

PROCEDURE (Fixed Output Voltage Version)
Efficiency rectifiers also provide good results. Ultra-fast recovery diodes typically have reverse recovery times of 50 ns or less. Rectifiers such as the 1N4001 series are much too slow and should not be used.
4. Input Capacitor ( $\mathrm{C}_{\mathrm{IN}}$ )

A low ESR aluminum or tantalum bypass capacitor is needed between the input pin and ground to prevent large voltage transients from appearing at the input. In addition, the RMS current rating of the input capacitor should be selected to be at least $1 / 2$ the DC load current. The capacitor manufacturers data sheet must be checked to assure that this current rating is not exceeded. The curve shown in Figure 15 shows typical RMS current ratings for several different aluminum electrolytic capacitor values.
This capacitor should be located close to the IC using short leads and the voltage rating should be approximately 1.5 times the maximum input voltage.
If solid tantalum input capacitors are used, it is recomended that they be surge current tested by the manufacturer.
Use caution when using ceramic capacitors for input bypassing, because it may cause severe ringing at the $\mathrm{V}_{\mathrm{IN}}$ pin.
For additional information, see section on input capacitors in Application Information section.

## EXAMPLE (Fixed Output Voltage Version)

4. Input Capacitor ( $\mathrm{C}_{\mathrm{IN}}$ )

The important parameters for the Input capacitor are the input voltage rating and the RMS current rating. With a nominal input voltage of 12 V , an aluminum electrolytic capacitor with a voltage rating greater than 18V (1.5 $\times$
$\mathrm{V}_{\mathrm{IN}}$ ) would be needed. The next higher capacitor voltage rating is 25 V .
The RMS current rating requirement for the input capacitor in a buck regulator is approximately $1 / 2$ the DC load current. In this example, with a 400 mA load, a capacitor with a RMS current rating of at least 200 mA is needed. The curves shown in Figure 15 can be used to select an appropriate input capacitor. From the curves, locate the 25 V line and note which capacitor values have RMS current ratings greater than 200 mA . Either a $47 \mu \mathrm{~F}$ or $68 \mu \mathrm{~F}, 25 \mathrm{~V}$ capacitor could be used.
For a through hole design, a $68 \mu \mathrm{~F} / 25 \mathrm{~V}$ electrolytic capacitor (Panasonic HFQ series or Nichicon PL series or equivalent) would be adequate. other types or other manufacturers capacitors can be used provided the RMS ripple current ratings are adequate.
For surface mount designs, solid tantalum capacitors are recommended. The TPS series available from AVX, and the 593D series from Sprague are both surge current tested.

| Conditions |  |  | Inductor |  | Output Capacitor |  |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  |  | Through Hole | Surface Mount |  |
| Output Voltage (V) | Load Current (A) | Max Input Voltage (V) |  |  | Inductance ( $\mu \mathrm{H}$ ) | Inductor (\#) | Panasonic HFQ Series ( $\mu \mathrm{F} / \mathrm{V}$ ) | Nichicon PL Series ( $\mu \mathrm{F} / \mathrm{V}$ ) | AVX TPS Series ( $\mu \mathrm{F} / \mathrm{V}$ ) | Sprague 595D Series ( $\mu \mathrm{F} / \mathrm{V}$ ) |
| 3.3 | 0.5 | 5 | 33 | L14 | 220/16 | 220/16 | 100/16 | 100/6.3 |
|  |  | 7 | 47 | L13 | 120/25 | 120/25 | 100/16 | 100/6.3 |
|  |  | 10 | 68 | L21 | 120/25 | 120/25 | 100/16 | 100/6.3 |
|  |  | 40 | 100 | L20 | 120/35 | 120/35 | 100/16 | 100/6.3 |
|  | 0.2 | 6 | 68 | L4 | 120/25 | 120/25 | 100/16 | 100/6.3 |
|  |  | 10 | 150 | L10 | 120/16 | 120/16 | 100/16 | 100/6.3 |
|  |  | 40 | 220 | L9 | 120/16 | 120/16 | 100/16 | 100/6.3 |
| 5 | 0.5 | 8 | 47 | L13 | 180/16 | 180/16 | 100/16 | 33/25 |
|  |  | 10 | 68 | L21 | 180/16 | 180/16 | 100/16 | 33/25 |
|  |  | 15 | 100 | L20 | 120/25 | 120/25 | 100/16 | 33/25 |
|  |  | 40 | 150 | L19 | 120/25 | 120/25 | 100/16 | 33/25 |
|  | 0.2 | 9 | 150 | L10 | 82/16 | 82/16 | 100/16 | 33/25 |
|  |  | 20 | 220 | L9 | 120/16 | 120/16 | 100/16 | 33/25 |
|  |  | 40 | 330 | L8 | 120/16 | 120/16 | 100/16 | 33/25 |
| 12 | 0.5 | 15 | 68 | L21 | 82/25 | 82/25 | 100/16 | 15/25 |
|  |  | 18 | 150 | L19 | 82/25 | 82/25 | 100/16 | 15/25 |
|  |  | 30 | 220 | L27 | 82/25 | 82/25 | 100/16 | 15/25 |
|  |  | 40 | 330 | L26 | 82/25 | 82/25 | 100/16 | 15/25 |
|  | 0.2 | 15 | 100 | L11 | 82/25 | 82/25 | 100/16 | 15/25 |
|  |  | 20 | 220 | L9 | 82/25 | 82/25 | 100/16 | 15/25 |
|  |  | 40 | 330 | L17 | 82/25 | 82/25 | 100/16 | 15/25 |

FIGURE 1. LM2597 Fixed Voltage Quick Design Component Selection Table

|  |  |
| :---: | :---: |
| PROCEDURE (Adjustable Output Voltage V | EXAMPLE (Adjustable Out |
|  | Given: |
| Given: | $\mathrm{V}_{\text {OUT }}=20 \mathrm{~V}$ |
| $\mathrm{V}_{\mathrm{IN}}($ max $)=$ Maximum Input Voltage | max) $=$ |
| $l_{\text {LOAD }}($ max $)=$ Maximum Load Curren | , |
| F $=$ Switching Freque | $\mathrm{F}=$ Switching |
| 1. Programming Output Voltage (Selecting $\mathrm{R}_{1}$ and $\mathrm{R}_{2}$, as shown in Figure 12) | 1. Programming Output Voltage (Selecting $R_{1}$ and $R_{2}$, as shown in Figure 12) |
| Use the following formula to select the appropriate resistor values. | Select $R_{1}$ to be $1 \mathrm{k} \Omega, 1 \%$. Solve for $R_{2}$. |
| $V_{\text {OUT }}=V_{\text {REF }}\left(1+\frac{R_{2}}{R_{1}}\right) \text { where } V_{R E F}=1.23 V$ <br> Select a value for $R_{1}$ between $240 \Omega$ and $1.5 \mathrm{k} \Omega$. The lower resistor values minimize noise pickup in the sensitive feedback pin. (For the lowest temperature coefficient and the best stability with time, use $1 \%$ metal film resistors.) | $\mathrm{R}_{2}=\mathrm{R}_{1}\left(\frac{\mathrm{~V}_{\mathrm{OUT}}}{\mathrm{~V}_{\mathrm{REF}}}-1\right)=1 \mathrm{k}\left(\frac{20 \mathrm{~V}}{1.23 \mathrm{~V}}-1\right)$ <br> $R_{2}=1 k(16.26-1)=15.26 k$, closest $1 \%$ value is $15.4 \mathrm{k} \Omega$. $\mathrm{R}_{2}=15.4 \mathrm{k} \Omega .$ |
|  |  |
|  |  |
| = $\mathrm{R}_{1}\left(\frac{\mathrm{~V}_{\text {OUT }}}{\mathrm{V}_{\mathrm{REF}}}-1\right)$ |  |
| 2. Inductor Selection (L1) <br> A. Calculate the inductor Volt microsecond constant $\mathrm{E} \bullet \mathrm{T}(\mathrm{V} \bullet \mu \mathrm{s})$, from the following formula: | 2. Inductor Selection (L1) <br> A. Calculate the inductor Volt - microsecond constant ( $\mathrm{E} \cdot \mathrm{T}$ ), |
|  |  |
| $E \bullet T=\left(V_{I N}-V_{\text {OUT }}-V_{S A T}\right) \cdot \frac{V_{\text {OUT }}+V_{D}}{V_{I N}-V_{S A T}+V_{D}} \cdot \frac{1000}{150 \mathrm{kHz}}(V \bullet \mu \mathrm{~s})$ | $\mathrm{E} \cdot \mathrm{~T}=(28-20-0.9) \cdot \frac{20+0.5}{28-0.9+0.5} \cdot \frac{1000}{150}(\mathrm{~V} \cdot \mu \mathrm{~s})$ |
| where $\mathrm{V}_{\text {SAT }}=$ internal switch saturation voltage $=0.9 \mathrm{~V}$ and $V_{D}=$ diode forward voltage drop $=0.5 \mathrm{~V}$ | $\mathrm{E} \cdot \mathrm{~T}=(7.1) \cdot \frac{20.5}{27.6} \bullet 6.67(\mathrm{~V} \bullet \mu \mathrm{~s})=35.2(\mathrm{~V} \cdot \mu \mathrm{~s})$ |
| B. Use the E - T value from the previous formula and match it with the $\mathrm{E} \cdot \mathrm{T}$ number on the vertical axis of the Inductor Value Selection Guide shown in Figure 6. | B. $\mathrm{E} \cdot \mathrm{T}=35.2(\mathrm{~V} \bullet \mu \mathrm{~s})$ |
|  | C. $\mathrm{ILOAD}^{\text {(max }}$ ) $=0.5 \mathrm{~A}$ |
| C. on the horizontal axis, select the maximum load current. | D. From the inductor value selection guide shown in Figure 6 , the inductance region intersected by the 35 (V • $\mu \mathrm{s}$ ) horizontal line and the 0.5 A vertical line is $150 \mu \mathrm{H}$, and the inductor code is L19. |
| D. Identify the inductance region intersected by the E•T value and the Maximum Load Current value. Each region is identified by an inductance value and an inductor code (LXX). |  |
|  | E. From the table in Figure 7, locate line L19, and select an inductor part number from the list of manufacturers part numbers. |
| E. Select an appropriate inductor from the four manufacturer's part numbers listed in Figure 7. |  |
| 3. Output Capacitor Se | Output Capacitor Selection (Cout) <br> A. See section on Cout in Application Information section. <br> B. From the quick design table shown in Figure 2, locate the output voltage column. From that column, locate the output voltage closest to the output voltage in your application. In this example, select the 24 V line. Under the output capacitor section, select a capacitor from the list of through hole electrolytic or surface mount tantalum types from four different capacitor manufacturers. It is recommended that both the manufacturers and the manufacturers series that are listed in the table be used. <br> In this example, through hole aluminum electrolytic capacitors from several different manufacturers are available. <br> $82 \mu \mathrm{~F}$ 50V Panasonic HFQ Series <br> $120 \mu \mathrm{~F}$ 50V Nichicon PL Series <br> Example continued on next page. |
| A. In the majority of applications, low ESR electrolytic or solid tantalum capacitors between $82 \mu \mathrm{~F}$ and $220 \mu \mathrm{~F}$ |  |
| provide the best results. This capacitor should be located close to the IC using short capacitor leads and short copper traces. Do not use capacitors larger than $220 \mu \mathrm{~F}$. For additional information, see section on output capacitors in application information section. |  |
| B. To simplify the capacitor selection procedure, refer to the quick design table shown in Figure 2. This table contains different output voltages, and lists various output capacitors that will provide the best design solutions. |  |
| C. The capacitor voltage rating should be at least 1.5 times greater than the output voltage, and often much higher voltage ratings are needed to satisfy the low ESR requirements needed for low output ripple voltage. |  |
|  |  |
| Procedure continued on next page. |  |

Procedure continued on next page.
A. See section on COUT in Application Information section.
hown in Figure 2, locate the output voltage column. From that column, locate the cation output capacitor section, select a capacitor from the list of through hole electrolytic or surface mount tantalum types from four different capacitor manufacturers. It is recommended that both the manufacturers and the man-解 pacitors from several different manufacturers are available.
$120 \mu \mathrm{~F} \quad 50 \mathrm{~V}$ Nichicon PL Series
Example continued on next page.

|  |  |
| :---: | :---: |
| PROCEDURE (Adjustable Output Voltage Version) | EXAMPLE (Adjustable Output Voltage Version) |
| 4. Feedforward Capacitor ( $\mathrm{C}_{\mathrm{FF}}$ ) (See Figure 12) <br> For output voltages greater than approximately 10 V , an additional capacitor is required. The compensation capacitor is typically between 50 pF and 10 nF , and is wired in parallel with the output voltage setting resistor, $\mathrm{R}_{2}$. It provides additional stability for high output voltages, low input-output voltages, and/or very low ESR output capacitors, such as solid tantalum capacitors. $\mathrm{C}_{\mathrm{FF}}=\frac{1}{31 \times 10^{3} \times \mathrm{R}_{2}}$ | C. For a 20 V output, a capacitor rating of at least 30 V or more is needed. In this example, either a 35 V or 50 V capacitor would work. A 50 V rating was chosen because it has a lower ESR which provides a lower output ripple voltage. <br> Other manufacturers or other types of capacitors may also be used, provided the capacitor specifications (especially the 100 kHz ESR) closely match the types listed in the table. Refer to the capacitor manufacturers data sheet for this information. <br> 4. Feedforward Capacitor ( $\mathrm{C}_{\mathrm{FF}}$ ) <br> The table shown in Figure 2 contains feed forward capacitor values for various output voltages. In this example, a 1 nF capacitor is needed. |
| 5. Catch Diode Selection (D1) <br> A. The catch diode current rating must be at least 1.3 times greater than the maximum load current. Also, if the power supply design must withstand a continuous output short, the diode should have a current rating equal to the maximum current limit of the LM2597. The most stressful condition for this diode is an overload or shorted output condition. | 5. Catch Diode Selection (D1) |
|  | A. Refer to the table shown in Figure 10. Schottky diodes provide the best performance, and in this example a 1A, 40V, 1 N5819 Schottky diode would be a good choice. The 1A diode rating is more than adequate and will not be overstressed even for a shorted output. <br> 6. Input Capacitor ( $\mathrm{C}_{\text {IN }}$ ) <br> The important parameters for the Input capacitor are the |
| B. The reverse voltage rating of the diode should be at least 1.25 times the maximum input voltage. | input voltage rating and the RMS current rating. With a nominal input voltage of 28 V , an aluminum electrolytic |
| C. This diode must be fast (short reverse recovery time) and must be located close to the LM2597 using short leads and short printed circuit traces. Because of their fast switching speed and low forward voltage drop, Schottky diodes provide the best performance and efficiency, and should be the first choice, especially in low | aluminum electrolytic capacitor with a voltage rating greater than 42V ( $1.5 \times \mathrm{V}_{\mathrm{IN}}$ ) would be needed. Since the the next higher capacitor voltage rating is 50 V , a 50 V capacitor should be used. The capacitor voltage rating of ( $1.5 \times \mathrm{V}_{\mathrm{IN}}$ ) is a conservative guideline, and can be modified somewhat if desired. |
| output voltage applications. Ultra-fast recovery, or HighEfficiency rectifiers are also a good choice, but some types with an abrupt turn-off characteristic may cause instability or EMI problems. Ultra-fast recovery diodes | The RMS current rating requirement for the input capacitor of a buck regulator is approximately $1 / 2$ the DC load current. In this example, with a 400 mA load, a capacitor with a RMS current rating of at least 200 mA is needed. |
| typically have reverse recovery times of 50 ns or less. Rectifiers such as the 1 N4001 series are much too slow and should not be used. | The curves shown in Figure 15 can be used to select an appropriate input capacitor. From the curves, locate the 50 V line and note which capacitor values have RMS cur- |
| 6. Input Capacitor ( $\mathrm{C}_{\mathbf{I N}}$ ) <br> A low ESR aluminum or tantalum bypass capacitor is | rent ratings greater than 200 mA . A $47 \mu \mathrm{~F} / 50 \mathrm{~V}$ low ESR electrolytic capacitor capacitor is needed. |
| needed between the input pin and ground to prevent large voltage transients from appearing at the input. In addition, the RMS current rating of the input capacitor should be selected to be at least $1 / 2$ the DC load current. The capacitor manufacturers data sheet must be | For a through hole design, a $47 \mu \mathrm{~F} / 50 \mathrm{~V}$ electrolytic capacitor (Panasonic HFQ series or Nichicon PL series or equivalent) would be adequate. Other types or other manufacturers capacitors can be used provided the RMS ripple current ratings are adequate. |
| checked to assure that this current rating is not exceeded. The curve shown in Figure 15 shows typical RMS current ratings for several different aluminum electrolytic capacitor values. | For surface mount designs, solid tantalum capacitors are recommended. The TPS series available from AVX, and the 593D series from Sprague are both surge current tested. |
| This capacitor should be located close to the IC using short leads and the voltage rating should be approximately 1.5 times the maximum input voltage. | To further simplify the buck regulator design procedure, National Semiconductor is making available computer design software to be used with the Simple Switcher line ot switch- |
| If solid tantalum input capacitors are used, it is recomended that they be surge current tested by the manufacturer. | ing regulators. Switchers Made Simple ${ }^{\circledR}$ (version 4.1 or later) is available on a $31 / 2^{\prime \prime}$ diskette for IBM compatible computers. |
| Use caution when using ceramic capacitors for input bypassing, because it may cause severe ringing at the $\mathrm{V}_{\mathrm{IN}}$ pin. |  |
| For additional information, see section on input capacitor in application information section. |  |


| LM2597 Series Buck Regulator Design Procedure (Adjustable Output)(Continued) |  |  |  |  |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  | Through Hole Output Capacitor |  |  | Surface Mount Output Capacitor |  |  |
| Voltage <br> (V) | Panasonic HFQ Series ( $\mu \mathrm{F} / \mathrm{V}$ ) | Nichicon PL <br> Series <br> ( $\mu \mathrm{F} / \mathrm{V}$ ) | Feedforward Capacitor | AVX TPS Series ( $\mu \mathrm{F} / \mathrm{V}$ ) | Sprague 595D Series ( $\mu \mathrm{F} / \mathrm{V}$ ) | Feedforward Capacitor |
| 1.2 | 220/25 | 220/25 | 0 | 220/10 | 220/10 | 0 |
| 4 | 180/25 | 180/25 | 4.7 nF | 100/10 | 120/10 | 4.7 nF |
| 6 | 82/25 | 82/25 | 4.7 nF | 100/10 | 120/10 | 4.7 nF |
| 9 | 82/25 | 82/25 | 3.3 nF | 100/16 | 100/16 | 3.3 nF |
| 12 | 82/25 | 82/25 | 2.2 nF | 100/16 | 100/16 | 2.2 nF |
| 15 | 82/25 | 82/25 | 1.5 nF | 68/20 | 100/20 | 1.5 nF |
| 24 | 82/50 | 120/50 | 1 nF | 10/35 | 15/35 | 220 pF |
| 28 | 82/50 | 120/50 | 820 pF | 10/35 | 15/35 | 220 pF |

FIGURE 2. Output Capacitor and Feedforward Capacitor Selection Table

## LM2597 Series Buck Regulator Design Procedure

INDUCTOR VALUE SELECTION GUIDES (For Continuous Mode Operation)


FIGURE 3. LM2597-3.3


FIGURE 5. LM2597-12


MAXIMUM LOAD CURRENT (A)
FIGURE 4. LM2597-5.0


FIGURE 6. LM2597-ADJ


## LM2597 Series Buck Regulator Design Procedure (Continued)

| VR | 1A Diodes |  |  |  |
| :---: | :---: | :---: | :---: | :---: |
|  | Surface Mount |  | Through Hole |  |
|  | Schottky | Ultra Fast Recovery | Schottky | Ultra Fast Recovery |
| 20V |  | All of these diodes are rated to at least 50 V . <br> MURS120 <br> 10BF10 | 1N5817 | All of these diodes are rated to at least 50 V . <br> MUR120 <br> HER101 <br> 11DF1 |
|  |  |  | SR102 |  |
| 30V | MBRS130 |  | 1N5818 |  |
|  |  |  | SR103 |  |
|  |  |  | 11DQ03 |  |
| 40V | MBRS140 |  | 1N5819 |  |
|  | 10BQ040 |  | SR104 |  |
|  | 10MQ040 |  | 11DQ04 |  |
| $\begin{gathered} 50 \mathrm{~V} \\ \text { or } \\ \text { more } \end{gathered}$ | MBRS160 |  | SR105 |  |
|  | 10BQ050 |  | MBR150 |  |
|  | 10MQ060 |  | 11DQ05 |  |

FIGURE 10. Diode Selection Table

## Block Diagram



## Test Circuit and Layout Guidelines



Component Values shown are for $\mathrm{V}_{\mathrm{IN}}=15 \mathrm{~V}$,
Typical Values
$\mathrm{V}_{\text {OUT }}=5 \mathrm{~V}, \mathrm{I}_{\text {LOAD }}=500 \mathrm{~mA}$.
$\mathrm{C}_{\mathrm{IN}}-47 \mu \mathrm{~F}, 50 \mathrm{~V}$, Aluminum Electrolytic
CSS $\quad-0.1 \mu \mathrm{~F}$
Nichicon "PL Series"
COUT - $120 \mu \mathrm{~F}, 25 \mathrm{~V}$ Aluminum Electrolytic,
$C_{\text {deLay }}-0.1 \mu \mathrm{~F}$
Reull Up -4.7 k
Nichicon "PL Series"

* Use Bias Supply pin for 5V and 12V Versions

D1 - 1A, 30V Schottky Rectifier, 1N5818
L1 $\quad-100 \mu \mathrm{H}, \mathrm{L} 20$


TL/H/12440-56
$\mathrm{V}_{\text {OUT }}=\mathrm{V}_{\text {REF }}\left(1+\frac{\mathrm{R}_{2}}{\mathrm{R}_{1}}\right) \quad$ where $\mathrm{V}_{\text {REF }}=1.23 \mathrm{~V}$
$R_{2}=R_{1}\left(\frac{V_{\text {OUT }}}{V_{\text {REF }}}-1\right) \quad \begin{aligned} & \text { Select } R_{1} \text { to be approximately } 1 \mathrm{k} \Omega, \\ & \text { use a } 1 \% \text { resistor for best stability. }\end{aligned}$
Component Values shown are for $\mathrm{V}_{\mathrm{IN}}=20 \mathrm{~V}$,
$\mathrm{V}_{\text {OUT }}=10 \mathrm{~V}$, I LOAD $=500 \mathrm{~mA}$.
$\mathrm{C}_{\mathrm{IN}}-68 \mu \mathrm{~F}, 35 \mathrm{~V}$, Aluminum Electrolytic Nichicon "PL Series"
COUT $-120 \mu \mathrm{~F}, 25 \mathrm{~V}$ Aluminum Electrolytic, Nichicon "PL Series"

D1 - 1A, 30V Schottky Rectifier, 1N5818
L1 $-150 \mu \mathrm{H}, \mathrm{L} 19$
$R_{1}-1 \mathrm{k} \Omega, 1 \%$
$R_{2}-7.15 \mathrm{k}, 1 \%$
$\mathrm{C}_{\mathrm{FF}}-3.3 \mathrm{nF}$, See Application Information Section
Typical Values
CSS-0.1 $\mu \mathrm{F}$
$\mathrm{C}_{\text {DELAY }}-0.1 \mu \mathrm{~F}$
Rpull up-4.7k

* For output voltages between 4 V and 20 V


## FIGURE 12. Standard Test Circuits and Layout Guides

As in any switching regulator, layout is very important. Rapidly switching currents associated with wiring inductance can generate voltage transients which can cause problems. For minimal inductance and ground loops, the wires indicated by heavy lines should be wide printed circuit traces and should be kept as short as possible. For best results, external components should be located as close to the switcher IC as possible using ground plane construction or single point grounding.

If open core inductors are used, special care must be taken as to the location and positioning of this type of inductor. Allowing the inductor flux to intersect sensitive feedback, IC groundpath and COUT wiring can cause problems. When using the adjustable version, special care must be taken as to the location of the feedback resistors and the associated wiring. Physically locate both resistors near the IC, and route the wiring away from the inductor, especially an open core type of inductor. (See application section for more information.)

## Application Information

## PIN FUNCTIONS

$+\mathbf{V}_{\mathbf{I N}}$ (Pin 7)—This is the positive input supply for the IC switching regulator. A suitable input bypass capacitor must be present at this pin to minimize voltage transients and to supply the switching currents needed by the regulator.
Ground (Pin 6)-Circuit ground.
Output (Pin 8)—Internal switch. The voltage at this pin switches between ( $+\mathrm{V}_{\mathrm{IN}}-\mathrm{V}_{\mathrm{SAT}}$ ) and approximately -0.5 V , with a duty cycle of $\mathrm{V}_{\mathrm{OUT}} / \mathrm{V}_{\text {IN }}$. To minimize coupling to sensitive circuitry, the PC board copper area connected to this pin should be kept to a minimum.
Feedback (Pin 4)—Senses the regulated output voltage to complete the feedback loop.
$\overline{\text { Shutdown/Soft-start (Pin 5)—This dual function pin pro- }}$ vides the following features: (a) Allows the switching regulator circuit to be shut down using logic level signals thus dropping the total input supply current to approximately $80 \mu \mathrm{~A}$. (b) Adding a capacitor to this pin provides a soft-start feature which minimizes startup current and provides a controlled ramp up of the output voltage.
Error Flag (Pin 1)—Open collector output that provides a low signal (flag transistor ON) when the regulated output voltage drops more than $5 \%$ from the nominal output voltage. On start up, Error Flag is low until $\mathrm{V}_{\text {OUT }}$ reaches $95 \%$ of the nominal output voltage and a delay time determined by the Delay pin capacitor. This signal can be used as a reset to a microprocessor on power-up.
Delay (Pin 2)—At power-up, this pin can be used to provide a time delay between the time the regulated output voltage reaches $95 \%$ of the nominal output voltage, and the time the error flag output goes high.
Bias Supply (Pin 3)—This feature allows the regulators internal circuitry to be powered from the regulated output voltage or an external supply, instead of the input voltage. This results in increased efficiency under some operating conditions, such as low output current and/or high input voltage.
Special Note If any of the above four features (Shutdown/ Soft-start, Error Flag, Delay, or Bias Supply) are not used, the respective pins should be left open.

## EXTERNAL COMPONENTS

## SOFT-START CAPACITOR

$\mathrm{C}_{\text {SS }}$-A capacitor on this pin provides the regulator with a Soft-start feature (slow start-up). When the DC input voltage is first applied to the regulator, or when the Shutdown/Softstart pin is allowed to go high, a constant current (approximately $5 \mu \mathrm{~A}$ begins charging this capacitor). As the capacitor voltage rises, the regulator goes through four operating regions (See the bottom curve in Figure 13).

1. Regulator in Shutdown. When the $\overline{\mathrm{SD}} / \mathrm{SS}$ pin voltage is between 0 V and 1.3 V , the regulator is in shutdown, the output voltage is zero, and the IC quiescent current is approximately $85 \mu \mathrm{~A}$.
2. Regulator ON, but the output voltage is zero. With the $\overline{\mathrm{SD}} / \mathrm{SS}$ pin voltage between approximately 1.3 V and 1.8 V , the internal regulatory circuitry is operating, the quiescent current rises to approximately 5 mA , but the output voltage is still zero. Also, as the 1.3 V threshold is exceeded, the Soft-start capacitor charging current decreases from $5 \mu \mathrm{~A}$ down to approximately $1.6 \mu \mathrm{~A}$. This decreases the slope of capacitor voltage ramp.
3. Soft-start Region. When the $\overline{\text { SD }} / \mathrm{SS}$ pin voltage is between 1.8 V and 2.8 V (@ $25^{\circ} \mathrm{C}$ ), the regulator is in a Softstart condition. The switch (Pin 8) duty cycle initially starts out very low, with narrow pulses and gradually get wider as the capacitor $\overline{\mathrm{SD}} / \mathrm{SS}$ pin ramps up towards 2.8 V . As the duty cycle increases, the output voltage also increases at a controlled ramp up. See the center curve in Figure 13. The input supply current requirement also starts out at a low level for the narrow pulses and ramp up in a controlled manner. This is a very useful feature in some switcher topologies that require large startup currents (such as the inverting configuration) which can load down the input power supply.
Note: The lower curve shown in Figure 13 shows the Soft-start region from $0 \%$ to $100 \%$. This is not the duty cycle percentage, but the output voltage percentage. Also, the Soft-start voltage range has a negative temperature coefficient associated with it. See the Soft-start curve in the electrical characteristics section.
4. Normal operation. Above 2.8 V , the circuit operates as a standard Pulse Width Modulated switching regulator. The capacitor will continue to charge up until it reaches the internal clamp voltage of approximately 7 V . If this pin is driven from a voltage source, the current must be limited to about 1 mA .

time dependent upon delay capacitor value


TIME DEPENDENT UPON SOFT-START CAPACITOR VALUE
TL/H/12440-33
FIGURE 13. Soft-start, Delay, Error, Output

## Application Information (Continued)



TL/H/12440-34
FIGURE 14. Timing Diagram for 5V Output

## DELAY CAPACITOR

CDELAY-Provides delay for the error flag output. See the upper curve in Figure 13, and also refer to timing diagrams in Figure 14. A capacitor on this pin provides a time delay between the time the regulated output voltage (when it is increasing in value) reaches $95 \%$ of the nominal output voltage, and the time the error flag output goes high. A $3 \mu \mathrm{~A}$ constant current from the delay pin charges the delay capacitor resulting in a voltage ramp. When this voltage reaches a threshold of approximately 1.3 V , the open collector error flag output (or power OK) goes high. This signal can be used to indicate that the regulated output has reached the correct voltage and has stabilized.
If, for any reason, the regulated output voltage drops by $5 \%$ or more, the error output flag (Pin 1) immediately goes low (internal transistor turns on). The delay capacitor provides very little delay if the regulated output is dropping out of regulation. The delay time for an output that is decreasing is approximately a 1000 times less than the delay for the rising output. For a $0.1 \mu \mathrm{~F}$ delay capacitor, the delay time would be approximately 50 ms when the output is rising and passes through the $95 \%$ threshold, but the delay for the output dropping would only be approximately $50 \mu \mathrm{~s}$.
RPull Up-The error flag output, (or power OK) is the collector of a NPN transistor, with the emitter internally grounded. To use the error flag, a pullup resistor to a positive voltage is needed. The error flag transistor is rated up to a maximum of 45 V and can sink approximately 3 mA . If the error flag is not used, it can be left open.

INPUT CAPACITOR
$\mathbf{C}_{I N}$-A low ESR aluminum or tantalum bypass capacitor is needed between the input pin and ground pin. It must be located near the regulator using short leads. This capacitor prevents large voltage transients from appearing at the input, and provides the instantaneous current needed each time the switch turns on.
The important parameters for the Input capacitor are the voltage rating and the RMS current rating. Because of the relatively high RMS currents flowing in a buck regulator's input capacitor, this capacitor should be chosen for its RMS current rating rather than its capacitance or voltage ratings, although the capacitance value and voltage rating are directly related to the RMS current rating.
The RMS current rating of a capacitor could be viewed as a capacitor's power rating. The RMS current flowing through the capacitors internal ESR produces power which causes the internal temperature of the capacitor to rise. The RMS current rating of a capacitor is determined by the amount of current required to raise the internal temperature approximately $10^{\circ} \mathrm{C}$ above an ambient temperature of $105^{\circ} \mathrm{C}$. The ability of the capacitor to dissipate this heat to the surrounding air will determine the amount of current the capacitor can safely sustain. Capacitors that are physically large and have a large surface area will typically have higher RMS current ratings. For a given capacitor value, a higher voltage electrolytic capacitor will be physically larger than a lower voltage capacitor, and thus be able to dissipate more heat to the surrounding air, and therefore will have a higher RMS current rating.

## Application Information (Continued)



FIGURE 15. RMS Current Ratings for Low ESR Electrolytic Capacitors (Typical)

The consequences of operating an electrolytic capacitor above the RMS current rating is a shortened operating life. The higher temperature speeds up the evaporation of the capacitor's electrolyte, resulting in eventual failure.
Selecting an input capacitor requires consulting the manufacturers data sheet for maximum allowable RMS ripple current. For a maximum ambient temperature of $40^{\circ} \mathrm{C}$, a general guideline would be to select a capacitor with a ripple current rating of approximately $50 \%$ of the DC load current. For ambient temperatures up to $70^{\circ} \mathrm{C}$, a current rating of $75 \%$ of the DC load current would be a good choice for a conservative design. The capacitor voltage rating must be at least 1.25 times greater than the maximum input voltage, and often a much higher voltage capacitor is needed to satisfy the RMS current requirements.
A graph shown in Figure 15 shows the relationship between an electrolytic capacitor value, its voltage rating, and the RMS current it is rated for. These curves were obtained from the Nichicon "PL" series of Iow ESR, high reliability electrolytic capacitors designed for switching regulator applications. Other capacitor manufacturers offer similar types of capacitors, but always check the capacitor data sheet.
"Standard" electrolytic capacitors typically have much higher ESR numbers, lower RMS current ratings and typically have a shorter operating lifetime.
Because of their small size and excellent performance, surface mount solid tantalum capacitors are often used for input bypassing, but several precautions must be observed. A small percentage of solid tantalum capacitors can short if the inrush current rating is exceeded. This can happen at turn on when the input voltage is suddenly applied, and of course, higher input voltages produce higher inrush currents. Several capacitor manufacturers do a $100 \%$ surge current testing on their products to minimize this potential


FIGURE 16. Capacitor ESR vs Capacitor Voltage Rating (Typical Low ESR Electrolytic Capacitor)
problem. If high turn on currents are expected, it may be necessary to limit this current by adding either some resistance or inductance before the tantalum capacitor, or select a higher voltage capacitor. As with aluminum electrolytic capacitors, the RMS ripple current rating must be sized to the load current.

## OUTPUT CAPACITOR

Cout-An output capacitor is required to filter the output and provide regulator loop stability. Low impedance or low ESR Electrolytic or solid tantalum capacitors designed for switching regulator applications must be used. When selecting an output capacitor, the important capacitor parameters are; the 100 kHz Equivalent Series Resistance (ESR), the RMS ripple current rating, voltage rating, and capacitance value. For the output capacitor, the ESR value is the most important parameter.
The output capacitor requires an ESR value that has an upper and lower limit. For low output ripple voltage, a low ESR value is needed. This value is determined by the maximum allowable output ripple voltage, typically $1 \%$ to $2 \%$ of the output voltage. But if the selected capacitor's ESR is extremely low, there is a possibility of an unstable feedback loop, resulting in an oscillation at the output. Using the capacitors listed in the tables, or similar types, will provide design solutions under all conditions.
If very low output ripple voltage (less than 15 mV ) is required, refer to the section on Output Voltage Ripple and Transients for a post ripple filter.
An aluminum electrolytic capacitor's ESR value is related to the capacitance value and its voltage rating. In most cases, Higher voltage electrolytic capacitors have lower ESR values (see Figure 16). Often, capacitors with much higher voltage ratings may be needed to provide the low ESR values required for low output ripple voltage.

## Application Information (Continued)

The output capacitor for many different switcher designs often can be satisfied with only three or four different capacitor values and several different voltage ratings. See the quick design component selection tables in Figures 1 and 2 for typical capacitor values, voltage ratings, and manufacturers capacitor types.
Electrolytic capacitors are not recommended for temperatures below $-25^{\circ} \mathrm{C}$. The ESR rises dramatically at cold temperatures and typically rises 3 X @ $-25^{\circ} \mathrm{C}$ and as much as 10 X at $-40^{\circ} \mathrm{C}$. See curve shown in Figure 17.
Solid tantalum capacitors have a much better ESR spec for cold temperatures and are recommended for temperatures below $-25^{\circ} \mathrm{C}$.

## CATCH DIODE

Buck regulators require a diode to provide a return path for the inductor current when the switch turns off. This must be a fast diode and must be located close to the LM2594 using short leads and short printed circuit traces.
Because of their very fast switching speed and low forward voltage drop, Schottky diodes provide the best performance, especially in low output voltage applications ( 5 V and lower). Ultra-fast recovery, or High-Efficiency rectifiers are also a good choice, but some types with an abrupt turnoff characteristic may cause instability or EMI problems. Ultrafast recovery diodes typically have reverse recovery times of 50 ns or less. Rectifiers such as the 1N4001 series are much too slow and should not be used.


TL/H/12440-37
FIGURE 17. Capacitor ESR Change vs Temperature

## INDUCTOR SELECTION

All switching regulators have two basic modes of operation; continuous and discontinuous. The difference between the two types relates to the inductor current, whether it is flowing continuously, or if it drops to zero for a period of time in the normal switching cycle. Each mode has distinctively different operating characteristics, which can affect the regulators performance and requirements. Most switcher designs will operate in the discontinuous mode when the load current is low.
The LM2597 (or any of the Simple Switcher family) can be used for both continuous or discontinuous modes of operation.
In many cases the preferred mode of operation is the continuous mode. It offers greater output power, lower peak switch, inductor and diode currents, and can have lower output ripple voltage. But it does require larger inductor values to keep the inductor current flowing continuously, especially at low output load currents and/or high input voltages.

To simplify the inductor selection process, an inductor selection guide (nomograph) was designed (see Figures 3 through 6). This guide assumes that the regulator is operating in the continuous mode, and selects an inductor that will allow a peak-to-peak inductor ripple current to be a certain percentage of the maximum design load current. This peak-to-peak inductor ripple current percentage is not fixed, but is allowed to change as different design load currents are selected. (See Figure 18.)


TL/H/12440-3
FIGURE 18. ( $\Delta l_{\text {IND }}$ ) Peak-to-Peak Inductor Ripple Current (as a Percentage of the Load Current) vs Load Current

By allowing the percentage of inductor ripple current to increase for low load currents, the inductor value and size can be kept relatively low.
When operating in the continuous mode, the inductor current waveform ranges from a triangular to a sawtooth type of waveform (depending on the input voltage), with the average value of this current waveform equal to the DC output load current.
Inductors are available in different styles such as pot core, toroid, E-core, bobbin core, etc., as well as different core materials, such as ferrites and powdered iron. The least expensive, the bobbin, rod or stick core, consists of wire wrapped on a ferrite bobbin. This type of construction makes for a inexpensive inductor, but since the magnetic flux is not completely contained within the core, it generates more Electro-Magnetic Interference (EMI). This magnetic flux can induce voltages into nearby printed circuit traces, thus causing problems with both the switching regulator operation and nearby sensitive circuitry, and can give incorrect scope readings because of induced voltages in the scope probe. Also see section on Open Core Inductors.
The inductors listed in the selection chart include ferrite E-core construction for Schott, ferrite bobbin core for Renco and Coilcraft, and powdered iron toroid for Pulse Engineering.
Exceeding an inductor's maximum current rating may cause the inductor to overheat because of the copper wire losses, or the core may saturate. If the inductor begins to saturate, the inductance decreases rapidly and the inductor begins to look mainly resistive (the DC resistance of the winding). This can cause the switch current to rise very rapidly and force the switch into a cycle-by-cycle current limit, thus reducing

## Application Information (Continued)

the DC output load current. This can also result in overheating of the inductor and/or the LM2597. Different inductor types have different saturation characteristics, and this should be kept in mind when selecting an inductor.
The inductor manufacturers data sheets include current and energy limits to avoid inductor saturation.

## DISCONTINUOUS MODE OPERATION

The selection guide chooses inductor values suitable for continuous mode operation, but for low current applications and/or high input voltages, a discontinuous mode design may be a better choice. It would use an inductor that would be physically smaller, and would need only one half to one third the inductance value needed for a continuous mode design. The peak switch and inductor currents will be higher in a discontinuous design, but at these low load currents ( 200 mA and below), the maximum switch current will still be less than the switch current limit.
Discontinuous operation can have voltage waveforms that are considerable different than a continuous design. The output pin (switch) waveform can have some damped sinusoidal ringing present. (See photo titled; Discontinuous Mode Switching Waveforms) This ringing is normal for discontinuous operation, and is not caused by feedback loop instabilities. In discontinuous operation, there is a period of time where neither the switch or the diode are conducting, and the inductor current has dropped to zero. During this time, a small amount of energy can circulate between the inductor and the switch/diode parasitic capacitance causing this characteristic ringing. Normally this ringing is not a problem, unless the amplitude becomes great enough to exceed the input voltage, and even then, there is very little energy present to cause damage.
Different inductor types and/or core materials produce different amounts of this characteristic ringing. Ferrite core inductors have very little core loss and therefore produce the most ringing. The higher core loss of powdered iron inductors produce less ringing. If desired, a series RC could be placed in parallel with the inductor to dampen the ringing. The computer aided design software Switchers Made Simple (version 4.1) will provide all component values for continuous and discontinuous modes of operation.


TL/H/12440-39
FIGURE 19. Post Ripple Filter Waveform

## OUTPUT VOLTAGE RIPPLE AND TRANSIENTS

The output voltage of a switching power supply operating in the continuous mode will contain a sawtooth ripple voltage at the switcher frequency, and may also contain short voltage spikes at the peaks of the sawtooth waveform.
The output ripple voltage is a function of the inductor sawtooth ripple current and the ESR of the output capacitor. A typical output ripple voltage can range from approximately $0.5 \%$ to $3 \%$ of the output voltage. To obtain low ripple voltage, the ESR of the output capacitor must be low, however, caution must be exercised when using extremely low ESR capacitors because they can affect the loop stability, resulting in oscillation problems. If very low output ripple voltage is needed (less than 15 mV ), a post ripple filter is recommended. (See Figure 12.) The inductance required is typically between $1 \mu \mathrm{H}$ and $5 \mu \mathrm{H}$, with low DC resistance, to maintain good load regulation. A low ESR output filter capacitor is also required to assure good dynamic load response and ripple reduction. The ESR of this capacitor may be as low as desired, because it is out of the regulator feedback loop. The photo shown in Figure 19 shows a typical output ripple voltage, with and without a post ripple filter.
When observing output ripple with a scope, it is essential that a short, low inductance scope probe ground connection be used. Most scope probe manufacturers provide a special probe terminator which is soldered onto the regulator board, preferable at the output capacitor. This provides a very short scope ground thus eliminating the problems associated with the 3 inch ground lead normally provided with the probe, and provides a much cleaner and more accurate picture of the ripple voltage waveform.
The voltage spikes are caused by the fast switching action of the output switch, the diode, and the parasitic inductance of the output filter capacitor, and its associated wiring. To minimize these voltage spikes, the output capacitor should be designed for switching regulator applications, and the lead lengths must be kept very short. Wiring inductance, stray capacitance, as well as the scope probe used to evaluate these transients, all contribute to the amplitude of these spikes.


TL/H/12440-40
FIGURE 20. Peak-to-Peak Inductor Ripple Current vs Load Current

## Application Information (Continued)

When a switching regulator is operating in the continuous mode, the inductor current waveform ranges from a triangular to a sawtooth type of waveform (depending on the input voltage). For a given input and output voltage, the peak-topeak amplitude of this inductor current waveform remains constant. As the load current increases or decreases, the entire sawtooth current waveform also rises and falls. The average value (or the center) of this current waveform is equal to the DC load current.
If the load current drops to a low enough level, the bottom of the sawtooth current waveform will reach zero, and the switcher will smoothly change from a continuous to a discontinuous mode of operation. Most switcher designs (irregardless how large the inductor value is) will be forced to run discontinuous if the output is lightly loaded. This is a perfectly acceptable mode of operation.
In a switching regulator design, knowing the value of the peak-to-peak inductor ripple current ( $\Delta l_{\text {IND }}$ ) can be useful for determining a number of other circuit parameters. Parameters such as, peak inductor or peak switch current, minimum load current before the circuit becomes discontinuous, output ripple voltage and output capacitor ESR can all be calculated from the peak-to-peak $\Delta I_{\text {IND }}$. When the inductor nomographs shown in Figures 3 through 6 are used to select an inductor value, the peak-to-peak inductor ripple current can immediately be determined. The curve shown in Figure 20 shows the range of $\left(\Delta \|_{\text {IND }}\right)$ that can be expected for different load currents. The curve also shows how the peak-to-peak inductor ripple current ( $\Delta l_{\text {IND }}$ ) changes as you go from the lower border to the upper border (for a given load current) within an inductance region. The upper border represents a higher input voltage, while the lower border represents a lower input voltage (see Inductor Selection Guides).
These curves are only correct for continuous mode operation, and only if the inductor selection guides are used to select the inductor value
Consider the following example:
$\mathrm{V}_{\mathrm{OUT}}=5 \mathrm{~V}$, maximum load current of 300 mA
$\mathrm{~V}_{\text {IN }}=15 \mathrm{~V}$, nominal, varying between 11 V and 20 V.

The selection guide in Figure 4 shows that the vertical line for a 0.3A load current, and the horizontal line for the 15 V input voltage intersect approximately midway between the upper and lower borders of the $150 \mu \mathrm{H}$ inductance region. A $150 \mu \mathrm{H}$ inductor will allow a peak-to-peak inductor current ( $\Delta I_{\text {IND }}$ ) to flow that will be a percentage of the maximum load current. Referring to Figure 20, follow the 0.3A line approximately midway into the inductance region, and read the peak-to-peak inductor ripple current ( $\Delta l_{\text {IND }}$ ) on the left hand axis (approximately $150 \mathrm{~mA} p-\mathrm{p}$ ).
As the input voltage increases to 20 V , it approaches the upper border of the inductance region, and the inductor ripple current increases. Referring to the curve in Figure 20, it can be seen that for a load current of 0.3A, the peak-topeak inductor ripple current ( $\Delta I_{\mathrm{IND}}$ ) is 150 mA with 15 V in, and can range from 175 mA at the upper border ( 20 V in ) to 120 mA at the lower border ( 11 V in ).

Once the $\Delta l_{\text {IND }}$ value is known, the following formulas can be used to calculate additional information about the switching regulator circuit.

1. Peak Inductor or peak switch current

$$
=\left(\mathrm{I}_{\mathrm{LOAD}}+\frac{\Delta \mathrm{l}_{\mathrm{IND}}}{2}\right)=\left(0.3 \mathrm{~A}+\frac{0.150}{2}\right)=0.375 \mathrm{~A}
$$

2. Minimum load current before the circuit becomes discontinuous

$$
=\frac{\Delta l_{\mathrm{IND}}}{2}=\frac{0.150}{2}=0.075 \mathrm{~A}
$$

$$
\text { 3. Output Ripple Voltage }=\left(\Delta I_{\text {IND }}\right) \times(\text { ESR of COUT })
$$

$$
=0.150 \mathrm{~A} \times 0.240 \Omega=36 \mathrm{mV} \mathrm{p}-\mathrm{p}
$$

4. ESR of $\mathrm{C}_{\text {OUT }}=\frac{\text { Output Ripple Voltage }\left(\Delta \mathrm{V}_{\text {OUT }}\right)}{\Delta \mathrm{I}_{\text {IND }}}$

$$
=\frac{0.036 \mathrm{~V}}{0.150 \mathrm{~A}}=0.240 \Omega
$$

## OPEN CORE INDUCTORS

Another possible source of increased output ripple voltage or unstable operation is from an open core inductor. Ferrite bobbin or stick inductors have magnetic lines of flux flowing through the air from one end of the bobbin to the other end. These magnetic lines of flux will induce a voltage into any wire or PC board copper trace that comes within the inductor's magnetic field. The strength of the magnetic field, the orientation and location of the PC copper trace to the magnetic field, and the distance between the copper trace and the inductor, determine the amount of voltage generated in the copper trace. Another way of looking at this inductive coupling is to consider the PC board copper trace as one turn of a transformer (secondary) with the inductor winding as the primary. Many millivolts can be generated in a copper trace located near an open core inductor which can cause stability problems or high output ripple voltage problems.
If unstable operation is seen, and an open core inductor is used, it's possible that the location of the inductor with respect to other PC traces may be the problem. To determine if this is the problem, temporarily raise the inductor away from the board by several inches and then check circuit operation. If the circuit now operates correctly, then the magnetic flux from the open core inductor is causing the problem. Substituting a closed core inductor such as a torroid or E-core will correct the problem, or re-arranging the PC layout may be necessary. Magnetic flux cutting the IC device ground trace, feedback trace, or the positive or negative traces of the output capacitor should be minimized.
Sometimes, locating a trace directly beneath a bobbin inductor will provide good results, provided it is exactly in the center of the inductor (because the induced voltages cancel themselves out), but if it is off center one direction or the other, then problems could arise. If flux problems are present, even the direction of the inductor winding can make a difference in some circuits.
This discussion on open core inductors is not to frighten the user, but to alert the user on what kind of problems to watch out for when using them. Open core bobbin or "stick" inductors are an inexpensive, simple way of making a compact efficient inductor, and they are used by the millions in many different applications.

## Application Information (Continued)



TL/H/12440-41

| Circuit Data for Temperature Rise Curve (DIP-8) |  |
| :--- | :--- |
| Capacitors | Through hole electrolytic |
| Inductor | Through hole, Schott, 100 $\mu \mathrm{H}$ |
| Diode | Through hole, 1A 40V, Schottky |
| PC board | 4 square inches single sided 2 oz. copper <br> $\left(0.0028^{\prime \prime}\right)$ |

FIGURE 21. Junction Temperature Rise, DIP-8


TL/H/12440-42

| Circuit Data for Temperature Rise Curve (Surface Mount) |  |
| :--- | :--- |
| Capacitors | Surface mount tantalum, molded "D" size |
| Inductor | Surface mount, Coilcraft DO33, 100 $\mu \mathrm{H}$ |
| Diode | Surface mount, 1A 40V, Schottky |
| PC board | 4 square inches single sided 2 oz. copper <br> $(0.0028$ " $)$ |

FIGURE 22. Junction Temperature Rise, SO-8

## THERMAL CONSIDERATIONS

The LM2597 is available in two packages, an 8-pin through hole DIP ( N ) and an 8-pin surface mount SO-8 (M). Both packages are molded plastic with a copper lead frame. When the package is soldered to the PC board, the copper and the board are the heat sink for the LM2597 and the other heat producing components.

For best thermal performance, wide copper traces should be used. Pins should be soldered to generous amounts of printed circuit board copper, (one exception to this is the output (switch) pin, which should not have large areas of copper). Large areas of copper provide the best transfer of heat (lower thermal resistance) to the surrounding air, and even double-sided or multilayer boards provide a better heat path to the surrounding air. Unless power levels are small, sockets are not recommended because of the added thermal resistance it adds and the resultant higher junction temperatures.
Package thermal resistance and junction temperature rise numbers are all approximate, and there are many factors that will affect the junction temperature. Some of these factors include board size, shape, thickness, position, location, and even board temperature. Other factors are, trace width, printed circuit copper area, copper thickness, single- or dou-ble-sided, multilayer board, and the amount of solder on the board. The effectiveness of the PC board to dissipate heat also depends on the size, quantity and spacing of other components on the board. Furthermore, some of these components such as the catch diode will add heat to the PC board and the heat can vary as the input voltage changes. For the inductor, depending on the physical size, type of core material and the DC resistance, it could either act as a heat sink taking heat away from the board, or it could add heat to the board.
The curves shown in Figures 21 and 22 show the LM2597 junction temperature rise above ambient temperature with a 500 mA load for various input and output voltages. The Bias Supply pin was not used (left open) for these curves. Connecting the Bias Supply pin to the output voltage would reduce the junction temperature by approximately $5^{\circ} \mathrm{C}$ to $15^{\circ} \mathrm{C}$, depending on the input and output voltages, and the load current. This data was taken with the circuit operating as a buck switcher with all components mounted on a PC board to simulate the junction temperature under actual operating conditions. This curve is typical, and can be used for a quick check on the maximum junction temperature for various conditions, but keep in mind that there are many factors that can affect the junction temperature.

## BIAS SUPPLY FEATURE

The bias supply ( $\mathrm{V}_{\mathrm{BS}}$ ) pin allows the LM2597's internal circuitry to be powered from a power source, other than $V_{I N}$, typically the output voltage. This feature can increase efficiency and lower junction temperatures under some operating conditions. The greatest increase in efficiency occur with light load currents, high input voltage and low output voltage ( 4 V to 12V). See efficiency curves shown in Figures 23 and 24. The curves with solid lines are with the $\mathrm{V}_{\mathrm{BS}}$ pin connected to the regulated output voltage, while the curves with dashed lines are with the $\mathrm{V}_{\mathrm{BS}}$ pin open.
The bias supply pin requires a minimum of approximately 3.5 V at room temperature ( 4 V @ $-40^{\circ} \mathrm{C}$ ), and can be as high as 30 V , but there is little advantage of using the bias supply feature with voltages greater than 15 V or 20 V . The current required for the $\mathrm{V}_{\mathrm{IN}}$ pin is typically 4 mA .
To use the bias supply feature with output voltages between 4 V and 15 V , wire the bias pin to the regulated output. Since the $\mathrm{V}_{\mathrm{BS}}$ pin requires a minimum of 4 V to operate, the 3.3 V part cannot be used this way. When the $\mathrm{V}_{\mathrm{BS}}$ pin is left open, the intemal regulator circuitry is powered from the input voltage.

## Application Information (Continued)



TL/H/12440-43
FIGURE 23. Effects of Bias Supply Feature on 5V Regulator Efficiency


TL/H/12440-45
FIGURE 24. Effects of Bias Supply Feature on 12V Regulator Efficiency

## SHUTDOWN/SOFT-START

The circuit shown in Figure 25 is a standard buck regulator with 24 V in, 12 V out, 100 mA load, and using a $0.068 \mu \mathrm{~F}$ Soft-start capacitor. The photo in Figures 26 and 27 show the effects of Soft-start on the output voltage, the input current, with, and without a Soft-start capacitor. Figure 26 also shows the error flag output going high when the output voltage reaches $95 \%$ of the nominal output voltage. The reduced input current required at startup is very evident when comparing the two photos. The Soft-start feature reduces


TL/H/12440-44
FIGURE 26. Output Voltage, Input Current, Error Flag Signal, at Start-Up, WITH Soft-start


FIGURE 27. Output Voltage, Input Current, at Start-Up, WITHOUT Soft-start
the startup current from 700 mA down to 160 mA , and delays and slows down the output voltage rise time.
This reduction in start up current is useful in situations where the input power source is limited in the amount of current it can deliver. In some applications Soft-start can be used to replace undervoltage lockout or delayed startup functions.
If a very slow output voltage ramp is desired, the Soft-start capacitor can be made much larger. Many seconds or even minutes are possible.
If only the shutdown feature is needed, the Soft-start capacitor can be eliminated.


## Application Information (Continued)



## INVERTING REGULATOR

The circuit in Figure 28 converts a positive input voltage to a negative output voltage with a common ground. The circuit operates by bootstrapping the regulators ground pin to the negative output voltage, then grounding the feedback pin, the regulator senses the inverted output voltage and regulates it.
This example uses the LM2597-5 to generate a -5 V output, but other output voltages are possible by selecting other output voltage versions, including the adjustable version. Since this regulator topology can produce an output voltage that is either greater than or less than the input voltage, the maximum output current greatly depends on both the input and output voltage. The curve shown in Figure 29 provides a guide as to the amount of output load current possible for the different input and output voltage conditions.
The maximum voltage appearing across the regulator is the absolute sum of the input and output voltage, and this must be limited to a maximum of 40 V . In this example, when converting +20 V to -5 V , the regulator would see 25 V between the input pin and ground pin. The LM2597 has a maximum input voltage rating of 40 V .


TL/H/12440-49
FIGURE 29. Maximum Load Current for Inverting Regulator Circuit

An additional diode is required in this regulator configuration. Diode D1 is used to isolate input voltage ripple or noise from coupling through the $\mathrm{C}_{I N}$ capacitor to the output, under light or no load conditions. Also, this diode isolation changes the topology to closely resemble a buck configuration thus providing good closed loop stability. A Schottky diode is recommended for low input voltages, (because of its lower voltage drop) but for higher input voltages, a 1N4001 diode could be used.
Because of differences in the operation of the inverting regulator, the standard design procedure is not used to select the inductor value. In the majority of designs, a $100 \mu \mathrm{H}$, 1 Amp inductor is the best choice. Capacitor selection can also be narrowed down to just a few values. Using the values shown in Figure 28 will provide good results in the majority of inverting designs.
This type of inverting regulator can require relatively large amounts of input current when starting up, even with light loads. Input currents as high as the LM2597 current limit (approximately 0.8 A ) are needed for 1 ms or more, until the output reaches its nominal output voltage. The actual time depends on the output voltage and the size of the output capacitor. Input power sources that are current limited or sources that can not deliver these currents without getting loaded down, may not work correctly. Because of the relatively high startup currents required by the inverting topology, the Soft-start feature shown in Figure 28 is recommended.
Also shown in Figure 28 are several shutdown methods for the inverting configuration. With the inverting configuration, some level shifting is required, because the ground pin of the regulator is no longer at ground, but is now at the negative output voltage. The shutdown methods shown accept ground referenced shutdown signals.

## Application Information (Continued)

## undervoltage lockout

Some applications require the regulator to remain off until the input voltage reaches a predetermined voltage. Figure 30 contains a undervoltage lockout circuit for a buck configuration, while Figures 31 and 32 are for the inverting types (only the circuitry pertaining to the undervoltage lockout is shown). Figure 30 uses a zener diode to establish the threshold voltage when the switcher begins operating. When the input voltage is less than the zener voltage, resistors R1 and R2 hold the Shutdown/Soft-start pin low, keeping the regulator in the shutdown mode. As the input voltage exceeds the zener voltage, the zener conducts, pulling the Shutdown/Soft-start pin high, allowing the regulator to begin switching. The threshold voltage for the undervoltage lockout feature is approximately 1.5 V greater than the zener voltage.


TL/H/12440-50
FIGURE 30. Undervoltage Lockout for a Buck Regulator
Figures 31 and 32 apply the same feature to an inverting circuit. Figure 31 features a constant threshold voltage for turn on and turn off (zener voltage plus approximately one volt). If hysteresis is needed, the circuit in Figure 32 has a turn ON voltage which is different than the turn OFF voltage. The amount of hysteresis is approximately equal to the value of the output voltage. Since the $\overline{\mathrm{SD}} / \mathrm{SS}$ pin has an internal 7 V zener clamp, R2 is needed to limit the current into this pin to approximately 1 mA when Q1 is on.


TL/H/12440-52
FIGURE 31. Undervoltage Lockout Without Hysteresis for an Inverting Regulator


FIGURE 32. Undervoltage Lockout With Hysteresis for an Inverting Regulator

## NEGATIVE VOLTAGE CHARGE PUMP

Occasionally a low current negative voltage is needed for biasing parts of a circuit. A simple method of generating a negative voltage using a charge pump technique and the switching waveform present at the OUT pin, is shown in Figure 33. This unregulated negative voltage is approximately equal to the positive input voltage (minus a few volts), and can supply up to a 100 mA of output current. There is a requirement however, that there be a minimum load of several hundred mA on the regulated positive output for the charge pump to work correctly. Also, resistor R1 is required to limit the charging current of C1 to some value less than the LM2597 current limit (typically 800 mA ).
This method of generating a negative output voltage without an additional inductor can be used with other members of the Simple Switcher Family, using either the buck or boost topology.


FIGURE 33. Charge Pump for Generating a Low Current, Negative Output Voltage

## Application Information (Continued)

 TYPICAL SURFACE MOUNT PC BOARD LAYOUT, FIXED OUTPUT (2X size)

TYPICAL SURFACE MOUNT PC BOARD LAYOUT, ADJUSTABLE OUTPUT (2X size)


FIGURE 34. 2X Printed Circuit Board Layout

## Physical Dimensions inches (millimeters)


LM2597 SIMPLE SWITCHER Power Converter

Physical Dimensions inches (millimeters) (Continued)


## LIFE SUPPORT POLICY

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| :---: | :---: | :---: | :---: |



Typical Application (Fixed Output Voltage Versions)


TL/H/12593-1
$\dagger$ Patent Number 5,382,918.
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## Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required please contact the National Semiconductor Sales Office/Distributors for availability and specifications.
Maximum Supply Voltage ( $\mathrm{V}_{\mathrm{IN}}$ ) 45V
$\overline{\text { SD/SS Pin Input Voltage (Note 2) 6V }}$
Delay Pin Voltage (Note 2) 1.5V
Flag Pin Voltage $\quad-0.3 \leq \mathrm{V} \leq 45 \mathrm{~V}$
Feedback Pin Voltage $\quad-0.3 \leq \mathrm{V} \leq+25 \mathrm{~V}$
Output Voltage to Ground (Steady State) -1V
Power Dissipation
Internally limited
Storage Temperature Range $\quad-65^{\circ} \mathrm{C}$ to $+150^{\circ} \mathrm{C}$
ESD Susceptibility
Human Body Model (Note 3) 2 kV

| Lead Temperature |  |
| :--- | :--- |
| S Package |  |
| $\quad$ Vapor Phase ( 60 sec.) | $+215^{\circ} \mathrm{C}$ |
| Infrared (10 sec.) | $+245^{\circ} \mathrm{C}$ |
| T Package (Soldering, 10 sec.) | $+260^{\circ} \mathrm{C}$ |
| Maximum Junction Temperature | $+150^{\circ} \mathrm{C}$ |

Operating Conditions
Temperature Range $\quad-25^{\circ} \mathrm{C} \leq \mathrm{T}_{\mathrm{J}}+125^{\circ} \mathrm{C}$
Supply Voltage 4.5 V to 40 V

## LM2598-3.3

Electrical Characteristics Specifications with standard type face are for $\mathrm{T}_{\mathrm{J}}=25^{\circ} \mathrm{C}$, and those with boldface type apply over full Operating Temperature Range.

| Symbol | Parameter | Conditions | LM2598-3.3 |  | Units (Limits) |
| :---: | :---: | :---: | :---: | :---: | :---: |
|  |  |  | Typ (Note 4) | Limit (Note 5) |  |
| SYSTEM PARAMETERS (Note 6) Test Circuit Figure 1 |  |  |  |  |  |
| V OUT | Output Voltage | $4.75 \mathrm{~V} \leq \mathrm{V}_{\mathrm{IN}} \leq 40 \mathrm{~V}, 0.1 \mathrm{~A} \leq \mathrm{I}_{\text {LOAD }} \leq 1 \mathrm{~A}$ | 3.3 | $\begin{aligned} & 3.168 / \mathbf{3 . 1 3 5} \\ & 3.432 / \mathbf{3 . 4 6 5} \end{aligned}$ |  |
| $\eta$ | Efficiency | $\mathrm{V}_{\text {IN }}=12 \mathrm{~V}, \mathrm{I}_{\text {LOAD }}=1 \mathrm{~A}$ | 78 |  | \% |

LM2598-5.0
Electrical Characteristics Specifications with standard type face are for $\mathrm{T}_{\mathrm{J}}=25^{\circ} \mathrm{C}$, and those with boldface type apply over full Operating Temperature Range.

| Symbol | Parameter | Conditions | LM2598-5.0 |  | Units (Limits) |
| :---: | :---: | :---: | :---: | :---: | :---: |
|  |  |  | $\begin{gathered} \text { Typ } \\ \text { (Note 4) } \end{gathered}$ | Limit (Note 5) |  |
| SYSTEM PARAMETERS (Note 6) Test Circuit Figure 1 |  |  |  |  |  |
| $\mathrm{V}_{\text {OUT }}$ | Output Voltage | $7 \mathrm{~V} \leq \mathrm{V}_{\text {IN }} \leq 40 \mathrm{~V}, 0.1 \mathrm{~A} \leq \mathrm{I}_{\text {LOAD }} \leq 1 \mathrm{~A}$ | 5 | $\begin{aligned} & 4.800 / 4.750 \\ & 5.200 / \mathbf{5 . 2 5 0} \end{aligned}$ | $V(\min )$ <br> V (max) |
| $\eta$ | Efficiency | $\mathrm{V}_{\text {IN }}=12 \mathrm{~V}, \mathrm{I}_{\text {LOAD }}=1 \mathrm{~A}$ | 82 |  | \% |

LM2598-12
Electrical Characteristics Specifications with standard type face are for $\mathrm{T}_{\mathrm{J}}=25^{\circ} \mathrm{C}$, and those with boldface type apply over full Operating Temperature Range.

| Symbol | Parameter | Conditions | LM2598-12 |  | Units |
| :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | Typ <br> (Note 4) | Limit <br> (Note 5) |  |  |

SYSTEM PARAMETERS (Note 6) Test Circuit Figure 1

| $V_{\text {OUT }}$ | Output Voltage | $15 \mathrm{~V} \leq \mathrm{V}_{\mathrm{IN}} \leq 40 \mathrm{~V}, 0.1 \mathrm{~A} \leq \mathrm{I}_{\text {LOAD }} \leq 1 \mathrm{~A}$ | 12 |  | V |
| :--- | :--- | :--- | :---: | :---: | :---: |
|  |  |  |  | $11.52 / \mathbf{1 1 . 4 0}$ <br> $12.48 / \mathbf{1 2 . 6 0}$ | $\mathrm{V}(\mathrm{min})$ <br> $(\mathrm{max})$ |
| $\eta$ | Efficiency | $\mathrm{V}_{\text {IN }}=25 \mathrm{~V}, \mathrm{I}_{\text {LOAD }}=1 \mathrm{~A}$ | 90 |  | $\%$ |


| Electrical Characteristics Specifications with standard type face are for $\mathrm{T}_{\mathrm{J}}=25^{\circ} \mathrm{C}$, and those with boldface type apply over full Operating Temperature Range. |  |  |  |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: |
|  |  |  |  | 98-ADJ |  |
| Symbol | Parameter | Conditions | $\begin{gathered} \text { Typ } \\ \text { (Note 4) } \end{gathered}$ | $\begin{aligned} & \text { Limit } \\ & \text { (Note 5) } \end{aligned}$ | (Limits) |
| SYSTEM PARAMETERS (Note 6) Test Circuit Figure 1 |  |  |  |  |  |
| $\mathrm{V}_{\text {FB }}$ | Feedback Voltage | $\begin{aligned} & 4.5 \mathrm{~V} \leq \mathrm{V}_{\mathbb{I N}} \leq 40 \mathrm{~V}, 0.1 \mathrm{~A} \leq \mathrm{I} \text { LOAD } \leq 1 \mathrm{~A} \\ & \mathrm{~V}_{\text {OUT }} \text { programmed for } 3 \mathrm{~V} \text {. Circuit of Figure } 12 . \end{aligned}$ | 1.230 | $\begin{aligned} & 1.193 / \mathbf{1 . 1 8 0} \\ & 1.267 / \mathbf{1 . 2 8 0} \end{aligned}$ | $\begin{gathered} \mathrm{V} \\ \mathrm{~V}(\mathrm{~min}) \end{gathered}$ $\mathrm{V}(\text { max })$ |
| $\eta$ | Efficiency | $\mathrm{V}_{\text {IN }}=12 \mathrm{~V}, \mathrm{~V}_{\text {OUT }}=3 \mathrm{~V}, \mathrm{~L}$ LOAD $=1 \mathrm{~A}$ | 78 |  | \% |

## All Output Voltage Versions

Electrical Characteristics Specifications with standard type face are for $\mathrm{T}_{J}=25^{\circ} \mathrm{C}$, and those with boldface type apply over full Operating Temperature Range. Unless otherwise specified, $\mathrm{V}_{\mathrm{IN}}=12 \mathrm{~V}$ for the $3.3 \mathrm{~V}, 5 \mathrm{~V}$, and Adjustable version and $\mathrm{V}_{\mathrm{IN}}=24 \mathrm{~V}$ for the 12 V version. ILOAD $=200 \mathrm{~mA}$

| Symbol |  |  |  | Parameter | Conditions |
| :---: | :---: | :---: | :---: | :---: | :---: |

DEVICE PARAMETERS

| $\mathrm{l}_{\mathrm{b}}$ | Feedback Bias Current | Adjustable Version Only, $\mathrm{V}_{\mathrm{FB}}=1.3 \mathrm{~V}$ | 10 | 50/100 | $\begin{gathered} \mathrm{nA} \\ \mathrm{nA}(\mathrm{max}) \end{gathered}$ |
| :---: | :---: | :---: | :---: | :---: | :---: |
| $\mathrm{f}_{\mathrm{O}}$ | Oscillator Frequency | (Note 7) | 150 | $\begin{aligned} & 127 / \mathbf{1 1 0} \\ & 173 / \mathbf{1 7 3} \end{aligned}$ | $\begin{gathered} \mathrm{kHz} \\ \mathrm{kHz}(\min ) \\ \mathrm{kHz}(\max ) \\ \hline \end{gathered}$ |
| $\mathrm{V}_{\text {SAT }}$ | Saturation Voltage | IOUT $=1 \mathrm{~A}($ Notes 8 and 9) | 1 | 1.2/1.3 | $\begin{gathered} V \\ \mathrm{~V}(\max ) \\ \hline \end{gathered}$ |
| DC | Max Duty Cycle (ON) Min Duty Cycle (OFF) | (Note 9) (Note 10) | $\begin{gathered} 100 \\ 0 \end{gathered}$ |  | \% |
| $\mathrm{I}_{\mathrm{CL}}$ | Current Limit | Peak Current, (Notes 8 and 9) | 1.5 | $\begin{gathered} 1.2 / \mathbf{1 . 1 5} \\ 2.4 / \mathbf{2 . 6} \end{gathered}$ | A A(min) A(max) |
| $\mathrm{I}_{\mathrm{L}}$ | Output Leakage Current | $\begin{array}{ll} (\text { Notes } 8,10 \text { and 11) } & \text { Output }=0 \mathrm{~V} \\ & \text { Output }=-1 \mathrm{~V} \end{array}$ | 2 | $\begin{aligned} & 50 \\ & 15 \end{aligned}$ | $\begin{gathered} \mu \mathrm{A}(\max ) \\ \mathrm{mA} \\ \mathrm{~mA}(\max ) \end{gathered}$ |
| $\mathrm{I}_{\mathrm{Q}}$ | Operating Quiescent Current | $\overline{\text { SD/ SS Pin Open, (Note 10) }}$ | 5 | 10 | $\begin{gathered} \mathrm{mA} \\ \mathrm{~mA}(\max ) \end{gathered}$ |
| ISTBY | Standby Quiescent Current | $\overline{\mathrm{SD}} / \mathrm{SS}$ pin $=0 \mathrm{~V},($ Note 11$)$ | 85 | 200/250 | $\begin{gathered} \mu \mathrm{A} \\ \mu \mathrm{~A}(\max ) \end{gathered}$ |
| $\theta_{\mathrm{JC}}$ <br> $\theta_{\mathrm{JA}}$ <br> $\theta_{J A}$ <br> $\theta_{J A}$ <br> $\theta_{\text {JA }}$ | Thermal Resistance | TO220 or TO263 Package, Junction to Case TO220 Package, Junction to Ambient (Note 12) TO263 Package, Junction to Ambient (Note 13) TO263 Package, Junction to Ambient (Note 14) TO263 Package, Junction to Ambient (Note 15) | $\begin{gathered} 2 \\ 50 \\ 50 \\ 30 \\ 20 \end{gathered}$ |  | ${ }^{\circ} \mathrm{C} / \mathrm{W}$ <br> ${ }^{\circ} \mathrm{C} / \mathrm{W}$ <br> ${ }^{\circ} \mathrm{C} / \mathrm{W}$ <br> ${ }^{\circ} \mathrm{C} / \mathrm{W}$ <br> ${ }^{\circ} \mathrm{C} / \mathrm{W}$ |

## All Output Voltage Versions (Continued)

Electrical Characteristics Specifications with standard type face are for $\mathrm{T}_{\mathrm{J}}=25^{\circ} \mathrm{C}$, and those with boldface type apply over full Operating Temperature Range. Unless otherwise specified, $\mathrm{V}_{\mathrm{IN}}=12 \mathrm{~V}$ for the $3.3 \mathrm{~V}, 5 \mathrm{~V}$, and Adjustable version and $\mathrm{V}_{\mathrm{IN}}=24 \mathrm{~V}$ for the 12 V version. ILOAD $=200 \mathrm{~mA}$

| Symbol | Parameter | Conditions | LM2598-XX |  | Units (Limits) |
| :---: | :---: | :---: | :---: | :---: | :---: |
|  |  |  |  | Limit (Note 5) |  |
| SHUTDOWN/SOFT-START CONTROL Test Circuit of Figure 1 |  |  |  |  |  |
| $\mathrm{V}_{\text {SD }}$ | Shutdown Threshold Voltage | Low, (Shutdown Mode) High, (Soft-start Mode) | 1.3 | $\begin{gathered} 0.6 \\ 2 \end{gathered}$ | V <br> V (max) <br> $\mathrm{V}(\min )$ |
| $\mathrm{V}_{\text {SS }}$ | Soft-start Voltage | $V_{\text {OUT }}=20 \%$ of Nominal Output Voltage <br> $V_{\text {OUT }}=100 \%$ of Nominal Output Voltage | $\begin{aligned} & 2 \\ & 3 \\ & \hline \end{aligned}$ |  | V |
| ${ }^{\text {ISD }}$ | Shutdown Current | $\mathrm{V}_{\overline{\text { SHUTDOWN }}}=0.5 \mathrm{~V}$ | 5 | 10 | $\begin{gathered} \mu \mathrm{A} \\ \mu \mathrm{~A}(\max ) \end{gathered}$ |
| Iss | Soft-start Current | $\mathrm{V}_{\text {Soft-start }}=2.5 \mathrm{~V}$ | 1.6 | 5 | $\begin{gathered} \mu \mathrm{A} \\ \mu \mathrm{~A}(\max ) \end{gathered}$ |

FLAG/DELAY CONTROL Test Circuit of Figure 1

|  | Regulator Dropout Detector Threshold Voltage | Low (Flag ON) | 96 | $\begin{aligned} & 92 \\ & 98 \end{aligned}$ | $\begin{gathered} \% \\ \%(\min ) \\ \%(\max ) \\ \hline \end{gathered}$ |
| :---: | :---: | :---: | :---: | :---: | :---: |
| VFSAT | Flag Output Saturation Voltage | $\begin{aligned} & \mathrm{I}_{\mathrm{SINK}}=3 \mathrm{~mA} \\ & \mathrm{~V}_{\text {DELAY }}=0.5 \mathrm{~V} \end{aligned}$ | 0.3 | 0.7/1.0 | $\begin{gathered} \mathrm{V} \\ \mathrm{~V}(\max ) \\ \hline \end{gathered}$ |
| $\mathrm{IF}_{\mathrm{L}}$ | Flag Output Leakage Current | $\mathrm{V}_{\mathrm{FLAG}}=40 \mathrm{~V}$ | 0.3 |  | $\mu \mathrm{A}$ |
|  | Delay Pin Threshold Voltage | Low (Flag ON) <br> High (Flag OFF) and $\mathrm{V}_{\text {OUT }}$ Regulated | 1.25 | $\begin{aligned} & 1.21 \\ & 1.29 \end{aligned}$ |  |
|  | Delay Pin Source Current | $\mathrm{V}_{\text {DELAY }}=0.5 \mathrm{~V}$ | 3 | 6 | $\begin{gathered} \mu \mathrm{A} \\ \mu \mathrm{~A}(\max ) \end{gathered}$ |
|  | Delay Pin Saturation | Low (Flag ON) | 55 | 350/400 | $\begin{gathered} \mathrm{mV} \\ \mathrm{mV}(\max ) \end{gathered}$ |

## Electrical Characteristics (Continued)

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but do not guarantee specific performance limits. For guaranteed specifications and test conditions, see the Electrical Characteristics
Note 2: Voltage internally clamped. If clamp voltage is exceeded, limit current to a maximum of 1 mA .
Note 3: The human body model is a 100 pF capacitor discharged through a 1.5 k resistor into each pin.
Note 4: Typical numbers are at $25^{\circ} \mathrm{C}$ and represent the most likely norm.
Note 5: All limits guaranteed at room temperature (standard type face) and at temperature extremes (bold type face). All room temperature limits are 100\% production tested. All limits at temperature extremes are guaranteed via correlation using standard Statistical Quality Control (SQC) methods. All limits are used to calculate Average Outgoing Quality Level (AOQL).
Note 6: External components such as the catch diode, inductor, input and output capacitors can affect switching regulator system performance. When the LM2598 is used as shown in the Figure 1 test circuit, system performance will be as shown in system parameters section of Electrical Characteristics.
Note 7: The switching frequency is reduced when the second stage current limit is activated. The amount of reduction is determined by the severity of current overload.
Note 8: No diode, inductor or capacitor connected to output pin
Note 9: Feedback pin removed from output and connected to OV to force the output transistor switch ON.
Note 10: Feedback pin removed from output and connected to 12 V for the $3.3 \mathrm{~V}, 5 \mathrm{~V}$, and the ADJ. version, and 15 V for the 12 V version, to force the output transistor switch OFF.
Note 11: $\mathrm{V}_{\mathrm{IN}}=40 \mathrm{~V}$.
Note 12: Junction to ambient thermal resistance (no external heat sink) for the TO-220 package mounted vertically, with the leads soldered to a printed circuit board with ( 1 oz .) copper area of approximately $1 \mathrm{in}^{2}$.
Note 13: Junction to ambient thermal resistance with the TO-263 package tab soldered to a single sided printed circuit board with 0.5 in 2 of ( 1 oz .) copper area. Note 14: Junction to ambient thermal resistance with the TO-263 package tab soldered to a single sided printed circuit board with $2.5 \mathrm{in}{ }^{2}$ of ( 1 oz .) copper area. Note 15: Junction to ambient thermal resistance with the TO-263 package tab soldered to a double sided printed circuit board with 3 in ${ }^{2}$ of ( 1 oz .) copper area on the LM2598S side of the board, and approximately $16 \mathrm{in}^{2}$ of copper on the other side of the p-c board. See application hints in this data sheet and the thermal model in Switchers Made Simple version 4.2 software

## Typical Performance Characteristics (Circuit of Figure 1)



Switch Saturation Voltage


Line Regulation


TL/H/12593-3

Switch Current Limit


Efficiency


TL/H/12593-14


## Typical Performance Characteristics (Circuit of Figure 1)

Continuous Mode Switching Waveforms
$\mathrm{V}_{\text {IN }}=20 \mathrm{~V}, \mathrm{~V}_{\text {OUT }}=5 \mathrm{~V}, \mathrm{I}_{\text {LOAD }}=1 \mathrm{~A}$
$\mathrm{L}=68 \mu \mathrm{H}$, C OUt $=120 \mu \mathrm{~F}$, C OUt $\mathrm{ESR}=100 \mathrm{~m} \Omega$


A: Output Pin Voltage, $10 \mathrm{~V} /$ div.
B: Inductor Current 0.5A/div.
C: Output Ripple Voltage, $50 \mathrm{mV} / \mathrm{div}$.
Horizontal Time Base: $2 \mu \mathrm{~s} /$ div.

Load Transient Response for Continuous Mode
$\mathrm{V}_{\mathrm{IN}}=\mathbf{2 0 V}, \mathrm{V}_{\text {OUT }}=\mathbf{5 V}$, $\mathrm{I}_{\text {LOAD }}=\mathbf{2 5 0} \mathrm{mA}$ to 750 mA
$L=68 \mu \mathrm{H}$, C OUt $=120 \mu \mathrm{~F}$, C OUt ESR $=100 \mathrm{~m} \Omega$


Discontinuous Mode Switching Waveforms
$\mathrm{V}_{\text {IN }}=20 \mathrm{~V}, \mathrm{~V}_{\text {OUT }}=5 \mathrm{~V}, \mathrm{I}_{\text {LOAD }}=600 \mathrm{~mA}$
$\mathbf{L}=22 \mu \mathrm{H}$, C OUT $=220 \mu \mathrm{~F}$, C $_{\text {OUT }} \mathrm{ESR}=50 \mathrm{~m} \Omega$


A: Output Pin Voltage, $10 \mathrm{~V} / \mathrm{div}$.
B: Inductor Current $0.5 \mathrm{~A} /$ div.
C: Output Ripple Voltage, $50 \mathrm{mV} /$ div. Horizontal Time Base: $2 \mu \mathrm{~s} / \mathrm{div}$.

Load Transient Response for Discontinuous Mode $\mathrm{V}_{\mathrm{IN}}=\mathbf{2 0 V}, \mathrm{V}_{\text {OUT }}=\mathbf{5 V}$, $\mathrm{I}_{\text {LOAD }}=\mathbf{2 5 0} \mathrm{mA}$ to $\mathbf{7 5 0} \mathbf{~ m A}$ L $=\mathbf{2 2} \mu \mathrm{H}$, C OUT $=\mathbf{2 2 0} \mu \mathrm{F}$, C $_{\text {OUT }} \mathrm{ESR}=50 \mathrm{~m} \Omega$


A: Output Voltage, $100 \mathrm{mV} /$ div. (AC B: 250 mA to 750 mA Load Pulse Horizontal Time Base: $200 \mu \mathrm{~s} /$ div.

Connection Diagrams and Order Information

Bent and Staggered Leads, Through Hole Package 7-Lead TO-220 (T)


TL/H/12593-50
Order Number LM2598T-3.3, LM2598T-5.0, LM2598T-12 or LM2598T-ADJ See NS Package Number TA07B

Surface Mount Package 7-Lead TO-263 (S)


TL/H/12593-22
Order Number LM2598S-3.3, LM2598S-5.0,
LM2598S-12 or LM2598S-ADJ
See NS Package Number TS7B

## Test Circuit and Layout Guidelines



```
Component Values shown are for }\mp@subsup{\textrm{V}}{IN}{}=15\textrm{V}\mathrm{ ,
V
C}\mp@subsup{\textrm{C}}{\textrm{N}}{}-120\mu\textrm{F},50\textrm{V}\mathrm{ , Aluminum Electrolytic
    Nichicon "PL Series"
COUT - 120 \muF, 35V Aluminum Electrolytic,
    Nichicon "PL Series"
D1 - 3A, 40V Schottky Rectifier, 1N5822
L1 - 68 \muH,L30
```

Typical Values
CSS $\quad-0.1 \mu \mathrm{~F}$


TL/H/12593-24
$V_{\text {OUT }}=V_{\text {REF }}\left(1+\frac{R_{2}}{R_{1}}\right) \quad$ where $V_{\text {REF }}=1.23 V$
$R_{2}=R_{1}\left(\frac{V_{\text {OUT }}}{V_{\text {REF }}}-1\right) \quad \begin{aligned} & \text { Select } R_{1} \text { to be approximately } 1 \mathrm{k} \Omega, \\ & \text { use a } 1 \% \text { resistor for best stability. }\end{aligned}$
Component Values shown are for $\mathrm{V}_{\mathrm{IN}}=20 \mathrm{~V}$,
$V_{\text {OUT }}=10 \mathrm{~V}$, I LOAD $=1 \mathrm{~A}$.
$\mathrm{C}_{\mathrm{IN}}-120 \mu \mathrm{~F}, 35 \mathrm{~V}$, Aluminum Electrolytic Nichicon "PL Series"
Cout - $120 \mu \mathrm{~F}, 35 \mathrm{~V}$ Aluminum Electrolytic, Nichicon "PL Series"

D1 - 3A, 40V Schottky Rectifier, 1N5822
L1 - $100 \mu \mathrm{H}$, L29
$R_{1}-1 \mathrm{k} \Omega, 1 \%$
$R_{2}-7.15 \mathrm{k}, 1 \%$
$C_{F F}-3.3 \mathrm{nF}$, See Application Information Sec-
tion
$R_{\text {FF }}-3 \mathrm{k} \Omega$, See Application Information Section
Typical Values
$\mathrm{C}_{S S}-0.1 \mu \mathrm{~F}$
$C_{\text {DELAY }}-0.1 \mu \mathrm{~F}$
RPULL UP-4.7k

## FIGURE 1. Standard Test Circuits and Layout Guides

As in any switching regulator, layout is very important. Rapidly switching currents associated with wiring inductance can generate voltage transients which can cause problems. For minimal inductance and ground loops, the wires indicated by heavy lines should be wide printed circuit traces and should be kept as short as possible. For best results, external components should be located as close to the switcher IC as possible using ground plane construction or single point grounding.

If open core inductors are used, special care must be taken as to the location and positioning of this type of inductor. Allowing the inductor flux to intersect sensitive feedback, IC groundpath and Cout wiring can cause problems. When using the adjustable version, special care must be taken as to the location of the feedback resistors and the associated wiring. Physically locate both resistors near the IC, and route the wiring away from the inductor, especially an open core type of inductor. (See application section for more information.)

## LM2598 Series Buck Regulator Design Procedure (Fixed Output)

| PROCEDURE (Fixed Output Voltage Version) |
| :--- |
| Given: |
| $\mathrm{V}_{\text {OUT }}=$ Regulated Output Voltage $(3.3 \mathrm{~V}, 5 \mathrm{~V}$ or 12 V$)$ |
| $\mathrm{V}_{\text {IN }}(\max )=$ Maximum DC Input Voltage |
| ILOAD $^{\text {(max })}=$ Maximum Load Current |

1. Inductor Selection (L1)
A. Select the correct inductor value selection guide from Figures 4, 5, or 6 . (Output voltages of $3.3 \mathrm{~V}, 5 \mathrm{~V}$, or 12 V respectively.) For all other voltages, see the design procedure for the adjustable version.
B. From the inductor value selection guide, identify the inductance region intersected by the Maximum Input Voltage line and the Maximum Load Current line. Each region is identified by an inductance value and an inductor code (LXX).
C. Select an appropriate inductor from the four manufacturer's part numbers listed in Figure 8.
2. Output Capacitor Selection (COUT)
A. In the majority of applications, low ESR (Equivalent Series Resistance) electrolytic capacitors between $47 \mu \mathrm{~F}$ and $330 \mu \mathrm{~F}$ and low ESR solid tantalum capacitors between $56 \mu \mathrm{~F}$ and $270 \mu \mathrm{~F}$ provide the best results. This capacitor should be located close to the IC using short capacitor leads and short copper traces. Do not use capacitors larger than $330 \mu \mathrm{~F}$.
For additional information, see section on output capacitors in application information section.
B. To simplify the capacitor selection procedure, refer to the quick design component selection table shown in Figure 2. This table contains different input voltages, output voltages, and load currents, and lists various inductors and output capacitors that will provide the best design solutions.
C. The capacitor voltage rating for electrolytic capacitors should be at least 1.5 times greater than the output voltage, and often much higher voltage ratings are needed to satisfy the low ESR requirements for low output ripple voltage.
D. For computer aided design software, see Switchers Made Simple ${ }^{\circledR}$ (version 4.2 or later).
3. Catch Diode Selection (D1)
A. The catch diode current rating must be at least 1.3 times greater than the maximum load current. Also, if the power supply design must withstand a continuous output short, the diode should have a current rating equal to the maximum current limit of the LM2598. The most stressful condition for this diode is an overload or shorted output condition.
B. The reverse voltage rating of the diode should be at least 1.25 times the maximum input voltage.
C. This diode must be fast (short reverse recovery time) and must be located close to the LM2598 using short leads and short printed circuit traces. Because of their fast switching speed and low forward voltage drop, Schottky diodes provide the best performance and efficiency, and should be the first choice, especially in low output voltage applications. Ultra-fast recovery, or High-

Procedure continued on next page.

EXAMPLE (Fixed Output Voltage Version)
Given:
$V_{\text {OUT }}=5 \mathrm{~V}$
$\mathrm{V}_{\mathrm{IN}}(\max )=12 \mathrm{~V}$
$\mathrm{I}_{\mathrm{LOAD}}(\max )=1 \mathrm{~A}$

1. Inductor Selection (L1)
A. Use the inductor selection guide for the 5 V version shown in Figure 5.
B. From the inductor value selection guide shown in Figure 5 , the inductance region intersected by the 12 V horizontal line and the 1A vertical line is $68 \mu \mathrm{H}$, and the inductor code is L30.
C. The inductance value required is $68 \mu \mathrm{H}$. From the table in Figure 8, go to the L30 line and choose an inductor part number from any of the four manufacturers shown. (In most instance, both through hole and surface mount inductors are available.)
2. Output Capacitor Selection (COUT)
A. See section on output capacitors in application information section.
B. From the quick design component selection table shown in Figure 2, locate the 5V output voltage section. In the load current column, choose the load current line that is closest to the current needed in your application, for this example, use the 1 A line. In the maximum input voltage column, select the line that covers the input voltage needed in your application, in this example, use the 15 V line. Continuing on this line are recommended inductors and capacitors that will provide the best overall performance.
The capacitor list contains both through hole electrolytic and surface mount tantalum capacitors from four different capacitor manufacturers. It is recommended that both the manufacturers and the manufacturer's series that are listed in the table be used.
In this example aluminum electrolytic capacitors from several different manufacturers are available with the range of ESR numbers needed.
$220 \mu \mathrm{~F} \quad 25 \mathrm{~V}$ Panasonic HFQ Series
$220 \mu \mathrm{~F} \quad 25 \mathrm{~V}$ Nichicon PL Series
C. For a 5 V output, a capacitor voltage rating at least 7.5 V or more is needed. But, in this example, even a low ESR, switching grade, $220 \mu \mathrm{~F} 10 \mathrm{~V}$ aluminum electrolytic capacitor would exhibit approximately $225 \mathrm{~m} \Omega$ of ESR (see the curve in Figure 16 for the ESR vs voltage rating). This amount of ESR would result in relatively high output ripple voltage. To reduce the ripple to $1 \%$ of the output voltage, or less, a capacitor with a higher voltage rating (lower ESR) should be selected. A 16 V or 25 V capacitor will reduce the ripple voltage by approximately half.
3. Catch Diode Selection (D1)
A. Refer to the table shown in Figure 11. In this example, a 3A, 20V, 1N5820 Schottky diode will provide the best performance, and will not be overstressed even for a shorted output.

Example continued on next page.

| PROCEDURE (Fixed Output Voltage Version) |  |  |  |  | EXAMPLE (Fixed Output Voltage Version) |  |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| Efficiency rectifiers also provide good results. Ultra-fast recovery diodes typically have reverse recovery times of 50 ns or less. Rectifiers such as the 1N5400 series are much too slow and should not be used. <br> 4. Input Capacitor ( $\mathrm{C}_{\mathrm{IN}}$ ) <br> A low ESR aluminum or tantalum bypass capacitor is needed between the input pin and ground to prevent large voltage transients from appearing at the input. In addition, the RMS current rating of the input capacitor should be selected to be at least $1 / 2$ the DC load current. The capacitor manufacturers data sheet must be checked to assure that this current rating is not exceeded. The curve shown in Figure 15 shows typical RMS current ratings for several different aluminum electrolytic capacitor values. <br> This capacitor should be located close to the IC using short leads and the voltage rating should be approximately 1.5 times the maximum input voltage. <br> If solid tantalum input capacitors are used, it is recomended that they be surge current tested by the manufacturer. <br> Use caution when using ceramic capacitors for input bypassing, because it may cause severe ringing at the $\mathrm{V}_{\mathrm{IN}}$ pin. <br> For additional information, see section on input capacitors in Application Information section. |  |  |  |  | 4. Input Capacitor ( $\mathrm{C}_{\mathrm{IN}}$ ) <br> The important parameters for the Input capacitor are the input voltage rating and the RMS current rating. With a nominal input voltage of 12 V , an aluminum electrolytic capacitor with a voltage rating greater than $18 \mathrm{~V}(1.5 \times$ $\mathrm{V}_{\mathrm{IN}}$ ) would be needed. The next higher capacitor voltage rating is 25 V . <br> The RMS current rating requirement for the input capacitor in a buck regulator is approximately $1 / 2$ the DC load current. In this example, with a 1A load, a capacitor with a RMS current rating of at least 500 mA is needed. The curves shown in Figure 15 can be used to select an appropriate input capacitor. From the curves, locate the 25 V line and note which capacitor values have RMS current ratings greater than 500 mA . Either a $180 \mu \mathrm{~F}$ or $220 \mu \mathrm{~F}, 25 \mathrm{~V}$ capacitor could be used. <br> For a through hole design, a $220 \mu \mathrm{~F} / 25 \mathrm{~V}$ electrolytic capacitor (Panasonic HFQ series or Nichicon PL series or equivalent) would be adequate. other types or other manufacturers capacitors can be used provided the RMS ripple current ratings are adequate. <br> For surface mount designs, solid tantalum capacitors are recommended. The TPS series available from AVX, and the 593D series from Sprague are both surge current tested. |  |  |  |
| Conditions |  |  | Inductor |  | Output Capacitor |  |  |  |
|  |  |  | Through Hole Electrolytic | Surface Mount Tantalum |  |
| Output Voltage (V) | Load Current (A) | Max Input Voltage (V) |  |  | Inductance ( $\mu \mathrm{H}$ ) | Inductor (\#) | Panasonic HFQ Series ( $\mu \mathrm{F} / \mathrm{V}$ ) | Nichicon PL Series ( $\mu \mathrm{F} / \mathrm{V}$ ) | AVX TPS Series ( $\mu \mathrm{F} / \mathrm{V}$ ) | Sprague 595D Series ( $\mu \mathrm{F} / \mathrm{V}$ ) |
| 3.3 | 1 | 5 | 22 | L24 | 330/16 | 330/16 | 220/10 | 330/10 |
|  |  | 7 | 33 | L23 | 270/25 | 270/25 | 220/10 | 270/10 |
|  |  | 10 | 47 | L31 | 220/25 | 220/35 | 220/10 | 220/10 |
|  |  | 40 | 68 | L30 | 180/35 | 220/35 | 220/10 | 180/10 |
|  | 0.5 | 6 | 47 | L13 | 220/25 | 220/16 | 220/16 | 220/10 |
|  |  | 10 | 68 | L21 | 150/35 | 150/25 | 100/16 | 150/16 |
|  |  | 40 | 100 | L20 | 150/35 | 82/35 | 100/16 | 100/20 |
| 5 | 1 | 8 | 33 | L28 | 330/16 | 330/16 | 220/10 | 270/10 |
|  |  | 10 | 47 | L31 | 220/25 | 220/25 | 220/10 | 220/10 |
|  |  | 15 | 68 | L30 | 180/35 | 180/35 | 220/10 | 150/16 |
|  |  | 40 | 100 | L29 | 180/35 | 120/35 | 100/16 | 120/16 |
|  | 0.5 | 9 | 68 | L21 | 180/16 | 180/16 | 220/10 | 150/16 |
|  |  | 20 | 150 | L19 | 120/25 | 120/25 | 100/16 | 100/20 |
|  |  | 40 | 150 | L19 | 100/25 | 100/25 | 68/20 | 68/25 |
| 12 | 1 | 15 | 47 | L31 | 220/25 | 220/25 | 68/20 | 120/20 |
|  |  | 18 | 68 | L30 | 180/35 | 120/25 | 68/20 | 120/20 |
|  |  | 30 | 150 | L36 | 82/25 | 82/25 | 68/20 | 100/20 |
|  |  | 40 | 220 | L35 | 82/25 | 82/25 | 68/20 | 68/25 |
|  | 0.5 | 15 | 68 | L21 | 180/25 | 180/25 | 68/20 | 120/20 |
|  |  | 20 | 150 | L19 | 82/25 | 82/25 | 68/20 | 100/20 |
|  |  | 40 | 330 | L26 | 56/25 | 56/25 | 68/20 | 68/25 |

FIGURE 2. LM2598 Fixed Voltage Quick Design Component Selection Table

## LM2598 Series Buck Regulator Design Procedure (Adjustable Output)

| PROCEDURE (Adjustable Output Voltage Version) |
| :--- |
| Given: |
| V OUT $^{\prime}=$ Regulated Output Voltage |
| $\mathrm{V}_{\text {IN }}(\max )=$ Maximum Input Voltage |
| $\mathrm{I}_{\text {LOAD }}(\max )=$ Maximum Load Current |
| F $=$ Switching Frequency (Fixed at a nominal 150 kHz ). |

1. Programming Output Voltage (Selecting $R_{1}$ and $R_{2}$, as shown in Figure 1)
Use the following formula to select the appropriate resistor values.

$$
\mathrm{V}_{\mathrm{OUT}}=\mathrm{V}_{\mathrm{REF}}\left(1+\frac{\mathrm{R}_{2}}{\mathrm{R}_{1}}\right) \quad \text { where } \mathrm{V}_{\mathrm{REF}}=1.23 \mathrm{~V}
$$

Select a value for $R_{1}$ between $240 \Omega$ and $1.5 \mathrm{k} \Omega$. The lower resistor values minimize noise pickup in the sensitive feedback pin. (For the lowest temperature coefficient and the best stability with time, use $1 \%$ metal film resistors.)

$$
\mathrm{R}_{2}=\mathrm{R}_{1}\left(\frac{\mathrm{~V}_{\mathrm{OUT}}}{\mathrm{~V}_{\mathrm{REF}}}-1\right)
$$

2. Inductor Selection (L1)
A. Calculate the inductor Volt - microsecond constant $E \bullet T(V \bullet \mu s)$, from the following formula:
$E \cdot T=\left(V_{\text {IN }}-V_{\text {OUT }}-V_{S A T}\right) \cdot \frac{V_{\text {OUT }}+V_{D}}{V_{\text {IN }}-V_{S A T}+V_{D}} \cdot \frac{1000}{150 \mathrm{kHz}}(\mathrm{V} \bullet \mu \mathrm{S})$
where $\mathrm{V}_{\text {SAT }}=$ internal switch saturation voltage $=1 \mathrm{~V}$ and $V_{D}=$ diode forward voltage drop $=0.5 \mathrm{~V}$
B. Use the E - T value from the previous formula and match it with the $\mathrm{E} \cdot \mathrm{T}$ number on the vertical axis of the Inductor Value Selection Guide shown in Figure 7.
C. on the horizontal axis, select the maximum load current.
D. Identify the inductance region intersected by the $\mathrm{E} \bullet \mathrm{T}$ value and the Maximum Load Current value. Each region is identified by an inductance value and an inductor code (LXX).
E. Select an appropriate inductor from the four manufacturer's part numbers listed in Figure 8.
3. Output Capacitor Selection (Cout)
A. In the majority of applications, low ESR electrolytic or solid tantalum capacitors between $82 \mu \mathrm{~F}$ and $220 \mu \mathrm{~F}$ provide the best results. This capacitor should be located close to the IC using short capacitor leads and short copper traces. Do not use capacitors larger than $220 \mu \mathrm{~F}$. For additional information, see section on output capacitors in application information section.
B. To simplify the capacitor selection procedure, refer to the quick design table shown in Figure 3. This table contains different output voltages, and lists various output capacitors that will provide the best design solutions.
C. The capacitor voltage rating should be at least 1.5 times greater than the output voltage, and often much higher voltage ratings are needed to satisfy the low ESR requirements needed for low output ripple voltage.

Procedure continued on next page.

EXAMPLE (Adjustable Output Voltage Version)

## Given:

$V_{\text {OUT }}=20 \mathrm{~V}$
$\mathrm{V}_{\mathrm{IN}}(\max )=28 \mathrm{~V}$
$\operatorname{loAD}(\max )=1 \mathrm{~A}$
$\mathrm{F}=$ Switching Frequency (Fixed at a nominal 150 kHz ).

1. Programming Output Voltage (Selecting $R_{1}$ and $R_{2}$, as shown in Figure 1)

Select $R_{1}$ to be $1 k \Omega, 1 \%$. Solve for $R_{2}$.

$$
\mathrm{R}_{2}=\mathrm{R}_{1}\left(\frac{\mathrm{~V}_{\mathrm{OUT}}}{\mathrm{~V}_{\mathrm{REF}}}-1\right)=1 \mathrm{k}\left(\frac{20 \mathrm{~V}}{1.23 \mathrm{~V}}-1\right)
$$

$R_{2}=1 \mathrm{k}(16.26-1)=15.26 \mathrm{k}$, closest $1 \%$ value is
$15.4 \mathrm{k} \Omega$.
$R_{2}=15.4 \mathrm{k} \Omega$.
2. Inductor Selection (L1)
A. Calculate the inductor Volt - microsecond constant
( $\mathrm{E} \bullet \mathrm{T}$ ),

$\mathrm{E} \bullet \mathrm{T}=(7) \cdot \frac{20.5}{27.6} \bullet 6.67(\mathrm{~V} \bullet \mu \mathrm{~s})=34.8(\mathrm{~V} \bullet \mu \mathrm{~s})$
B. $\mathrm{E} \cdot \mathrm{T}=34.8(\mathrm{~V} \bullet \mu \mathrm{~s})$
C. $\mathrm{I}_{\text {LOAD }}(\max )=1 \mathrm{~A}$
D. From the inductor value selection guide shown in Figure 7, the inductance region intersected by the 35 (V • $\mu \mathrm{s}$ ) horizontal line and the 1A vertical line is $100 \mu \mathrm{H}$, and the inductor code is L29.
E. From the table in Figure 8, locate line L29, and select an inductor part number from the list of manufacturers part numbers.
3. Output Capacitor Selection (Cout)
A. See section on COUT in Application Information section.
B. From the quick design table shown in Figure 3, locate the output voltage column. From that column, locate the output voltage closest to the output voltage in your application. In this example, select the 24 V line. Under the output capacitor section, select a capacitor from the list of through hole electrolytic or surface mount tantalum types from four different capacitor manufacturers. It is recommended that both the manufacturers and the manufacturers series that are listed in the table be used.
In this example, through hole aluminum electrolytic capacitors from several different manufacturers are available.

| $82 \mu \mathrm{~F}$ |
| :--- |
| $82 \mu \mathrm{~V}$ | Panasonic HFQ Series

$82 \mathrm{~F} \quad 35 \mathrm{~V}$ Nichicon PL Series
Example continued on next page.


| LM2598 Series Buck Regulator Design Procedure (Adjustable Output) <br> (Continued) |  |  |  |  |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  | Through Hole Electrolytic Output Capacitor |  |  | Surface Mount Tantalum Output Capacitor |  |  |
| Voltage <br> (V) | Panasonic HFQ Series ( $\mu \mathrm{F} / \mathrm{V}$ ) | Nichicon PL Series ( $\mu$ F/V) | Feedforward Capacitor | AVX TPS <br> Series ( $\mu \mathrm{F} / \mathrm{V}$ ) | Sprague 595D Series ( $\mu \mathrm{F} / \mathrm{V}$ ) | Feedforward Capacitor |
| 1.2 | 330/50 | 330/50 | 0 | 330/6.3 | 330/6.3 | 0 |
| 4 | 220/25 | 220/25 | 4.7 nF | 220/10 | 220/10 | 4.7 nF |
| 6 | 220/25 | 220/25 | 3.3 nF | 220/10 | 220/10 | 3.3 nF |
| 9 | 180/25 | 180/25 | 1.5 nF | 100/16 | 180/16 | 1.5 nF |
| 12 | 120/25 | 120/25 | 1.5 nF | 68/20 | 120/20 | 1.5 nF |
| 15 | 120/25 | 120/25 | 1.5 nF | 68/20 | 100/20 | 1.5 nF |
| 24 | 82/35 | 82/35 | 1 nF | 33/25 | 33/35 | 220 pF |
| 28 | 82/50 | 82/50 | 1 nF | 10/35 | 33/35 | 220 pF |

## LM2598 Series Buck Regulator Design Procedure

INDUCTOR VALUE SELECTION GUIDES (For Continuous Mode Operation)


TL/H/12593-25
FIGURE 4. LM2598-3.3


MAXIMUM LOAD CURRENT (A)

FIGURE 6. LM2598-12


TL/H/12593-26
FIGURE 5. LM2598-5.0


| LM2598 Series Buck Regulator Design Procedure (Continued) |  |  |  |  |  |  |  |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  | Inductance ( $\mu \mathrm{H}$ ) | Current <br> (A) | Schott |  | Renco |  | Pulse Engineering |  | Coilcraft <br> Surface Mount |
|  |  |  | Through Hole | Surface Mount | Through Hole | Surface <br> Mount | Through Hole | Surface Mount |  |
| L4 | 68 | 0.32 | 67143940 | 67144310 | RL-1284-68-43 | RL1500-68 | PE-53804 | PE-53804-S | DO1608-68 |
| L5 | 47 | 0.37 | 67148310 | 67148420 | RL-1284-47-43 | RL1500-47 | PE-53805 | PE-53805-S | DO1608-473 |
| L6 | 33 | 0.44 | 67148320 | 67148430 | RL-1284-33-43 | RL1500-33 | PE-53806 | PE-53806-S | DO1608-333 |
| L9 | 220 | 0.32 | 67143960 | 67144330 | RL-5470-3 | RL1500-220 | PE-53809 | PE-53809-S | DO3308-224 |
| L10 | 150 | 0.39 | 67143970 | 67144340 | RL-5470-4 | RL1500-150 | PE-53810 | PE-53810-S | DO3308-154 |
| L11 | 100 | 0.48 | 67143980 | 67144350 | RL-5470-5 | RL1500-100 | PE-53811 | PE-53811-S | DO3308-104 |
| L12 | 68 | 0.58 | 67143990 | 67144360 | RL-5470-6 | RL1500-68 | PE-53812 | PE-53812-S | DO3308-683 |
| L13 | 47 | 0.70 | 67144000 | 67144380 | RL-5470-7 | RL1500-47 | PE-53813 | PE-53813-S | DO3308-473 |
| L14 | 33 | 0.83 | 67148340 | 67148450 | RL-1284-33-43 | RL1500-33 | PE-53814 | PE-53814-S | DO3308-333 |
| L15 | 22 | 0.99 | 67148350 | 67148460 | RL-1284-22-43 | RL1500-22 | PE-53815 | PE-53815-S | DO3308-223 |
| L16 | 15 | 1.24 | 67148360 | 67148470 | RL-1284-15-43 | RL1500-15 | PE-53816 | PE-53816-S | DO3308-153 |
| L17 | 330 | 0.42 | 67144030 | 67144410 | RL-5471-1 | RL1500-330 | PE-53817 | PE-53817-S | DO3316-334 |
| L18 | 220 | 0.55 | 67144040 | 67144420 | RL-5471-2 | RL1500-220 | PE-53818 | PE-53818-S | DO3316-224 |
| L19 | 150 | 0.66 | 67144050 | 67144430 | RL-5471-3 | RL1500-150 | PE-53819 | PE-53819-S | DO3316-154 |
| L20 | 100 | 0.82 | 67144060 | 67144440 | RL-5471-4 | RL1500-100 | PE-53820 | PE-53820-S | DO3316-104 |
| L21 | 68 | 0.99 | 67144070 | 67144450 | RL-5471-5 | RL1500-68 | PE-53821 | PE-53821-S | DO3316-683 |
| L22 | 47 | 1.17 | 67144080 | 67144460 | RL-5471-6 | - | PE-53822 | PE-53822-S | DO3316-473 |
| L23 | 33 | 1.40 | 67144090 | 67144470 | RL-5471-7 | - | PE-53823 | PE-53823-S | DO3316-333 |
| L24 | 22 | 1.70 | 67148370 | 67144480 | RL-1283-22-43 | - | PE-53824 | PE-53824-S | DO3316-223 |
| L26 | 330 | 0.80 | 67144100 | 67144480 | RL-5471-1 | - | PE-53826 | PE-53826-S | DO5022P-334 |
| L27 | 220 | 1.00 | 67144110 | 67144490 | RL-5471-2 | - | PE-53827 | PE-53827-S | DO5022P-224 |
| L28 | 150 | 1.20 | 67144120 | 67144500 | RL-5471-3 | - | PE-53828 | PE-53828-S | DO5022P-154 |
| L29 | 100 | 1.47 | 67144130 | 67144510 | RL-5471-4 | - | PE-53829 | PE-53829-S | DO5022P-104 |
| L30 | 68 | 1.78 | 67144140 | 67144520 | RL-5471-5 | - | PE-53830 | PE-53830-S | DO5022P-683 |
| L35 | 47 | 2.15 | 67144170 | - | RL-5473-1 | - | PE-53935 | PE-53935-S | - |

FIGURE 8. Inductor Manufacturers Part Numbers

| Coilcraft Inc. | Phone | $(800) 322-2645$ |
| :--- | :--- | :--- |
|  | FAX | $(708) 639-1469$ |
| Coilcraft Inc., Europe | Phone | +111236730595 |
|  | FAX | +441236730627 |
| Pulse Engineering Inc. | Phone | $(619) 674-8100$ |
|  | FAX | $(619) 674-8262$ |
| Pulse Engineering Inc., <br> Europe | Phone | +3539324107 |
|  | FAX | +3539324459 |
|  | Phone | $(800) 645-5828$ |
|  | FAX | $(516) 586-5562$ |
| Schott Corp. | Phone | $(612) 475-1173$ |
|  | FAX | $(612) 475-1786$ |


| Nichicon Corp. | Phone | (708) 843-7500 |
| :--- | :--- | :--- |
|  | FAX | $(708) 843-2798$ |
| Panasonic | Phone | $(714) 373-7857$ |
|  | FAX | $(714) 373-7102$ |
| AVX Corp. | Phone | $(803) 448-9411$ |
|  | FAX | $(803) 448-1943$ |
| Sprague/Vishay | Phone | $(207) 324-4140$ |
|  | FAX | $(207) 324-7223$ |

FIGURE 10. Capacitor Manufacturers Phone Numbers

FIGURE 9. Inductor Manufacturers Phone Numbers

## LM2598 Series Buck Regulator Design Procedure (Continued)

| VR | 1A Diodes |  |  |  | 3A Diodes |  |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  | Surface Mount |  | Through Hole |  | Surface Mount |  | Through Hole |  |
|  | Schottky | Ultra Fast Recovery | Schottky | Ultra Fast Recovery | Schottky | Ultra Fast Recovery | Schottky | Ultra Fast Recovery |
| 20V | SK12 | All of these diodes are rated to at least 50V. | 1N5817 | All of these diodes are rated to at least 50V. <br> MUR120 |  | All of these diodes are rated to at least 50 V . <br> MURS320 30WF10 | IN5820 | All of these diodes are rated to at least 50 V . <br> MUR320 <br> 30WF10 |
|  |  |  | SR102 |  | SK32 |  | SR302 |  |
|  |  |  |  |  |  |  | MBR320 |  |
|  | SK13 |  | 1N5818 |  |  |  | 1N5821 |  |
| 30 V | MBRS130 |  | SR103 |  | SK33 |  | MBR330 |  |
|  |  |  | 11DQ03 |  |  |  | 31DQ03 |  |
| 40 V | SK14 |  |  |  |  |  | 1N5822 |  |
|  | MBRS140 |  | 1N5819 |  | SK34 |  | SR304 |  |
|  | 10BQ040 |  | SR104 |  | MBRS340 |  | MBR340 |  |
|  | 10MQ040 | MURS12010BF10 | 11DQ04 |  | 30WQ04 |  | 31DQ04 |  |
| $\begin{gathered} 50 \mathrm{~V} \\ \text { or } \\ \text { more } \end{gathered}$ | MBRS160 |  | SR105 |  | SK35 |  | SR305 |  |
|  | 10BQ050 |  | MBR150 |  | MBRS360 |  | MBR350 |  |
|  | 10MQ060 |  | 11DQ05 |  | 30WQ05 |  | 31DQ05 |  |

FIGURE 11. Diode Selection Table

## Block Diagram



FIGURE 12

## Application Information

## PIN FUNCTIONS

$+\mathbf{V}_{\mathbf{I N}}$ (Pin 2)—This is the positive input supply for the IC switching regulator. A suitable input bypass capacitor must be present at this pin to minimize voltage transients and to supply the switching currents needed by the regulator.
Ground (Pin 4)—Circuit ground.
Output (Pin 1)—Internal switch. The voltage at this pin switches between approximately ( $+\mathrm{V}_{\text {IN }}-\mathrm{V}_{\text {SAT }}$ ) and approximately -0.5 V , with a duty cycle of $\mathrm{V}_{\mathrm{OUT}} / \mathrm{V}_{\text {IN }}$. To minimize coupling to sensitive circuitry, the PC board copper area connected to this pin should be kept to a minimum.
Feedback (Pin 6)—Senses the regulated output voltage to complete the feedback loop.
$\overline{\text { Shutdown/Soft-start (Pin 7)—This dual function pin pro- }}$ vides the following features: (a) Allows the switching regulator circuit to be shut down using logic level signals thus dropping the total input supply current to approximately $85 \mu \mathrm{~A}$. (b) Adding a capacitor to this pin provides a soft-start feature which minimizes startup current and provides a controlled ramp up of the output voltage.
Error Flag (Pin 3)—Open collector output that provides a low signal (flag transistor ON) when the regulated output voltage drops more than $5 \%$ from the nominal output voltage. On start up, Error Flag is low until $\mathrm{V}_{\text {OUT }}$ reaches $95 \%$ of the nominal output voltage and a delay time determined by the Delay pin capacitor. This signal can be used as a reset to a microprocessor on power-up.
Delay (Pin 5)—At power-up, this pin can be used to provide a time delay between the time the regulated output voltage reaches $95 \%$ of the nominal output voltage, and the time the error flag output goes high.
Special Note If any of the above three features ( (Shutdown/ Soft-start, Error Flag, or Delay) are not used, the respective pins should be left open.

## EXTERNAL COMPONENTS

## SOFT-START CAPACITOR

$\mathbf{C}_{\text {SS-A }}$ capacitor on this pin provides the regulator with a Soft-start feature (slow start-up). When the DC input voltage is first applied to the regulator, or when the Shutdown/Softstart pin is allowed to go high, a constant current (approximately $5 \mu \mathrm{~A}$ begins charging this capacitor). As the capacitor voltage rises, the regulator goes through four operating regions (See the bottom curve in Figure 13).

1. Regulator in Shutdown. When the $\overline{\mathrm{SD}} / \mathrm{SS}$ pin voltage is between 0 V and 1.3 V , the regulator is in shutdown, the output voltage is zero, and the IC quiescent current is approximately $85 \mu \mathrm{~A}$.
2. Regulator ON, but the output voltage is zero. With the $\overline{\mathrm{SD}} / \mathrm{SS}$ pin voltage between approximately 1.3 V and 1.8 V , the internal regulator circuitry is operating, the quiescent current rises to approximately 5 mA , but the output voltage is still zero. Also, as the 1.3 V threshold is exceeded, the Soft-start capacitor charging current decreases from $5 \mu \mathrm{~A}$ down to approximately $1.6 \mu \mathrm{~A}$. This decreases the slope of capacitor voltage ramp.
3. Soft-start Region. When the $\overline{\text { SD }} / \mathrm{SS}$ pin voltage is between 1.8 V and 2.8 V (@ $25^{\circ} \mathrm{C}$ ), the regulator is in a Softstart condition. The switch (Pin 1) duty cycle initially starts out very low, with narrow pulses and gradually get wider as the capacitor $\overline{\mathrm{SD}} / \mathrm{SS}$ pin ramps up towards 2.8 V . As the duty cycle increases, the output voltage also increases at a controlled ramp up. See the center curve in Figure 13. The input supply current requirement also starts out at a low level for the narrow pulses and ramp up in a controlled manner. This is a very useful feature in some switcher topologies that require large startup currents (such as the inverting configuration) which can load down the input power supply.
Note: The lower curve shown in Figure 13 shows the Soft-start region from $0 \%$ to $100 \%$. This is not the duty cycle percentage, but the output voltage percentage. Also, the Soft-start voltage range has a negative temperature coefficient associated with it. See the Soft-start curve in the electrical characteristics section.
4. Normal operation. Above 2.8 V , the circuit operates as a standard Pulse Width Modulated switching regulator. The capacitor will continue to charge up until it reaches the internal clamp voltage of approximately 7 V . If this pin is driven from a voltage source, the current must be limited to about 1 mA .

time dependent upon delay capacitor value


TIME DEPENDENT UPON SOFT-START CAPACITOR VALUE
TL/H/12593-30
FIGURE 13. Soft-start, Delay, Error, Output

## Application Information (Continued)



TL/H/12593-31
FIGURE 14. Timing Diagram for 5V Output

## DELAY CAPACITOR

CDELAY—Provides delay for the error flag output. See the upper curve in Figure 13, and also refer to timing diagrams in Figure 14. A capacitor on this pin provides a time delay between the time the regulated output voltage (when it is increasing in value) reaches $95 \%$ of the nominal output voltage, and the time the error flag output goes high. A $3 \mu \mathrm{~A}$ constant current from the delay pin charges the delay capacitor resulting in a voltage ramp. When this voltage reaches a threshold of approximately 1.3 V , the open collector error flag output (or power OK) goes high. This signal can be used to indicate that the regulated output has reached the correct voltage and has stabilized.
If, for any reason, the regulated output voltage drops by $5 \%$ or more, the error output flag (Pin 3) immediately goes low (internal transistor turns on). The delay capacitor provides very little delay if the regulated output is dropping out of regulation. The delay time for an output that is decreasing is approximately a 1000 times less than the delay for the rising output. For a $0.1 \mu \mathrm{~F}$ delay capacitor, the delay time would be approximately 50 ms when the output is rising and passes through the $95 \%$ threshold, but the delay for the output dropping would only be approximately $50 \mu \mathrm{~s}$.
RPull Up-The error flag output, (or power OK) is the collector of a NPN transistor, with the emitter internally grounded. To use the error flag, a pullup resistor to a positive voltage is needed. The error flag transistor is rated up to a maximum of 45 V and can sink approximately 3 mA . If the error flag is not used, it can be left open.

## FEEDFORWARD CAPACITOR

(Adjustable Output Voltage Version)
$\mathrm{C}_{\mathrm{FF}}$-A Feedforward Capacitor $\mathrm{C}_{\mathrm{FF}}$, shown across R2 in Figure 1 is used when the output voltage is greater than 10 V or then COUT has a very low ESR. This capacitor adds lead compensation to the feedback loop and increases the phase margin for better loop stability. For $\mathrm{C}_{\text {FF }}$ selection, see the design procedure section.

If the output ripple is large ( $>5 \%$ of the nominal output voltage), this ripple can be coupled to the feedback pin through the feedforward capacitor and cause the error comparator to trigger the error flag. In this situation, adding a resistor, $\mathrm{R}_{\mathrm{FF}}$, in series with the feedforward capacitor, approximately 3 times R1, will attenuate the ripple voltage at the feedback pin.

## INPUT CAPACITOR

$\mathbf{C}_{\mathbf{I N}}$-A low ESR aluminum or tantalum bypass capacitor is needed between the input pin and ground pin. It must be located near the regulator using short leads. This capacitor prevents large voltage transients from appearing at the input, and provides the instantaneous current needed each time the switch turns on.
The important parameters for the Input capacitor are the voltage rating and the RMS current rating. Because of the relatively high RMS currents flowing in a buck regulator's input capacitor, this capacitor should be chosen for its RMS current rating rather than its capacitance or voltage ratings, although the capacitance value and voltage rating are directly related to the RMS current rating.
The RMS current rating of a capacitor could be viewed as a capacitor's power rating. The RMS current flowing through the capacitors internal ESR produces power which causes the internal temperature of the capacitor to rise. The RMS current rating of a capacitor is determined by the amount of current required to raise the internal temperature approximately $10^{\circ} \mathrm{C}$ above an ambient temperature of $105^{\circ} \mathrm{C}$. The ability of the capacitor to dissipate this heat to the surrounding air will determine the amount of current the capacitor can safely sustain. Capacitors that are physically large and have a large surface area will typically have higher RMS current ratings. For a given capacitor value, a higher voltage electrolytic capacitor will be physically larger than a lower voltage capacitor, and thus be able to dissipate more heat to the surrounding air, and therefore will have a higher RMS current rating.

## Application Information (Continued)



FIGURE 15. RMS Current Ratings for Low ESR Electrolytic Capacitors (Typical)

The consequences of operating an electrolytic capacitor above the RMS current rating is a shortened operating life. The higher temperature speeds up the evaporation of the capacitor's electrolyte, resulting in eventual failure.
Selecting an input capacitor requires consulting the manufacturers data sheet for maximum allowable RMS ripple current. For a maximum ambient temperature of $40^{\circ} \mathrm{C}$, a general guideline would be to select a capacitor with a ripple current rating of approximately $50 \%$ of the DC load current. For ambient temperatures up to $70^{\circ} \mathrm{C}$, a current rating of $75 \%$ of the DC load current would be a good choice for a conservative design. The capacitor voltage rating must be at least 1.25 times greater than the maximum input voltage, and often a much higher voltage capacitor is needed to satisfy the RMS current requirements.
A graph shown in Figure 15 shows the relationship between an electrolytic capacitor value, its voltage rating, and the RMS current it is rated for. These curves were obtained from the Nichicon "PL" series of low ESR, high reliability electrolytic capacitors designed for switching regulator applications. Other capacitor manufacturers offer similar types of capacitors, but always check the capacitor data sheet.
"Standard" electrolytic capacitors typically have much higher ESR numbers, lower RMS current ratings and typically have a shorter operating lifetime.
Because of their small size and excellent performance, surface mount solid tantalum capacitors are often used for input bypassing, but several precautions must be observed. A small percentage of solid tantalum capacitors can short if the inrush current rating is exceeded. This can happen at turn on when the input voltage is suddenly applied, and of course, higher input voltages produce higher inrush currents. Several capacitor manufacturers do a 100\% surge current testing on their products to minimize this potential


FIGURE 16. Capacitor ESR vs Capacitor Voltage Rating (Typical Low ESR Electrolytic Capacitor)
problem. If high turn on currents are expected, it may be necessary to limit this current by adding either some resistance or inductance before the tantalum capacitor, or select a higher voltage capacitor. As with aluminum electrolytic capacitors, the RMS ripple current rating must be sized to the load current.

## OUTPUT CAPACITOR

Cout-An output capacitor is required to filter the output and provide regulator loop stability. Low impedance or low ESR Electrolytic or solid tantalum capacitors designed for switching regulator applications must be used. When selecting an output capacitor, the important capacitor parameters are; the 100 kHz Equivalent Series Resistance (ESR), the RMS ripple current rating, voltage rating, and capacitance value. For the output capacitor, the ESR value is the most important parameter.
The output capacitor requires an ESR value that has an upper and lower limit. For low output ripple voltage, a low ESR value is needed. This value is determined by the maximum allowable output ripple voltage, typically $1 \%$ to $2 \%$ of the output voltage. But if the selected capacitor's ESR is extremely low, there is a possibility of an unstable feedback loop, resulting in an oscillation at the output. Using the capacitors listed in the tables, or similar types, will provide design solutions under all conditions.
If very low output ripple voltage (less than 15 mV ) is required, refer to the section on Output Voltage Ripple and Transients for a post ripple filter.
An aluminum electrolytic capacitor's ESR value is related to the capacitance value and its voltage rating. In most cases, higher voltage electrolytic capacitors have lower ESR values (see Figure 16). Often, capacitors with much higher voltage ratings may be needed to provide the low ESR values required for low output ripple voltage.

## Application Information (Continued)

The output capacitor for many different switcher designs often can be satisfied with only three or four different capacitor values and several different voltage ratings. See the quick design component selection tables in Figures 2 and 3 for typical capacitor values, voltage ratings, and manufacturers capacitor types.
Electrolytic capacitors are not recommended for temperatures below $-25^{\circ} \mathrm{C}$. The ESR rises dramatically at cold temperatures and typically rises 3 X @ $-25^{\circ} \mathrm{C}$ and as much as 10 X at $-40^{\circ} \mathrm{C}$. See curve shown in Figure 17.
Solid tantalum capacitors have a much better ESR spec for cold temperatures and are recommended for temperatures below $-25^{\circ} \mathrm{C}$.

## CATCH DIODE

Buck regulators require a diode to provide a return path for the inductor current when the switch turns off. This must be a fast diode and must be located close to the LM2598 using short leads and short printed circuit traces.
Because of their very fast switching speed and low forward voltage drop, Schottky diodes provide the best performance, especially in low output voltage applications (5V and lower). Ultra-fast recovery, or High-Efficiency rectifiers are also a good choice, but some types with an abrupt turnoff characteristic may cause instability or EMI problems. Ultrafast recovery diodes typically have reverse recovery times of 50 ns or less. Rectifiers such as the 1N5400 series are much too slow and should not be used.


TL/H/12593-34
FIGURE 17. Capacitor ESR Change vs Temperature

## INDUCTOR SELECTION

All switching regulators have two basic modes of operation; continuous and discontinuous. The difference between the two types relates to the inductor current, whether it is flowing continuously, or if it drops to zero for a period of time in the normal switching cycle. Each mode has distinctively different operating characteristics, which can affect the regulators performance and requirements. Most switcher designs will operate in the discontinuous mode when the load current is low.
The LM2598 (or any of the Simple Switcher family) can be used for both continuous or discontinuous modes of operation.
In many cases the preferred mode of operation is the continuous mode. It offers greater output power, lower peak switch, inductor and diode currents, and can have lower output ripple voltage. But it does require larger inductor values to keep the inductor current flowing continuously, especially at low output load currents and/or high input voltages.

To simplify the inductor selection process, an inductor selection guide (nomograph) was designed (see Figures 3 through 6). This guide assumes that the regulator is operating in the continuous mode, and selects an inductor that will allow a peak-to-peak inductor ripple current to be a certain percentage of the maximum design load current. This peak-to-peak inductor ripple current percentage is not fixed, but is allowed to change as different design load currents are selected. (See Figure 18.)


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FIGURE 18. ( $\Delta I_{I N D}$ ) Peak-to-Peak Inductor Ripple Current (as a Percentage of the Load Current) vs Load Current

By allowing the percentage of inductor ripple current to increase for low load currents, the inductor value and size can be kept relatively low.
When operating in the continuous mode, the inductor current waveform ranges from a triangular to a sawtooth type of waveform (depending on the input voltage), with the average value of this current waveform equal to the DC output load current.
Inductors are available in different styles such as pot core, toroid, E-core, bobbin core, etc., as well as different core materials, such as ferrites and powdered iron. The least expensive, the bobbin, rod or stick core, consists of wire wound on a ferrite bobbin. This type of construction makes for an inexpensive inductor, but since the magnetic flux is not completely contained within the core, it generates more Electro-Magnetic Interference (EMI). This magnetic flux can induce voltages into nearby printed circuit traces, thus causing problems with both the switching regulator operation and nearby sensitive circuitry, and can give incorrect scope readings because of induced voltages in the scope probe. Also see section on Open Core Inductors.
When multiple switching regulators are located on the same PC board, open core magnetics can cause interference between two or more of the regulator circuits, especially at high currents. A torroid or E-core inductor (closed magnetic structure) should be used in these situations.
The inductors listed in the selection chart include ferrite E-core construction for Schott, ferrite bobbin core for Renco and Coilcraft, and powdered iron toroid for Pulse Engineering.
Exceeding an inductor's maximum current rating may cause the inductor to overheat because of the copper wire losses, or the core may saturate. If the inductor begins to saturate, the inductance decreases rapidly and the inductor begins to look mainly resistive (the DC resistance of the winding). This can cause the switch current to rise very rapidly and force the switch into a cycle-by-cycle current limit, thus reducing

## Application Information (Continued)

the DC output load current. This can also result in overheating of the inductor and/or the LM2598. Different inductor types have different saturation characteristics, and this should be kept in mind when selecting an inductor.
The inductor manufacturer's data sheets include current and energy limits to avoid inductor saturation.

## DISCONTINUOUS MODE OPERATION

The selection guide chooses inductor values suitable for continuous mode operation, but for low current applications and/or high input voltages, a discontinuous mode design may be a better choice. It would use an inductor that would be physically smaller, and would need only one half to one third the inductance value needed for a continuous mode design. The peak switch and inductor currents will be higher in a discontinuous design, but at these low load currents ( 200 mA and below), the maximum switch current will still be less than the switch current limit.
Discontinuous operation can have voltage waveforms that are considerable different than a continuous design. The output pin (switch) waveform can have some damped sinusoidal ringing present. (See photo titled; Discontinuous Mode Switching Waveforms) This ringing is normal for discontinuous operation, and is not caused by feedback loop instabilities. In discontinuous operation, there is a period of time where neither the switch or the diode are conducting, and the inductor current has dropped to zero. During this time, a small amount of energy can circulate between the inductor and the switch/diode parasitic capacitance causing this characteristic ringing. Normally this ringing is not a problem, unless the amplitude becomes great enough to exceed the input voltage, and even then, there is very little energy present to cause damage.
Different inductor types and/or core materials produce different amounts of this characteristic ringing. Ferrite core inductors have very little core loss and therefore produce the most ringing. The higher core loss of powdered iron inductors produce less ringing. If desired, a series RC could be placed in parallel with the inductor to dampen the ringing. The computer aided design software Switchers Made Simple (version 4.2) will provide all component values for continuous and discontinuous modes of operation.


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FIGURE 19. Post Ripple Filter Waveform

## OUTPUT VOLTAGE RIPPLE AND TRANSIENTS

The output voltage of a switching power supply operating in the continuous mode will contain a sawtooth ripple voltage at the switcher frequency, and may also contain short voltage spikes at the peaks of the sawtooth waveform.
The output ripple voltage is a function of the inductor sawtooth ripple current and the ESR of the output capacitor. A typical output ripple voltage can range from approximately $0.5 \%$ to $3 \%$ of the output voltage. To obtain low ripple voltage, the ESR of the output capacitor must be low, however, caution must be exercised when using extremely low ESR capacitors because they can affect the loop stability, resulting in oscillation problems. If very low output ripple voltage is needed (less than 20 mV ), a post ripple filter is recommended. (See Figure 1.) The inductance required is typically between $1 \mu \mathrm{H}$ and $5 \mu \mathrm{H}$, with low DC resistance, to maintain good load regulation. A low ESR output filter capacitor is also required to assure good dynamic load response and ripple reduction. The ESR of this capacitor may be as low as desired, because it is out of the regulator feedback loop. The photo shown in Figure 19 shows a typical output ripple voltage, with and without a post ripple filter.
When observing output ripple with a scope, it is essential that a short, low inductance scope probe ground connection be used. Most scope probe manufacturers provide a special probe terminator which is soldered onto the regulator board, preferable at the output capacitor. This provides a very short scope ground thus eliminating the problems associated with the 3 inch ground lead normally provided with the probe, and provides a much cleaner and more accurate picture of the ripple voltage waveform.
The voltage spikes are caused by the fast switching action of the output switch, the diode, and the parasitic inductance of the output filter capacitor, and its associated wiring. To minimize these voltage spikes, the output capacitor should be designed for switching regulator applications, and the lead lengths must be kept very short. Wiring inductance, stray capacitance, as well as the scope probe used to evaluate these transients, all contribute to the amplitude of these spikes.


FIGURE 20. Peak-to-Peak Inductor Ripple Current vs Load Current

## Application Information (Continued)

When a switching regulator is operating in the continuous mode, the inductor current waveform ranges from a triangular to a sawtooth type of waveform (depending on the input voltage). For a given input and output voltage, the peak-topeak amplitude of this inductor current waveform remains constant. As the load current increases or decreases, the entire sawtooth current waveform also rises and falls. The average value (or the center) of this current waveform is equal to the DC load current.
If the load current drops to a low enough level, the bottom of the sawtooth current waveform will reach zero, and the switcher will smoothly change from a continuous to a discontinuous mode of operation. Most switcher designs (irregardless how large the inductor value is) will be forced to run discontinuous if the output is lightly loaded. This is a perfectly acceptable mode of operation.
In a switching regulator design, knowing the value of the peak-to-peak inductor ripple current ( $\Delta \mathrm{I}_{\mathrm{IND}}$ ) can be useful for determining a number of other circuit parameters. Parameters such as, peak inductor or peak switch current, minimum load current before the circuit becomes discontinuous, output ripple voltage and output capacitor ESR can all be calculated from the peak-to-peak $\Delta I_{\text {IND }}$. When the inductor nomographs shown in Figures 4 through 7 are used to select an inductor value, the peak-to-peak inductor ripple current can immediately be determined. The curve shown in Figure 20 shows the range of $\left(\Delta \|_{\text {IND }}\right)$ that can be expected for different load currents. The curve also shows how the peak-to-peak inductor ripple current ( $\Delta l_{\text {IND }}$ ) changes as you go from the lower border to the upper border (for a given load current) within an inductance region. The upper border represents a higher input voltage, while the lower border represents a lower input voltage (see Inductor Selection Guides).
These curves are only correct for continuous mode operation, and only if the inductor selection guides are used to select the inductor value
Consider the following example:
$\mathrm{V}_{\mathrm{OUT}}=5 \mathrm{~V}$, maximum load current of 800 mA
$\mathrm{~V}_{\mathrm{IN}}=12 \mathrm{~V}$, nominal, varying between 10 V and 14 V.

The selection guide in Figure 5 shows that the vertical line for a 0.8A load current, and the horizontal line for the 12 V input voltage intersect approximately midway between the upper and lower borders of the $68 \mu \mathrm{H}$ inductance region. A $68 \mu \mathrm{H}$ inductor will allow a peak-to-peak inductor current ( $\Delta l_{\text {IND }}$ ) to flow that will be a percentage of the maximum load current. Referring to Figure 20, follow the 0.8A line approximately midway into the inductance region, and read the peak-to-peak inductor ripple current $\left(\Delta I_{I N D}\right)$ on the left hand axis (approximately $300 \mathrm{~mA} p-\mathrm{p}$ ).
As the input voltage increases to 14 V , it approaches the upper border of the inductance region, and the inductor ripple current increases. Referring to the curve in Figure 20, it can be seen that for a load current of 0.8 A , the peak-topeak inductor ripple current ( $\Delta I_{\mathrm{IND}}$ ) is 300 mA with 12 V in, and can range from 340 mA at the upper border ( 14 V in ) to 225 mA at the lower border (10V in).

Once the $\Delta l_{\text {IND }}$ value is known, the following formulas can be used to calculate additional information about the switching regulator circuit.

1. Peak Inductor or peak switch current

$$
=\left(\mathrm{I}_{\mathrm{LOAD}}+\frac{\Delta \mathrm{I}_{\mathrm{IND}}}{2}\right)=\left(0.8 \mathrm{~A}+\frac{0.3}{2}\right)=0.95 \mathrm{~A}
$$

2. Minimum load current before the circuit becomes discontinuous

$$
=\frac{\Delta l_{\mathrm{IND}}}{2}=\frac{0.3}{2}=0.15 \mathrm{~A}
$$

3. Output Ripple Voltage $=\left(\Delta I_{\text {IND }}\right) \times\left(E S R\right.$ of $\left.C_{\text {OUT }}\right)$

$$
=0.3 \mathrm{~A} \times 0.16 \Omega=48 \mathrm{mV} p-\mathrm{p}
$$

4. ESR of $\mathrm{C}_{\text {OUT }}=\frac{\text { Output Ripple Voltage }\left(\Delta \mathrm{V}_{\text {OUT }}\right)}{\Delta \mathrm{I}_{\text {IND }}}$

$$
=\frac{0.048 \mathrm{~V}}{0.30 \mathrm{~A}}=0.16 \Omega
$$

## OPEN CORE INDUCTORS

Another possible source of increased output ripple voltage or unstable operation is from an open core inductor. Ferrite bobbin or stick inductors have magnetic lines of flux flowing through the air from one end of the bobbin to the other end. These magnetic lines of flux will induce a voltage into any wire or PC board copper trace that comes within the inductor's magnetic field. The strength of the magnetic field, the orientation and location of the PC copper trace to the magnetic field, and the distance between the copper trace and the inductor, determine the amount of voltage generated in the copper trace. Another way of looking at this inductive coupling is to consider the PC board copper trace as one turn of a transformer (secondary) with the inductor winding as the primary. Many millivolts can be generated in a copper trace located near an open core inductor which can cause stability problems or high output ripple voltage problems.
If unstable operation is seen, and an open core inductor is used, it's possible that the location of the inductor with respect to other PC traces may be the problem. To determine if this is the problem, temporarily raise the inductor away from the board by several inches and then check circuit operation. If the circuit now operates correctly, then the magnetic flux from the open core inductor is causing the problem. Substituting a closed core inductor such as a torroid or E-core will correct the problem, or re-arranging the PC layout may be necessary. Magnetic flux cutting the IC device ground trace, feedback trace, or the positive or negative traces of the output capacitor should be minimized.
Sometimes, locating a trace directly beneath a bobbin inductor will provide good results, provided it is exactly in the center of the inductor (because the induced voltages cancel themselves out), but if it is off center one direction or the other, then problems could arise. If flux problems are present, even the direction of the inductor winding can make a difference in some circuits.
This discussion on open core inductors is not to frighten the user, but to alert the user on what kind of problems to watch out for when using them. Open core bobbin or "stick" inductors are an inexpensive, simple way of making a compact efficient inductor, and they are used by the millions in many different applications.

## Application Information (Continued)



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| Circuit Data for Temperature Rise Curve TO-220 Package (T) |  |
| :--- | :--- |
| Capacitors | Through hole electrolytic |
| Inductor | Through hole, Schott, 68 $\mu \mathrm{H}$ |
| Diode | Through hole, 3A 40V, Schottky |
| PC board | 3 square inches single sided 2 oz. copper <br> $\left(0.0028^{\prime \prime}\right)$ |

FIGURE 21. Junction Temperature Rise, TO-220


TL/H/12593-39

| Circuit Data for Temperature Rise Curve TO-263 Package (S) |  |
| :--- | :--- |
| Capacitors | Surface mount tantalum, molded "D" size |
| Inductor | Surface mount, Schott, $68 \mu \mathrm{H}$ |
| Diode | Surface mount, 3A 40V, Schottky |
| PC board | 3 square inches single sided 2 oz. copper <br> $(0.0028$ " $)$ |

FIGURE 22. Junction Temperature Rise, TO-263

## THERMAL CONSIDERATIONS

The LM2598 is available in two packages, a 7-pin TO-220 ( T ) and a 7-pin surface mount TO-263 (S).
The TO-220 package can be used without a heat sink for ambient temperatures up to approximately $50^{\circ} \mathrm{C}$ (depending on the output voltage and load current). The curves in Figure 21 show the LM2598T junction temperature rises above ambient temperature for different input and output voltages. The data for these curves was taken with the LM2598T (TO220 package) operating as a switching regulator in an ambient temperature of $25^{\circ} \mathrm{C}$ (still air). These temperature rise numbers are all approximate and there are many factors that can affect these temperatures. Higher ambient temperatures require some heat sinking, either to the PC board or a small external heat sink.
The TO-263 surface mount package tab is designed to be soldered to the copper on a printed circuit board. The copper and the board are the heat sink for this package and the other heat producing components, such as the catch diode and inductor. The PC board copper area that the package is soldered to should be at least $0.4 \mathrm{in}^{2}$, and ideally should have 2 or more square inches of 2 oz . ( 0.0028 ) in) copper. Additional copper area improves the thermal characteristics, but with copper areas greater than approximately 3 in ${ }^{2}$, only small improvements in heat dissipation are realized. If further thermal improvements are needed, double sided or multilayer PC-board with large copper areas are recommended.
The curves shown in Figure 22 show the LM2598S (TO-263 package) junction temperature rise above ambient temperature with a 1A load for various input and output voltages. This data was taken with the circuit operating as a buck switching regulator with all components mounted on a PC board to simulate the junction temperature under actual operating conditions. This curve can be used for a quick check for the approximate junction temperature for various conditions, but be aware that there are many factors that can affect the junction temperature.
For the best thermal performance, wide copper traces and generous amounts of printed circuit board copper should be used in the board layout. (One exception to this is the output (switch) pin, which should not have large areas of copper.) Large areas of copper provide the best transfer of heat (lower thermal resistance) to the surrounding air, and moving air lowers the thermal resistance even further.
Package thermal resistance and junction temperature rise numbers are all approximate, and there are many factors that will affect these numbers. Some of these factors include board size, shape, thickness, position, location, and even board temperature. Other factors are, trace width, total printed circuit copper area, copper thickness, single- or dou-ble-sided, multilayer board and the amount of solder on the board. The effectiveness of the PC board to dissipate heat also depends on the size, quantity and spacing of other components on the board, as well as whether the surrounding air is still or moving. Furthermore, some of these components such as the catch diode will add heat to the PC board and the heat can vary as the input voltage changes. For the inductor, depending on the physical size, type of core material and the DC resistance, it could either act as a heat sink taking heat away from the board, or it could add heat to the board.

## Application Information (Continued)

## SHUTDOWN/SOFT-START

The circuit shown in Figure 23 is a standard buck regulator with 24 V in, 12 V out, 280 mA load, and using a $0.068 \mu \mathrm{~F}$ Soft-start capacitor. The photo in Figures 24 and 25 show the effects of Soft-start on the output voltage, the input current, with, and without a Soft-start capacitor. Figure 24 also shows the error flag output going high when the output voltage reaches $95 \%$ of the nominal output voltage. The reduced input current required at startup is very evident when comparing the two photos. The Soft-start feature reduces the startup current from 1A down to 240 mA , and delays and slows down the output voltage rise time.
This reduction in start up current is useful in situations where the input power source is limited in the amount of current it can deliver. In some applications Soft-start can be used to replace undervoltage lockout or delayed startup functions.
If a very slow output voltage ramp is desired, the Soft-start capacitor can be made much larger. Many seconds or even minutes are possible.

If only the shutdown feature is needed, the Soft-start capactor can be eliminated.


FIGURE 24. Output Voltage, Input Current, Error Flag Signal, at Start-Up, WITH Soft-start


FIGURE 25. Output Voltage, Input Current, at Start-Up, WITHOUT Soft-start


## Application Information (Continued)



## INVERTING REGULATOR

The circuit in Figure 26 converts a positive input voltage to a negative output voltage with a common ground. The circuit operates by bootstrapping the regulators ground pin to the negative output voltage, then grounding the feedback pin, the regulator senses the inverted output voltage and regulates it.
This example uses the LM2598-5 to generate a -5 V output, but other output voltages are possible by selecting other output voltage versions, including the adjustable version. Since this regulator topology can produce an output voltage that is either greater than or less than the input voltage, the maximum output current greatly depends on both the input and output voltage. The curve shown in Figure 27 provides a guide as to the amount of output load current possible for the different input and output voltage conditions.
The maximum voltage appearing across the regulator is the absolute sum of the input and output voltage, and this must be limited to a maximum of 40 V . In this example, when converting +20 V to -5 V , the regulator would see 25 V between the input pin and ground pin. The LM2598 has a maximum input voltage rating of 40 V .


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FIGURE 27. Maximum Load Current for Inverting Regulator Circuit

## Application Information (Continued)

## undervoltage lockout

Some applications require the regulator to remain off until the input voltage reaches a predetermined voltage. Figure 28 contains a undervoltage lockout circuit for a buck configuration, while Figures 29 and 30 are for the inverting types (only the circuitry pertaining to the undervoltage lockout is shown). Figure 28 uses a zener diode to establish the threshold voltage when the switcher begins operating. When the input voltage is less than the zener voltage, resistors R1 and R2 hold the Shutdown/Soft-start pin low, keeping the regulator in the shutdown mode. As the input voltage exceeds the zener voltage, the zener conducts, pulling the Shutdown/Soft-start pin high, allowing the regulator to begin switching. The threshold voltage for the undervoltage lockout feature is approximately 1.5 V greater than the zener voltage.


TL/H/12593-45
FIGURE 28. Undervoltage Lockout for a Buck Regulator
Figures 29 and 30 apply the same feature to an inverting circuit. Figure 29 features a constant threshold voltage for turn on and turn off (zener voltage plus approximately one volt). Since the $\overline{\mathrm{SD}} / \mathrm{SS}$ pin has an internal 7 V zener clamp, R2 is needed to limit the current into this pin to approximately 1 mA when Q1 is on. If hysteresis is needed, the circuit in Figure 30 has a turn ON voltage which is different than the turn OFF voltage. The amount of hysteresis is approximately equal to the value of the output voltage.


TL/H/12593-47
FIGURE 29. Undervoltage Lockout Without Hysteresis for an Inverting Regulator


TL/H/12593-46
FIGURE 30. Undervoltage Lockout With Hysteresis for an Inverting Regulator

## NEGATIVE VOLTAGE CHARGE PUMP

Occasionally a low current negative voltage is needed for biasing parts of a circuit. A simple method of generating a negative voltage using a charge pump technique and the switching waveform present at the OUT pin, is shown in Figure 31. This unregulated negative voltage is approximately equal to the positive input voltage (minus a few volts), and can supply up to a 200 mA of output current. There is a requirement however, that there be a minimum load of several hundred mA on the regulated positive output for the charge pump to work correctly. Also, resistor R1 is required to limit the charging current of C 1 to some value less than the LM2598 current limit (typically 1.5A).

This method of generating a negative output voltage without an additional inductor can be used with other members of the Simple Switcher Family, using either the buck or boost topology.


FIGURE 31. Charge Pump for Generating a Low Current, Negative Output Voltage

## Application Information (Continued)

TYPICAL THROUGH HOLE PC BOARD LAYOUT, FIXED OUTPUT (1X SIZE), DOUBLE SIDED, THROUGH HOLE PLATED
 THROUGH HOLE PLATED

$\mathrm{C}_{\mathrm{IN}}-150 \mu \mathrm{~F} / 50 \mathrm{~V}$, Aluminum Electrolytic, Panasonic "HFQ series"
CoUT-120 $\mu \mathrm{F} / 25 \mathrm{~V}$ Aluminum Electrolytic, Panasonic "HFQ series"
D1-3A, 40V Schottky Rectifier, 1N5822
L1-68 $\mu \mathrm{H}$, L30, Renco, Through hole
R1—1 k $\Omega, 1 \%$
R2-Use formula in Design Procedure
$\mathrm{C}_{\mathrm{FF}}$-See Figure 4.
RFF-See Application Information Section (C $\mathrm{C}_{\mathrm{FF}}$ Section)


RPULL-UP-10 k $\Omega$
TL/H/12593-52
$C_{\text {DeLAY }}-0.1 \mu \mathrm{~F}$
C $\overline{S D} / S S-0.1 \mu \mathrm{~F}$
_ On)

FIGURE 32. PC Board Layout

## Physical Dimensions inches (millimeters) unless otherwise noted



Physical Dimensions inches (millimeters) unless otherwise noted (Continued)


7-Lead TO-263 Surface Mount Package (S) Order Number LM2598S-3.3, LM2598S-5.0, LM2598S-12 or LM2598S-ADJ NS Package Number TS7B

## LIFE SUPPORT POLICY

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| :---: | :---: | :---: | :---: |

by current. Self protection features include a two stage current limit for the output switch and an over temperature shutdown for complete protection under fault conditions.

## Features

- 3.3V, $5 \mathrm{~V}, 12 \mathrm{~V}$, and adjustable output versions
- Adjustable version output voltage range, 1.2 V to 37 V $\pm 4 \%$ max over line and load conditions
- Guaranteed 3A output current
- Available in 7-pin TO-220 and TO-263 (surface mount) Package
- Input voltage range up to 40 V
- 150 kHz fixed frequency internal oscillator
- Shutdown/Soft-start
- Out of regulation error flag
- Error output delay
- Low power standby mode, $\mathrm{I}_{\mathrm{Q}}$ typically $80 \mu \mathrm{~A}$
- High Efficiency
- Uses readily available standard inductors
- Thermal shutdown and current limit protection


## Applications

■ Simple high-efficiency step-down (buck) regulator

- Efficient pre-regulator for linear regulators
- On-card switching regulators
- Positive to Negative converter

Other features include a guaranteed $\pm 4 \%$ tolerance on output voltage under all conditions of input voltage and output load conditions, and $\pm 15 \%$ on the oscillator frequency. External shutdown is included, featuring typically $80 \mu \mathrm{~A}$ stand-

Typical Application (Fixed Output Voltage Versions)


TL/H/12582-1

[^6]SIMPLE SWITCHER ${ }^{\text {® }}$ and Switchers Made Simple® are registered trademarks of National Semiconductor Corporation.

## Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required please contact the National Semiconductor Sales Office/Distributors for availability and specifications.
Maximum Supply Voltage ( $\mathrm{V}_{\mathrm{IN}}$ ) 45V
$\overline{\text { SD/SS Pin Input Voltage (Note 2) 6V }}$
Delay Pin Voltage (Note 2) 1.5V
Flag Pin Voltage $\quad-0.3 \leq \mathrm{V} \leq 45 \mathrm{~V}$
Feedback Pin Voltage $\quad-0.3 \leq \mathrm{V} \leq+25 \mathrm{~V}$
Output Voltage to Ground (Steady State) -1V
Power Dissipation
Internally limited
Storage Temperature Range $\quad-65^{\circ} \mathrm{C}$ to $+150^{\circ} \mathrm{C}$
ESD Susceptibility
Human Body Model (Note 3) 2 kV

| Lead Temperature |  |
| :--- | :--- |
| S Package |  |
| $\quad$ Vapor Phase ( 60 sec.) | $+215^{\circ} \mathrm{C}$ |
| $\quad$ Infrared (10 sec.) | $+245^{\circ} \mathrm{C}$ |
| T Package (Soldering, 10 sec.) | $+260^{\circ} \mathrm{C}$ |
| Maximum Junction Temperature | $+150^{\circ} \mathrm{C}$ |

## Operating Conditions

Temperature Range $\quad-40^{\circ} \mathrm{C} \leq \mathrm{T}_{\mathrm{J}} \leq+125^{\circ} \mathrm{C}$
Supply Voltage 4.5 V to 40 V

## LM2599-3.3

Electrical Characteristics Specifications with standard type face are for $\mathrm{T}_{\mathrm{J}}=22^{\circ} \mathrm{C}$, and those with boldface type apply over full Operating Temperature Range.

| Symbol | Parameter | Conditions | LM2599-3.3 |  | Units (Limits) |
| :---: | :---: | :---: | :---: | :---: | :---: |
|  |  |  | Typ (Note 4) | Limit (Note 5) |  |
| SYSTEM PARAMETERS (Note 6) Test Circuit Figure 1 |  |  |  |  |  |
| V OUT | Output Voltage | $4.75 \mathrm{~V} \leq \mathrm{V}_{\mathrm{IN}} \leq 40 \mathrm{~V}, 0.2 \mathrm{~A} \leq \mathrm{I}_{\text {LOAD }} \leq 3 \mathrm{~A}$ | 3.3 | $\begin{aligned} & 3.168 / \mathbf{3 . 1 3 5} \\ & 3.432 / \mathbf{3 . 4 6 5} \end{aligned}$ |  |
| $\eta$ | Efficiency | $\mathrm{V}_{\text {IN }}=12 \mathrm{~V}, \mathrm{I}_{\text {LOAD }}=3 \mathrm{~A}$ | 73 |  | \% |

LM2599-5.0
Electrical Characteristics Specifications with standard type face are for $\mathrm{T}_{\mathrm{J}}=25^{\circ} \mathrm{C}$, and those with boldface type apply over full Operating Temperature Range.

| Symbol | Parameter | Conditions | LM2599-5.0 |  | Units (Limits) |
| :---: | :---: | :---: | :---: | :---: | :---: |
|  |  |  | $\begin{gathered} \text { Typ } \\ \text { (Note 4) } \end{gathered}$ | Limit (Note 5) |  |
| SYSTEM PARAMETERS (Note 6) Test Circuit Figure 1 |  |  |  |  |  |
| $\mathrm{V}_{\text {OUT }}$ | Output Voltage | $7 \mathrm{~V} \leq \mathrm{V}_{\text {IN }} \leq 40 \mathrm{~V}, 0.2 \mathrm{~A} \leq \mathrm{I}_{\text {LOAD }} \leq 3 \mathrm{~A}$ | 5 | $\begin{aligned} & 4.800 / 4.750 \\ & 5.200 / \mathbf{5 . 2 5 0} \end{aligned}$ | $V(\min )$ <br> V (max) |
| $\eta$ | Efficiency | $\mathrm{V}_{\text {IN }}=12 \mathrm{~V}, \mathrm{I}_{\text {LOAD }}=3 \mathrm{~A}$ | 80 |  | \% |

LM2599-12
Electrical Characteristics Specifications with standard type face are for $\mathrm{T}_{\mathrm{J}}=25^{\circ} \mathrm{C}$, and those with boldface type apply over full Operating Temperature Range.

| Symbol | Parameter | Conditions | LM2599-12 |  | Units |
| :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | Typ <br> (Note 4) | Limit <br> (Note 5) |  |  |

SYSTEM PARAMETERS (Note 6) Test Circuit Figure 1

| $V_{\text {OUT }}$ | Output Voltage | $15 \mathrm{~V} \leq \mathrm{V}_{\text {IN }} \leq 40 \mathrm{~V}, 0.2 \mathrm{~A} \leq \mathrm{I}_{\text {LOAD }} \leq 3 \mathrm{~A}$ | 12 |  | V |
| :---: | :--- | :--- | :---: | :---: | :---: |
|  |  |  |  | $11.52 / \mathbf{1 1 . 4 0}$ | $\mathrm{V}(\mathrm{min})$ |
| $\eta$ | Efficiency | $\mathrm{V}_{\text {IN }}=25 \mathrm{~V}, \mathrm{I}_{\text {LOAD }}=3 \mathrm{~A}$ | 90 |  | $\%$ |

## LM2599-ADJ

Electrical Characteristics Specifications with standard type face are for $\mathrm{T}_{\mathrm{J}}=25^{\circ} \mathrm{C}$, and those with boldface type apply over full Operating Temperature Range.

| Symbol | Parameter | Conditions | LM2599-ADJ |  | Units (Limits) |
| :---: | :---: | :---: | :---: | :---: | :---: |
|  |  |  | $\begin{gathered} \text { Typ } \\ \text { (Note 4) } \end{gathered}$ | Limit (Note 5) |  |
| SYSTEM PARAMETERS (Note 6) Test Circuit Figure 1 |  |  |  |  |  |
| $\mathrm{V}_{\mathrm{FB}}$ | Feedback Voltage | $\begin{aligned} & 4.5 \mathrm{~V} \leq \mathrm{V}_{\text {IN }} \leq 40 \mathrm{~V}, 0.2 \mathrm{~A} \leq \mathrm{I} \text { LOAD } \leq 3 \mathrm{~A} \\ & \mathrm{~V}_{\text {OUT }} \text { programmed for } 3 \mathrm{~V} \text {. Circuit of Figure } 1 . \end{aligned}$ | 1.230 | $\begin{aligned} & 1.193 / \mathbf{1 . 1 8 0} \\ & 1.267 / \mathbf{1 . 2 8 0} \end{aligned}$ |  |
| $\eta$ | Efficiency | $\mathrm{V}_{\text {IN }}=12 \mathrm{~V}, \mathrm{~V}_{\text {OUT }}=3 \mathrm{~V}, \mathrm{I}_{\text {LOAD }}=3 \mathrm{~A}$ | 73 |  | \% |

## All Output Voltage Versions

Electrical Characteristics Specifications with standard type face are for $\mathrm{T}^{\mathrm{J}}=25^{\circ} \mathrm{C}$, and those with boldface
type apply over full Operating Temperature Range. Unless otherwise specified, $\mathrm{V}_{\mathrm{IN}}=12 \mathrm{~V}$ for the 3.3 V , 5 V , and Adjustable version and $\mathrm{V}_{\mathrm{IN}}=24 \mathrm{~V}$ for the 12 V version. ILOAD $=500 \mathrm{~mA}$

| Symbol | Parameter | Conditions | LM2599-XX |  | Units |
| :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | Typ <br> (Note 4) | Limit <br> (Note 5) |  |  |

## DEVICE PARAMETERS

| $\mathrm{l}_{\mathrm{b}}$ | Feedback Bias Current | Adjustable Version Only, $\mathrm{V}_{\mathrm{FB}}=1.3 \mathrm{~V}$ | 10 | 50/100 | $\begin{gathered} \mathrm{nA} \\ \mathrm{nA}(\max ) \end{gathered}$ |
| :---: | :---: | :---: | :---: | :---: | :---: |
| $\mathrm{f}_{\mathrm{O}}$ | Oscillator Frequency | (Note 7) | 150 | $\begin{aligned} & 127 / 110 \\ & 173 / 173 \\ & \hline \end{aligned}$ | $\begin{gathered} \mathrm{kHz} \\ \mathrm{kHz}(\min ) \\ \mathrm{kHz}(\max ) \\ \hline \end{gathered}$ |
| $\mathrm{V}_{\text {SAT }}$ | Saturation Voltage | IOUT $=3 \mathrm{~A}($ Notes 8 and 9) | 1.16 | 1.4/1.5 | $\begin{gathered} V \\ V(\max ) \end{gathered}$ |
| DC | Max Duty Cycle (ON) <br> Min Duty Cycle (OFF) | (Note 9) <br> (Note 10) | $\begin{gathered} 100 \\ 0 \\ \hline \end{gathered}$ |  | \% |
| $\mathrm{I}_{\mathrm{CL}}$ | Current Limit | Peak Current, (Notes 8 and 9) | 4.5 | $\begin{aligned} & 3.6 / 3.4 \\ & 6.9 / 7.5 \end{aligned}$ |  |
| $\mathrm{I}_{\mathrm{L}}$ | Output Leakage Current | $\begin{array}{ll} (\text { Notes } 8,10 \text { and 11) } & \text { Output }=0 \mathrm{~V} \\ \text { Output }=-1 \mathrm{~V} \end{array}$ | 2 | $\begin{aligned} & 50 \\ & 30 \end{aligned}$ | $\begin{gathered} \mu \mathrm{A}(\max ) \\ \mathrm{mA} \\ \mathrm{~mA}(\max ) \end{gathered}$ |
| $\mathrm{I}_{\mathrm{Q}}$ | Operating Quiescent Current | $\overline{\text { SD/SS Pin Open (Note 10) }}$ | 5 | 10 | $\begin{gathered} \mathrm{mA} \\ \mathrm{~mA}(\max ) \end{gathered}$ |
| Istby | Standby Quiescent Current | $\overline{\mathrm{SD}} / \mathrm{SS}$ pin $=0 \mathrm{~V} \quad($ Note 11) | 80 | 200/250 | $\begin{gathered} \mu \mathrm{A} \\ \mu \mathrm{~A}(\mathrm{max}) \end{gathered}$ |
| $\begin{aligned} & \theta_{\mathrm{JC}} \\ & \theta_{\mathrm{JA}} \\ & \theta_{\mathrm{JA}} \\ & \theta_{\mathrm{JA}} \\ & \theta_{\mathrm{JA}} \\ & \hline \end{aligned}$ | Thermal Resistance | TO220 or TO263 Package, Junction to Case TO220 Package, Juncton to Ambient (Note 12) TO263 Package, Juncton to Ambient (Note 13) TO263 Package, Juncton to Ambient (Note 14) TO263 Package, Juncton to Ambient (Note 15) | $\begin{gathered} 2 \\ 50 \\ 50 \\ 30 \\ 20 \end{gathered}$ |  | ${ }^{\circ} \mathrm{C} / \mathrm{W}$ <br> ${ }^{\circ} \mathrm{C} / \mathrm{W}$ <br> ${ }^{\circ} \mathrm{C} / \mathrm{W}$ <br> ${ }^{\circ} \mathrm{C} / \mathrm{W}$ <br> ${ }^{\circ} \mathrm{C} / \mathrm{W}$ |

## All Output Voltage Versions (Continued)

Electrical Characteristics Specifications with standard type face are for $\mathrm{T}_{\mathrm{J}}=25^{\circ} \mathrm{C}$, and those with boldface type apply over full Operating Temperature Range. Unless otherwise specified, $\mathrm{V}_{\mathbb{I N}}=12 \mathrm{~V}$ for the $3.3 \mathrm{~V}, 5 \mathrm{~V}$, and Adjustable version and $\mathrm{V}_{\mathrm{IN}}=24 \mathrm{~V}$ for the 12 V version. ILOAD $=500 \mathrm{~mA}$

| Symbol | Parameter | Conditions | LM2599-XX |  | Units <br> (Limits) |
| :---: | :---: | :---: | :---: | :---: | :---: |
|  |  |  |  | Limit (Note 5) |  |
| SHUTDOWN/SOFT-START CONTROL Test Circuit of Figure 1 |  |  |  |  |  |
| $\mathrm{V}_{\text {SD }}$ | Shutdown Threshold Voltage | Low, (Shutdown Mode) <br> High, (Soft-start Mode) | 1.3 | $\begin{gathered} 0.6 \\ 2 \end{gathered}$ |  |
| $\mathrm{V}_{\text {SS }}$ | Soft-start Voltage | $\mathrm{V}_{\text {OUT }}=20 \%$ of Nominal Output Voltage <br> $V_{\text {OUT }}=100 \%$ of Nominal Output Voltage | $\begin{aligned} & 2 \\ & 3 \end{aligned}$ |  | V |
| ${ }_{\text {ISD }}$ | Shutdown Current | $\mathrm{V}_{\overline{\text { SHUTDOWN }}}=0.5 \mathrm{~V}$ | 5 | 10 | $\begin{gathered} \mu \mathrm{A} \\ \mu \mathrm{~A}(\max ) \end{gathered}$ |
| Iss | Soft-start Current | $\mathrm{V}_{\text {Soft-start }}=2.5 \mathrm{~V}$ | 1.6 | 5 | $\begin{gathered} \mu \mathrm{A} \\ \mu \mathrm{~A}(\text { max }) \end{gathered}$ |

FLAG/DELAY CONTROL Test Circuit of Figure 1

|  | Regulator Dropout Detector Threshold Voltage | Low (Flag ON) | 96 | $\begin{aligned} & 92 \\ & 98 \end{aligned}$ | $\begin{gathered} \% \\ \%(\min ) \\ \%(\max ) \\ \hline \end{gathered}$ |
| :---: | :---: | :---: | :---: | :---: | :---: |
| VFSAT | Flag Output Saturation Voltage | $\begin{aligned} & \mathrm{I}_{\mathrm{SINK}}=3 \mathrm{~mA} \\ & \mathrm{~V}_{\text {DELAY }}=0.5 \mathrm{~V} \end{aligned}$ | 0.3 | 0.7/1.0 | $\begin{gathered} \mathrm{V} \\ \mathrm{~V}(\max ) \\ \hline \end{gathered}$ |
| $\mathrm{IF}_{\mathrm{L}}$ | Flag Output Leakage Current | $\mathrm{V}_{\mathrm{FLAG}}=40 \mathrm{~V}$ | 0.3 |  | $\mu \mathrm{A}$ |
|  | Delay Pin Threshold Voltage | Low (Flag ON) <br> High (Flag OFF) and $\mathrm{V}_{\text {OUT }}$ Regulated | 1.25 | $\begin{aligned} & 1.21 \\ & 1.29 \end{aligned}$ |  |
|  | Delay Pin Source Current | $\mathrm{V}_{\text {DELAY }}=0.5 \mathrm{~V}$ | 3 | 6 | $\begin{gathered} \mu \mathrm{A} \\ \mu \mathrm{~A}(\max ) \end{gathered}$ |
|  | Delay Pin Saturation | Low (Flag ON) | 55 | 350/400 | $\begin{gathered} \mathrm{mV} \\ \mathrm{mV}(\max ) \end{gathered}$ |

## Electrical Characteristics (Continued)

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but do not guarantee specific performance limits. For guaranteed specifications and test conditions, see the Electrical Characteristics.
Note 2: Voltage internally clamped. If clamp voltage is exceeded, limit current to a maximum of 1 mA .
Note 3: The human body model is a 100 pF capacitor discharged through a 1.5 k resistor into each pin.
Note 4: Typical numbers are at $25^{\circ} \mathrm{C}$ and represent the most likely norm.
Note 5: All limits guaranteed at room temperature (standard type face) and at temperature extremes (bold type face). All room temperature limits are 100\% production tested. All limits at temperature extremes are guaranteed via correlation using standard Statistical Quality Control (SQC) methods. All limits are used to calculate Average Outgoing Quality Level (AOQL).
Note 6: External components such as the catch diode, inductor, input and output capacitors can affect switching regulator system performance. When the LM2599 is used as shown in the Figure 1 test circuit, system performance will be as shown in system parameters section of Electrical Characteristics.
Note 7: The switching frequency is reduced when the second stage current limit is activated. The amount of reduction is determined by the severity of current overload.
Note 8: No diode, inductor or capacitor connected to output pin
Note 9: Feedback pin removed from output and connected to OV to force the output transistor switch ON.
Note 10: Feedback pin removed from output and connected to 12 V for the $3.3 \mathrm{~V}, 5 \mathrm{~V}$, and the ADJ. version, and 15 V for the 12 V version, to force the output transistor switch OFF.
Note 11: $\mathrm{V}_{\mathbb{I N}}=40 \mathrm{~V}$.
Note 12: Junction to ambient thermal resistance (no external heat sink) for the package mounted TO-220 package mounted vertically, with the leads soldered to a printed circuit board with ( 1 oz .) copper area of approximately $1 \mathrm{in}^{2}$.
Note 13: Junction to ambient thermal resistance with the TO-263 package tab soldered to a single sided printed circuit board with $0.5 \mathrm{in}{ }^{2}$ of ( 1 oz .) copper area. Note 14: Junction to ambient thermal resistance with the TO-263 package tab soldered to a single sided printed circuit board with 2.5 in 2 of ( 1 oz .) copper area. Note 15: Junction to ambient thermal resistance with the TO-263 package tab soldered to a double sided printed circuit board with 3 in ${ }^{2}$ of ( 1 oz .) copper area on the LM2599S side of the board, and approximately $16 \mathrm{in}^{2}$ of copper on the other side of the p-c board. See application hints in this data sheet and the thermal model in Switchers Made Simple version 4.3 software.

## Typical Performance Characteristics (Circuit of Figure 1)



Switch Saturation Voltage


Line Regulation


TL/H/12582-3

Switch Current Limit


Efficiency




## Typical Performance Characteristics (Circuit of Figure 1)

Continuous Mode Switching Waveforms
$\mathrm{V}_{\text {IN }}=20 \mathrm{~V}, \mathrm{~V}_{\text {OUT }}=5 \mathrm{~V}, \mathrm{I}_{\text {LOAD }}=2 \mathrm{~A}$
$\mathbf{L}=\mathbf{3 2 \mu H}$, C OUT $=220 \mu \mathrm{~F}$, C OUT ESR $=50 \mathrm{~m} \Omega$


A: Output Pin Voltage, 10V/div.
B: Inductor Current 1A/div.
C: Output Ripple Voltage, $50 \mathrm{mV} / \mathrm{div}$.
Horizontal Time Base: $\mathbf{2 \mu s} /$ div.

Load Transient Response for Continuous Mode
$\mathrm{V}_{\mathrm{IN}}=20 \mathrm{~V}, \mathrm{~V}_{\text {OUT }}=5 \mathrm{~V}, \mathrm{I}_{\text {LOAD }}=500 \mathrm{~mA}$ to 2 A
L $=\mathbf{3 2} \mu \mathrm{H}$, C OUT $=220 \mu \mathrm{~F}$, C OUT ESR $=50 \mathrm{~m} \Omega$


Discontinuous Mode Switching Waveforms
$\mathrm{V}_{\text {IN }}=20 \mathrm{~V}, \mathrm{~V}_{\text {OUT }}=5 \mathrm{~V}, \mathrm{I}_{\text {LOAD }}=500 \mathrm{~mA}$
$\mathrm{L}=10 \mu \mathrm{H}$, C OUT $=330 \mu \mathrm{~F}, \mathrm{C}_{\text {OUT }} \mathrm{ESR}=45 \mathrm{~m} \Omega$


A: Output Pin Voltage, 10V/div.
B: Inductor Current $0.5 \mathrm{~A} /$ div.
C: Output Ripple Voltage, $100 \mathrm{mV} /$ div. Horizontal Time Base: $2 \mu \mathrm{~s} /$ div.

Load Transient Response for Discontinuous Mode
$\mathrm{V}_{\mathrm{IN}}=\mathbf{2 0 V}, \mathrm{V}_{\text {OUT }}=5 \mathrm{~V}$, $\mathrm{I}_{\text {LOAD }}=500 \mathrm{~mA}$ to 2 A $L=10 \mu \mathrm{H}$, Cout $=330 \mu \mathrm{~F}$, C OUt $\mathrm{ESR}=45 \mathrm{~m} \Omega$


A: Output Voltage, $100 \mathrm{mV} /$ div. (AC)
B: 500 mA to 2A Load Pulse
Horizontal Time Base: $200 \mu \mathrm{~s} /$ div.

## Connection Diagrams and Order Information

Bent and Staggered Leads, Through Hole Package 7-Lead TO-220 (T)


TL/H/12582-50
Order Number LM2599T-3.3, LM2599T-5.0,
LM2599T-12 or LM2599T-ADJ
See NS Package Number TA07B


TL/H/12582-23
Order Number LM2599S-3.3, LM2599S-5.0,
LM2599S-12 or LM2599S-ADJ
See NS Package Number TS7B

## Test Circuit and Layout Guidelines



```
Component Values shown are for }\mp@subsup{\textrm{V}}{IN}{}=15\textrm{V}\mathrm{ ,
V OUT }=5\textrm{V},\mp@subsup{I}{\mathrm{ LOAD }}{}=3\textrm{A}
C
    Nichicon "PL Series"
COUT - 220 \muF,25V Aluminum Electrolytic,
    Nichicon "PL Series"
D1 - 5A, 40V Schottky Rectifier, 1N5825
L1 -68 \muH, L38
COUT - \(220 \mu \mathrm{~F}, 25 \mathrm{~V}\) Aluminum Electrolytic, Nichicon "PL Series"
L1 \(\quad-68 \mu \mathrm{H}, \mathrm{L} 38\)
```

$$
\begin{aligned}
& \text { Typical Values } \\
& \mathrm{C}_{S S} \quad-0.1 \mu \mathrm{~F} \\
& \mathrm{C}_{\text {DELAY }} \\
& \text { RPull Up }-0.1 \mu \mathrm{~F} \\
& \hline
\end{aligned}
$$



TL/H/12582-25
$\mathrm{V}_{\text {OUT }}=\mathrm{V}_{\text {REF }}\left(1+\frac{\mathrm{R}_{2}}{\mathrm{R}_{1}}\right) \quad$ where $\mathrm{V}_{\text {REF }}=1.23 \mathrm{~V}$
$R_{2}=R_{1}\left(\frac{V_{\text {OUT }}}{V_{\text {REF }}}-1\right) \quad \begin{aligned} & \text { Select } R_{1} \text { to be approximately } 1 \mathrm{k} \Omega, \\ & \text { use a } 1 \% \text { resistor for best stability. }\end{aligned}$
Component Values shown are for $\mathrm{V}_{\mathrm{IN}}=20 \mathrm{~V}$,
$\mathrm{V}_{\text {OUT }}=10 \mathrm{~V}, \mathrm{~L}_{\text {LOAD }}=3 \mathrm{~A}$.
$\mathrm{C}_{\mathrm{IN}}-470 \mu \mathrm{~F}, 35 \mathrm{~V}$, Aluminum Electrolytic Nichicon "PL Series"
COUT - $220 \mu \mathrm{~F}, 35 \mathrm{~V}$ Aluminum Electrolytic, Nichicon "PL Series"
D1 - 5A, 30V Schottky Rectifier, 1N5824

L1 - $68 \mu \mathrm{H}, \mathrm{L} 38$
$R_{1}-1 \mathrm{k} \Omega, 1 \%$
$\mathrm{R}_{2}-7.15 \mathrm{k}, 1 \%$
$\mathrm{C}_{\mathrm{FF}}-3.3 \mathrm{nF}$, See Application Information Section
$R_{\text {FF }}-3 \mathrm{k} \Omega$, See Application Information Section
Typical Values
$\mathrm{C}_{S S}-0.1 \mu \mathrm{~F}$
$C_{\text {DELAY }}-0.1 \mu \mathrm{~F}$
RPULL UP-4.7k

## FIGURE 1. Standard Test Circuits and Layout Guides

As in any switching regulator, layout is very important. Rapidly switching currents associated with wiring inductance can generate voltage transients which can cause problems. For minimal inductance and ground loops, the wires indicated by heavy lines should be wide printed circuit traces and should be kept as short as possible. For best results, external components should be located as close to the switcher IC as possible using ground plane construction or single point grounding.

If open core inductors are used, special care must be taken as to the location and positioning of this type of inductor. Allowing the inductor flux to intersect sensitive feedback, IC groundpath and Cout wiring can cause problems. When using the adjustable version, special care must be taken as to the location of the feedback resistors and the associated wiring. Physically locate both resistors near the IC, and route the wiring away from the inductor, especially an open core type of inductor. (See application section for more information.)

## LM2599 Series Buck Regulator Design Procedure (Fixed Output)

| PROCEDURE (Fixed Output Voltage Version) |
| :--- |
| Given: |
| $\mathrm{V}_{\text {OUT }}=$ Regulated Output Voltage $(3.3 \mathrm{~V}, 5 \mathrm{~V}$ or 12 V$)$ |
| $\mathrm{V}_{\text {IN }}(\max )=$ Maximum DC Input Voltage |
| $\mathrm{I}_{\text {LOAD }}(\max )=$ Maximum Load Current |

1. Inductor Selection (L1)
A. Select the correct inductor value selection guide from Figures 4, 5, or 6 . (Output voltages of $3.3 \mathrm{~V}, 5 \mathrm{~V}$, or 12 V respectively.) For all other voltages, see the design procedure for the adjustable version.
B. From the inductor value selection guide, identify the inductance region intersected by the Maximum Input Voltage line and the Maximum Load Current line. Each region is identified by an inductance value and an inductor code (LXX).
C. Select an appropriate inductor from the four manufacturer's part numbers listed in Figure 8.
2. Output Capacitor Selection (COUT)
A. In the majority of applications, low ESR (Equivalent Series Resistance) electrolytic capacitors between $82 \mu \mathrm{~F}$ and $820 \mu \mathrm{~F}$ and low ESR solid tantalum capacitors between $10 \mu \mathrm{~F}$ and $470 \mu \mathrm{~F}$ provide the best results. This capacitor should be located close to the IC using short capacitor leads and short copper traces. Do not use capacitors larger than $820 \mu \mathrm{~F}$.
For additional information, see section on output capacitors in application information section.
B. To simplify the capacitor selection procedure, refer to the quick design component selection table shown in Figure 2. This table contains different input voltages, output voltages, and load currents, and lists various inductors and output capacitors that will provide the best design solutions.
C. The capacitor voltage rating for electrolytic capacitors should be at least 1.5 times greater than the output voltage, and often much higher voltage ratings are needed to satisfy the low ESR requirements for low output ripple voltage.
D. For computer aided design software, see Switchers Made Simple ${ }^{\circledR}$ (version 4.3 or later).
3. Catch Diode Selection (D1)
A. The catch diode current rating must be at least 1.3 times greater than the maximum load current. Also, if the power supply design must withstand a continuous output short, the diode should have a current rating equal to the maximum current limit of the LM2599. The most stressful condition for this diode is an overload or shorted output condition.
B. The reverse voltage rating of the diode should be at least 1.25 times the maximum input voltage.
C. This diode must be fast (short reverse recovery time) and must be located close to the LM2599 using short leads and short printed circuit traces. Because of their fast switching speed and low forward voltage drop, Schottky diodes provide the best performance and efficiency, and should be the first choice, especially in low output voltage applications. Ultra-fast recovery, or High-

Procedure continued on next page.

EXAMPLE (Fixed Output Voltage Version)
Given:
$V_{\text {OUT }}=5 \mathrm{~V}$
$\mathrm{V}_{\mathrm{IN}}(\max )=12 \mathrm{~V}$
$\mathrm{I}_{\text {LOAD }}(\mathrm{max})=3 \mathrm{~A}$

1. Inductor Selection (L1)
A. Use the inductor selection guide for the 5 V version shown in Figure 5.
B. From the inductor value selection guide shown in Figure 5 , the inductance region intersected by the 12 V horizontal line and the 3A vertical line is $33 \mu \mathrm{H}$, and the inductor code is L40.
C. The inductance value required is $33 \mu \mathrm{H}$. From the table in Figure 8, go to the L40 line and choose an inductor part number from any of the four manufacturers shown. (In most instance, both through hole and surface mount inductors are available.)
2. Output Capacitor Selection (COUT)
A. See section on output capacitors in application information section.
B. From the quick design component selection table shown in Figure 2, locate the 5V output voltage section. In the load current column, choose the load current line that is closest to the current needed in your application, for this example, use the 3A line. In the maximum input voltage column, select the line that covers the input voltage needed in your application, in this example, use the 15 V line. Continuing on this line are recommended inductors and capacitors that will provide the best overall performance.
The capacitor list contains both through hole electrolytic and surface mount tantalum capacitors from four different capacitor manufacturers. It is recommended that both the manufacturers and the manufacturer's series that are listed in the table be used.
In this example aluminum electrolytic capacitors from several different manufacturers are available with the range of ESR numbers needed.
$330 \mu \mathrm{~F}$ 35V Panasonic HFQ Series
$330 \mu \mathrm{~F}$ 35V Nichicon PL Series
C. For a 5 V output, a capacitor voltage rating at least 7.5 V or more is needed. But even a low ESR, switching grade, $220 \mu \mathrm{~F} 10 \mathrm{~V}$ aluminum electrolytic capacitor would exhibit approximately $225 \mathrm{~m} \Omega$ of ESR (see the curve in Figure 16 for the ESR vs voltage rating). This amount of ESR would result in relatively high output ripple voltage. To reduce the ripple to $1 \%$ of the output voltage, or less, a capacitor with a higher value or with a higher voltage rating (lower ESR) should be selected. A 16 V or 25 V capacitor will reduce the ripple voltage by approximately half.
3. Catch Diode Selection (D1)
A. Refer to the table shown in Figure 11. In this example, a $5 \mathrm{~A}, 20 \mathrm{~V}$, 1N5823 Schottky diode will provide the best performance, and will not be overstressed even for a shorted output.

Example continued on next page.

## LM2599 Series Buck Regulator Design Procedure (Fixed Output) (Continued)

PROCEDURE (Fixed Output Voltage Version)

Efficiency rectifiers also provide good results. Ultra-fast recovery diodes typically have reverse recovery times of 50 ns or less. Rectifiers such as the IN5400 series are much too slow and should not be used.
4. Input Capacitor ( $\mathrm{C}_{\mathbf{I N}}$ )

A low ESR aluminum or tantalum bypass capacitor is needed between the input pin and ground to prevent large voltage transients from appearing at the input. In addition, the RMS current rating of the input capacitor should be selected to be at least $1 / 2$ the DC load current. The capacitor manufacturers data sheet must be checked to assure that this current rating is not exceeded. The curve shown in Figure 15 shows typical RMS current ratings for several different aluminum electrolytic capacitor values.
This capacitor should be located close to the IC using short leads and the voltage rating should be approximately 1.5 times the maximum input voltage.
If solid tantalum input capacitors are used, it is recomended that they be surge current tested by the manufacturer.
Use caution when using ceramic capacitors for input bypassing, because it may cause severe ringing at the $\mathrm{V}_{\mathrm{IN}}$ pin.
For additional information, see section on input capacitors in Application Information section.

EXAMPLE (Fixed Output Voltage Version)

## 4. Input Capacitor ( $\mathrm{C}_{\mathrm{IN}}$ )

The important parameters for the Input capacitor are the input voltage rating and the RMS current rating. With a nominal input voltage of 12 V , an aluminum electrolytic capacitor with a voltage rating greater than $18 \mathrm{~V}(1.5 \times$ $\mathrm{V}_{\mathrm{IN}}$ ) would be needed. The next higher capacitor voltage rating is 25 V .
The RMS current rating requirement for the input capacitor in a buck regulator is approximately $1 / 2$ the DC load current. In this example, with a 3A load, a capacitor with a RMS current rating of at least 1.5 A is needed. The curves shown in Figure 15 can be used to select an appropriate input capacitor. From the curves, locate the 35 V line and note which capacitor values have RMS current ratings greater than 1.5 A . A $680 \mu \mathrm{~F}, 35 \mathrm{~V}$ capacitor could be used.
For a through hole design, a $680 \mu \mathrm{~F} / 35 \mathrm{~V}$ electrolytic capacitor (Panasonic HFQ series or Nichicon PL series or equivalent) would be adequate. other types or other manufacturers capacitors can be used provided the RMS ripple current ratings are adequate.
For surface mount designs, solid tantalum capacitors are recommended. The TPS series available from AVX, and the 593D series from Sprague are both surge current tested.

| Conditions |  |  | Inductor |  | Output Capacitor |  |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  |  | Through Hole Electrolytic | Surface Mount Tantalum |  |
| Output Voltage (V) | Load Current (A) | Max Input Voltage (V) |  |  | Inductance ( $\mu \mathrm{H}$ ) | Inductor (\#) | Panasonic HFQ Series ( $\mu \mathrm{F} / \mathrm{V}$ ) | Nichicon PL Series ( $\mu \mathrm{F} / \mathrm{V}$ ) | AVX TPS Series ( $\mu \mathrm{F} / \mathrm{V}$ ) | Sprague 595D Series $(\mu \mathrm{F} / \mathrm{V})$ |
| 3.3 | 3 | 5 | 22 | L41 | 470/25 | 560/16 | 330/6.3 | 390/6.3 |
|  |  | 7 | 22 | L41 | 560/35 | 560/35 | 330/6.3 | 390/6.3 |
|  |  | 10 | 22 | L41 | 680/35 | 680/35 | 330/6.3 | 390/6.3 |
|  |  | 40 | 33 | L40 | 560/35 | 470/35 | 330/6.3 | 390/6.3 |
|  | 2 | 6 | 22 | L33 | 470/25 | 470/35 | 330/6.3 | 390/6.3 |
|  |  | 10 | 33 | L32 | 330/35 | 330/35 | 330/6.3 | 390/6.3 |
|  |  | 40 | 47 | L39 | 330/35 | 270/50 | 220/10 | 330/10 |
| 5 | 3 | 8 | 22 | L41 | 470/25 | 560/16 | 220/10 | 330/10 |
|  |  | 10 | 22 | L41 | 560/25 | 560/25 | 220/10 | 330/10 |
|  |  | 15 | 33 | L40 | 330/35 | 330/35 | 220/10 | 330/10 |
|  |  | 40 | 47 | L39 | 330/35 | 270/35 | 220/10 | 330/10 |
|  | 2 | 9 | 22 | L33 | 470/25 | 560/16 | 220/10 | 330/10 |
|  |  | 20 | 68 | L38 | 180/35 | 180/35 | 100/10 | 270/10 |
|  |  | 40 | 68 | L38 | 180/35 | 180/35 | 100/10 | 270/10 |
| 12 | 3 | 15 | 22 | L41 | 470/25 | 470/25 | 100/16 | 180/16 |
|  |  | 18 | 33 | L40 | 330/25 | 330/25 | 100/16 | 180/16 |
|  |  | 30 | 68 | L44 | 180/25 | 180/25 | 100/16 | 120/20 |
|  |  | 40 | 68 | L44 | 180/35 | 180/35 | 100/16 | 120/20 |
|  | 2 | 15 | 33 | L32 | 330/25 | 330/25 | 100/16 | 180/16 |
|  |  | 20 | 68 | L38 | 180/25 | 180/25 | 100/16 | 120/20 |
|  |  | 40 | 150 | L42 | 82/25 | 82/25 | 68/20 | 68/25 |

FIGURE 2. LM2599 Fixed Voltage Quick Design Component Selection Table

## LM2599 Series Buck Regulator Design Procedure (Adjustable Output)

| PROCEDURE (Adjustable Output Voltage Version) |
| :--- |
| Given: |
| V OUT $^{\prime}=$ Regulated Output Voltage |
| $\mathrm{V}_{\text {IN }}(\max )=$ Maximum Input Voltage |
| $\mathrm{I}_{\text {LOAD }}(\max )=$ Maximum Load Current |
| F $=$ Switching Frequency (Fixed at a nominal 150 kHz ). |

1. Programming Output Voltage (Selecting $R_{1}$ and $R_{2}$, as shown in Figure 1)
Use the following formula to select the appropriate resistor values.

$$
\mathrm{V}_{\mathrm{OUT}}=\mathrm{V}_{\mathrm{REF}}\left(1+\frac{\mathrm{R}_{2}}{\mathrm{R}_{1}}\right) \quad \text { where } \mathrm{V}_{\mathrm{REF}}=1.23 \mathrm{~V}
$$

Select a value for $R_{1}$ between $240 \Omega$ and $1.5 \mathrm{k} \Omega$. The lower resistor values minimize noise pickup in the sensitive feedback pin. (For the lowest temperature coefficient and the best stability with time, use $1 \%$ metal film resistors.)

$$
R_{2}=R_{1}\left(\frac{V_{\text {OUT }}}{V_{\text {REF }}}-1\right)
$$

2. Inductor Selection (L1)
A. Calculate the inductor Volt - microsecond constant $E \bullet T(V \bullet \mu s)$, from the following formula:
$E \cdot T=\left(V_{\text {IN }}-V_{\text {OUT }}-V_{S A T}\right) \cdot \frac{V_{\text {OUT }}+V_{D}}{V_{\text {IN }}-V_{S A T}+V_{D}} \cdot \frac{1000}{150 \mathrm{kHz}}(\mathrm{V} \bullet \mu \mathrm{s})$
where $\mathrm{V}_{\text {SAT }}=$ internal switch saturation voltage $=$
1.16 V and $\mathrm{V}_{\mathrm{D}}=$ diode forward voltage drop $=0.5 \mathrm{~V}$
B. Use the E - T value from the previous formula and match it with the $\mathrm{E} \cdot \mathrm{T}$ number on the vertical axis of the Inductor Value Selection Guide shown in Figure 7.
C. on the horizontal axis, select the maximum load current.
D. Identify the inductance region intersected by the $\mathrm{E} \bullet \mathrm{T}$ value and the Maximum Load Current value. Each region is identified by an inductance value and an inductor code (LXX).
E. Select an appropriate inductor from the four manufacturer's part numbers listed in Figure 8.
3. Output Capacitor Selection (COUT)
A. In the majority of applications, low ESR electrolytic or solid tantalum capacitors between $82 \mu \mathrm{~F}$ and $820 \mu \mathrm{~F}$ provide the best results. This capacitor should be located close to the IC using short capacitor leads and short copper traces. Do not use capacitors larger than $820 \mu \mathrm{~F}$. For additional information, see section on output capacitors in application information section.
B. To simplify the capacitor selection procedure, refer to the quick design table shown in Figure 3. This table contains different output voltages, and lists various output capacitors that will provide the best design solutions.
C. The capacitor voltage rating should be at least 1.5 times greater than the output voltage, and often much higher voltage ratings are needed to satisfy the low ESR requirements needed for low output ripple voltage.

Procedure continued on next page.

EXAMPLE (Adjustable Output Voltage Version)
Given:
$V_{\text {OUT }}=20 \mathrm{~V}$
$\mathrm{V}_{\mathrm{IN}}(\max )=28 \mathrm{~V}$
$\operatorname{loAD}(\max )=3 \mathrm{~A}$
$\mathrm{F}=$ Switching Frequency (Fixed at a nominal 150 kHz ).

1. Programming Output Voltage (Selecting $R_{1}$ and $R_{2}$, as shown in Figure 1)
Select $R_{1}$ to be $1 k \Omega, 1 \%$. Solve for $R_{2}$.

$$
\mathrm{R}_{2}=\mathrm{R}_{1}\left(\frac{\mathrm{~V}_{\mathrm{OUT}}}{\mathrm{~V}_{\mathrm{REF}}}-1\right)=1 \mathrm{k}\left(\frac{20 \mathrm{~V}}{1.23 \mathrm{~V}}-1\right)
$$

$R_{2}=1 \mathrm{k}(16.26-1)=15.26 \mathrm{k}$, closest $1 \%$ value is
$15.4 \mathrm{k} \Omega$.
$R_{2}=15.4 \mathrm{k} \Omega$.
2. Inductor Selection (L1)
A. Calculate the inductor Volt - microsecond constant
( $\mathrm{E} \bullet \mathrm{T}$ ),

$$
\begin{gathered}
E \bullet T=(28-20-1.16) \bullet \frac{20+0.5}{28-1.16+0.5} \bullet \frac{1000}{150}(\mathrm{~V} \bullet \mu \mathrm{~s}) \\
E \bullet T=(6.84) \bullet \frac{20.5}{27.34} \bullet 6.67(\mathrm{~V} \bullet \mu \mathrm{~s})=34.2(\mathrm{~V} \bullet \mu \mathrm{~s})
\end{gathered}
$$

B. $\mathrm{E} \cdot \mathrm{T}=34.2(\mathrm{~V} \bullet \mu \mathrm{~s})$
C. $I_{\text {LOAD }}(\max )=3 \mathrm{~A}$
D. From the inductor value selection guide shown in Figure 7 , the inductance region intersected by the 34 (V • $\mu \mathrm{s}$ ) horizontal line and the 3 A vertical line is $47 \mu \mathrm{H}$, and the inductor code is L39.
E. From the table in Figure 8, locate line L39, and select an inductor part number from the list of manufacturers part numbers.
3. Output Capacitor Selection (Cout)
A. See section on COUT in Application Information section.
B. From the quick design table shown in Figure 3, locate the output voltage column. From that column, locate the output voltage closest to the output voltage in your application. In this example, select the 24 V line. Under the output capacitor section, select a capacitor from the list of through hole electrolytic or surface mount tantalum types from four different capacitor manufacturers. It is recommended that both the manufacturers and the manufacturers series that are listed in the table be used.
In this example, through hole aluminum electrolytic capacitors from several different manufacturers are available.

220/35 Panasonic HFQ Series
150/35 Nichicon PL Series
Example continued on next page.


| LM2599 Series Buck Regulator Design Procedure (Adjustable Output) <br> (Continued) |  |  |  |  |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  | Through Hole Output Capacitor |  |  | Surface Mount Output Capacitor |  |  |
| Voltage <br> (V) | Panasonic HFQ Series ( $\mu \mathrm{F} / \mathrm{V}$ ) | $\begin{gathered} \text { Nichicon PL } \\ \text { Series } \\ (\mu \mathrm{F} / \mathrm{V}) \\ \hline \end{gathered}$ | Feedforward Capacitor | AVX TPS <br> Series ( $\mu \mathrm{F} / \mathrm{V}$ ) | Sprague 595D Series ( $\mu \mathrm{F} / \mathrm{V}$ ) | Feedforward Capacitor |
| 2 | 820/35 | 820/35 | 33 nF | 330/6.3 | 470/4 | 33 nF |
| 4 | 560/35 | 470/35 | 10 nF | 330/6.3 | 390/6.3 | 10 nF |
| 6 | 470/25 | 470/25 | 3.3 nF | 220/10 | 330/10 | 3.3 nF |
| 9 | 330/25 | 330/25 | 1.5 nF | 100/16 | 180/16 | 1.5 nF |
| 12 | 330/25 | 330/25 | 1 nF | 100/16 | 180/16 | 1 nF |
| 15 | 220/35 | 220/35 | 680 pF | 68/20 | 120/20 | 680 pF |
| 24 | 220/35 | 150/35 | 560 pF | 33/25 | 33/25 | 220 pF |
| 28 | 100/50 | 100/50 | 390 pF | 10/35 | 15/50 | 220 pF |

FIGURE 3. Output Capacitor and Feedforward Capacitor Selection Table

## LM2599 Series Buck Regulator Design Procedure

INDUCTOR VALUE SELECTION GUIDES (For Continuous Mode Operation)

maximum load current (a)
FIGURE 4. LM2599-3.3


FIGURE 6. LM2599-12


TL/H/12582-27
FIGURE 5. LM2599-5.0



## LM2599 Series Buck Regulator Design Procedure (Continued)

| VR | 3 Amp Diodes |  |  |  | 4 to 6 Amp Diodes |  |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  | Surface Mount |  | Through Hole |  | Surface Mount |  | Through Hole |  |
|  | Schottky | Ultra Fast <br> Recovery | Schottky | Ultra Fast <br> Recovery | Schottky | Ultra Fast Recovery | Schottky | Ultra Fast Recovery |
| 20V |  | All of these diodes are rated to at least 50 V . <br> MURS320 30WF10 | 1N5820 | All of these diodes are rated to at least 50 V . <br> MUR320 |  | All of these diodes are rated to at least 50 V . <br> MURS620 50WF10 | SR502 | All of these diodes are rated to at least 50 V . <br> MUR620 <br> HER601 |
|  | SK32 |  | SR302 |  |  |  | 1N5823 |  |
|  |  |  | MBR320 |  |  |  | SB520 |  |
| 30 V | 30WQ03 |  | 1N5821 |  |  |  |  |  |
|  | SK33 |  | MBR330 |  | 50WQ03 |  | SR503 |  |
|  |  |  | 31DQ03 |  |  |  | 1N5824 |  |
| 40V |  |  | 1N5822 |  |  |  | SB530 |  |
|  | SK34 |  | SR304 |  | 50WQ04 |  | SR504 |  |
|  | MBRS340 |  | MBR340 |  |  |  | 1N5825 |  |
|  | 30WQ04 |  | 31DQ04 |  |  |  | SB540 |  |
| $\begin{aligned} & 50 \mathrm{~V} \\ & \text { or } \\ & \text { more } \end{aligned}$ | SK35 |  | SR305 |  |  |  |  |  |
|  | MBRS360 |  | MBR350 |  | 50WQ05 |  | SB550 |  |
|  | 30WQ05 |  | 31DQ05 |  |  |  | 50SQ080 |  |

FIGURE 11. Diode Selection Table

## Block Diagram



FIGURE 12

## Application Information

## PIN FUNCTIONS

$+\mathbf{V}_{\mathbf{I N}}$ (Pin 1)—This is the positive input supply for the IC switching regulator. A suitable input bypass capacitor must be present at this pin to minimize voltage transients and to supply the switching currents needed by the regulator.
Ground (Pin 4)-Circuit ground.
Output (Pin 2)—Internal switch. The voltage at this pin switches between approximately ( $+\mathrm{V}_{\text {IN }}-\mathrm{V}_{\text {SAT }}$ ) and approximately -0.5 V , with a duty cycle of $\mathrm{V}_{\mathrm{OUT}} / \mathrm{V}_{\text {IN }}$. To minimize coupling to sensitive circuitry, the PC board copper area connected to this pin should be kept to a minimum.
Feedback (Pin 6)—Senses the regulated output voltage to complete the feedback loop.
$\overline{\text { Shutdown/Soft-start (Pin 7)—This dual function pin pro- }}$ vides the following features: (a) Allows the switching regulator circuit to be shut down using logic level signals thus dropping the total input supply current to approximately $80 \mu \mathrm{~A}$. (b) Adding a capacitor to this pin provides a soft-start feature which minimizes startup current and provides a controlled ramp up of the output voltage.
Error Flag (Pin 3)—Open collector output that provides a low signal (flag transistor ON) when the regulated output voltage drops more than $5 \%$ from the nominal output voltage. On start up, Error Flag is low until $\mathrm{V}_{\text {OUT }}$ reaches $95 \%$ of the nominal output voltage and a delay time determined by the Delay pin capacitor. This signal can be used as a reset to a microprocessor on power-up.
Delay (Pin 5)—At power-up, this pin can be used to provide a time delay between the time the regulated output voltage reaches $95 \%$ of the nominal output voltage, and the time the error flag output goes high.
Special Note If any of the above three features ( (Shutdown/ Soft-start, Error Flag, or Delay) are not used, the respective pins should be left open.

## EXTERNAL COMPONENTS

## SOFT-START CAPACITOR

$\mathbf{C}_{\text {SS-A }}$ capacitor on this pin provides the regulator with a Soft-start feature (slow start-up). When the DC input voltage is first applied to the regulator, or when the Shutdown/Softstart pin is allowed to go high, a constant current (approximately $5 \mu \mathrm{~A}$ begins charging this capacitor). As the capacitor voltage rises, the regulator goes through four operating regions (See the bottom curve in Figure 13).

1. Regulator in Shutdown. When the $\overline{\mathrm{SD}} / \mathrm{SS}$ pin voltage is between 0 V and 1.3 V , the regulator is in shutdown, the output voltage is zero, and the IC quiescent current is approximately $85 \mu \mathrm{~A}$.
2. Regulator ON, but the output voltage is zero. With the $\overline{\mathrm{SD}} / \mathrm{SS}$ pin voltage between approximately 1.3 V and 1.8 V , the internal regulator circuitry is operating, the quiescent current rises to approximately 5 mA , but the output voltage is still zero. Also, as the 1.3 V threshold is exceeded, the Soft-start capacitor charging current decreases from $5 \mu \mathrm{~A}$ down to approximately $1.6 \mu \mathrm{~A}$. This decreases the slope of capacitor voltage ramp.
3. Soft-start Region. When the $\overline{\text { SD }} / \mathrm{SS}$ pin voltage is between 1.8 V and 2.8 V (@ $25^{\circ} \mathrm{C}$ ), the regulator is in a Softstart condition. The switch (Pin 2) duty cycle initially starts out very low, with narrow pulses and gradually get wider as the capacitor $\overline{\mathrm{SD}} / \mathrm{SS}$ pin ramps up towards 2.8 V . As the duty cycle increases, the output voltage also increases at a controlled ramp up. See the center curve in Figure 13. The input supply current requirement also starts out at a low level for the narrow pulses and ramp up in a controlled manner. This is a very useful feature in some switcher topologies that require large startup currents (such as the inverting configuration) which can load down the input power supply.
Note: The lower curve shown in Figure 13 shows the Soft-start region from $0 \%$ to $100 \%$. This is not the duty cycle percentage, but the output voltage percentage. Also, the Soft-start voltage range has a negative temperature coefficient associated with it. See the Soft-start curve in the electrical characteristics section.
4. Normal operation. Above 2.8 V , the circuit operates as a standard Pulse Width Modulated switching regulator. The capacitor will continue to charge up until it reaches the internal clamp voltage of approximately 7 V . If this pin is driven from a voltage source, the current must be limited to about 1 mA .

time dependent upon delay capacitor value


TIME DEPENDENT UPON SOFT-START CAPACITOR VALUE
TL/H/12582-31
FIGURE 13. Soft-start, Delay, Error, Output

## Application Information (Continued)



TL/H/12582-32
FIGURE 14. Timing Diagram for 5V Output

## DELAY CAPACITOR

CDELAY-Provides delay for the error flag output. See the upper curve in Figure 13, and also refer to timing diagrams in Figure 14. A capacitor on this pin provides a time delay between the time the regulated output voltage (when it is increasing in value) reaches $95 \%$ of the nominal output voltage, and the time the error flag output goes high. A $3 \mu \mathrm{~A}$ constant current from the delay pin charges the delay capacitor resulting in a voltage ramp. When this voltage reaches a threshold of approximately 1.3 V , the open collector error flag output (or power OK) goes high. This signal can be used to indicate that the regulated output has reached the correct voltage and has stabilized.
If, for any reason, the regulated output voltage drops by $5 \%$ or more, the error output flag (Pin 3) immediately goes low (internal transistor turns on). The delay capacitor provides very little delay if the regulated output is dropping out of regulation. The delay time for an output that is decreasing is approximately a 1000 times less than the delay for the rising output. For a $0.1 \mu \mathrm{~F}$ delay capacitor, the delay time would be approximately 50 ms when the output is rising and passes through the $95 \%$ threshold, but the delay for the output dropping would only be approximately $50 \mu \mathrm{~s}$.
$\mathbf{R}_{\text {Pull Up-The }}$-The error flag output, (or power OK) is the collector of a NPN transistor, with the emitter internally grounded. To use the error flag, a pullup resistor to a positive voltage is needed. The error flag transistor is rated up to a maximum of 45 V and can sink approximately 3 mA . If the error flag is not used, it can be left open.

## FEEDFORWARD CAPACITOR

(Adjustable Output Voltage Version)
$C_{\text {FF }}$ - A Feedforward Capacitor $\mathrm{C}_{\mathrm{FF}}$, shown across R2 in Figure 1 is used when the output voltage is greater than 10 V or when COUT has a very low ESR. This capacitor adds lead compensation to the feedback loop and increases the phase margin for better loop stability. For $\mathrm{C}_{\text {FF }}$ selection, see the design procedure section.

If the output ripple is large ( $>5 \%$ of the nominal output voltage), this ripple can be coupled to the feedback pin through the feedforward capacitor and cause the error comparator to trigger the error flag. In this situation, adding a resistor, $\mathrm{R}_{\mathrm{FF}}$, in series with the feedforward capacitor, approximately 3 times R1, will attenuate the ripple voltage at the feedback pin.

## INPUT CAPACITOR

$\mathbf{C}_{\text {IN }}$-A low ESR aluminum or tantalum bypass capacitor is needed between the input pin and ground pin. It must be located near the regulator using short leads. This capacitor prevents large voltage transients from appearing at the input, and provides the instantaneous current needed each time the switch turns on.
The important parameters for the Input capacitor are the voltage rating and the RMS current rating. Because of the relatively high RMS currents flowing in a buck regulator's input capacitor, this capacitor should be chosen for its RMS current rating rather than its capacitance or voltage ratings, although the capacitance value and voltage rating are directly related to the RMS current rating.
The RMS current rating of a capacitor could be viewed as a capacitor's power rating. The RMS current flowing through the capacitors internal ESR produces power which causes the internal temperature of the capacitor to rise. The RMS current rating of a capacitor is determined by the amount of current required to raise the internal temperature approximately $10^{\circ} \mathrm{C}$ above an ambient temperature of $105^{\circ} \mathrm{C}$. The ability of the capacitor to dissipate this heat to the surrounding air will determine the amount of current the capacitor can safely sustain. Capacitors that are physically large and have a large surface area will typically have higher RMS current ratings. For a given capacitor value, a higher voltage electrolytic capacitor will be physically larger than a lower voltage capacitor, and thus be able to dissipate more heat to the surrounding air, and therefore will have a higher RMS current rating.

## Application Information (Continued)



FIGURE 15. RMS Current Ratings for Low ESR Electrolytic Capacitors (Typical)

The consequences of operating an electrolytic capacitor above the RMS current rating is a shortened operating life. The higher temperature speeds up the evaporation of the capacitor's electrolyte, resulting in eventual failure.
Selecting an input capacitor requires consulting the manufacturers data sheet for maximum allowable RMS ripple current. For a maximum ambient temperature of $40^{\circ} \mathrm{C}$, a general guideline would be to select a capacitor with a ripple current rating of approximately $50 \%$ of the DC load current. For ambient temperatures up to $70^{\circ} \mathrm{C}$, a current rating of $75 \%$ of the DC load current would be a good choice for a conservative design. The capacitor voltage rating must be at least 1.25 times greater than the maximum input voltage, and often a much higher voltage capacitor is needed to satisfy the RMS current requirements.
A graph shown in Figure 15 shows the relationship between an electrolytic capacitor value, its voltage rating, and the RMS current it is rated for. These curves were obtained from the Nichicon "PL" series of Iow ESR, high reliability electrolytic capacitors designed for switching regulator applications. Other capacitor manufacturers offer similar types of capacitors, but always check the capacitor data sheet.
"Standard" electrolytic capacitors typically have much higher ESR numbers, lower RMS current ratings and typically have a shorter operating lifetime.
Because of their small size and excellent performance, surface mount solid tantalum capacitors are often used for input bypassing, but several precautions must be observed. A small percentage of solid tantalum capacitors can short if the inrush current rating is exceeded. This can happen at turn on when the input voltage is suddenly applied, and of course, higher input voltages produce higher inrush currents. Several capacitor manufacturers do a 100\% surge current testing on their products to minimize this potential


FIGURE 16. Capacitor ESR vs Capacitor Voltage Rating (Typical Low ESR Electrolytic Capacitor)
problem. If high turn on currents are expected, it may be necessary to limit this current by adding either some resistance or inductance before the tantalum capacitor, or select a higher voltage capacitor. As with aluminum electrolytic capacitors, the RMS ripple current rating must be sized to the load current.

## OUTPUT CAPACITOR

Cout-An output capacitor is required to filter the output and provide regulator loop stability. Low impedance or low ESR Electrolytic or solid tantalum capacitors designed for switching regulator applications must be used. When selecting an output capacitor, the important capacitor parameters are; the 100 kHz Equivalent Series Resistance (ESR), the RMS ripple current rating, voltage rating, and capacitance value. For the output capacitor, the ESR value is the most important parameter.
The output capacitor requires an ESR value that has an upper and lower limit. For low output ripple voltage, a low ESR value is needed. This value is determined by the maximum allowable output ripple voltage, typically $1 \%$ to $2 \%$ of the output voltage. But if the selected capacitor's ESR is extremely low, there is a possibility of an unstable feedback loop, resulting in an oscillation at the output. Using the capacitors listed in the tables, or similar types, will provide design solutions under all conditions.
If very low output ripple voltage (less than 15 mV ) is required, refer to the section on Output Voltage Ripple and Transients for a post ripple filter.
An aluminum electrolytic capacitor's ESR value is related to the capacitance value and its voltage rating. In most cases, higher voltage electrolytic capacitors have lower ESR values (see Figure 16). Often, capacitors with much higher voltage ratings may be needed to provide the low ESR values required for low output ripple voltage.

## Application Information (Continued)

The output capacitor for many different switcher designs often can be satisfied with only three or four different capacitor values and several different voltage ratings. See the quick design component selection tables in Figures 2 and 3 for typical capacitor values, voltage ratings, and manufacturers capacitor types.
Electrolytic capacitors are not recommended for temperatures below $-25^{\circ} \mathrm{C}$. The ESR rises dramatically at cold temperatures and typically rises 3 X @ $-25^{\circ} \mathrm{C}$ and as much as 10 X at $-40^{\circ} \mathrm{C}$. See curve shown in Figure 17.
Solid tantalum capacitors have a much better ESR spec for cold temperatures and are recommended for temperatures below $-25^{\circ} \mathrm{C}$.

## CATCH DIODE

Buck regulators require a diode to provide a return path for the inductor current when the switch turns off. This must be a fast diode and must be located close to the LM2599 using short leads and short printed circuit traces.
Because of their very fast switching speed and low forward voltage drop, Schottky diodes provide the best performance, especially in low output voltage applications ( 5 V and lower). Ultra-fast recovery, or High-Efficiency rectifiers are also a good choice, but some types with an abrupt turnoff characteristic may cause instability or EMI problems. Ultrafast recovery diodes typically have reverse recovery times of 50 ns or less. Rectifiers such as the IN5400 series are much too slow and should not be used.


TL/H/12582-35

## FIGURE 17. Capacitor ESR Change vs Temperature

## INDUCTOR SELECTION

All switching regulators have two basic modes of operation; continuous and discontinuous. The difference between the two types relates to the inductor current, whether it is flowing continuously, or if it drops to zero for a period of time in the normal switching cycle. Each mode has distinctively different operating characteristics, which can affect the regulators performance and requirements. Most switcher designs will operate in the discontinuous mode when the load current is low.
The LM2599 (or any of the Simple Switcher family) can be used for both continuous or discontinuous modes of operation.
In many cases the preferred mode of operation is the continuous mode. It offers greater output power, lower peak switch, inductor and diode currents, and can have lower out-
put ripple voltage. But it does require larger inductor values to keep the inductor current flowing continuously, especially at low output load currents and/or high input voltages.
To simplify the inductor selection process, an inductor selection guide (nomograph) was designed (see Figures 4 through 7). This guide assumes that the regulator is operating in the continuous mode, and selects an inductor that will allow a peak-to-peak inductor ripple current to be a certain percentage of the maximum design load current. This peak-to-peak inductor ripple current percentage is not fixed, but is allowed to change as different design load currents are selected. (See Figure 18.)


TL/H/12582-36
FIGURE 18. ( $\Delta_{I_{\text {IND }}}$ ) Peak-to-Peak Inductor Ripple Current (as a Percentage of the Load Current) vs Load Current

By allowing the percentage of inductor ripple current to increase for low load currents, the inductor value and size can be kept relatively low.
When operating in the continuous mode, the inductor current waveform ranges from a triangular to a sawtooth type of waveform (depending on the input voltage), with the average value of this current waveform equal to the DC output load current.
Inductors are available in different styles such as pot core, toroid, E-core, bobbin core, etc., as well as different core materials, such as ferrites and powdered iron. The least expensive, the bobbin, rod or stick core, consists of wire wound on a ferrite bobbin. This type of construction makes for an inexpensive inductor, but since the magnetic flux is not completely contained within the core, it generates more Electro-Magnetic Interference (EMI). This magnetic flux can induce voltages into nearby printed circuit traces, thus causing problems with both the switching regulator operation and nearby sensitive circuitry, and can give incorrect scope readings because of induced voltages in the scope probe. Also see section on Open Core Inductors.
When multiple switching regulators are located on the same PC board, open core magnetics can cause interference between two or more of the regulator circuits, especially at high currents. A torroid or E-core inductor (closed magnetic structure) should be used in these situations.
The inductors listed in the selection chart include ferrite E-core construction for Schott, ferrite bobbin core for Renco and Coilcraft, and powdered iron toroid for Pulse Engineering.

## Application Information (Continued)

Exceeding an inductor's maximum current rating may cause the inductor to overheat because of the copper wire losses, or the core may saturate. If the inductor begins to saturate, the inductance decreases rapidly and the inductor begins to look mainly resistive (the DC resistance of the winding). This can cause the switch current to rise very rapidly and force the switch into a cycle-by-cycle current limit, thus reducing the DC output load current. This can also result in overheating of the inductor and/or the LM2599. Different inductor types have different saturation characteristics, and this should be kept in mind when selecting an inductor.
The inductor manufacturer's data sheets include current and energy limits to avoid inductor saturation.

## DISCONTINUOUS MODE OPERATION

The selection guide chooses inductor values suitable for continuous mode operation, but for low current applications and/or high input voltages, a discontinuous mode design may be a better choice. It would use an inductor that would be physically smaller, and would need only one half to one third the inductance value needed for a continuous mode design. The peak switch and inductor currents will be higher in a discontinuous design, but at these low load currents (1A and below), the maximum switch current will still be less than the switch current limit.
Discontinuous operation can have voltage waveforms that are considerable different than a continuous design. The output pin (switch) waveform can have some damped sinusoidal ringing present. (See photo titled; Discontinuous Mode Switching Waveforms) This ringing is normal for discontinuous operation, and is not caused by feedback loop instabilities. In discontinuous operation, there is a period of time where neither the switch or the diode are conducting, and the inductor current has dropped to zero. During this time, a small amount of energy can circulate between the inductor and the switch/diode parasitic capacitance causing this characteristic ringing. Normally this ringing is not a problem, unless the amplitude becomes great enough to exceed the input voltage, and even then, there is very little energy present to cause damage.
Different inductor types and/or core materials produce different amounts of this characteristic ringing. Ferrite core inductors have very little core loss and therefore produce the most ringing. The higher core loss of powdered iron inductors produce less ringing. If desired, a series RC could be placed in parallel with the inductor to dampen the ringing. The computer aided design software Switchers Made Simple (version 4.3) will provide all component values for continuous and discontinuous modes of operation.


TL/H/12582-37
FIGURE 19. Post Ripple Filter Waveform

## OUTPUT VOLTAGE RIPPLE AND TRANSIENTS

The output voltage of a switching power supply operating in the continuous mode will contain a sawtooth ripple voltage at the switcher frequency, and may also contain short voltage spikes at the peaks of the sawtooth waveform.
The output ripple voltage is a function of the inductor sawtooth ripple current and the ESR of the output capacitor. A typical output ripple voltage can range from approximately $0.5 \%$ to $3 \%$ of the output voltage. To obtain low ripple voltage, the ESR of the output capacitor must be low, however, caution must be exercised when using extremely low ESR capacitors because they can affect the loop stability, resulting in oscillation problems. If very low output ripple voltage is needed (less than 20 mV ), a post ripple filter is recommended. (See Figure 1.) The inductance required is typically between $1 \mu \mathrm{H}$ and $5 \mu \mathrm{H}$, with low DC resistance, to maintain good load regulation. A low ESR output filter capacitor is also required to assure good dynamic load response and ripple reduction. The ESR of this capacitor may be as low as desired, because it is out of the regulator feedback loop. The photo shown in Figure 19 shows a typical output ripple voltage, with and without a post ripple filter.
When observing output ripple with a scope, it is essential that a short, low inductance scope probe ground connection be used. Most scope probe manufacturers provide a special probe terminator which is soldered onto the regulator board, preferable at the output capacitor. This provides a very short scope ground thus eliminating the problems associated with the 3 inch ground lead normally provided with the probe, and provides a much cleaner and more accurate picture of the ripple voltage waveform.
The voltage spikes are caused by the fast switching action of the output switch, the diode, and the parasitic inductance of the output filter capacitor, and its associated wiring. To minimize these voltage spikes, the output capacitor should be designed for switching regulator applications, and the lead lengths must be kept very short. Wiring inductance, stray capacitance, as well as the scope probe used to evaluate these transients, all contribute to the amplitude of these spikes.


FIGURE 20. Peak-to-Peak Inductor Ripple Current vs Load Current

## Application Information (Continued)

When a switching regulator is operating in the continuous mode, the inductor current waveform ranges from a triangular to a sawtooth type of waveform (depending on the input voltage). For a given input and output voltage, the peak-topeak amplitude of this inductor current waveform remains constant. As the load current increases or decreases, the entire sawtooth current waveform also rises and falls. The average value (or the center) of this current waveform is equal to the DC load current.
If the load current drops to a low enough level, the bottom of the sawtooth current waveform will reach zero, and the switcher will smoothly change from a continuous to a discontinuous mode of operation. Most switcher designs (irregardless how large the inductor value is) will be forced to run discontinuous if the output is lightly loaded. This is a perfectly acceptable mode of operation.
In a switching regulator design, knowing the value of the peak-to-peak inductor ripple current ( $\Delta \mathrm{I}_{\mathrm{IND}}$ ) can be useful for determining a number of other circuit parameters. Parameters such as, peak inductor or peak switch current, minimum load current before the circuit becomes discontinuous, output ripple voltage and output capacitor ESR can all be calculated from the peak-to-peak $\Delta I_{\text {IND }}$. When the inductor nomographs shown in Figures 4 through 7 are used to select an inductor value, the peak-to-peak inductor ripple current can immediately be determined. The curve shown in Figure 20 shows the range of ( $\Delta \|_{\text {IND }}$ ) that can be expected for different load currents. The curve also shows how the peak-to-peak inductor ripple current ( $\Delta l_{\text {IND }}$ ) changes as you go from the lower border to the upper border (for a given load current) within an inductance region. The upper border represents a higher input voltage, while the lower border represents a lower input voltage (see Inductor Selection Guides).
These curves are only correct for continuous mode operation, and only if the inductor selection guides are used to select the inductor value
Consider the following example:
$V_{\mathrm{OUT}}=5 \mathrm{~V}$, maximum load current of 2.5 A
$\mathrm{~V}_{\mathrm{IN}}=12 \mathrm{~V}$, nominal, varying between 10 V and 16 V .

The selection guide in Figure 5 shows that the vertical line for a 2.5A load current, and the horizontal line for the 12 V input voltage intersect approximately midway between the upper and lower borders of the $33 \mu \mathrm{H}$ inductance region. A $33 \mu \mathrm{H}$ inductor will allow a peak-to-peak inductor current ( $\Delta l_{\text {IND }}$ ) to flow that will be a percentage of the maximum load current. Referring to Figure 20, follow the 2.5A line approximately midway into the inductance region, and read the peak-to-peak inductor ripple current ( $\Delta l_{\text {IND }}$ ) on the left hand axis (approximately $620 \mathrm{~mA} p-\mathrm{p}$ ).
As the input voltage increases to 16 V , it approaches the upper border of the inductance region, and the inductor ripple current increases. Referring to the curve in Figure 20, it can be seen that for a load current of 2.5 A , the peak-topeak inductor ripple current ( $\Delta I_{\mathrm{IND}}$ ) is 620 mA with 12 V in, and can range from 740 mA at the upper border ( $16 \mathrm{~V} \mathrm{in)}$ to 500 mA at the lower border (10V in).

Once the $\Delta l_{\text {IND }}$ value is known, the following formulas can be used to calculate additional information about the switching regulator circuit.

1. Peak Inductor or peak switch current

$$
=\left(I_{\mathrm{LOAD}}+\frac{\Delta l_{\mathrm{IND}}}{2}\right)=\left(2.5 \mathrm{~A}+\frac{0.62}{2}\right)=2.81 \mathrm{~A}
$$

2. Minimum load current before the circuit becomes discontinuous
$=\frac{\Delta l_{\mathrm{IND}}}{2}=\frac{0.62}{2}=0.31 \mathrm{~A}$
3. Output Ripple Voltage $=\left(\Delta I_{\text {IND }}\right) \times\left(E S R\right.$ of $\left.C_{\text {OUT }}\right)$

$$
=0.62 \mathrm{~A} \times 0.1 \Omega=62 \mathrm{mV} \text { p-p }
$$

4. ESR of $\mathrm{C}_{\text {OUT }}=\frac{\text { Output Ripple Voltage }\left(\Delta \mathrm{V}_{\text {OUT }}\right)}{\Delta \mathrm{I}_{\mathrm{IND}}}$

$$
=\frac{0.062 \mathrm{~V}}{0.62 \mathrm{~A}}=0.1 \Omega
$$

## OPEN CORE INDUCTORS

Another possible source of increased output ripple voltage or unstable operation is from an open core inductor. Ferrite bobbin or stick inductors have magnetic lines of flux flowing through the air from one end of the bobbin to the other end. These magnetic lines of flux will induce a voltage into any wire or PC board copper trace that comes within the inductor's magnetic field. The strength of the magnetic field, the orientation and location of the PC copper trace to the magnetic field, and the distance between the copper trace and the inductor, determine the amount of voltage generated in the copper trace. Another way of looking at this inductive coupling is to consider the PC board copper trace as one turn of a transformer (secondary) with the inductor winding as the primary. Many millivolts can be generated in a copper trace located near an open core inductor which can cause stability problems or high output ripple voltage problems.
If unstable operation is seen, and an open core inductor is used, it's possible that the location of the inductor with respect to other PC traces may be the problem. To determine if this is the problem, temporarily raise the inductor away from the board by several inches and then check circuit operation. If the circuit now operates correctly, then the magnetic flux from the open core inductor is causing the problem. Substituting a closed core inductor such as a torroid or E-core will correct the problem, or re-arranging the PC layout may be necessary. Magnetic flux cutting the IC device ground trace, feedback trace, or the positive or negative traces of the output capacitor should be minimized.
Sometimes, locating a trace directly beneath a bobbin inductor will provide good results, provided it is exactly in the center of the inductor (because the induced voltages cancel themselves out), but if it is off center one direction or the other, then problems could arise. If flux problems are present, even the direction of the inductor winding can make a difference in some circuits.
This discussion on open core inductors is not to frighten the user, but to alert the user on what kind of problems to watch out for when using them. Open core bobbin or "stick" inductors are an inexpensive, simple way of making a compact efficient inductor, and they are used by the millions in many different applications.

Application Information (Continued)


TL/H/12582-38

| Circuit Data for Temperature Rise Curve TO-220 Package (T) |  |
| :--- | :--- |
| Capacitors | Through hole electrolytic |
| Inductor | Through hole Renco |
| Diode | Through hole, 5A 40V, Schottky |
| PC board | 3 square inches single sided 2 oz. copper <br> $\left(0.0028^{\prime \prime}\right)$ |

FIGURE 21. Junction Temperature Rise, TO-220


TL/H/12582-39

| Circuit Data for Temperature Rise Curve TO-263 Package (S) |  |
| :--- | :--- |
| Capacitors | Surface mount tantalum, molded "D" size |
| Inductor | Surface mount, Pulse engineering, $68 \mu \mathrm{H}$ |
| Diode | Surface mount, 5A 40V, Schottky |
| PC board | 9 square inches single sided 2 oz. copper <br> $(0.0028 ")$ |

FIGURE 22. Junction Temperature Rise, TO-263

## thermal considerations

The LM2599 is available in two packages, a 7-pin TO-220 ( T ) and a 7-pin surface mount TO-263 (S).
The TO-220 package needs a heat sink under most conditions. The size of the heat sink depends on the input voltage,
the output voltage, the load current and the ambient temperature. The curves in Figure 21 show the LM2599T junction temperature rises above ambient temperature for a 3A load and different input and output voltages. The data for these curves was taken with the LM2599T (TO-220 package) operating as a buck switching regulator in an ambient temperature of $25^{\circ} \mathrm{C}$ (still air). These temperature rise numbers are all approximate and there are many factors that can affect these temperatures. Higher ambient temperatures require more heat sinking.
The TO-263 surface mount package tab is designed to be soldered to the copper on a printed circuit board. The copper and the board are the heat sink for this package and the other heat producing components, such as the catch diode and inductor. The pc board copper area that the package is soldered to should be at least $0.4 \mathrm{in}^{2}$, and ideally should have 2 or more square inches of 2 oz . ( 0.0028 in ) copper. Additional copper area improves the thermal characteristics, but with copper areas greater than approximately 6 in $^{2}$, only small improvements in heat dissipation are realized. If further thermal improvements are needed, double sided, multilayer pc-board with large copper areas and/or airflow are recommended.
The curves shown in Figure 22 show the LM2599S (TO-263 package) junction temperature rise above ambient temperature with a 2A load for various input and output voltages. This data was taken with the circuit operating as a buck switching regulator with all components mounted on a pc board to simulate the junction temperature under actual operating conditions. This curve can be used for a quick check for the approximate junction temperature for various conditions, but be aware that there are many factors that can affect the junction temperature. When load currents higher than 2A are used, double sided or multilayer pc-boards with large copper areas and/or airflow might be needed, especially for high ambient temperatures and high output voltages.
For the best thermal performance, wide copper traces and generous amounts of printed circuit board copper should be used in the board layout. (One exception to this is the output (switch) pin, which should not have large areas of copper.) Large areas of copper provide the best transfer of heat (lower thermal resistance) to the surrounding air, and moving air lowers the thermal resistance even further.
Package thermal resistance and junction temperature rise numbers are all approximate, and there are many factors that will affect these numbers. Some of these factors include board size, shape, thickness, position, location, and even board temperature. Other factors are, trace width, total printed circuit copper area, copper thickness, single- or dou-ble-sided, multilayer board and the amount of solder on the board. The effectiveness of the pc board to dissipate heat also depends on the size, quantity and spacing of other components on the board, as well as whether the surrounding air is still or moving. Furthermore, some of these components such as the catch diode will add heat to the pc board and the heat can vary as the input voltage changes. For the inductor, depending on the physical size, type of core material and the DC resistance, it could either act as a heat sink taking heat away from the board, or it could add heat to the board.

## Application Information (Continued)

## SHUTDOWN/SOFT-START

The circuit shown in Figure 23 is a standard buck regulator with 20 V in, 12 V out, 1 A load, and using a $0.068 \mu \mathrm{~F}$ Softstart capacitor. The photo in Figures 24 and 25 show the effects of Soft-start on the output voltage, the input current, with, and without a Soft-start capacitor. The reduced input current required at startup is very evident when comparing the two photos. The Soft-start feature reduces the startup current from 2.6A down to 650 mA , and delays and slows down the output voltage rise time.


TL/H/12582-40
FIGURE 24. Output Voltage, Input Current, at Start-Up, WITH Soft-start


FIGURE 25. Output Voltage, Input Current, at Start-Up, WITHOUT Soft-start
This reduction in start up current is useful in situations where the input power source is limited in the amount of current it can deliver. In some applications Soft-start can be used to replace undervoltage lockout or delayed startup functions.
If a very slow output voltage ramp is desired, the Soft-start capacitor can be made much larger. Many seconds or even minutes are possible.
If only the shutdown feature is needed, the Soft-start capacitor can be eliminated.


TL/H/12582-42
FIGURE 23. Typical Circuit Using Shutdown/Soft-start and Error Flag Features

## Application Information (Continued)



## FIGURE 26. Inverting - 5V Regulator With Shutdown and Soft-start

## INVERTING REGULATOR

The circuit in Figure 26 converts a positive input voltage to a negative output voltage with a common ground. The circuit operates by bootstrapping the regulator's ground pin to the negative output voltage, then grounding the feedback pin, the regulator senses the inverted output voltage and regulates it.
This example uses the LM2599-5 to generate a -5 V output, but other output voltages are possible by selecting other output voltage versions, including the adjustable version. Since this regulator topology can produce an output voltage that is either greater than or less than the input voltage, the maximum output current greatly depends on both the input and output voltage. The curve shown in Figure 27 provides a guide as to the amount of output load current possible for the different input and output voltage conditions.
The maximum voltage appearing across the regulator is the absolute sum of the input and output voltage, and this must be limited to a maximum of 40 V . In this example, when converting +20 V to -5 V , the regulator would see 25 V between the input pin and ground pin. The LM2599 has a maximum input voltage rating of 40 V .


TL/H/12582-44
FIGURE 27. Maximum Load Current for Inverting Regulator Circuit

An additional diode is required in this regulator configuration. Diode D1 is used to isolate input voltage ripple or noise from coupling through the $\mathrm{C}_{\mathrm{IN}}$ capacitor to the output, under light or no load conditions. Also, this diode isolation changes the topology to closely resemble a buck configuration thus providing good closed loop stability. A Schottky diode is recommended for low input voltages, (because of its lower voltage drop) but for higher input voltages, a IN5400 diode could be used.
Because of differences in the operation of the inverting regulator, the standard design procedure is not used to select the inductor value. In the majority of designs, a $33 \mu \mathrm{H}, 3.5 \mathrm{~A}$ inductor is the best choice. Capacitor selection can also be narrowed down to just a few values. Using the values shown in Figure 26 will provide good results in the majority of inverting designs.
This type of inverting regulator can require relatively large amounts of input current when starting up, even with light loads. Input currents as high as the LM2599 current limit (approximately 4.5 A ) are needed for 2 ms or more, until the output reaches its nominal output voltage. The actual time depends on the output voltage and the size of the output capacitor. Input power sources that are current limited or sources that can not deliver these currents without getting loaded down, may not work correctly. Because of the relatively high startup currents required by the inverting topology, the Soft-start feature shown in Figure 26 is recommended.
Also shown in Figure 26 are several shutdown methods for the inverting configuration. With the inverting configuration, some level shifting is required, because the ground pin of the regulator is no longer at ground, but is now at the negative output voltage. The shutdown methods shown accept ground referenced shutdown signals.

## Application Information (Continued)

## undervoltage lockout

Some applications require the regulator to remain off until the input voltage reaches a predetermined voltage. Figure 28 contains a undervoltage lockout circuit for a buck configuration, while Figures 29 and 30 are for the inverting types (only the circuitry pertaining to the undervoltage lockout is shown). Figure 28 uses a zener diode to establish the threshold voltage when the switcher begins operating. When the input voltage is less than the zener voltage, resistors R1 and R2 hold the Shutdown/Soft-start pin low, keeping the regulator in the shutdown mode. As the input voltage exceeds the zener voltage, the zener conducts, pulling the Shutdown/Soft-start pin high, allowing the regulator to begin switching. The threshold voltage for the undervoltage lockout feature is approximately 1.5 V greater than the zener voltage.


TL/H/12582-45
FIGURE 28. Undervoltage Lockout for a Buck Regulator
Figures 29 and 30 apply the same feature to an inverting circuit. Figure 29 features a constant threshold voltage for turn on and turn off (zener voltage plus approximately one volt). If hysteresis is needed, the circuit in Figure 30 has a turn ON voltage which is different than the turn OFF voltage. The amount of hysteresis is approximately equal to the value of the output voltage. Since the $\overline{\mathrm{SD}} / \mathrm{SS}$ pin has an internal 7V zener clamp, R2 is needed to limit the current into this pin to approximately 1 mA when Q1 is on.


TL/H/12582-47
FIGURE 29. Undervoltage Lockout Without Hysteresis for an Inverting Regulator


FIGURE 30. Undervoltage Lockout With Hysteresis for an Inverting Regulator

## NEGATIVE VOLTAGE CHARGE PUMP

Occasionally a low current negative voltage is needed for biasing parts of a circuit. A simple method of generating a negative voltage using a charge pump technique and the switching waveform present at the OUT pin, is shown in Figure 31. This unregulated negative voltage is approximately equal to the positive input voltage (minus a few volts), and can supply up to a 600 mA of output current. There is a requirement however, that there be a minimum load of 1.2 A on the regulated positive output for the charge pump to work correctly. Also, resistor R1 is required to limit the charging current of C1 to some value less than the LM2599 current limit (typically 4.5A).
This method of generating a negative output voltage without an additional inductor can be used with other members of the Simple Switcher Family, using either the buck or boost topology.


FIGURE 31. Charge Pump for Generating a Low Current, Negative Output Voltage

## Application Information (Continued)

TYPICAL THROUGH HOLE PC BOARD LAYOUT, FIXED OUTPUT (1X SIZE), DOUBLE SIDED

$\mathrm{C}_{\mathrm{IN}}-470 \mu \mathrm{~F}, 50 \mathrm{~V}$, Aluminum Electrolytic Panasonic, "HFQ Series" COUT - $330 \mu \mathrm{~F}, 35 \mathrm{~V}$, Aluminum Electrolytic Panasonic, "HFQ Series" D1 - 5A, 40V Schottky Rectifier, 1N5825
L1 $-47 \mu \mathrm{H}, \mathrm{L} 39$, Renco, Through Hole

Top Side (Component Side)


TL/H/12582-51
Rpull up - 10k
$\mathrm{C}_{\text {DeLAY }}-0.1 \mu \mathrm{~F}$
$\mathrm{C}_{\text {SD/SS }}-0.1 \mu \mathrm{~F}$
Thermalloy Heat Sink \#7020

Application Information (Continued)
TYPICAL THROUGH HOLE PC BOARD LAYOUT, ADJUSTABLE OUTPUT (1X SIZE), DOUBLE SIDED


TL/H/12582-52

```
CIN - 470 \mu\textrm{F},50\textrm{V}\mathrm{ , Aluminum Electrolytic Panasonic, "HFQ Series"}
COUT - 220 \muF,35V Aluminum Electrolytic Panasonic, "HFQ Series"
D1 - 5A, 40V Schottky Rectifier, 1N5825
L1 - 47 \muH, L39, Renco, Through Hole
R1 - 1 k\Omega,1%
R2 - Use formula in Design Procedure
CFF - See Figure 4.
R
```



## Physical Dimensions inches (millimeters) unless otherwise noted



Physical Dimensions inches (millimeters) unless otherwise noted (Continued)


7-Lead TO-263 Bent and Formed Package
Order Number LM2599S-3.3, LM2599S-5.0, LM2599S-12 or LM2599S-ADJ NS Package Number TS7B

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2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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| Onational semiconductor |  |
| :---: | :---: |
| LM2650 |  |
| Synchronous Step-Down DC/DC Converter |  |
| General Description | Features |
| The LM2650 is a step-down DC/DC converter featuring | - Ultra high efficiencries (95\% possible) |
| high efficiency over a 3 A to milimperes load range. This feature makes the LM2650 an ideal fit in bater--owered |  |
| applications that demand long battery lie in both run a | - Wide input voltage range ( 4.5 V to 18V) |
| The LM2650 also features a logic-controlled shutdown A |  |
|  |  |
|  |  |
|  |  |
| high efficiencies. In many applications, efficiencies reach to heavy loads from 0.2A to 2A |  |
|  |  |
| high at light loads. The LM2650 enters and exts sleep Applications |  |
|  |  |
|  |  |
|  |  |
| and keep the LM2650 in PWM mode regardless level. |  |
|  |  |
|  |  |

## Typical Application




FIGURE 1. Converting a Four-Cell Li Ion Battery to 5V

## Absolute Maximum Ratings (Note 1)

(All voltages referred to the PGND and GND)

| DC Voltage at PVIN and VIN | 20 V |
| :--- | ---: |
| DC Voltage at SD, SLEEP LOGIC and SYNC | 15 V |
| DC Current into SW | $\pm 7.5 \mathrm{~A}$ |
| Junction Temperature | Limited by the IC |
| DC Power Dissipation (Note 2) | 1.28 W |
| Storage Temperature | $-65^{\circ} \mathrm{C}$ to $+150^{\circ} \mathrm{C}$ |


| Soldering Time, Temperature (Note 3) |  |
| :---: | :---: |
| Wave | 4 seconds, $260^{\circ} \mathrm{C}$ |
| Infrared | 10 seconds, $240^{\circ} \mathrm{C}$ |
| Vapor Phase | 75 seconds, $219^{\circ} \mathrm{C}$ |
| ESD Susceptibility (Note 4) | 1.3 kV |
| Operating Ratings (Note 1) |  |
| Supply Voltage Range ( $\mathrm{P}_{\text {IN }}$ and $\mathrm{V}_{\text {IN }}$ ) | 4.5 V to 18 V |
| Junction Temperature Range | $-40^{\circ} \mathrm{C}$ to $+125^{\circ} \mathrm{C}$ |

## Electrical Characteristics

$\mathrm{V}_{P V_{I N}}=\mathrm{V}_{\mathrm{V}_{I N}}=15 \mathrm{~V}, \mathrm{~V}_{\text {SLEEP LOGIC }}=0 \mathrm{~V}$, and $\mathrm{V}_{S D}=0 \mathrm{~V}$ unless superseded under Conditions. Typicals and limits appearing in plain type apply for $\mathrm{T}_{\mathrm{A}}=\mathrm{T}_{J}=+25^{\circ} \mathrm{C}$. Limits appearing in boldface type apply over the full junction temperature range shown under Operating Ratings.

| Symbol | Parameter | Conditions | Typical (Note 5) | $\begin{aligned} & \text { Limit } \\ & \text { (Note 6) } \end{aligned}$ | Units (Limits) |
| :---: | :---: | :---: | :---: | :---: | :---: |
| $\mathrm{V}_{\text {OUT }}$ | Output Voltage | $\begin{aligned} & \mathrm{R} 1=75 \mathrm{k} \Omega, 1 \%, \mathrm{R} 2=25 \mathrm{k} \Omega, 1 \%, \\ & 7.5 \mathrm{~V} \leq \mathrm{V}_{\mathrm{P}, ~} \mathrm{IN} \leq 18 \mathrm{~V}, \\ & 0.12 \mathrm{~A} \leq \mathrm{I}_{\mathrm{LOAD}} \leq 3 \mathrm{~A} \end{aligned}$ | 5.00 | $\begin{aligned} & 4.80 / 4.75 \\ & 5.20 / 5.25 \end{aligned}$ |  |
| $\eta 1$ | System Efficiency | $\mathrm{I}_{\text {LOAD }}=1 \mathrm{~A}, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$, Fosc Not Adjusted | 94 |  | \% |
| $\eta 2$ | System Efficiency | $\mathrm{I}_{\text {LOAD }}=3 \mathrm{~A}, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$, Fosc Not Adjusted | 89 |  | \% |
| $V_{\text {REF }}$ | Reference Voltage | $\mathrm{V}_{\text {SLEEP LOGIC }}=3 \mathrm{~V}$ <br> (Note 7) | 1.25 | $\begin{aligned} & 1.281 / 1.294 \\ & 1.219 / 1.206 \end{aligned}$ | $\mathrm{V}(\min )$ <br> $V$ (max) |
| $\mathrm{I}_{\mathrm{Q}}$ | Quiescent Current in PWM Mode | $\begin{aligned} & V_{F B}=V_{R E F}-20 \mathrm{mV} \\ & (\text { Note 8) } \end{aligned}$ | 4.0 | 6.5/7.0 | $\begin{gathered} \mathrm{mA} \\ \mathrm{~mA}(\max ) \end{gathered}$ |
| $\mathrm{I}_{\text {Q }}$ | Quiescent Current in Sleep Mode | $\begin{aligned} & \mathrm{V}_{\mathrm{FB}}=\mathrm{V}_{\mathrm{REF}}-20 \mathrm{mV}, \\ & \mathrm{~V}_{\mathrm{SLEEP}} \text { LOGIC }=3 \mathrm{~V} \\ & \text { (Note 8) } \end{aligned}$ | 850 | 1.35/1.60 | $\begin{gathered} \mu \mathrm{A} \\ \mathrm{~mA}(\max ) \end{gathered}$ |
| $\mathrm{I}_{\text {QSD }}$ | Quiescent Current in Shutdown Mode | $V_{S D}=3 \mathrm{~V}$ <br> (Note 8) | 9 | 20/25 | $\begin{gathered} \mu \mathrm{A} \\ \mu \mathrm{~A}(\text { max }) \end{gathered}$ |
| $\begin{aligned} & \mathrm{R}_{\mathrm{DS}(o n)} \\ & \mathrm{HS} \end{aligned}$ | DC On-Resistance Drain-to-Source of the High-Side Power Switch | $\begin{aligned} & \mathrm{I}_{\mathrm{DS}}=1 \mathrm{~A}, \mathrm{~V}_{\mathrm{SLEEP} \text { LOGIC }}=3 \mathrm{~V}, \\ & \mathrm{~V}_{\mathrm{FB}}=3 \mathrm{~V}, \\ & \mathrm{~V}_{\mathrm{BOOT}}=24 \mathrm{~V} \end{aligned}$ | 130 | 170/245 | $\begin{gathered} \mathrm{m} \Omega \\ \mathrm{~m} \Omega(\max ) \end{gathered}$ |
| $\mathrm{R}_{\mathrm{DS}(o n)}$ LS | DC On-Resistance Drain-to-Source of the Low-Side Power Switch | $\begin{aligned} & \mathrm{I}_{\mathrm{DS}}=1 \mathrm{~A}, \\ & \mathrm{~V}_{\mathrm{FB}}=3 \mathrm{~V} \end{aligned}$ | 125 | 175/245 | $\begin{gathered} \mathrm{m} \Omega \\ \mathrm{~m} \Omega(\max ) \end{gathered}$ |
| ILHS | Leakage Current of the High-Side Power Switch | $\begin{aligned} & \mathrm{V}_{\mathrm{PV}_{I N}}=18 \mathrm{~V}, \mathrm{~V}_{\mathrm{SW}}=0 \mathrm{~V}, \\ & \mathrm{~V}_{S D}=3 \mathrm{~V} \end{aligned}$ | 100 | 10 | nA $\mu \mathrm{A}$ (max) |
| ILLS | Leakage Current of the Low-Side Power Switch | $\begin{aligned} & \mathrm{V}_{\mathrm{PV},}=18 \mathrm{~V}, \mathrm{~V}_{\mathrm{SW}}=18 \mathrm{~V}, \\ & \mathrm{~V}_{\mathrm{SD}}=3 \mathrm{~V} \end{aligned}$ | 95 | 210 | $\begin{gathered} \mu \mathrm{A} \\ \mu \mathrm{~A}(\mathrm{max}) \\ \hline \end{gathered}$ |
| ILIMIT | Active Current Limit of the High-Side Power Switch | $\begin{aligned} & \mathrm{V}_{\mathrm{PV} \text { IN }}=15 \mathrm{~V}, \\ & \mathrm{~V}_{\mathrm{BOOT}}=24 \mathrm{~V}, \\ & \mathrm{~V}_{\mathrm{FB}}=3 \mathrm{~V}, \\ & \mathrm{~V}_{\text {SLEEP LOGIC }}=3 \mathrm{~V} \end{aligned}$ | 5.5 | $\begin{aligned} & 3.5 \\ & 7.5 \end{aligned}$ | A <br> A(min) <br> A(max) |

## Electrical Characteristics (Continued)

$\mathrm{V}_{\mathrm{PV}}=\mathrm{V}_{\mathrm{V}_{I N}}=15 \mathrm{~V}, \mathrm{~V}_{\text {SLEEP LOGIC }}=0 \mathrm{~V}$, and $\mathrm{V}_{\mathrm{SD}}=0 \mathrm{~V}$ unless superseded under Conditions. Typicals and limits appearing in plain type apply for $T_{A}=T_{J}=+25^{\circ} \mathrm{C}$. Limits appearing in boldface type apply over the full junction temperature range shown under Operating Ratings.

| Symbol | Parameter | Conditions | Typical (Note 5) | Limit (Note 6) | Units (Limits) |
| :---: | :---: | :---: | :---: | :---: | :---: |
| Fosc | Oscillator Frequency | $\mathrm{V}_{\mathrm{FB}}=\mathrm{V}_{\mathrm{REF}}-20 \mathrm{mV}$ | 90 | $\begin{gathered} 80 / 75 \\ 100 / 105 \end{gathered}$ | $\begin{gathered} \mathrm{kHz} \\ \mathrm{kHz}(\min ) \\ \mathrm{kHz}(\max ) \\ \hline \end{gathered}$ |
| $\mathrm{F}_{\text {MAX }}$ | Maximum Oscillator Frequency | $I_{\text {FREQ ADJ }}=100 \mu \mathrm{~A}$ (Note 9), $\mathrm{V}_{\mathrm{FB}}=\mathrm{V}_{\mathrm{REF}}-20 \mathrm{mV}$ | 315 | $\begin{aligned} & 270 / \mathbf{2 6 0} \\ & 360 / \mathbf{3 7 0} \end{aligned}$ | $\begin{gathered} \mathrm{kHz} \\ \mathrm{kHz}(\min ) \\ \mathrm{kHz}(\max ) \\ \hline \end{gathered}$ |
| $\mathrm{D}_{\text {MAX }}$ | Maximum Duty Cycle | $\begin{aligned} & \mathrm{V}_{\mathrm{FB}}=\mathrm{V}_{\mathrm{REF}}-20 \mathrm{mV}, \\ & \mathrm{~F}_{\mathrm{OSC}} \text { Not Adjusted } \end{aligned}$ | 97 | 94/93 | $\begin{gathered} \% \\ \%(\min ) \end{gathered}$ |
| $\mathrm{D}_{\text {MIN }}$ | Minimum Duty Cycle | $V_{F B}=V_{R E F}+50 \mathrm{mV},$ <br> Fosc Not Adjusted | 2.8 | 5 | $\begin{gathered} \% \\ \%(\max ) \\ \hline \end{gathered}$ |
| $V_{D D}$ | Internal Rail Voltage | $\mathrm{I}_{\mathrm{VDD}}=1 \mathrm{~mA}$ | 4.0 | $\begin{aligned} & 3.6 / 3.4 \\ & 4.2 / 4.3 \end{aligned}$ | $\begin{gathered} \mathrm{V} \\ \mathrm{~V}(\min ) \\ \mathrm{V}(\max ) \end{gathered}$ |
| $\mathrm{V}_{\text {BOOT }}$ | Bootstrap Regulator Voltage (VRegH) | $\mathrm{I}_{\text {BOOT }}=1 \mathrm{~mA}$ | 7.5 | 6.5/6.0 | $\begin{gathered} \mathrm{V} \\ \mathrm{~V}(\min ) \end{gathered}$ |
| Iss | Soft Start Current |  | 10 | 13.5/20.0 | $\begin{gathered} \mu \mathrm{A} \\ \mu \mathrm{~A}(\mathrm{max}) \end{gathered}$ |
| $\mathrm{V}_{\text {HYST }}$ | Hysteresis of the Sleep Comparator (C2 in Figure 3) | $\mathrm{V}_{\text {SLEEP LOGIC }}=3 \mathrm{~V}$ | 30 | $\begin{aligned} & 10 \\ & 50 \end{aligned}$ | $\begin{gathered} \mathrm{mV} \\ \mathrm{mV}(\mathrm{~min}) \\ \mathrm{mV}(\mathrm{max}) \end{gathered}$ |
|  | $\mathrm{V}_{\text {IL }}$ of SD |  |  | 0.95 | V (max) |
|  | $\mathrm{V}_{\mathrm{IH}}$ of SD |  |  | 2.10 | $V(\min )$ |
|  | $\mathrm{V}_{\text {IL }}$ of SLEEP LOGIC |  |  | 0.9 | $V$ (max) |
|  | $\mathrm{V}_{\text {IH }}$ of SLEEP LOGIC |  |  | 2.0 | $V(\min )$ |
|  | $\mathrm{V}_{\text {IL }}$ of SYNC |  |  | 0.50 | $V$ (max) |
|  | $\mathrm{V}_{\mathrm{IH}}$ of SYNC |  |  | 1.45 | $V(\min )$ |
| TSD | $\mathrm{T}_{\mathrm{J}}$ for Thermal Shutdown |  | 170 |  | ${ }^{\circ} \mathrm{C}$ |

Note 1: Absolute Maximum Ratings are limits beyond which damage to the device may occur. Operating ratings are conditions under which the device operates correctly. Operating Ratings do not imply guaranteed performance limits. For guaranteed performance limits and associated test conditions, see the Electrical Characteristics

Note 2: This rating is calculated using the formula $P_{D C \max }=\left(T_{J \max }-T_{A}\right) / \theta_{J A}$, where $P_{D C \max }$ is the absolute maximum $D C$ power dissipation, $T_{J m a x}$ is the maximum junction temperature, $T_{A}$ is the ambient temperature, and $\theta_{\mathrm{JA}}$ is the junction-to-ambient thermal resistance of the package. The $\mathrm{P}_{\mathrm{DCmax}}$ rating of 1.28 W results from substituting $170^{\circ} \mathrm{C}, 70^{\circ} \mathrm{C}$, and $78^{\circ} \mathrm{C} / \mathrm{W}$ for $\mathrm{T}_{\mathrm{Jmax}}, \mathrm{T}_{\mathrm{A}}$, and $\theta_{\mathrm{JA}}$ respectively. A $\theta_{\mathrm{JA}}$ of $78^{\circ} \mathrm{C} / \mathrm{W}$ represents the worst-case condition of no heat sinking of the M24B small-outline package. Heat sinking allows the safe dissipation of more power. See Application Notes on thermal management. The LM2650 actively limits its junction temperature to about $170^{\circ} \mathrm{C}$.

Note 3: For detailed information on soldering plastic small-outline packages, refer to the Packaging Databook published by National Semiconductor Corporation.
Note 4: ESD is applied using the human-body model, a 100 pF capacitor discharged through a $1.5 \mathrm{k} \Omega$ resistor.
Note 5: A typical is the center of characterization data taken at $T_{A}=T_{J}=25^{\circ} \mathrm{C}$.
Note 6: All limits are guaranteed. The guarantee is backed with $100 \%$ testing at $T_{A}=T_{J}=125^{\circ} \mathrm{C}$ and statistical correlation for room temperature and cold limits . Note 7: $\mathrm{V}_{\text {REF }}$ is measured at SLEEP OUT ADJ.
Note 8: Quiescent current is the total current flowing into the $\mathrm{P}_{\mathrm{V}_{I N}}$ and $\mathrm{V}_{\mathbb{I N}}$ pins. $\mathrm{I}_{\mathrm{Q}}$ includes the current used to drive the gates of the two NMOS power FETs at the nominal switching frequency. IQS includes no such current.
Note 9: Pulling $100 \mu \mathrm{~A}$ out of FREQ ADJ simulates adjusting the oscillator frequency with a $12.5 \mathrm{k} \Omega$ resistor connected from FREQ ADJ to GND. The sleep mode cannot be used at switching frequencies above 250 kHz .

## Typical Performance Characteristics




Oscillator Frequency vs Adjusting Resistor

Current Limit vs Junction Temperature


TL/H/12848-13

## Connection Diagram



Pin Descriptions (Refer to the Block Diagrams)

| Pins | Description |
| :---: | :---: |
| 1,12 | SUB: These pins make electrical contact with the substrate of the die. Ground them. For best thermal performance, ground them to the same large, uninterrupted copper plane as the PGND pins. |
| 2 | SLEEP LOGIC: Use this logic input to select the conversion mode; low selects PWM, high selects sleep, and high impedance (open) permits the LM2650 to move freely and automatically between the modes, using PWM for moderate to heavy loads and sleep for light loads. |
| 3, 4, 9, 10 | PGND: The ground return of the power stage. The power stage consists of the two power switches Q1 and Q2, the gate drivers DH and DL, and the linear voltage regulators VRegH and VRegL. For best electrical and thermal performance, ground these pins to a large, uninterrupted copper plane. |
| 5, 8 | SW: The output node of the power stage. It swings from slightly below ground to slightly below the voltage at $P V_{I N}$. To minimize the effects of switching noise on nearby circuitry, keep all traces originating from SW short and to the point. Route all traces carrying signals well away from SW and SW traces. |
| 6, 7 | $P V_{I N}$ : The positive supply rail of the power stage. Bypass each $P V_{I N}$ pin to $P G N D$ with a $0.1 \mu \mathrm{~F}$ capacitor. Use capacitors having low ESL and low ESR, and locate them close to the IC. |
| 11 | BOOT: The positive supply rail of the high-side gate driver DH. Connect a $0.1 \mu \mathrm{~F}$ capacitor from this node to SW . Bootstrapping action creates a supply rail about 9 V above that at $\mathrm{PV} \mathrm{IN}_{\mathrm{IN}}$, and DH uses this rail to overdrive the gate of the NMOS power FET Q1. Overdriving ensures low $R_{D S}(o n)$. |
| 13 | FB: The feedback input. |
| 14 | $\mathbf{V}_{\mathrm{DD}}$ : An internal regulator steps the input voltage down to a 4 V rail used by the signal-level circuitry. $\mathrm{V}_{\mathrm{DD}}$ is the output node of this regulator. Bypass $\mathrm{V}_{\mathrm{DD}}$ to GND close to the IC with a $0.2 \mu \mathrm{~F}$ capacitor. |
| 15 | COMP: The inverting input of the error amplifier EA. |
| 16 | EA OUT: The output node of the error amplifier EA. |
| 17 | SS: The soft start node. Connect a capacitor from SS to GND. |
| 18 | GND: The ground return of the signal-level circuitry. |
| 19 | $\mathrm{V}_{\text {IN }}$ : The positive supply rail of the internal 4 V regulator. Bypass $\mathrm{V}_{\text {IN }}$ to GND close to the IC with a $0.1 \mu \mathrm{~F}$ capacitor. |
| 20 | FREQ ADJ: The LM2650 switches at a nominal 90 kHz . Connect a resistor between FREQ ADJ and GND to adjust the frequency up from the nominal. Use the graph under Typical Performance Characteristics to select the resistor. |
| 21 | SYNC: The synchronization input. If the switching frequency is to be synchronized with an external clock signal, apply the clock signal here. |
| 22 | SD: Use this logic input to control shutdown; pull low for operation, high for shutdown. |
| 23 | SLEEP OUT ADJ (SOA): The value of the resistor connected between SOA and ground programs the sleep-out threshold. Higher values program lower thresholds. |
| 24 | SLEEP IN ADJ (SIA): The value of the resistor connected between SIA and ground programs the sleep-in threshold. Hgher values program lower thresholds. |

Block Diagrams


TL/H/12848-16
FIGURE 3. The Hysteretic or "Sleep" Circuit with External Components in a Closed Control Loop


TL/H/12848-21
FIGURE 4. The Internal Voltage Regulator and Voltage Reference Used by Both the PWM and Hysteretic Circuits

## Operation

## overview

The LM2650 uses two step-down conversion modes: fixedfrequency pulse-width modulation (PWM) and hysteretic. It moves freely and automatically between them, using PWM for moderate to heavy loads and hysteretic for light loads.
For clarity, separate block diagrams for each conversion mode have been included. See Figures 2 and 3. Blocks used in both modes appear in both diagrams with the same label. For example, both modes use the input buffer B. To keep the diagrams simple, most power supply rails have been omitted. R3, C10, $\mathrm{R}_{\mathrm{C}}, \mathrm{C}_{\mathrm{C}}, \mathrm{C}_{\mathrm{B}}, \mathrm{L} 1, \mathrm{R} 1, \mathrm{R} 2$, and $\mathrm{C}_{\mathrm{OUT}}$ are outside the IC.

## THE PWM CIRCUIT (Figure 2)

The PWM circuit is a fixed-frequency, voltage-mode pulsewidth modulator. It consists of four functional blocks: an input buffer, an error amplifier, a modulator, and a power stage.

1. The input buffer $B$ : $B$ is a voltage follower. $A$ fraction of the output voltage is fed back to its noninverting input FB. Circumventing $B$ by using the COMP input as the feedback input will cause the IC to malfunction.
2. The error amplifier EA: EA is a voltage amplifier. It subtracts the feedback voltage from the 1.25 V reference and amplifies the difference to produce an error voltage for the control loop. For the purpose of loop compensation, EA is typically configured as an integrator. In this configuration, a capacitor $\mathrm{C}_{\mathrm{C}}$ and a resistor $\mathrm{R}_{\mathrm{C}}$ are connected in series between the inverting input COMP and the output terminal EA OUT. The capacitor and the internal $6.5 \mathrm{k} \Omega$ resistor create a pole, while the capacitor and series resistor create a zero
3. The modulator: The modulator is the heart of the PWM circuit. It consists of the 90 kHz oscillator, the voltage comparator C1, and output logic represented here as a simple SR latch.
The modulator generates a continuous stream of rectangular, signal-level pulses. It generates the pulses at a fixed frequency, and it modulates or varies their widths in response to variations in the error voltage. The pulses appear at Q, the output of the SR latch. An increase in the error voltage results in a proportional increase in the pulse widths, and, conversely, a decrease in the error voltage results in a proportional decrease in the pulse widths.
The oscillator produces a 90 kHz sawtooth that ramps between 1 V and 2 V . At the beginning of each ramp, the oscillator sets the SR latch sending $Q$ high. As the ramp voltage surpasses the error voltage, C1 resets the SR latch sending $Q$ low. An increase in the error voltage increases the time between the setting and the resetting of the SR latch which, in turn, results in an equal increase in the pulse widths; that is, an equal increase in the time $Q$ spends high each cycle. A decrease in the error voltage has the opposite effect on the pulse widths as it decreases the time between the setting and resetting of the SR latch.
4. The power stage: The power stage puts some punch behind the output of the modulator by translating the stream of signal-level pulses generated by the modulator into a stream of power pulses that swing from ground up to the input voltage while sinking and sourcing as much as 3.5A. The power stage consists of two gate drivers DH and DL, two linear voltage regulators VRegH and VRegL, and two NMOS power FETs Q1 and Q2.
The power pulses appear at the SW node. When Q goes high, DL drives the gate of Q2 low turning Q2 off. While Q2 turns off, the SW potential may remain at just below ground as the body diode of Q2 conducts what was previously reverse current (source-to-drain) in Q2, or the SW potential may swing up to just above the input voltage as the body diode of Q1 conducts what was previously forward current (drain-to-source) in Q2. About 50 ns after Q goes high, DH drives the gate of Q1 high turning Q1 on. If the task remains, Q1 pulls the SW potential up, if not, Q1 simply takes over conduction responsibility from its own body diode. When Q goes low, the inverse action occurs resulting in the SW potential swinging from the input voltage to ground. The 50 ns delay between one switch beginning to turn off and the other switch beginning to turn on prevents the switches from conducting at the same time and therefore prevents current from "shooting through" directly from the input supply to ground.
The PWM circuit drives the pulse stream into the lowpass filter made up of L1 and COUT. The filter passes the DC component of the stream and attenuates the AC components. The output of the filter is the DC voltage VOUT superimposed with a small ripple voltage. Since the DC component of any periodic waveform is the average value of the waveform, VOUT can be found using:

$$
\begin{equation*}
\mathrm{V}_{\text {OUT }}=\frac{1}{\mathrm{~T}} \times \int_{0}^{\mathrm{T}} \mathrm{v}(\mathrm{t}) \mathrm{dt} . \tag{1}
\end{equation*}
$$

Here $T$ is the switching period in seconds and $v(t)$ is the pulse stream. Under DC steady-state conditions, (1) yields

$$
\begin{equation*}
V_{\text {OUT }}=V_{I N} \times \frac{t_{O N}}{T}=V_{I N} \times D \tag{2}
\end{equation*}
$$

Here $\mathrm{V}_{\mathrm{IN}}$ is the input voltage, and therefore the height of the pulses, in volts, toN is the width of the pulses in seconds, and $D$ is the ratio of $t_{O N}$ to $T$, the duty ratio or duty cycle.
The output voltage is programmed using the resistive divider made up of R1 and R2,

$$
\begin{equation*}
\mathrm{V}_{\text {OUT }}=1.25 \times\left(1+\frac{\mathrm{R} 1}{\mathrm{R} 2}\right) \tag{3}
\end{equation*}
$$

As Q1 turns on, its source voltage swings up to just below the input voltage. The LM2650 uses a simple technique called "bootstrapping" to pull the positive supply rail of DH (at BOOT) up along with the source voltage of Q1, but to a voltage above the input voltage. Because the source of Q1 and the positive supply rail of DH make the same voltage swing together, DH maintains the positive gate-

## Operation (Continued)

to-source voltage required to turn Q1 on. Q1 plays an active role in pulling the supply rail of DH up and is therefore said to pull itself up by its "bootstraps", thus the name of the technique and of the BOOT pin.
In the typical application, a capacitor CB is connected outside the IC between the BOOT and SW pins. When Q2 is on, the input supply charges CB through VRegH and the internal diode D.

## THE HYSTERETIC CIRCUIT AND LOOP (Figure 3)

Except for C2, the hysteretic circuit borrows all its circuit blocks from the PWM circuit.
The hysteretic comparator C2 is a voltage comparator with built-in hysteresis $\mathrm{V}_{\text {HYST }}$ of typically 30 mV centered at 1.25 V .

The diode D2 is the body diode of Q2. The hysteretic circuit uses D2 as a rectifier instead of switching Q2 as a synchronous rectifier.
When the load current drops below the prescribed sleep-in threshold, the LM2650 shuts down the PWM loop and starts up the hysteretic loop. The hysteretic loop supports light loads more efficiently because it uses less power to support its own operation; it uses less bias power because it's a simpler loop having less circuit blocks to bias, and it switches slower, so it incurs lower switching losses.
The hysteretic control loop does not switch at a constant frequency. Instead, it monitors $\mathrm{V}_{\text {OUT }}$ and switches only when $V_{\text {OUT }}$ reaches either side of a narrow window centered on the desired output voltage. C2 directs the switching based on its reading of the feedback voltage. Switching in this manner yields a regulated voltage consisting of the desired output voltage and an AC ripple voltage. The magnitude of the AC component can be approximated using

$$
\begin{equation*}
V_{\text {OUT_PP }}=V_{\text {HYST }} \times \frac{(R 1+R 2)}{R 2} \tag{4}
\end{equation*}
$$

For example, with $\mathrm{V}_{\text {OUT }}$ set to 5 V , $\mathrm{V}_{\text {OUT_PP }}$ is approximately 120 mV ,

$$
\mathrm{V}_{\text {OUT_PP }}=0.03 \times \frac{(75+24.9)}{24.9}=120 \mathrm{mV}
$$

When it starts up, the hysteretic loop turns Q1 on. While Q1 is on, the input power supply charges COUT and supplies current to the load. Current from the supply reaches COUT and the load via the series path provided by Q1 and L1. As the feedback voltage just surpasses the upper hysteretic threshold of C2, the output of C2 changes states from high to low, and DH responds by pulling the gate of Q1 down turning Q1 off. As Q1 turns off, L1 generates a negative-going voltage transient that D2 clamps at just below ground. D2 remains on only briefly as the current in L1 runs out. While both Q1 and D2 are off, COUT alone supplies current to the load. As the feedback voltage just surpasses the lower hysteretic threshold of C2, the output of C2 changes states from low to high, and DH responds by pulling the gate of Q1 up turning Q1 on and starting the hysteretic cycle over.
Notice that as the load current decreases, it takes increasingly longer periods for the load current to discharge COUT through the hysteretic window, and as the load current increases, the periods become ever shorter. It can be seen from the above observation that the switching frequency of the hysteretic loop varies as the load varies. The switching frequency can be approximated using

$$
\begin{equation*}
f=\frac{1}{\left(\mathrm{C}_{\text {OUT }} \times \mathrm{V}_{\text {OUT_PPP }}\right)} \tag{5}
\end{equation*}
$$

Here $f$ is the switching frequency in hertz, $I$ is the load current in amperes, COUT is the value of the output capacitor in farads, and VOUT_PP is the magnitude of the AC ripple voltage in volts. Typical switching frequencies range anywhere from a few hertz for very light loads to a few thousand hertz for light loads bordering on the moderate level.

## Application Circuits

Figure 5 is a schematic of the typical application circuit. Use the component values shown in the figure and those contained in Table I to build a 5V, 3A or 3.3V, 3A step-down DC/DC converter. As with the design of any DC/DC converter, the design of these circuits involved tradeoffs between efficiency, size, and cost. Here more weight was given to efficiency than to size as evidenced by the low switching frequency which keeps switching losses low but pushes the value and size of the inductor up.

For a smaller circuit, use the component values shown in Figure 5 and those contained in Table III. These circuits trade slightly higher switching losses for a much smaller inductor. Note, Figure 5 does not show $\mathrm{R}_{\mathrm{FA}}$, the resistor required to adjust the switching frequency from 90 kHz up to 200 kHz . Connect RFA between the FREQ ADJ pin and ground.


TL/H/12848-19
FIGURE 5. The Typical 90 kHz Application Circuit
TABLE I. Components for the Typical 90 kHz Application Circuit

| Input Voltage | 7 V to 18V IN |  |
| :---: | :---: | :---: |
| Applicable Cell Stacks | 8 to 12 Cell NiCd or NiMH, 3 to 4 Cell Li Ion, 8 to 11 Cell Alkaline, 6 Cell Lead Acid |  |
| Output | 5V, 3A Out | 3.3V, 3A Out |
| Input Capacitor $\mathrm{C}_{\mathrm{IN}}$ | $2 \times 22 \mu \mathrm{~F}, 35 \mathrm{~V}$ AVX TPS <br> Series or Sprague 593D Series | $2 \times 22 \mu \mathrm{~F}, 35 \mathrm{~V}$ AVX TPS <br> Series or Sprague 593D Series |
| Inductor L1 | $40 \mu \mathrm{H}$ (See Table II) | $33 \mu \mathrm{H}$ (See Table II) |
| Output Capacitor Cout | $3 \times 220 \mu \mathrm{~F}, 10 \mathrm{~V}$ AVX TPS <br> Series or Sprague 593D Series | $3 \times 220 \mu \mathrm{~F}, 10 \mathrm{~V}$ AVX TPS <br> Series or Sprague 593D Series |
| Feedback Resistors R1 and R2 | $\begin{aligned} & \mathrm{R} 1=75 \mathrm{k} \Omega, 1 \%, \\ & \mathrm{R} 2=24.9 \mathrm{k} \Omega, 1 \% \\ & \hline \end{aligned}$ | $\begin{aligned} & \mathrm{R} 1=41.2 \mathrm{k} \Omega, 1 \%, \\ & \mathrm{R} 2=24.9 \mathrm{k} \Omega, 1 \% \end{aligned}$ |
| Compensation Components $\mathrm{R}_{\mathrm{C}}, \mathrm{C}_{\mathrm{C}}, \mathrm{R} 3$, and C10 | $\begin{aligned} & \mathrm{R}_{\mathrm{C}}=37.4 \mathrm{k} \Omega, \\ & \mathrm{C}_{\mathrm{C}}=4.7 \mathrm{nF}, \\ & \mathrm{R} 3=3.57 \mathrm{k} \Omega, \\ & \mathrm{C} 10=5.6 \mathrm{nF} \end{aligned}$ | $\begin{aligned} & \mathrm{R}_{\mathrm{C}}=23.2 \mathrm{k} \Omega, \\ & \mathrm{C}_{\mathrm{C}}=8.2 \mathrm{nF}, \\ & \mathrm{R} 3=2.0 \mathrm{k} \Omega, \\ & \mathrm{C} 10=10 \mathrm{nF} \end{aligned}$ |
| Sleep Resistors R SIA and $\mathrm{R}_{\mathrm{SOA}}$ | $\begin{aligned} & \mathrm{R}_{\mathrm{SIA}}=33 \mathrm{k} \Omega, \\ & \mathrm{R}_{\mathrm{SOA}}=200 \mathrm{k} \Omega \end{aligned}$ | $\begin{aligned} & \mathrm{R}_{\mathrm{SIA}}=39 \mathrm{k} \Omega, \\ & \mathrm{R}_{\mathrm{SOA}}=130 \mathrm{k} \Omega \end{aligned}$ |

## Application Circuits (Continued)

TABLE II. Toroidal Inductors Using Cores from MICROMETALS, INC.

|  | Core Number | Core Material | Wire Gauge | Number of Strands | Number of Turns |
| :---: | :---: | :---: | :---: | :---: | :---: |
| $15 \mu \mathrm{H}$ | T38 | -52 | AWG \#23 | 1 | 21 |
| $20 \mu \mathrm{H}$ | T38 | -52 | AWG \#23 | 1 | 25 |
| $33 \mu \mathrm{H}$ | T50 | -52 | AWG \#21 | 1 | 41 |
| $40 \mu \mathrm{H}$ | T50 (B) | -18 | AGW \#21 | 1 | 41 |

micRometals
5615 E. La Palma Ave. Anaheim, CA 92807 USA (800) 356-5977
TABLE III. Components for Typical 200 kHz Applications

| Input Voltage | 7V to 18V IN |  |
| :---: | :---: | :---: |
| Applicable Cell Stacks | 8 to 12 Cell NiCd or NiMH, 3 to 4 Cell Li Ion, 8 to 11 Cell Alkaline, 6 Cell Lead Acid |  |
| Output | 5V, 3A Out | 3.3V, 3A Out |
| Input Capacitor $\mathrm{C}_{\mathrm{IN}}$ | $2 \times 22 \mu \mathrm{~F}, 35 \mathrm{~V}$ AVX TPS <br> Series or Sprague 593D Series | $2 \times 22 \mu \mathrm{~F}, 35 \mathrm{~V}$ AVX TPS <br> Series or Sprague 593D Series |
| Inductor L1 | $20 \mu \mathrm{H}$ (See Table II) | $15 \mu \mathrm{H}$ (See Table II) |
| Output Capacitor COUT | $3 \times 220 \mu \mathrm{~F}, 10 \mathrm{~V}$ AVX TPS <br> Series or Sprague 593D Series | $3 \times 220 \mu \mathrm{~F}, 10 \mathrm{~V}$ AVX TPS <br> Series or Sprague 593D Series |
| Feedback Resistors R1 and R2 | $\begin{aligned} & \mathrm{R} 1=75 \mathrm{k} \Omega, 1 \%, \\ & \mathrm{R} 2=24.9 \mathrm{k} \Omega, 1 \% \end{aligned}$ | $\begin{aligned} & \mathrm{R} 1=41.2 \mathrm{k} \Omega, 1 \%, \\ & \mathrm{R} 2=24.9 \mathrm{k} \Omega, 1 \% \end{aligned}$ |
| Compensation Components $\mathrm{R}_{\mathrm{C}}, \mathrm{C}_{\mathrm{C}}, \mathrm{R} 3$, and C10 | $\begin{aligned} & \mathrm{R}_{\mathrm{C}}=53.6 \mathrm{k} \Omega, \\ & \mathrm{C}_{\mathrm{C}}=2.7 \mathrm{nF}, \\ & \mathrm{R}_{3}=4.02 \mathrm{k} \Omega, \\ & \mathrm{C} 10=4.7 \mathrm{nF} \end{aligned}$ | $\begin{aligned} & \mathrm{R}_{\mathrm{C}}=33.2 \mathrm{k} \Omega, \\ & \mathrm{C}_{\mathrm{C}}=3.9 \mathrm{nF}, \\ & \mathrm{R} 3=3.01 \mathrm{k} \Omega, \\ & \mathrm{C} 10=6.8 \mathrm{nF} \end{aligned}$ |
| Sleep Resistors RSIA and RSOA | $\begin{aligned} & \mathrm{R}_{\mathrm{SIA}}=47 \mathrm{k} \Omega, \\ & \mathrm{R}_{\mathrm{SOA}}=200 \mathrm{k} \Omega \end{aligned}$ | $\begin{aligned} & \mathrm{R}_{\mathrm{SIA}}=47 \mathrm{k} \Omega, \\ & \mathrm{R}_{\mathrm{SOA}}=91 \mathrm{k} \Omega \end{aligned}$ |
| Frequency Adjusting Resistor R $\mathrm{FA}_{\mathrm{F}}$ | $\mathrm{R}_{\mathrm{FA}}=24.9 \mathrm{k} \Omega$, | $\mathrm{R}_{\mathrm{FA}}=24.9 \mathrm{k} \Omega$ |

## Application Circuits (Continued)




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National Semiconductor

## LM2825 SIMPLE SWITCHER ${ }^{\circledR}$

## 1A DC-DC Converter in 24-Pin DIP Package

## General Description

The LM2825 is a complete 1A DC-DC Buck converter packaged in a 24 -lead molded Dual-In-Line integrated circuit package.
Contained within the package are all the active and passive components for a high efficiency step-down (buck) switching regulator. Available in fixed output voltages of 3.3 V and 5 V , these devices can provide up to 1 A of load current with fully guaranteed electrical specifications over the full operating temperature range.
Self-contained, this converter is also fully protected from output fault conditions, such as excessive load current, short circuits, or excessive temperatures.

## Highlights

- Integrated circuit reliability
- MTBF over 20 million hours
- Radiated EMI meets Class B stipulated by CISPR 22
- High power density, $35 \mathrm{~W} / \mathrm{in}^{3}$

■ 24-pin DIP package profile ( $1.25 \times 0.54 \times 0.26$ inches)

- Package weight 6 grams

■ No external components required

## Features

- Minimum design time required
- 3.3 V and 5 V fixed output versions
- Guaranteed 1A output current
- Wide input voltage range, up to 40 V

■ Low-power standby mode, $\mathrm{I}_{\mathrm{Q}}$ typically $65 \mu \mathrm{~A}$

- High efficiency, typically $80 \%$
- $\pm 4 \%$ output voltage tolerance
- Excellent line and load regulation

■ TTL shutdown capability/programmable Soft-start

- Thermal shutdown and current limit protection


## Applications

■ Simple high-efficiency step-down (buck) regulator

- On-card switching regulators
- Efficient pre-regulator for linear regulators
- Distributed power systems
- DC/DC module replacement



## Radiated EMI

Radiated emission of electromagnetic fields is measured at 10 m distance. The emission levels are within the Class B limits stipulated by CISPR 22.

| $30 \ldots .230 \mathrm{MHz}$ | $30 \mathrm{~dB} \mu \mathrm{~V} / \mathrm{m}$ |
| :--- | :--- |
| $230 \ldots .1000 \mathrm{MHz}$ | $37 \mathrm{~dB} \mu \mathrm{~V} / \mathrm{m}$ |
| $1 \ldots .10 \mathrm{GHz}$ | $46 \mathrm{~dB} \mu \mathrm{~V} / \mathrm{m}$ |

Connection Diagram


Note: "NC (Do not use)" pins: See Figure 5.
Top View

## Order Information

Order Number LM2825N-3.3 or LM2825N-5.0 See NS Package Number NA24F

| Absolute Maximum Ratings (Note 1) |  |
| :---: | :---: |
| If Military/Aerospace specified dev please contact the National Ser Office/Distributors for availability and | vices are required, miconductor Sales and specifications. |
| Maximum Input Supply ( $\mathrm{V}_{\text {IN }}$ ) | $+45 \mathrm{~V}$ |
| SD/SS Pin Input Voltage (Note 2) | 6 V |
| Output Voltage to Ground (steady state) | -1V |
| Power Dissipation | Internally Limited |
| Storage Temperature Range | $-40^{\circ} \mathrm{C}$ to $+125^{\circ} \mathrm{C}$ |
| ESD Susceptibility |  |
| Human Body Model (Note 3) | 2 kV |
| Lead Temperature (Soldering 10 sec .) | $260^{\circ} \mathrm{C}$ |

## Operating Ratings

Ambient Temperature Range
Junction Temperature Range
Input Supply Voltage (3.3V version)
Input Supply Voltage (5V version)
$0^{\circ} \mathrm{C} \leq \mathrm{T}_{\mathrm{A}} \leq+70^{\circ} \mathrm{C}$
$0^{\circ} \mathrm{C} \leq \mathrm{T}_{\mathrm{J}} \leq+125^{\circ} \mathrm{C}$
4.75 V to 40 V 7 V to 40 V

## LM2825-3.3 Electrical Characteristics

Specifications with standard type face are for $T_{A}=25^{\circ} \mathrm{C}$, and those with boldface type apply over full Operating Temperature Range. (Note 4) Test Circuit Figure 2.


## LM2825-5.0 Electrical Characteristics

Specifications with standard type face are for $\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$, and those with boldface type apply over full Operating Temperature Range. (Note 4) Test Circuit Figure 2.

| Symbol | Parameter | Conditions | LM2825-5.0 |  | Units (Limits) |
| :---: | :---: | :---: | :---: | :---: | :---: |
|  |  |  | Typical <br> (Note 5) | Limit (Note 6) |  |
| VOUT | Output Voltage | $7 \mathrm{~V} \leq \mathrm{V}_{\mathrm{IN}} \leq 40 \mathrm{~V}, 0.1 \mathrm{~A} \leq \mathrm{I}_{\text {LOAD }} \leq 1 \mathrm{~A}$ | 5.0 | $\begin{aligned} & 4.800 / 4.750 \\ & 5.200 / 5.250 \end{aligned}$ | $V(\min )$ <br> V (max) |
|  | Line Regulation | $\begin{aligned} & 7 \mathrm{~V} \leq \mathrm{V}_{\mathrm{IN}} \leq 40 \mathrm{~V} \\ & \mathrm{I}_{\mathrm{LOAD}}=100 \mathrm{~mA} \end{aligned}$ | 2.7 |  | mV |
|  | Load Regulation | $\begin{aligned} & 0.1 \mathrm{~A} \leq \mathrm{I}_{\mathrm{LOAD}} \leq 1 \mathrm{~A} \\ & \mathrm{~V}_{\mathrm{IN}}=12 \mathrm{~V} \end{aligned}$ | 8 |  | mV |
|  | Output Ripple Voltage | $\mathrm{V}_{\text {IN }}=12 \mathrm{~V}, \mathrm{I}_{\text {LOAD }}=1 \mathrm{~A}$ | 40 |  | mV p-p |
| $\eta$ | Efficiency | $\mathrm{V}_{\text {IN }}=12 \mathrm{~V}, \mathrm{I}_{\text {LOAD }}=1 \mathrm{~A}$ | 80 |  | \% |

## All Output Voltage Versions Electrical Characteristics

Specifications with standard type face are for $T_{A}=25^{\circ} \mathrm{C}$, and those with boldface type apply over full Operating Range. Unless otherwise specified, $\mathrm{V}_{\mathrm{IN}}=12 \mathrm{~V}$, $\mathrm{L}_{\text {LOAD }}=100 \mathrm{~mA}$.

| Symbol | Parameter | Conditions | LM2825-XX |  | Units <br> (Limits) |
| :---: | :---: | :---: | :---: | :---: | :---: |
|  |  |  | Typical (Note 5) | Limit (Note 6) |  |
| ${ }^{\text {ICL }}$ | DC Output Current Limit | $\mathrm{V}_{\mathrm{IN}}=12 \mathrm{~V}, \mathrm{R}_{\mathrm{L}}=0 \Omega$ | 1.4 | $\begin{aligned} & 1.2 \\ & 2.4 \end{aligned}$ |  |
| $\mathrm{I}_{\mathrm{Q}}$ | Operating Quiescent Current | $\begin{aligned} & \text { SD/SS Pin }=3 V \\ & \text { (Note 7) } \end{aligned}$ | 5 | 10 | $\begin{gathered} \mathrm{mA} \\ \mathrm{~mA}(\max ) \end{gathered}$ |
| IstBy | Standby Quiescent Current | $\begin{aligned} & \text { SD/SS Pin }=0 \mathrm{~V} \\ & \text { (Note 7) } \end{aligned}$ | 65 | 200 | $\begin{gathered} \mu \mathrm{A} \\ \mu \mathrm{~A}(\max ) \end{gathered}$ |
| $\mathrm{fo}_{0}$ | Oscillator Frequency | (Note 8) | 150 |  | kHz |
| $\theta_{\text {JA }}$ | Thermal Resistance | Junction to Ambient (Note 9) | 30 |  | ${ }^{\circ} \mathrm{C} / \mathrm{W}$ |
| SHUTDOWN/SOFT-START CONTROL Test Circuit Figure 2 |  |  |  |  |  |
| $\mathrm{V}_{\text {SD }}$ | Shutdown Threshold Voltage | Low (Shutdown Mode) <br> High (Soft-start Mode) | 1.3 | $\begin{aligned} & 0.6 \\ & 2.0 \\ & \hline \end{aligned}$ | V <br> V (max) <br> V (min) |
| $\mathrm{V}_{\text {SS }}$ | Soft-start Voltage | $\mathrm{V}_{\text {OUT }}=20 \%$ of Nominal Output Voltage <br> $V_{\text {OUT }}=100 \%$ of Nominal Output Voltage | $\begin{aligned} & 2 \\ & 3 \end{aligned}$ |  | V |
| ISD | Shutdown Current | $V_{\text {SHUTDOWN }}=0.5 \mathrm{~V}$ <br> (Note 7) | 5 | 10 | $\mu \mathrm{A}$ $\mu \mathrm{A}$ (max) |
| Iss | Soft-start Current | $\mathrm{V}_{\text {SOFT-START }}=2.5 \mathrm{~V}$ <br> (Note 7) | 1.6 | 5 | $\mu \mathrm{A}$ $\mu \mathrm{A}$ (max) |

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but do not guarantee specific performance limits. For guaranteed specifications and test conditions, see the Electrical Characteristics
Note 2: Voltage internally clamped. If clamp voltage is exceeded, limit current to a maximum of 5 mA .
Note 3: The human body model is a 100 pF capacitor discharged through a 1.5 k resistor into each pin.
Note 4: When the LM2825 is used as shown in Figure 2 test circuit, system performance will be as shown in Electrical Characteristics.
Note 5: Typical numbers are at $25^{\circ} \mathrm{C}$ and represent the most likely norm.
Note 6: All limits guaranteed at room temperature (standard type face) and at temperature extremes (bold type face). All room temperature limits are $100 \%$ production tested. All limits at temperature extremes are guaranteed via correlation using standard Statistical Quality Control (SQC) methods. All limits are used to calculate Average Outgoing Quality Level (AOQL).
Note 7: $I_{\text {LOAD }}=0 \mathrm{~A}$.
Note 8: The switching frequency is reduced when the second stage current limit is activated. The amount of reduction is determined by the severity of current overload.
Note 9: Junction to ambient thermal resistance (no external heat sink) for the DIP-24 package with the leads soldered to a printed circuit board with (1 oz.) copper area of approximately $2 \mathrm{in}^{2}$.


## Typical Performance Characteristics

(Circuit of Figure 2) Unless otherwise specified, $\mathrm{V}_{\mathrm{IN}}=12 \mathrm{~V}, \mathrm{I}_{\text {LOAD }}=100 \mathrm{~mA}$ (Continued)



FIGURE 1. Typical Load Transient Response

## Test Circuit



TL/H/12661-19
*Optional—Required if package is more than 6" away from main filter or bypass capacitor.
**Optional Soft-start Capacitor
$\mathrm{V}_{\mathrm{IN}}=40 \mathrm{~V}$ (max)
$\mathrm{V}_{\text {OUT }}=3.3 \mathrm{~V}$ or 5 V
$I_{\text {LOAD }}=1 \mathrm{~A}$

FIGURE 2. Standard Test Circuit

## Application Information

## OPTIONAL EXTERNAL COMPONENTS

## SOFT-START CAPACITOR

$\mathrm{C}_{\text {ss }}$ : A capacitor on this pin provides the regulator with a Soft-start feature (slow start-up). The current drawn from the source starts out at a low average level with narrow pulses, and ramps up in a controlled manner as the pulses expand to their steady-state width. This reduces the startup current considerably, and delays and slows down the output voltage rise time.
It is especially useful in situations where the input power source is limited in the amount of current it can deliver, since you avoid loading down this type of power supply.
Under some operating conditions, a Soft-start capacitor is required for proper operation. Figure 3 indicates the input voltage and ambient temperature conditions for which a Soft-start capacitor may be required.
This curve is typical for full 1 A loads and can be used as a guideline. As the output current decreases, the operating area requiring a Soft-start capacitor decreases. Capacitor values between $0.1 \mu \mathrm{~F}$ and $1 \mu \mathrm{~F}$ are recommended. Tantalum or ceramic capacitors are appropriate for this application.

## INPUT CAPACITOR

$\mathbf{C}_{\mathbf{I N}}$ : An optional input capacitor is required if the package is more than $6^{\prime \prime}$ away from the main filter or bypass capacitor. A low ESR aluminum or tantalum bypass capacitor is recommended between the input pin and ground to prevent large voltage transients from appearing at the input. In addition, to be conservative, the RMS current rating of the input capacitor should be selected to be at least $1 / 2$ the DC load current. With a 1A load, a capacitor with a RMS current rating of at least 500 mA is recommended.
The voltage rating should be approximately 1.25 times the maximum input voltage. With a nominal input voltage of 12V, an aluminum electrolytic capacitor (Panasonic HFQ series or Nichicon PL series or equivalent) with a voltage rating greater than $15 \mathrm{~V}\left(1.25 \times \mathrm{V}_{\mathrm{IN}}\right)$ would be needed.

Solid tantalum input capacitors should only be used where the input source is impedance current limited. High $\mathrm{dV} / \mathrm{dt}$ applied at the input can cause excessive charge current through low ESR tantalum capacitors. This high charge current can result in shorting within the capacitor. It is recommended that they be surge current tested by the manufacturer.The TPS series available from AVX, and the 593D series from Sprague are both surge current tested.
Use caution when using ceramic capacitors for input bypassing, because it may cause ringing at the $\mathrm{V}_{\mathrm{IN}}$ pin.

## SHUTDOWN

The circuit shown in Figure 4 shows 2 circuits for the $\overline{\text { Shutdown }}$ /Soft-start feature using different logic signals for shutdown and using a $0.1 \mu \mathrm{~F}$ Soft-start capacitor.

## THERMAL CONSIDERATIONS

The LM2825 is available in a 24 -pin through hole DIP. The package is molded plastic with a copper lead frame. When the package is soldered to the PC board, the copper and the board are the heat sink for the LM2825.


TL/H/12661-22
FIGURE 3. Usage of the Soft-start Capacitor

## Application Information (Continued)



FIGURE 4. Typical Circuits Using Shutdown/Soft-Start Features

TYPICAL THROUGH HOLE PC BOARD LAYOUT (2X SIZE), SINGLE SIDED, THROUGH HOLE PLATED


## Note: Holes are not shown.

"No Connect Pins" are connected to copper pads for thermal reasons only and must remain electrically isolated.

FIGURE 5. 2X Printed Circuit Board Layout


24-Lead ( $0.600^{\prime \prime}$ Wide) Molded Dual-In-Line Package
Order Number LM2825N-3.3 or LM2825N-5.0 NS Package Number NA24F

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| :---: | :---: | :---: | :---: |

# Boost/Flyback DC/DC Converters 

- LM2585 3A Simple Switcher ${ }^{\text {TM }}$ Converter
- LM2586 3A Simple Switcher ${ }^{\text {TM }}$ Converter with Shutdown
- LM2587 5A Simple Switcher ${ }^{\text {TM }}$ Converter
- LM2588 5A Simple Switcher ${ }^{\text {TM }}$ Converter with Shutdown


Absolute Maximum Ratings (Note 1)
If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

| Input Voltage | $-0.4 \mathrm{~V} \leq \mathrm{V}_{\text {IN }} \leq 45 \mathrm{~V}$ |
| :--- | ---: |
| Switch Voltage | $-0.4 \mathrm{~V} \leq \mathrm{V}_{\mathrm{SW}} \leq 65 \mathrm{~V}$ |
| Switch Current (Note 2) | Internally Limited |
| Compensation Pin Voltage | $-0.4 \mathrm{~V} \leq \mathrm{V}_{\mathrm{COMP}} \leq 2.4 \mathrm{~V}$ |
| Feedback Pin Voltage | $-0.4 \mathrm{~V} \leq \mathrm{V}_{\mathrm{FB}} \leq 2 \mathrm{~V}_{\mathrm{OUT}}$ |
| Power Dissipation (Note 3) | Internally Limited |


| Storage Temperature Range | $-65^{\circ} \mathrm{C}$ to $+150^{\circ} \mathrm{C}$ |
| :--- | ---: |
| Lead Temperature (Soldering, 10 sec.$)$ | $260^{\circ} \mathrm{C}$ |
| Maximum Junction Temperature (Note 3) | $150^{\circ} \mathrm{C}$ |
| Minimum ESD Rating (C = $100 \mathrm{pF}, \mathrm{R}=1.5 \mathrm{k} \Omega)$ | 2 kV |

## Operating Ratings

| Supply Voltage | $4 \mathrm{~V} \leq \mathrm{V}_{I N} \leq 40 \mathrm{~V}$ |
| :--- | ---: |
| Output Switch Voltage | $0 \mathrm{~V} \leq \mathrm{V}_{\text {SW }} \leq 60 \mathrm{~V}$ |
| Output Switch Current | $\mathrm{ISW}^{2} \leq 3.0 \mathrm{~A}$ |
| Junction Temperature Range | $-40^{\circ} \mathrm{C} \leq \mathrm{TJ}_{\mathrm{J}} \leq+125^{\circ} \mathrm{C}$ |

## Electrical Characteristics

Specifications with standard type face are for $T_{J}=25^{\circ} \mathrm{C}$, and those in bold type face apply over full Operating Temperature Range. Unless otherwise specified, $\mathrm{V}_{\mathrm{IN}}=5 \mathrm{~V}$.

## LM2585-3.3

| Symbol | Parameters | Conditions | Typical | Min | Max | Units |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| SYSTEM PARAMETERS Test Circuit of Figure 2 (Note 4) |  |  |  |  |  |  |
| V OUT | Output Voltage | $\begin{aligned} & \mathrm{V}_{I N}=4 \mathrm{~V} \text { to } 12 \mathrm{~V} \\ & \mathrm{I}_{\text {LOAD }}=0.3 \mathrm{~A} \text { to } 1.2 \mathrm{~A} \end{aligned}$ | 3.3 | 3.17/3.14 | 3.43/3.46 | V |
| $\Delta V_{\text {OUT }} /$ <br> $\Delta \mathrm{V}_{\mathrm{IN}}$ | Line Regulation | $\begin{aligned} & \mathrm{V}_{I N}=4 \mathrm{~V} \text { to } 12 \mathrm{~V} \\ & \mathrm{I}_{\text {LOAD }}=0.3 \mathrm{~A} \end{aligned}$ | 20 |  | 50/100 | mV |
| $\Delta \mathrm{V}_{\text {OUT }} /$ <br> $\Delta I_{\text {LOAD }}$ | Load Regulation | $\begin{aligned} & \mathrm{V}_{I N}=12 \mathrm{~V} \\ & \mathrm{I}_{\mathrm{LOAD}}=0.3 \mathrm{~A} \text { to } 1.2 \mathrm{~A} \end{aligned}$ | 20 |  | 50/100 | mV |
| $\eta$ | Efficiency | $\mathrm{V}_{\mathrm{IN}}=5 \mathrm{~V}, \mathrm{I}_{\text {LOAD }}=0.3 \mathrm{~A}$ | 76 |  |  | \% |
| UNIQUE DEVICE PARAMETERS (Note 5) |  |  |  |  |  |  |
| $V_{\text {REF }}$ | Output Reference Voltage | Measured at Feedback Pin $\mathrm{V}_{\mathrm{COMP}}=1.0 \mathrm{~V}$ | 3.3 | 3.242/3.234 | 3.358/3.366 | V |
| $\Delta \mathrm{V}_{\text {REF }}$ | Reference Voltage Line Regulation | $\mathrm{V}_{\mathrm{IN}}=4 \mathrm{~V}$ to 40 V | 2.0 |  |  | mV |
| $\mathrm{G}_{\mathrm{M}}$ | Error Amp <br> Transconductance | $\begin{aligned} & \mathrm{I}_{\mathrm{COMP}}=-30 \mu \mathrm{~A} \text { to }+30 \mu \mathrm{~A} \\ & \mathrm{~V}_{\mathrm{COMP}}=1.0 \mathrm{~V} \end{aligned}$ | 1.193 | 0.678 | 2.259 | mmho |
| Avol | Error Amp <br> Voltage Gain | $\begin{aligned} & \mathrm{V}_{\mathrm{COMP}}=0.5 \mathrm{~V} \text { to } 1.6 \mathrm{~V} \\ & \left.\mathrm{R}_{\mathrm{COMP}}=1.0 \mathrm{M} \Omega \text { (Note } 6\right) \end{aligned}$ | 260 | 151/75 |  | V/V |

LM2585-5.0

| Symbol | Parameters | Conditions | Typical | Min | Max | Units |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| SYSTEM PARAMETERS Test Circuit of Figure 2 (Note 4) |  |  |  |  |  |  |
| $V_{\text {OUT }}$ | Output Voltage | $\begin{aligned} & \mathrm{V}_{\text {IN }}=4 \mathrm{~V} \text { to } 12 \mathrm{~V} \\ & \mathrm{I}_{\text {LOAD }}=0.3 \mathrm{~A} \text { to } 1.1 \mathrm{~A} \end{aligned}$ | 5.0 | 4.80/4.75 | 5.20/5.25 | V |
| $\Delta \mathrm{V}_{\text {OUT }} /$ <br> $\Delta \mathrm{V}_{\mathrm{IN}}$ | Line Regulation | $\begin{aligned} & \mathrm{V}_{\text {IN }}=4 \mathrm{~V} \text { to } 12 \mathrm{~V} \\ & \mathrm{I}_{\text {LOAD }}=0.3 \mathrm{~A} \end{aligned}$ | 20 |  | 50/100 | mV |
| $\Delta \mathrm{V}_{\text {OUT }} /$ <br> $\Delta$ loAd $^{\prime}$ | Load Regulation | $\begin{aligned} & \mathrm{V}_{I N}=12 \mathrm{~V} \\ & \mathrm{I}_{\text {LOAD }}=0.3 \mathrm{~A} \text { to } 1.1 \mathrm{~A} \end{aligned}$ | 20 |  | 50/100 | mV |
| $\eta$ | Efficiency | $\mathrm{V}_{\mathrm{IN}}=12 \mathrm{~V}, \mathrm{I}$ LOAD $=0.6 \mathrm{~A}$ | 80 |  |  | \% |

## Electrical Characteristics

Specifications with standard type face are for $\mathrm{T}_{J}=25^{\circ} \mathrm{C}$, and those in bold type face apply over full Operating Temperature Range. Unless otherwise specified, $\mathrm{V}_{\mathrm{IN}}=5 \mathrm{~V}$. (Continued)
LM2585-5.0 (Continued)

| Symbol | Parameters | Conditions | Typical | Min | Max | Units |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| UNIQUE DEVICE PARAMETERS (Note 5) |  |  |  |  |  |  |
| $V_{\text {REF }}$ | Output Reference Voltage | Measured at Feedback Pin $\mathrm{V}_{\mathrm{COMP}}=1.0 \mathrm{~V}$ | 5.0 | 4.913/4.900 | 5.088/5.100 | V |
| $\Delta V_{\text {REF }}$ | Reference Voltage Line Regulation | $\mathrm{V}_{\mathrm{IN}}=4 \mathrm{~V}$ to 40 V | 3.3 |  |  | mV |
| $\mathrm{G}_{\mathrm{M}}$ | Error Amp <br> Transconductance | $\begin{aligned} & \mathrm{I}_{\mathrm{COMP}}=-30 \mu \mathrm{~A} \text { to }+30 \mu \mathrm{~A} \\ & \mathrm{~V}_{\mathrm{COMP}}=1.0 \mathrm{~V} \end{aligned}$ | 0.750 | 0.447 | 1.491 | mmho |
| Avol | Error Amp <br> Voltage Gain | $\begin{aligned} & \mathrm{V}_{\mathrm{COMP}}=0.5 \mathrm{~V} \text { to } 1.6 \mathrm{~V} \\ & \left.\mathrm{R}_{\mathrm{COMP}}=1.0 \mathrm{M} \Omega \text { (Note } 6\right) \end{aligned}$ | 165 | 99/49 |  | V/V |

## LM2585-12

| Symbol | Parameters | Conditions | Typical | Min | Max | Units |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| SYSTEM PARAMETERS Test Circuit of Figure 3 (Note 4) |  |  |  |  |  |  |
| Vout | Output Voltage | $\begin{aligned} & \mathrm{V}_{\text {IN }}=4 \mathrm{~V} \text { to } 10 \mathrm{~V} \\ & \mathrm{I}_{\text {LOAD }}=0.2 \mathrm{~A} \text { to } 0.8 \mathrm{~A} \end{aligned}$ | 12.0 | 11.52/11.40 | 12.48/12.60 | V |
| $\Delta \mathrm{V}_{\text {OUT }} /$ <br> $\Delta V_{\text {IN }}$ | Line Regulation | $\begin{aligned} & \mathrm{V}_{\mathrm{IN}}=4 \mathrm{~V} \text { to } 10 \mathrm{~V} \\ & \mathrm{I}_{\text {LOAD }}=0.2 \mathrm{~A} \end{aligned}$ | 20 |  | 100/200 | mV |
| $\Delta \mathrm{V}_{\text {OUT }} /$ <br> $\Delta l_{\text {LOAD }}$ | Load Regulation | $\begin{aligned} & \mathrm{V}_{I N}=10 \mathrm{~V} \\ & \mathrm{I}_{\text {LOAD }}=0.2 \mathrm{~A} \text { to } 0.8 \mathrm{~A} \end{aligned}$ | 20 |  | 100/200 | mV |
| $\eta$ | Efficiency | $\mathrm{V}_{\mathrm{IN}}=10 \mathrm{~V}, \mathrm{ILOAD}=0.6 \mathrm{~A}$ | 93 |  |  | \% |
| UNIQUE DEVICE PARAMETERS (Note 5) |  |  |  |  |  |  |
| $V_{\text {REF }}$ | Output Reference Voltage | Measured at Feedback Pin $\mathrm{V}_{\mathrm{COMP}}=1.0 \mathrm{~V}$ | 12.0 | 11.79/11.76 | 12.21/12.24 | V |
| $\Delta V_{\text {REF }}$ | Reference Voltage Line Regulation | $\mathrm{V}_{\text {IN }}=4 \mathrm{~V}$ to 40 V | 7.8 |  |  | mV |
| $\mathrm{G}_{\mathrm{M}}$ | Error Amp <br> Transconductance | $\begin{aligned} & \mathrm{I}_{\mathrm{COMP}}=-30 \mu \mathrm{~A} \text { to }+30 \mu \mathrm{~A} \\ & \mathrm{~V}_{\mathrm{COMP}}=1.0 \mathrm{~V} \end{aligned}$ | 0.328 | 0.186 | 0.621 | mmho |
| Avol | Error Amp Voltage Gain | $\begin{aligned} & \mathrm{V}_{\mathrm{COMP}}=0.5 \mathrm{~V} \text { to } 1.6 \mathrm{~V} \\ & \mathrm{R}_{\mathrm{COMP}}=1.0 \mathrm{M} \Omega(\text { Note } 6) \end{aligned}$ | 70 | 41/21 |  | V/V |

## LM2585-ADJ

| Symbol | Parameters | Conditions | Typical | Min | Max | Units |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| SYSTEM PARAMETERS Test Circuit of Figure 3 (Note 4) |  |  |  |  |  |  |
| V OUT | Output Voltage | $\begin{aligned} & \mathrm{V}_{\mathrm{IN}}=4 \mathrm{~V} \text { to } 10 \mathrm{~V} \\ & \mathrm{I}_{\text {LOAD }}=0.2 \mathrm{~A} \text { to } 0.8 \mathrm{~A} \end{aligned}$ | 12.0 | 11.52/11.40 | 12.48/12.60 | V |
| $\Delta \mathrm{V}_{\text {OUT }} /$ $\Delta \mathrm{V}_{\mathrm{IN}}$ | Line Regulation | $\begin{aligned} & \mathrm{V}_{\text {IN }}=4 \mathrm{~V} \text { to } 10 \mathrm{~V} \\ & \mathrm{I}_{\text {LOAD }}=0.2 \mathrm{~A} \end{aligned}$ | 20 |  | 100/200 | mV |
| $\begin{aligned} & \Delta V_{\text {OUT }} / \\ & \Delta I_{\text {LOAD }} \end{aligned}$ | Load Regulation | $\begin{aligned} & \mathrm{V}_{I N}=10 \mathrm{~V} \\ & \mathrm{I}_{\text {LOAD }}=0.2 \mathrm{~A} \text { to } 0.8 \mathrm{~A} \end{aligned}$ | 20 |  | 100/200 | mV |
| $\eta$ | Efficiency | $\mathrm{V}_{\mathrm{IN}}=10 \mathrm{~V}, \mathrm{ILOAD}=0.6 \mathrm{~A}$ | 93 |  |  | \% |

## Electrical Characteristics

Specifications with standard type face are for $T_{J}=25^{\circ} \mathrm{C}$, and those in bold type face apply over full Operating Temperature Range. Unless otherwise specified, $\mathrm{V}_{\mathrm{IN}}=5 \mathrm{~V}$. (Continued)
LM2585-ADJ (Continued)

| Symbol | Parameters | Conditions | Typical | Min | Max | Units |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| UNIQUE DEVICE PARAMETERS (Note 5) |  |  |  |  |  |  |
| $V_{\text {REF }}$ | Output Reference Voltage | Measured at Feedback Pin $\mathrm{V}_{\mathrm{COMP}}=1.0 \mathrm{~V}$ | 1.230 | 1.208/1.205 | 1.252/1.255 | V |
| $\Delta \mathrm{V}_{\text {REF }}$ | Reference Voltage Line Regulation | $\mathrm{V}_{\mathrm{IN}}=4 \mathrm{~V}$ to 40 V | 1.5 |  |  | mV |
| $\mathrm{G}_{\mathrm{M}}$ | Error Amp <br> Transconductance | $\begin{aligned} & \mathrm{I}_{\mathrm{COMP}}=-30 \mu \mathrm{~A} \text { to }+30 \mu \mathrm{~A} \\ & \mathrm{~V}_{\mathrm{COMP}}=1.0 \mathrm{~V} \end{aligned}$ | 3.200 | 1.800 | 6.000 | mmho |
| Avol | Error Amp <br> Voltage Gain | $\begin{aligned} & \mathrm{V}_{\mathrm{COMP}}=0.5 \mathrm{~V} \text { to } 1.6 \mathrm{~V} \\ & \left.\mathrm{R}_{\mathrm{COMP}}=1.0 \mathrm{M} \Omega \text { (Note } 6\right) \end{aligned}$ | 670 | 400/200 |  | V/V |
| $\mathrm{I}_{\mathrm{B}}$ | Error Amp Input Bias Current | $\mathrm{V}_{\text {COMP }}=1.0 \mathrm{~V}$ | 125 |  | 425/600 | nA |

COMMON DEVICE PARAMETERS for all versions (Note 5)

| Symbol | Parameters | Conditions | Typical | Min | Max | Units |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| Is | Input Supply Current | (Switch Off) (Note 8) | 11 |  | 15.5/16.5 | mA |
|  |  | $\mathrm{I}_{\text {SWITCH }}=1.8 \mathrm{~A}$ | 50 |  | 100/115 | mA |
| Vuv | Input Supply Undervoltage Lockout | $\mathrm{R}_{\text {LOAD }}=100 \Omega$ | 3.30 | 3.05 | 3.75 | V |
| $\mathrm{f}_{\mathrm{O}}$ | Oscillator Frequency | Measured at Switch Pin $\begin{aligned} & R_{\text {LOAD }}=100 \Omega \\ & \mathrm{~V}_{\mathrm{COMP}}=1.0 \mathrm{~V} \end{aligned}$ | 100 | 85/75 | 115/125 | kHz |
| $\mathrm{f}_{\text {SC }}$ | Short-Circuit <br> Frequency | Measured at Switch Pin <br> $R_{\text {LOAD }}=100 \Omega$ <br> $\mathrm{V}_{\text {FEEDBACK }}=1.15 \mathrm{~V}$ | 25 |  |  | kHz |
| $\mathrm{V}_{\text {EAO }}$ | Error Amplifier Output Swing | Upper Limit (Note 7) | 2.8 | 2.6/2.4 |  | V |
|  |  | Lower Limit (Note 8) | 0.25 |  | 0.40/0.55 | V |
| $\mathrm{I}_{\text {EAO }}$ | Error Amp <br> Output Current <br> (Source or Sink) | (Note 9) | 165 | 110/70 | 260/320 | $\mu \mathrm{A}$ |
| Iss | Soft Start Current | $\begin{aligned} & \mathrm{V}_{\text {FEEDBACK }}=0.92 \mathrm{~V} \\ & \mathrm{~V}_{\text {COMP }}=1.0 \mathrm{~V} \end{aligned}$ | 11.0 | 8.0/7.0 | 17.0/19.0 | $\mu \mathrm{A}$ |
| D | Maximum Duty Cycle | $\begin{aligned} & \mathrm{R}_{\mathrm{LOAD}}=100 \Omega \\ & \text { (Note 7) } \end{aligned}$ | 98 | 93/90 |  | \% |
| $I_{L}$ | Switch Leakage Current | Switch Off $\mathrm{V}_{\text {SWITCH }}=60 \mathrm{~V}$ | 15 |  | 300/600 | $\mu \mathrm{A}$ |
| $\mathrm{V}_{\text {SUS }}$ | Switch Sustaining Voltage | $\mathrm{dV} / \mathrm{dT}=1.5 \mathrm{~V} / \mathrm{ns}$ |  | 65 |  | V |
| $\mathrm{V}_{\text {SAT }}$ | Switch Saturation Voltage | $\mathrm{I}_{\text {SWITCH }}=3.0 \mathrm{~A}$ | 0.45 |  | 0.65/0.9 | V |
| $\mathrm{I}_{\mathrm{CL}}$ | NPN Switch Current Limit |  | 4.0 | 3.0 | 7.0 | A |

## Electrical Characteristics

Specifications with standard type face are for $\mathrm{T}_{J}=25^{\circ} \mathrm{C}$, and those in bold type face apply over full Operating Temperature Range. Unless otherwise specified, $\mathrm{V}_{\mathrm{IN}}=5 \mathrm{~V}$. (Continued)
COMMON DEVICE PARAMETERS (Note 4) (Continued)

| Symbol | Parameters | Conditions | Typical | Min | Max | Units |
| :--- | :---: | :---: | :---: | :---: | :---: | :---: |
| $\theta_{\text {JA }}$ | Thermal Resistance | T Package, Junction to Ambient (Note 10) | 65 |  |  |  |
| $\theta_{\text {JA }}$ |  | T Package, Junction to Ambient (Note 11) | 45 |  |  |  |
| $\theta_{\text {JC }}$ |  | T Package, Junction to Case | 2 |  |  |  |
| $\theta_{\text {JA }}$ |  | S Package, Junction to Ambient (Note 12) | 56 |  |  | ${ }^{\circ} \mathrm{C} / \mathrm{W}$ |
| $\theta_{\text {JA }}$ |  | S Package, Junction to Ambient (Note 13) | 35 |  |  |  |
| $\theta_{\text {JA }}$ |  | S Package, Junction to Ambient (Note 14) | 26 |  |  |  |
| $\theta_{\text {JC }}$ |  | S Package, Junction to Case | 2 |  |  |  |

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating ratings indicate conditions the device is intended to be functional, but device parameter specifications may not be guaranteed under these conditions. For guaranteed specifications and test conditions, see the Electrical Characteristics.
Note 2: Note that switch current and output current are not identical in a step-up regulator. Output current cannot be internally limited when the LM2585 is used as a step-up regulator. To prevent damage to the switch, the output current must be externally limited to 3A. However, output current is internally limited when the LM2585 is used as a flyback regulator (see the Application Hints section for more information).
Note 3: The junction temperature of the device ( $\left.T_{J}\right)$ is a function of the ambient temperature ( $T_{A}$ ), the junction-to-ambient thermal resistance $\left(\theta_{\mathrm{JA}}\right)$, and the power dissipation of the device ( $P_{D}$ ). A thermal shutdown will occur if the temperature exceeds the maximum junction temperature of the device: $P_{D} \times \theta_{\mathrm{JA}}+T_{A(M A X)} \geq$ $T_{J(M A X)}$. For a safe thermal design, check that the maximum power dissipated by the device is less than: $\left.P_{D} \leq\left[T_{J(M A X)}-T_{A(M A X)}\right)\right] / \theta_{J A}$. When calculating the maximum allowable power dissipation, derate the maximum junction temperature-this ensures a margin of safety in the thermal design.
Note 4: External components such as the diode, inductor, input and output capacitors can affect switching regulator performance. When the LM2585 is used as shown in Figures 2 and 3, system performance will be as specified by the system parameters.
Note 5: All room temperature limits are $100 \%$ production tested, and all limits at temperature extremes are guaranteed via correlation using standard Statistical Quality Control (SQC) methods.
Note 6: A $1.0 \mathrm{M} \Omega$ resistor is connected to the compensation pin (which is the error amplifier output) to ensure accuracy in measuring AvoL-
Note 7: To measure this parameter, the feedback voltage is set to a low value, depending on the output version of the device, to force the error amplifier output high. Adj: $\mathrm{V}_{\mathrm{FB}}=1.05 \mathrm{~V} ; 3.3 \mathrm{~V}: \mathrm{V}_{\mathrm{FB}}=2.81 \mathrm{~V} ; 5.0 \mathrm{~V}: \mathrm{V}_{\mathrm{FB}}=4.25 \mathrm{~V} ; 12 \mathrm{~V}: \mathrm{V}_{\mathrm{FB}}=10.20 \mathrm{~V}$.
Note 8: To measure this parameter, the feedback voltage is set to a high value, depending on the output version of the device, to force the error amplifier output low. Adj: $\mathrm{V}_{\mathrm{FB}}=1.41 \mathrm{~V} ; 3.3 \mathrm{~V}: \mathrm{V}_{\mathrm{FB}}=3.80 \mathrm{~V} ; 5.0 \mathrm{~V}: \mathrm{V}_{\mathrm{FB}}=5.75 \mathrm{~V} ; 12 \mathrm{~V}: \mathrm{V}_{\mathrm{FB}}=13.80 \mathrm{~V}$.
Note 9: To measure the worst-case error amplifier output current, the LM2585 is tested with the feedback voltage set to its low value (specified in Note 7) and at its high value (specified in Note 8).
Note 10: Junction to ambient thermal resistance (no external heat sink) for the 5 lead TO-220 package mounted vertically, with $1 / 2$ inch leads in a socket, or on a PC board with minimum copper area.
Note 11: Junction to ambient thermal resistance (no external heat sink) for the 5 lead TO-220 package mounted vertically, with $1 / 2$ inch leads soldered to a PC board containing approximately 4 square inches of (10z.) copper area surrounding the leads.
Note 12: Junction to ambient thermal resistance for the 5 lead TO-263 mounted horizontally against a PC board area of 0.136 square inches (the same size as the TO-263 package) of 1 oz . ( 0.0014 in. thick) copper.
Note 13: Junction to ambient thermal resistance for the 5 lead TO-263 mounted horizontally against a PC board area of 0.4896 square inches ( 3.6 times the area of the TO-263 package) of 1 oz. ( 0.0014 in. thick) copper.
Note 14: Junction to ambient thermal resistance for the 5 lead TO-263 mounted horizontally against a PC board copper area of 1.0064 square inches ( 7.4 times the area of the TO-263 package) of 1 oz . ( 0.0014 in. thick) copper. Additional copper area will reduce thermal resistance further. See the thermal model in Switchers Made Simple ${ }^{\circledR}$ software.

Typical Performance Characteristics


TL/H/12515-2


TL/H/12515-5
Switch Saturation Voltage vs Temperature




TL/H/12515-3


Switch Transconductance vs Temperature


TL/H/12515-9

## Error Amp Voltage

Gain vs Temperature



Feedback Pin Bias Current vs Temperature


TL/H/12515-7
Oscillator Frequency vs Temperature


TL/H/12515-10
Short Circuit Frequency vs Temperature


## Connection Diagrams



## Block Diagram




## Flyback Regulator Operation

The LM2585 is ideally suited for use in the flyback regulator topology. The flyback regulator can produce a single output voltage, such as the one shown in Figure 4, or multiple output voltages. In Figure 4, the flyback regulator generates an output voltage that is inside the range of the input voltage. This feature is unique to flyback regulators and cannot be duplicated with buck or boost regulators.
The operation of a flyback regulator is as follows (refer to Figure 4): when the switch is on, current flows through the primary winding of the transformer, T1, storing energy in the magnetic field of the transformer. Note that the primary and secondary windings are out of phase, so no current flows through the secondary when current flows through the primary. When the switch turns off, the magnetic field col-
lapses, reversing the voltage polarity of the primary and secondary windings. Now rectifier D1 is forward biased and current flows through it, releasing the energy stored in the transformer. This produces voltage at the output.
The output voltage is controlled by modulating the peak switch current. This is done by feeding back a portion of the output voltage to the error amp, which amplifies the difference between the feedback voltage and a 1.230 V reference. The error amp output voltage is compared to a ramp voltage proportional to the switch current (i.e., inductor current during the switch on time). The comparator terminates the switch on time when the two voltages are equal, thereby controlling the peak switch current to maintain a constant output voltage.


TL/H/12515-21
As shown in Figure 4, the LM2585 can be used as a flyback regulator by using a minimum number of external components. The switching waveforms of this regulator are shown in Figure 5. Typical Performance Characteristics observed during the operation of this circuit are shown in Figure 6.

FIGURE 4. 12V Flyback Regulator Design Example

## Typical Performance Characteristics



A: Switch Voltage, $20 \mathrm{~V} / \mathrm{div}$
B: Switch Current, 2 A/div
C: Output Rectifier Current, $2 \mathrm{~A} / \mathrm{div}$ D: Output Ripple Voltage, $50 \mathrm{mV} /$ div AC-Coupled
Horizontal: $2 \mu \mathrm{~s} / \mathrm{div}$


## Typical Flyback Regulator Applications

Figures 7 through 12 show six typical flyback applications, varying from single output to triple output. Each drawing contains the part number(s) and manufacturer(s) for every component except the transformer. For the transformer part numbers and manufacturers names, see the table in

Figure 13. For applications with different output voltagesrequiring the LM2585-ADJ—or different output configurations that do not match the standard configurations, refer to the Switchers Made Simple ${ }^{\circledR}$ software.


TL/H/12515-24
FIGURE 7. Single-Output Flyback Regulator


TL/H/12515-25

## Typical Flyback Regulator Applications (Continued)



FIGURE 9. Single-Output Flyback Regulator


FIGURE 10. Dual-Output Flyback Regulator

## Typical Flyback Regulator Applications (Continued)



FIGURE 11. Dual-Output Flyback Regulator


FIGURE 12. Triple-Output Flyback Regulator


FIGURE 14. Transformer Manufacturer Guide



## Typical Flyback Regulator Applications (Continued)



## Step-Up (Boost) Regulator Operation

Figure 30 shows the LM2585 used as a step-up (boost) regulator. This is a switching regulator that produces an output voltage greater than the input supply voltage.
A brief explanation of how the LM2585 Boost Regulator works is as follows (refer to Figure 30). When the NPN switch turns on, the inductor current ramps up at the rate of $\mathrm{V}_{\mathrm{IN}} / \mathrm{L}$, storing energy in the inductor. When the switch turns
off, the lower end of the inductor flies above $\mathrm{V}_{\mathrm{IN}}$, discharging its current through diode (D) into the output capacitor (COUT) at a rate of $\left(\mathrm{V}_{\text {OUT }}-\mathrm{V}_{\mathrm{IN}}\right) / \mathrm{L}$. Thus, energy stored in the inductor during the switch on time is transferred to the output during the switch off time. The output voltage is controlled by adjusting the peak switch current, as described in the flyback regulator section.


TL/H/12515-48
By adding a small number of external components (as shown in Figure 30), the LM2585 can be used to produce a regulated output voltage that is greater than the applied input voltage. The switching waveforms observed during the operation of this circuit are shown in Figure 31. Typical performance of this regulator is shown in Figure 32.

FIGURE 30. 12V Boost Regulator

## Typical Performance Characteristics



FIGURE 31. Switching Waveforms


FIGURE 32. V

## Typical Boost Regulator Applications

Figures 33 and 35 through 37 show four typical boost appli-cations)-one fixed and three using the adjustable version of the LM2585. Each drawing contains the part number(s) and manufacturer(s) for every component. For the fixed 12 V
output application, the part numbers and manufacturers' names for the inductor are listed in a table in Figure 34. For applications with different output voltages, refer to the Switchers Made Simple ${ }^{\circledR}$ software.


TL/H/12515-51
FIGURE 33. $+\mathbf{5 V}$ to $+\mathbf{1 2 V}$ Boost Regulator

Figure 34 contains a table of standard inductors, by part number and corresponding manufacturer, for the fixed output regulator of Figure 33.

| Coilcraft $^{1}$ | Pulse $^{2}$ | Renco $^{3}$ | Schott $^{4}$ | Schott $^{\mathbf{4}}$ (Surface Mount) |
| :---: | :---: | :---: | :---: | :---: |
| D03316-153 | PE-53898 | RL-5471-7 | 67146510 | 67146540 |

Note 1: Coilcraft Inc.,
1102 Silver Lake Road, Cary, IL 60013
Note 2: Pulse Engineering Inc.,
12220 World Trade Drive, San Diego, CA 92128
Note 3: Renco Electronics Inc.,
60 Jeffryn Blvd. East, Deer Park, NY 11729
Note 4: Schott Corp.,
1000 Parkers Lane Road, Wayzata, MN 55391

Phone: (800) 322-2645 Fax: (708) 639-1469
Phone: (619) 674-8100
Fax: (619) 674-8262
Phone: (800) 645-5828 Fax: (516) 586-5562
Phone: (612) 475-1173
Fax: (612) 475-1786

FIGURE 34. Inductor Selection Table

## Typical Boost Regulator Applications (Continued)



FIGURE 35. +12 V to +24 V Boost Regulator


FIGURE 36. +24 V to +36 V Boost Regulator


FIGURE 37. +24 V to +48 V Boost Regulator
*The LM2585 will require a heat sink in these applications. The size of the heat sink will depend on the maximum ambient temperature. To calculate the thermal resistance of the IC and the size of the heat sink needed, see the "Heat Sink/Thermal Considerations" section in the Application Hints.

## Application Hints



TL/H/12515-55
FIGURE 38. Boost Regulator

## PROGRAMMING OUTPUT VOLTAGE

(SELECTING $\mathrm{R}_{1}$ AND $\mathrm{R}_{2}$ )
Referring to the adjustable regulator in Figure 38, the output voltage is programmed by the resistors $R_{1}$ and $R_{2}$ by the following formula:

$$
V_{\text {OUT }}=V_{\text {REF }}\left(1+R_{1} / R_{2}\right) \quad \text { where } V_{\text {REF }}=1.23 V
$$

Resistors $R_{1}$ and $R_{2}$ divide the output voltage down so that it can be compared with the 1.23 V internal reference. With $R_{2}$ between $1 k$ and $5 k, R_{1}$ is:

$$
R_{1}=R_{2}\left(V_{\text {OUT }} / V_{\text {REF }}-1\right) \quad \text { where } V_{R E F}=1.23 V
$$

For best temperature coefficient and stability with time, use $1 \%$ metal film resistors.

## SHORT CIRCUIT CONDITION

Due to the inherent nature of boost regulators, when the output is shorted (see Figure 38), current flows directly from the input, through the inductor and the diode, to the output, bypassing the switch. The current limit of the switch does not limit the output current for the entire circuit. To protect the load and prevent damage to the switch, the current must be externally limited, either by the input supply or at the out-
put with an external current limit circuit. The external limit should be set to the maximum switch current of the device, which is 3 A .
In a flyback regulator application (Figure 39), using the standard transformers, the LM2585 will survive a short circuit to the main output. When the output voltage drops to $80 \%$ of its nominal value, the frequency will drop to 25 kHz . With a lower frequency, off times are larger. With the longer off times, the transformer can release all of its stored energy before the switch turns back on. Hence, the switch turns on initially with zero current at its collector. In this condition, the switch current limit will limit the peak current, saving the device.

## FLYBACK REGULATOR INPUT CAPACITORS

A flyback regulator draws discontinuous pulses of current from the input supply. Therefore, there are two input capacitors needed in a flyback regulator; one for energy storage and one for filtering (see Figure 39). Both are required due to the inherent operation of a flyback regulator. To keep a stable or constant voltage supply to the LM2585, a stor-


TL/H/12515-56
FIGURE 39. Flyback Regulator

## Application Hints (Continued)

age capacitor $(\geq 100 \mu \mathrm{~F})$ is required. If the input source is a rectified DC supply and/or the application has a wide temperature range, the required rms current rating of the capacitor might be very large. This means a larger value of capacitance or a higher voltage rating will be needed of the input capacitor. The storage capacitor will also attenuate noise which may interfere with other circuits connected to the same input supply voltage.
In addition, a small bypass capacitor is required due to the noise generated by the input current pulses. To eliminate the noise, insert a $1.0 \mu \mathrm{~F}$ ceramic capacitor between $\mathrm{V}_{\mathrm{IN}}$ and ground as close as possible to the device.

## SWITCH VOLTAGE LIMITS

In a flyback regulator, the maximum steady-state voltage appearing at the switch, when it is off, is set by the transformer turns ratio, N , the output voltage, $\mathrm{V}_{\text {OUT }}$, and the maximum input voltage, $\mathrm{V}_{\mathrm{IN}}($ Max):

$$
\mathrm{V}_{\mathrm{SW}(\mathrm{OFF})}=\mathrm{V}_{\mathrm{IN}}(\mathrm{Max})+\left(\mathrm{V}_{\mathrm{OUT}}+\mathrm{V}_{\mathrm{F}}\right) / \mathrm{N}
$$

where $V_{F}$ is the forward biased voltage of the output diode, and is 0.5 V for Schottky diodes and 0.8 V for ultra-fast recovery diodes (typically). In certain circuits, there exists a voltage spike, $\mathrm{V}_{\mathrm{LL}}$, superimposed on top of the steady-state voltage (see Figure 5, waveform A). Usually, this voltage spike is caused by the transformer leakage inductance and/ or the output rectifier recovery time. To "clamp" the voltage at the switch from exceeding its maximum value, a transient suppressor in series with a diode is inserted across the transformer primary (as shown in the circuit on the front page and other flyback regulator circuits throughout the datasheet). The schematic in Figure 39 shows another method of clamping the switch voltage. A single voltage transient suppressor (the SA51A) is inserted at the switch pin. This method clamps the total voltage across the switch, not just the voltage across the primary.
If poor circuit layout techniques are used (see the "Circuit Layout Guideline" section), negative voltage transients may appear on the Switch pin (pin 4). Applying a negative voltage (with respect to the IC's ground) to any monolithic IC pin causes erratic and unpredictable operation of that IC. This holds true for the LM2585 IC as well. When used in a flyback regulator, the voltage at the Switch pin (pin 4) can go negative when the switch turns on. The "ringing" voltage at the switch pin is caused by the output diode capacitance and the transformer leakage inductance forming a resonant circuit at the secondary(ies). The resonant circuit generates the "ringing" voltage, which gets reflected back through the transformer to the switch pin. There are two common methods to avoid this problem. One is to add an RC snubber around the output rectifier(s), as in Figure 39. The values of the resistor and the capacitor must be chosen so that the voltage at the Switch pin does not drop below -0.4 V . The resistor may range in value between $10 \Omega$ and $1 \mathrm{k} \Omega$, and the capacitor will vary from $0.001 \mu \mathrm{~F}$ to $0.1 \mu \mathrm{~F}$. Adding a snubber will (slightly) reduce the efficiency of the overall circuit. The other method to reduce or eliminate the "ringing" is to insert a Schottky diode clamp between pins 4 and 3 (ground), also shown in Figure 39. This prevents the voltage at pin 4 from dropping below -0.4 V . The reverse voltage rating of the diode must be greater than the switch off voltage.


FIGURE 40. Input Line Filter

## OUTPUT VOLTAGE LIMITATIONS

The maximum output voltage of a boost regulator is the maximum switch voltage minus a diode drop. In a flyback regulator, the maximum output voltage is determined by the turns ratio, N , and the duty cycle, D , by the equation:

$$
V_{\text {OUT }} \approx N \times V_{\text {IN }} \times D /(1-D)
$$

The duty cycle of a flyback regulator is determined by the following equation:

$$
\mathrm{D}=\frac{\mathrm{V}_{\mathrm{OUT}}+\mathrm{V}_{\mathrm{F}}}{\mathrm{~N}\left(\mathrm{~V}_{\text {IN }}-\mathrm{V}_{\mathrm{SAT}}\right)+\mathrm{V}_{\text {OUT }}+\mathrm{V}_{\mathrm{F}}} \approx \frac{\mathrm{~V}_{\mathrm{OUT}}}{\mathrm{~N}\left(\mathrm{~V}_{\mathrm{IN}}\right)+\mathrm{V}_{\mathrm{OUT}}}
$$

Theoretically, the maximum output voltage can be as large as desired-just keep increasing the turns ratio of the transformer. However, there exists some physical limitations that prevent the turns ratio, and thus the output voltage, from increasing to infinity. The physical limitations are capacitances and inductances in the LM2585 switch, the output diode(s), and the transformer-such as reverse recovery time of the output diode (mentioned above).

## NOISY INPUT LINE CONDITION

A small, low-pass RC filter should be used at the input pin of the LM2585 if the input voltage has an unusual large amount of transient noise, such as with an input switch that bounces. The circuit in Figure 40 demonstrates the layout of the filter, with the capacitor placed from the input pin to ground and the resistor placed between the input supply and the input pin. Note that the values of $\mathrm{R}_{I N}$ and $\mathrm{C}_{I N}$ shown in the schematic are good enough for most applications, but some readjusting might be required for a particular application. If efficiency is a major concern, replace the resistor with a small inductor (say $10 \mu \mathrm{H}$ and rated at 100 mA ).

## STABILITY

All current-mode controlled regulators can suffer from an instability, known as subharmonic oscillation, if they operate with a duty cycle above $50 \%$. To eliminate subharmonic oscillations, a minimum value of inductance is required to ensure stability for all boost and flyback regulators. The minimum inductance is given by:
$\mathrm{L}(\mathrm{Min})=\frac{2.92\left[\left(\mathrm{~V}_{\text {IN }}(\mathrm{Min})-\mathrm{V}_{\text {SAT }}\right) \times(2 \mathrm{D}(\mathrm{Max})-1)\right]}{1-\mathrm{D}(\mathrm{Max})}(\mu \mathrm{H})$
where $\mathrm{V}_{\text {SAT }}$ is the switch saturation voltage and can be found in the Characteristic Curves.

## Application Hints (Continued)



TL/H/12515-58
FIGURE 41. Circuit Board Layout

## CIRCUIT LAYOUT GUIDELINES

As in any switching regulator, layout is very important. Rapidly switching currents associated with wiring inductance generate voltage transients which can cause problems. For minimal inductance and ground loops, keep the length of the leads and traces as short as possible. Use single point grounding or ground plane construction for best results. Separate the signal grounds from the power grounds (as indicated in Figure 41). When using the Adjustable version, physically locate the programming resistors as near the regulator IC as possible, to keep the sensitive feedback wiring short.

## HEAT SINK/THERMAL CONSIDERATIONS

In many cases, no heat sink is required to keep the LM2585 junction temperature within the allowed operating range. For each application, to determine whether or not a heat sink will be required, the following must be identified:

1) Maximum ambient temperature (in the application).
2) Maximum regulator power dissipation (in the application).
3) Maximum allowed junction temperature $\left(125^{\circ} \mathrm{C}\right.$ for the LM2585). For a safe, conservative design, a temperature approximately $15^{\circ} \mathrm{C}$ cooler than the maximum junction temperature should be selected $\left(110^{\circ} \mathrm{C}\right)$.
4) LM2585 package thermal resistances $\theta_{\mathrm{JA}}$ and $\theta_{\mathrm{JC}}$ (given in the Electrical Characteristics).
Total power dissipated ( $\mathrm{P}_{\mathrm{D}}$ ) by the LM2585 can be estimated as follows:
Boost:
$P_{D}=0.15 \Omega \times\left(\frac{I_{\text {LOAD }}}{1-D}\right)^{2} \times D+\frac{I_{\text {LOAD }}}{50 \times(1-D)} \times D \times V_{I N}$
Flyback:

$$
\begin{aligned}
\mathrm{P}_{\mathrm{D}}= & 0.15 \Omega \times\left(\frac{\mathrm{N} \times \Sigma \mathrm{I}_{\mathrm{LOAD}}}{1-\mathrm{D}}\right)^{2} \times \mathrm{D} \\
& +\frac{\mathrm{N} \times \Sigma \mathrm{I}_{\mathrm{LOAD}}}{50 \times(1-\mathrm{D})} \times \mathrm{D} \times \mathrm{V}_{\mathrm{IN}}
\end{aligned}
$$

$\mathrm{V}_{\text {IN }}$ is the minimum input voltage, $\mathrm{V}_{\text {OUT }}$ is the output voltage, N is the transformer turns ratio, D is the duty cycle, and $I_{\text {LOAD }}$ is the maximum load current (and $\Sigma l_{\text {LOAD }}$ is the sum of the maximum load currents for multiple-output flyback regulators). The duty cycle is given by:
Boost:

$$
\mathrm{D}=\frac{\mathrm{V}_{\mathrm{OUT}}+\mathrm{V}_{\mathrm{F}}-\mathrm{V}_{\text {IN }}}{\mathrm{V}_{\text {OUT }}+\mathrm{V}_{\mathrm{F}}-\mathrm{V}_{\mathrm{SAT}}} \approx \frac{\mathrm{~V}_{\text {OUT }}-\mathrm{V}_{\text {IN }}}{V_{\text {OUT }}}
$$

Flyback:

$$
\mathrm{D}=\frac{\mathrm{V}_{\mathrm{OUT}}+\mathrm{V}_{\mathrm{F}}}{\mathrm{~N}\left(\mathrm{~V}_{\text {IN }}-\mathrm{V}_{\mathrm{SAT}}\right)+\mathrm{V}_{\mathrm{OUT}}+\mathrm{V}_{\mathrm{F}}} \approx \frac{\mathrm{~V}_{\mathrm{OUT}}}{\mathrm{~N}\left(\mathrm{~V}_{\text {IN }}\right)+\mathrm{V}_{\mathrm{OUT}}}
$$

where $\mathrm{V}_{\mathrm{F}}$ is the forward biased voltage of the diode and is typically 0.5 V for Schottky diodes and 0.8 V for fast recovery diodes. $\mathrm{V}_{\text {SAT }}$ is the switch saturation voltage and can be found in the Characteristic Curves.
When no heat sink is used, the junction temperature rise is:

$$
\Delta T_{J}=P_{D} \times \theta_{J A}
$$

Adding the junction temperature rise to the maximum ambient temperature gives the actual operating junction temperature:

$$
T_{J}=\Delta T_{J}+T_{A} .
$$

If the operating junction temperature exceeds the maximum junction temperatue in item 3 above, then a heat sink is required. When using a heat sink, the junction temperature rise can be determined by the following:

$$
\Delta T_{J}=P_{\mathrm{D}} \times\left(\theta_{\mathrm{JC}}+\theta_{\text {Interface }}+\theta_{\text {Heat Sink }}\right)
$$

Again, the operating junction temperature will be:

$$
\mathrm{T}_{\mathrm{J}}=\Delta \mathrm{T}_{\mathrm{J}}+\mathrm{T}_{\mathrm{A}}
$$

## Application Hints (Continued)

As before, if the maximum junction temperature is exceeded, a larger heat sink is required (one that has a lower thermal resistance).
Included in the Switchers Made Simple ${ }^{\circledR}$ design software is a more precise (non-linear) thermal model that can be used to determine junction temperature with different inputoutput parameters or different component values. It can also calculate the heat sink thermal resistance required to maintain the regulator junction temperature below the maximum operating temperature.
To further simplify the flyback regulator design procedure, National Semiconductor is making available computer design software to be used with the Simple Switcher ${ }^{\circledR}$ line of switching regulators. Switchers Made Simple ${ }^{\circledR}$ is available on a $31 / 2^{\prime \prime}$ diskette for IBM compatible computers from a National Semiconductor sales office in your area or the National Semiconductor Customer Response Center (1-800-272-9959).

## European Magnetic Vendor Contacts

Please contact the following addresses for details of local distributors or representatives:

## Coilcraft

21 Napier Place Wardpark North
Cumbernauld, Scotland G68 0LL
Phone: +44 1236730595
Fax: +441236730627

## Pulse Engineering

Dunmore Road
Tuam
Co. Galway, Ireland
Phone: + 3539324107
Fax: +3539324459

Physical Dimensions inches (millimeters) unless otherwise noted


Physical Dimensions inches (millimeters) unless otherwise noted (Continued)


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| :---: | :---: | :---: | :---: |

## Ordering Information

| Package Type | NSC Package <br> Drawing | Order Number |
| :--- | :---: | :--- |
| 7-Lead TO-220 Bent, Staggered Leads | TA07B | LM2586T-3.3, LM2586T-5.0, LM2586T-12, LM2586T-ADJ |
| 7-Lead TO-263 | TS7B | LM2586S-3.3, LM2586S-5.0, LM2586S-12, LM2586S-ADJ |
| 7-Lead TO-263 Tape and Reel | TS7B | LM2586SX-3.3, LM2586SX-5.0, LM2586SX-12, LM2586SX-ADJ |
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Absolute Maximum Ratings (Note 1) If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

| Input Voltage | $-0.4 \mathrm{~V} \leq \mathrm{V}_{\text {IN }} \leq 45 \mathrm{~V}$ |
| :--- | ---: |
| Switch Voltage | $-0.4 \mathrm{~V} \leq \mathrm{V}_{\text {SW }} \leq 65 \mathrm{~V}$ |
| Switch Current (Note 2) | Internally Limited |
| Compensation Pin Voltage | $-0.4 \mathrm{~V} \leq \mathrm{V}_{\text {COMP }} \leq 2.4 \mathrm{~V}$ |
| Feedback Pin Voltage | $-0.4 \mathrm{~V} \leq \mathrm{V}_{\mathrm{FB}} \leq 2 \mathrm{~V}_{\text {OUT }}$ |
| $\overline{\text { ON }}$ OFF Pin Voltage | $-0.4 \mathrm{~V} \leq \mathrm{V}_{\text {SH }} \leq 6 \mathrm{~V}$ |
| Sync Pin Voltage | $-0.4 \mathrm{~V} \leq \mathrm{V}_{\text {SYNC }} \leq 2 \mathrm{~V}$ |


| Power Dissipation (Note 3) | Internally Limited |
| :--- | ---: |
| Storage Temperature Range | $-65^{\circ} \mathrm{C}$ to $+150^{\circ} \mathrm{C}$ |
| Lead Temperature (Soldering, 10 sec.) | $260^{\circ} \mathrm{C}$ |
| Maximum Junction Temperature (Note 3) | $150^{\circ} \mathrm{C}$ |
| Minimum ESD Rating |  |
| $\quad(\mathrm{C}=100 \mathrm{pF}, \mathrm{R}=1.5 \mathrm{k} \Omega)$ | 2 kV |

## Operating Ratings

| Supply Voltage | $4 \mathrm{~V} \leq \mathrm{V}_{\mathrm{IN}} \leq 40 \mathrm{~V}$ |
| :--- | ---: |
| Output Switch Voltage | $0 \mathrm{~V} \leq \mathrm{V}_{\mathrm{SW}} \leq 60 \mathrm{~V}$ |
| Output Switch Current | $\mathrm{I}_{\mathrm{SW}} \leq 3.0 \mathrm{~A}$ |
| Junction Temp. Range | $-40^{\circ} \mathrm{C} \leq \mathrm{TJ}_{\mathrm{J}} \leq+125^{\circ} \mathrm{C}$ |

## Electrical Characteristics

Specifications with standard type face are for $T_{J}=25^{\circ} \mathrm{C}$, and those in bold type face apply over full Operating Temperature Range. Unless otherwise specified, $\mathrm{V}_{\mathrm{IN}}=5 \mathrm{~V}$.
LM2586-3.3

| Symbol | Parameters | Conditions | Typical | Min | Max | Units |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| SYSTEM PARAMETERS Test Circuit of Figure 1 (Note 4) |  |  |  |  |  |  |
| V ${ }_{\text {OUT }}$ | Output Voltage | $\begin{aligned} & \mathrm{V}_{\mathrm{IN}}=4 \mathrm{~V} \text { to } 12 \mathrm{~V} \\ & \mathrm{I}_{\text {LOAD }}=0.3 \text { to } 1.2 \mathrm{~A} \end{aligned}$ | 3.3 | 3.17/3.14 | 3.43/3.46 | V |
| $\Delta \mathrm{V}_{\text {OUT }} /$ <br> $\Delta \mathrm{V}_{\mathrm{IN}}$ | Line Regulation | $\begin{aligned} & \mathrm{V}_{I N}=4 \mathrm{~V} \text { to } 12 \mathrm{~V} \\ & \mathrm{I}_{\text {LOAD }}=0.3 \mathrm{~A} \end{aligned}$ | 20 |  | 50/100 | mV |
| $\Delta V_{\text {OUT }} /$ <br> $\Delta I_{\text {LOAD }}$ | Load Regulation | $\begin{aligned} & \mathrm{V}_{\mathrm{IN}}=12 \mathrm{~V} \\ & \mathrm{I}_{\text {LOAD }}=0.3 \mathrm{~A} \text { to } 1.2 \mathrm{~A} \end{aligned}$ | 20 |  | 50/100 | mV |
| $\eta$ | Efficiency | $\mathrm{V}_{\mathrm{IN}}=5 \mathrm{~V}, \mathrm{I}_{\text {LOAD }}=0.3 \mathrm{~A}$ | 76 |  |  | \% |
| UNIQUE DEVICE PARAMETERS (Note 5) |  |  |  |  |  |  |
| $V_{\text {REF }}$ | Output Reference Voltage | Measured at Feedback Pin $\mathrm{V}_{\mathrm{COMP}}=1.0 \mathrm{~V}$ | 3.3 | 3.242/3.234 | 3.358/3.366 | V |
| $\Delta \mathrm{V}_{\text {REF }}$ | Reference Voltage Line Regulation | $\mathrm{V}_{\text {IN }}=4 \mathrm{~V}$ to 40 V | 2.0 |  |  | mV |
| $\mathrm{G}_{\mathrm{M}}$ | Error Amp <br> Transconductance | $\begin{aligned} & \mathrm{I}_{\mathrm{COMP}}=-30 \mu \mathrm{~A} \text { to }+30 \mu \mathrm{~A} \\ & \mathrm{~V}_{\text {COMP }}=1.0 \mathrm{~V} \end{aligned}$ | 1.193 | 0.678 | 2.259 | mmho |
| Avol | Error Amp Voltage Gain | $\begin{aligned} & \mathrm{V}_{\mathrm{COMP}}=0.5 \mathrm{~V} \text { to } 1.6 \mathrm{~V} \\ & \mathrm{R}_{\mathrm{COMP}}=1.0 \mathrm{M} \Omega \text { (Note } 6 \text { ) } \end{aligned}$ | 260 | 151/75 |  | V/V |

LM2586-5.0

| Symbol | Parameters | Conditions | Typical | Min | Max | Units |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| SYSTEM PARAMETERS Test Circuit of Figure 1 (Note 4) |  |  |  |  |  |  |
| V OUT | Output Voltage | $\begin{aligned} & \mathrm{V}_{\mathrm{IN}}=4 \mathrm{~V} \text { to } 12 \mathrm{~V} \\ & \mathrm{I}_{\text {LOAD }}=0.3 \mathrm{~A} \text { to } 1.1 \mathrm{~A} \end{aligned}$ | 5.0 | 4.80/4.75 | 5.20/5.25 | V |
| $\Delta \mathrm{V}_{\text {OUT }} /$ <br> $\Delta \mathrm{V}_{\text {IN }}$ | Line Regulation | $\begin{aligned} & \mathrm{V}_{\text {IN }}=4 \mathrm{~V} \text { to } 12 \mathrm{~V} \\ & \mathrm{I}_{\text {LOAD }}=0.3 \mathrm{~A} \end{aligned}$ | 20 |  | 50/100 | mV |
| $\Delta \mathrm{V}_{\text {OUT }} /$ <br> $\Delta$ LIOAD | Load Regulation | $\begin{aligned} & \mathrm{V}_{\mathrm{IN}}=12 \mathrm{~V} \\ & \mathrm{I}_{\mathrm{LOAD}}=0.3 \mathrm{~A} \text { to } 1.1 \mathrm{~A} \end{aligned}$ | 20 |  | 50/100 | mV |
| $\eta$ | Efficiency | $\mathrm{V}_{\mathrm{IN}}=12 \mathrm{~V}, \mathrm{I}_{\mathrm{LOAD}}=0.6 \mathrm{~A}$ | 80 |  |  | \% |

## Electrical Characteristics

Specifications with standard type face are for $T_{J}=25^{\circ} \mathrm{C}$, and those in bold type face apply over full Operating Temperature Range. Unless otherwise specified, $\mathrm{V}_{\mathrm{IN}}=5 \mathrm{~V}$. (Continued)
LM2586-5.0 (Continued)

| Symbol | Parameters | Conditions | Typical | Min | Max | Units |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| UNIQUE DEVICE PARAMETERS (Note 5) |  |  |  |  |  |  |
| $\mathrm{V}_{\text {REF }}$ | Output Reference Voltage | Measured at Feedback Pin $\mathrm{V}_{\mathrm{COMP}}=1.0 \mathrm{~V}$ | 5.0 | 4.913/4.900 | 5.088/5.100 | V |
| $\Delta \mathrm{V}_{\text {REF }}$ | Reference Voltage Line Regulation | $\mathrm{V}_{\text {IN }}=4 \mathrm{~V}$ to 40 V | 3.3 |  |  | mV |
| $\mathrm{G}_{\mathrm{M}}$ | Error Amp <br> Transconductance | $\begin{aligned} & \mathrm{I}_{\mathrm{COMP}}=-30 \mu \mathrm{~A} \text { to }+30 \mu \mathrm{~A} \\ & \mathrm{~V}_{\text {COMP }}=1.0 \mathrm{~V} \end{aligned}$ | 0.750 | 0.447 | 1.491 | mmho |
| Avol | Error Amp Voltage Gain | $\begin{aligned} & \mathrm{V}_{\mathrm{COMP}}=0.5 \mathrm{~V} \text { to } 1.6 \mathrm{~V} \\ & \mathrm{R}_{\mathrm{COMP}}=1.0 \mathrm{M} \Omega \text { (Note } 6 \text { ) } \end{aligned}$ | 165 | 99/49 |  | V/V |

## LM2586-12

| Symbol | Parameters | Conditions | Typical | Min | Max | Units |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| SYSTEM PARAMETERS Test Circuit of Figure 2 (Note 4) |  |  |  |  |  |  |
| V OUT | Output Voltage | $\begin{aligned} & \mathrm{V}_{\text {IN }}=4 \mathrm{~V} \text { to } 10 \mathrm{~V} \\ & \mathrm{I}_{\text {LOAD }}=0.2 \mathrm{~A} \text { to } 0.8 \mathrm{~A} \end{aligned}$ | 12.0 | 11.52/11.40 | 12.48/12.60 | V |
| $\Delta \mathrm{V}_{\text {OUT }} /$ <br> $\Delta \mathrm{V}_{\text {IN }}$ | Line Regulation | $\begin{aligned} & \mathrm{V}_{I N}=4 \mathrm{~V} \text { to } 10 \mathrm{~V} \\ & \mathrm{I}_{\text {LOAD }}=0.2 \mathrm{~A} \end{aligned}$ | 20 |  | 100/200 | mV |
| $\Delta \mathrm{V}_{\text {OUT }} /$ <br> $\Delta I_{\text {LOAD }}$ | Load Regulation | $\begin{aligned} & \mathrm{V}_{I N}=10 \mathrm{~V} \\ & \mathrm{I}_{\text {LOAD }}=0.2 \mathrm{~A} \text { to } 0.8 \mathrm{~A} \end{aligned}$ | 20 |  | 100/200 | mV |
| $\eta$ | Efficiency | $\mathrm{V}_{\mathrm{IN}}=10 \mathrm{~V}, \mathrm{I}$ LOAD $=0.6 \mathrm{~A}$ | 93 |  |  | \% |

UNIQUE DEVICE PARAMETERS (Note 5)

| $V_{\text {REF }}$ | Output Reference <br> Voltage | Measured at Feedback Pin $\mathrm{V}_{\mathrm{COMP}}=1.0 \mathrm{~V}$ | 12.0 | 11.79/11.76 | 12.21/12.24 | V |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| $\Delta \mathrm{V}_{\text {REF }}$ | Reference Voltage Line Regulation | $\mathrm{V}_{\text {IN }}=4 \mathrm{~V}$ to 40 V | 7.8 |  |  | mV |
| $\mathrm{G}_{\mathrm{M}}$ | Error Amp <br> Transconductance | $\begin{aligned} & \mathrm{I}_{\mathrm{COMP}}=-30 \mu \mathrm{~A} \text { to }+30 \mu \mathrm{~A} \\ & \mathrm{~V}_{\mathrm{COMP}}=1.0 \mathrm{~V} \end{aligned}$ | 0.328 | 0.186 | 0.621 | mmho |
| AVOL | Error Amp Voltage Gain | $\begin{aligned} & \mathrm{V}_{\mathrm{COMP}}=0.5 \mathrm{~V} \text { to } 1.6 \mathrm{~V} \\ & \left.\mathrm{R}_{\mathrm{COMP}}=1.0 \mathrm{M} \Omega \text { (Note } 6\right) \end{aligned}$ | 70 | 41/21 |  | V/V |
| LM2586-ADJ |  |  |  |  |  |  |
| Symbol | Parameters | Conditions | Typical | Min | Max | Units |
| SYSTEM PARAMETERS Test Circuit of Figure 2 (Note 4) |  |  |  |  |  |  |
| V OUT | Output Voltage | $\begin{aligned} & \mathrm{V}_{\text {IN }}=4 \mathrm{~V} \text { to } 10 \mathrm{~V} \\ & \mathrm{I}_{\text {LOAD }}=0.2 \mathrm{~A} \text { to } 0.8 \mathrm{~A} \end{aligned}$ | 12.0 | 11.52/11.40 | 12.48/12.60 | V |
| $\Delta \mathrm{V}_{\text {OUT }} /$ <br> $\Delta \mathrm{V}_{\mathrm{IN}}$ | Line Regulation | $\begin{aligned} & \mathrm{V}_{\text {IN }}=4 \mathrm{~V} \text { to } 10 \mathrm{~V} \\ & \mathrm{I}_{\text {LOAD }}=0.2 \mathrm{~A} \end{aligned}$ | 20 |  | 100/200 | mV |
| $\Delta V_{\text {OUT }} /$ $\Delta I_{\text {LOAD }}$ | Load Regulation | $\begin{aligned} & \mathrm{V}_{I N}=10 \mathrm{~V} \\ & \mathrm{I}_{\text {LOAD }}=0.2 \mathrm{~A} \text { to } 0.8 \mathrm{~A} \end{aligned}$ | 20 |  | 100/200 | mV |
| $\eta$ | Efficiency | $\mathrm{V}_{\mathrm{IN}}=10 \mathrm{~V}, \mathrm{I}_{\text {LOAD }}=0.6 \mathrm{~A}$ | 93 |  |  | \% |


| Electrical Characteristics |  |  |  |  |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| Specifications with standard type face are for $T_{J}=25^{\circ} \mathrm{C}$, and those in bold type face apply over full Operating Temperature Range. Unless otherwise specified, $\mathrm{V}_{\mathrm{IN}}=5 \mathrm{~V}$. (Continued) |  |  |  |  |  |  |
| LM2586-ADJ (Continued) |  |  |  |  |  |  |
| Symbol | Parameters | Conditions | Typical | Min | Max | Units |
| UNIQUE DEVICE PARAMETERS (Note 5) |  |  |  |  |  |  |
| $\mathrm{V}_{\text {REF }}$ | Output Reference Voltage | Measured at Feedback Pin $\mathrm{V}_{\mathrm{COMP}}=1.0 \mathrm{~V}$ | 1.230 | 1.208/1.205 | 1.252/1.255 | V |
| $\Delta \mathrm{V}_{\text {REF }}$ | Reference Voltage Line Regulation | $\mathrm{V}_{\mathrm{IN}}=4 \mathrm{~V}$ to 40 V | 1.5 |  |  | mV |
| $\mathrm{G}_{\mathrm{M}}$ | Error Amp <br> Transconductance | $\begin{aligned} & \mathrm{I}_{\mathrm{COMP}}=-30 \mu \mathrm{~A} \text { to }+30 \mu \mathrm{~A} \\ & \mathrm{~V}_{\mathrm{COMP}}=1.0 \mathrm{~V} \end{aligned}$ | 3.200 | 1.800 | 6.000 | mmho |
| Avol | Error Amp Voltage Gain | $\begin{aligned} & \mathrm{V}_{\mathrm{COMP}}=0.5 \mathrm{~V} \text { to } 1.6 \mathrm{~V} \\ & \mathrm{R}_{\mathrm{COMP}}=1.0 \mathrm{M} \Omega \text { (Note } 6 \text { ) } \end{aligned}$ | 670 | 400/200 |  | V/V |
| $\mathrm{I}_{\mathrm{B}}$ | Error Amp Input Bias Current | $\mathrm{V}_{\text {COMP }}=1.0 \mathrm{~V}$ | 125 |  | 425/600 | nA |
| COMMON DEVICE PARAMETERS for all versions (Note 5) |  |  |  |  |  |  |
| Is | Input Supply Current | Switch Off (Note 8) | 11 |  | 15.5/16.5 | mA |
|  |  | $\mathrm{I}_{\text {SWITCH }}=1.8 \mathrm{~A}$ | 50 |  | 100/115 | mA |
| $I_{\text {S/D }}$ | Shutdown Input Supply Current | $\mathrm{V}_{S H}=3 \mathrm{~V}$ | 16 |  | 100/300 | $\mu \mathrm{A}$ |
| $\mathrm{V}_{\mathrm{UV}}$ | Input Supply Undervoltage Lockout | $\mathrm{R}_{\text {LOAD }}=100 \Omega$ | 3.30 | 3.05 | 3.75 | V |
| $\mathrm{fo}_{0}$ | Oscillator Frequency | Measured at Switch Pin <br> $R_{\text {LOAD }}=100 \Omega, V_{\text {COMP }}=1.0 \mathrm{~V}$ <br> Freq. Adj. Pin Open (Pin 1) | 100 | 85/75 | 115/125 | kHz |
|  |  | $\mathrm{R}_{\text {SET }}=22 \mathrm{k} \Omega$ | 200 |  |  | kHz |
| fsc | Short-Circuit Frequency | Measured at Switch Pin $R_{\text {LOAD }}=100 \Omega$ <br> $\mathrm{V}_{\text {FEEDBACK }}=1.15 \mathrm{~V}$ | 25 |  |  | kHz |
| $\mathrm{V}_{\text {EAO }}$ | Error Amplifier Output Swing | Upper Limit (Note 7) | 2.8 | 2.6/2.4 |  | V |
|  |  | Lower Limit (Note 8) | 0.25 |  | 0.40/0.55 | V |
| $\mathrm{I}_{\text {EAO }}$ | Error Amp Output Current (Source or Sink) | (Note 9) | 165 | 110/70 | 260/320 | $\mu \mathrm{A}$ |
| Iss | Soft Start Current | $\begin{aligned} & \mathrm{V}_{\text {FEEDBACK }}=0.92 \mathrm{~V} \\ & \mathrm{~V}_{\text {COMP }}=1.0 \mathrm{~V} \end{aligned}$ | 11.0 | 8.0/7.0 | 17.0/19.0 | $\mu \mathrm{A}$ |
| $\mathrm{D}_{\text {MAX }}$ | Maximum Duty Cycle | $\begin{aligned} & R_{\text {LOAD }}=100 \Omega \\ & \text { (Note 7) } \end{aligned}$ | 98 | 93/90 |  | \% |
| IL | Switch Leakage Current | Switch Off $V_{\text {SWITCH }}=60 \mathrm{~V}$ | 15 |  | 300/600 | $\mu \mathrm{A}$ |
| $\mathrm{V}_{\text {SUS }}$ | Switch Sustaining Voltage | $\mathrm{dV} / \mathrm{dT}=1.5 \mathrm{~V} / \mathrm{ns}$ |  | 65 |  | V |
| $\mathrm{V}_{\text {SAT }}$ | Switch Saturation Voltage | $\mathrm{I}_{\text {SWITCH }}=3.0 \mathrm{~A}$ | 0.45 |  | 0.65/0.9 | V |
| $\mathrm{I}_{\mathrm{CL}}$ | NPN Switch Current Limit |  | 4.0 | 3.0 | 7.0 | A |

## Electrical Characteristics

Specifications with standard type face are for $T_{J}=25^{\circ} \mathrm{C}$, and those in bold type face apply over full Operating Temperature Range. Unless otherwise specified, $\mathrm{V}_{\mathrm{IN}}=5 \mathrm{~V}$. (Continued)

## LM2586-ADJ (Continued)

| Symbol | Parameters | Conditions | Typical | Min | Max | Units |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| COMMON DEVICE PARAMETERS (Note 5) (Continued) |  |  |  |  |  |  |
| $V_{\text {STH }}$ | Synchronization <br> Threshold Voltage | $\begin{aligned} & \mathrm{F}_{\mathrm{SYNC}}=200 \mathrm{kHz} \\ & \mathrm{~V}_{\mathrm{COMP}}=1 \mathrm{~V}, \mathrm{~V}_{\mathrm{IN}}=5 \mathrm{~V} \end{aligned}$ | 0.75 | 0.625/0.40 | 0.875/1.00 | V |
| ISYNC | Synchronization <br> Pin Current | $\begin{aligned} & \mathrm{V}_{\mathrm{IN}}=5 \mathrm{~V} \\ & \mathrm{~V}_{\mathrm{COMP}}=1 \mathrm{~V}, \mathrm{~V}_{\mathrm{SYNC}}=\mathrm{V}_{\mathrm{STH}} \end{aligned}$ | 100 |  | 200 | $\mu \mathrm{A}$ |
| $\mathrm{V}_{\text {SHTH }}$ | $\overline{O N} / O F F$ Pin (Pin 1) <br> Threshold Voltage | $\begin{aligned} & \mathrm{V}_{\text {COMP }}=1 \mathrm{~V} \\ & (\text { Note } 10) \end{aligned}$ | 1.6 | 1.0/0.8 | 2.2/2.4 | V |
| $\mathrm{I}_{\text {SH }}$ | $\overline{O N} / O F F$ Pin (Pin 1) <br> Current | $\begin{aligned} & \mathrm{V}_{\mathrm{COMP}}=1 \mathrm{~V} \\ & \mathrm{~V}_{\mathrm{SH}}=\mathrm{V}_{\mathrm{SH}} \end{aligned}$ | 40 | 15/10 | 65/75 | $\mu \mathrm{A}$ |
| $\theta_{\mathrm{JA}}$ <br> $\theta_{\text {JA }}$ <br> $\theta_{\mathrm{JC}}$ | Thermal Resistance | T Package, Junction to Ambient (Note 11) <br> T Package, Junction to Ambient (Note 12) <br> T Package, Junction to Case | $\begin{gathered} 65 \\ 45 \\ 2 \end{gathered}$ |  |  |  |
| $\begin{aligned} & \theta_{\mathrm{JA}} \\ & \theta_{\mathrm{JA}} \\ & \theta_{\mathrm{JA}} \\ & \theta_{\mathrm{JC}} \end{aligned}$ |  | S Package, Junction to Ambient (Note 13) <br> S Package, Junction to Ambient (Note 14) <br> S Package, Junction to Ambient (Note 15) <br> S Package, Junction to Case | $\begin{gathered} 56 \\ 35 \\ 26 \\ 2 \end{gathered}$ |  |  | ${ }^{\circ} \mathrm{C} / \mathrm{W}$ |

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. These ratings apply when the current is limited to less than 1.2 mA for pins $1,2,3$, and 6 . Operating ratings indicate conditions for which the device is intended to be functional, but device parameter specifications may not be guaranteed under these conditions. For guaranteed specifications and test conditions, see the Electrical Characteristics.
Note 2: Note that switch current and output current are not identical in a step-up regulator. Output current cannot be internally limited when the LM2586 is used as a step-up regulator. To prevent damage to the switch, the output current must be externally limited to 3 A . However, output current is internally limited when the LM2586 is used as a flyback regulator (see the Application Hints section for more information).
Note 3: The junction temperature of the device $\left(T_{J}\right)$ is a function of the ambient temperature ( $T_{A}$ ), the junction-to-ambient thermal resistance ( $\theta_{\mathrm{JA}}$ ), and the power dissipation of the device ( $P_{D}$ ). A thermal shutdown will occur if the temperature exceeds the maximum junction temperature of the device: $P_{D} \times \theta_{J A}+T_{A(M A X} \geq$
$T_{J(M A X)}$. For a safe thermal design, check that the maximum power dissipated by the device is less than: $P_{D} \leq\left[T_{J(M A X)}-T_{A(M A X)}\right] / \theta_{J A}$. When calculating the maximum allowable power dissipation, derate the maximum junction temperature-this ensures a margin of safety in the thermal design.
Note 4: External components such as the diode, inductor, input and output capacitors can affect switching regulator performance. When the LM2586 is used as shown in Figures 1 and 2, system performance will be as specified by the system parameters.
Note 5: All room temperature limits are 100\% production tested, and all limits at temperature extremes are guaranteed via correlation using standard Statistical Quality Control (SQC) methods.
Note 6: A $1.0 \mathrm{M} \Omega$ resistor is connected to the compensation pin (which is the error amplifier output) to ensure accuracy in measuring Avol.
Note 7: To measure this parameter, the feedback voltage is set to a low value, depending on the output version of the device, to force the error amplifier output high and the switch on.
Note 8: To measure this parameter, the feedback voltage is set to a high value, depending on the output version of the device, to force the error amplifier output low and the switch off

Note 9: To measure the worst-case error amplifier output current, the LM2586 is tested with the feedback voltage set to its low value (specified in Note 7) and at its high value (specified in Note 8).
Note 10: When testing the minimum value, do not sink current from this pin-isolate it with a diode. If current is drawn from this pin, the frequency adjust circuit will begin operation (see Figure 41).
Note 11: Junction to ambient thermal resistance (no external heat sink) for the 7 lead TO-220 package mounted vertically, with $1 / 2$ inch leads in a socket, or on a PC board with minimum copper area.
Note 12: Junction to ambient thermal resistance (no external heat sink) for the 7 lead TO-220 package mounted vertically, with $1 / 2$ inch leads soldered to a PC board containing approximately 4 square inches of ( 1 oz .) copper area surrounding the leads.
Note 13: Junction to ambient thermal resistance for the 7 lead TO-263 mounted horizontally against a PC board area of 0.136 square inches (the same size as the TO-263 package) of 1 oz . ( 0.0014 in . thick) copper.
Note 14: Junction to ambient thermal resistance for the 7 lead TO-263 mounted horizontally against a PC board area of 0.4896 square inches ( 3.6 times the area of the TO-263 package) of 1 oz ( ( 0.0014 in. thick) copper.
Note 15: Junction to ambient thermal resistance for the 7 lead TO-263 mounted horizontally against a PC board copper area of 1.0064 square inches ( 7.4 times the area of the TO-263 package) of 1 oz. ( 0.0014 in. thick) copper. Additional copper area will reduce thermal resistance further. See the thermal model in Switchers Made Simple ${ }^{\circledR}$ software.

## Typical Performance Characteristics






TL/H/12516-8
Error Amp Transconductance vs Temperature
 TEMPERATURE (C)

TL/H/12516-11



TL/H/12516-6
Switch Transconductance vs Temperature


TL/H/12516-9



TL/H/12516-4
Feedback Pin Bias Current vs Temperature


$$
\mathrm{TL} / \mathrm{H} / 12516-7
$$

## Oscillator Frequency

vs Temperature

temperature (c)
TL/H/12516-10
Short Circuit Frequency vs Temperature


## Typical Performance Characteristics (Continued)


$\overline{\text { ON }}$ /OFF Pin Current vs Voltage


Oscillator Frequency vs Resistance


## Connection Diagrams



Order Number LM2586T-3.3, LM2586T-5.0,
LM2586T-12 or LM2586T-ADJ See NS Package Number TA07B

TL/H/12516-15
TL/H/12516-16

7-Lead TO-263 (S)
Top View


TL/H/12516-19
Order Number LM2586S-3.3, LM2586S-5.0,
LM2586S-12 or LM2586S-ADJ
Tape and Reel Order Number LM2586SX-3.3, LM2586SX-5.0, LM2586SX-12 or LM2586SX-ADJ

See NS Package Number TS7B

## Test Circuits



FIGURE 2. LM2586-12 and LM2586-ADJ

## Block Diagram



For Fixed Versions
$3.3 \mathrm{~V}, \mathrm{R} 1=3.4 \mathrm{k}, \mathrm{R} 2=2 \mathrm{k}$
$5.0 \mathrm{~V}, \mathrm{R} 1=6.15 \mathrm{k}, \mathrm{R} 2=2 \mathrm{k}$
$12 \mathrm{~V}, \mathrm{R} 1=8.73 \mathrm{k}, \mathrm{R} 2=1 \mathrm{k}$
For Adj. Version
R1 $=$ Short $(0 \Omega), R 2=$ Open

## FIGURE 3

## Flyback Regulator Operation

The LM2586 is ideally suited for use in the flyback regulator topology. The flyback regulator can produce a single output voltage, such as the one shown in Figure 4, or multiple output voltages. In Figure 4, the flyback regulator generates an output voltage that is inside the range of the input voltage. This feature is unique to flyback regulators and cannot be duplicated with buck or boost regulators.
The operation of a flyback regulator is as follows (refer to Figure 4): when the switch is on, current flows through the primary winding of the transformer, T 1 , storing energy in the magnetic field of the transformer. Note that the primary and secondary windings are out of phase, so no current flows through the secondary when current flows through the primary. When the switch turns off, the magnetic field col-
lapses, reversing the voltage polarity of the primary and secondary windings. Now rectifier D1 is forward biased and current flows through it, releasing the energy stored in the transformer. This produces voltage at the output.
The output voltage is controlled by modulating the peak switch current. This is done by feeding back a portion of the output voltage to the error amp, which amplifies the difference between the feedback voltage and a 1.230 V reference. The error amp output voltage is compared to a ramp voltage proportional to the switch current (i.e., inductor current during the switch on time). The comparator terminates the switch on time when the two voltages are equal, thereby controlling the peak switch current to maintain a constant output voltage.


TL/H/12516-24 As shown in Figure 4, the LM2586 can be used as a flyback regulator by using a minimum number of external components. The switching waveforms of this regulator are shown in Figure 5. Typical Performance Characteristics observed during the operation of this circuit are shown in Figure 6.

FIGURE 4. 12V Flyback Regulator Design Example

## Typical Performance Characteristics

A


A: Switch Voltage, 20V/div
B: Switch Current, 2A/div
C: Output Rectifier Current, 2A/div
D: Output Ripple Voltage, $50 \mathrm{mV} / \mathrm{div}$
AC-Coupled
c
D

TL/H/12516-25
FIGURE 5. Switching Waveforms


Horizontal: $2 \mathrm{~ms} /$ div
FIGURE 6. V

## Typical Flyback Regulator Applications

Figures 7 through 12 show six typical flyback applications, varying from single output to triple output. Each drawing contains the part number(s) and manufacturer(s) for every component except the transformer. For the transformer part numbers and manufacturers' names, see the table in

Figure 13. For applications with different output voltagesrequiring the LM2586-ADJ-or different output configurations that do not match the standard configurations, refer to the Switchers Made Simple ${ }^{\circledR}$ software.


FIGURE 7. Single-Output Flyback Regulator


FIGURE 8. Single-Output Flyback Regulator

## Typical Flyback Regulator Applications (Continued)



TL/H/12516-29
FIGURE 9. Single-Output Flyback Regulator


TL/H/12516-30
FIGURE 10. Dual-Output Flyback Regulator

Typical Flyback Regulator Applications (Continued)


FIGURE 12. Triple-Output Flyback Regulator

## Typical Flyback Regulator Applications (Continued)

Transformer Selection (T)
Figure 13 lists the standard transformers available for flyback regulator applications. Included in the table are the turns ratio(s) for each transformer, as well as the output voltages, input voltage ranges, and the maximum load currents for each circuit.

| Applications | Figure 7 | Figure 8 | Figure 9 | Figure 10 | Figure 11 | Figure 12 |
| :--- | :---: | :---: | :---: | :---: | :---: | :---: |
| Transformers | T7 | T7 | T7 | T6 | T6 | T5 |
| $\mathrm{V}_{\text {IN }}$ | $4 \mathrm{~V}-6 \mathrm{~V}$ | $4 \mathrm{~V}-6 \mathrm{~V}$ | $8 \mathrm{~V}-16 \mathrm{~V}$ | $4 \mathrm{~V}-6 \mathrm{~V}$ | $18 \mathrm{~V}-36 \mathrm{~V}$ | $18 \mathrm{~V}-36 \mathrm{~V}$ |
| $\mathrm{~V}_{\text {OUT1 }}$ | 3.3 V | 5 V | 12 V | 12 V | 12 V | 5 V |
| $\mathrm{I}_{\text {OUT1 }}(\mathrm{Max})$ | 1.4 A | 1 A | 0.8 A | 0.15 A | 0.6 A | 1.8 A |
| $\mathrm{~N}_{1}$ | 1 | 1 | 1 | 1.2 | 1.2 | 0.5 |
| $\mathrm{~V}_{\text {OUT2 }}$ |  |  |  | -12 V | -12 V | 12 V |
| $\mathrm{I}_{\text {OUT2 }}(\mathrm{Max})$ |  |  |  | 0.15 A | 0.6 A | 0.25 A |
| $\mathrm{~N}_{2}$ |  |  | 1.2 | 1.2 | 1.15 |  |
| $\mathrm{~V}_{\text {OUT3 }}$ |  |  |  |  | -12 V |  |
| $\mathrm{I}_{\text {OUT3 }}$ (Max) |  |  |  |  |  | 0.25 A |
| $\mathrm{~N}_{3}$ |  |  |  |  | 1.15 |  |

FIGURE 13. Transformer Selection Table

| Transformer Type | Manufacturers' Part Numbers |  |  |  |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  | Coilcraft(1) | Coilcraft(1) Surface Mount | Pulse ${ }^{(2)}$ <br> Surface Mount | Pulse ${ }^{(2)}$ | Renco(3) | Schott(4) |
| T5 | Q4338-B | Q4437-B | PE-68413 | - | RL-5532 | 67140890 |
| T6 | Q4339-B | Q4438-B | PE-68414 | - | RL-5533 | 67140900 |
| T7 | S6000-A | S6057-A | - | PE-68482 | RL-5751 | 26606 |
|  |  | oilcraft Inc., <br> er Lake Road, Cary, IL Headquarters, 21 Na North, Cumbernauld, ulse Engineering Inc., orld Trade Drive, San Dis Headquarters, Dunm Galway, Ireland Renco Electronics Inc., Blvd. East, Deer Park chott Corp., <br> kers Lane Road, Wayz | ce <br> Ad G68 0LL <br> A 92128 <br> ad <br> 1729 <br> N 55391 | (800) 322-26 (708) 639-1 4412367305 4412367306 <br> : (619) 674-81 <br> : (619) 674-82 <br> $+35393241$ <br> $+35393244$ <br> : (800) 645-58 <br> (516) 586-55 <br> : (612) 475-11 <br> : (612) 475-17 |  |  |

FIGURE 14. Transformer Manufacturer Guide

## Typical Flyback Regulator Applications (Continued)

## Transformer Footprints

Figures 15 through 29 show the footprints of each transformer, listed in Figure 14.


FIGURE 15. Coilcraft S6000-A


TL/H/12516-35
FIGURE 17. Coilcraft Q4437-B (Surface Mount)


FIGURE 19. Coilcraft S6057-A (Surface Mount)


TL/H/12516-34
Top View
FIGURE 16. Coilcraft Q4339-B


TL/H/12516-36
Top View
FIGURE 18. Coilcraft Q4338-B


FIGURE 20. Coilcraft Q4438-B (Surface Mount)

## Typical Flyback Regulator Applications (Continued)



FIGURE 21. Pulse PE-68482


FIGURE 23. Pulse PE-68413 (Surface Mount)

FIGURE 25. Renco RL-5533


T6


FIGURE 22. Pulse PE-68414
(Surface Mount)

T7


FIGURE 24. Renco RL-5751


TL/H/12516-46
Top View
FIGURE 26. Renco RL-5532

## Typical Flyback Regulator Applications (Continued)



## Step-Up (Boost) Regulator Operation

Figure 30 shows the LM2586 used as a step-up (boost) regulator. This is a switching regulator that produces an output voltage greater than the input supply voltage.
A brief explanation of how the LM2586 Boost Regulator works is as follows (refer to Figure 30). When the NPN switch turns on, the inductor current ramps up at the rate of $\mathrm{V}_{\mathrm{IN}} / \mathrm{L}$, storing energy in the inductor. When the switch turns
off, the lower end of the inductor flies above $\mathrm{V}_{\mathrm{IN}}$, discharging its current through diode (D) into the output capacitor (COUT) at a rate of $\left(\mathrm{V}_{\text {OUT }}-\mathrm{V}_{\text {IN }}\right) / \mathrm{L}$. Thus, energy stored in the inductor during the switch on time is transferred to the output during the switch off time. The output voltage is controlled by adjusting the peak switch current, as described in the flyback regulator section.


FIGURE 30. 12V Boost Regulator
By adding a small number of external components (as shown in Figure 30), the LM2586 can be used to produce a regulated output voltage that is greater than the applied input voltage. The switching waveforms observed during the operation of this circuit are shown in Figure 31. Typical performance of this regulator is shown in Figure 32.
Typical Performance Characteristics


A: Switch Voltage, 10V/div
B: Switch Current, 2A/div
C: Inductor Current, 2A/div
D: Output Ripple Voltage,
$100 \mathrm{mV} / \mathrm{div}$, AC-Coupled
FIGURE 31. Switching Waveforms


FIGURE 32. V

## Typical Boost Regulator Applications

Figures 33 and 35 through 37 show four typical boost appli-cations-one fixed and three using the adjustable version of the LM2586. Each drawing contains the part number(s) and manufacturer(s) for every component. For the fixed 12 V
output application, the part numbers and manufacturers' names for the inductor are listed in a table in Figure 34. For applications with different output voltages, refer to the Switchers Made Simple ${ }^{\circledR}$ software.


TL/H/12516-54
FIGURE 33. +5 V to $+\mathbf{1 2 V}$ Boost Regulator

Figure 34 contains a table of standard inductors, by part number and corresponding manufacturer, for the fixed output regulator of Figure 33.

| Coilcraft (Note 1) | Pulse (Note 2) | Renco (Note 3) | Schott (Note 4) | Schott (Note 4) <br> (Surface Mount) |
| :---: | :---: | :---: | :---: | :---: |
| DO3316-153 | PE-53898 | RL-5471-7 | 67146510 | 67146540 |

Note 1: Coilcraft Inc.,
Phone: (800) 322-2645 Fax: (708) 639-1469
European Headquarters, 21 Napier Place Phone: + 441236730595
Wardpark North, Cumbernauld, Scotland G68 OLL Fax: + 441236730627
Note 2: Pulse Engineering Inc.,
12220 World Trade Drive, San Diego, CA 92128
European Headquarters, Dunmore Road
Tuam, Co. Galway, Ireland
Note 3: Renco Electronics Inc.,
60 Jeffryn Blvd. East, Deer Park, NY 11729
Note 4: Schott Corp.,
1000 Parkers Lane Road, Wayzata, MN 55391

Phone: (619) 674-8100 Fax: (619) 674-8262
Phone: + 3539324107 Fax: + 3539324459
Phone: (800) 645-5828 Fax: (516) 586-5562

Phone: (612) 475-1173 Fax: (612) 475-1786

FIGURE 34. Inductor Selection Table

## Typical Boost Regulator Applications (Continued)



TL/H/12516-55
FIGURE 35. +12 V to +24 V Boost Regulator


TL/H/12516-56
FIGURE 36. +24 V to +36 V Boost Regulator


TL/H/12516-57
FIGURE 37. +24 V to $+\mathbf{4 8 V}$ Boost Regulator
*The LM2586 will require a heat sink in these applications. The size of the heat sink will depend on the maximum ambient temperature. To calculate the thermal resistance of the IC and the size of the heat sink needed, see the "Heat Sink/Thermal Considerations" section in the Application Hints.

## Application Hints

LM2586 SPECIAL FEATURES


TL/H/12516-58
FIGURE 38. Shutdown Operation

## SHUTDOWN CONTROL

A feature of the LM2586 is its ability to be shut down using the ON/OFF pin (pin 1). This feature conserves input power by turning off the device when it is not in use. For proper operation, an isolation diode is required (as shown in Figure 38).

The device will shut down when 3 V or greater is applied on the $\overline{O N} / O F F$ pin, sourcing current into pin 1 . In shut down mode, the device will draw typically $56 \mu \mathrm{~A}$ of supply current ( $16 \mu \mathrm{~A}$ to $\mathrm{V}_{\mathrm{IN}}$ and $40 \mu \mathrm{~A}$ to the $\overline{\mathrm{ON}} /$ OFF pin). To turn the device back on, leave pin 1 floating, using an (isolation) diode, as shown in Figure 38 (for normal operation, do not source or sink current to or from this pin-see the next section).

## FREQUENCY ADJUSTMENT

The switching frequency of the LM2586 can be adjusted with the use of an external resistor. This feature allows the user to optimize the size of the magnetics and the output capacitor(s) by tailoring the operating frequency. A resistor connected from pin 1 (the Freq. Adj. pin) to ground will set the switching frequency from 100 kHz to 200 kHz (maximum). As shown in Figure 38, the pin can be used to adjust the frequency while still providing the shut down function. A curve in the Performance Characteristics Section graphs the resistor value to the corresponding switching frequency. The table in Figure 39 shows resistor values corresponding to commonly used frequencies.
However, changing the LM2586's operating frequency from its nominal value of 100 kHz will change the magnetics selection and compensation component values.

| $\mathbf{R}_{\mathbf{S E T}}(\mathbf{k} \Omega$ ) | Frequency (kHz) |
| :---: | :---: |
| Open | 100 |
| 200 | 125 |
| 47 | 150 |
| 33 | 175 |
| 22 | 200 |

FIGURE 39. Frequency Setting Resistor Guide


## FIGURE 40. Frequency Synchronization

## FREQUENCY SYNCHRONIZATION

Another feature of the LM2586 is the ability to synchronize the switching frequency to an external source, using the sync pin (pin 6). This feature allows the user to parallel multiple devices to deliver more output power.
A negative falling pulse applied to the sync pin will synchronize the LM2586 to an external oscillator (see Figures 40 and 41).
Use of this feature enables the LM2586 to be synchronized to an external oscillator, such as a system clock. This operation allows multiple power supplies to operate at the same frequency, thus eliminating frequency-related noise problems.


FIGURE 41. Waveforms of a Synchronized 12V Boost Regulator
The scope photo in Figure 41 shows a LM2586 12V Boost Regulator synchronized to a 200 kHz signal. There is a 700 ns delay between the falling edge of the sync signal and the turning on of the switch.

## Application Hints (Continued)



TL/H/12516-61
FIGURE 42. Boost Regulator

## PROGRAMMING OUTPUT VOLTAGE <br> output with an external current limit circuit. The external limit

 (SELECTING R1 AND R2)Referring to the adjustable regulator in Figure 42, the output voltage is programmed by the resistors R1 and R2 by the following formula:

$$
V_{\text {OUT }}=V_{\text {REF }}(1+R 1 / R 2) \quad \text { where } V_{\text {REF }}=1.23 V
$$

Resistors R1 and R2 divide the output voltage down so that it can be compared with the 1.23 V internal reference. With R2 between $1 k$ and $5 k, R 1$ is:

$$
\mathrm{R} 1=\mathrm{R} 2\left(\mathrm{~V}_{\mathrm{OUT}} / \mathrm{V}_{\mathrm{REF}}-1\right) \quad \text { where } \mathrm{V}_{\mathrm{REF}}=1.23 \mathrm{~V}
$$

For best temperature coefficient and stability with time, use $1 \%$ metal film resistors.

## SHORT CIRCUIT CONDITION

Due to the inherent nature of boost regulators, when the output is shorted (see Figure 42), current flows directly from the input, through the inductor and the diode, to the output, bypassing the switch. The current limit of the switch does not limit the output current for the entire circuit. To protect the load and prevent damage to the switch, the current must be externally limited, either by the input supply or at the
should be set to the maximum switch current of the device, which is 3A.
In a flyback regulator application (Figure 43), using the standard transformers, the LM2586 will survive a short circuit to the main output. When the output voltage drops to $80 \%$ of its nominal value, the frequency will drop to 25 kHz . With a lower frequency, off times are larger. With the longer off times, the transformer can release all of its stored energy before the switch turns back on. Hence, the switch turns on initially with zero current at its collector. In this condition, the switch current limit will limit the peak current, saving the device.

## FLYBACK REGULATOR INPUT CAPACITORS

A flyback regulator draws discontinuous pulses of current from the input supply. Therefore, there are two input capacitors needed in a flyback regulator-one for energy storage and one for filtering (see Figure 43). Both are required due to the inherent operation of a flyback regulator. To keep a stable or constant voltage supply to the LM2586, a storage capacitor $(\geq 100 \mu \mathrm{~F})$ is required. If the input source is a


FIGURE 43. Flyback Regulator

## Application Hints (Continued)

rectified DC supply and/or the application has a wide temperature range, the required rms current rating of the capacitor might be very large. This means a larger value of capacitance or a higher voltage rating will be needed for the input capacitor. The storage capacitor will also attenuate noise which may interfere with other circuits connected to the same input supply voltage.
In addition, a small bypass capacitor is required due to the noise generated by the input current pulses. To eliminate the noise, insert a $1.0 \mu \mathrm{~F}$ ceramic capacitor between $\mathrm{V}_{\mathrm{IN}}$ and ground as close as possible to the device.

## SWITCH VOLTAGE LIMITS

In a flyback regulator, the maximum steady-state voltage appearing at the switch, when it is off, is set by the transformer turns ratio, N , the output voltage, $\mathrm{V}_{\text {OUT }}$, and the maximum input voltage, $\mathrm{V}_{\mathrm{IN}}(\mathrm{Max})$ :

$$
V_{\text {SW }(\mathrm{OFF})}=\mathrm{V}_{\text {IN }}(\mathrm{Max})+\left(\mathrm{V}_{\text {OUT }}+\mathrm{V}_{\mathrm{F}}\right) / \mathrm{N}
$$

where $V_{F}$ is the forward biased voltage of the output diode, and is typically 0.5 V for Schottky diodes and 0.8 V for ultrafast recovery diodes. In certain circuits, there exists a voltage spike, $\mathrm{V}_{\mathrm{LL}}$, superimposed on top of the steady-state voltage (see Figure 5, waveform A). Usually, this voltage spike is caused by the transformer leakage inductance and/ or the output rectifier recovery time. To "clamp" the voltage at the switch from exceeding its maximum value, a transient suppressor in series with a diode is inserted across the transformer primary (as shown in the circuit in Figure 4 and other flyback regulator circuits throughout the datasheet). The schematic in Figure 43 shows another method of clamping the switch voltage. A single voltage transient suppressor (the SA51A) is inserted at the switch pin. This method clamps the total voltage across the switch, not just the voltage across the primary.
If poor circuit layout techniques are used (see the "Circuit Layout Guideline" section), negative voltage transients may appear on the Switch pin (pin 5). Applying a negative voltage (with respect to the IC's ground) to any monolithic IC pin causes erratic and unpredictable operation of that IC. This holds true for the LM2586 IC as well. When used in a flyback regulator, the voltage at the Switch pin (pin 5) can go negative when the switch turns on. The "ringing" voltage at the switch pin is caused by the output diode capacitance and the transformer leakage inductance forming a resonant circuit at the secondary(ies). The resonant circuit generates the "ringing" voltage, which gets reflected back through the transformer to the switch pin. There are two common methods to avoid this problem. One is to add an RC snubber around the output rectifier(s), as in Figure 43. The values of the resistor and the capacitor must be chosen so that the voltage at the Switch pin does not drop below -0.4 V . The resistor may range in value between $10 \Omega$ and $1 \mathrm{k} \Omega$, and the capacitor will vary from $0.001 \mu \mathrm{~F}$ to $0.1 \mu \mathrm{~F}$. Adding a snubber will (slightly) reduce the efficiency of the overall circuit.
The other method to reduce or eliminate the "ringing" is to insert a Schottky diode clamp between pins 5 and 4 (ground), also shown in Figure 43. This prevents the voltage at pin 5 from dropping below -0.4 V . The reverse voltage rating of the diode must be greater than the switch off voltage.


FIGURE 44. Input Line Filter

## OUTPUT VOLTAGE LIMITATIONS

The maximum output voltage of a boost regulator is the maximum switch voltage minus a diode drop. In a flyback regulator, the maximum output voltage is determined by the turns ratio, N , and the duty cycle, D , by the equation:

$$
V_{\text {OUT }} \approx N \times V_{\text {IN }} \times D /(1-D)
$$

The duty cycle of a flyback regulator is determined by the following equation:

$$
\mathrm{D}=\frac{\mathrm{V}_{\mathrm{OUT}}+\mathrm{V}_{\mathrm{F}}}{\mathrm{~N}\left(\mathrm{~V}_{\text {IN }}-\mathrm{V}_{\mathrm{SAT}}\right)+\mathrm{V}_{\mathrm{OUT}}+\mathrm{V}_{\mathrm{F}}} \approx \frac{\mathrm{~V}_{\mathrm{OUT}}}{\mathrm{~N}\left(\mathrm{~V}_{\text {IN }}\right)+\mathrm{V}_{\mathrm{OUT}}}
$$

Theoretically, the maximum output voltage can be as large as desired-just keep increasing the turns ratio of the transformer. However, there exists some physical limitations that prevent the turns ratio, and thus the output voltage, from increasing to infinity. The physical limitations are capacitances and inductances in the LM2586 switch, the output diode(s), and the transformer-such as reverse recovery time of the output diode (mentioned above).

## NOISY INPUT LINE CONDITION

A small, low-pass RC filter should be used at the input pin of the LM2586 if the input voltage has an unusually large amount of transient noise, such as with an input switch that bounces. The circuit in Figure 44 demonstrates the layout of the filter, with the capacitor placed from the input pin to ground and the resistor placed between the input supply and the input pin. Note that the values of $\mathrm{R}_{\text {IN }}$ and $\mathrm{C}_{I N}$ shown in the schematic are good enough for most applications, but some readjusting might be required for a particular application. If efficiency is a major concern, replace the resistor with a small inductor (say $10 \mu \mathrm{H}$ and rated at 200 mA ).

## STABILITY

All current-mode controlled regulators can suffer from an instability, known as subharmonic oscillation, if they operate with a duty cycle above $50 \%$. To eliminate subharmonic oscillations, a minimum value of inductance is required to ensure stability for all boost and flyback regulators. The minimum inductance is given by:

$$
\mathrm{L}(\operatorname{Min})=\frac{2.92\left[\left(\mathrm{~V}_{\mathrm{IN}}(\operatorname{Min})-\mathrm{V}_{\mathrm{SAT}}\right) \bullet(2 \mathrm{D}(\operatorname{Max})-1)\right]}{1-\mathrm{D}(\operatorname{Max})}(\mu \mathrm{H})
$$

where $\mathrm{V}_{\text {SAT }}$ is the switch saturation voltage and can be found in the Characteristic Curves.

## Application Hints (Continued)



TL/H/12516-64
FIGURE 45. Circuit Board Layout

## CIRCUIT LAYOUT GUIDELINES

As in any switching regulator, layout is very important. Rapidly switching currents associated with wiring inductance generate voltage transients which can cause problems. For minimal inductance and ground loops, keep the length of the leads and traces as short as possible. Use single point grounding or ground plane construction for best results. Separate the signal grounds from the power grounds (as indicated in Figure 45). When using the Adjustable version, physically locate the programming resistors as near the regulator IC as possible, to keep the sensitive feedback wiring short.

## HEAT SINK/THERMAL CONSIDERATIONS

In many cases, a heat sink is not required to keep the LM2586 junction temperature within the allowed operating temperature range. For each application, to determine whether or not a heat sink will be required, the following must be identified:

1) Maximum ambient temperature (in the application).
2) Maximum regulator power dissipation (in the application).
3) Maximum allowed junction temperature $\left(125^{\circ} \mathrm{C}\right.$ for the LM2586). For a safe, conservative design, a temperature approximately $15^{\circ} \mathrm{C}$ cooler than the maximum junction temperature should be selected $\left(110^{\circ} \mathrm{C}\right)$.
4) LM2586 package thermal resistances $\theta_{\mathrm{JA}}$ and $\theta_{\mathrm{JC}}$ (given in the Electrical Characteristics).
Total power dissipated ( $\mathrm{P}_{\mathrm{D}}$ ) by the LM2586 can be estimated as follows:
Boost:

$$
P_{D}=0.15 \Omega \cdot\left(\frac{I_{L O A D}}{1-D}\right)^{2} \bullet D+\frac{I_{L O A D}}{50 \bullet(1-D)} \bullet D \bullet V_{I N}
$$

Flyback:

$$
\begin{aligned}
\mathrm{P}_{\mathrm{D}}= & 0.15 \Omega \cdot\left(\frac{\mathrm{~N} \cdot \Sigma \mathrm{I}_{\mathrm{LOAD}}}{1-\mathrm{D}}\right)^{2} \bullet \mathrm{D} \\
& +\frac{\mathrm{N} \cdot \Sigma I_{\mathrm{LOAD}}}{50 \cdot(1-\mathrm{D})} \bullet \mathrm{D} \bullet \mathrm{~V}_{I N}
\end{aligned}
$$

$\mathrm{V}_{\mathrm{IN}}$ is the minimum input voltage, $\mathrm{V}_{\mathrm{OUT}}$ is the output voltage, $N$ is the transformer turns ratio, $D$ is the duty cycle, and $l_{\text {LOAD }}$ is the maximum load current (and $\Sigma$ lomad $_{\text {LOA }}$ is the sum of the maximum load currents for multiple-output flyback regulators). The duty cycle is given by:
Boost:

$$
\mathrm{D}=\frac{\mathrm{V}_{\text {OUT }}+\mathrm{V}_{\mathrm{F}}-\mathrm{V}_{\text {IN }}}{\mathrm{V}_{\text {OUT }}+\mathrm{V}_{\mathrm{F}}-\mathrm{V}_{\text {SAT }}} \approx \frac{\mathrm{V}_{\text {OUT }}-\mathrm{V}_{\text {IN }}}{\mathrm{V}_{\text {OUT }}}
$$

Flyback:

$$
\mathrm{D}=\frac{\mathrm{V}_{\mathrm{OUT}}+\mathrm{V}_{\mathrm{F}}}{\mathrm{~N}\left(\mathrm{~V}_{\text {IN }}-\mathrm{V}_{\mathrm{SAT}}\right)+\mathrm{V}_{\mathrm{OUT}}+\mathrm{V}_{\mathrm{F}}} \approx \frac{\mathrm{~V}_{\mathrm{OUT}}}{\mathrm{~N}\left(\mathrm{~V}_{I N}\right)+\mathrm{V}_{\mathrm{OUT}}}
$$

where $\mathrm{V}_{\mathrm{F}}$ is the forward biased voltage of the diode and is typically 0.5 V for Schottky diodes and 0.8 V for fast recovery diodes. $\mathrm{V}_{\text {SAT }}$ is the switch saturation voltage and can be found in the Characteristic Curves.
When no heat sink is used, the junction temperature rise is:

$$
\Delta T_{J}=P_{D} \bullet \theta_{J A} .
$$

Adding the junction temperature rise to the maximum ambient temperature gives the actual operating junction temperature:

$$
\mathrm{T}_{\mathrm{J}}=\Delta \mathrm{T}_{\mathrm{J}}+\mathrm{T}_{\mathrm{A}} .
$$

If the operating junction temperature exceeds the maximum junction temperatue in item 3 above, then a heat sink is required. When using a heat sink, the junction temperature rise can be determined by the following:

$$
\Delta \mathrm{T}_{\mathrm{J}}=\mathrm{P}_{\mathrm{D}} \bullet\left(\theta_{\mathrm{JC}}+\theta_{\text {Interface }}+\theta_{\text {Heat Sink }}\right)
$$

Again, the operating junction temperature will be:

$$
T_{J}=\Delta T_{J}+T_{A}
$$

## Application Hints (Continued)

As before, if the maximum junction temperature is exceeded, a larger heat sink is required (one that has a lower thermal resistance).
Included in the Switchers Made Simple ${ }^{\circledR}$ design software is a more precise (non-linear) thermal model that can be used to determine junction temperature with different inputoutput parameters or different component values. It can also calculate the heat sink thermal resistance required to maintain the regulator junction temperature below the maximum operating temperature.

To further simplify the flyback regulator design procedure, National Semiconductor is making available computer design software to be used with the Simple Switcher ${ }^{\circledR}$ line of switching regulators. Switchers Made Simple ${ }^{\circledR}$ is available on a $31 / 2^{\prime \prime}$ diskette for IBM compatible computers from a National Semiconductor sales office in your area or the National Semiconductor Customer Response Center (1-800-272-9959).

## Physical Dimensions inches (millimeters) unless otherwise noted


LM2586 SIMPLE SWITCHER 3A Flyback Regulator with Shutdown
Physical Dimensions inches (millimeters) unless otherwise noted (Continued)


## LIFE SUPPORT POLICY

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| :---: | :---: | :---: | :---: |



Absolute Maximum Ratings (Note 1)
If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

| Input Voltage | $-0.4 \mathrm{~V} \leq \mathrm{V}_{\text {IN }} \leq 45 \mathrm{~V}$ |
| :--- | ---: |
| Switch Voltage | $-0.4 \mathrm{~V} \leq \mathrm{V}_{\mathrm{SW}} \leq 65 \mathrm{~V}$ |
| Switch Current (Note 2) | Internally Limited |
| Compensation Pin Voltage | $-0.4 \mathrm{~V} \leq \mathrm{V}_{\mathrm{COMP}} \leq 2.4 \mathrm{~V}$ |
| Feedback Pin Voltage | $-0.4 \mathrm{~V} \leq \mathrm{V}_{\mathrm{FB}} \leq 2 \mathrm{~V}_{\mathrm{OUT}}$ |
| Power Dissipation (Note 3) | Internally Limited |


| Storage Temperature Range | $-65^{\circ} \mathrm{C}$ to $+150^{\circ} \mathrm{C}$ |
| :--- | ---: |
| Lead Temperature (Soldering, 10 sec.$)$ | $260^{\circ} \mathrm{C}$ |
| Maximum Junction Temperature (Note 3) | $150^{\circ} \mathrm{C}$ |
| Minimum ESD Rating (C = $100 \mathrm{pF}, \mathrm{R}=1.5 \mathrm{k} \Omega$ | 2 kV |

## Operating Ratings

| Supply Voltage | $4 \mathrm{~V} \leq \mathrm{V}_{I N} \leq 40 \mathrm{~V}$ |
| :--- | ---: |
| Output Switch Voltage | $0 \mathrm{~V} \leq \mathrm{V}_{\text {SW }} \leq 60 \mathrm{~V}$ |
| Output Switch Current | $\mathrm{ISW}^{2} \leq 5.0 \mathrm{~A}$ |
| Junction Temperature Range | $-40^{\circ} \mathrm{C} \leq \mathrm{TJ}_{\mathrm{J}} \leq+125^{\circ} \mathrm{C}$ |

## Electrical Characteristics

Specifications with standard type face are for $T_{J}=25^{\circ} \mathrm{C}$, and those in bold type face apply over full Operating Temperature Range. Unless otherwise specified, $\mathrm{V}_{\mathrm{IN}}=5 \mathrm{~V}$.

## LM2587-3.3

| Symbol | Parameters | Conditions | Typical | Min | Max | Units |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| SYSTEM PARAMETERS Test Circuit of Figure 2 (Note 4) |  |  |  |  |  |  |
| V OUT | Output Voltage | $\begin{aligned} & \mathrm{V}_{\mathrm{IN}}=4 \mathrm{~V} \text { to } 12 \mathrm{~V} \\ & \mathrm{I}_{\mathrm{LOAD}}=400 \mathrm{~mA} \text { to } 1.75 \mathrm{~A} \end{aligned}$ | 3.3 | 3.17/3.14 | 3.43/3.46 | V |
| $\Delta V_{\text {OUT }} /$ <br> $\Delta \mathrm{V}_{\mathrm{IN}}$ | Line Regulation | $\begin{aligned} & \mathrm{V}_{\mathrm{IN}}=4 \mathrm{~V} \text { to } 12 \mathrm{~V} \\ & \mathrm{I}_{\mathrm{LOAD}}=400 \mathrm{~mA} \end{aligned}$ | 20 |  | 50/100 | mV |
| $\Delta \mathrm{V}_{\text {OUT }} /$ <br> $\Delta I_{\text {LOAD }}$ | Load Regulation | $\begin{aligned} & \mathrm{V}_{\mathrm{IN}}=12 \mathrm{~V} \\ & \mathrm{I}_{\mathrm{LOAD}}=400 \mathrm{~mA} \text { to } 1.75 \mathrm{~A} \end{aligned}$ | 20 |  | 50/100 | mV |
| $\eta$ | Efficiency | $\mathrm{V}_{\text {IN }}=12 \mathrm{~V}, \mathrm{I}_{\text {LOAD }}=1 \mathrm{~A}$ | 75 |  |  | \% |
| UNIQUE DEVICE PARAMETERS (Note 5) |  |  |  |  |  |  |
| $V_{\text {REF }}$ | Output Reference Voltage | Measured at Feedback Pin $\mathrm{V}_{\mathrm{COMP}}=1.0 \mathrm{~V}$ | 3.3 | 3.242/3.234 | 3.358/3.366 | V |
| $\Delta \mathrm{V}_{\text {REF }}$ | Reference Voltage Line Regulation | $\mathrm{V}_{\mathrm{IN}}=4 \mathrm{~V}$ to 40 V | 2.0 |  |  | mV |
| $\mathrm{G}_{\mathrm{M}}$ | Error Amp <br> Transconductance | $\begin{aligned} & \mathrm{I}_{\mathrm{COMP}}=-30 \mu \mathrm{~A} \text { to }+30 \mu \mathrm{~A} \\ & \mathrm{~V}_{\mathrm{COMP}}=1.0 \mathrm{~V} \end{aligned}$ | 1.193 | 0.678 | 2.259 | mmho |
| Avol | Error Amp <br> Voltage Gain | $\begin{aligned} & \mathrm{V}_{\mathrm{COMP}}=0.5 \mathrm{~V} \text { to } 1.6 \mathrm{~V} \\ & \left.\mathrm{R}_{\mathrm{COMP}}=1.0 \mathrm{M} \Omega \text { (Note } 6\right) \end{aligned}$ | 260 | 151/75 |  | V/V |

LM2587-5.0

| Symbol | Parameters | Conditions | Typical | Min | Max | Units |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| SYSTEM PARAMETERS Test Circuit of Figure 2 (Note 4) |  |  |  |  |  |  |
| V OUT | Output Voltage | $\begin{aligned} & \mathrm{V}_{\mathrm{IN}}=4 \mathrm{~V} \text { to } 12 \mathrm{~V} \\ & \mathrm{I}_{\mathrm{LOAD}}=500 \mathrm{~mA} \text { to } 1.45 \mathrm{~A} \end{aligned}$ | 5.0 | 4.80/4.75 | 5.20/5.25 | V |
| $\Delta \mathrm{V}_{\text {OUT }} /$ <br> $\Delta V_{\text {IN }}$ | Line Regulation | $\begin{aligned} & \mathrm{V}_{\mathrm{IN}}=4 \mathrm{~V} \text { to } 12 \mathrm{~V} \\ & \mathrm{I}_{\mathrm{LOAD}}=500 \mathrm{~mA} \end{aligned}$ | 20 |  | 50/100 | mV |
| $\Delta \mathrm{V}_{\text {OUT }} /$ <br> $\Delta$ LOAD | Load Regulation | $\begin{aligned} & \mathrm{V}_{\mathrm{IN}}=12 \mathrm{~V} \\ & \mathrm{I}_{\text {LOAD }}=500 \mathrm{~mA} \text { to } 1.45 \mathrm{~A} \end{aligned}$ | 20 |  | 50/100 | mV |
| $\eta$ | Efficiency | $\mathrm{V}_{\text {IN }}=12 \mathrm{~V}, \mathrm{I}_{\text {LOAD }}=750 \mathrm{~mA}$ | 80 |  |  | \% |

## Electrical Characteristics

Specifications with standard type face are for $\mathrm{T}_{J}=25^{\circ} \mathrm{C}$, and those in bold type face apply over full Operating Temperature Range. Unless otherwise specified, $\mathrm{V}_{\mathrm{IN}}=5 \mathrm{~V}$. (Continued)
LM2587-5.0 (Continued)

| Symbol | Parameters | Conditions | Typical | Min | Max | Units |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| UNIQUE DEVICE PARAMETERS (Note 5) |  |  |  |  |  |  |
| $V_{\text {REF }}$ | Output Reference Voltage | Measured at Feedback Pin $\mathrm{V}_{\mathrm{COMP}}=1.0 \mathrm{~V}$ | 5.0 | 4.913/4.900 | 5.088/5.100 | V |
| $\Delta V_{\text {REF }}$ | Reference Voltage Line Regulation | $\mathrm{V}_{\mathrm{IN}}=4 \mathrm{~V}$ to 40 V | 3.3 |  |  | mV |
| $\mathrm{G}_{\mathrm{M}}$ | Error Amp <br> Transconductance | $\begin{aligned} & \mathrm{I}_{\mathrm{COMP}}=-30 \mu \mathrm{~A} \text { to }+30 \mu \mathrm{~A} \\ & \mathrm{~V}_{\mathrm{COMP}}=1.0 \mathrm{~V} \end{aligned}$ | 0.750 | 0.447 | 1.491 | mmho |
| Avol | Error Amp Voltage Gain | $\begin{aligned} & \mathrm{V}_{\mathrm{COMP}}=0.5 \mathrm{~V} \text { to } 1.6 \mathrm{~V} \\ & \mathrm{R}_{\mathrm{COMP}}=1.0 \mathrm{M} \Omega \text { (Note } 6 \text { ) } \end{aligned}$ | 165 | 99/49 |  | V/V |

## LM2587-12

| Symbol | Parameters | Conditions | Typical | Min | Max | Units |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| SYSTEM PARAMETERS Test Circuit of Figure 3 (Note 4) |  |  |  |  |  |  |
| $\mathrm{V}_{\text {OUT }}$ | Output Voltage | $\begin{aligned} & V_{I N}=4 \mathrm{~V} \text { to } 10 \mathrm{~V} \\ & \mathrm{I}_{\text {LOAD }}=300 \mathrm{~mA} \text { to } 1.2 \mathrm{~A} \end{aligned}$ | 12.0 | 11.52/11.40 | 12.48/12.60 | V |
| $\begin{aligned} & \Delta \mathrm{V}_{\text {OUT }} / \\ & \Delta \mathrm{V}_{\text {IN }} \end{aligned}$ | Line Regulation | $\begin{aligned} & \mathrm{V}_{I N}=4 \mathrm{~V} \text { to } 10 \mathrm{~V} \\ & \mathrm{I}_{\text {LOAD }}=300 \mathrm{~mA} \\ & \hline \end{aligned}$ | 20 |  | 100/200 | mV |
| $\Delta \mathrm{V}_{\text {OUT }} /$ <br> $\Delta$ loAd $^{\text {LOAD }}$ | Load Regulation | $\begin{aligned} & \mathrm{V}_{I N}=10 \mathrm{~V} \\ & \mathrm{I}_{\text {LOAD }}=300 \mathrm{~mA} \text { to } 1.2 \mathrm{~A} \end{aligned}$ | 20 |  | 100/200 | mV |
| $\eta$ | Efficiency | $\mathrm{V}_{\text {IN }}=10 \mathrm{~V}, \mathrm{I}_{\text {LOAD }}=1 \mathrm{~A}$ | 90 |  |  | \% |
| UNIQUE DEVICE PARAMETERS (Note 5) |  |  |  |  |  |  |
| $V_{\text {REF }}$ | Output Reference Voltage | Measured at Feedback Pin $\mathrm{V}_{\mathrm{COMP}}=1.0 \mathrm{~V}$ | 12.0 | 11.79/11.76 | 12.21/12.24 | V |
| $\Delta V_{\text {REF }}$ | Reference Voltage Line Regulation | $\mathrm{V}_{\text {IN }}=4 \mathrm{~V}$ to 40 V | 7.8 |  |  | mV |
| $\mathrm{G}_{\mathrm{M}}$ | Error Amp <br> Transconductance | $\begin{aligned} & \mathrm{I}_{\mathrm{COMP}}=-30 \mu \mathrm{~A} \text { to }+30 \mu \mathrm{~A} \\ & \mathrm{~V}_{\mathrm{COMP}}=1.0 \mathrm{~V} \end{aligned}$ | 0.328 | 0.186 | 0.621 | mmho |
| $\mathrm{A}_{\mathrm{VOL}}$ | Error Amp <br> Voltage Gain | $\begin{aligned} & \mathrm{V}_{\mathrm{COMP}}=0.5 \mathrm{~V} \text { to } 1.6 \mathrm{~V} \\ & \mathrm{R}_{\mathrm{COMP}}=1.0 \mathrm{M} \Omega \text { (Note } 6 \text { ) } \end{aligned}$ | 70 | 41/21 |  | V/V |

LM2587-ADJ

| Symbol | Parameters | Conditions | Typical | Min | Max | Units |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| SYSTEM PARAMETERS Test Circuit of Figure 3 (Note 4) |  |  |  |  |  |  |
| V OUT | Output Voltage | $\begin{aligned} & \mathrm{V}_{\mathrm{IN}}=4 \mathrm{~V} \text { to } 10 \mathrm{~V} \\ & \mathrm{I}_{\text {LOAD }}=300 \mathrm{~mA} \text { to } 1.2 \mathrm{~A} \end{aligned}$ | 12.0 | 11.52/11.40 | 12.48/12.60 | V |
| $\Delta V_{\text {OUT }} /$ <br> $\Delta \mathrm{V}_{\mathrm{IN}}$ | Line Regulation | $\begin{aligned} & \mathrm{V}_{\mathrm{IN}}=4 \mathrm{~V} \text { to } 10 \mathrm{~V} \\ & \mathrm{I}_{\text {LOAD }}=300 \mathrm{~mA} \end{aligned}$ | 20 |  | 100/200 | mV |
| $\Delta \mathrm{V}_{\text {OUT }} /$ <br> $\Delta$ LOAD | Load Regulation | $\begin{aligned} & \mathrm{V}_{I N}=10 \mathrm{~V} \\ & \mathrm{I}_{\text {LOAD }}=300 \mathrm{~mA} \text { to } 1.2 \mathrm{~A} \end{aligned}$ | 20 |  | 100/200 | mV |
| $\eta$ | Efficiency | $\mathrm{V}_{\mathrm{IN}}=10 \mathrm{~V}, \mathrm{I}_{\text {LOAD }}=1 \mathrm{~A}$ | 90 |  |  | \% |

## Electrical Characteristics

Specifications with standard type face are for $T_{J}=25^{\circ} \mathrm{C}$, and those in bold type face apply over full Operating Temperature Range. Unless otherwise specified, $\mathrm{V}_{\mathrm{IN}}=5 \mathrm{~V}$. (Continued)
LM2587-ADJ (Continued)

| Symbol | Parameters | Conditions | Typical | Min | Max | Units |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| UNIQUE DEVICE PARAMETERS (Note 5) |  |  |  |  |  |  |
| $V_{\text {REF }}$ | Output Reference Voltage | Measured at Feedback Pin $\mathrm{V}_{\mathrm{COMP}}=1.0 \mathrm{~V}$ | 1.230 | 1.208/1.205 | 1.252/1.255 | V |
| $\Delta \mathrm{V}_{\text {REF }}$ | Reference Voltage Line Regulation | $\mathrm{V}_{\mathrm{IN}}=4 \mathrm{~V}$ to 40 V | 1.5 |  |  | mV |
| $\mathrm{G}_{\mathrm{M}}$ | Error Amp <br> Transconductance | $\begin{aligned} & \mathrm{I}_{\mathrm{COMP}}=-30 \mu \mathrm{~A} \text { to }+30 \mu \mathrm{~A} \\ & \mathrm{~V}_{\text {COMP }}=1.0 \mathrm{~V} \end{aligned}$ | 3.200 | 1.800 | 6.000 | mmho |
| Avol | Error Amp <br> Voltage Gain | $\begin{aligned} & \mathrm{V}_{\mathrm{COMP}}=0.5 \mathrm{~V} \text { to } 1.6 \mathrm{~V} \\ & \left.\mathrm{R}_{\mathrm{COMP}}=1.0 \mathrm{M} \Omega \text { (Note } 6\right) \end{aligned}$ | 670 | 400/200 |  | V/V |
| $\mathrm{I}_{\mathrm{B}}$ | Error Amp Input Bias Current | $\mathrm{V}_{\text {COMP }}=1.0 \mathrm{~V}$ | 125 |  | 425/600 | nA |

COMMON DEVICE PARAMETERS for all versions (Note 5)

| Symbol | Parameters | Conditions | Typical | Min | Max | Units |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| Is | Input Supply Current | (Switch Off) (Note 8) | 11 |  | 15.5/16.5 | mA |
|  |  | $\mathrm{I}_{\text {SWITCH }}=3.0 \mathrm{~A}$ | 85 | 140 | 165 | mA |
| Vuv | Input Supply Undervoltage Lockout | $R_{\text {LOAD }}=100 \Omega$ | 3.30 | 3.05 | 3.75 | V |
| $\mathrm{f}_{0}$ | Oscillator Frequency | Measured at Switch Pin $\begin{aligned} & R_{\text {LOAD }}=100 \Omega \\ & \mathrm{~V}_{\mathrm{COMP}}=1.0 \mathrm{~V} \end{aligned}$ | 100 | 85/75 | 115/125 | kHz |
| $\mathrm{f}_{\text {SC }}$ | Short-Circuit <br> Frequency | Measured at Switch Pin <br> $R_{\text {LOAD }}=100 \Omega$ <br> $\mathrm{V}_{\text {FEEDBACK }}=1.15 \mathrm{~V}$ | 25 |  |  | kHz |
| $\mathrm{V}_{\text {EAO }}$ | Error Amplifier Output Swing | Upper Limit (Note 7) | 2.8 | 2.6/2.4 |  | V |
|  |  | Lower Limit (Note 8) | 0.25 |  | 0.40/0.55 | V |
| IEAO | Error Amp Output Current (Source or Sink) | (Note 9) | 165 | 110/70 | 260/320 | $\mu \mathrm{A}$ |
| Iss | Soft Start Current | $\begin{aligned} & \mathrm{V}_{\text {FEEDBACK }}=0.92 \mathrm{~V} \\ & \mathrm{~V}_{\text {COMP }}=1.0 \mathrm{~V} \end{aligned}$ | 11.0 | 8.0/7.0 | 17.0/19.0 | $\mu \mathrm{A}$ |
| D | Maximum Duty Cycle | $\begin{aligned} & \mathrm{R}_{\text {LOAD }}=100 \Omega \\ & \text { (Note 7) } \end{aligned}$ | 98 | 93/90 |  | \% |
| $I_{L}$ | Switch Leakage Current | Switch Off $V_{\text {SWITCH }}=60 \mathrm{~V}$ | 15 |  | 300/600 | $\mu \mathrm{A}$ |
| V ${ }_{\text {SUS }}$ | Switch Sustaining Voltage | $\mathrm{dV} / \mathrm{dT}=1.5 \mathrm{~V} / \mathrm{ns}$ |  | 65 |  | V |
| $\mathrm{V}_{\text {SAT }}$ | Switch Saturation Voltage | $\mathrm{ISWITCH}=5.0 \mathrm{~A}$ | 0.7 |  | 1.1/1.4 | V |
| $\mathrm{I}_{\mathrm{CL}}$ | NPN Switch Current Limit |  | 6.5 | 5.0 | 9.5 | A |

## Electrical Characteristics

Specifications with standard type face are for $\mathrm{T}_{J}=25^{\circ} \mathrm{C}$, and those in bold type face apply over full Operating Temperature Range. Unless otherwise specified, $\mathrm{V}_{\mathrm{IN}}=5 \mathrm{~V}$. (Continued)
COMMON DEVICE PARAMETERS (Note 4) (Continued)

| Symbol | Parameters | Conditions | Typical | Min | Max | Units |
| :--- | :---: | :---: | :---: | :---: | :---: | :---: |
| $\theta_{\text {JA }}$ | Thermal Resistance | T Package, Junction to Ambient (Note 10) | 65 |  |  |  |
| $\theta_{\text {JA }}$ |  | T Package, Junction to Ambient (Note 11) | 45 |  |  |  |
| $\theta_{\text {JC }}$ |  | T Package, Junction to Case | 2 |  |  |  |
| $\theta_{\text {JA }}$ |  | S Package, Junction to Ambient (Note 12) | 56 |  |  | ${ }^{\circ} \mathrm{C} / \mathrm{W}$ |
| $\theta_{\text {JA }}$ |  | S Package, Junction to Ambient (Note 13) | 35 |  |  |  |
| $\theta_{\text {JA }}$ |  | S Package, Junction to Ambient (Note 14) | 26 |  |  |  |
| $\theta_{\text {JC }}$ |  | S Package, Junction to Case | 2 |  |  |  |

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating ratings indicate conditions the device is intended to be functional, but device parameter specifications may not be guaranteed under these conditions. For guaranteed specifications and test conditions, see the Electrical Characteristics.
Note 2: Note that switch current and output current are not identical in a step-up regulator. Output current cannot be internally limited when the LM2587 is used as a step-up regulator. To prevent damage to the switch, the output current must be externally limited to 5A. However, output current is internally limited when the LM2587 is used as a flyback regulator (see the Application Hints section for more information).
Note 3: The junction temperature of the device ( $\left.T_{J}\right)$ is a function of the ambient temperature ( $T_{A}$ ), the junction-to-ambient thermal resistance $\left(\theta_{\mathrm{JA}}\right)$, and the power dissipation of the device ( $P_{D}$ ). A thermal shutdown will occur if the temperature exceeds the maximum junction temperature of the device: $P_{D} \times \theta_{\mathrm{JA}}+T_{A(M A X)} \geq$ $T_{J(M A X)}$. For a safe thermal design, check that the maximum power dissipated by the device is less than: $\left.P_{D} \leq\left[T_{J(M A X)}-T_{A(M A X)}\right)\right] / \theta_{J A}$. When calculating the maximum allowable power dissipation, derate the maximum junction temperature-this ensures a margin of safety in the thermal design.
Note 4: External components such as the diode, inductor, input and output capacitors can affect switching regulator performance. When the LM2587 is used as shown in Figures 2 and 3, system performance will be as specified by the system parameters.
Note 5: All room temperature limits are $100 \%$ production tested, and all limits at temperature extremes are guaranteed via correlation using standard Statistical Quality Control (SQC) methods.
Note 6: A $1.0 \mathrm{M} \Omega$ resistor is connected to the compensation pin (which is the error amplifier output) to ensure accuracy in measuring AvoL-
Note 7: To measure this parameter, the feedback voltage is set to a low value, depending on the output version of the device, to force the error amplifier output high. Adj: $\mathrm{V}_{\mathrm{FB}}=1.05 \mathrm{~V} ; 3.3 \mathrm{~V}: \mathrm{V}_{\mathrm{FB}}=2.81 \mathrm{~V} ; 5.0 \mathrm{~V}: \mathrm{V}_{\mathrm{FB}}=4.25 \mathrm{~V} ; 12 \mathrm{~V}: \mathrm{V}_{\mathrm{FB}}=10.20 \mathrm{~V}$.
Note 8: To measure this parameter, the feedback voltage is set to a high value, depending on the output version of the device, to force the error amplifier output low. Adj: $\mathrm{V}_{\mathrm{FB}}=1.41 \mathrm{~V} ; 3.3 \mathrm{~V}: \mathrm{V}_{\mathrm{FB}}=3.80 \mathrm{~V} ; 5.0 \mathrm{~V}: \mathrm{V}_{\mathrm{FB}}=5.75 \mathrm{~V} ; 12 \mathrm{~V}: \mathrm{V}_{\mathrm{FB}}=13.80 \mathrm{~V}$.
Note 9: To measure the worst-case error amplifier output current, the LM2587 is tested with the feedback voltage set to its low value (specified in Note 7) and at its high value (specified in Note 8).
Note 10: Junction to ambient thermal resistance (no external heat sink) for the 5 lead TO-220 package mounted vertically, with $1 / 2$ inch leads in a socket, or on a PC board with minimum copper area.
Note 11: Junction to ambient thermal resistance (no external heat sink) for the 5 lead TO-220 package mounted vertically, with $1 / 2$ inch leads soldered to a PC board containing approximately 4 square inches of (10z.) copper area surrounding the leads.
Note 12: Junction to ambient thermal resistance for the 5 lead TO-263 mounted horizontally against a PC board area of 0.136 square inches (the same size as the TO-263 package) of 1 oz . ( 0.0014 in. thick) copper.
Note 13: Junction to ambient thermal resistance for the 5 lead TO-263 mounted horizontally against a PC board area of 0.4896 square inches ( 3.6 times the area of the TO-263 package) of 1 oz. ( 0.0014 in. thick) copper.
Note 14: Junction to ambient thermal resistance for the 5 lead TO-263 mounted horizontally against a PC board copper area of 1.0064 square inches ( 7.4 times the area of the TO-263 package) of 1 oz . ( 0.0014 in . thick) copper. Additional copper area will reduce thermal resistance further. See the thermal model in Switchers Made Simple ${ }^{\circledR}$ software.

Typical Performance Characteristics










$\Delta$ Reference Voltage vs Supply Voltage



## Connection Diagrams

| Bent, Staggered Leads 5-Lead TO-220 (T) Top View |
| :---: |
|  |
| Order |
| 5-Lead TO-263 (S) Top View |
|  |
| Order Number LM2587S-3.3, LM2587S-5.0, LM2587S-12 or LM2587S-ADJ See NS Package Number TS5B |

## Block Diagram




## Flyback Regulator Operation

The LM2587 is ideally suited for use in the flyback regulator topology. The flyback regulator can produce a single output voltage, such as the one shown in Figure 4, or multiple output voltages. In Figure 4, the flyback regulator generates an output voltage that is inside the range of the input voltage. This feature is unique to flyback regulators and cannot be duplicated with buck or boost regulators.
The operation of a flyback regulator is as follows (refer to Figure 4): when the switch is on, current flows through the primary winding of the transformer, T1, storing energy in the magnetic field of the transformer. Note that the primary and secondary windings are out of phase, so no current flows through the secondary when current flows through the primary. When the switch turns off, the magnetic field col-
lapses, reversing the voltage polarity of the primary and secondary windings. Now rectifier D1 is forward biased and current flows through it, releasing the energy stored in the transformer. This produces voltage at the output.
The output voltage is controlled by modulating the peak switch current. This is done by feeding back a portion of the output voltage to the error amp, which amplifies the difference between the feedback voltage and a 1.230 V reference. The error amp output voltage is compared to a ramp voltage proportional to the switch current (i.e., inductor current during the switch on time). The comparator terminates the switch on time when the two voltages are equal, thereby controlling the peak switch current to maintain a constant output voltage.


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As shown in Figure 4, the LM2587 can be used as a flyback regulator by using a minimum number of external components. The switching waveforms of this regulator are shown in Figure 5. Typical Performance Characteristics observed during the operation of this circuit are shown in Figure 6.

FIGURE 4. 12V Flyback Regulator Design Example

## Typical Performance Characteristics



## Typical Flyback Regulator Applications

Figures 7 through 12 show six typical flyback applications, varying from single output to triple output. Each drawing contains the part number(s) and manufacturer(s) for every component except the transformer. For the transformer part numbers and manufacturers names, see the table in

Figure 13. For applications with different output voltagesrequiring the LM2587-ADJ—or different output configurations that do not match the standard configurations, refer to the Switchers Made Simple ${ }^{\circledR}$ software.


FIGURE 7. Single-Output Flyback Regulator


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## Typical Flyback Regulator Applications (Continued)



FIGURE 9. Single-Output Flyback Regulator


FIGURE 10. Dual-Output Flyback Regulator

## Typical Flyback Regulator Applications (Continued)



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FIGURE 11. Dual-Output Flyback Regulator


TL/H/12316-18
FIGURE 12. Triple-Output Flyback Regulator

| Typical Flyback Regulator Applications (Continued) <br> Transformer Selection (T) <br> Figure 13 lists the standard transformers available for flyback regulator applications. Included in the table are the turns ratio(s) for each transformer, as well as the output voltages, input voltage ranges, and the maximum load currents for each circuit. |  |  |  |  |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| Applications | Figure 7 | Figure 8 | Figure 9 | Figure 10 | Figure 11 | Figure 12 |
| Transformers | T1 | T1 | T1 | T2 | T3 | T4 |
| $\mathrm{V}_{\text {IN }}$ | 4V-6V | $4 \mathrm{~V}-6 \mathrm{~V}$ | 8V-16V | 4V-6V | 18V-36V | 18V-36V |
| $\mathrm{V}_{\text {OUT1 }}$ | 3.3 V | 5 V | 12 V | 12 V | 12 V | 5 V |
| lout1 (Max) | 1.8 A | 1.4A | 1.2A | 0.3A | 1A | 2.5A |
| $\mathrm{N}_{1}$ | 1 | 1 | 1 | 2.5 | 0.8 | 0.35 |
| $\mathrm{V}_{\text {OUT2 }}$ |  |  |  | -12V | -12V | 12 V |
| IOUT2 (Max) |  |  |  | 0.3 A | 1A | 0.5A |
| $\mathrm{N}_{2}$ |  |  |  | 2.5 | 0.8 | 0.8 |
| $\mathrm{V}_{\text {OUT3 }}$ |  |  |  |  |  | -12V |
| IOUT3 (Max) |  |  |  |  |  | 0.5A |
| $\mathrm{N}_{3}$ |  |  |  |  |  | 0.8 |
| FIGURE 13. Transformer Selection Table |  |  |  |  |  |  |
| Transformer Type | Manufacturers' Part Numbers |  |  |  |  |  |
|  | Coilcraft ${ }^{1}$ | Coil <br> Surfac |  | Pulse ${ }^{2}$ <br> Surface Mount | Renco ${ }^{3}$ | Schott ${ }^{4}$ |
| T1 | Q4434-B | Q4 |  | PE-68411 | RL-5530 | 67141450 |
| T2 | Q4337-B | Q4 |  | PE-68412 | RL-5531 | 67140860 |
| T3 | Q4343-B |  |  | PE-68421 | RL-5534 | 67140920 |
| T4 | Q4344-B |  |  | PE-68422 | RL-5535 | 67140930 |
| Note 1: Coilcraft Inc., Phone: $(800) 322-2645$ <br> 1102 Silver Lake Road, Cary, IL 60013 Fax: (708) 639-1469 |  |  |  |  |  |  |
| Note 2: Pulse Engineering Inc., <br> 12220 World Trade Drive, San Diego, CA 92128 |  |  |  | Phone: (619) 674-8100Fax: (619) 674-8262 |  |  |
| Note 3: Renco Electronics Inc., 60 Jeffryn Blvd. East, Deer Park, NY 11729 |  |  |  | Phone: (800) 645-5828 <br> Fax: (516) 586-5562 |  |  |
| Note 4: Schott Corp., 1000 Parkers Lane Road, Wayzata, MN 55391 |  |  |  | Phone: (612) 475-1173 <br> Fax: (612) 475-1786 |  |  |
| FIGURE 14. Transformer Manufacturer Guide |  |  |  |  |  |  |





## Step-Up (Boost) Regulator Operation

Figure 33 shows the LM2587 used as a step-up (boost) regulator. This is a switching regulator that produces an output voltage greater than the input supply voltage.
A brief explanation of how the LM2587 Boost Regulator works is as follows (refer to Figure 33). When the NPN switch turns on, the inductor current ramps up at the rate of $\mathrm{V}_{\mathrm{IN}} / \mathrm{L}$, storing energy in the inductor. When the switch turns
off, the lower end of the inductor flies above $\mathrm{V}_{\mathrm{IN}}$, discharging its current through diode (D) into the output capacitor (COUT) at a rate of $\left(\mathrm{V}_{\text {OUT }}-\mathrm{V}_{\text {IN }}\right) / \mathrm{L}$. Thus, energy stored in the inductor during the switch on time is transferred to the output during the switch off time. The output voltage is controlled by adjusting the peak switch current, as described in the flyback regulator section.


TL/H/12316-19 By adding a small number of external components (as shown in Figure 33), the LM2587 can be used to produce a regulated output voltage that is greater than the applied input voltage. The switching waveforms observed during the operation of this circuit are shown in Figure 34. Typical performance of this regulator is shown in Figure 35.

FIGURE 33. 12V Boost Regulator

## Typical Performance Characteristics



A: Switch Voltage, $10 \mathrm{~V} / \mathrm{div}$
B: Switch Current, $5 \mathrm{~A} / \mathrm{div}$
C: Inductor Current, $5 \mathrm{~A} / \mathrm{div}$
D: Output Ripple Voltage,
$100 \mathrm{mV} / \mathrm{div}$, AC-Coupled
Horizontal: $2 \mu \mathrm{~s} / \mathrm{div}$

FIGURE 34. Switching Waveforms


## Typical Boost Regulator Applications

Figures 36 and 38 through 40 show four typical boost appli-cations)-one fixed and three using the adjustable version of the LM2587. Each drawing contains the part number(s) and manufacturer(s) for every component. For the fixed 12 V
output application, the part numbers and manufacturers' names for the inductor are listed in a table in Figure 40. For applications with different output voltages, refer to the Switchers Made Simple ${ }^{\circledR}$ software.


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FIGURE 36. $+\mathbf{5 V}$ to $+\mathbf{1 2 V}$ Boost Regulator

Figure 37 contains a table of standard inductors, by part number and corresponding manufacturer, for the fixed output regulator of Figure 36.

| Coilcraft $^{\mathbf{1}}$ | Pulse $^{2}$ | Renco $^{3}$ | Schott $^{\mathbf{4}}$ |
| :---: | :---: | :---: | :---: |
| R4793-A | PE-53900 | RL-5472-5 | 67146520 |

Note 1: Coilcraft Inc.,
1102 Silver Lake Road, Cary, IL 60013
Phone: (800) 322-2645 Fax: (708) 639-1469
Note 2: Pulse Engineering Inc.,
Phone: (619) 674-8100
12220 World Trade Drive, San Diego, CA 92128
Note 3: Renco Electronics Inc.,
60 Jeffryn Blvd. East, Deer Park, NY 11729 Fax: (619) 674-8262 Note 4: Schott Corp., hone: (800) 645-5828 Fax: (516) 586-5562

1000 Parkers Lane Road, Wayzata, MN 55391
Fax: (612) 475-1786
FIGURE 37. Inductor Selection Table

## Typical Boost Regulator Applications (Continued)



FIGURE 38. $+\mathbf{1 2 V}$ to $+24 V$ Boost Regulator


FIGURE 39. +24 V to +36 V Boost Regulator


FIGURE 40. +24 V to +48 V Boost Regulator
*The LM2587 will require a heat sink in these applications. The size of the heat sink will depend on the maximum ambient temperature. To calculate the thermal resistance of the IC and the size of the heat sink needed, see the "Heat Sink/Thermal Considerations" section in the Application Hints.

## Application Hints



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FIGURE 41. Boost Regulator

PROGRAMMING OUTPUT VOLTAGE
(SELECTING $\mathrm{R}_{1}$ AND $\mathrm{R}_{2}$ )
Referring to the adjustable regulator in Figure 41, the output voltage is programmed by the resistors $R_{1}$ and $R_{2}$ by the following formula:

$$
V_{\text {OUT }}=V_{\text {REF }}\left(1+R_{1} / R_{2}\right) \quad \text { where } V_{\text {REF }}=1.23 V
$$

Resistors $R_{1}$ and $R_{2}$ divide the output voltage down so that it can be compared with the 1.23 V internal reference. With $R_{2}$ between $1 k$ and $5 k, R_{1}$ is:

$$
R_{1}=R_{2}\left(V_{\text {OUT }} / V_{\text {REF }}-1\right) \quad \text { where } V_{R E F}=1.23 V
$$

For best temperature coefficient and stability with time, use $1 \%$ metal film resistors.

## SHORT CIRCUIT CONDITION

Due to the inherent nature of boost regulators, when the output is shorted (see Figure 41), current flows directly from the input, through the inductor and the diode, to the output, bypassing the switch. The current limit of the switch does not limit the output current for the entire circuit. To protect the load and prevent damage to the switch, the current must be externally limited, either by the input supply or at the out-
put with an external current limit circuit. The external limit should be set to the maximum switch current of the device, which is 5 A .
In a flyback regulator application (Figure 42), using the standard transformers, the LM2587 will survive a short circuit to the main output. When the output voltage drops to $80 \%$ of its nominal value, the frequency will drop to 25 kHz . With a lower frequency, off times are larger. With the longer off times, the transformer can release all of its stored energy before the switch turns back on. Hence, the switch turns on initially with zero current at its collector. In this condition, the switch current limit will limit the peak current, saving the device.

## FLYBACK REGULATOR INPUT CAPACITORS

A flyback regulator draws discontinuous pulses of current from the input supply. Therefore, there are two input capacitors needed in a flyback regulator; one for energy storage and one for filtering (see Figure 42). Both are required due to the inherent operation of a flyback regulator. To keep a stable or constant voltage supply to the LM2587, a stor-


FIGURE 42. Flyback Regulator

## Application Hints (Continued)

age capacitor ( $2100 \mu \mathrm{~F}$ ) is required. If the input source is a recitified DC supply and/or the application has a wide temperature range, the required rms current rating of the capacitor might be very large. This means a larger value of capacitance or a higher voltage rating will be needed of the input capacitor. The storage capacitor will also attenuate noise which may interfere with other circuits connected to the same input supply voltage.
In addition, a small bypass capacitor is required due to the noise generated by the input current pulses. To eliminate the noise, insert a $1.0 \mu \mathrm{~F}$ ceramic capacitor between $\mathrm{V}_{\mathrm{IN}}$ and ground as close as possible to the device.

## SWITCH VOLTAGE LIMITS

In a flyback regulator, the maximum steady-state voltage appearing at the switch, when it is off, is set by the transformer turns ratio, N , the output voltage, $\mathrm{V}_{\text {OUT }}$, and the maximum input voltage, $\mathrm{V}_{\mathrm{IN}}($ Max):

$$
\mathrm{V}_{\mathrm{SW}(\mathrm{OFF})}=\mathrm{V}_{\mathrm{IN}}(\mathrm{Max})+\left(\mathrm{V}_{\mathrm{OUT}}+\mathrm{V}_{\mathrm{F}}\right) / \mathrm{N}
$$

where $V_{F}$ is the forward biased voltage of the output diode, and is 0.5 V for Schottky diodes and 0.8 V for ultra-fast recovery diodes (typically). In certain circuits, there exists a voltage spike, $\mathrm{V}_{\mathrm{LL}}$, superimposed on top of the steady-state voltage (see Figure 5, waveform A). Usually, this voltage spike is caused by the transformer leakage inductance and/ or the output rectifier recovery time. To "clamp" the voltage at the switch from exceeding its maximum value, a transient suppressor in series with a diode is inserted across the transformer primary (as shown in the circuit on the front page and other flyback regulator circuits throughout the datasheet). The schematic in Figure 42 shows another method of clamping the switch voltage. A single voltage transient suppressor (the SA51A) is inserted at the switch pin. This method clamps the total voltage across the switch, not just the voltage across the primary.
If poor circuit layout techniques are used (see the "Circuit Layout Guideline" section), negative voltage transients may appear on the Switch pin (pin 4). Applying a negative voltage (with respect to the IC's ground) to any monolithic IC pin causes erratic and unpredictable operation of that IC. This holds true for the LM2587 IC as well. When used in a flyback regulator, the voltage at the Switch pin (pin 4) can go negative when the switch turns on. The "ringing" voltage at the switch pin is caused by the output diode capacitance and the transformer leakage inductance forming a resonant circuit at the secondary(ies). The resonant circuit generates the "ringing" voltage, which gets reflected back through the transformer to the switch pin. There are two common methods to avoid this problem. One is to add an RC snubber around the output rectifier(s), as in Figure 42. The values of the resistor and the capacitor must be chosen so that the voltage at the Switch pin does not drop below -0.4 V . The resistor may range in value between $10 \Omega$ and $1 \mathrm{k} \Omega$, and the capacitor will vary from $0.001 \mu \mathrm{~F}$ to $0.1 \mu \mathrm{~F}$. Adding a snubber will (slightly) reduce the efficiency of the overall circuit. The other method to reduce or eliminate the "ringing" is to insert a Schottky diode clamp between pins 4 and 3 (ground), also shown in Figure 42. This prevents the voltage at pin 4 from dropping below -0.4 V . The reverse voltage rating of the diode must be greater than the switch off voltage.


FIGURE 43. Input Line Filter

## OUTPUT VOLTAGE LIMITATIONS

The maximum output voltage of a boost regulator is the maximum switch voltage minus a diode drop. In a flyback regulator, the maximum output voltage is determined by the turns ratio, N , and the duty cycle, D , by the equation:

$$
V_{\text {OUT }} \approx N \times V_{\text {IN }} \times D /(1-D)
$$

The duty cycle of a flyback regulator is determined by the following equation:

$$
\mathrm{D}=\frac{\mathrm{V}_{\mathrm{OUT}}+\mathrm{V}_{\mathrm{F}}}{\mathrm{~N}\left(\mathrm{~V}_{\text {IN }}-\mathrm{V}_{\mathrm{SAT}}\right)+\mathrm{V}_{\text {OUT }}+\mathrm{V}_{\mathrm{F}}} \approx \frac{\mathrm{~V}_{\mathrm{OUT}}}{\mathrm{~N}\left(\mathrm{~V}_{\mathrm{IN}}\right)+\mathrm{V}_{\mathrm{OUT}}}
$$

Theoretically, the maximum output voltage can be as large as desired-just keep increasing the turns ratio of the transformer. However, there exists some physical limitations that prevent the turns ratio, and thus the output voltage, from increasing to infinity. The physical limitations are capacitances and inductances in the LM2587 switch, the output diode(s), and the transformer-such as reverse recovery time of the output diode (mentioned above).

## NOISY INPUT LINE CONDITION)

A small, low-pass RC filter should be used at the input pin of the LM2587 if the input voltage has an unusual large amount of transient noise, such as with an input switch that bounces. The circuit in Figure 43 demonstrates the layout of the filter, with the capacitor placed from the input pin to ground and the resistor placed between the input supply and the input pin. Note that the values of $\mathrm{R}_{I N}$ and $\mathrm{C}_{I N}$ shown in the schematic are good enough for most applications, but some readjusting might be required for a particular application. If efficiency is a major concern, replace the resistor with a small inductor (say $10 \mu \mathrm{H}$ and rated at 100 mA ).

## STABILITY

All current-mode controlled regulators can suffer from an instability, known as subharmonic oscillation, if they operate with a duty cycle above $50 \%$. To eliminate subharmonic oscillations, a minimum value of inductance is required to ensure stability for all boost and flyback regulators. The minimum inductance is given by:
$\mathrm{L}(\mathrm{Min})=\frac{2.92\left[\left(\mathrm{~V}_{\text {IN }}(\mathrm{Min})-\mathrm{V}_{\text {SAT }}\right) \times(2 \mathrm{D}(\mathrm{Max})-1)\right]}{1-\mathrm{D}(\mathrm{Max})}(\mu \mathrm{H})$
where $\mathrm{V}_{\text {SAT }}$ is the switch saturation voltage and can be found in the Characteristic Curves.

## Application Hints (Continued)



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FIGURE 44. Circuit Board Layout

## CIRCUIT LAYOUT GUIDELINES

As in any switching regulator, layout is very important. Rapidly switching currents associated with wiring inductance generate voltage transients which can cause problems. For minimal inductance and ground loops, keep the length of the leads and traces as short as possible. Use single point grounding or ground plane construction for best results. Separate the signal grounds from the power grounds (as indicated in Figure 44). When using the Adjustable version, physically locate the programming resistors as near the regulator IC as possible, to keep the sensitive feedback wiring short.

## HEAT SINK/THERMAL CONSIDERATIONS

In many cases, no heat sink is required to keep the LM2587 junction temperature within the allowed operating range. For each application, to determine whether or not a heat sink will be required, the following must be identified:

1) Maximum ambient temperature (in the application).
2) Maximum regulator power dissipation (in the application).
3) Maximum allowed junction temperature $\left(125^{\circ} \mathrm{C}\right.$ for the LM2587). For a safe, conservative design, a temperature approximately $15^{\circ} \mathrm{C}$ cooler than the maximum junction temperature should be selected $\left(110^{\circ} \mathrm{C}\right)$.
4) LM2587 package thermal resistances $\theta_{\mathrm{JA}}$ and $\theta_{\mathrm{JC}}$ (given in the Electrical Characteristics).
Total power dissipated ( $\mathrm{P}_{\mathrm{D}}$ ) by the LM2587 can be estimated as follows:
Boost:
$P_{D}=0.15 \Omega \times\left(\frac{I_{\text {LOAD }}}{1-D}\right)^{2} \times D+\frac{l_{\text {LOAD }}}{50 \times(1-D)} \times D \times V_{I N}$
Flyback:

$$
\begin{aligned}
\mathrm{P}_{\mathrm{D}}= & 0.15 \Omega \times\left(\frac{\mathrm{N} \times \Sigma \mathrm{I}_{\mathrm{LOAD}}}{1-\mathrm{D}}\right)^{2} \times \mathrm{D} \\
& +\frac{\mathrm{N} \times \Sigma I_{\mathrm{LOAD}}}{50 \times(1-\mathrm{D})} \times \mathrm{D} \times \mathrm{V}_{\mathrm{IN}}
\end{aligned}
$$

$\mathrm{V}_{\mathrm{IN}}$ is the minimum input voltage, $\mathrm{V}_{\text {OUT }}$ is the output voltage, N is the transformer turns ratio, D is the duty cycle, and $I_{\text {LOAD }}$ is the maximum load current (and $\Sigma I_{\text {LOAD }}$ is the sum of the maximum load currents for multiple-output flyback regulators). The duty cycle is given by:
Boost:

$$
\mathrm{D}=\frac{\mathrm{V}_{\mathrm{OUT}}+\mathrm{V}_{\mathrm{F}}-\mathrm{V}_{\text {IN }}}{\mathrm{V}_{\text {OUT }}+\mathrm{V}_{\mathrm{F}}-\mathrm{V}_{\mathrm{SAT}}} \approx \frac{\mathrm{~V}_{\text {OUT }}-\mathrm{V}_{\text {IN }}}{V_{\text {OUT }}}
$$

Flyback:

$$
\mathrm{D}=\frac{\mathrm{V}_{\mathrm{OUT}}+\mathrm{V}_{\mathrm{F}}}{\mathrm{~N}\left(\mathrm{~V}_{\text {IN }}-\mathrm{V}_{\mathrm{SAT}}\right)+\mathrm{V}_{\mathrm{OUT}}+\mathrm{V}_{\mathrm{F}}} \approx \frac{\mathrm{~V}_{\mathrm{OUT}}}{\mathrm{~N}\left(\mathrm{~V}_{\text {IN }}\right)+\mathrm{V}_{\mathrm{OUT}}}
$$

where $\mathrm{V}_{\mathrm{F}}$ is the forward biased voltage of the diode and is typically 0.5 V for Schottky diodes and 0.8 V for fast recovery diodes. $\mathrm{V}_{\text {SAT }}$ is the switch saturation voltage and can be found in the Characteristic Curves.
When no heat sink is used, the junction temperature rise is:

$$
\Delta T_{J}=P_{D} \times \theta_{J A}
$$

Adding the junction temperature rise to the maximum ambient temperature gives the actual operating junction temperature:

$$
T_{J}=\Delta T_{J}+T_{A} .
$$

If the operating junction temperature exceeds the maximum junction temperatue in item 3 above, then a heat sink is required. When using a heat sink, the junction temperature rise can be determined by the following:

$$
\Delta \mathrm{T}_{\mathrm{J}}=\mathrm{P}_{\mathrm{D}} \times\left(\theta_{\mathrm{JC}}+\theta_{\text {Interface }}+\theta_{\text {Heat Sink }}\right)
$$

Again, the operating junction temperature will be:

$$
\mathrm{T}_{\mathrm{J}}=\Delta \mathrm{T}_{\mathrm{J}}+\mathrm{T}_{\mathrm{A}}
$$

## Application Hints (Continued)

As before, if the maximum junction temperature is exceeded, a larger heat sink is required (one that has a lower thermal resistance).
Included in the Switchers Made Simple ${ }^{\circledR}$ design software is a more precise (non-linear) thermal model that can be used to determine junction temperature with different inputoutput parameters or different component values. It can also calculate the heat sink thermal resistance required to maintain the regulator junction temperature below the maximum operating temperature.
To further simplify the flyback regulator design procedure, National Semiconductor is making available computer design software. Switchers Made Simple ${ }^{\circledR}$ software is available on a ( $3^{1} 1 / 2^{\prime \prime}$ ) diskette for IBM compatable computers from a National Semiconductor sales office in your area or the National Semiconductor Customer Response Center (1-800-272-9959).

## European Magnetic Vendor Contacts

Please contact the following addresses for details of local distributors or representatives:

## Coilcraft

21 Napier Place Wardpark North
Cumbernauld, Scotland G68 0LL
Phone: +44 1236730595
Fax: +441236730627

## Pulse Engineering

Dunmore Road
Tuam
Co. Galway, Ireland
Phone: +353 9324107
Fax: + 3539324459

Physical Dimensions inches (millimeters)


Physical Dimensions inches (millimeters) (Continued)


## LIFE SUPPORT POLICY

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| :---: | :---: | :---: | :---: |

## LM2588 SIMPLE SWITCHER ${ }^{\circledR}$ 5A Flyback Regulator with Shutdown

## General Description

The LM2588 series of regulators are monolithic integrated circuits specifically designed for flyback, step-up (boost), and forward converter applications. The device is available in 4 different output voltage versions: $3.3 \mathrm{~V}, 5.0 \mathrm{~V}, 12 \mathrm{~V}$, and adjustable.
Requiring a minimum number of external components, these regulators are cost effective, and simple to use. Included in the datasheet are typical circuits of boost and flyback regulators. Also listed are selector guides for diodes and capacitors and a family of standard inductors and flyback transformers designed to work with these switching regulators.
The power switch is a 5.0A NPN device that can stand-off 65 V . Protecting the power switch are current and thermal limiting circuits, and an undervoltage lockout circuit. This IC contains an adjustable frequency oscillator that can be programmed up to 200 kHz . The oscillator can also be synchronized with other devices, so that multiple devices can operate at the same switching frequency.
Other features include soft start mode to reduce in-rush current during start up, and current mode control for improved rejection of input voltage and output load transients and cy-cle-by-cycle current limiting. The device also has a shutdown pin, so that it can be turned off externally. An output voltage tolerance of $\pm 4 \%$, within specified input voltages and output load conditions, is guaranteed for the power supply system.

## Features

- Requires few external components
- Family of standard inductors and transformers
- NPN output switches 5.0 A , can stand off 65 V

■ Wide input voltage range: 4 V to 40 V
■ Adjustable switching frequency: 100 kHz to 200 kHz

- External shutdown capability
- Draws less than $60 \mu \mathrm{~A}$ when shut down
- Frequency synchronization
- Current-mode operation for improved transient response, line regulation, and current limit
- Internal soft-start function reduces in-rush current during start-up
- Output transistor protected by current limit, under voltage lockout, and thermal shutdown
■ System output voltage tolerance of $\pm 4 \%$ max over line and load conditions

Typical Applications

- Flyback regulator
- Forward converter
- Multiple-output regulator
- Simple boost regulator

Flyback Regulator


TL/H/12420-1
Ordering Information

| Package Type | NSC Package <br> Drawing | Order Number |
| :--- | :---: | :---: |
| 7-Lead TO-220 Bent, Staggered Leads | TA07B | LM2588T-3.3, LM2588T-5.0, LM2588T-12, LM2588T-ADJ |
| 7-Lead TO-263 | TS7B | LM2588S-3.3, LM2588S-5.0, LM2588S-12, LM2588S-ADJ |
| 7-Lead TO-263 Tape and Reel | TS7B | LM2588SX-3.3, LM2588SX-5.0, LM2588SX-12, LM2588SX-ADJ |

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Absolute Maximum Ratings (Note 1)
If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

| Input Voltage | $-0.4 \mathrm{~V} \leq \mathrm{V}_{\text {IN }} \leq 45 \mathrm{~V}$ |
| :--- | ---: |
| Switch Voltage | $-0.4 \mathrm{~V} \leq \mathrm{V}_{\text {SW }} \leq 65 \mathrm{~V}$ |
| Switch Current (Note 2) | Internally Limited |
| Compensation Pin Voltage | $-0.4 \mathrm{~V} \leq \mathrm{V}_{\mathrm{COMP}} \leq 2.4 \mathrm{~V}$ |
| Feedback Pin Voltage | $-0.4 \mathrm{~V} \leq \mathrm{V}_{\mathrm{FB}} \leq 2 \mathrm{~V}_{\mathrm{OUT}}$ |
| $\overline{\text { ON/OFF Pin Voltage }}$ | $-0.4 \mathrm{~V} \leq \mathrm{V}_{\mathrm{SH}} \leq 6 \mathrm{~V}$ |
| Sync Pin Voltage | $-0.4 \mathrm{~V} \leq \mathrm{V}_{\text {SYNC }} \leq 2 \mathrm{~V}$ |


| Power Dissipation (Note 3) | Internally Limited |
| :--- | ---: |
| Storage Temperature Range | $-65^{\circ} \mathrm{C}$ to $+150^{\circ} \mathrm{C}$ |
| Lead Temperature (Soldering, 10 sec.$)$ | $260^{\circ} \mathrm{C}$ |
| Maximum Junction Temperature (Note 3) | $150^{\circ} \mathrm{C}$ |
| Minimum ESD Rating (C $=100 \mathrm{pF}, \mathrm{R}=1.5 \mathrm{k} \Omega$ ) | 2 kV |
| Operating Ratings |  |
| Cupply Voltage | $4 \mathrm{~V} \leq \mathrm{V}_{\mathrm{IN}} \leq 40 \mathrm{~V}$ |
| Output Switch Voltage | $0 \mathrm{~V} \leq \mathrm{V}_{\mathrm{SW}} \leq 60 \mathrm{~V}$ |
| Output Switch Current | $\mathrm{ISW} \leq 5.0 \mathrm{~A}$ |
| Junction Temperature Range | $-40^{\circ} \mathrm{C} \leq \mathrm{T}_{\mathrm{J}} \leq+125^{\circ} \mathrm{C}$ |

## Electrical Characteristics

Specifications with standard type face are for $T_{J}=25^{\circ} \mathrm{C}$, and those in bold type face apply over full Operating Temperature Range. Unless otherwise specified, $\mathrm{V}_{\mathrm{IN}}=5 \mathrm{~V}$.

## LM2588-3.3

| Symbol | Parameters | Conditions | Typical | Min | Max | Units |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| SYSTEM PARAMETERS Test Circuit of Figure 1 (Note 4) |  |  |  |  |  |  |
| V OUT | Output Voltage | $\begin{aligned} & \mathrm{V}_{\mathrm{IN}}=4 \mathrm{~V} \text { to } 12 \mathrm{~V} \\ & \mathrm{I}_{\text {LOAD }}=400 \mathrm{~mA} \text { to } 1.75 \mathrm{~A} \end{aligned}$ | 3.3 | 3.17/3.14 | 3.43/3.46 | V |
| $\Delta \mathrm{V}_{\text {OUT }} /$ <br> $\Delta \mathrm{V}_{\text {IN }}$ | Line Regulation | $\begin{aligned} & \mathrm{V}_{\mathrm{IN}}=4 \mathrm{~V} \text { to } 12 \mathrm{~V} \\ & \mathrm{I}_{\text {LOAD }}=400 \mathrm{~mA} \end{aligned}$ | 20 |  | 50/100 | mV |
| $\Delta \mathrm{V}_{\text {OUT }} /$ <br> $\Delta I_{\text {LOAD }}$ | Load Regulation | $\begin{aligned} & \mathrm{V}_{\mathrm{IN}}=12 \mathrm{~V} \\ & \mathrm{I}_{\text {LOAD }}=400 \mathrm{~mA} \text { to } 1.75 \mathrm{~A} \end{aligned}$ | 20 |  | 50/100 | mV |
| $\eta$ | Efficiency | $\mathrm{V}_{\mathrm{IN}}=12 \mathrm{~V}, \mathrm{I}_{\text {LOAD }}=1 \mathrm{~A}$ | 75 |  |  | \% |
| UNIQUE DEVICE PARAMETERS (Note 5) |  |  |  |  |  |  |
| $V_{\text {REF }}$ | Output Reference Voltage | Measured at Feedback Pin $\mathrm{V}_{\mathrm{COMP}}=1.0 \mathrm{~V}$ | 3.3 | 3.242/3.234 | 3.358/3.366 | V |
| $\Delta \mathrm{V}_{\text {REF }}$ | Reference Voltage Line Regulation | $\mathrm{V}_{\text {IN }}=4 \mathrm{~V}$ to 40 V | 2.0 |  |  | mV |
| $\mathrm{G}_{\mathrm{M}}$ | Error Amp <br> Transconductance | $\begin{aligned} & \mathrm{I}_{\mathrm{COMP}}=-30 \mu \mathrm{~A} \text { to }+30 \mu \mathrm{~A} \\ & \mathrm{~V}_{\mathrm{COMP}}=1.0 \mathrm{~V} \end{aligned}$ | 1.193 | 0.678 | 2.259 | mmho |
| Avol | Error Amp Voltage Gain | $\begin{aligned} & \mathrm{V}_{\mathrm{COMP}}=0.5 \mathrm{~V} \text { to } 1.6 \mathrm{~V} \\ & \mathrm{R}_{\mathrm{COMP}}=1.0 \mathrm{M} \Omega \text { (Note } 6 \text { ) } \end{aligned}$ | 260 | 151/75 |  | V/V |

## LM2588-5.0

| Symbol | Parameters | Conditions | Typical | Min | Max | Units |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| SYSTEM PARAMETERS Test Circuit of Figure 1 (Note 4) |  |  |  |  |  |  |
| V OUT | Output Voltage | $\begin{aligned} & \mathrm{V}_{\text {IN }}=4 \mathrm{~V} \text { to } 12 \mathrm{~V} \\ & \mathrm{I}_{\text {LOAD }}=500 \mathrm{~mA} \text { to } 1.45 \mathrm{~A} \end{aligned}$ | 5.0 | 4.80/4.75 | 5.20/5.25 | V |
| $\Delta \mathrm{V}_{\text {OUT }} /$ <br> $\Delta V_{\text {IN }}$ | Line Regulation | $\begin{aligned} & \mathrm{V}_{\mathrm{IN}}=4 \mathrm{~V} \text { to } 12 \mathrm{~V} \\ & \mathrm{I}_{\text {LOAD }}=500 \mathrm{~mA} \end{aligned}$ | 20 |  | 50/100 | mV |
| $\Delta \mathrm{V}_{\text {OUT }} /$ <br> $\Delta I_{\text {LOAD }}$ | Load Regulation | $\begin{aligned} & \mathrm{V}_{\text {IN }}=12 \mathrm{~V} \\ & \mathrm{I}_{\text {LOAD }}=500 \mathrm{~mA} \text { to } 1.45 \mathrm{~A} \end{aligned}$ | 20 |  | 50/100 | mV |
| $\eta$ | Efficiency | $\mathrm{V}_{\mathrm{IN}}=12 \mathrm{~V}, \mathrm{I}_{\text {LOAD }}=750 \mathrm{~mA}$ | 80 |  |  | \% |

## Electrical Characteristics

Specifications with standard type face are for $\mathrm{T}_{J}=25^{\circ} \mathrm{C}$, and those in bold type face apply over full Operating Temperature Range. Unless otherwise specified, $\mathrm{V}_{\mathrm{IN}}=5 \mathrm{~V}$. (Continued)
LM2588-5.0 (Continued)

| Symbol | Parameters | Conditions | Typical | Min | Max | Units |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| UNIQUE DEVICE PARAMETERS (Note 5) |  |  |  |  |  |  |
| $\mathrm{V}_{\text {REF }}$ | Output Reference Voltage | Measured at Feedback Pin $\mathrm{V}_{\mathrm{COMP}}=1.0 \mathrm{~V}$ | 5.0 | 4.913/4.900 | 5.088/5.100 | V |
| $\Delta \mathrm{V}_{\text {REF }}$ | Reference Voltage Line Regulation | $\mathrm{V}_{\text {IN }}=4 \mathrm{~V}$ to 40 V | 3.3 |  |  | mV |
| $\mathrm{G}_{\mathrm{M}}$ | Error Amp <br> Transconductance | $\begin{aligned} & \mathrm{I}_{\mathrm{COMP}}=-30 \mu \mathrm{~A} \text { to }+30 \mu \mathrm{~A} \\ & \mathrm{~V}_{\mathrm{COMP}}=1.0 \mathrm{~V} \end{aligned}$ | 0.750 | 0.447 | 1.491 | mmho |
| Avol | Error Amp <br> Voltage Gain | $\begin{aligned} & \mathrm{V}_{\mathrm{COMP}}=0.5 \mathrm{~V} \text { to } 1.6 \mathrm{~V} \\ & \mathrm{R}_{\mathrm{COMP}}=1.0 \mathrm{M} \Omega \text { (Note } 6 \text { ) } \end{aligned}$ | 165 | 99/49 |  | V/V |

## LM2588-12

| Symbol | Parameters | Conditions | Typical | Min | Max | Units |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| SYSTEM PARAMETERS Test Circuit of Figure 2 (Note 4) |  |  |  |  |  |  |
| $V_{\text {OUT }}$ | Output Voltage | $\begin{aligned} & \mathrm{V}_{I N}=4 \mathrm{~V} \text { to } 10 \mathrm{~V} \\ & \mathrm{I}_{\text {LOAD }}=300 \mathrm{~mA} \text { to } 1.2 \mathrm{~A} \end{aligned}$ | 12.0 | 11.52/11.40 | 12.48/12.60 | V |
| $\Delta \mathrm{V}_{\text {OUT }} /$ <br> $\Delta \mathrm{V}_{\mathrm{IN}}$ | Line Regulation | $\begin{aligned} & \mathrm{V}_{\mathrm{IN}}=4 \mathrm{~V} \text { to } 10 \mathrm{~V} \\ & \mathrm{I}_{\mathrm{LOAD}}=300 \mathrm{~mA} \end{aligned}$ | 20 |  | 100/200 | mV |
| $\Delta \mathrm{V}_{\text {OUT }} /$ <br> $\Delta l_{\text {LOAD }}$ | Load Regulation | $\begin{aligned} & \mathrm{V}_{I N}=10 \mathrm{~V} \\ & \mathrm{I}_{\text {LOAD }}=300 \mathrm{~mA} \text { to } 1.2 \mathrm{~A} \end{aligned}$ | 20 |  | 100/200 | mV |
| $\eta$ | Efficiency | $\mathrm{V}_{\text {IN }}=10 \mathrm{~V}, \mathrm{I}_{\text {LOAD }}=1 \mathrm{~A}$ | 90 |  |  | \% |

UNIQUE DEVICE PARAMETERS (Note 5)

| $\mathrm{V}_{\text {REF }}$ | Output Reference <br> Voltage | Measured at Feedback Pin <br> $\mathrm{V}_{\mathrm{COMP}}=1.0 \mathrm{~V}$ | 12.0 | $11.79 / \mathbf{1 1 . 7 6}$ | $12.21 / \mathbf{1 2 . 2 4}$ | V |
| :--- | :--- | :--- | :---: | :---: | :---: | :---: |
| $\Delta \mathrm{V}_{\text {REF }}$ | Reference Voltage <br> Line Regulation | $\mathrm{V}_{\mathrm{IN}}=4 \mathrm{~V}$ to 40 V | 7.8 |  |  | mV |
| $\mathrm{G}_{\mathrm{M}}$ | Error Amp <br> Transconductance | $\mathrm{I}_{\mathrm{COMP}}=-30 \mu \mathrm{~A}$ to $+30 \mu \mathrm{~A}$ <br> $\mathrm{~V}_{\mathrm{COMP}}=1.0 \mathrm{~V}$ | 0.328 | $\mathbf{0 . 1 8 6}$ | $\mathbf{0 . 6 2 1}$ | mmho |
| $\mathrm{A}_{\mathrm{VOL}}$ | Error Amp <br> Voltage | $\mathrm{V}_{\mathrm{COMP}}=0.5 \mathrm{~V}$ to 1.6 V <br> $\mathrm{R}_{\mathrm{COMP}}=1.0 \mathrm{M} \Omega($ Note 6$)$ | 70 | $41 / \mathbf{2 1}$ |  | $\mathrm{V} / \mathrm{V}$ |

## LM2588-ADJ

| Symbol | Parameters | Conditions | Typical | Min | Max | Units |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| SYSTEM PARAMETERS Test Circuit of Figure 2 (Note 4) |  |  |  |  |  |  |
| V OUT | Output Voltage | $\begin{aligned} & \mathrm{V}_{I N}=4 \mathrm{~V} \text { to } 10 \mathrm{~V} \\ & \mathrm{I}_{\mathrm{LOAD}}=300 \mathrm{~mA} \text { to } 1.2 \mathrm{~A} \end{aligned}$ | 12.0 | 11.52/11.40 | 12.48/12.60 | V |
| $\begin{aligned} & \Delta \mathrm{V}_{\text {OUT }} / \\ & \Delta \mathrm{V}_{\text {IN }} \\ & \hline \end{aligned}$ | Line Regulation | $\begin{aligned} & \mathrm{V}_{\mathrm{IN}}=4 \mathrm{~V} \text { to } 10 \mathrm{~V} \\ & \mathrm{I}_{\text {LOAD }}=300 \mathrm{~mA} \\ & \hline \end{aligned}$ | 20 |  | 100/200 | mV |
| $\begin{aligned} & \Delta V_{\text {OUT }} / \\ & \Delta l_{\text {LOAD }} \\ & \hline \end{aligned}$ | Load Regulation | $\begin{aligned} & \mathrm{V}_{I N}=10 \mathrm{~V} \\ & \mathrm{I}_{\text {LOAD }}=300 \mathrm{~mA} \text { to } 1.2 \mathrm{~A} \end{aligned}$ | 20 |  | 100/200 | mV |
| $\eta$ | Efficiency | $\mathrm{V}_{\mathrm{IN}}=10 \mathrm{~V}, \mathrm{I}_{\text {LOAD }}=1 \mathrm{~A}$ | 90 |  |  | \% |

## Electrical Characteristics

Specifications with standard type face are for $\mathrm{T}_{J}=25^{\circ} \mathrm{C}$, and those in bold type face apply over full Operating Temperature Range. Unless otherwise specified, $\mathrm{V}_{\mathrm{IN}}=5 \mathrm{~V}$. (Continued)

## LM2588-ADJ (Continued)

| Symbol | Parameters | Conditions | Typical | Min | Max | Units |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| UNIQUE DEVICE PARAMETERS (Note 5) |  |  |  |  |  |  |
| $\mathrm{V}_{\text {REF }}$ | Output Reference Voltage | Measured at Feedback Pin $\mathrm{V}_{\mathrm{COMP}}=1.0 \mathrm{~V}$ | 1.230 | 1.208/1.205 | 1.252/1.255 | V |
| $\Delta \mathrm{V}_{\text {REF }}$ | Reference Voltage Line Regulation | $\mathrm{V}_{\text {IN }}=4 \mathrm{~V}$ to 40 V | 1.5 |  |  | mV |
| $\mathrm{G}_{\mathrm{M}}$ | Error Amp <br> Transconductance | $\begin{aligned} & \mathrm{I}_{\mathrm{COMP}}=-30 \mu \mathrm{~A} \text { to }+30 \mu \mathrm{~A} \\ & \mathrm{~V}_{\mathrm{COMP}}=1.0 \mathrm{~V} \end{aligned}$ | 3.200 | 1.800 | 6.000 | mmho |
| Avol | Error Amp Voltage Gain | $\begin{aligned} & V_{\mathrm{COMP}}=0.5 \mathrm{~V} \text { to } 1.6 \mathrm{~V} \\ & R_{\mathrm{COMP}}=1.0 \mathrm{M} \Omega \text { (Note } 6 \text { ) } \end{aligned}$ | 670 | 400/200 |  | V/V |
| $\mathrm{I}_{\mathrm{B}}$ | Error Amp Input Bias Current | $\mathrm{V}_{\text {COMP }}=1.0 \mathrm{~V}$ | 125 |  | 425/600 | $n \mathrm{~A}$ |

COMMON DEVICE PARAMETERS for all versions (Note 5)

| Is | Input Supply Current | Switch Off <br> (Note 8) | 11 |  | 15.5/16.5 | mA |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | ISWITCH $=3.0 \mathrm{~A}$ | 85 |  | 140/165 | mA |
| $I_{\text {S/D }}$ | Shutdown Input Supply Current | $\mathrm{V}_{\mathrm{SH}}=3 \mathrm{~V}$ | 16 |  | 100/300 | $\mu \mathrm{A}$ |
| $\mathrm{V}_{\mathrm{UV}}$ | Input Supply Undervoltage Lockout | $\mathrm{R}_{\text {LOAD }}=100 \Omega$ | 3.30 | 3.05 | 3.75 | V |
| $\mathrm{fo}_{0}$ | Oscillator Frequency | Measured at Switch Pin $R_{\text {LOAD }}=100 \Omega, \mathrm{~V}_{\text {COMP }}=1.0 \mathrm{~V}$ Freq. Adj. Pin Open (Pin 1) | 100 | 85/75 | 115/125 | kHz |
|  |  | $\mathrm{R}_{\text {SET }}=22 \mathrm{k} \Omega$ | 200 |  |  | kHz |
| $\mathrm{f}_{\text {SC }}$ | Short-Circuit Frequency | Measured at Switch Pin <br> $R_{\text {LOAD }}=100 \Omega$ <br> $\mathrm{V}_{\text {FEEDBACK }}=1.15 \mathrm{~V}$ | 25 |  |  | kHz |
| $\mathrm{V}_{\text {EAO }}$ | Error Amplifier Output Swing | Upper Limit (Note 7) | 2.8 | 2.6/2.4 |  | V |
|  |  | Lower Limit (Note 8) | 0.25 |  | 0.40/0.55 | V |
| $I_{\text {EAO }}$ | Error Amp <br> Output Current <br> (Source or Sink) | (Note 9) | 165 | 110/70 | 260/320 | $\mu \mathrm{A}$ |
| Iss | Soft Start Current | $\begin{aligned} & \mathrm{V}_{\text {FEEDBACK }}=0.92 \mathrm{~V} \\ & \mathrm{~V}_{\text {COMP }}=1.0 \mathrm{~V} \end{aligned}$ | 11.0 | 8.0/7.0 | 17.0/19.0 | $\mu \mathrm{A}$ |
| $\mathrm{D}_{\text {MAX }}$ | Maximum Duty Cycle | $\begin{aligned} & R_{\text {LOAD }}=100 \Omega \\ & (\text { Note 7) } \end{aligned}$ | 98 | 93/90 |  | \% |
| $\mathrm{I}_{\mathrm{L}}$ | Switch Leakage Current | Switch Off $\mathrm{V}_{\text {SWITCH }}=60 \mathrm{~V}$ | 15 |  | 300/600 | $\mu \mathrm{A}$ |
| $\mathrm{V}_{\text {SUS }}$ | Switch Sustaining Voltage | $\mathrm{dV} / \mathrm{dT}=1.5 \mathrm{~V} / \mathrm{ns}$ |  | 65 |  | V |
| $\mathrm{V}_{\text {SAT }}$ | Switch Saturation Voltage | $\mathrm{I}_{\text {SWITCH }}=5.0 \mathrm{~A}$ | 0.7 |  | 1.1/1.4 | V |
| $\mathrm{I}_{\mathrm{CL}}$ | NPN Switch Current Limit |  | 6.5 | 5.0 | 9.5 | A |

## Electrical Characteristics

Specifications with standard type face are for $\mathrm{T}_{J}=25^{\circ} \mathrm{C}$, and those in bold type face apply over full Operating Temperature Range. Unless otherwise specified, $\mathrm{V}_{\mathrm{IN}}=5 \mathrm{~V}$. (Continued)

## LM2588-ADJ (Continued)

| Symbol | Parameters | Conditions | Typical | Min | Max | Units |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| COMMON DEVICE PARAMETERS (Note 5) (Continued) |  |  |  |  |  |  |
| $\mathrm{V}_{\text {STH }}$ | Synchronization Threshold Voltage | $\begin{aligned} & \mathrm{F}_{\text {SYNC }}=200 \mathrm{kHz} \\ & \mathrm{~V}_{\mathrm{COMP}}=1 \mathrm{~V}, \mathrm{~V}_{\mathrm{IN}}=5 \mathrm{~V} \end{aligned}$ | 0.75 | 0.625/0.40 | 0.875/1.00 | V |
| $\mathrm{I}_{\text {SYNC }}$ | Synchronization Pin Current | $\begin{aligned} & \mathrm{V}_{\mathrm{IN}}=5 \mathrm{~V} \\ & \mathrm{~V}_{\mathrm{COMP}}=1 \mathrm{~V}, \mathrm{~V}_{\mathrm{SYNC}}=\mathrm{V}_{\mathrm{STH}} \end{aligned}$ | 100 |  | 200 | $\mu \mathrm{A}$ |
| $\mathrm{V}_{\text {SHTH }}$ | $\overline{O N} / O F F$ Pin (Pin 1) <br> Threshold Voltage | $\begin{aligned} & \mathrm{V}_{\mathrm{COMP}}=1 \mathrm{~V} \\ & (\text { Note 10) } \end{aligned}$ | 1.6 | 1.0/0.8 | 2.2/2.4 | V |
| ISH | $\overline{O N} / O F F$ Pin (Pin 1) <br> Current | $\begin{aligned} & \mathrm{V}_{\mathrm{COMP}}=1 \mathrm{~V} \\ & \mathrm{~V}_{\mathrm{SH}}=\mathrm{V}_{\mathrm{SHTH}} \end{aligned}$ | 40 | 15/10 | 65/75 | $\mu \mathrm{A}$ |
| $\begin{aligned} & \theta_{\mathrm{JA}} \\ & \theta_{\mathrm{JA}} \\ & \theta_{\mathrm{JC}} \\ & \hline \end{aligned}$ | Thermal Resistance | T Package, Junction to Ambient (Note 11) T Package, Junction to Ambient (Note 12) T Package, Junction to Case | $\begin{gathered} 65 \\ 45 \\ 2 \end{gathered}$ |  |  |  |
| $\begin{aligned} & \theta_{\mathrm{JA}} \\ & \theta_{\mathrm{JA}} \\ & \theta_{\mathrm{JA}} \\ & \theta_{\mathrm{JC}} \\ & \hline \end{aligned}$ |  | S Package, Junction to Ambient (Note 13) <br> S Package, Junction to Ambient (Note 14) <br> S Package, Junction to Ambient (Note 15) <br> S Package, Junction to Case | $\begin{gathered} 56 \\ 35 \\ 26 \\ 2 \end{gathered}$ |  |  | ${ }^{\circ} \mathrm{C} / \mathrm{W}$ |

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. These ratings apply when the current is limited to less than 1.2 mA for pins $1,2,3$, and 6 . Operating ratings indicate conditions for which the device is intended to be functional, but device parameter specifications may not be guaranteed under these conditions. For guaranteed specifications and test conditions, see the Electrical Characteristics.
Note 2: Note that switch current and output current are not identical in a step-up regulator. Output current cannot be internally limited when the LM2588 is used as a step-up regulator. To prevent damage to the switch, the output current must be externally limited to 5 A . However, output current is internally limited when the LM2588 is used as a flyback regulator (see the Application Hints section for more information).
Note 3: The junction temperature of the device $\left(T_{J}\right)$ is a function of the ambient temperature ( $T_{A}$ ), the junction-to-ambient thermal resistance ( $\theta_{\mathrm{JA}}$ ), and the power dissipation of the device $\left(P_{D}\right)$. A thermal shutdown will occur if the temperature exceeds the maximum junction temperature of the device: $P_{D} \times \theta_{J A}+T_{A(M A X} \geq$
$T_{J(M A X)}$. For a safe thermal design, check that the maximum power dissipated by the device is less than: $P_{D} \leq\left[T_{J(M A X)}-T_{A(M A X)}\right] / \theta_{J A}$. When calculating the maximum allowable power dissipation, derate the maximum junction temperature-this ensures a margin of safety in the thermal design.
Note 4: External components such as the diode, inductor, input and output capacitors can affect switching regulator performance. When the LM2588 is used as shown in Figures 1 and 2, system performance will be as specified by the system parameters.
Note 5: All room temperature limits are 100\% production tested, and all limits at temperature extremes are guaranteed via correlation using standard Statistical Quality Control (SQC) methods.
Note 6: A $1.0 \mathrm{M} \Omega$ resistor is connected to the compensation pin (which is the error amplifier output) to ensure accuracy in measuring Avol.
Note 7: To measure this parameter, the feedback voltage is set to a low value, depending on the output version of the device, to force the error amplifier output high and the switch on.
Note 8: To measure this parameter, the feedback voltage is set to a high value, depending on the output version of the device, to force the error amplifier output ow and the switch off

Note 9: To measure the worst-case error amplifier output current, the LM2588 is tested with the feedback voltage set to its low value (specified in Note 7) and at its high value (specified in Note 8).
Note 10: When testing the minimum value, do not sink current from this pin-isolate it with a diode. If current is drawn from this pin, the frequency adjust circuit will begin operation (see Figure 41).
Note 11: Junction to ambient thermal resistance (no external heat sink) for the 7 lead TO-220 package mounted vertically, with $1 / 2$ inch leads in a socket, or on a PC board with minimum copper area.
Note 12: Junction to ambient thermal resistance (no external heat sink) for the 7 lead TO-220 package mounted vertically, with $1 / 2$ inch leads soldered to a PC board containing approximately 4 square inches of ( 1 oz. ) copper area surrounding the leads.
Note 13: Junction to ambient thermal resistance for the 7 lead TO-263 mounted horizontally against a PC board area of 0.136 square inches (the same size as the TO-263 package) of 1 oz . ( 0.0014 in . thick) copper.
Note 14: Junction to ambient thermal resistance for the 7 lead TO-263 mounted horizontally against a PC board area of 0.4896 square inches ( 3.6 times the area of the TO-263 package) of 1 oz . ( 0.0014 in. thick) copper.
Note 15: Junction to ambient thermal resistance for the 7 lead TO-263 mounted horizontally against a PC board copper area of 1.0064 square inches ( 7.4 times the area of the TO-263 package) of 1 oz. ( 0.0014 in. thick) copper. Additional copper area will reduce thermal resistance further. See the thermal model in Switchers Made Simple ${ }^{\circledR}$ software.

## Typical Performance Characteristics






Error Amp Transconductance vs Temperature
 TEMPERATURE (C) TL/H/12420-11


TL/H/12420-3


TL/H/12420-6

## Switch Transconductance

 vs Temperature

Error Amp Voltage Gain vs Temperature



TL/H/12420-4
Feedback Pin Bias Current vs Temperature


temperature (c)
TL/H/12420-10
Short Circuit Frequency vs Temperature


## Typical Performance Characteristics (Continued)



TL/H/12420-14


TL/H/12420-15


## Connection Diagrams



Order Number LM2588T-3.3, LM2588T-5.0, LM2588T-12 or LM2588T-ADJ See NS Package Number TA07B

7-Lead TO-263 (S) Side View



TL/H/12420-19
Order Number LM2588S-3.3, LM2588S-5.0,
LM2588S-12 or LM2588S-ADJ
Tape and Reel Order Number LM2588SX-3.3, LM2588SX-5.0, LM2588SX-12 or LM2588SX-ADJ

See NS Package Number TS7B

## Test Circuits



FIGURE 2. LM2588-12 and LM2588-ADJ

## Block Diagram



For Fixed Versions
$3.3 \mathrm{~V}, \mathrm{R} 1=3.4 \mathrm{k}, \mathrm{R} 2=2 \mathrm{k}$
$5.0 \mathrm{~V}, \mathrm{R} 1=6.15 \mathrm{k}, \mathrm{R} 2=2 \mathrm{k}$
$12 \mathrm{~V}, \mathrm{R} 1=8.73 \mathrm{k}, \mathrm{R} 2=1 \mathrm{k}$
For Adj. Version
R1 $=$ Short $(0 \Omega), R 2=$ Open

## FIGURE 3

## Flyback Regulator Operation

The LM2588 is ideally suited for use in the flyback regulator topology. The flyback regulator can produce a single output voltage, such as the one shown in Figure 4, or multiple output voltages. In Figure 4, the flyback regulator generates an output voltage that is inside the range of the input voltage. This feature is unique to flyback regulators and cannot be duplicated with buck or boost regulators.
The operation of a flyback regulator is as follows (refer to Figure 4): when the switch is on, current flows through the primary winding of the transformer, T 1 , storing energy in the magnetic field of the transformer. Note that the primary and secondary windings are out of phase, so no current flows through the secondary when current flows through the primary. When the switch turns off, the magnetic field col-
lapses, reversing the voltage polarity of the primary and secondary windings. Now rectifier D1 is forward biased and current flows through it, releasing the energy stored in the transformer. This produces voltage at the output.
The output voltage is controlled by modulating the peak switch current. This is done by feeding back a portion of the output voltage to the error amp, which amplifies the difference between the feedback voltage and a 1.230 V reference. The error amp output voltage is compared to a ramp voltage proportional to the switch current (i.e., inductor current during the switch on time). The comparator terminates the switch on time when the two voltages are equal, thereby controlling the peak switch current to maintain a constant output voltage.


TL/H/12420-24 As shown in Figure 4, the LM2588 can be used as a flyback regulator by using a minimum number of external components. The switching waveforms of this regulator are shown in Figure 5. Typical Performance Characteristics observed during the operation of this circuit are shown in Figure 6.

FIGURE 4. 12V Flyback Regulator Design Example

## Typical Performance Characteristics

A


TL/H/12420-60
FIGURE 5. Switching Waveforms


Horizontal: $2 \mathrm{~ms} / \mathrm{div}$
h Voltage, 10V/div
B: Switch Current, 5A/div
C: Output Rectifier Current, 5A/div
D: Output Ripple Voltage, $100 \mathrm{mV} / \mathrm{div}$
AC-Coupled
c
D

FIGURE 6. V ${ }_{\text {OUT }}$ Response to Load Current Step

## Typical Flyback Regulator Applications

Figures 7 through 12 show six typical flyback applications, varying from single output to triple output. Each drawing contains the part number(s) and manufacturer(s) for every component except the transformer. For the transformer part numbers and manufacturers' names, see the table in

Figure 13. For applications with different output voltagesrequiring the LM2588-ADJ-or different output configurations that do not match the standard configurations, refer to the Switchers Made Simple ${ }^{\circledR}$ software.


FIGURE 7. Single-Output Flyback Regulator


TL/H/12420-26
FIGURE 8. Single-Output Flyback Regulator

## Typical Flyback Regulator Applications (Continued)



TL/H/12420-27
FIGURE 9. Single-Output Flyback Regulator


FIGURE 10. Dual-Output Flyback Regulator
TL/H/12420-28

## FIGUE 10. Dual Output Flyback Regulator

Typical Flyback Regulator Applications (Continued)


## Typical Flyback Regulator Applications (Continued)

Transformer Selection (T)
Figure 13 lists the standard transformers available for flyback regulator applications. Included in the table are the turns ratio(s) for each transformer, as well as the output voltages, input voltage ranges, and the maximum load currents for each circuit.

| Applications | Figure 7 | Figure 8 | Figure 9 | Figure 10 | Figure 11 | Figure 12 |
| :--- | :---: | :---: | :---: | :---: | :---: | :---: |
| Transformers | T1 | T1 | T1 | T2 | T3 | T4 |
| $\mathrm{V}_{\text {IN }}$ | $4 \mathrm{~V}-6 \mathrm{~V}$ | $4 \mathrm{~V}-6 \mathrm{~V}$ | $8 \mathrm{~V}-16 \mathrm{~V}$ | $4 \mathrm{~V}-6 \mathrm{~V}$ | $18 \mathrm{~V}-36 \mathrm{~V}$ | $18 \mathrm{~V}-36 \mathrm{~V}$ |
| $\mathrm{~V}_{\text {OUT1 }}$ | 3.3 V | 5 V | 12 V | 12 V | 12 V | 5 V |
| $\mathrm{I}_{\text {OUT1 }}$ (Max) | 1.8 A | 1.4 A | 1.2 A | 0.3 A | 1 A | 2.5 A |
| $\mathrm{~N}_{1}$ | 1 | 1 | 1 | 2.5 | 0.8 | 0.35 |
| $\mathrm{~V}_{\text {OUT2 }}$ |  |  |  | -12 V | -12 V | 12 V |
| $\mathrm{I}_{\text {OUT2 }}$ (Max) |  |  |  | 0.3 A | 1 A | 0.5 A |
| $\mathrm{~N}_{2}$ |  |  | 2.5 | 0.8 | 0.8 |  |
| $\mathrm{~V}_{\text {OUT3 }}$ |  |  |  |  | -12 V |  |
| $\mathrm{I}_{\text {OUT3 }}$ (Max) |  |  |  |  |  | 0.5 A |
| $\mathrm{~N}_{3}$ |  |  |  |  | 0.8 |  |

FIGURE 13. Transformer Selection Table

| Transformer <br> Type | Manufacturers' Part Numbers |  |  |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: |
|  | Coilcraft <br> (Note 1) | Coilcraft (Note 1) <br> Surface Mount | Pulse (Note 2) <br> Surface Mount | Renco <br> (Note 3) | Schott <br> (Note 4) |
| T1 | Q4434-B | Q4435-B | PE-68411 | RL-5530 | 67141450 |
| T2 | Q4337-B | Q4436-B | PE-68412 | RL-5531 | 67140860 |
| T3 | Q4343-B | - | PE-68421 | RL-5534 | 67140920 |
| T4 | Q4344-B | - | PE-68422 | RL-5535 | 67140930 |


| Note 1: Coilcraft Inc., | Phone: (800) 322-2645 |
| :---: | :---: |
| 1102 Silver Lake Road, Cary, IL 60013 | Fax: (708) 639-1469 |
| European Headquarters, 21 Napier Place | Phone: + 441236730595 |
| Wardpark North, Cumbernauld, Scotland G68 0LL | Fax: +441236730627 |
| Note 2: Pulse Engineering Inc., | Phone: (619) 674-8100 |
| 12220 World Trade Drive, San Diego, CA 92128 | Fax: (619) 674-8262 |
| European Headquarters, Dunmore Road | Phone: + 3539324107 |
| Tuam, Co. Galway, Ireland | Fax: + 3539324459 |
| Note 3: Renco Electronics Inc., | Phone: (800) 645-5828 |
| 60 Jeffryn Blvd. East, Deer Park, NY 11729 | Fax: (516) 586-5562 |
| Note 4: Schott Corp., | Phone: (612) 475-1173 |
| 1000 Parkers Lane Road, Wayzata, MN 55391 | Fax: (612) 475-1786 |

FIGURE 14. Transformer Manufacturer Guide

## Typical Flyback Regulator Applications (Continued)

## Transformer Footprints

Figures 15 through 32 show the footprints of each transformer, listed in Figure 14.


FIGURE 15. Coilcraft Q4434-B


FIGURE 17. Coilcraft Q4343-B


FIGURE 19. Coilcraft Q4435-B (Surface Mount)


TL/H/12420-32
Top View FIGURE 16. Coilcraft Q4337-B


TL/H/12420-34
Top View
FIGURE 18. Coilcraft Q4344-B


FIGURE 20. Coilcraft Q4436-B (Surface Mount)

## Typical Flyback Regulator Applications (Continued)



FIGURE 21. Pulse PE-68411
(Surface Mount)


FIGURE 23. Pulse PE-68421
(Surface Mount)


TL/H/12420-41
Top View
FIGURE 25. Renco RL-5530

T2


FIGURE 22. Pulse PE-68412
(Surface Mount)


TL/H/12420-40
Top View
FIGURE 24. Pulse PE-68422 (Surface Mount)



## Step-Up (Boost) Regulator Operation

Figure 33 shows the LM2588 used as a step-up (boost) regulator. This is a switching regulator that produces an output voltage greater than the input supply voltage.
A brief explanation of how the LM2588 Boost Regulator works is as follows (refer to Figure 33). When the NPN switch turns on, the inductor current ramps up at the rate of $\mathrm{V}_{\mathrm{IN}} / \mathrm{L}$, storing energy in the inductor. When the switch turns
off, the lower end of the inductor flies above $\mathrm{V}_{\mathrm{IN}}$, discharging its current through diode (D) into the output capacitor (COUT) at a rate of $\left(\mathrm{V}_{\text {OUT }}-\mathrm{V}_{\text {IN }}\right) / \mathrm{L}$. Thus, energy stored in the inductor during the switch on time is transferred to the output during the switch off time. The output voltage is controlled by adjusting the peak switch current, as described in the flyback regulator section.


FIGURE 33. 12V Boost Regulator
By adding a small number of external components (as shown in Figure 33), the LM2588 can be used to produce a regulated output voltage that is greater than the applied input voltage. The switching waveforms observed during the operation of this circuit are shown in Figure 34. Typical performance of this regulator is shown in Figure 35.

## Typical Performance Characteristics



A: Switch Voltage,10V/div
B: Switch Current, 5A/div
C: Inductor Current, 5A/div
D: Output Ripple Voltage,
$100 \mathrm{mV} / \mathrm{div}$, AC-Coupled


FIGURE 35. V OUT Response to Load Current Step

FIGURE 34. Switching Waveforms

## Typical Boost Regulator Applications

Figures 36 and 38 through 40 show four typical boost appli-cations-one fixed and three using the adjustable version of the LM2588. Each drawing contains the part number(s) and manufacturer(s) for every component. For the fixed 12 V
output application, the part numbers and manufacturers' names for the inductor are listed in a table in Figure 37. For applications with different output voltages, refer to the Switchers Made Simple ${ }^{\circledR}$ software.


TL/H/12420-50
FIGURE 36. +5 V to $+\mathbf{1 2 V}$ Boost Regulator

Figure 37 contains a table of standard inductors, by part number and corresponding manufacturer, for the fixed output regulator of Figure 36.

| Coilcraft (Note 1) | Pulse (Note 2) | Renco (Note 3) | Schott (Note 4) |
| :---: | :---: | :---: | :---: |
| R4793-A | PE-53900 | RL-5472-5 | 67146520 |

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European Headquarters, 21 Napier Place Phone: +441236730595 Wardpark North, Cumbernauld, Scotland G68 OLL Fax: + 441236730627 Note 2: Pulse Engineering Inc.,
12220 World Trade Drive, San Diego, CA 92128
European Headquarters, Dunmore Road
Tuam, Co. Galway, Ireland
Note 3: Renco Electronics Inc.,
60 Jeffryn Blvd. East, Deer Park, NY 11729
Note 4: Schott Corp.,
Phone: (619) 674-8100 Fax: (619) 674-8262
Phone: + 3539324107 Fax: + 3539324459
Phone: (800) 645-5828 Fax: (516) 586-5562

1000 Parkers Lane Road, Wayzata, MN 55391
FIGURE 37. Inductor Selection Table

## Typical Boost Regulator Applications (Continued)



TL/H/12420-51
FIGURE 38. $+\mathbf{1 2 V}$ to +24 V Boost Regulator


TL/H/12420-53
FIGURE 40. +24 V to +48 V Boost Regulator
*The LM2588 will require a heat sink in these applications. The size of the heat sink will depend on the maximum ambient temperature. To calculate the thermal resistance of the IC and the size of the heat sink needed, see the "Heat Sink/Thermal Considerations" section in the Application Hints.

## Application Hints

LM2588 SPECIAL FEATURES


TL/H/12420-54
FIGURE 41. Shutdown Operation

## SHUTDOWN CONTROL

A feature of the LM2588 is its ability to be shut down using the ON/OFF pin (pin 1). This feature conserves input power by turning off the device when it is not in use. For proper operation, an isolation diode is required (as shown in Figure 41).

The device will shut down when 3 V or greater is applied on the $\overline{O N} / O F F$ pin, sourcing current into pin 1 . In shut down mode, the device will draw typically $56 \mu \mathrm{~A}$ of supply current ( $16 \mu \mathrm{~A}$ to $\mathrm{V}_{\mathrm{IN}}$ and $40 \mu \mathrm{~A}$ to the $\overline{\mathrm{ON}} /$ OFF pin). To turn the device back on, leave pin 1 floating, using an (isolation) diode, as shown in Figure 41 (for normal operation, do not source or sink current to or from this pin-see the next section).

## FREQUENCY ADJUSTMENT

The switching frequency of the LM2588 can be adjusted with the use of an external resistor. This feature allows the user to optimize the size of the magnetics and the output capacitor(s) by tailoring the operating frequency. A resistor connected from pin 1 (the Freq. Adj. pin) to ground will set the switching frequency from 100 kHz to 200 kHz (maximum). As shown in Figure 41, the pin can be used to adjust the frequency while still providing the shut down function. A curve in the Performance Characteristics Section graphs the resistor value to the corresponding switching frequency. The table in Figure 42 shows resistor values corresponding to commonly used frequencies.
However, changing the LM2588's operating frequency from its nominal value of 100 kHz will change the magnetics selection and compensation component values.

| $\mathbf{R}_{\mathbf{S E T}}(\mathbf{k} \Omega$ ) | Frequency (kHz) |
| :---: | :---: |
| Open | 100 |
| 200 | 125 |
| 47 | 150 |
| 33 | 175 |
| 22 | 200 |

FIGURE 42. Frequency Setting Resistor Guide


## FIGURE 43. Frequency Synchronization

## FREQUENCY SYNCHRONIZATION

Another feature of the LM2588 is the ability to synchronize the switching frequency to an external source, using the sync pin (pin 6). This feature allows the user to parallel multiple devices to deliver more output power.
A negative falling pulse applied to the sync pin will synchronize the LM2588 to an external oscillator (see Figures 43 and 44).
Use of this feature enables the LM2588 to be synchronized to an external oscillator, such as a system clock. This operation allows multiple power supplies to operate at the same frequency, thus eliminating frequency-related noise problems.


FIGURE 44. Waveforms of a Synchronized 12V Boost Regulator
The scope photo in Figure 44 shows a LM2588 12V Boost Regulator synchronized to a 200 kHz signal. There is a 700 ns delay between the falling edge of the sync signal and the turning on of the switch.

## Application Hints (Continued)



FIGURE 45. Boost Regulator

## PROGRAMMING OUTPUT VOLTAGE <br> output with an external current limit circuit. The external limit

 (SELECTING R1 AND R2)Referring to the adjustable regulator in Figure 45, the output voltage is programmed by the resistors R1 and R2 by the following formula:
$V_{\text {OUT }}=V_{\text {REF }}(1+R 1 / R 2) \quad$ where $V_{\text {REF }}=1.23 V$
Resistors R1 and R2 divide the output voltage down so that it can be compared with the 1.23 V internal reference. With R2 between 1 k and $5 \mathrm{k}, \mathrm{R} 1$ is:

$$
R 1=R 2\left(V_{\text {OUT }} / V_{R E F}-1\right) \quad \text { where } V_{R E F}=1.23 V
$$

For best temperature coefficient and stability with time, use $1 \%$ metal film resistors.

## SHORT CIRCUIT CONDITION

Due to the inherent nature of boost regulators, when the output is shorted (see Figure 45), current flows directly from the input, through the inductor and the diode, to the output, bypassing the switch. The current limit of the switch does not limit the output current for the entire circuit. To protect the load and prevent damage to the switch, the current must be externally limited, either by the input supply or at the
should be set to the maximum switch current of the device, which is 5 A .
In a flyback regulator application (Figure 46), using the standard transformers, the LM2588 will survive a short circuit to the main output. When the output voltage drops to $80 \%$ of its nominal value, the frequency will drop to 25 kHz . With a lower frequency, off times are larger. With the longer off times, the transformer can release all of its stored energy before the switch turns back on. Hence, the switch turns on initially with zero current at its collector. In this condition, the switch current limit will limit the peak current, saving the device.

## FLYBACK REGULATOR INPUT CAPACITORS

A flyback regulator draws discontinuous pulses of current from the input supply. Therefore, there are two input capacitors needed in a flyback regulator-one for energy storage and one for filtering (see Figure 46). Both are required due to the inherent operation of a flyback regulator. To keep a stable or constant voltage supply to the LM2588, a storage capacitor ( $2100 \mu \mathrm{~F}$ ) is required. If the input source is a


TL/H/12420-57
FIGURE 46. Flyback Regulator

## Application Hints (Continued)

recitified DC supply and/or the application has a wide temperature range, the required rms current rating of the capacitor might be very large. This means a larger value of capacitance or a higher voltage rating will be needed for the input capacitor. The storage capacitor will also attenuate noise which may interfere with other circuits connected to the same input supply voltage.
In addition, a small bypass capacitor is required due to the noise generated by the input current pulses. To eliminate the noise, insert a $1.0 \mu \mathrm{~F}$ ceramic capacitor between $\mathrm{V}_{\mathrm{IN}}$ and ground as close as possible to the device.

## SWITCH VOLTAGE LIMITS

In a flyback regulator, the maximum steady-state voltage appearing at the switch, when it is off, is set by the transformer turns ratio, N , the output voltage, $\mathrm{V}_{\text {OUT }}$, and the maximum input voltage, $\mathrm{V}_{\mathrm{IN}}(\mathrm{Max})$ :

$$
V_{\text {SW }(\mathrm{OFF})}=\mathrm{V}_{\text {IN }}(\mathrm{Max})+\left(\mathrm{V}_{\text {OUT }}+\mathrm{V}_{\mathrm{F}}\right) / \mathrm{N}
$$

where $V_{F}$ is the forward biased voltage of the output diode, and is typically 0.5 V for Schottky diodes and 0.8 V for ultrafast recovery diodes. In certain circuits, there exists a voltage spike, $\mathrm{V}_{\mathrm{LL}}$, superimposed on top of the steady-state voltage (see Figure 5, waveform A). Usually, this voltage spike is caused by the transformer leakage inductance and/ or the output rectifier recovery time. To "clamp" the voltage at the switch from exceeding its maximum value, a transient suppressor in series with a diode is inserted across the transformer primary (as shown in the circuit in Figure 4 and other flyback regulator circuits throughout the datasheet). The schematic in Figure 46 shows another method of clamping the switch voltage. A single voltage transient suppressor (the SA51A) is inserted at the switch pin. This method clamps the total voltage across the switch, not just the voltage across the primary.
If poor circuit layout techniques are used (see the "Circuit Layout Guideline" section), negative voltage transients may appear on the Switch pin (pin 5). Applying a negative voltage (with respect to the IC's ground) to any monolithic IC pin causes erratic and unpredictable operation of that IC. This holds true for the LM2588 IC as well. When used in a flyback regulator, the voltage at the Switch pin (pin 5) can go negative when the switch turns on. The "ringing" voltage at the switch pin is caused by the output diode capacitance and the transformer leakage inductance forming a resonant circuit at the secondary(ies). The resonant circuit generates the "ringing" voltage, which gets reflected back through the transformer to the switch pin. There are two common methods to avoid this problem. One is to add an RC snubber around the output rectifier(s), as in Figure 46. The values of the resistor and the capacitor must be chosen so that the voltage at the Switch pin does not drop below -0.4 V . The resistor may range in value between $10 \Omega$ and $1 \mathrm{k} \Omega$, and the capacitor will vary from $0.001 \mu \mathrm{~F}$ to $0.1 \mu \mathrm{~F}$. Adding a snubber will (slightly) reduce the efficiency of the overall circuit.
The other method to reduce or eliminate the "ringing" is to insert a Schottky diode clamp between pins 5 and 4 (ground), also shown in Figure 46. This prevents the voltage at pin 5 from dropping below -0.4 V . The reverse voltage rating of the diode must be greater than the switch off voltage.


FIGURE 47. Input Line Filter

## OUTPUT VOLTAGE LIMITATIONS

The maximum output voltage of a boost regulator is the maximum switch voltage minus a diode drop. In a flyback regulator, the maximum output voltage is determined by the turns ratio, N , and the duty cycle, D , by the equation:

$$
V_{\text {OUT }} \approx N \times V_{\text {IN }} \times D /(1-D)
$$

The duty cycle of a flyback regulator is determined by the following equation:

$$
\mathrm{D}=\frac{\mathrm{V}_{\mathrm{OUT}}+\mathrm{V}_{\mathrm{F}}}{\mathrm{~N}\left(\mathrm{~V}_{\text {IN }}-\mathrm{V}_{\mathrm{SAT}}\right)+\mathrm{V}_{\mathrm{OUT}}+\mathrm{V}_{\mathrm{F}}} \approx \frac{\mathrm{~V}_{\mathrm{OUT}}}{\mathrm{~N}\left(\mathrm{~V}_{\text {IN }}\right)+\mathrm{V}_{\mathrm{OUT}}}
$$

Theoretically, the maximum output voltage can be as large as desired-just keep increasing the turns ratio of the transformer. However, there exists some physical limitations that prevent the turns ratio, and thus the output voltage, from increasing to infinity. The physical limitations are capacitances and inductances in the LM2588 switch, the output diode(s), and the transformer-such as reverse recovery time of the output diode (mentioned above).

## NOISY INPUT LINE CONDITION

A small, low-pass RC filter should be used at the input pin of the LM2588 if the input voltage has an unusually large amount of transient noise, such as with an input switch that bounces. The circuit in Figure 47 demonstrates the layout of the filter, with the capacitor placed from the input pin to ground and the resistor placed between the input supply and the input pin. Note that the values of $\mathrm{R}_{\text {IN }}$ and $\mathrm{C}_{I N}$ shown in the schematic are good enough for most applications, but some readjusting might be required for a particular application. If efficiency is a major concern, replace the resistor with a small inductor (say $10 \mu \mathrm{H}$ and rated at 200 mA ).

## STABILITY

All current-mode controlled regulators can suffer from an instability, known as subharmonic oscillation, if they operate with a duty cycle above $50 \%$. To eliminate subharmonic oscillations, a minimum value of inductance is required to ensure stability for all boost and flyback regulators. The minimum inductance is given by:

$$
\mathrm{L}(\operatorname{Min})=\frac{2.92\left[\left(\mathrm{~V}_{\mathrm{IN}}(\operatorname{Min})-\mathrm{V}_{\mathrm{SAT}}\right) \bullet(2 \mathrm{D}(\operatorname{Max})-1)\right]}{1-\mathrm{D}(\operatorname{Max})}(\mu \mathrm{H})
$$

where $\mathrm{V}_{\text {SAT }}$ is the switch saturation voltage and can be found in the Characteristic Curves.

## Application Hints (Continued)



TL/H/12420-59
FIGURE 48. Circuit Board Layout

## CIRCUIT LAYOUT GUIDELINES

As in any switching regulator, layout is very important. Rapidly switching currents associated with wiring inductance generate voltage transients which can cause problems. For minimal inductance and ground loops, keep the length of the leads and traces as short as possible. Use single point grounding or ground plane construction for best results. Separate the signal grounds from the power grounds (as indicated in Figure 48). When using the Adjustable version, physically locate the programming resistors as near the regulator IC as possible, to keep the sensitive feedback wiring short.

## HEAT SINK/THERMAL CONSIDERATIONS

In many cases, a heat sink is not required to keep the LM2588 junction temperature within the allowed operating temperature range. For each application, to determine whether or not a heat sink will be required, the following must be identified:

1) Maximum ambient temperature (in the application).
2) Maximum regulator power dissipation (in the application).
3) Maximum allowed junction temperature $\left(125^{\circ} \mathrm{C}\right.$ for the LM2588). For a safe, conservative design, a temperature approximately $15^{\circ} \mathrm{C}$ cooler than the maximum junction temperature should be selected $\left(110^{\circ} \mathrm{C}\right)$.
4) LM2588 package thermal resistances $\theta_{\mathrm{JA}}$ and $\theta_{\mathrm{JC}}$ (given in the Electrical Characteristics).
Total power dissipated ( $\mathrm{P}_{\mathrm{D}}$ ) by the LM2588 can be estimated as follows:
Boost:

$$
P_{D}=0.15 \Omega \cdot\left(\frac{I_{L O A D}}{1-D}\right)^{2} \bullet D+\frac{I_{L O A D}}{50 \bullet(1-D)} \bullet D \bullet V_{I N}
$$

Flyback:

$$
\begin{aligned}
\mathrm{P}_{\mathrm{D}}= & 0.15 \Omega \cdot\left(\frac{\mathrm{~N} \cdot \Sigma \mathrm{I}_{\mathrm{LOAD}}}{1-\mathrm{D}}\right)^{2} \bullet \mathrm{D} \\
& +\frac{\mathrm{N} \cdot \Sigma I_{\mathrm{LOAD}}}{50 \cdot(1-\mathrm{D})} \bullet \mathrm{D} \bullet \mathrm{~V}_{I N}
\end{aligned}
$$

$\mathrm{V}_{\mathrm{IN}}$ is the minimum input voltage, $\mathrm{V}_{\mathrm{OUT}}$ is the output voltage, N is the transformer turns ratio, D is the duty cycle, and $l_{\text {LOAD }}$ is the maximum load current (and $\Sigma$ lomad $_{\text {LOA }}$ is the sum of the maximum load currents for multiple-output flyback regulators). The duty cycle is given by:
Boost:

$$
\mathrm{D}=\frac{\mathrm{V}_{\text {OUT }}+\mathrm{V}_{\mathrm{F}}-\mathrm{V}_{\text {IN }}}{\mathrm{V}_{\text {OUT }}+\mathrm{V}_{\mathrm{F}}-\mathrm{V}_{\text {SAT }}} \approx \frac{\mathrm{V}_{\text {OUT }}-\mathrm{V}_{\text {IN }}}{\mathrm{V}_{\text {OUT }}}
$$

Flyback:

$$
\mathrm{D}=\frac{\mathrm{V}_{\mathrm{OUT}}+\mathrm{V}_{\mathrm{F}}}{\mathrm{~N}\left(\mathrm{~V}_{\text {IN }}-\mathrm{V}_{\mathrm{SAT}}\right)+\mathrm{V}_{\mathrm{OUT}}+\mathrm{V}_{\mathrm{F}}} \approx \frac{\mathrm{~V}_{\mathrm{OUT}}}{\mathrm{~N}\left(\mathrm{~V}_{\text {IN }}\right)+\mathrm{V}_{\mathrm{OUT}}}
$$

where $\mathrm{V}_{\mathrm{F}}$ is the forward biased voltage of the diode and is typically 0.5 V for Schottky diodes and 0.8 V for fast recovery diodes. $\mathrm{V}_{\text {SAT }}$ is the switch saturation voltage and can be found in the Characteristic Curves.
When no heat sink is used, the junction temperature rise is:

$$
\Delta T_{J}=P_{D} \bullet \theta_{J A} .
$$

Adding the junction temperature rise to the maximum ambient temperature gives the actual operating junction temperature:

$$
\mathrm{T}_{\mathrm{J}}=\Delta \mathrm{T}_{\mathrm{J}}+\mathrm{T}_{\mathrm{A}} .
$$

If the operating junction temperature exceeds the maximum junction temperatue in item 3 above, then a heat sink is required. When using a heat sink, the junction temperature rise can be determined by the following:

$$
\Delta \mathrm{T}_{\mathrm{J}}=\mathrm{P}_{\mathrm{D}} \bullet\left(\theta_{\mathrm{JC}}+\theta_{\text {Interface }}+\theta_{\text {Heat Sink }}\right)
$$

Again, the operating junction temperature will be:

$$
T_{J}=\Delta T_{J}+T_{A}
$$

## Application Hints (Continued)

As before, if the maximum junction temperature is exceeded, a larger heat sink is required (one that has a lower thermal resistance).
Included in the Switchers Made Simple ${ }^{\circledR}$ design software is a more precise (non-linear) thermal model that can be used to determine junction temperature with different inputoutput parameters or different component values. It can also calculate the heat sink thermal resistance required to maintain the regulator junction temperature below the maximum operating temperature.

To further simplify the flyback regulator design procedure, National Semiconductor is making available computer design software Switchers Made Simple ${ }^{\circledR}$ software is available on a ( $31 / 2^{\prime \prime}$ ) diskette for IBM compatible computers from a National Semiconductor sales office in your area or the National Semiconductor Customer Response Center (1-800-272-9959).

## Physical Dimensions inches (millimeters)


LM2588 SIMPLE SWITCHER 5A Flyback Regulator

Physical Dimensions inches (millimeters) (Continued)


## LIFE SUPPORT POLICY

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1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and whose failure to perform, when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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## System Products

- Analog to Digital Converters
- CCD/CIS Sensor Processor LM9801
- Temperature Sensors
- System Monitors


# Analog to Digital Converters 

- ADC12041
- ADC12048
- ADC14061

12Bit+Sign, 1 Channel, 216kHz, Successive Approximation Analog to Digital Converter
8 Channel Version of ADC12041
Auto-Calibrating, $14 \mathrm{Bit}, 2.2 \mathrm{MHz}$, Pipelined Architecture A/D Converter


## Connection Diagrams

|  | 28-Pin SSOP |  |
| :---: | :---: | :---: |
| $\overline{W R}-1 \mathrm{O}$ | 28 | -CLK |
| $\overline{\mathrm{RD}}$ - 2 | 27 | -SYNC |
| $\overline{C S}-3$ | 26 | -D12 |
| WMode - 4 | 25 | -011 |
| $\mathrm{v}_{\text {IN }}+$ - 5 | 24 | -D10 |
| $\mathrm{v}_{\text {IN }}-{ }^{\text {d }}$ - | 23 | -09 |
| $\mathrm{v}_{\mathrm{A}}{ }^{+}-7$ | 22 | -DGND |
| AGND-8 | ADC12041 21 | - $\mathrm{V}_{\mathrm{D}}{ }^{+}$ |
| $V_{\text {REF }}{ }^{-}-9$ | 20 | -08 |
| $\mathrm{V}_{\text {REF }}{ }^{+}-10$ | 19 | -07 |
| $\overline{\mathrm{RDY}}$ - 11 | 18 | -06 |
| D0- 12 | 17 | -05 |
| D1-13 | 16 | -D4 |
| D2-14 | 15 | -03 |



TL/H/12441-3 Order Number ADC12041CIV See NS Package Number V28A

Order Number ADC12041CIMSA
See NS Package Number MSA28

## Ordering Information

| Industrial Temperature Range <br> $-\mathbf{4 0} \mathbf{C} \leq \mathbf{T}_{\mathbf{A}} \leq+\mathbf{8 5}^{\circ} \mathbf{C}$ | NS <br> Package <br> Number |
| :--- | :--- |
| ADC12041CIV | V28A |
| ADC12041CIMSA | MSA28, SSOP |


| Absolute Maximum Ratings <br> (Notes 1 and 2) |  |
| :---: | :---: |
| Supply Voltage ( $\mathrm{V}_{\mathrm{A}}{ }^{+}$and $\mathrm{V}_{\mathrm{D}}{ }^{+}$) | 6.0 V |
| Voltage at all Inputs | -0.3 V to $\mathrm{V}^{+}+0.3 \mathrm{~V}$ |
| $\left\|\mathrm{V}_{\mathrm{A}}+-\mathrm{V}_{\mathrm{D}}{ }^{+}\right\|$ | 300 mV |
| \|AGND - DGND| | 300 mV |
| Input Current at Any Pin (Note 3) | $\pm 30 \mathrm{~mA}$ |
| Package Input Current (Note 3) | $\pm 120 \mathrm{~mA}$ |
| Power Dissipation (Note 4) at $\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$ | 500 mW |
| Storage Temperature | $-65^{\circ} \mathrm{C}$ to $+150^{\circ} \mathrm{C}$ |
| Lead Temperature |  |
| SSOP Package |  |
| Vapor Phase (60 sec.) | $210^{\circ} \mathrm{C}$ |
| Infared (15 sec.) | $220{ }^{\circ} \mathrm{C}$ |
| $\checkmark$ Package, Infared (15 sec.) | $300^{\circ} \mathrm{C}$ |
| ESD Susceptibility (Note 5) | 3.0 kV |

Operating Ratings (Notes 1 and 2 )


Converter DC Characteristics the following specifications apply to the $\operatorname{ADC12041}$ for $\mathrm{V}_{\mathrm{A}}{ }^{+}=\mathrm{V}_{\mathrm{D}}{ }^{+}=5 \mathrm{~V}$, $\mathrm{V}_{\mathrm{REF}}{ }^{+}=4.096 \mathrm{~V}, \mathrm{~V}_{\mathrm{REF}}{ }^{-}=0.0 \mathrm{~V}$, 12 -bit + sign conversion mode, $\mathrm{f}_{\mathrm{CLK}}=12.0 \mathrm{MHz}, \mathrm{R}_{\mathrm{S}}=25 \Omega$, source impedance for $\mathrm{V}_{\mathrm{REF}}{ }^{+}$ and $\mathrm{V}_{\text {REF }}{ }^{-} \leq 1 \Omega$, fully differential input with fixed 2.048 V common-mode voltage ( $\mathrm{V}_{\text {INCM }}$ ), and minimum acquisition time, unless otherwise specified. Boldface limits apply for $\mathbf{T}_{\mathbf{A}}=\mathbf{T}_{\mathbf{J}}=\mathbf{T}_{\text {MIN }}$ to $\mathbf{T}_{\mathbf{M A X}}$; all other limits $\mathrm{T}_{\mathbf{A}}=\mathrm{T}_{\mathbf{J}}=25^{\circ} \mathrm{C}$

| Symbol | Parameter | Conditions | Typical (Note 10) | Limits (Note 11) | Units (Limit) |
| :---: | :---: | :---: | :---: | :---: | :---: |
|  | Resolution with No Missing Codes | After Auto-Cal |  | 13 | Bits (max) |
| ILE | Positive and Negative Integral Linearity Error | After Auto-Cal (Notes 12 and 17) | $\pm 0.6$ | $\pm 1$ | LSB (max) |
| DNL | Differential Non-Linearity | After Auto-Cal |  | $\pm 1$ | LSB (max) |
|  | Zero Error | After Auto-Cal (Notes 13 and 17) $\begin{aligned} & \mathrm{V}_{\text {INCM }}=5.0 \mathrm{~V} \\ & \mathrm{~V}_{\text {INCM }}=2.048 \mathrm{~V} \\ & \mathrm{~V}_{\text {INCM }}=0 \mathrm{~V} \end{aligned}$ |  | $\begin{array}{r}  \pm 5.5 \\ \pm \mathbf{2 . 0} \\ \pm \mathbf{5 . 5} \\ \hline \end{array}$ | LSB (max) |
|  | Positive Full-Scale Error | After Auto-Cal (Notes 12 and 17) | $\pm 1.0$ | $\pm 2.5$ | LSB (max) |
|  | Negative Full-Scale Error | After Auto-Cal (Notes 12 and 17) | $\pm 1.0$ | $\pm 2.5$ | LSB (max) |
|  | DC Common Mode Error | After Auto-Cal (Note 14) | $\pm 2$ | $\pm 5.5$ | LSB (max) |
| TUE | Total Unadjusted Error | After Auto-Cal (Note 18) | $\pm 1$ |  | LSB |

Power Supply Characteristics The following specifications apply to the ADC12041 for $\mathrm{V}_{\mathrm{A}^{+}}=\mathrm{V}_{\mathrm{D}}{ }^{+}=5 \mathrm{~V}$, $\mathrm{V}_{\mathrm{REF}}{ }^{+}=4.096 \mathrm{~V}, \mathrm{~V}_{\mathrm{REF}}{ }^{-}=0.0 \mathrm{~V}, 12$-bit + sign conversion mode, $\mathrm{f}_{\mathrm{CLK}}=12.0 \mathrm{MHz}, \mathrm{R}_{\mathrm{S}}=25 \Omega$, source impedance for $\mathrm{V}_{\mathrm{REF}}{ }^{+}$ and $V_{\text {REF }}{ }^{-1} 1 \Omega$, fully differential input with fixed 2.048 V common-mode voltage, and minimum acquisition time, unless otherwise specified. Boldface limits apply for $\mathbf{T}_{\mathbf{A}}=\mathbf{T}_{\mathbf{J}}=\mathbf{T}_{\text {MIN }}$ to $\mathbf{T}_{\mathbf{M A X}}$; all other limits $\mathrm{T}_{\mathrm{A}}=\mathrm{T}_{\mathrm{J}}=25^{\circ} \mathrm{C}$

| Symbol | Parameter | Conditions | Typical (Note 10) | Limits (Note 11) | Unit (Limit) |
| :---: | :---: | :---: | :---: | :---: | :---: |
| PSS | Power Supply Sensitivity <br> Zero Error <br> Full-Scale Error <br> Linearity Error | $\begin{aligned} & \mathrm{V}_{\mathrm{D}^{+}}=\mathrm{V}_{\mathrm{A}}{ }^{+}=5.0 \mathrm{~V} \pm 10 \% \\ & \mathrm{~V}_{\mathrm{REF}^{+}}=4.096 \mathrm{~V} \\ & \mathrm{~V}_{\mathrm{REF}}{ }^{-}=0 \mathrm{~V} \end{aligned}$ | $\begin{aligned} & \pm 0.1 \\ & \pm 0.5 \\ & \pm 0.1 \\ & \hline \end{aligned}$ |  | $\begin{aligned} & \text { LSB } \\ & \text { LSB } \\ & \text { LSB } \\ & \hline \end{aligned}$ |
| $\mathrm{ID}^{+}$ | $\mathrm{V}_{\mathrm{D}}+$ Digital Supply Current | Start Command (Performing a conversion) with SYNC configured as an input and driven with a 214 kHz signal. Bus width set to 13 . <br> $\mathrm{f}_{\mathrm{CLK}}=12.0 \mathrm{MHz}$, Reset Mode <br> $\mathrm{f}_{\mathrm{CLK}}=12.0 \mathrm{MHz}$, Conversion | $\begin{aligned} & 850 \\ & 2.45 \end{aligned}$ | 2.6 | $\begin{gathered} \mu \mathrm{A} \\ \mathrm{~mA}(\max ) \end{gathered}$ |
| $\mathrm{I}_{\mathrm{A}}+$ | $\mathrm{V}_{\mathrm{A}}+$ Analog Supply Current | Start Command (Performing a conversion) with SYNC configured as an input and driven with a 214 kHz signal. Bus width set to 13 . <br> $\mathrm{f}_{\mathrm{CLK}}=12.0 \mathrm{MHz}$, Reset Mode <br> $\mathrm{f}_{\mathrm{CLK}}=12.0 \mathrm{MHz}$, Conversion | $\begin{aligned} & 2.3 \\ & 2.3 \end{aligned}$ | 4.0 | $\begin{gathered} \mathrm{mA} \\ \mathrm{~mA}(\max ) \end{gathered}$ |
| $\mathrm{I}_{\text {ST }}$ | Standby Supply Current $\left(I_{D}{ }^{+}+I_{A}^{+}\right)$ | Standby Mode <br> $\mathrm{f}_{\mathrm{CLK}}=$ Stopped <br> $\mathrm{f}_{\mathrm{CLK}}=12.0 \mathrm{MHz}$ | $\begin{gathered} 5 \\ 100 \end{gathered}$ | $\begin{gathered} 15 \\ 120 \end{gathered}$ | $\mu \mathrm{A}$ (max) <br> $\mu \mathrm{A}(\max )$ |

Analog Input Characteristics The following specifications apply to the ADC12041 for $\mathrm{V}_{\mathrm{A}^{+}}=\mathrm{V}_{\mathrm{D}^{+}}=5 \mathrm{~V}$, $\mathrm{V}_{\mathrm{REF}}{ }^{+}=4.096 \mathrm{~V}, \mathrm{~V}_{\mathrm{REF}}{ }^{-}=0.0 \mathrm{~V}$, 12 -Bit + sign conversion mode, $\mathrm{f} C \mathrm{LK}=12.0 \mathrm{MHz}, \mathrm{R}_{\mathrm{S}}=25 \Omega$, source impedance for $\mathrm{V}_{\text {REF }}{ }^{+}$and $\mathrm{V}_{\text {REF }}{ }^{+} \leq 1 \Omega$, fully differential input with fixed 2.048 V common-mode voltage, and minimum acquisition time, unless otherwise specified. Boldface limits apply for $\mathbf{T}_{\mathbf{A}}=\mathbf{T}_{\mathbf{J}}=\mathbf{T}_{\mathbf{M I N}}$ to $\mathbf{T}_{\mathbf{M A X}}$; all other limits $\mathbf{T}_{\mathbf{A}}=\mathbf{T}_{\mathbf{J}}=\mathbf{2 5}{ }^{\circ} \mathbf{C}$

| Symbol | Parameter | Conditions | Typical <br> (Note 10) | Limits <br> (Note 11) | Unit <br> (Limit) |
| :--- | :--- | :--- | :---: | :---: | :---: |
| $\mathrm{I}_{\mathbb{N}}$ | $\mathrm{V}_{\mathrm{IN}^{+}}$and $\mathrm{V}_{\mathrm{IN}^{-}}$Input Leakage Current | $\mathrm{V}_{\mathbb{I N}^{+}=5 \mathrm{~V}}$ <br> $\mathrm{~V}_{\mathbb{N}^{-}}=0 \mathrm{~V}$ | 0.05 <br> -0.05 | $\mathbf{2 . 0}$ | $\mu \mathrm{~A}$ (max) |
| $\mathrm{RON}_{\mathrm{ON}}$ | ADC Input On Resistance | $\mathrm{V}_{\mathbb{N}}=2.5 \mathrm{~V}$ <br> Refer to section titled INPUT CURRENT. | 1000 |  | $\Omega$ |
| $\mathrm{CV}_{\mathbb{I N}}$ | ADC Input Capacitance |  | 10 |  | pF |

Reference Inputs The following specifications apply to the $\mathrm{ADC1} 2041$ for $\mathrm{V}_{\mathrm{A}}{ }^{+}=\mathrm{V}_{\mathrm{D}^{+}}=5 \mathrm{~V}, \mathrm{~V}_{\mathrm{REF}}{ }^{+}=4.096 \mathrm{~V}$, $\mathrm{V}_{\text {REF }}{ }^{-}=0.0 \mathrm{~V}, 12$-bit + sign conversion mode, f fCLK $=12.0 \mathrm{MHz}, \mathrm{R}_{\mathrm{S}}=25 \Omega$, source impedance for $\mathrm{V}_{\text {REF }}{ }^{+}$and $\mathrm{V}_{\text {REF }}{ }^{-} \leq$ $1 \Omega$, fully differential input with fixed 2.048 V common-mode voltage, and minimum acquisition time, unless otherwise specified. Boldface limits apply for $\mathbf{T}_{\mathbf{A}}=\mathbf{T}_{\mathbf{J}}=\mathbf{T}_{\mathbf{M I N}}$ to $\mathbf{T}_{\mathbf{M A X}}$; all other limits $\mathrm{T}_{\mathbf{A}}=\mathrm{T}_{\mathrm{J}}=25^{\circ} \mathrm{C}$

| Symbol | Parameter | Conditions | Typical <br> (Note 10) | Limits <br> (Note 11) | Unit <br> (Limit) |
| :--- | :---: | :---: | :---: | :---: | :---: |
| $\mathrm{I}_{\text {REF }}$ | Reference Input Current | $\mathrm{V}_{\text {REF }}+4.096 \mathrm{~V}, \mathrm{~V}_{\mathrm{REF}}-=0 \mathrm{~V}$ |  |  |  |
|  |  | Analog Input Signal: 1 kHz <br> (Note 20) | 145 |  | $\mu \mathrm{~A}$ |
|  |  | 80 kHz | 136 |  | $\mu \mathrm{~A}$ |
| $\mathrm{C}_{\text {REF }}$ | Reference Input Capacitance |  | 85 |  | pF |

Digital Logic Input/Output Characteristics The following specifications apply to the ADC12041 for $\mathrm{V}_{\mathrm{A}^{+}}=\mathrm{V}_{\mathrm{D}^{+}}=5 \mathrm{~V}, \mathrm{~V}_{\text {REF }^{+}}=4.096 \mathrm{~V}, \mathrm{~V}_{\text {REF }}{ }^{-}=0.0 \mathrm{~V}, 12$-bit + sign conversion mode, $\mathrm{f}_{\text {CLK }}=12.0 \mathrm{MHz}$, $\mathrm{R}_{\mathrm{S}}=25 \Omega$, source impedance for $\mathrm{V}_{\text {REF }}{ }^{+}$and $\mathrm{V}_{\text {REF }}{ }^{-} \leq 1 \Omega$, fully differential input with fixed 2.048 V common-mode voltage, and minimum acquisition time, unless otherwise specified. Boldface limits apply for $\mathbf{T}_{\mathbf{A}}=\mathbf{T}_{\mathbf{J}}=\mathbf{T}_{\mathbf{M I N}}$ to $\mathbf{T}_{\mathbf{M A X}}$; all other limits $\mathrm{T}_{\mathbf{A}}=\mathrm{T}_{\mathrm{J}}=$ $25^{\circ} \mathrm{C}$

| Symbol | Parameter | Conditions | Typical (Note 10) | Limits (Note 11) | Unit (Limit) |
| :---: | :---: | :---: | :---: | :---: | :---: |
| $\mathrm{V}_{\mathrm{IH}}$ | Logic High Input Voltage | $\mathrm{V}_{\mathrm{A}}{ }^{+}=\mathrm{V}_{\mathrm{D}}{ }^{+}=5.5 \mathrm{~V}$ |  | 2.2 | $V(\min )$ |
| $\mathrm{V}_{\text {IL }}$ | Logic Low Input Voltage | $\mathrm{V}_{\mathrm{A}}{ }^{+}=\mathrm{V}_{\mathrm{D}}{ }^{+}=4.5 \mathrm{~V}$ |  | 0.8 | V (max) |
| $\mathrm{IIH}^{\text {H }}$ | Logic High Input Current | $\mathrm{V}_{\mathrm{IN}}=5 \mathrm{~V}$ | 0.035 | 2.0 | $\mu \mathrm{A}$ (max) |
| IIL | Logic Low Input Current | $\mathrm{V}_{\mathrm{IN}}=0 \mathrm{~V}$ | -0.035 | -2.0 | $\mu \mathrm{A}$ (max) |
| $\mathrm{V}_{\mathrm{OH}}$ | Logic High Output Voltage | $\begin{aligned} & \mathrm{V}_{\mathrm{A}^{+}}=\mathrm{V}_{\mathrm{D}}+=4.5 \mathrm{~V} \\ & \mathrm{I}_{\text {OUT }}=-1.6 \mathrm{~mA} \end{aligned}$ | 2.4 | 2.4 | $V(\min )$ |
| V OL | Logic Low Output Voltage | $\begin{aligned} & \mathrm{V}_{\mathrm{A}}^{+}=\mathrm{V}_{\mathrm{D}}+=4.5 \mathrm{~V} \\ & \mathrm{I} \text { OUT }=1.6 \mathrm{~mA} \end{aligned}$ | 0.4 | 0.4 | $V$ (max) |
| loff | TRI-STATE Output Leakage Current | $\begin{aligned} & \mathrm{V}_{\text {OUT }}=0 \mathrm{~V} \\ & \mathrm{~V}_{\text {OUT }}=5 \mathrm{~V} \end{aligned}$ |  | $\pm 2.0$ | $\mu \mathrm{A}$ (max) |
| $\mathrm{C}_{\text {IN }}$ | D12-D0 Input Capacitance |  | 10 |  | pF |

Converter AC Characteristics the following specifications apply to the ADC12041 for $\mathrm{V}_{\mathrm{S}^{+}}=\mathrm{V}_{\mathrm{D}}{ }^{+}=5 \mathrm{~V}$, $\mathrm{V}_{\mathrm{REF}}{ }^{+}=4.096 \mathrm{~V}, \mathrm{~V}_{\mathrm{REF}}{ }^{-}=0.0 \mathrm{~V}, 12$-bit + sign conversion mode, $\mathrm{f}_{\mathrm{CLK}}=12.0 \mathrm{MHz}, \mathrm{R}_{\mathrm{S}}=25 \Omega$, source impedance for $\mathrm{V}_{\mathrm{REF}}{ }^{+}$ and $\mathrm{V}_{\text {REF }}{ }^{-} \leq 1 \Omega$, fully differential input with fixed 2.048 V common-mode voltage, and minimum acquisition time, unless otherwise specified. Boldface limits apply for $\mathbf{T}_{\mathbf{A}}=\mathbf{T}_{\mathbf{J}}=\mathbf{T}_{\mathbf{M I N}}$ to $\mathbf{T}_{\mathbf{M A X}}$; all other limits $\mathrm{T}_{\mathbf{A}}=\mathrm{T}_{\mathrm{J}}=25^{\circ} \mathrm{C}$

| Symbol | Parameter | Conditions | Typical (Note 10) | Limits (Note 11) | Unit (Limit) |
| :---: | :---: | :---: | :---: | :---: | :---: |
| $\mathrm{t}_{\mathrm{z}}$ | Auto Zero Time |  | 78 | 78 clks + 120 ns | clks (max) |
| $\mathrm{t}_{\mathrm{CAL}}$ | Full Calibration Time |  | 4946 | 4946 clks + 120 ns | clks (max) |
|  | CLK Duty Cycle |  | 50 | $\begin{aligned} & 40 \\ & 60 \end{aligned}$ | $\begin{gathered} \% \\ \%(\min ) \\ \%(\max ) \end{gathered}$ |
| tconv | Conversion Time | Sync-Out Mode | 44 | 44 | clks (max) |
| $\mathrm{t}_{\text {AcqSYNCOUT }}$ | Acquisition Time (Programmable) | Minimum for 13 Bits Maximum for 13 Bits | $\begin{gathered} 9 \\ 79 \\ \hline \end{gathered}$ | $\begin{gathered} 9 \text { clks }+120 \text { ns } \\ 79 \text { clks }+120 \text { ns } \end{gathered}$ | clks (max) clks (max) |

Digital Timing Characteristics The following specifications apply to the ADC12041, 13-bit data bus width, $\mathrm{V}_{\mathrm{A}}{ }^{+}=\mathrm{V}_{\mathrm{D}}{ }^{+}=5 \mathrm{~V}, \mathrm{f}_{\mathrm{CLK}}=12 \mathrm{MHz}, \mathrm{t}_{\mathrm{f}}=3 \mathrm{~ns}$ and $\mathrm{C}_{\mathrm{L}}=50 \mathrm{pF}$ on data $\mathrm{I} / \mathrm{O}$ lines

| Symbol <br> (Figure 7) | Parameter | Conditions | Typical (Note 10) | Limits (Note 11) | $\begin{aligned} & \text { Unit } \\ & \text { (Limit) } \end{aligned}$ |
| :---: | :---: | :---: | :---: | :---: | :---: |
| ${ }_{\text {t }}$ | Throughput Rate | Sync-Out Mode (SYNC Bit = "0") 9 Clock Cycles of Acquisition Time | 222 |  | kHz |
| $t_{\text {cSWR }}$ | Falling Edge of $\overline{C S}$ to Falling Edge of $\overline{W R}$ |  | 0 |  | ns |
| twrcs | Active Edge of $\overline{W R}$ <br> to Rising Edge of $\overline{\mathrm{CS}}$ |  | 0 |  | ns |
| tWR | $\overline{\text { WR Pulse Width }}$ |  | 20 | 30 | ns (min) |
| twRSETFalling | Write Setup Time | WMODE $=$ " 1 " |  | 20 | ns (min) |
| tWRHOLDFalling | Write Hold Time | WMODE $=$ " 1 " |  | 5 | ns (min) |
| ${ }^{\text {t }}$ WRSETRising | Write Setup Time | WMODE $=$ " 0 " |  | 20 | ns (min) |
| $t^{\text {twRHOLDRising }}$ | Write Hold Time | WMODE $=$ " 0 "' |  | 5 | ns (min) |
| ${ }^{\text {t }}$ CSRD | Falling Edge of $\overline{C S}$ to Falling Edge of $\overline{R D}$ |  | 0 |  | ns |
| $t_{\text {RDCS }}$ | Rising Edge of $\overline{R D}$ to Rising Edge of $\overline{C S}$ |  | 0 |  | ns |
| $t_{\text {RDDATA }}$ | Falling Edge of $\overline{\mathrm{RD}}$ to Valid Data | 8-Bit Mode (BW Bit = '0") | 40 | 58 | ns (max) |
| $t_{\text {RDDATA }}$ | Falling Edge of $\overline{\mathrm{RD}}$ to Valid Data | 13-Bit Mode (BW Bit = "1") | 26 | 44 | ns (max) |
| $\mathrm{t}_{\text {RDHOLD }}$ | Read Hold Time |  | 23 | 32 | ns (max) |
| $t_{\text {RDRDY }}$ | Rising Edge of $\overline{R D}$ to Rising Edge of $\overline{\text { RDY }}$ |  | 24 | 38 | $n \mathrm{~ns}$ (max) |
| twrRDY | Active Edge of $\overline{W R}$ to Rising Edge of $\overline{\mathrm{RDY}}$ | WMODE $=$ " 1 " | 37 | 60 | $n \mathrm{~ns}$ (max) |
| ${ }^{\text {tstDRDY }}$ | Active Edge of $\overline{W R}$ to Falling Edge of $\overline{\mathrm{RDY}}$ | WMODE = " 0 ". Writing the RESET Command into the Configuration Register | 1.4 | 2.5 | ms (max) |
| $\mathrm{t}_{\text {SYNC }}$ | Minimum SYNC Pulse Width |  | 5 | 10 | ns (min) |

## Notes on Specifications

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional, but do not guarantee specific performance limits. For guaranteed specifications and test conditions, see the Electrical Characteristics. The guaranteed specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions.
Note 2: All voltages are measured with respect to GND, unless otherwise specified.
Note 3: When the input voltage $\left(\mathrm{V}_{\mathrm{IN}}\right)$ at any pin exceeds the power supply rails $\left(\mathrm{V}_{\mathrm{IN}}<G N D\right.$ or $\mathrm{V}_{\text {IN }}>\left(\mathrm{V}_{\mathrm{A}}+\right.$ or $\left.\mathrm{V}_{\mathrm{D}}+\right)$ ), the current at that pin should be limited to 30 mA . The 120 mA maximum package input current limits the number of pins that can safely exceed the power supplies with an input current of 30 mA to four.
Note 4: The maximum power dissipation must he derated at elevated temperatures and is dictated by $T_{J m a x}$, (maximum junction temperature), $\theta_{J A}$ (package junction to ambient thermal resistance), and $T_{A}$ (ambient temperature). The maximum allowable power dissipation at any temperature is $P_{D \max }=\left(T_{J m a x}-T_{A}\right) /$ $\theta_{\mathrm{JA}}$ or the number given in the Absolute Maximum Ratings, whichever is lower. For this device, $\mathrm{T}_{\mathrm{Jmax}}=150^{\circ} \mathrm{C}$, and the typical thermal resistance ( $\theta_{\mathrm{JA}}$ ) of the ADC12041 in the V package, when board mounted, is $55^{\circ} \mathrm{C} / \mathrm{W}$, and in the SSOP package, when board mounted, is $130^{\circ} \mathrm{C} / \mathrm{W}$.
Note 5: Human body model, 100 pF discharged through $1.5 \Omega \mathrm{k}$ resistor.

## Notes on Specifications (Continued)

Note 6: Each input is protected by a nominal 6.5 V breakdown voltage zener diode to GND, as shown below, input voltage magnitude up to 5 V above $\mathrm{V}_{\mathrm{A}}+$ or 5 V below GND will not damage the ADC12041. There are parasitic diodes that exist between the inputs and the power supply rails and errors in the A/D conversion can occur if these diodes are forward biased by more than 50 mV . As an example, if $\mathrm{V}_{\mathrm{A}}{ }^{+}$is $4.50 \mathrm{~V}_{\mathrm{DC}}$, full-scale input voltage must be $4.55 \mathrm{~V}_{\mathrm{DC}}$ to ensure accurate conversions.


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Note 7: $\mathrm{V}_{\mathrm{A}}{ }^{+}$and $\mathrm{V}_{\mathrm{D}^{+}}$must be connected together to the same power supply voltage and bypassed with separate capacitors at each $\mathrm{V}+$ pin to assure conversion/comparison accuracy. Refer to the Power Supply Considerations section for a detailed discussion.
Note 8: Accuracy is guaranteed when operating at $\mathrm{f}_{\mathrm{CLK}}=12 \mathrm{MHz}$.
Note 9: With the test condition for $\mathrm{V}_{\mathrm{REF}}\left(\mathrm{V}_{\mathrm{REF}^{+}}-\mathrm{V}_{\mathrm{REF}}{ }^{-}\right)$given as +4.096 V , the 12 -bit LSB is 1.000 mV .
Note 10: Typicals are at $\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$ and represent most likely parametric norm.
Note 11: Limits are guaranteed to National's AOQL (Average Outgoing Quality Level).
Note 12: Positive integral linearity error is defined as the deviation of the analog value, expressed in LSBs, from the straight line that passes through positive fullscale and zero. For negative integral linearity error, the straight line passes through negative full-scale and zero.
Note 13: Zero error is a measure of the deviation from the mid-scale voltage (a code of zero), expressed in LSB. It is the average value of the code transitions between -1 to 0 and 0 to +1 (see Figure 6).
Note 14: The DC common-mode error is measured with both inputs shorted together and driven from 0 V to 5 V . The measured value is referred to the resulting output value when the inputs are driven with a 2.5 V input.
Note 15: Power Supply Sensitivity is measured after an Auto-Zero and Auto Calibration cycle has been completed with $\mathrm{V}_{A^{+}}$and $\mathrm{V}_{\mathrm{D}^{+}}$at the specified extremes.
Note 16: $\mathrm{V}_{\text {REFCM }}$ (Reference Voltage Common Mode Range) is defined as $\left(\frac{\mathrm{V}_{\mathrm{REF}^{+}}+\mathrm{V}_{\mathrm{REF}^{-}}}{2}\right)$
Note 17: The ADC12041's self-calibration technique ensures linearity and offset errors as specified, but noise inherent in the self-calibration process will result in a repeatability uncertainty of $\pm 0.20$ LSB.
Note 18: Total Unadjusted Error (TUE) includes offset, full scale linearity and MUX errors
Note 19: The ADC12041 parts used to gather the information for these curves were auto-calibrated prior to taking the measurements at each test condition. The auto-calibration cycle cancels any first order drifts due to test conditions. However, each measurement has a repeatability uncertainty error of 0.2 LSB. See Note 17.

Note 20: This is a DC average current drawn by the reference input with a full-scale sinewave input. The ADC12041 is continuously converting with a throughput rate of 206 kHz .
Note 21: These typical curves were measured during continuous conversions with a positive half-scale DC input. A $240 \mathrm{~ns} \overline{\mathrm{RD}}$ pulse was applied 25 ns after the $\overline{R D Y}$ signal went low. The data bus lines were loaded with 2 HC family CMOS inputs ( $\mathrm{C}_{\mathrm{L}} \sim 20 \mathrm{pF}$ ).
Note 22: Any other values placed in the command field are meaningless. However, if a code of 101 or 110 is placed in the command field and the $\overline{\mathrm{CS}}, \overline{\mathrm{RD}}$ and $\overline{\mathrm{WR}}$ go low the same time, the ADC12041 will enter a test mode. These test modes are only to be used by the manufacturer of this device. A hardware power-off and power-on reset must be done to get out of these test modes.

## Electrical Characteristics



FIGURE 1. Output Digital Code vs the Operating Input Voltage Range (General Case)


FIGURE 2. Output Digital Code vs the Operating Input Voltage Range for $\mathrm{V}_{\text {REF }}=4.096 \mathrm{~V}$

## Electrical Characteristics (Continued)



FIGURE 3. $V_{\text {REF }}$ Operating Range (General Case)

$\mathrm{V}_{\mathrm{REF}+}(\mathrm{V})$
FIGURE 4. $\mathrm{V}_{\text {REF }}$ Operating Range for $\mathrm{V}_{\mathbf{A}}=\mathbf{5 V}$

## Electrical Characteristics (Continued)



FIGURE 5b. Simplified Error vs Output Code without Auto-Calibration or Auto-Zero Cycles

## Electrical Characteristics (Continued)




FIGURE 6. Offset or Zero Error Voltage (Note 13)

## Timing Diagrams



FIGURE 7a. Sync-Out Write (WMODE = 1, BW = 1), Read and Convert Cycles

Timing Diagrams (Continued)


FIGURE 7c. Sync-Out Write (WMODE $=0, B W=1$ ), Read and Convert Cycles



Timing Diagrams (Continued)


FIGURE 7g. 8-bit Bus Read Cycle (Sync-Out)



## Typical Performance Characteristics (See Note 19, Electrical Characteristic Section)



TL/H/12441-17
Integral Linearity Error (INL) Change vs Temperature


L/H/12441-20



TL/H/12441-26

Full-Scale Error Change vs Clock Frequency


Full-Scale Error Change vs Temperature


TL/H/12441-21
Full-Scale Error Change vs Reference Voltage


TL/H/12441-24
Full-Scale Error Change vs Supply Voltage


TL/H/12441-27


Zero Error Change vs Temperature


TL/H/12441-22


TL/H/12441-25


Typical Performance Characteristics (See Note 21, Electrical Characteristic Section) (Continued)



TL/H/12441-30


TL/H/12441-31


Typical Performance Characteristics (Continued) The curves were obtained under the following conditions. $\mathrm{R}_{\mathrm{S}}=50 \Omega, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}, \mathrm{V}_{\mathrm{A}}{ }^{+}=\mathrm{V}_{\mathrm{D}}{ }^{+}=5 \mathrm{~V}, \mathrm{~V}_{\mathrm{REF}}=4.096 \mathrm{~V}, \mathrm{f}_{\mathrm{CLK}}=12 \mathrm{MHz}$, and the sampling rate $\mathrm{f}_{\mathrm{S}}=215 \mathrm{kHz}$ unless otherwise stated.

Full Scale Differential $\mathbf{3 8 , 4 5 2 ~ H z}$ Sine Wave Input


Half Scale Differential $\mathbf{1} \mathbf{~ k H z}$
Sine Wave Input, $\mathrm{f}_{\mathrm{S}}=153.6 \mathbf{~ k H z}$

(Hz)
TL/H/12441-37

## Half Scale Differential 40 kHz

Sine Wave Input, $\mathrm{f}_{\mathbf{S}}=153.6 \mathbf{k H z}$

( Hz )
TL/H/12441-39

Full Scale Differential $18,677 \mathrm{~Hz}$ Sine Wave Input

( Hz )
TL/H/12441-34
Full Scale Differential $79,468 \mathrm{~Hz}$ Sine Wave Input


Half Scale Differential 20 kHz Sine Wave Input, fs $=153.6 \mathbf{k H z}$


Half Scale Differential 75 kHz Sine Wave Input, $\mathrm{f}_{\mathrm{S}}=153.6 \mathbf{k H z}$


| Pin Description |  |  |
| :---: | :---: | :---: |
| PLCC and SSOP Pkg. Pin Number | Pin Name | Description |
| 5 | $\begin{aligned} & \mathrm{V}_{\mathrm{IN}^{+}} \\ & \mathrm{V}_{\text {IN }} \end{aligned}$ | The analog ADC inputs. $\mathrm{V}_{\mathrm{IN}}+$ is the non-inverting (positive) input and $\mathrm{V}_{\mathrm{IN}}$ - is the inverting (negative) input into the ADC. |
| 10 | $\mathrm{V}_{\text {REF }}{ }^{+}$ | Positive reference input. The operating voltage range for this input is $1 \mathrm{~V} \leq \mathrm{V}_{\mathrm{REF}}{ }^{+} \leq \mathrm{V}_{\mathrm{A}}{ }^{+}$(see Figures 3 and 4 ). This pin should be bypassed to AGND at least with a parallel combination of a $10 \mu \mathrm{~F}$ and a $0.1 \mu \mathrm{~F}$ (ceramic) capacitor. The capacitors should be placed as close to the part as possible. |
| 9 | $\mathrm{V}_{\text {REF }}{ }^{-}$ | Negative reference input. The operating voltage range for this input is $0 \mathrm{~V} \leq \mathrm{V}_{\mathrm{REF}^{-}} \leq \mathrm{V}_{\text {REF }}{ }^{+}-1$ (see Figures 3 and 4 ). This pin should be bypassed to AGND at least with a parallel combination of a $10 \mu \mathrm{~F}$ and a $0.1 \mu \mathrm{~F}$ (ceramic) capacitor. The capacitors should be placed as close to the part as possible. |
| 4 | WMODE | The logic state of this pin at power-up determines which edge of the write signal ( $\overline{W R}$ ) will latch in data from the data bus. If tied low, the ADC12041 will latch in data on the rising edge of the $\overline{W R}$ signal. If tied to a logic high, data will be latched in on the falling edge of the $\overline{\mathrm{WR}}$ signal. The state of this pin should not be changed after power-up. |
| 27 | SYNC | The SYNC pin can be programmed as an input or an output. The Configuration register's bit b4 controls the function of this pin. When programmed as an input pin ( $b 4=1$ ), a rising edge on this pin causes the ADC's sample-and-hold to hold the analog input signal and begin conversion. When programmed as an output pin ( $\mathrm{b} 4=0$ ), the SYNC pin goes high when a conversion begins and returns low when completed. |
| $\begin{aligned} & 12-20 \\ & 23-26 \end{aligned}$ | $\begin{aligned} & \text { D0-D8 } \\ & \text { D9-D12 } \end{aligned}$ | 13-bit Data bus of the ADC12041. D12 is the most significant bit and D0 is the least significant. The BW (bus width) bit of the Configuration register (b3) selects between an 8-bit or 13-bit data bus width. When the $\mathbf{B W}$ bit is cleared $(B W=0), D 7-D 0$ are active and D12-D8 are always in TRI-STATE ${ }^{\circledR}$. When the BW bit is set (BW = 1), D12-D0 are active. |
| 28 | CLK | The clock input pin used to drive the ADC12041. The operating range is 0.05 MHz to 12 MHz . |
| 1 | $\overline{W R}$ | WR is the active low WRITE control input pin. A logic low on this pin and the $\overline{C S}$ will enable the input buffers of the data pins D12-D0. The signal at this pin is used by the ADC12041 to latch in data on D12-D0. The sense of the WMODE pin at power-up will determine which edge of the $\overline{W R}$ signal the ADC12041 will latch in data. See WMODE pin description. |
| 2 | $\overline{\mathrm{RD}}$ | $\overline{\mathrm{RD}}$ is the active low read control input pin. A logic low on this pin and $\overline{\mathrm{CS}}$ will enable the active output buffers to drive the data bus. |
| 3 | $\overline{\text { CS }}$ | $\overline{\mathrm{CS}}$ is the active low Chip Select input pin. Used in conjunction with the $\overline{\mathrm{WR}}$ and $\overline{\mathrm{RD}}$ signals to control the active data bus input/output buffers of the data bus. |
| 11 | $\overline{\text { RDY }}$ | $\overline{\mathrm{RDY}}$ is an active low output pin. The signal at this pin indicates when a requested function has begun or ended. Refer to section Functional Description and the digital timing diagrams for more detail. |
| 7 | $\mathrm{V}_{\mathrm{A}}{ }^{+}$ | Analog supply input pin. The device operating supply voltage range is $+5 \mathrm{~V} \pm 10 \%$. Accuracy is guaranteed only if the $\mathrm{V}_{\mathrm{A}}{ }^{+}$and $\mathrm{V}_{\mathrm{D}}{ }^{+}$are connected to the same potential. This pin should be bypassed to AGND with a parallel combination of a $10 \mu \mathrm{~F}$ and a $0.1 \mu \mathrm{~F}$ (ceramic) capacitor. The capacitors should be placed as close to the supply pins of the part as possible. |
| 8 | AGND | Analog ground pin. This is the device's analog supply ground connection. It should be connected through a low resistance and low inductance ground return to the system power supply. |
| 21 | $\mathrm{V}_{\mathrm{D}}{ }^{+}$ | Digital supply input pins. The device operating supply voltage range is $+5 \mathrm{~V} \pm 10 \%$. Accuracy is guaranteed only if the $\mathrm{V}_{\mathrm{A}}{ }^{+}$and $\mathrm{V}_{\mathrm{D}}+$ are connected to the same potential. This pin should be bypassed to DGND with a parallel combination of a $10 \mu \mathrm{~F}$ and a $0.1 \mu \mathrm{~F}$ (ceramic) capacitor. The capacitors should be placed as close to the supply pins of the part as possible. |
| 22 | DGND | Digital ground pin. This is the device's digital supply ground connection. It should be connected through a low resistance and low inductance ground return to the system power supply. |
|  | in SSOP |  <br> 28-Pin PLCC |

## Register Bit Description

## configuration register (Write Only)

This is an 8-bit write-only register that is used to program the functionality of the ADC12041. All data written to the ADC12041 will always go to this register only. The contents of this register cannot be read.
MSB

| $\mathrm{b}_{7}$ | $\mathrm{~b}_{6}$ | $\mathrm{~b}_{5}$ | $\mathrm{~b}_{4}$ | $\mathrm{~b}_{3}$ | $\mathrm{~b}_{2}$ | $\mathrm{~b}_{1}$ | $\mathrm{~b}_{0}$ |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| COMMAND <br> FIELD |  |  | SYNC | BW | SE | ACQ TIME |  |

Power on State: 10 Hex
$\mathbf{b}_{\mathbf{1}}-\mathbf{b}_{\mathbf{0}}$ : The ACQ TIME bits select one of four possible acquistion times in the SYNC-OUT mode ( $\mathbf{b}_{4}=0$ ). (Refer to Selectable Acquisition Time section, page 22).

| $\mathbf{b}_{\mathbf{1}}$ | $\mathbf{b}_{\mathbf{0}}$ | Clocks |
| :---: | :---: | :---: |
| 0 | 0 | 9 |
| 0 | 1 | 15 |
| 1 | 0 | 47 |
| 1 | 1 | 79 |

$\mathbf{b}_{\mathbf{2}}$ : When the Single-Ended bit (SE bit) is set, conversion results will be limited to positive values only and any negative conversion results will appear as a code of zero in the Data register. The SE bit is cleared at power-up
$b_{3}$ : This is the Bus Width (BW) bit. When this bit is cleared the ADC12041 is configured to interface with an 8-bit data bus; data pins $D_{7}-D_{0}$ are active and pins $D_{12}-D_{9}$ are in TRI-STATE. When the BW bit is set, the ADC12041 is configured to interface with a 16-bit data bus and data pins $D_{12}-D_{0}$ are all active. The BW bit is cleared at power-up.
$\mathbf{b}_{4}$ : The SYNC bit. When the SYNC bit is set, the SYNC pin is programmed as an input and the converter is in synchronous mode. In this mode a rising edge on the SYNC pin causes the ADC to hold the input signal and begin a conversion. When $b_{8}$ is cleared, the SYNC pin is programmed as an output and the converter is in an asynchronous mode. In this mode the signal at the SYNC pin indicates the status of the converter. The SYNC pin is high when a conversion is taking place. The SYNC bit is set at power-up.
$\mathbf{b}_{\mathbf{7}}-\mathbf{b}_{5}$ : The command field. These bits select the mode of operation of the ADC12041. Power-up value is 000 . (See Note 22)

| $\mathbf{b}_{\mathbf{7}}$ | $\mathbf{b}_{\mathbf{6}}$ | $\mathbf{b}_{\mathbf{5}}$ | Command |
| :---: | :---: | :---: | :--- |
| 0 | 0 | 0 | Standby command. This puts the ADC in a low power consumption mode. |
| 0 | 0 | 1 | Ful-Cal command. This will cause the ADC to perform a self-calibrating cycle that will correct linearity and zero <br> errors. |
| 0 | 1 | 0 | Auto-zero command. This will cause the ADC to perform an auto-zero cycle that corrects offset errors. |
| 0 | 1 | 1 | Reset command. This puts the ADC in an idle mode. |
| 1 | 0 | 0 | Start command. This will put the converter in a start mode, preparing it to perform a conversion. If in asynchronous <br> mode ( $\mathrm{b}_{4}=$ " 0 "), conversions will immediately begin after the programmed acquisition time has ended. In <br> synchronous mode $\left(b_{4}=" 1 "\right)$, conversions will begin after a rising edge appears on the SYNC pin. |

## DATA REGISTER (Read Only)

This is a 13-bit read only register that holds the 12-bit + sign conversion result in two's complement form. All reads performed from the ADC12041 will place the contents of this register on the data bus. When reading the data register in 8 -bit mode, the sign bit is extended.
MSB

| $\mathrm{b}_{12}$ | $\mathrm{~b}_{11}$ | $\mathrm{~b}_{10}$ | $\mathrm{~b}_{9}$ | $\mathrm{~b}_{8}$ | $\mathrm{~b}_{7}$ | $\mathrm{~b}_{6}$ | $\mathrm{~b}_{5}$ | $\mathrm{~b}_{4}$ | $\mathrm{~b}_{3}$ | $\mathrm{~b}_{2}$ | $\mathrm{~b}_{1}$ | $\mathrm{~b}_{0}$ |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| sign | Conversion Data |  |  |  |  |  |  |  |  |  |  |  |

Power on State: 0000 Hex
$\mathbf{b}_{11}-\mathbf{b}_{0}: b_{11}$ is the most significant bit and $b_{0}$ is the least significant bit of the conversion result. $\mathbf{b}_{12}$ : This bit contains the sign of the conversion result. 0 for positive results and 1 for negative.

## Functional Description

The ADC12041 is programmed through a digital interface that supports an 8 -bit or 16 -bit data bus. The digital interface consists of a 13-bit data input/output bus ( $D_{12}-D_{0}$ ), digital control signals and two internal registers: a write only 8 -bit Configuration register and a read only 13-bit Data register.
The Configuration register programs the functionality of the ADC12041. The 8 bits of the Configuration register are divided into 5 fields. Each field controls a specific function of the ADC12041: the acquisition time, synchronous or asynchronous conversions, mode of operation and the data bus size.

## Features and Operating Modes

## SELECTABLE BUS WIDTH

The ADC12041 can be programmed to interface with an 8 -bit or 16 -bit data bus. The BW bit $\left(b_{3}\right)$ in the Configuration register controls the bus size. The bus width is set to 8 bits ( $\mathrm{D}_{7}-\mathrm{D}_{0}$ are active and $\mathrm{D}_{12}-\mathrm{D}_{8}$ are in TRI-STATE) if the BW bit is cleared or 13 bits ( $D_{12}-D_{0}$ are active) if the $B W$ bit is set. At power-up the default bus width is 8 bits ( $\mathrm{BW}=0$ ). In 8-bit mode the Configuration register is accessed with a single write. When reading the ADC in 8 -bit mode, the first read cycle places the lower byte of the Data register on the data bus followed by the upper byte during the next read cycle.
In 13-bit mode all bits of the Data register and Configuration register are accessible with a single read or write cycle. Since the bus width of the ADC12041 defaults to 8 bits after power-up, the first action when 13-bit mode is desired must be to set the bus width to 13 bits.

## WMODE

The WMODE pin is used to determine the active edge of the write pulse. The state of this pin determines which edge of the $\overline{W R}$ signal will cause the ADC to latch in data. This is processor dependent. If the processor has valid data on the bus during the falling edge of the $\overline{\mathrm{WR}}$ signal, the WMODE pin must be tied to $\mathrm{V}_{\mathrm{D}}{ }^{+}$. This will cause the ADC to latch the data on the falling edge of the $\overline{W R}$ signal. If data is valid on the rising edge of the $\overline{\mathrm{WR}}$ signal, the WMODE pin must be tied to DGND causing the ADC to latch in the data on the rising edge of the $\overline{W R}$ signal.

## ANALOG INPUTS

The ADCIN + and ADCIN - are the fully differential noninverting (positive) and inverting (negative) inputs into the analog-to-digital converter (ADC) of the ADC12041.

## STANDBY MODE

The ADC12041 has a low power consumption mode ( $75 \mu \mathrm{~W}$ @ 5 V ). This mode is entered when a Standby command is written in the command field of the Configuration register. The RDY ouput pin is high when the ADC12041 is in the Standby mode. Any command other than the Standby command written to the Configuration register will get the ADC12041 out of the Standby mode. The RDY pin will immediately switch to a logic " 0 " when the ADC12041 is out of the standby mode. The ADC12041 defaults to the Standby mode following a hardware power-up.

## SYNC/ASYNC MODE

The ADC12041 may be programmed to operate in synchronous (SYNC-IN) or asynchronous (SYNC-OUT) mode. To enter synchronous mode, the SYNC bit in the Configuration register must be set. The ADC12041 is in synchronous mode after a hardware power-up. In this mode, the SYNC pin is programmed as an input and conversions are synchronized to the rising edges of the signal applied at the SYNC pin. Acquisition time can also be controlled by the SYNC signal when in synchronous mode. Refer to the syncin timing diagrams. When the SYNC bit is cleared, the ADC is in asynchronous mode and the SYNC pin is programmed as an output. In asynchronous mode, the signal at the SYNC pin indicates the status of the converter. This pin is high when the converter is performing a conversion. Refer to the sync-out timing diagrams.

## SELECTABLE ACQUISITION TIME

The ADC12041's internal sample/hold circuitry samples an input voltage by connecting the input to an internal sampling capacitor (approximately 70 pF ) through an effective resistance equal to the "On" resistance of the analog switch at the input to the sample/hold circuit ( $2500 \Omega$ typical) and the effective output resistance of the source. For conversion results to be accurate, the period during which the sampling capacitor is connected to the source (the "acquisition time") must be long enough to charge the capacitor to within a small fraction of an LSB of the input voltage. An acquisition time of 750 ns is sufficient when the external source resistance is less than $1 \mathrm{k} \Omega$ and any active or reactive source circuitry settles to 12 bits in less than 500 ns . When source resistance or source settling time increase beyond these limits, the acquisition time must also be increased to preserve precision.
In asynchronous (SYNC-OUT) mode, the acquisition time is controlled by an internal counter. The minimum acquisition period is 9 clock cycles, which corresponds to the nominal value of 750 ns when the clock frequency is 12 MHz . Bits $\mathrm{b}_{0}$ and $b_{1}$ of the Configuration Register are used to select the acquisition time from among four possible values ( $9,15,47$, or 79 clock cycles). Since acquisition time in the asynchronous mode is based on counting clock cycles, it is also inversely proportional to clock frequency:
$T_{\text {ACQ }}(\mu \mathrm{s})=\frac{\text { number of clock cycles }}{\mathrm{f}_{\mathrm{CLK}}(\mathrm{MHz})}$
Note that the actual acquisition time will be longer than $\mathrm{T}_{\mathrm{ACQ}}$ because acquisition begins either when the multiplexer channel is changed or when RDY goes low, if the multiplexer channel is not changed. After a read is performed, RDY goes high, which starts the $\mathrm{T}_{\mathrm{ACQ}}$ counter (see Figure 7).
In synchronous (SYNC-IN) mode, bits $b_{0}$ and $b_{1}$ are ignored, and the acquisition time depends on the sync signal applied to the SYNC pin. The acquisition period begins on the falling edge of RDY, which occurs at the end of the previous conversion (or at the end of an autozero or autocalibration procedure. The acquisition period ends when SYNC goes high.
To estimate the acquisition time necessary for accurate conversions when the source resistance is greater than $1 \mathrm{k} \Omega$, use the following expression:
$T_{\text {ACQMIN }}(\mu \mathrm{s})=\frac{0.75\left(\mathrm{R}_{\mathrm{S}}+\mathrm{R}_{\mathrm{S} / \mathrm{H}}\right)}{1 \mathrm{k} \Omega+\mathrm{R}_{\mathrm{S} / \mathrm{H}}}=\frac{0.75\left(\mathrm{R}_{\mathrm{S}}+2500\right)}{3500}$
where $\mathrm{R}_{\mathrm{S}}$ is the source resistance, and $\mathrm{R}_{\mathrm{S} / \mathrm{H}}$ is the sample/ hold "On" resistance.

## Features and Operating Modes (Continued)

If the settling time of the source is greater than 500 ns , the acquisition time should be about 300 ns longer than the settling time for a "well-behaved", smooth settling characteristic.

## FULL CALIBRATION CYCLE

A full calibration cycle compensates for the ADC's linearity and offset errors. The converter's DC specifications are guaranteed only after a full calibration has been performed. A full calibration cycle is initated by writing a Ful-Cal command to the ADC12041. During a full calibration, the offset error is measured eight times, averaged and a correction coefficient is created. The offset correction coefficient is stored in an internal offset correction register.
The overall linearity correction is achieved by correcting the internal DAC's capacitor mismatches. Each capacitor is compared eight times against all remaining smaller value capacitors. The errors are averaged out and correction coefficients are created.
Once the converter has been calibrated, an arithmetic logic unit (ALU) uses the offset and linearity correction coefficients to reduce the conversion offset and linearity errors to within guaranteed limits.

## AUTO-ZERO CYCLE

During an auto-zero cycle, the offset is measured only once and a correction coefficient is created and stored in an internal offset register. An auto-zero cycle is initiated by writing an Auto-Zero command to the ADC12041.

## DIGITAL INTERFACE

The digital control signals are $\overline{\mathrm{CS}}, \overline{\mathrm{RD}}, \overline{\mathrm{WR}}$ and $\overline{\mathrm{RDY}}$. Specific timing relationships are associated with the interaction of these signals. Refer to the Digital Timing Diagrams section for detailed timing specifications. The active low RDY signal indicates when a certain event begins and ends. It is recommended that the ADC12041 should only be accessed when the RDY signal is low. It is in this state that the ADC12041 is ready to accept a new command. This will minimize the effect of noise generated by a switching data bus on the ADC. The only exception to this is when the ADC12041 is in the standby mode at which time the $\overline{\mathrm{RDY}}$ is high. The ADC12041 is in the standby mode at power up or when a STANDBY command is issued. A Ful-Cal, Auto-Zero, Reset or Start command will get the ADC12041 out of the standby mode. This may be observed by monitoring the status of the $\overline{\text { RDY }}$ signal. The $\overline{R D Y}$ signal will go low when the ADC12041 leaves the standby mode.
The following describes the state of the digital control signals for each programmed event in both 8 -bit and 13-bit mode. $\overline{\text { RDY }}$ should be low before each command is issued except for the case when the device is in standby mode.

## FUL-CAL OR AUTO-ZERO COMMAND

8-bit mode: A Ful-Cal or Auto-Zero command must be issued and the BW bit $\left(b_{3}\right)$ cleared. The active edge of the write pulse on the WR pin will force the RDY signal high. At this time the converter begins executing a full calibration or auto-zero cycle. The RDY signal will automatically go low when the full calibration or auto-zero cycle is done.

13-bit mode: A Ful-Cal or Auto-Zero command must be issued and the BW bit $\left(b_{3}\right)$ set. The active edge of the write pulse on the WR pin will force the RDY signal high. At this time the converter begins executing a full calibration or auto-zero cycle. The $\overline{\text { RDY signal will automatically go low }}$ when the full calibration or auto-zero cycle is done.

## STARTING A CONVERSION: START COMMAND

In order to completely describe the events associated with the Start command, both the SYNC-OUT and SYNC-IN modes must be considered.
SYNC-OUT/Asynchronous
8-bit mode: A write to the ADC12041 should set the acquisition time, clear the BW and SYNC bit and select the START command in the Configuration register. In order to initiate a conversion, two reads must be performed from the ADC12041. The rising edge of the second read pulse will force the $\overline{\operatorname{RDY}}$ pin high and begin the programmed acquisition time selected by bits $b_{1}$ and $b_{0}$ of the Configuration register. The SYNC pin will go high indicating that a conversion sequence has begun following the end of the acquisition period. The RDY and SYNC signal will fall low when the conversion is done. At this time new information, such as a new acquisition time and operational command can be written into the Configuration register or it can remain unchanged. Assuming that the START command is in the Configuration register, the previous conversion can be read. The first read places the lower byte of the conversion result contained in the Data register on the data bus. The second read will place the upper byte of the conversion result stored in the Data register on the data bus. The rising edge on the second read pulse will begin another conversion sequence and raise the RDY and SYNC signals appropriately.
13-bit mode: The acquisition time should be set, the BW bit set, the SYNC bit cleared and the START command issued with a write to the ADC12041. In order to initiate a conversion, a single read must be performed from the ADC12041. The rising edge of the read signal will force the RDY signal high and begin the programmed acquisition time selected by bits $b_{1}$ and $b_{0}$ of the configuration register. The SYNC pin will go high indicating that a conversion sequence has begun following the end of the acquisition period. The RDY and SYNC signal will fall low when the conversion is done. At this time new information, such as a new acquisition time and operational command can be written into the Configuration register or it can remain unchanged. With the START command in the Configuration register, a read from the ADC12041 will place the entire 13-bit conversion result stored in the data register on the data bus. The rising edge of the read pulse will immediately force the $\overline{\text { RDY output high }}$ and begin the programmed acquisition time selected by bits $b_{1}$ and $b_{0}$ of the configuration register. The SYNC will then go high at the end of the programmed acquisition time.

## Features and Operating Modes (Continued)

SYNC-IN/Synchronous
For the SYNC-IN case, it is assumed that a series of SYNC pulses at the desired sampling rate are applied at the SYNC pin of the ADC12041.
8-bit mode: A write to the ADC12041 should set the SYNC bit, write the START command and clear the BW bit. The programmed acquisition time in bits $b_{1}$ and $b_{0}$ is a don't care condition in the SYNC-IN mode.
A rising edge on the SYNC pin or the second rising edge of two consecutive reads from the ADC12041 will force the $\overline{\mathrm{RDY}}$ signal high. It is recommended that the action of reading from the ADC12041 (not the rising edge of the SYNC signal) be used to raise the $\overline{\mathrm{RDY}}$ signal. This will ensure that the conversion result is read during the acquisition period of the next conversion cycle, eliminating a read from the ADC12041 while it is performing a conversion. Noise generated by accessing the ADC12041 while it is converting may degrade the conversion result. In the SYNC-IN mode, only the rising edge of the SYNC signal will begin a conversion cycle. The rising edge of the SYNC also ends the acquisition period. The acquisition period begins after the falling edge of the RDY signal. The input is sampled until the rising edge of the SYNC pulse, at which time the signal will be held and conversion begins. The RDY signal will go low when the conversion is done and a new operational command may be written into the Configuration register at this time, if needed. Two consecutive read cycles are required to retrieve the entire 13 -bit conversion result from the ADC12041's Data register. The first read will place the lower byte of the conversion result contained in the Data register on the data bus. The second read will place the upper byte of the conversion result stored in the Data register on the data bus. With the START command in the configuration register, the rising edge of the second read pulse will raise the RDY signal high and begin a conversion cycle following a rising edge on the SYNC pin.

13-bit mode: The SYNC bit and the BW bit should be set and the START command issued with a write to the ADC12041. A rising edge on the SYNC pin or on the RD pin will force the $\overline{\mathrm{RDY}}$ signal high. It is recommended that the action of reading from the ADC12041 (not the rising edge of the SYNC signal) be used to raise the $\overline{\mathrm{RDY}}$ signal. This will ensure that the conversion result is read during the acquisition period of the next conversion cycle, eliminating a read from the ADC12041 while it is performing a conversion. Noise generated by accessing the ADC12041 while it is converting may degrade the conversion result. In the SYNCIN mode, only the rising edge of the SYNC signal will begin a conversion cycle. The $\overline{R D Y}$ signal will go low when the conversion cycle is done. The acquisition time is controlled by the SYNC signal. The acquisition period begins after the falling edge of the $\overline{\operatorname{RDY}}$ signal. The input is sampled until the rising edge of the SYNC pulse, at which time the signal will be held and conversion begins. The $\overline{\mathrm{RDY}}$ signal will go low when the conversion is done and a new operational command may be written into the Configuration register at this time, if needed. With the START command in the Configuration register, a read from the ADC12041 will place the entire conversion result stored in the Data register on the data bus and the rising edge of the read pulse will force the RDY signal high.

## STANDBY COMMAND

8-bit mode: A write to the ADC12041 should clear the BW bit and issue the Standby command.
13-bit mode: A write to the ADC12041 should set the BW bit and issue the Standby command.

## RESET

The RESET command places the ADC12041 into a ready state and forces the RDY signal low. The RESET command can be used to interrupt the ADC12041 while it is performing a conversion, full-calibration or auto-zero cycle. It can also be used to get the ADC12041 out of the standby mode.

## Analog Application Information

## reference voltage

The ADC12041 has two reference inputs, $\mathrm{V}_{\text {REF }}{ }^{+}$and $\mathrm{V}_{\text {REF }}{ }^{-}$. They define the zero to full-scale range of the analog input signals over which 4095 positive and 4096 negative codes exist. The reference inputs can be connected to span the entire supply voltage range ( $\mathrm{V}_{\mathrm{REF}}{ }^{-}=$AGND, $\mathrm{V}_{\mathrm{REF}}{ }^{+}=\mathrm{V}_{\mathrm{A}}{ }^{+}$) or they can be connected to different voltages when other input spans are required. The reference inputs of the ADC12041 have transient capacitive switching currents. The voltage sources driving $\mathrm{V}_{\text {REF }}{ }^{+}$and $\mathrm{V}_{\text {REF }}{ }^{-}$ must have very low output impedence and noise and must be adequately bypassed. The circuit in Figure 8 is an example of a very stable reference source.
The ADC12041 can be used in either ratiometric or absolute reference applications. In ratiometric systems, the analog input voltage is proportional to the voltage used for the ADC's reference voltage. This technique relaxes the system reference requirements because the analog input voltage moves with the ADC's reference. The system power supply can be used as the reference voltage by connecting the $\mathrm{V}_{\mathrm{REF}}{ }^{+}$pin to $\mathrm{V}_{\mathrm{A}}{ }^{+}$and the $\mathrm{V}_{\text {REF }}{ }^{-}$pin to AGND. For absolute accuracy, where the analog input voltage varies between very specific voltage limits, a time and temperature stable voltage source can be connected to the reference inputs. Typically, the reference voltage's magnitude will require an initial adjustment to null reference voltage induced full-scale errors.
The reference voltage inputs are not fully differential. The ADC12041 will not generate correct conversions if $\mathrm{V}_{\text {REF }}{ }^{+}$$\mathrm{V}_{\mathrm{REF}}{ }^{-}$is below 1 V . Figure 9 shows the allowable relationship between $\mathrm{V}_{\text {REF }}{ }^{+}$and $\mathrm{V}_{\text {REF }}{ }^{-}$.


TL/H/12441-43
FIGURE 9. VREF Operating Range OUTPUT DIGITAL CODE VERSUS ANALOG INPUT VOLTAGE
The ADC12041's fully differential 12-bit + sign ADC generates a two's complement output that is found by using the equation shown below:
Output code $=\frac{\left(\mathrm{V}_{\mathrm{IN}^{+}}-\mathrm{V}_{\mathrm{IN}^{-}}\right)(4096)}{\left(\mathrm{V}_{\text {REF }^{+}}-\mathrm{V}_{\mathrm{REF}^{-}}\right)}$
Round off the result to the nearest integer value between -


FIGURE 8. Low Drift Extremely Stable Reference Circuit

| Part Number | Output Voltage <br> Tolerance | Temperature <br> Coefficient |
| :--- | :---: | :---: |
| LM4041CI-Adj | $\pm 0.5 \%$ | $\pm 100 \mathrm{ppm} /{ }^{\circ} \mathrm{C}$ |
| LM4040AI-4.1 | $\pm 0.1 \%$ | $\pm 100 \mathrm{ppm} /{ }^{\circ} \mathrm{C}$ |
| LM9140BYZ-4.1 | $\pm 0.5 \%$ | $\pm 25 \mathrm{ppm} /{ }^{\circ} \mathrm{C}$ |
| LM368Y-5.0 | $\pm 0.1 \%$ | $\pm 20 \mathrm{ppm} /{ }^{\circ} \mathrm{C}$ |
| Circuit of Figure 8 | Adjustable | $\pm 2 \mathrm{ppm} /{ }^{\circ} \mathrm{C}$ |

## Analog Application Information (Continued)

## INPUT CURRENT

At the start of the acquisition window ( $\mathrm{t}_{\text {AcqSYNOUT }}$ ) a charging current (due to capacitive switching) flows through the analog input pins (ADCIN + and ADCIN-). The peak value of this input current will depend on the amplitude and frequency of the input voltage applied, the source impedance and the ADCIN + and ADCIN - input switch ON resistance of $2500 \Omega$.

For low impedance voltage sources ( $1000<\Omega$ for 12 MHz operation), the input charging current will decay to a value that will not introduce any conversion errors before the end of the default sample-and-hold (S/H) acquisition time ( 9 clock cycles). For higher source impedances (1000 $>\Omega$ for 12 MHz operation), the S/H acquisition time should be increased to allow the charging current to settle within spec ified limits. In asynchronous mode, the acquisition time may be increased to 15,47 or 79 clock cycles. If different acquisition times are needed, the synchronous mode can be used to fully control the acquisition time.

## INPUT BYPASS CAPACITANCE

External capacitors ( $0.01 \mu \mathrm{~F}-0.1 \mu \mathrm{~F}$ ) can be connected between the ADCIN + and ADCIN - analog input pins and the analog ground to filter any noise caused by inductive pickup associated with long leads.

## POWER SUPPLY CONSIDERATIONS

Decoupling and bypassing the power supply on a high resolution ADC is an important design task. Noise spikes on the $\mathrm{V}_{\mathrm{A}}{ }^{+}$(analog supply) or $\mathrm{V}_{\mathrm{D}}{ }^{+}$(digital supply) can cause conversion errors. The analog comparator used in the ADC will respond to power supply noise and will make erroneous conversion decisions. The ADC is especially sensitive to power supply spikes that occur during the auto-zero or linearity calibration cycles.
The ADC12041 is designed to operate from a single +5 V power supply. The separate supply and ground pins for the analog and digital portions of the circuit allow separate external bypassing. To minimize power supply noise and ripple, adequate bypass capacitors should be placed directly between power supply pins and their associated grounds. Both supply pins should be connected to the same supply source. In systems with separate analog and digital supplies, the ADC should be powered from the analog supply. At least a $10 \mu \mathrm{~F}$ tantalum electrolytic capacitor in parallel with a $0.1 \mu \mathrm{~F}$ monolithic ceramic capacitor is recommended for bypassing each power supply. The key consideration for these capacitors is to have low series resistance and inductance. The capacitors should be placed as close as physically possible to the supply and ground pins with the smaller capacitor closer to the device. The capacitors also should have the shortest possible leads in order to minimize series lead inductance. Surface mount chip capacitors are optimal in this respect and should be used when possible.
When the power supply regulator is not local on the board, adequate bypassing (a high value electrolytic capacitor) should be placed at the power entry point. The value of the capacitor depends on the total supply current of the circuits
on the PC board. All supply currents should be supplied by the capacitor instead of being drawn from the external supply lines, while the external supply charges the capacitor at a steady rate.
The ADC has two $\mathrm{V}_{\mathrm{D}}{ }^{+}$and DGND pins. It is recommended to use a $0.1 \mu \mathrm{~F}$ plus a $10 \mu \mathrm{~F}$ capacitor between pin $21\left(\mathrm{~V}_{\mathrm{D}}+\right.$ ) and 22 (DGND) the SSOP and PLCC package. The layout diagram in Figure 10 shows the recommended placement for the supply bypass capacitors.

## PC BOARD LAYOUT AND GROUNDING

 CONSIDERATIONSTo get the best possible performance from the ADC12041, the printed circuit boards should have separate analog and digital ground planes. The reason for using two ground planes is to prevent digital and analog ground currents from sharing the same path until they reach a very low impedance power supply point. This will prevent noisy digital switching currents from being injected into the analog ground.
Figure 10 illustrates a favorable layout for ground planes, power supply and reference input bypass capacitors. It shows a layout using a 28 -pin PLCC socket and throughhole assembly. A similar approach should be used for the SSOP package.
The analog ground plane should encompass the area under the analog pins and any other analog components such as the reference circuit, input amplifiers, signal conditioning circuits, and analog signal traces.
The digital ground plane should encompass the area under the digital circuits and the digital input/output pins of the ADC12041. Having a continuous digital ground plane under the data and clock traces is very important. This reduces the overshoot/undershoot and high frequency ringing on these lines that can be capacitively coupled to analog circuitry sections through stray capacitances.
The AGND and DGND in the ADC12041 are not internally connected together. They should be connected together on the PC board right at the chip. This will provide the shortest return path for the signals being exchanged between the internal analog and digital sections of the ADC.
It is also a good design practice to have power plane layers in the PC board. This will improve the supply bypassing (an effective distributed capacitance between power and ground plane layers) and voltage drops on the supply lines. However, power planes are not as essential as ground planes are for satisfactory performance. If power planes are used, they should be separated into two planes and the area and connections should follow the same guidelines as mentioned for the ground planes. Each power plane should be laid out over its associated ground planes, avoiding any overlap between power and ground planes of different types. When the power planes are not used, it is recommended to use separate supply traces for the $\mathrm{V}_{\mathrm{A}^{+}}$and $\mathrm{V}_{\mathrm{D}}{ }^{+}$pins from a low impedance supply point (the regulator output or the power entry point to the PC board). This will help ensure that the noisy digital supply does not corrupt the analog supply.

## Analog Application Information (Continued)



FIGURE 10. Top View of Printed Circuit Board for a 28-Pin PLCC ADC12041

When measuring AC input signals, any crosstalk between analog input lines and the reference lines (ADCIN $\pm$, $\mathrm{V}_{\text {REF }}{ }^{ \pm}$) should be minimized. Crosstalk is minimized by reducing any stray capacitance between the lines. This can be done by increasing the clearance between traces, keeping the traces as short as possible, shielding traces from each other by placing them on different sides of the AGND plane, or running AGND traces between them.
Figure 10 also shows the reference input bypass capacitors. Here the reference inputs are considered to be differential. The performance improves by having a $0.1 \mu \mathrm{~F}$ capacitor
between the $\mathrm{V}_{\text {REF }}{ }^{+}$and $\mathrm{V}_{\text {REF }}{ }^{-}$, and by bypassing in a manner similar to that described for the supply pins. When a single ended reference is used, $\mathrm{V}_{\mathrm{REF}}{ }^{-}$is connected to AGND and only two capacitors are used between $\mathrm{V}_{\text {REF }}{ }^{+}$ and $\mathrm{V}_{\text {REF }}{ }^{-}(0.1 \mu \mathrm{~F}+10 \mu \mathrm{~F})$. It is recommended to directly connect the AGND side of these capacitors to the $\mathrm{V}_{\text {REF }}{ }^{-}$ instead of connecting $\mathrm{V}_{\text {REF }}{ }^{-}$and the ground sides of the capacitors separately to the ground planes. This provides a significantly lower-impedance connection when using surface mount technology.


Physical Dimensions inches (millimeters)


## 28-Lead Molded Plastic Leaded Chip Carrier <br> Order Number ADC12041CIV <br> NS Package Number V28A




## Connection Diagrams



Order Number ADC12048CIV See NS Package Number V44A


TL/H/12387-3
Order Number ADC12048CIVF See NS Package Number VGZ44A

## Ordering Information

| Industrial Temperature Range <br> $-\mathbf{4 0} \mathbf{C} \leq \mathbf{T}_{\mathbf{A}} \leq+\mathbf{8 5}$ <br>  <br> $\mathbf{C}$ | Package |
| :---: | :---: |
| ADC 12048 CIV | V44A |
| $\mathrm{ADC12048CIVF}$ | VGZ44A |

Absolute Maximum Ratings (Notes 1 and 2)
If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.
Supply Voltage ( $\mathrm{V}_{\mathrm{A}}{ }^{+}$and $\mathrm{V}_{\mathrm{D}}{ }^{+}$) 6.0 V

Voltage at all Inputs
$\left|V_{A^{+}}-V_{D}{ }^{+}\right|$
|AGND - DGND|
Input Current at Any Pin (Note 3)
-0.3 V to $\mathrm{V}^{+}+0.3 \mathrm{~V}$
300 mV
$\pm 30 \mathrm{~mA}$
$\pm 120 \mathrm{~mA}$


Converter DC Characteristics The following specifications apply to the $\operatorname{ADC12048}$ for $\mathrm{V}_{\mathrm{A}}{ }^{+}=\mathrm{V}_{\mathrm{D}}{ }^{+}=5 \mathrm{~V}$, $\mathrm{V}_{\mathrm{REF}}{ }^{+}=4.096 \mathrm{~V}, \mathrm{~V}_{\mathrm{REF}}{ }^{-}=0.0 \mathrm{~V}, 12$-bit + sign conversion mode, $\mathrm{f}_{\mathrm{CLK}}=12.0 \mathrm{MHz}, \mathrm{R}_{\mathrm{S}}=25 \Omega$, source impedance for $\mathrm{V}_{\mathrm{REF}}{ }^{+}$ and $\mathrm{V}_{\text {REF }}{ }^{-} \leq 1 \Omega$, fully differential input with fixed 2.048 V common-mode voltage ( $\mathrm{V}_{\text {INCM }}$ ), and minimum acquisition time, unless otherwise specified. Boldface limits apply for $\mathbf{T}_{\mathbf{A}}=\mathbf{T}_{\mathbf{J}}=\mathbf{T}_{\mathbf{M I N}}$ to $\mathbf{T}_{\mathbf{M A X}}$; all other limits $\mathrm{T}_{\mathbf{A}}=\mathrm{T}_{\mathrm{J}}=25^{\circ} \mathrm{C}$

| Symbol | Parameter | Conditions | Typical (Note 10) | Limits (Note 11) | $\begin{gathered} \text { Unit } \\ \text { (Limit) } \end{gathered}$ |
| :---: | :---: | :---: | :---: | :---: | :---: |
|  | Resolution with No Missing Codes | After Auto-Cal |  | 13 | Bits (max) |
| ILE | Positive and Negative Integral Linearity Error | After Auto-Cal <br> (Notes 12 and 17) | $\pm 0.6$ | $\pm 1$ | LSB (max) |
| DNL | Differential Non-Linearity | After Auto-Cal |  | $\pm 1$ | LSB (max) |
|  | Zero Error | After Auto-Cal (Notes 13 and 17) $\begin{aligned} & \mathrm{V}_{\text {INCM }}=5.0 \mathrm{~V} \\ & \mathrm{~V}_{\text {INCM }}=2.048 \mathrm{~V} \\ & \mathrm{~V}_{\text {INCM }}=0 \mathrm{~V} \end{aligned}$ |  | $\begin{array}{r}  \pm 5.5 \\ \pm \mathbf{2 . 5} \\ \pm \mathbf{5 . 5} \\ \hline \end{array}$ | LSB (max) |
|  | Positive Full-Scale Error | After Auto-Cal (Notes 12 and 17) | $\pm 1.0$ | $\pm 2.5$ | LSB (max) |
|  | Negative Full-Scale Error | After Auto-Cal (Notes 12 and 17) | $\pm 1.0$ | $\pm 2.5$ | LSB (max) |
|  | DC Common Mode Error | After Auto-Cal (Note 14) | $\pm 2$ | $\pm 5.5$ | LSB (max) |
| TUE | Total Unadjusted Error | After Auto-Cal (Note 18) | $\pm 1$ |  | LSB |

Power Supply Characteristics The following specifications apply to the ADC12048 for $\mathrm{V}_{\mathrm{A}}{ }^{+}=\mathrm{V}_{\mathrm{D}}{ }^{+}=5 \mathrm{~V}$, $\mathrm{V}_{\text {REF }}{ }^{+}=4.096 \mathrm{~V}, \mathrm{~V}_{\text {REF }}{ }^{-}=0.0 \mathrm{~V}$, 12 -bit + sign conversion mode, $\mathrm{f}_{\mathrm{CLK}}=12.0 \mathrm{MHz}, \mathrm{R}_{\mathrm{S}}=25 \Omega$, source impedance for $\mathrm{V}_{\text {REF }}{ }^{+}$ and $\mathrm{V}_{\text {REF }}{ }^{-} \leq 1 \Omega$, fully differential input with fixed 2.048 V common-mode voltage, and minimum acquisition time, unless otherwise specified. Boldface limits apply for $\mathbf{T}_{\mathbf{A}}=\mathbf{T}_{\mathbf{J}}=\mathbf{T}_{\mathbf{M I N}}$ to $\mathbf{T}_{\mathbf{M A X}}$; all other limits $\mathrm{T}_{\mathbf{A}}=\mathrm{T}_{\mathrm{J}}=25^{\circ} \mathrm{C}$

| Symbol | Parameter | Conditions | Typical (Note 10) | Limits (Note 11) | $\begin{aligned} & \text { Unit } \\ & \text { (Limit) } \end{aligned}$ |
| :---: | :---: | :---: | :---: | :---: | :---: |
| PSS | Power Supply Sensitivity Zero Error Full-Scale Error Linearity Error | $\begin{aligned} & \mathrm{V}_{\mathrm{D}^{+}}=\mathrm{V}_{\mathrm{A}^{+}}=5.0 \mathrm{~V} \pm 10 \% \\ & \mathrm{~V}_{\mathrm{REF}}{ }^{+}=4.096 \mathrm{~V} \\ & \mathrm{~V}_{\mathrm{REF}}{ }^{-}=0 \mathrm{~V} \end{aligned}$ | $\begin{aligned} & \pm 0.1 \\ & \pm 0.5 \\ & \pm 0.1 \end{aligned}$ |  | $\begin{aligned} & \text { LSB } \\ & \text { LSB } \\ & \text { LSB } \end{aligned}$ |
| $\mathrm{ID}^{+}$ | $\mathrm{V}_{\mathrm{D}}+$ Digital Supply Current | Start Command (Performing a conversion) with SYNC configured as an input and driven with a 214 kHz signal. Bus width set to 13 . <br> $\mathrm{f}_{\mathrm{CLK}}=12.0 \mathrm{MHz}$, Reset Mode <br> $\mathrm{f}_{\mathrm{CLK}}=12.0 \mathrm{MHz}$, Conversion | $\begin{aligned} & 850 \\ & 2.45 \end{aligned}$ | 2.8 | $\begin{gathered} \mu \mathrm{A} \\ \mathrm{~mA}(\max ) \end{gathered}$ |
| $\mathrm{I}_{\mathrm{A}}+$ | $\mathrm{V}_{\mathrm{A}}+$ Analog Supply Current | Start Command (Performing a conversion) with SYNC configured as an input and driven with a 214 kHz signal. Bus width set to 13 . <br> $\mathrm{f}_{\mathrm{CLK}}=12.0 \mathrm{MHz}$, Reset Mode <br> $\mathrm{f}_{\mathrm{CLK}}=12.0 \mathrm{MHz}$, Conversion | $\begin{aligned} & 2.3 \\ & 2.3 \end{aligned}$ | 4.0 | $\begin{gathered} \mathrm{mA} \\ \mathrm{~mA}(\max ) \end{gathered}$ |
| $\mathrm{I}_{\text {ST }}$ | Standby Supply Current $\left(I_{D^{+}}+I_{A}^{+}\right)$ | Standby Mode <br> $\mathrm{f}_{\mathrm{CLK}}=$ Stopped <br> $\mathrm{f}_{\mathrm{CLK}}=12.0 \mathrm{MHz}$ | $\begin{gathered} 5 \\ 100 \end{gathered}$ | $\begin{gathered} 15 \\ 120 \end{gathered}$ | $\mu \mathrm{A}$ (max) <br> $\mu \mathrm{A}$ (max) |

Analog MUX Inputs Characteristics The following specifications apply to the ADC12048 for $\mathrm{V}_{\mathrm{A}^{+}}=$ $\mathrm{V}_{\mathrm{D}+}=5 \mathrm{~V}, \mathrm{~V}_{\mathrm{REF}}{ }^{+}=4.096 \mathrm{~V}, \mathrm{~V}_{\mathrm{REF}}{ }^{-}=0.0 \mathrm{~V}$, 12 -Bit + sign conversion mode, $\mathrm{f}_{\mathrm{CLK}}=12.0 \mathrm{MHz}, \mathrm{Rs}_{\mathrm{S}}=25 \Omega$, source impedance for $\mathrm{V}_{\text {REF }}{ }^{+}$and $\mathrm{V}_{\text {REF }}{ }^{+} \leq 1 \Omega$, fully differential input with fixed 2.048 V common-mode voltage, and minimum acquisition time, unless otherwise specified. Boldface limits apply for $\mathbf{T}_{\mathbf{A}}=\mathbf{T}_{\mathbf{J}}=\mathbf{T}_{\mathbf{M I N}}$ to $\mathbf{T}_{\mathbf{M A X}}$; all other limits $\mathrm{T}_{\mathbf{A}}=\mathrm{T}_{\mathrm{J}}=$ $25^{\circ} \mathrm{C}$

| Symbol | Parameter | Conditions | Typical (Note 10) | Limits (Note 11) | Unit (Limit) |
| :---: | :---: | :---: | :---: | :---: | :---: |
| Ion | MUX ON Channel Leakage Current | ON Channel $=5 \mathrm{~V}$, OFF Channel $=0 \mathrm{~V}$ ON Channel $=0 \mathrm{~V}$, OFF Channel $=5 \mathrm{~V}$ | $\begin{gathered} 0.05 \\ -0.05 \end{gathered}$ | $\begin{gathered} 1.0 \\ -1.0 \end{gathered}$ | $\mu \mathrm{A}(\min )$ <br> $\mu \mathrm{A}$ (max) |
| IofF | MUX OFF Channel Leakage Current | ON Channel $=5 \mathrm{~V}$, OFF Channel $=0 \mathrm{~V}$ ON Channel $=0 \mathrm{~V}$, OFF Channel $=5 \mathrm{~V}$ | $\begin{gathered} 0.05 \\ -0.05 \end{gathered}$ | $\begin{gathered} 1.0 \\ -1.0 \end{gathered}$ | $\mu \mathrm{A}$ (min) <br> $\mu \mathrm{A}$ (max) |
| $\mathrm{I}_{\text {ADCIN }}$ | ADCIN Input Leakage Current |  | 0.05 | 2.0 | $\mu \mathrm{A}$ (max) |
| RON | MUX On Resistance | $\mathrm{V}_{\text {IN }}=2.5 \mathrm{~V}$ | 310 | 500 | $\Omega$ (max) |
|  | MUX Channel-to-Channel RON Matching | $\mathrm{V}_{\mathrm{IN}}=2.5 \mathrm{~V}$ | $\pm 20 \%$ |  | $\Omega$ |
| $\mathrm{C}_{\text {mux }}$ | MUX Channel and COM Input Capacitance |  | 10 |  | pF |
| $\mathrm{C}_{\text {ADC }}$ | ADCIN Input Capacitance |  | 70 |  | pF |
| $\mathrm{C}_{\text {MUXOUT }}$ | MUX Output Capacitance |  | 20 |  | pF |

Reference Inputs The following specifications apply to the $\mathrm{ADC1} 2048$ for $\mathrm{V}_{\mathrm{A}^{+}}=\mathrm{V}_{\mathrm{D}^{+}}=5 \mathrm{~V}, \mathrm{~V}_{\mathrm{REF}}{ }^{+}=4.096 \mathrm{~V}$, $\mathrm{V}_{\text {REF }}{ }^{-}=0.0 \mathrm{~V}, 12$-bit + sign conversion mode, $\mathrm{f}_{\mathrm{CLK}}=12.0 \mathrm{MHz}, \mathrm{R}_{\mathrm{S}}=25 \Omega$, source impedance for $\mathrm{V}_{\text {REF }}{ }^{+}$and $\mathrm{V}_{\text {REF }}{ }^{-} \leq$ $1 \Omega$, fully differential input with fixed 2.048 V common-mode voltage, and minimum acquisition time, unless otherwise specified. Boldface limits apply for $\mathbf{T}_{\mathbf{A}}=\mathbf{T}_{\mathbf{J}}=\mathbf{T}_{\mathbf{M I N}}$ to $\mathbf{T}_{\mathbf{M A X}}$; all other limits $\mathrm{T}_{\mathbf{A}}=\mathrm{T}_{\mathbf{J}}=25^{\circ} \mathrm{C}$

| Symbol | Parameter | Conditions | Typical <br> (Note 10) | Limits <br> (Note 11) | Unit <br> (Limit) |
| :--- | :---: | :---: | :---: | :---: | :---: |
| $I_{\text {REF }}$ | Reference Input Current | $\mathrm{V}_{\text {REF }}+4.096 \mathrm{~V}, \mathrm{~V}_{\text {REF- }}=0 \mathrm{~V}$ |  |  |  |
|  |  | Analog Input Signal: 1 kHz | 145 |  | $\mu \mathrm{~A}$ |
|  |  | (Note 20) $\quad 80 \mathrm{kHz}$ | 136 |  | $\mu \mathrm{~A}$ |
| C |  |  | 85 |  | pF |

Digital Logic Input/Output Characteristics The following specifications apply to the ADC12048 for $\mathrm{V}_{\mathrm{A}^{+}}=\mathrm{V}_{\mathrm{D}}{ }^{+}=5 \mathrm{~V}, \mathrm{~V}_{\mathrm{REF}}{ }^{+}=4.096 \mathrm{~V}, \mathrm{~V}_{\mathrm{REF}}{ }^{-}=0.0 \mathrm{~V}, 12$-bit + sign conversion mode, $\mathrm{f}_{\mathrm{CLK}}=12.0 \mathrm{MHz}, \mathrm{R}_{\mathrm{S}}=25 \Omega$, source impedance for $\mathrm{V}_{\text {REF }}{ }^{+}$and $\mathrm{V}_{\text {REF }}{ }^{-} \leq 1 \Omega$, fully differential input with fixed 2.048 V common-mode voltage, and minimum acquisition time, unless otherwise specified. Boldface limits apply for $\mathbf{T}_{\mathbf{A}}=\mathbf{T}_{\mathbf{J}}=\mathbf{T}_{\mathbf{M I N}} \mathbf{t o} \mathbf{T}_{\mathbf{M A X}}$; all other limits $\mathrm{T}_{\mathbf{A}}=\mathrm{T}_{\mathbf{J}}=$ $25^{\circ} \mathrm{C}$

| Symbol | Parameter | Conditions | Typical (Note 10) | $\begin{aligned} & \text { Limits } \\ & \text { (Note 11) } \end{aligned}$ | Unit (Limit) |
| :---: | :---: | :---: | :---: | :---: | :---: |
| $\mathrm{V}_{1 \mathrm{H}}$ | Logic High Input Voltage | $\mathrm{V}_{\mathrm{A}^{+}}=\mathrm{V}^{+}{ }^{+}=5.5 \mathrm{~V}$ |  | 2.0 | V (min) |
| $\mathrm{V}_{\text {IL }}$ | Logic Low Input Voltage | $\mathrm{V}_{\mathrm{A}^{+}}=\mathrm{V}_{\mathrm{D}}{ }^{+}=4.5 \mathrm{~V}$ |  | 0.8 | $V(\max )$ |
| $\mathrm{I}_{\mathrm{H}}$ | Logic High Input Current | $\mathrm{V}_{\mathrm{IN}}=5 \mathrm{~V}$ | 0.035 | 2.0 | $\mu \mathrm{A}$ (max) |
| I/L | Logic Low Input Current | $\mathrm{V}_{\mathrm{IN}}=0 \mathrm{~V}$ | -0.035 | -2.0 | $\mu \mathrm{A}$ (max) |
| $\mathrm{V}_{\mathrm{OH}}$ | Logic High Output Voltage | $\begin{aligned} & \mathrm{V}_{\mathrm{A}^{+}}=\mathrm{V}_{\mathrm{D}^{+}}=4.5 \mathrm{~V} \\ & \mathrm{I}_{\text {OUT }}=-1.6 \mathrm{~mA} \\ & \hline \end{aligned}$ |  | 2.4 | $V$ (min) |
| VOL | Logic Low Output Voltage | $\begin{aligned} & \mathrm{V}_{\mathrm{A}^{+}}=\mathrm{V}_{\mathrm{D}^{+}}=4.5 \mathrm{~V} \\ & \text { IOUT }=1.6 \mathrm{~mA} \end{aligned}$ |  | 0.4 | V (max) |
| IofF | TRI-STATE® Output Leakage Current | $\begin{aligned} & \mathrm{V}_{\text {OUT }}=0 \mathrm{~V} \\ & \mathrm{~V}_{\text {OUT }}=5 \mathrm{~V} \end{aligned}$ |  | $\pm 2.0$ | $\mu \mathrm{A}$ (max) |
| $\mathrm{ClN}_{\text {IN }}$ | D12-D0 Input Capacitance |  | 10 |  | pF |

Converter AC Characteristics The following specifications apply to the ADC12048 for $\mathrm{V}_{\mathrm{S}^{+}}=\mathrm{V}_{\mathrm{D}}{ }^{+}=5 \mathrm{~V}$, $\mathrm{V}_{\text {REF }}{ }^{+}=4.096 \mathrm{~V}, \mathrm{~V}_{\text {REF }}{ }^{-}=0.0 \mathrm{~V}, 12$-bit + sign conversion mode, $\mathrm{f}_{\mathrm{CLK}}=12.0 \mathrm{MHz}, \mathrm{R}_{\mathrm{S}}=25 \Omega$, source impedance for $\mathrm{V}_{\text {REF }}{ }^{+}$ and $\mathrm{V}_{\text {REF }}{ }^{-} \leq 1 \Omega$, fully differential input with fixed 2.048 V common-mode voltage, and minimum acquisition time, unless otherwise specified. Boldface limits apply for $\mathbf{T}_{\mathbf{A}}=\mathbf{T}_{\mathbf{J}}=\mathbf{T}_{\text {MIN }}$ to $\mathbf{T}_{\mathbf{M A X}}$; all other limits $\mathrm{T}_{\mathbf{A}}=\mathrm{T}_{\mathbf{J}}=25^{\circ} \mathrm{C}$

| Symbol | Parameter | Conditions | Typical (Note 10) | Limits (Note 11) | Unit (Limit) |
| :---: | :---: | :---: | :---: | :---: | :---: |
| $\mathrm{t}_{\mathrm{z}}$ | Auto Zero Time |  | 78 | 78 clks + 120 ns | clks (max) |
| $\mathrm{t}_{\mathrm{CAL}}$ | Full Calibration Time |  | 4946 | 4946 clks + 120 ns | clks (max) |
|  | CLK Duty Cycle |  | 50 | $\begin{aligned} & 40 \\ & 60 \end{aligned}$ |  |
| $\mathrm{t}_{\text {CONV }}$ | Conversion Time | Sync-Out Mode | 44 | 44 | clks (max) |
| $\mathrm{t}_{\text {AcqSYNCOUT }}$ | Acquisition Time (Programmable) | Minimum for 13 Bits Maximum for 13 Bits | $\begin{gathered} 9 \\ 79 \end{gathered}$ | $\begin{aligned} & 9 \text { clks }+120 \text { ns } \\ & 79 \text { clks }+120 \text { ns } \end{aligned}$ | clks (max) clks (max) |

Digital Timing Characteristics The following specifications apply to the ADC12048, 13-bit data bus width, $\mathrm{V}_{\mathrm{A}^{+}}=\mathrm{V}_{\mathrm{D}}{ }^{+}=5 \mathrm{~V}$, $\mathrm{f}_{\mathrm{CLK}}=12 \mathrm{MHz}, \mathrm{t}_{\mathrm{f}}=3 \mathrm{~ns}$ and $\mathrm{C}_{\mathrm{L}}=50 \mathrm{pF}$ on data $\mathrm{I} / \mathrm{O}$ lines

| Symbol (Figure 7) | Parameter | Conditions | Typical (Note 10) | Limits (Note 11) | Units (Limit) |
| :---: | :---: | :---: | :---: | :---: | :---: |
| $t_{\text {TPR }}$ | Throughput Rate | Sync-Out Mode (SYNC Bit = " 0 ") 9 Clock Cycles of Acquisition Time | 222 |  | kHz |
| $\mathrm{t}_{\text {CSWR }}$ | Falling Edge of $\overline{\mathrm{CS}}$ to Falling Edge of $\overline{\mathrm{WR}}$ |  | 0 |  | ns |
| twrics | Active Edge of $\overline{W R}$ to Rising Edge of $\overline{C S}$ |  | 0 |  | ns |
| twR | $\overline{\text { WR Pulse Width }}$ |  | 20 | 30 | ns (min) |
| twrSETFalling | Write Setup Time | WMODE $=$ "1" |  | 20 | ns (min) |
| ${ }^{\text {t }}$ WRHOLDFalling | Write Hold Time | WMODE $=$ " 1 " |  | 5 | ns (min) |
| twrsetrising | Write Setup Time | WMODE $=$ "0" |  | 20 | ns (min) |
| ${ }^{\text {twRHOLDRising }}$ | Write Hold Time | WMODE $=$ " 0 "' |  | 5 | ns (min) |
| tCSRD | Falling Edge of $\overline{C S}$ to Falling Edge of $\overline{\mathrm{RD}}$ |  | 0 |  | ns |
| $\mathrm{t}_{\text {RDCS }}$ | Rising Edge of $\overline{\mathrm{RD}}$ to Rising Edge of $\overline{\mathrm{CS}}$ |  | 0 |  | ns |
| $t_{\text {RDDATA }}$ | Falling Edge of $\overline{\mathrm{RD}}$ to Valid Data | 8 -Bit Mode (BW Bit = "0") | 40 | 58 | ns (max) |
| $t_{\text {RDDATA }}$ | Falling Edge of $\overline{\mathrm{RD}}$ to Valid Data | 13-Bit Mode (BW Bit = '1") | 26 | 44 | ns (max) |
| $\mathrm{t}_{\text {RDHOLD }}$ | Read Hold Time |  | 23 | 32 | ns (max) |
| $t_{\text {RDRDY }}$ | Rising Edge of $\overline{\mathrm{RD}}$ to Rising Edge of $\overline{\mathrm{RDY}}$ |  | 24 | 38 | ns (max) |
| twRRDY | Active Edge of $\overline{W R}$ to Rising Edge of $\overline{\text { RDY }}$ | WMODE $=$ " 1 " | 42 | 65 | ns (max) |
| ${ }^{\text {t }}$ STNDBY | Active Edge of $\overline{W R}$ to Falling Edge of STDBY | WMODE $=$ " 0 ". Writing the Standby Command into the Configuration Register | 200 | 230 | ns (max) |
| tstDONE | Active Edge of $\overline{W R}$ to Rising Edge of STDBY | WMODE $=$ " 0 ". Writing the RESET Command into the Configuration Register | 30 | 45 | ns (max) |
| tstDRDY | Active Edge of $\overline{W R}$ to Falling Edge of $\overline{\mathrm{RDY}}$ | WMODE $=$ " 0 ". Writing the RESET Command into the Configuration Register | 1.4 | 2.5 | ms (max) |
| $t_{\text {SYNC }}$ | Minimum SYNC Pulse Width |  | 5 | 10 | $\mathrm{ns}(\mathrm{min})$ |

## Notes on Specifications

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional, but do not guarantee specific performance limits. For guaranteed specifications and test conditions, see the Electrical Characteristics. The guaranteed specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions.
Note 2: All voltages are measured with respect to GND, unless otherwise specified.
Note 3: When the input voltage $\left(\mathrm{V}_{I N}\right)$ at any pin exceeds the power supply rails $\left(\mathrm{V}_{I N}<G N D\right.$ or $\mathrm{V}_{I N}>\left(\mathrm{V}_{\mathrm{A}}{ }^{+}\right.$or $\left.\mathrm{V}_{\mathrm{D}}{ }^{+}\right)$), the current at that pin should be limited to 30 mA . The 120 mA maximum package input current limits the number of pins that can safely exceed the power supplies with an input current of 30 mA to four.
Note 4: The maximum power dissipation must he derated at elevated temperatures and is dictated by $T_{J m a x}$, (maximum junction temperature), $\theta_{\mathrm{JA}}$ (package junction to ambient thermal resistance), and $\mathrm{T}_{\mathrm{A}}$ (ambient temperature). The maximum allowable power dissipation at any temperature is $\mathrm{P}_{\mathrm{Dmax}}=\left(\mathrm{T}_{\mathrm{Jmax}}-\mathrm{T}_{\mathrm{A}}\right) /$ $\theta_{J A}$ or the number given in the Absolute Maximum Ratings, whichever is lower. For this device, $T_{J m a x}=150^{\circ} \mathrm{C}$, and the typical thermal resistance ( $\theta_{\mathrm{JA}}$ ) of the ADC12048 in the V package, when board mounted, is $55^{\circ} \mathrm{C} / \mathrm{W}$, and in the VF package, when board mounted, is $67.8^{\circ} \mathrm{C} / \mathrm{W}$.
Note 5: Human body model, 100 pF discharged through $1.5 \mathrm{k} \Omega$ resistor.

Notes on Specifications (Continued)
Note 6: Each input and output is protected by a nominal 6.5 V breakdown voltage zener diode to GND; as shown below, input voltage magnitude up to 0.3 V above $\mathrm{V}_{\mathrm{A}}+$ or 0.3 V below GND will not damage the ADC12048. There are parasitic diodes that exist between the inputs and the power supply rails and errors in the $\mathrm{A} / \mathrm{D}$ conversion can occur if these diodes are forward biased by more than 50 mV . As an example, if $\mathrm{V}_{\mathrm{A}}{ }^{+}$is $4.50 \mathrm{~V}_{\mathrm{DC}}$, full-scale input voltage must be $\leq 4.55 \mathrm{~V}_{\mathrm{DC}}$ to ensure accurate conversions.


TL/H/12387-4
Note 7: $\mathrm{V}_{\mathrm{A}}{ }^{+}$and $\mathrm{V}_{\mathrm{D}}{ }^{+}$must be connected together to the same power supply voltage and bypassed with separate capacitors at each $\mathrm{V}^{+}$pin to assure conversion/comparison accuracy. Refer to the Power Supply Considerations section for a detailed discussion.
Note 8: Accuracy is guaranteed when operating at $\mathbf{f} \mathbf{C L K}=\mathbf{1 2} \mathbf{~ M H z}$.
Note 9: With the test condition for $\mathrm{V}_{\mathrm{REF}}\left(\mathrm{V}_{\mathrm{REF}}{ }^{+}-\mathrm{V}_{\mathrm{REF}}{ }^{-}\right)$given as +4.096 V , the 12-bit LSB is 1.000 mV .
Note 10: Typicals are at $\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$ and represent most likely parametric norm.
Note 11: Limits are guaranteed to National's AOQL (Average Outgoing Quality Level).
Note 12: Positive integral linearity error is defined as the deviation of the analog value, expressed in LSBs, from the straight line that passes through positive fullscale and zero. For negative integral linearity error, the straight line passes through negative full-scale and zero.
Note 13: Zero error is a measure of the deviation from the mid-scale voltage (a code of zero), expressed in LSB. It is the average value of the code transitions between -1 to 0 and 0 to +1 (see Figure 6).
Note 14: The DC common-mode error is measured with both inputs shorted together and driven from 0 V to 5 V . The measured value is referred to the resulting output value when the inputs are driven with a 2.5 V input.
Note 15: Power Supply Sensitivity is measured after an Auto-Zero and Auto Calibration cycle has been completed with $\mathrm{V}_{A^{+}}$and $\mathrm{V}_{\mathrm{D}}{ }^{+}$at the specified extremes.
Note 16: $\mathrm{V}_{\text {REFCM }}$ (Reference Voltage Common Mode Range) is defined as $\left(\frac{\mathrm{V}_{\text {REF }}{ }^{+}+\mathrm{V}_{\text {REF }^{-}}}{2}\right)$
Note 17: The ADC12048's self-calibration technique ensures linearity and offset errors as specified, but noise inherent in the self-calibration process will result in a repeatability uncertainly of $\pm 0.20$ LSB.
Note 18: Total Unadjusted Error (TUE) includes offset, full scale linearity and MUX errors.
Note 19: The ADC12048 parts used to gather the information for these curves were auto-calibrated prior to taking the measurements at each test condition. The auto-calibration cycle cancels any first order drifts due to test conditions. However, each measurement has a repeatability uncertainty error of 0.2 LSB. See Note 17.

Note 20: This is a DC average current drawn by the reference input with a full-scale sinewave input. The ADC12048 is continuously converting with a throughput rate of 206 kHz .
Note 21: These typical curves were measured during continuous conversions with a positive half-scale DC input. A $240 \mathrm{~ns} \overline{\mathrm{RD}}$ pulse was applied 25 ns after the $\overline{R D Y}$ signal went low. The data bus lines were loaded with 2 HC family CMOS inputs ( $\mathrm{C}_{\mathrm{L}} \sim 20 \mathrm{pF}$ ).
Note 22: Any other values placed in the command field are meaningless. However, if a code of 101 or 110 is placed in the command field and the $\overline{\mathrm{CS}}, \overline{\mathrm{RD}}$ and $\overline{\mathrm{WR}}$ go low at the same time, the ADC12048 will enter a test mode. These test modes are only to be used by the manufacturer of this device. A hardware power-off and power-on reset must be done to get out of these test modes.

## Electrical Characteristics



FIGURE 1. Output Digital Code vs the Operating Input Voltage Range (General Case)

$\mathrm{V}_{\mathrm{IN}+}(\mathrm{V})$
TL/H/12387-6
FIGURE 2. Output Digital Code vs the Operating Input Voltage Range for $\mathrm{V}_{\text {REF }}=4.096 \mathrm{~V}$


## Electrical Characteristics (Continued)



FIGURE 5b. Simplified Error vs Output Code without Auto-Calibration or Auto-Zero Cycles

## Electrical Characteristics (Continued)



FIGURE 6. Offset or Zero Error Voltage (Note 13)

## Timing Diagrams



Timing Diagrams (Continued)


TL/H/12387-46
FIGURE 7c. Sync-Out Write (WMODE $=0, B W=1$ ), Read and Convert Cycles


Timing Diagrams (Continued)


Timing Diagrams (Continued)


FIGURE 7h. 8-Bit Bus Read Cycle (Sync-In)

Timing Diagrams (Continued)


TL/H/12387-15
FIGURE 7i. Write Signal Negates $\overline{\text { RDY }}$ (Writing the Standby, Auto-Cal or Auto-Zero Command)


## Typical Performance Characteristics (See Note 19, Electrical Characteristic Section)




TL/H/12387-20


TL/H/12387-23




TL/H/12387-21


TL/H/12387-24






## Typical Performance Characteristics (Continued) (See Note 21, Electrical Characteristic Section)



Typical Performance Characteristics (Continued) The curves were obtained under the following conditions. $\mathrm{R}_{\mathrm{S}}=50 \Omega, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}, \mathrm{V}_{\mathrm{A}}+=\mathrm{V}_{\mathrm{D}}+=5 \mathrm{~V}, \mathrm{~V}_{\mathrm{REF}}=4.096 \mathrm{~V}$, $\mathrm{f}_{\mathrm{CLK}}=12 \mathrm{MHz}$, and the sampling rate $\mathrm{f}_{\mathrm{S}}=215 \mathrm{kHz}$ unless otherwise stated.


Full Scale Differential $\mathbf{3 8 , 4 5 2 ~ H z}$ Sine Wave Input


( Hz )
TL/H/12387-30

Half Scale Differential 40 kHz
Sine Wave Input, $\mathrm{f}_{\mathbf{S}}=153.6 \mathbf{k H z}$

( Hz )

Full Scale Differential 18,677 Hz Sine Wave Input


Full Scale Differential 79,468 Hz Sine Wave Input


Half Scale Differential 20 kHz Sine Wave Input, $\mathrm{f}_{\mathrm{S}}=153.6 \mathbf{k H z}$

( Hz )
TL/H/12387-31
Half Scale Differential 75 kHz Sine Wave Input, $\mathrm{f}_{\mathbf{S}}=153.6 \mathbf{~ k H z}$

( Hz )

Pin Description

| PLCC Pkg. Pin Number | PQFP Pkg. Pin Number | Pin Name | Description |
| :---: | :---: | :---: | :---: |
| $\begin{array}{r} 6 \\ 7 \\ 8 \\ 9 \\ 9 \\ 15 \\ 16 \\ 17 \\ 18 \\ \hline \end{array}$ | $\begin{array}{r} 44 \\ 1 \\ 2 \\ 3 \\ 9 \\ 10 \\ 11 \\ 12 \\ \hline \end{array}$ | $\begin{aligned} & \mathrm{CHO} \\ & \mathrm{CH} 1 \\ & \mathrm{CH} 2 \\ & \mathrm{CH} 3 \\ & \mathrm{CH} 4 \\ & \mathrm{CH} 5 \\ & \mathrm{CH} 6 \\ & \mathrm{CH} 7 \\ & \hline \end{aligned}$ | The eight analog inputs to the Multiplexer. Active channels are selected based on the contents of bits b3-b0 of the Configuration register. Refer to section titled MUX for more details. |
| 14 | 8 | COM | This pin is another analog input pin used as a pseudo ground when the multiplexer is configured in single-ended mode. |
| 13 | 7 | $\mathrm{V}_{\text {REF }}{ }^{+}$ | Positive reference input. The operating voltage range for this input is $1 \mathrm{~V} \leq \mathrm{V}_{\mathrm{REF}}{ }^{+} \leq \mathrm{V}_{\mathrm{A}}{ }^{+}$(see Figures 3 and 4). This pin should be bypassed to AGND at least with a parallel combination of a $10 \mu \mathrm{~F}$ and a $0.1 \mu \mathrm{~F}$ (ceramic) capacitors. The capacitors should be placed as close to the part as possible. |
| 12 | 6 | $\mathrm{V}_{\text {REF }}{ }^{-}$ | Negative reference input. The operating voltage range for this input is $0 \mathrm{~V} \leq \mathrm{V}_{\mathrm{REF}}{ }^{-} \leq \mathrm{V}_{\mathrm{REF}}{ }^{+}-1$ (see Figures 3 and 4 ). This pin should be bypassed to AGND at least with a parallel combination of a $10 \mu \mathrm{~F}$ and a $0.1 \mu \mathrm{~F}$ (ceramic) capacitor. The capacitors should be placed as close to the part as possible. |
| $\begin{aligned} & 19 \\ & 21 \end{aligned}$ | $\begin{aligned} & 13 \\ & 15 \end{aligned}$ | MUX OUT MUX OUT+ | The inverting (negative) and non-inverting (positive) outputs of the multiplexer. The analog inputs to the MUX selected by bits b3-b0 of the Configuration register appear at these pins. |
| $\begin{aligned} & 20 \\ & 22 \\ & \hline \end{aligned}$ | $\begin{array}{r} 14 \\ 16 \\ \hline \end{array}$ | $\begin{aligned} & \text { ADCIN- } \\ & \text { ADCIN+ } \end{aligned}$ | ADC inputs. The inverting (negative) and non-inverting (positive) inputs into the ADC. |
| 24 | 18 | WMODE | The logic state of this pin at power-up determines which edge of the write signal ( $\overline{\mathrm{WR})}$ will latch in data from the data bus. If tied low, the ADC12048 will latch in data on the rising edge of the WR signal. If tied to a logic high, data will he latched in on the falling edge of the $\overline{W R}$ signal. The state of this pin should not be changed after power-up. |
| 25 | 19 | SYNC | The SYNC pin can be programmed as an input or an output. The Configuration register's bit b8 controls the function of this pin. When programmed as an input pin ( $\mathrm{b} 8=1$ ), a rising edge on this pin causes the ADC's sample-and-hold to hold the analog input signal and begin conversion. When programmed as an output pin ( $\mathrm{b} 8=0$ ), the SYNC pin goes high when a conversion begins and returns low when completed. |
| $\begin{aligned} & 26-31 \\ & 34-40 \end{aligned}$ | $\begin{aligned} & 20-25 \\ & 29-34 \end{aligned}$ | $\begin{aligned} & \hline \text { D0-D5 } \\ & \text { D6-D12 } \end{aligned}$ | 13-bit Data bus of the ADC12048. D12 is the most significant bit and D0 is the least significant. The BW (bus width) bit of the Configuration register (b12) selects between an 8 -bit or 13 -bit data bus width. When the $B W$ bit is cleared ( $B W=0$ ), D7-D0 are active and D12-D8 are always in TRI-STATE. When the BW bit is set ( $B W=1$ ), D12-D0 are active. |
| 43 | 37 | CLK | The clock input pin used to drive the ADC12048. The operating range is 0.05 MHz to 12 MHz . |
| 44 | 38 | $\overline{W R}$ | $\overline{W R}$ is the active low WRITE control input pin. A logic low on this pin and the $\overline{\mathrm{CS}}$ will enable the input buffers of the data pins D12-D0. The signal at this pin is used by the ADC12048 to latch in data on D12-D0. The sense of the WMODE pin at power-up will determine which edge of the $\overline{\mathrm{WR}}$ signal the ADC12048 will latch in data. See WMODE pin description. |
| 1 | 39 | $\overline{\mathrm{RD}}$ | $\overline{\mathrm{RD}}$ is the active low read control input pin. A logic low on this pin and $\overline{\mathrm{CS}}$ will enable the active output buffers to drive the data bus. |
| 2 | 40 | $\overline{\mathrm{CS}}$ | $\overline{\mathrm{CS}}$ is the active low Chip Select input pin. Used in conjunction with the $\overline{\mathrm{WR}}$ and $\overline{\mathrm{RD}}$ signals to control the active data bus input/output buffers of the data bus. |
| 3 | 41 | $\overline{\text { RDY }}$ | $\overline{R D Y}$ is an active low output pin. The signal at this pin indicates when a requested function has begun or ended. Refer to section Functional Description and the digital timing diagrams for more detail. |
| 4 | 42 | STDBY | This is the standby active low output pin. This pin is low when the ADC12048 is in the standby mode and high when the ADC12048 is out of the standby mode or has been requested to leave the standby mode. |
| 10 | 4 | $\mathrm{V}_{\mathrm{A}}{ }^{+}$ | Analog supply input pin. The device operating supply voltage range is $+5 \mathrm{~V} \pm 10 \%$. Accuracy is guaranteed only if the $\mathrm{V}_{\mathrm{A}^{+}}$and $\mathrm{V}_{\mathrm{D}}{ }^{+}$are connected to the same potential. This pin should be bypassed to AGND with a parallel combination of a $10 \mu \mathrm{~F}$ and a $0.1 \mu \mathrm{~F}$ (ceramic) capacitor. The capacitors should be placed as close to the supply pins of the part as possible. |
| 11 | 5 | AGND | Analog ground pin. This is the device's analog supply ground connection. It should be connected through a low resistance and low inductance ground return to the system power supply. |
| 32 and 41 | 26 and 35 | $\mathrm{V}_{\mathrm{D}}{ }^{+}$ | Digital supply input pins. The device operating supply voltage range is $+5 \mathrm{~V} \pm 10 \%$. Accuracy is guaranteed only if the $\mathrm{V}_{\mathrm{A}}{ }^{+}$and $\mathrm{V}_{\mathrm{D}}{ }^{+}$are connected to the same potential. This pin should be bypassed to DGND with a parallel combination of a $10 \mu \mathrm{~F}$ and a $0.1 \mu \mathrm{~F}$ (ceramic) capacitor. The capacitors should be placed as close to the supply pins of the part as possible. |
| 33 and 42 | 27 and 36 | DGND | Digital ground pin. This is the device's digital supply ground connection. It should be connected through a low resistance and low inductance ground return to the system power supply. |



## Register Bit Description

## CONFIGURATION REGISTER (Write Only)

This is a 13-bit write-only register that is used to program the functionality of the ADC12048. All data written to the ADC12048 will always go to this register only The contents of this register cannot be read.

| MSB |  |  |  |  |  |  |  |  |  |  |  | SB |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| $\mathrm{b}_{12}$ | $\mathrm{b}_{11}$ | $\mathrm{b}_{10}$ | $\mathrm{b}_{9}$ | $\mathrm{b}_{8}$ | $\mathrm{b}_{7}$ | $\mathrm{b}_{6}$ | $\mathrm{b}_{5}$ | $\mathrm{b}_{4}$ | $\mathrm{b}_{3}$ | $\mathrm{b}_{2}$ | $\mathrm{b}_{1}$ | $\mathrm{b}_{0}$ |
| BW | COMMAND FIELD |  |  | SYNC | HB | SE | ACQ TIME |  | MUX ADDRESS |  |  |  |

Power on State: 0100 Hex
$\mathbf{b}_{\mathbf{3}}-\mathbf{b}_{\mathbf{0}}$ : The MUX ADDRESS bits configure the analog input MUX. They select which input channels of the MUX will connect to the MUXOUT+ and MUXOUTpins. (Refer to the MUX section for more details on the MUX.) Power-up value is 0000.

TABLE I. MUX Channel Assignment

| $\mathrm{b}_{3}$ | $\mathrm{b}_{2}$ | $\mathrm{b}_{1}$ | $\mathrm{b}_{0}$ | MUXOUT+ | MUXOUT - |
| :---: | :---: | :---: | :---: | :---: | :---: |
| 0 | 0 | 0 | 0 | CH0 | CH1 |
| 0 | 0 | 0 | 1 | CH1 | CHO |
| 0 | 0 | 1 | 0 | CH2 | CH3 |
| 0 | 0 | 1 | 1 | CH3 | CH2 |
| 0 | 1 | 0 | 0 | CH4 | CH5 |
| 0 | 1 | 0 | 1 | CH5 | CH4 |
| 0 | 1 | 1 | 0 | CH6 | CH7 |
| 0 | 1 | 1 | 1 | CH7 | CH6 |
| 1 | 0 | 0 | 0 | CHO | COM |
| 1 | 0 | 0 | 1 | CH1 | COM |
| 1 | 0 | 1 | 0 | CH2 | COM |
| 1 | 0 | 1 | 1 | CH3 | COM |
| 1 | 1 | 0 | 0 | CH4 | COM |
| 1 | 1 | 0 | 1 | CH5 | COM |
| 1 | 1 | 1 | 0 | CH6 | COM |
| 1 | 1 | 1 | 1 | CH7 | COM |

$\mathbf{b}_{\mathbf{5}} \mathbf{-} \mathbf{b}_{\mathbf{4}}$ : The ACQ TIME bits select one of four possible acquistion times in SYNC-OUT mode. (Refer to Selectable Acquisition Time section.)

| $\mathbf{b}_{\mathbf{5}}$ | $\mathbf{b}_{\mathbf{4}}$ | Clocks |
| :---: | :---: | :---: |
| 0 | 0 | 9 |
| 0 | 1 | 15 |
| 1 | 0 | 47 |
| 1 | 1 | 79 |

$\mathbf{b}_{6}$ : When the Single-Ended bit (SE bit) is set, conversion results will be limited to positive values only and any negative conversion results will appear as a code of zero in the Data register. The SE bit is cleared at power-up.
$\mathbf{b}_{7}$ : The High Byte bit (HB) is meaningful only in 8 -bit mode (BW bit $\mathrm{b}_{12}=$ " 0 ") and is a don't care condition in 13-bit mode (BW bit $\mathrm{b}_{12}=$ " 1 "). This bit is used to access the upper byte of the Configuration Register in 8 -bit mode. When this bit is set and bit $\mathrm{b}_{12}=0$, the next byte written to the ADC12048 will program the upper byte of the Configuration register. The HB bit will automatically be cleared when data is written to the upper byte of the Configuration register, allowing the lower byte to be accessed with the next write. The HB bit is cleared at power-up.
$\mathbf{b}_{8}$ : The SYNC bit. When the SYNC bit is set, the SYNC pin is programmed as an input and the converter is in synchronous mode. In this mode a rising edge on the SYNC pin causes the ADC to hold the input signal and begin a conversion. When $b_{15}$ cleared, the SYNC pin is programmed as an output and the converter is in an asynchronous mode. In this mode the signal at the SYNC pin indicates the status of the converter. The SYNC pin is high when a conversion is taking place. The SYNC bit is set at power-up.
$\mathbf{b}_{11}-\mathbf{b}_{\mathbf{g}}$ : The command field. These bits select the mode of operation of the ADC12048. Power-up value is 000. (See Note 22)

| $\mathbf{b}_{\mathbf{1 1}}$ | $\mathbf{b}_{\mathbf{1 0}}$ | $\mathbf{b}_{\mathbf{9}}$ | Command |
| :---: | :---: | :---: | :--- |
| 0 | 0 | 0 | Standby command. This puts the ADC in a low power consumption mode |
| 0 | 0 | 1 | Ful-Cal command. This will cause the ADC to perform a self-calibrating cycle that will correct linearity and zero errors. |
| 0 | 1 | 0 | Auto-zero command. This will cause the ADC to perform an auto-zero cycle that corrects offset errors. |
| 0 | 1 | 1 | Reset command. This puts the ADC in an idle mode. |
| 1 | 0 | 0 | Start command. This will put the converter in a start mode, preparing it to perform a conversion. If in asynchronous mode ( $\mathrm{b}_{8}=$ " 0 ""), conversions <br> will immediately begin after the programmed acquisition time has ended. In synchronous mode ( $\mathrm{b}_{8}=$ <br> edge appears on the SYNC pin. |

$\mathbf{b}_{12}$ : This is the Bus Width (BW) bit. When this bit is cleared the ADC12048 is configured to interface with an 8 -bit data bus; data pins $D_{7}-D_{0}$ are active and pins $D_{12}-D_{9}$ are in TRI-STATE. When the BW bit is set, the ADC12048 is configured to interface with a 16 -bit data bus and data pins $D_{13}-D_{0}$ are all active. The BW bit is cleared at power-up.

## DATA REGISTER (Read Only)

This is a 13 -bit read only register that holds the 12-bit + sign conversion result in two's compliment form. All reads performed from the ADC12048 will place the contents of this register on the data bus. When reading the data register in 8 -bit mode, the sign bit is extended.

| MSB |  |  |  |  |  |  |  |  |  |  |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| $\mathrm{b}_{12}$ | $\mathrm{b}_{11}$ | $\mathrm{b}_{10}$ | $\mathrm{b}_{9}$ | $\mathrm{b}_{8}$ | $\mathrm{b}_{7}$ | $\mathrm{b}_{6}$ | $\mathrm{b}_{5}$ | $\mathrm{b}_{4}$ | $\mathrm{b}_{3}$ | $\mathrm{b}_{2}$ | $\mathrm{b}_{1}$ | $\mathrm{b}_{0}$ |
| sign | Conversion Data |  |  |  |  |  |  |  |  |  |  |  |

Power on State: 0000 Hex
$\mathbf{b}_{11}-\mathbf{b}_{\mathbf{0}}$ : $\mathrm{b}_{11}$ is the most significant bit and $\mathrm{b}_{0}$ is the least significant bit of the conversion result. $\mathbf{b}_{\mathbf{1 2}}$ : This bit contains the sign of the conversion result. 0 for positive results and 1 for negative.

## Functional Description

The ADC12048 is programmed through a digital interface that supports an 8 -bit or 16 -bit data bus. The digital interface consists of a 13-bit data input/output bus ( $D_{12}-D_{0}$ ), digital control signals and two internal registers: a write only 13-bit Configuration register and a read only 13-bit Data register.
The Configuration register programs the functionality of the ADC12048. The 13 bits of the Configuration register are divided into 7 fields. Each field controls a specific function of the ADC12048: the channel selection of the MUX, the acquisition time, synchronous or asynchronous conversions, mode of operation and the data bus size.

## Features and Operating Modes

## SELECTABLE BUS WIDTH

The ADC12048 can be programmed to interface with an 8 -bit or 16 -bit data bus. The BW bit $\left(\mathrm{b}_{12}\right)$ in the Configuration register controls the bus size. The bus width is set to 8 bits ( $D_{7}-D_{0}$ are active and $D_{12}-D_{8}$ are in TRI-STATE) if the BW bit is cleared or 13 bits ( $D_{12}-D_{0}$ are active) if the BW bit is set. At power-up the bus width defaults to 8 bits and any initial programming of the ADC12048 should take this into consideration.
In 8-bit mode the Configuration register is byte accessible. The HB bit in the lower byte of the Configuration register is used to access the upper byte. If the HB bit is set with a write to the lower byte, the next byte written to the ADC will be placed in the upper byte of the Configuration register. After data is written to the upper byte of the Configuration register, the HB bit will automatically be cleared, causing the next byte written to the ADC to go to the lower byte of the Configuration register. When reading the ADC in 8 -bit mode, the first read cycle places the lower byte of the Data register on the data bus followed by the upper byte during the next read cycle.
In 13-bit mode the HB bit is a don't care condition and all bits of the data register and Configuration register are accessible with a single read or write cycle. Since the bus width of the ADC12048 defaults to 8 bits after power-up, the first action when 13-bit mode is desired must be set to the bus width to 13 bits.

## WMODE

The WMODE pin is used to determine the active edge of the write pulse. The state of this pin determines which edge of the $\overline{\mathrm{WR}}$ signal will cause the ADC to latch in data. This is processor dependent. If the processor has valid data on the bus during the falling edge of the $\overline{\mathrm{WR}}$ signal, the WMODE pin must be tied to $V_{D}{ }^{+}$. This will cause the ADC to latch the data on the falling edge of the $\overline{W R}$ signal. If data is valid on the rising edge of the $\overline{\mathrm{WR}}$ signal, the WMODE pin must be tied to DGND causing the ADC to latch in the data on the rising edge of the $\overline{W R}$ signal.

## INPUT MULTIPLEXER

The ADC12048 has an eight channel input multiplexer with a COM input that can be used in a single-ended, pseudo-differential or fully-differential mode. The MUX select bits ( $b_{3}-$ $b_{0}$ ) in the Configuration register determine which channels will appear at the MUXOUT + and MUXOUT - multiplexer output pins. (Refer to Register Bit Description Section.) Analog signal conditioning with fixed-gain amplifiers, program-mable-gain amplifiers, filters and other processing circuits
can be used at the output of the multiplexer before being applied to the ADC inputs. The ADCIN+ and ADCIN - are the fully differential non-inverting (positive) and inverting (negative) inputs to the analog-to-digital converter (ADC) of the ADC12048. If no external signal conditioning is required on the signal output of the multiplexer, MUXOUT + should be connected to ADCIN + and MUXOUT - should be connected to ADCIN-.
The analog input multiplexer can be set up to operate in either one of eight differential or eight single-ended (the COM input as the zero reference) modes. In the differential mode, the analog inputs are paired as follows: CHO with $\mathrm{CH} 1, \mathrm{CH} 2$ with $\mathrm{CH} 3, \mathrm{CH} 4$ with CH 5 and CH 6 with CH 7 . The input channel pairs can be connected to the MUXOUT+ and MUXOUT- pins in any order. In the single-ended mode, one of the input channels, CH 0 through CH 7 , can be assigned to MUXOUT+ while the MUXOUT - is always assigned to the COM input.

## STANDBY MODE

The ADC12048 has a low power consumption mode ( $75 \mu \mathrm{~W}$ $@ 5 \mathrm{~V}$ ). This mode is entered when a Standby command is written in the command field of the Configuration register. A logic low appearing on the STDBY output pin indicates that the ADC12048 is in the Standby mode. Any command other than the Standby command written to the Configuration register will get the ADC12048 out of the Standby mode. The STDBY pin will immediately switch to a logic " 1 " as soon as the ADC12048 is requested to get out of the standby mode. The $\overline{R D Y}$ pin will then be asserted low when the ADC is actually out of the Standby mode and ready for normal operation. The ADC12048 defaults to the Standby mode following a hardware power-up. This can be verified by examining the logic low status of the STDBY pin.

## SYNC/ASYNC MODE

The ADC12048 may be programmed to operate in synchronous (SYNC-IN) or asynchronous (SYNC-OUT) mode. To enter synchronous mode, the SYNC bit in the Configuration register must be set. The ADC12048 is in synchronous mode after a hardware power-up. In this mode, the SYNC pin is programmed as an input and conversions are synchronized to the rising edges of the signal applied at the SYNC pin. Acquisition time can also be controlled by the SYNC signal when in synchronous mode. Refer to the syncin timing diagrams. When the SYNC bit is cleared, the ADC is in asynchronous mode and the SYNC pin is programmed as an output. In asynchronous mode, the signal at the SYNC pin indicates the status of the converter. This pin is high when the converter is performing a conversion. Refer to the sync-out timing diagrams.

## SELECTABLE ACQUISITION TIME

The ADC12048's internal sample/hold circuitry samples an input voltage by connecting the input to an internal sampling capacitor (approximately 70 pF ) through an effective resistance equal to the multiplexer "On" resistance ( $300 \Omega$ max) plus the "On" resistance of the analog switch at the input to the sample/hold circuit ( $2500 \Omega$ typical) and the effective output resistance of the source. For conversion results to be accurate, the period during which the sampling capacitor is connected to the source (the "acquisition time") must be long enough to charge the capacitor to within a small fraction of an LSB of the input voltage. An acquisition time of 750 ns is sufficient when the external source resistance is

## Features and Operating Modes (Continued)

less than $1 \mathrm{k} \Omega$ and any active or reactive source circuitry settles to 12 bits in less than 500 ns. When source resistance or source settling time increase beyond these limits, the acquisition time must also be increased to preserve precision.
In asynchronous (SYNC-OUT) mode, the acquisition time is controlled by an internal counter. The minimum acquisition period is 9 clock cycles, which corresponds to the nominal value of 750 ns when the clock frequency is 12 MHz . Bits $\mathrm{b}_{4}$ and $b_{5}$ of the Configuration Register are used to select the acquisition time from among four possible values (9, 15, 47, or 79 clock cycles). Since acquisition time in the asynchronous mode is based on counting clock cycles, it is also inversely proportional to clock frequency:

$$
\mathrm{T}_{\mathrm{ACQ}}(\mu \mathrm{~s})=\frac{\text { number of clock cycles }}{\mathrm{f}_{\mathrm{CLK}}(\mathrm{MHz})}
$$

Note that the actual acquisition time will be longer than $\mathrm{T}_{\mathrm{ACQ}}$ because acquisition begins either when the multiplexer channel is changed or when $\overline{\text { RDY }}$ goes low, if the multiplexer channel is not changed. After a read is performed, $\overline{R D Y}$ goes high, which starts the $\mathrm{T}_{\mathrm{ACQ}}$ counter (see Figure 7).

In synchronous (SYNC-IN) mode, bits $b_{4}$ and $b_{5}$ are ignored, and the acquisition time depends on the sync signal applied at the SYNC pin. If a new MUX channel is selected at the start of the conversion, the acquisition period begins on the active edge of the $\overline{W R}$ signal that latches in the new MUX channel (see Figure 7). If no new MUX channel is selected, the acquisition period begins on the falling edge of RDY, which occurs at the end of the previous conversion (or at the end of an autozero or autocalibration procedure). The acquisition period ends when SYNC goes high.
To estimate the acquisition time necessary for accurate conversions when the source resistance is greater than $1 \mathrm{k} \Omega$, use the following expression:

$$
\begin{aligned}
T_{\text {ACQMIN }}(\mu \mathrm{s}) & =\frac{0.75\left(R_{S}+R_{M}+R_{S / H}\right)}{1 \mathrm{k} \Omega+R_{M}+R_{S / H}} \\
& =\frac{0.75\left(R_{S}+2800\right)}{3800}
\end{aligned}
$$

where $R_{S}$ is the source resistance, $R_{M}$ is the MUX "On" resistance, and $\mathrm{R}_{\mathrm{S} / \mathrm{H}}$ is the sample/hold "On" resistance.
If the settling time of the source is greater than 500 ns , the acquisition time should be about 300 ns longer than the settling time for a "well-behaved", smooth settling characteristic.

## FULL CALIBRATION CYCLE

A full calibration cycle compensates for the ADC's linearity and offset errors. The converter's DC specifications are guaranteed only after a full calibration has been performed. A full calibration cycle is initated by writing a Ful-Cal command to the ADC12048. During a full calibration, the offset error is measured eight times, averaged and a correction coefficient is created. The offset correction coefficient is stored in an internal offset correction register.
The overall linearity correction is achieved by correctng the internal DAC's capacitor mismatches. Each capacitor is compared eight times against all remaining smaller value capacitors. The errors are averaged and correction coefficients are created.

Once the converter has been calibrated, an arithmetic logic unit (ALU) uses the offset and linearity correction coefficients to reduce the conversion offset and linearity errors to within guaranteed limits.

## AUTO-ZERO CYCLE

During an auto-zero cycle, the offset is measured only once and a correction coefficient is created and stored in an internal offset register. An auto-zero cycle is initiated by writing an Auto-Zero command to the ADC12048.

## DIGITAL INTERFACE

The digital control signals are $\overline{\mathrm{CS}}, \overline{\mathrm{RD}}, \overline{\mathrm{WR}}, \overline{\mathrm{RD}} \mathrm{Y}$ and STDBY. Specific timing relationships are associated with the interaction of these signals. Refer to the Digital Timing Diagrams section for detailed timing specifications. The active low RDY signal indicates when a certain event begins and ends. It is recommended that the ADC12048 should only be accessed when the RDY signal is low. It is in this state that the ADC12048 is ready to accept a new command. This will minimize the effect of noise generated by a switching data bus on the ADC. The only exception to this is when the ADC12048 is in the standby mode at which time the $\overline{R D Y}$ is high and the STDBY signal is low. The ADC12048 is in the standby mode at power up or when a STANDBY command is issued. A Ful-Cal, Auto-Zero, Reset or Start command will get the ADC12048 out of the standby mode. This may be observed by monitoring the status of the $\overline{R D Y}$ and STDBY signals. The RDY signal will go low and the STDBY signal high when the ADC12048 leaves the standby mode.

The following describes the state of the digital control signals for each programmed event in both 8 -bit and 13 -bit mode. $\overline{\text { RDY }}$ should be low before each command is issued except for the case when the device is in standby mode.

## FUL-CAL OR AUTO-ZERO COMMAND

8-bit mode: The first write to the ADC12048 will place the data in the lower byte of the Configuration register. This byte must set the HB bit ( $\mathrm{b}_{7}$ ) to allow access to the upper byte of the Configuration register during the next write cycle. During the second write cycle, the Ful-Cal or Auto-Zero command must be issued. The edge of the second write pulse on the WR pin will force the RDY signal high. At this time the converter begins executing a full calibration or auto-zero cycle.
 bration or auto-zero cycle is done.
13-bit mode: In a single write cycle the Ful-Cal or Auto-Zero command must be written to the ADC12048. The edge of the $\overline{\mathrm{WR}}$ signal will force the $\overline{\mathrm{RDY}}$ high. At this time the converter begins executing a full calibration or auto-zero cycle. The RDY signal will automatically go low when the full calibration or auto-zero cycle is done.

## STARTING A CONVERSION: START COMMAND

In order to completely describe the events associated with the Start command, both the SYNC-OUT and SYNC-IN modes must be considered.

## SYNC-OUT/Asynchronous

8-bit mode: The first byte written to the ADC12048 should set the MUX channel, the acquisition time and the HB bit. The second byte should clear the SYNC bit, write the START command and clear the BW bit. In order to initiate a

## Features and Operating Modes (Continued)

conversion, two reads must be performed from the ADC12048. The rising edge of the second read pulse will force the RDY pin high and begin the programmed acquisition time selected by bits $b_{5}$ and $b_{4}$ of the configuration register. The SYNC pin will go high indicating that a conversion sequence has begun following the end of the acquisition period. The RDY and SYNC signal will fall low when the conversion is done. At this time new information, such as a new MUX channel, acquisition time and operational command can be written into the configuration register or it can remain unchanged. Assuming that the START command is in the Configuration register, the previous conversion can be read. The first read places the lower byte of the conversion result contained in the Data register on the data bus. The second read will place the upper byte of the conversion result stored in the Data register on the data bus. The rising edge on the second read pulse will begin another conversion sequence and raise the $\overline{\mathrm{RDY}}$ and SYNC signals appropriately
13-bit mode: The MUX channel and the acquisition time should be set, the SYNC bit cleared and the START command issued with a single write to the ADC12048. In order to initiate a conversion, a single read must be performed from the ADC12048. The rising edge of the read signal will force the RDY signal high and begin the programmed acquisition time selected by bits $b_{5}$ and $b_{4}$ of the configuration register. The SYNC pin will go high indicating that a conversion sequence has begun following the end of the acquisition period. The $\overline{\mathrm{RDY}}$ and SYNC signal will fall low when the conversion is done. At this time new information, such as a new MUX channel, acquisition time and operational command can be written into the configuration register or it can remain unchanged. With the START command in the Configuration register, a read from the ADC12048 will place the entire 13-bit conversion result stored in the data register on the data bus. The rising edge of the read pulse will immediately force the $\overline{\text { RDY }}$ output high. The SYNC will then go high following the elapse of the programmed acquisition time in the configuration register's bits $b_{5}$ and $b_{4}$.

## SYNC-IN/Synchronous

For the SYNC-IN case, it is assumed that a series of SYNC pulses at the desired sampling rate are applied at the SYNC pin of the ADC12048.

8 -bit mode: The first byte written to the ADC12048 should set the MUX channel and the HB bit. The second byte should set the SYNC bit, write the START command and clear the BW bit.
A rising edge on the SYNC pin or the second rising edge of two consecutive reads from the ADC12048 will force the $\overline{\mathrm{RDY}}$ signal high. It is recommended that the action of reading from the ADC12048 (not the rising edge of the SYNC signal) be used to raise the RDY signal. In the SYNC-IN mode, only the rising edge of the SYNC signal will begin a conversion cycle. The rising edge of the SYNC also ends the acquisition period. The acquisition period begins following a write cycle containing MUX channel information. The selected MUX channel is sampled after the rising edge of the WR signal until the rising edge of the SYNC pulse, at which time the signal will be held and conversion begins.

The $\overline{\mathrm{RDY}}$ signal will go low when the conversion is done. A new MUX channel and/or operational command may be written into the Configuration register at this time, if needed. Two consecutive read cycles are required to retrieve the entire 13-bit conversion result from the ADC12048's data register. The first read will place the lower byte of the conversion result contained in the Data register on the data bus. The second read will place the upper byte of the conversion result stored in the Data register on the data bus. With the START command in the configuration register, the rising edge of the second read pulse will raise the $\overline{\text { RDY }}$ signal high and begin a conversion cycle following a rising edge on the SYNC pin.
13-bit mode: The MUX channel should be selected, the SYNC bit should be set and the START command issued with a single write to the ADC12048. A rising edge on the SYNC pin or on the $\overline{\mathrm{RD}}$ pin will force the $\overline{\mathrm{RDY}}$ signal high. It is recommended that the action of reading from the ADC12048 (not the rising edge of the SYNC signal) be used to raise the $\overline{\mathrm{RDY}}$ signal. This will ensure that the conversion result is read during the acquisition period of the next conversion cycle, eliminating a read from the ADC12048 while it is performing a conversion. Noise generated by accessing the ADC12048 while it is converting may degrade the conversion result. In the SYNC-IN mode, only the rising edge of the SYNC signal will begin a conversion cycle. The $\overline{\text { RDY }}$ signal will go low when the conversion cycle is done. The acquisition time is controlled by the SYNC signal. The acquisition period begins following a write cycle containing MUX channel information. The selected MUX channel is sampled after the rising edge of the $\overline{\mathrm{WR}}$ signal until the rising edge of the SYNC pulse, at which time the signal will be held and conversion begins. A new MUX channel and/or operational command may be written into the Configuration register at this time, if needed. With the START command in the Configuration register, a read from the ADC12048 will place the entire conversion result stored in the Data register on the data bus and the rising edge of the read pulse will force the RDY signal high. The selected MUX channel will be sampled until a rising edge appears on the SYNC pin, at which the time sampled signal will be held and a conversion cycle started.

## STANDBY COMMAND

8-bit mode: The first byte written to the ADC12048 should set the HB bit in the Configuration register (bit $\mathrm{b}_{7}$ ). The second byte must issue the Standby command (bits $\mathrm{b}_{11}, \mathrm{~b}_{10}, \mathrm{~b}_{9}$ $=0,0,0)$.
13-bit mode: The Standby command must be issued to the ADC12048 in single write (bits $b_{11}, b_{10}, b_{9}=0,0,0$ ).

## RESET

The RESET command places the ADC12048 into a ready state and forces the RDY signal low. The RESET command can be used to interrupt the ADC12048 while it is performing a conversion, full-calibration or auto-zero cycle. It can also be used to get the ADC12048 out of the standby mode.

## Analog Application Information

## REFERENCE VOLTAGE

The ADC12048 has two reference inputs, $\mathrm{V}_{\text {REF }}{ }^{+}$and $\mathrm{V}_{\mathrm{REF}}{ }^{-}$. They define the zero to full-scale range of the analog input signals over which 4095 positive and 4096 negative codes exist. The reference inputs can be connected to span the entire supply voltage range ( $\mathrm{V}_{\mathrm{REF}}{ }^{-}=\mathrm{AGND}$, $\mathrm{V}_{\text {REF }}{ }^{+}=\mathrm{V}_{\mathrm{A}}{ }^{+}$) or they can be connected to different voltages when other input spans are required. The reference inputs of the ADC12048 have transient capacitive switching currents. The voltage sources driving $\mathrm{V}_{\text {REF }}{ }^{+}$and $\mathrm{V}_{\text {REF }}{ }^{-}$ must have very low output impedence and noise and must be adequately bypassed. The circuit in Figure 8 is an example of a very stable reference source.
The ADC12048 can be used in either ratiometric or absolute reference appplications. In ratiometric systems, the analog

input voltage is proportional to the voltage used for the ADC's reference voltage. This technique relaxes the system reference requirements because the analog input voltage moves with the ADC's reference. The system power supply can be used as the reference voltage by connecting the $\mathrm{V}_{\text {REF }}{ }^{+}$pin to $\mathrm{V}_{\mathrm{A}}{ }^{+}$and the $\mathrm{V}_{\text {REF }}{ }^{-}$pin to AGND. For absolute accuracy, where the analog input voltage varies between very specific voltage limits, a time and temperature stable voltage source can be connected to the reference inputs. Typically, the reference voltage's magnitude will require an initial adjustment to null reference voltage induced full-scale errors.
The reference voltage inputs are not fully differential. The ADC12048 will not generate correct conversions if $\mathrm{V}_{\text {REF }}{ }^{+}$ $\mathrm{V}_{\text {REF }}{ }^{-}$is below 1 V . Figure 9 shows the allowable relationship between $\mathrm{V}_{\text {REF }}{ }^{+}$and $\mathrm{V}_{\text {REF }}{ }^{-}$.

## OUTPUT DIGITAL CODE VERSUS ANALOG INPUT VOLTAGE

The ADC12048's fully differential 12-bit + sign ADC generates a two's complement output that is found by using the equation shown below:

$$
\text { Output code } \left.=\frac{\left(\mathrm{V}_{\mathrm{IN}^{+}}-\mathrm{V}_{\mathrm{IN}^{-}}\right)(4096)}{\left(\mathrm{V}_{\text {REF }}\right.}-\mathrm{V}_{\mathrm{REF}^{-}}\right)
$$

Round off the result to the nearest integer value between -4096 and 4095.

FIGURE 9. VREF Operating Range


FIGURE 8. Low Drift Extremely Stable Reference Circuit

| Part Number | Output Voltage <br> Tolerance | Temperature <br> Coefficient |
| :---: | :---: | :---: |
| LM4041CI-Adj | $\pm 0.5 \%$ | $\pm 100 \mathrm{ppm} /{ }^{\circ} \mathrm{C}$ |
| LM4040AI-4.1 | $\pm 0.1 \%$ | $\pm 100 \mathrm{ppm} /{ }^{\circ} \mathrm{C}$ |
| LM9140BYZ-4.1 | $\pm 0.5 \%$ | $\pm 25 \mathrm{ppm} /{ }^{\circ} \mathrm{C}$ |
| LM368Y-5.0 | $\pm 0.1 \%$ | $\pm 20 \mathrm{ppm} /{ }^{\circ} \mathrm{C}$ |
| Circuit of Figure 8 | Adjustable | $\pm 2 \mathrm{ppm} /{ }^{\circ} \mathrm{C}$ |

## Analog Application Information (Continued)

 input CurrentAt the start of the acquisition window ( $\mathrm{t}_{\text {AcqSYNOUT }}$ ) a charging current (due to capacitive switching) flows through the analog input pins ( $\mathrm{CH} 0-\mathrm{CH} 7, \mathrm{ADCIN}+$ and $\operatorname{ADCIN}-$, and the COM). The peak value of this input current will depend on the amplitude and frequency of the input voltage applied, the source impedance and the input switch ON resistance. With the MUXOUT + connected to the ADCIN+ and the MUXOUT - connected to the ADCIN - the on resistance is typically $2800 \Omega$. Bypassing the MUX and using just the ADCIN + and ADCIN - inputs the on resistance is typically $2500 \Omega$.
For low impedance voltage sources ( $1000<\Omega$ for 12 MHz operation), the input charging current will decay to a value that will not introduce any conversion errors before the end of the default sample-and-hold (S/H) acquisition time (9 clock cycles). For higher source impedances ( $1000>\Omega$ for 12 MHz operation), the S/H acquisition time should be increased to allow the charging current to settle within specified limits. In asynchronous mode, the acquisition time may be increased to 15,47 or 79 clock cycles. If different acquisition times are needed, the synchronous mode can be used to fully control the acquisition time.

## INPUT BYPASS CAPACITANCE

External capacitors ( $0.01 \mu \mathrm{~F}-0.1 \mu \mathrm{~F})$ can be connected between the analog input pins ( $\mathrm{CH} 0-\mathrm{CH} 7$ ) and the analog ground to filter any noise caused by inconductive pickup associated with long leads.

## POWER SUPPLY CONSIDERATIONS

Decoupling and bypassing the power supply on a high resolution ADC is an important design task. Noise spikes on the $\mathrm{V}_{\mathrm{A}}{ }^{+}$(analog supply) or $\mathrm{V}_{\mathrm{D}}{ }^{+}$(digital supply) can cause conversion errors. The analog comparator used in the ADC will respond to power supply noise and will make erroneous conversion decisions. The ADC is especially sensitive to power supply spikes that occur during the auto-zero or linearity calibration cycles.
The ADC12048 is designed to operate from a single +5 V power supply. The separate supply and ground pins for the analog and digital portions of the circuit allow separate external bypassing. To minimize power supply noise and ripple, adequate bypass capacitors should be placed directly between power supply pins and their associated grounds. Both supply pins should be connected to the same supply source. In systems with separate analog and digital supplies, the ADC should be powered from the analog supply. At least a $10 \mu \mathrm{~F}$ tantalum electrolytic capacitor in parallel with a $0.1 \mu \mathrm{~F}$ monolithic ceramic capacitor is recommended for bypassing each power supply. The key consideration for these capacitors is to have low series resistance and inductance. The capacitors should be placed as close as physically possible to the supply and ground pins with the smaller capacitor closer to the device. The capacitors also should have the shortest possible leads in order to minimize series lead inductance. Surface mount chip capacitors are optimal in this respect and should be used when possible.
When the power supply regulator is not local on the board, adequate bypassing (a high value electrolytic capacitor) should be placed at the power entry point. The value of the capacitor depends on the total supply current of the circuits
on the PC board. All supply currents should be supplied by the capacitor instead of being drawn from the external supply lines, while the external supply charges the capacitor at a steady rate.
The ADC has two $\mathrm{V}_{\mathrm{D}}{ }^{+}$and DGND pins. It is recommended to use a $0.1 \mu \mathrm{~F}$ plus a $10 \mu \mathrm{~F}$ capacitor between pins 15 and $16\left(\mathrm{~V}_{\mathrm{D}}{ }^{+}\right)$and 14 (DGND) and a $0.1 \mu \mathrm{~F}$ capacitor between pins $28\left(\mathrm{~V}_{\mathrm{D}}{ }^{+}\right)$and 1 (DGND) for the PLCC package. The respective pins for the SO package are 21 and $22\left(\mathrm{~V}_{\mathrm{D}}{ }^{+}\right)$ and 20 (DGND), $6\left(\mathrm{~V}_{\mathrm{D}}{ }^{+}\right)$and 7 (DGND). The layout diagram in Figure 10 shows the recommended placement for the supply bypass capacitors.

## PC BOARD LAYOUT AND GROUNDING

## CONSIDERATIONS

To get the best possible performance from the ADC12048, the printed circuit boards should have separate analog and digital ground planes. The reason for using two ground planes is to prevent digital and analog ground currents from sharing the same path until they reach a very low impedance power supply point. This will prevent noisy digital switching currents from being injected into the analog ground.
Figure 10 illustrates a favorable layout for ground planes, power supply and reference input bypass capacitors. It shows a layout using a 44-pin PLCC socket and throughhole assembly. A similar approach should be used for the PQFP package.
The analog ground plane should encompass the area under the analog pins and any other analog components such as the reference circuit, input amplifiers, signal conditioning circuits, and analog signal traces.
The digital ground plane should encompass the area under the digital circuits and the digital input/output pins of the ADC12048. Having a continuous digital ground plane under the data and clock traces is very important. This reduces the overshoot/undershoot and high frequency ringing on these lines that can be capacitively coupled to analog circuitry sections through stray capacitances.
The AGND and DGND in the ADC12048 are not internally connected together. They should be connected together on the PC board right at the chip. This will provide the shortest return path for the signals being exchanged between the internal analog and digital sections of the ADC.
It is also a good design practice to have power plane layers in the PC board. This will improve the supply bypassing (an effective distributed capacitance between power and ground plane layers) and voltage drops on the supply lines. However, power planes are not as essential as ground planes are for satisfactory performance. If power planes are used, they should be separated into two planes and the area and connections should follow the same guidelines as mentioned for the ground planes. Each power plane should be laid out over its associated ground planes, avoiding any overlap between power and ground planes of different types. When the power planes are not used, it is recommended to use separate supply traces for the $\mathrm{V}_{\mathrm{A}}{ }^{+}$and $\mathrm{V}_{\mathrm{D}}{ }^{+}$pins from a low impedance supply point (the regulator output or the power entry point to the PC board). This will help ensure that the noisy digital supply does not corrupt the analog supply.

## Analog Application Information (Continued)



TL/H/12387-38 FIGURE 10. Top View of Printed Circuit Board for a 44-Pin PLCC ADC12048

When measuring AC input signals, any crosstalk between analog input/output lines and the reference lines ( CHO CH7, MUXOUT $\pm$, ADC $I N \pm, \mathrm{V}_{\text {REF }}{ }^{ \pm}$) should be minimized. Crosstalk is minimized by reducing any stray capacitance between the lines. This can be done by increasing the clearance between traces, keeping the traces as short as possible, shielding traces from each other by placing them on different sides of the AGND plane, or running AGND traces between them.

Figure 10 also shows the reference input bypass capacitors. Here the reference inputs are considered to be differential. The performance improves by having a $0.1 \mu \mathrm{~F}$ capacitor between the $\mathrm{V}_{\text {REF }}{ }^{+}$and $\mathrm{V}_{\text {REF }}{ }^{-}$, and by bypassing in a manner similar to that described for the supply pins. When a single ended reference is used, $\mathrm{V}_{\mathrm{REF}^{-}}$is connected to AGND and only two capacitors are used between $\mathrm{V}_{\text {REF }}{ }^{+}$ and $\mathrm{V}_{\text {REF }}-(0.1 \mu \mathrm{~F}+10 \mu \mathrm{~F})$. It is recommended to directly connect the AGND side of these capacitors to the $\mathrm{V}_{\mathrm{REF}}{ }^{-}$ instead of connecting $\mathrm{V}_{\text {REF }}{ }^{-}$and the ground sides of the capacitors separately to the ground planes. This provides a significantly lower-impedance connection when using surface mount technology.


Physical Dimensions inches (millimeters)


44-Lead Molded Plastic Leaded Chip Carrier
Order Number ADC12048CIV
NS Package Number V44A


| ヘnational semiconducto | Preliminary: Version 2. <br> $r \quad$ April 1997 |  |
| :---: | :---: | :---: |
| ADC14061 Auto-Calibrating 14-Bit, 2.2MHz, Sampling A/D Converter |  |  |
| General Description <br> The ADC14061 is a high performance integrated analog-to-digital converter. Using an innovative pipelined architecture, the ADC14061 digitizes signals to 14 bits at a sampling rate of 2.2MHz while consuming 300 mW from a single 5 V supply. Autocalibration and digital error correction keep INL and DNL at 14 - levels. levels. |  |  |
|  | Key Specifications | ${ }^{13}$ Bits Plus Sign |
| Auto-calibration eliminates the need for thin film trimming and the linearity drifts associated with the packaging and aging effects of hin film | El Converion Rate | $\begin{array}{r} 300 \mathrm{Hzz}-2.2 \mathrm{MHF} \\ 0.27 \mathrm{CB} \\ 0.25 \mathrm{SBB} \end{array}$ |
|  | ESuply Voltage | +5V 5\% |
| The Power Down input can be used to put the converter in a low power state when it is not converting. In this mode the ADC consumes less than 1 mW while maintaining all the autocalibrationcoefficients required for neariy instant conversions upoo exiting the Power Down Mode |  |  |
|  | Applications |  |
|  | - Preatision CCOD Imaging |  |
|  | - PC. Fisased Data A Acquisition |  |
|  |  |  |
|  | C Sood Analyzers |  |

## Connection Diagram


Ordering Information

| Commercial (0C to +70C) | Package |
| :--- | :---: |
| ADC14061CVF | VEG52A 52 Pin Thin Quad Flat Pack |

## LM9801 8-Bit Greyscale/24-Bit Color Linear CCD Sensor Processor

## General Description

The LM9801 is a high performance integrated signal processor/digitizer for linear CCD image scanners. The LM9801 performs all the analog processing (correlated double sampling for black level and offset compensation, pixel-by-pixel gain (shading) correction, and 8-bit analog-to-digital conversion) necessary to maximize the performance of a wide range of linear CCD sensors.
The LM9801 can be digitally programmed to work with a wide variety of CCDs from different manufacturers. An internal configuration register sets CCD and sampling timing to maximize performance, simplifying the design and manufacturing processes.
The LM9801 can be used with parallel output color CCDs. A signal inversion mode eases use with CIS sensors. For complementary voltage reference see the LM4041.

## Applications

- Color and Greyscale Flatbed and Sheetfed Scanners
- Fax and Multifunction Peripherals
- Digital Copiers

■ General Purpose Linear CCD Imaging

Features

- 2.5 Million pixels/s conversion rate
- Pixel-rate shading correction for individual pixels maximizes dynamic range and resolution, even on "weak" pixels
- Implements Correlated Double Sampling for minimum noise and offset error
- Reference and signal sampling points digitally controlled in 25 ns increments for maximum performance
- Generates all necessary CCD clock signals
- Compatible with a wide range of linear CCDs
- Supports some Contact Image Sensors (CIS)
- TTL/CMOS input/output compatible


## Key Specifications

- Resolution

8 Bits

- Pixel Conversion Rate
2.5 MHz

■ Supply Voltage +5V $\pm 5 \%$

- Supply Voltage (Digital I/O)
$+3.3 \mathrm{~V} \pm 10 \%$ or $+5 \mathrm{~V} \pm 5 \%$
- Power Dissipation 230 mW (max)


## Connection Diagrams




TL/H/12814-1
TL/H/12814-2

## Ordering Information

| Commercial ( $\left.\mathbf{0}^{\circ} \mathbf{C} \leq \mathbf{T}_{\mathbf{A}} \leq+\mathbf{7 0}^{\circ} \mathbf{C}\right)$ | Package |
| :--- | :---: |
| LM9801CCV | V52A 52-Pin Plastic Leaded Chip Carrier |
| LM9801CCVF | VEG52A 52-Pin Thin Quad Flatpack |

[^7]


| Electrical Characteristics (Continued) |  |  |  |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: |
| The following specifications apply for AGND $=\mathrm{DGND}=\mathrm{DGND}(\mathrm{I} / \mathrm{O})=0 \mathrm{~V}, \mathrm{~V}_{\mathrm{A}}=\mathrm{V}_{\mathrm{D}}=+5.0 \mathrm{~V}_{\mathrm{DC}}, \mathrm{V}_{\mathrm{D}(\mathrm{I} / \mathrm{O})}=+5.0$ or $+3.0 \mathrm{~V}_{\mathrm{DC}}$, REF $\mathrm{IN}=+1.225 \mathrm{~V}_{\mathrm{DC}}, \mathrm{f}_{\mathrm{MCLK}}=20 \mathrm{MHz}, \mathrm{R}_{\mathrm{S}}=25 \Omega$. All LSB units are ADC LSBs unless otherwise specified. Boldface limits apply for $\mathbf{T}_{\mathbf{A}}=\mathbf{T}_{\mathbf{J}}=\mathbf{T}_{\mathbf{M I N}}$ to $\mathbf{T}_{\mathbf{M A X}}$; all other limits $\mathrm{T}_{\mathrm{A}}=\mathrm{T}_{\mathrm{J}}=25^{\circ} \mathrm{C}$. (Notes 7, 8 and 11) |  |  |  |  |  |
| Symbol | Parameter | Conditions | Typical (Note 9) | Limits (Note 10) | Units (Limits) |
| SYSTEM CHARACTERISTICS |  |  |  |  |  |
|  | Full Channel Gain Error | VGA Gain $=1$, PGA Gain $=1$ | $\pm 0.6$ | $\pm 3.0$ | \% (max) |
| $\mathrm{V}_{\text {OS } 1}$ | Pre-PGA Offset Error | VGA Gain $=1$, Offset DAC $=0$ | $\pm 1$ |  | LSB |
| $\mathrm{V}_{\text {OS2 }}$ | Post-PGA Offset Error | Offset Add $=0$ | $\pm 1$ |  | LSB |
| REFERENCE AND ANALOG INPUT CHARACTERSTICS |  |  |  |  |  |
|  | OS Input Capacitance |  | 5 |  | pF |
|  | OS Input Leakage Current | Measured with $\mathrm{OS}=2.45 \mathrm{~V}_{\mathrm{DC}}$ | 2 | 20 | $n \mathrm{n}$ (max) |
| RREF | ADC Reference Ladder (REF OUT ${ }_{H I}$ to REF IN) Impedance |  | 950 | $\begin{gathered} 500 \\ 1400 \end{gathered}$ | $\Omega$ (min) <br> $\Omega$ (max) |
| REF IN | Reference Voltage (Note 13) |  | 1.225 | $\begin{aligned} & 1.19 \\ & 1.26 \end{aligned}$ | $V(\min )$ <br> V (max) |
| DC and Logic Electrical Characteristics <br> The following specifications apply for AGND $=\mathrm{DGND}=\mathrm{DGND}_{(\mathrm{I} / \mathrm{O})}=0 \mathrm{~V}, \mathrm{~V}_{\mathrm{A}}=\mathrm{V}_{\mathrm{D}}=+5.0 \mathrm{~V}_{\mathrm{DC}}, \mathrm{V}_{\mathrm{D}(\mathrm{I} / \mathrm{O})}=+5.0$ or $+3.0 \mathrm{~V}_{\mathrm{DC}}, R \mathrm{REF} \operatorname{IN}=+1.225 \mathrm{~V}_{\mathrm{DC}}, f_{\mathrm{MCLK}}=20 \mathrm{MHz}, \mathrm{R}_{\mathrm{S}}=25 \Omega$. Boldface limits apply for $\mathbf{T}_{\mathbf{A}}=\mathbf{T}_{\mathbf{J}}=\mathbf{T}_{\text {MIN }}$ to $\mathbf{T}_{\text {MAX }}$; all other limits $T_{A}=T_{J}=25^{\circ} \mathrm{C}$. (Notes 7 and 8) |  |  |  |  |  |
| Symbol | Parameter | Conditions | Typical (Note 9) | Limits (Note 10) | Units (Limits) |
| CDO-CD7, MCLK, SYNC, SDI, SCLK, $\overline{C S}, \overline{\text { RD }}$ DIGITAL INPUT CHARACTERISTICS |  |  |  |  |  |
| $\mathrm{V}_{\mathrm{IN}(1)}$ | Logical "1" Input Voltage ${ }^{\text {a }}$ | $\begin{aligned} & \mathrm{V}_{\mathrm{D}(\mathrm{I} / \mathrm{O})}=5.25 \mathrm{~V} \\ & \mathrm{~V}_{\mathrm{D}(\mathrm{I} / \mathrm{O})}=3.6 \mathrm{~V} \end{aligned}$ |  | $\begin{array}{r} 2.0 \\ 2.0 \\ \hline \end{array}$ | $\begin{aligned} & V(\min ) \\ & V(\min ) \end{aligned}$ |
| $\mathrm{V}_{\mathrm{IN}(0)}$ | Logical "0" Input Voltage | $\begin{aligned} & \mathrm{V}_{\mathrm{D}(I / O)}=4.75 \mathrm{~V} \\ & \mathrm{~V}_{\mathrm{D}(\mathrm{I} / \mathrm{O})}=2.7 \mathrm{~V} \end{aligned}$ |  | $\begin{aligned} & 0.8 \\ & 0.7 \\ & \hline \end{aligned}$ | $V$ (max) <br> $V$ (max) |
| IIN | Input Leakage Current $V$ <br>  $V$ | $\begin{aligned} & \mathrm{V}_{\mathrm{IN}}=\mathrm{V}_{\mathrm{D}} \\ & \mathrm{~V}_{\mathrm{IN}}=\mathrm{DGND} \end{aligned}$ | $\begin{gathered} 0.1 \\ -0.1 \\ \hline \end{gathered}$ |  | $\mu \mathrm{A}$ <br> $\mu \mathrm{A}$ |
| $\mathrm{C}_{\text {IN }}$ | Input Capacitance |  | 5 |  | pF |
| DD0-DD7, EOC, CCLK, SDO DIGITAL OUTPUT CHARACTERISTICS |  |  |  |  |  |
| $\mathrm{V}_{\text {OUT(1) }}$ | Logical "1" Output Voltage ${ }^{\text {a }}$ |  |  | $\begin{aligned} & 2.4 \\ & 4.4 \\ & 2.1 \\ & 2.5 \end{aligned}$ | $\begin{aligned} & \text { V }(\min ) \\ & \text { V }(\min ) \\ & \text { V }(\min ) \\ & \text { V }(\min ) \end{aligned}$ |
| $\mathrm{V}_{\text {OUT(0) }}$ | Logical '0" Output Voltage ${ }^{\text {a }}$ | $\begin{aligned} & \mathrm{V}_{\mathrm{D}(\mathrm{I} / \mathrm{O})}=5.25 \mathrm{~V}, \text { I IOUT } \\ & \mathrm{V}_{\mathrm{D}(\mathrm{I} / \mathrm{O})}=3.6 \mathrm{~V}, \mathrm{I}, 6 \mathrm{~mA} \\ & \text { IUT } \end{aligned}=1.6 \mathrm{~mA}$ |  | $\begin{aligned} & 0.4 \\ & 0.4 \\ & \hline \end{aligned}$ | $\begin{aligned} & \mathrm{V}(\max ) \\ & \mathrm{V}(\max ) \end{aligned}$ |
| Iout | TRI-STATE ${ }^{\circledR}$ Output Current (DD0-DD7 only) | $\begin{aligned} & \mathrm{V}_{\text {OUT }}=\mathrm{DGND} \\ & \mathrm{~V}_{\text {OUT }}=\mathrm{V}_{\mathrm{D}} \end{aligned}$ | $\begin{gathered} 0.1 \\ -0.1 \\ \hline \end{gathered}$ |  | $\mu \mathrm{A}$ <br> $\mu \mathrm{A}$ |
| COUT | TRI-STATE Output Capacitance |  | 5 |  | pF |
| $\phi 1, \phi 2$, RS, TR DIGITAL OUTPUT CHARACTERISTICS |  |  |  |  |  |
| V OUT(1) | Logical "1" Output Voltage ${ }^{\text {c\| }}$ | $\begin{aligned} & \mathrm{V}_{\mathrm{D}}=4.75 \mathrm{~V}, \text { I OUT }=-360 \mu \mathrm{~A} \\ & \mathrm{~V}_{\mathrm{D}}=4.75 \mathrm{~V}, \mathrm{I}_{\text {OUT }}=-10 \mu \mathrm{~A} \end{aligned}$ |  | $\begin{array}{r} 2.4 \\ 4.4 \\ \hline \end{array}$ | $\begin{aligned} & V(\min ) \\ & V(\min ) \end{aligned}$ |
| $\mathrm{V}_{\text {OUT(0) }}$ | Logical "0" Output Voltage ${ }^{\text {a }}$ | $\mathrm{V}_{\mathrm{D}}=5.25 \mathrm{~V}, \mathrm{l}_{\text {OUT }}=1.6 \mathrm{~mA}$ |  | 0.4 | $V$ (max) |

DC and Logic Electrical Characteristics (Continued)
The following specifications apply for $\mathrm{AGND}=\mathrm{DGND}=\mathrm{DGND}_{(/ / 0)}=0 \mathrm{~V}, \mathrm{~V}_{\mathrm{A}}=\mathrm{V}_{\mathrm{D}}=+5.0 \mathrm{~V}_{\mathrm{DC}}, \mathrm{V}_{\mathrm{D}(/ / 0)}=+5.0$ or $+3.0 \mathrm{~V}_{\mathrm{DC}}$, REF $I N=+1.225 \mathrm{~V}_{\mathrm{DC}}, \mathrm{f}_{\mathrm{MCLK}}=20 \mathrm{MHz}, \mathrm{R}_{\mathrm{S}}=25 \Omega$. Boldface limits apply for $\mathbf{T}_{\mathbf{A}}=\mathbf{T}_{\mathbf{J}}=\mathbf{T}_{\text {MIN }}$ to $\mathbf{T}_{\text {MAX }}$; all other limits $T_{A}=T_{J}=25^{\circ} \mathrm{C}$. (Notes 7 and 8 )

| Symbol | Parameter | Conditions | Typical (Note 9) | $\begin{aligned} & \text { Limits } \\ & \text { (Note 10) } \end{aligned}$ | Units (Limits) |
| :---: | :---: | :---: | :---: | :---: | :---: |
| POWER SUPPLY CHARACTERISTICS |  |  |  |  |  |
| ${ }^{\text {I }}$ A | Analog Supply Current | Operating Standby | $\begin{aligned} & 25 \\ & 50 \end{aligned}$ | 32 | $\mathrm{mA}_{\mu \mathrm{A}}^{\mathrm{max})}$ |
| ID | Digital Supply Current | Operating <br> MCLK = 0 | $\begin{gathered} 6 \\ 65 \\ \hline \end{gathered}$ | 8 | $\begin{gathered} \mathrm{mA}(\max ) \\ \mu \mathrm{A} \\ \hline \end{gathered}$ |
| $\mathrm{I}_{\mathrm{D}(1 / 0)}$ | Digital I/O Supply Current | Operating, $\mathrm{V}_{\mathrm{D}(1 / 0)}=5.0 \mathrm{~V}$ <br> Operating, $\mathrm{V}_{\mathrm{D}(/ / 0)}=3.0 \mathrm{~V}$ <br> MCLK $=0, \mathrm{~V}_{\mathrm{D}(/ / 0)}=5.0 \mathrm{~V}$ or 3.0 V | $\begin{aligned} & 3.1 \\ & 1.6 \\ & 1.7 \end{aligned}$ | $\begin{aligned} & 6 \\ & 4 \end{aligned}$ | mA (max) mA (max) mA |

AC Electrical Characteristics, MCLK Independent
The following specifications apply for AGND $=\mathrm{DGND}=\mathrm{DGND}_{(/ / 0)}=0 \mathrm{~V}, \mathrm{~V}_{\mathrm{A}}=\mathrm{V}_{\mathrm{D}}=\mathrm{V}_{\mathrm{D}(/ / 0)}=+5.0 \mathrm{~V}_{\mathrm{DC}}, \operatorname{REF} \operatorname{IN}=$ $+1.225 \mathrm{~V}_{\text {DC }}, \mathrm{f}_{\text {MCLK }}=20 \mathrm{MHz}, \mathrm{t}_{\text {MCLK }}=1 / \mathrm{f}_{\mathrm{MCLK}}, \mathrm{t}_{\mathrm{r}}=\mathrm{t}_{\mathrm{f}}=5 \mathrm{~ns}, \mathrm{R}_{\mathrm{s}}=25 \Omega, \mathrm{C}_{\mathrm{L}}$ (databus loading) $=50 \mathrm{pF} /$ pin. Boldface limits apply for $\mathbf{T}_{\mathbf{A}}=\mathbf{T}_{\mathbf{J}}=\mathbf{T}_{\text {MIN }}$ to $\mathbf{T}_{\mathbf{M A X}}$; all other limits $\mathrm{T}_{\mathbf{A}}=\mathrm{T}_{\mathbf{J}}=25^{\circ} \mathrm{C}$. (Notes 7 and 8)

| Symbol | Parameter | Conditions | Typical (Note 9) | Limits (Note 10) | Units (Limits) |
| :---: | :---: | :---: | :---: | :---: | :---: |
| $\mathrm{f}_{\text {MCLK }}$ | Maximum MCLK Frequency Minimum MCLK Frequency |  |  | $\begin{gathered} 20 \\ 1 \end{gathered}$ | MHz (min) <br> MHz (max) |
|  | MCLK Duty Cycle |  | $\begin{aligned} & 30 \\ & 70 \end{aligned}$ | $\begin{aligned} & 40 \\ & 60 \end{aligned}$ | \% (min) <br> \% (max) |
| $t_{\text {A }}$ | SYNC Setup of MCLK |  | 5 | 10 | ns (min) |
| tCDSETUP | Correction Data Valid to CLK Setup |  | 14 | 20 | ns (min) |
| $\mathrm{t}_{\text {CDHOLD }}$ | Correction Data Valid to CLK Hold |  | -12 | 0 | ns (min) |
| $t_{\text {D1H }}, t_{\text {DOH }}$ | $\overline{\mathrm{RD}}$ High to DD0-DD7 TRI-STATE |  | 5 | 15 | ns (max) |
| $t_{\text {DACC }}$ | Access Time Delay from $\overline{\mathrm{RD}}$ Low to DD0-DD7 Data Valid |  | 15 | 30 | ns (max) |
| $\mathrm{f}_{\text {SCLK }}$ | Maximum SCLK Frequency |  |  | 20 | $\mathrm{MHz}(\min )$ |
|  | SCLK Duty Cycle |  |  | $\begin{aligned} & 40 \\ & 60 \end{aligned}$ | $\begin{aligned} & \%(\min ) \\ & \%(\max ) \end{aligned}$ |
| ${ }_{\text {tSDI }}$ | SDI Set-Up Time from SCLK Rising Edge |  | 3 | 10 | ns (min) |
| $t_{\text {HDI }}$ | SDI Hold Time from SCLK Rising Edge |  | 2 | 15 | ns (min) |
| $t_{\text {DDO }}$ | Delay from SCLK Falling Edge to SDO Data Valid |  | 25 | 50 | ns (max) |
| $\mathrm{t}_{\mathrm{HDO}}$ | SDO Hold Time from SCLK Falling Edge | $\mathrm{R}_{\mathrm{L}}=3 \mathrm{k}, \mathrm{C}_{\mathrm{L}}=50 \mathrm{pF}$ | 30 | $\begin{gathered} 50 \\ 5 \\ \hline \end{gathered}$ | ns (max) ns (min) |
| ${ }^{\text {t }}$ DELAY | DELAY from SCLK Falling Edge to $\overline{\text { CS Rising or Falling Edge }}$ |  | 5 | 10 | ns (min) |
| ${ }^{\text {t SETUP }}$ | Set-Up Time of $\overline{C S}$ Rising or Falling Edge to SCLK Rising Edge |  | 0 | 10 | ns (min) |

AC Electrical Characteristics, MCLK Independent (Continued)
The following specifications apply for $A G N D=D G N D=D G N D_{(I / O)}=0 \mathrm{~V}, \mathrm{~V}_{\mathrm{A}}=\mathrm{V}_{\mathrm{D}}=\mathrm{V}_{\mathrm{D}(\mathrm{I} / \mathrm{O})}=+5.0 \mathrm{~V}_{\mathrm{DC}}$, REF $I \mathrm{~N}=$ $+1.225 \mathrm{~V}_{\text {DC }}, \mathrm{f}_{\text {MCLK }}=20 \mathrm{MHz}, \mathrm{t}_{\mathrm{MCLK}}=1 / \mathrm{f}_{\mathrm{MCLK}}, \mathrm{t}_{\mathrm{r}}=\mathrm{t}_{\mathrm{f}}=5 \mathrm{~ns}, \mathrm{R}_{\mathrm{S}}=25 \Omega, \mathrm{C}_{\mathrm{L}}$ (databus loading) $=50 \mathrm{pF} /$ pin. Boldface limits apply for $\mathbf{T}_{\mathbf{A}}=\mathbf{T}_{\mathbf{J}}=\mathbf{T}_{\text {MIN }}$ to $\mathbf{T}_{\text {MAX }}$; all other limits $\mathrm{T}_{\mathrm{A}}=\mathrm{T}_{\mathrm{J}}=25^{\circ} \mathrm{C}$. (Notes 7 and 8)

| Symbol | Parameter | Conditions | Typical (Note 9) | Limits (Note 10) | Units <br> (Limits) |
| :---: | :---: | :---: | :---: | :---: | :---: |
| $\mathrm{t}_{\mathrm{S} 1 \mathrm{H},} \mathrm{tsOH}^{\text {d }}$ | Delay from $\overline{\mathrm{CS}}$ Rising Edge to SDO TRI-STATE | $\mathrm{R}_{\mathrm{L}}=3 \mathrm{k}, \mathrm{C}_{\mathrm{L}}=50 \mathrm{pF}$ | 25 | 50 | ns (max) |
| $t_{\text {RDO }}$ | SDO Rise Time, TRI-STATE to High SDO Rise Time, Low to High | $\mathrm{R}_{\mathrm{L}}=3 \mathrm{k}, \mathrm{C}_{\mathrm{L}}=50 \mathrm{pF}$ | $\begin{aligned} & 20 \\ & 20 \end{aligned}$ |  | $\begin{aligned} & \text { ns } \\ & \text { ns } \end{aligned}$ |
| $\mathrm{t}_{\text {FDO }}$ | SDO Fall Time, TRI-STATE to Low SDO Fall Time, High to Low | $\mathrm{R}_{\mathrm{L}}=3 \mathrm{k}, \mathrm{C}_{\mathrm{L}}=50 \mathrm{pF}$ | $\begin{aligned} & 20 \\ & 20 \end{aligned}$ |  | $\begin{aligned} & \mathrm{ns} \\ & \mathrm{~ns} \end{aligned}$ |

## AC Electrical Characteristics, MCLK Dependent

The following specifications apply for $A G N D=D G N D=D G N D_{(I / O)}=0 \mathrm{~V}, \mathrm{~V}_{\mathrm{A}}=\mathrm{V}_{\mathrm{D}}=\mathrm{V}_{\mathrm{D}(\mathrm{I} / \mathrm{O})}=+5.0 \mathrm{~V}_{\mathrm{DC}}$, REF IN $=$ $+1.225 \mathrm{~V}_{\mathrm{DC}}, \mathrm{f}_{\mathrm{MCLK}}=20 \mathrm{MHz}, \mathrm{t}_{\mathrm{MCLK}}=1 / \mathrm{f}_{\mathrm{MCLK}}, \mathrm{t}_{\mathrm{r}}=\mathrm{t}_{\mathrm{f}}=5 \mathrm{~ns}, \mathrm{R}_{\mathrm{s}}=25 \Omega, \mathrm{C}_{\mathrm{L}}$ (databus loading) $=50 \mathrm{pF} / \mathrm{pin}$. Refer to Table 2, Configuration Register Parameters, for limits labelled C.R. Boldface limits apply for $\mathbf{T}_{\mathbf{A}}=\mathbf{T}_{\mathbf{J}}=\mathbf{T}_{\text {min }}$ to $\mathbf{T}_{\text {MAX }}$; all other limits $\mathrm{T}_{\mathrm{A}}=\mathrm{T}_{\mathrm{J}}=25^{\circ} \mathrm{C}$. (Notes 7 and 8 )

| Symbol | Parameter | Conditions | Typical <br> (Note 9) | Limits (Note 10) | Units (Limits) |
| :---: | :---: | :---: | :---: | :---: | :---: |
| $\mathrm{t}_{\text {START }}$ | MCLK to first $\phi 1$ High |  | 50 ns | 1 | $\mathrm{t}_{\text {MCLK }}$ |
| $\mathrm{t}_{\phi}$ | $\phi 1, \phi 2$ Clock Period | Standard CCD Mode Even/Odd CCD Mode | $400 \mathrm{~ns}$ $800 \mathrm{~ns}$ | $\begin{gathered} 8 \\ 16 \end{gathered}$ | $\mathrm{t}_{\text {MCLK }}$ <br> $\mathrm{t}_{\text {MCLK }}$ |
| ${ }_{\text {t }}$ TRWIDTH | Transfer Pulse (TR) Width |  |  | C.R. | $\mu \mathrm{s}$ |
| $\mathrm{t}_{\text {GUARD }}$ | $\phi 1$ to TR, TR to $\phi 1$ Guardband |  |  | C.R. | ns |
| $\mathrm{t}_{\text {RSWIDTH }}$ | Reset Pulse (RS) Width |  |  | C.R. | ns |
| $t_{\text {RS }}$ | Falling Edge of $\phi 1$ to RS Either Edge of $\phi 1$ to RS | Standard CCD Mode Even/Odd CCD Mode |  | C.R. | ns |
| ts/HREF | Falling Edge of $\phi 1$ to Ref. Sample Either Edge of $\phi 1$ to Ref. Sample | Standard CCD Mode Even/Odd CCD Mode |  | C.R. | ns |
| ts/HSIG | Falling Edge of $\phi 1$ to Sig. Sample Either Edge of $\phi 1$ to Sig. Sample | Standard CCD Mode Even/Odd CCD Mode |  | C.R. | ns |
| $\mathrm{t}_{\text {S/HWIDTH }}$ | Sample Pulse Width (Acquisition Time) |  | 50 ns | 1 | ${ }^{\text {tMCLK }}$ |
| tsYnclow | SYNC Low Between Lines |  | 100 ns | 2 | $\mathrm{t}_{\text {MCLK }}(\mathrm{min})$ |
| $t_{B}$ | SYNC Setup of $\phi 1$ to End Line |  |  | 2 | $\mathrm{t}_{\text {MCLK }}$ (max) |
| ${ }^{\text {t CCLKWWIDTH }}$ | CCLK Pulse Width |  | 250 ns | 5 | $\mathrm{t}_{\text {MCLK }}$ |
| t DATAVALID | Data Valid Time from EOC Low |  |  | 300 | ns (min) |
| teOCWIDTH | EOC Pulse Width |  | 250 ns | 5 | $\mathrm{t}_{\text {MCLK }}$ |
|  | $\phi 1$ and $\phi 2$ Frequency | Standard CCD Mode Even/Odd CCD Mode | $\begin{aligned} & 2.5 \mathrm{MHz} \\ & 1.25 \mathrm{MHz} \end{aligned}$ | $\begin{array}{r} \mathrm{f}_{\mathrm{MCLK}} / \mathbf{8} \\ \mathrm{f}_{\mathrm{MCLK}} / \mathbf{1 6} \\ \hline \end{array}$ | $\begin{aligned} & \mathrm{Hz} \\ & \mathrm{~Hz} \end{aligned}$ |
|  | $\phi 1$ and $\phi 2$ Duty Cycle |  |  | 50 | \% |

## Electrical Characteristics (Continued)

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional, but do not guarantee specific performance limits. For guaranteed specifications and test conditions, see the Electrical Characteristics. The guaranteed specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed les conditions.

Note 2: All voltages are measured with respect to $G N D=A G N D=D G N D=D G N D_{(I / O)}=0 V$, unless otherwise specified.
Note 3: When the input voltage $\left(V_{I N}\right)$ at any pin exceeds the power supplies ( $\mathrm{V}_{\mathrm{IN}}<G N D$ or $\mathrm{V}_{\mathrm{IN}}>\mathrm{V}_{A}$ or $\mathrm{V}_{\mathrm{D}}$ ), the current at that pin should be limited to 25 mA . The 50 mA maximum package input current rating limits the number of pins that can simultaneously safely exceed the power supplies with an input current of 25 mA to two.

Note 4: The maximum power dissipation must be derated at elevated temperatures and is dictated by $\mathrm{T}_{\mathrm{Jmax}}, \theta_{\mathrm{JA}}$ and the ambient temperature, $\mathrm{T}_{\mathrm{A}}$. The maximum allowable power dissipation at any temperature is $P_{D}=\left(T_{J \max }-T_{A}\right) / \theta_{J A}$. $T_{J \max }=150^{\circ} \mathrm{C}$ for this device. The typical thermal resistance $\left(\theta_{J A}\right)$ of this part when board mounted is $52^{\circ} \mathrm{C} / \mathrm{W}$ for the V52A PLCC package, and $70^{\circ} \mathrm{C} / \mathrm{W}$ for the VEG52A TQFP package.
Note 5: Human body model, 100 pF capacitor discharged through a $1.5 \mathrm{k} \Omega$ resistor
Note 6: See AN450 "Surface Mounting Methods and Their Effect on Product Reliability" or the section titled "Surface Mount" found in any National Semiconductor Linear Data Book for other methods of soldering surface mount devices.
Note 7: A Zener diode clamps the OS analog input to AGND as shown below. This input protection, in combination with the external clamp capacitor and the output impedance of the CCD, prevents damage to the LM9801 from transients during power-up.


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Note 8: To guarantee accuracy, it is required that $V_{A}$ and $V_{D}$ be connected together to the same power supply with separate bypass capacitors at each supply pin. Note 9: Typicals are at $T_{J}=T_{A}=25^{\circ} \mathrm{C}, \mathrm{f}_{\mathrm{MCLK}}=20 \mathrm{MHz}$, and represent most likely parametric norm.
Note 10: Tested limits are guaranteed to National's AOQL (Average Outgoing Quality Level).
Note 11: For CCDs, $V_{B L A C K}$ is defined as the CCD OS voltage for the reference period following the reset feedthrough pulse. $V_{\text {WHITE }}$ is defined as the peak CCD pixel output voltage for a white (full scale) image with respect to the reference level, $V_{B L A C K}-V_{R F T}$ is defined as the peak positive deviation above $\mathrm{V}_{\text {BLACK }}$ of the reset feedthrough pulse. For CIS, $\mathrm{V}_{\text {WHITE }}$ is defined as the peak CCD pixel output voltage for a white (full scale) image with respect to GND (OV). The maximum correctable range of pixel-to-pixel $\mathrm{V}_{\text {WHITE }}$ variation is defined as the maximum variation in $\mathrm{V}_{\text {WHITE }}$ (due to PRNU, light source intensity variation, optics, etc.) that the LM9801 can correct for using its internal PGA.


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TL/H/12814-5
Note 12: Integral linearity error is defined as the deviation of the analog value, expressed in LSBs, from the straight line that best fits the actual transfer function of the ADC.
Note 13: Reference voltages below 1.19 V may decrease SNR. Reference voltages above 1.26 V may cause clipping errors inside the LM9801. The LM4041EIM3-1.2 (SOT-23 package) or the LM4041EIZ-1.2 (TO-92 package) bandgap voltage references are recommended for this application.
Note 14: PGA Gain Error is the maximum difference between the measured gain for any PGA code and the ideal gain calculated by using the formula Gain $_{P G A}\left(\frac{V}{V}\right)=1+C \frac{P G A ~ c o d e}{256}$ where $C=(P G A$ RANGE -1$) \frac{256}{255}$ and PGA RANGE $=$ the PGA adjustment range (in V/V) of the LM9801 under test.

Note 15: VGA Gain Error is the maximum difference between the measured gain for any VGA code and the ideal gain calculated by using the formula Gain $_{\text {VGA }}(\mathrm{dB})=\mathrm{C} \frac{\mathrm{VGA} \text { code }}{16}$ where $\mathrm{C}=\left(\right.$ VGA RANGE) $\frac{16}{15}$ and VGA RANGE $=$ the VGA adjustment range (in dB ) of the LM9801 under test.

## Typical Performance Characteristics

$\phi 1, \phi 2$, ns, and TR Rise and Fal
Times Through a Series Resistance
vs Load Capacitance

load capacitance (pF)

Pin Descriptions

| CCD Driver Signals |  |
| :---: | :---: |
| $\phi 1$ | Digital Output. CCD clock signal, phase 1. |
| ¢2 | Digital Output. CCD clock signal, phase 2. |
| RS | Digital Output. Reset pulse for the CCD. |
| TR | Digital Output. Transfer pulse for the CCD. |
| Analog I/O |  |
| OS | Analog Input. This is the OS (Output Signal) from the CCD. The maximum peak signal that can be accurately digitized is equal to the voltage at REF IN, typically 1.225 V . |
| REF IN | Analog Inputs. These two pins are the system reference voltage inputs and should be tied together to a 1.225 V voltage source and bypassed to AGND with a 0.1 $\mu \mathrm{F}$ monolithic capacitor. |
| REF OUT ${ }_{\text {HI }}$ | Analog Output. This reference voltage is developed internally by the LM9801, and is equal to 3 times REF IN. It should be bypassed to AGND with a $0.1 \mu \mathrm{~F}$ monolithic capacitor. |
| REF OUT ${ }_{\text {MID }}$ | Analog Output. This reference voltage is developed internally by the LM9801, and is equal to 2 times REF IN. It should be bypassed to AGND using a $0.1 \mu \mathrm{~F}$ monolithic capacitor. |
| $V_{\text {TEST1 }}$, <br> $V_{\text {TEST2 }}$ | Analog Inputs/Outputs. These pins are used for testing the device during manufacture and should be left unconnected. |
| General Digital I/O |  |
| MCLK | Digital Input. This is the 20 MHz (typical) master system clock. |
| SYNC | Digital Input. A low-to-high transition on this input begins a line scan operation. The line scan operation terminates when this input is taken low. |
| Configuration Register I/O |  |
| SDI | Digital Input. Serial Data Input pin. |
| SDO | Digital Output. Serial Data Output pin. |
| SCLK | Digital Input. This is the serial data clock, used to clock data in through SDI and out through SDO. SCLK is asynchronous to MCLK. Input data is latched and output data is changed on the rising edge of SCLK. |
| $\overline{\mathrm{CS}}$ | Digital Input. This is the Chip Select signal for writing to the Configuration Register through the serial interface. This input must be low in order to communicate with the Configuration Register. This pin is used for serial I/O only-it has no effect on any other section of the chip. |

## Timing Diagrams



TL/H/12814-9
DIAGRAM 1. Line Scan Timing Overview



## Timing Diagrams (Continued)



TL/H/12814-15
Note: Clamp signal only active during optical black pixels at beginning of line
DIAGRAM 7. CCD Timing


Timing Diagrams (Continued)


TL/H/12814-17
Note: $\mathrm{i}=$ value programmed in Dummy Pixel Register - 1 (for example: Dummy Pixel Register $=17 \rightarrow \mathrm{i}=16 \rightarrow 16$ dummy pixels). $j=$ value programmed in Optical Black Register

DIAGRAM 9. Dummy Pixel and Optical Black Pixel Timing


DIAGRAM 10. Coefficient Data Timing


* Signal internal to LM9801

DIAGRAM 11. Output Data Timing

Timing Diagrams (Continued)


> DIAGRAM 12. Data Timing (Output and Coefficient Data Sharing Same Bus)

## Serial Configuration Register Timing Diagrams



## Serial Configuration Register Timing Diagrams (Continued)




Note: $\mathrm{t}_{\text {MCLK }}=1 / \mathrm{f}_{\text {MCLK }}=1$ MCLK period. Examples given in parenthesis are for $\mathrm{f}_{\text {MCLK }}=20 \mathrm{MHz}\left(\mathrm{t}_{\text {MCLK }}=50 \mathrm{~ns}\right)$.

| TABLE II. Configuration Register Parameters (Continued) |  |  |  |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: |
| Parameter | Control Bits |  |  |  | Result |
| RS Pulse Position (tRS) | RSPOS3 | RSPOS2 | RSPOS1 | RSPOSO |  |
|  | 0 | 0 | 0 | 0 | $0.0 \mathrm{t}_{\text {MCLK }}(0 \mathrm{~ns}$ ) |
|  | 0 | 0 | 0 | 1 | $0.5 \mathrm{t}_{\text {MCLK }}(25 \mathrm{~ns})$ |
|  | 0 | 0 | 1 | 0 | $1.0 \mathrm{t}_{\text {MCLK }}(50 \mathrm{~ns})$ |
|  | 0 | 0 | 1 | 1 | $1.5 \mathrm{t}_{\text {MCLK }}(75 \mathrm{~ns})$ |
|  | 0 | 1 | 0 | 0 | $2.0 \mathrm{t}_{\text {MCLK }}(100 \mathrm{~ns})$ |
|  | 0 | 1 | 0 | 1 | $2.5 \mathrm{t}_{\text {MCLK }}(125 \mathrm{~ns})$ |
|  | 0 | 1 | 1 | 0 | $3.0 \mathrm{t}_{\text {MCLK }}(150 \mathrm{~ns})$ |
|  | 0 | 1 | 1 | 1 | $3.5 \mathrm{t}_{\text {MCLK }}(175 \mathrm{~ns})$ |
|  | 1 | 0 | 0 | 0 | $4.0 \mathrm{t}_{\text {MCLK }}(200 \mathrm{~ns})$ |
|  | 1 | 0 | 0 | 1 | $4.5 \mathrm{t}_{\text {MCLK }}(225 \mathrm{~ns})$ |
|  | 1 | 0 | 1 | 0 | $5.0 \mathrm{t}_{\text {MCLK }}(250 \mathrm{~ns})$ |
|  | 1 | 0 | 1 | 1 | $5.5 \mathrm{t}_{\text {MCLK }}(275 \mathrm{~ns})$ |
|  | 1 | 1 | 0 | 0 | $6.0 \mathrm{t}_{\text {MCLK }}(300 \mathrm{~ns})$ |
|  | 1 | 1 | 0 | 1 | $6.5 \mathrm{t}_{\text {MCLK }}(325 \mathrm{~ns})$ |
|  | 1 | 1 | 1 | 0 | $7.0 \mathrm{t}_{\text {MCLK }}(350 \mathrm{~ns})$ |
|  | 1 | 1 | 1 | 1 | $7.5 \mathrm{t}_{\text {MCLK }}(375 \mathrm{~ns}$ ) |
| Sample Reference Position (ts/HREF) | SR3 | SR2 | SR1 | SR0 |  |
|  | 0 | 0 | 0 | 0 | 0.01 ${ }_{\text {MCLK }}$ (0 ns) |
|  | 0 | 0 | 0 | 1 | $0.5 \mathrm{t}_{\text {MCLK }}(25 \mathrm{~ns})$ |
|  | 0 | 0 | 1 | 0 | $1.0 \mathrm{t}_{\text {MCLK }}(50 \mathrm{~ns})$ |
|  | 0 | 0 | 1 | 1 | $1.5 \mathrm{t}_{\text {MCLK }}(75 \mathrm{~ns})$ |
|  | 0 | 1 | 0 | 0 | $2.0 \mathrm{t}_{\text {MCLK }}(100 \mathrm{~ns})$ |
|  | 0 | 1 | 0 | 1 | $2.5 \mathrm{t}_{\text {MCLK }}(125 \mathrm{~ns})$ |
|  | 0 | 1 | 1 | 0 | $3.0 \mathrm{t}_{\text {MCLK }}(150 \mathrm{~ns})$ |
|  | 0 | 1 | 1 | 1 | $3.5 \mathrm{t}_{\text {MCLK }}(175 \mathrm{~ns})$ |
|  | 1 | 0 | 0 | 0 | $4.0 \mathrm{t}_{\text {MCLK }}(200 \mathrm{~ns})$ |
|  | 1 | 0 | 0 | 1 | $4.5 \mathrm{t}_{\text {MCLK }}(225 \mathrm{~ns})$ |
|  | 1 | 0 | 1 | 0 | $5.0 \mathrm{t}_{\text {MCLK }}(250 \mathrm{~ns})$ |
|  | 1 | 0 | 1 | 1 | $5.5 \mathrm{t}_{\text {MCLK }}(275 \mathrm{~ns})$ |
|  | 1 | 1 | 0 | 0 | $6.0 \mathrm{t}_{\text {MCLK }}(300 \mathrm{~ns})$ |
|  | 1 | 1 | 0 | 1 | $6.5 \mathrm{t}_{\text {MCLK }}(325 \mathrm{~ns})$ |
|  | 1 | 1 | 1 | 0 | $7.0 \mathrm{t}_{\text {MCLK }}(350 \mathrm{~ns}$ ) |
|  | 1 | 1 | 1 | 1 | Not Valid |
| Sample Signal Position ( $\mathrm{t}_{\mathrm{S} / \mathrm{HSIG}}$ ) | SS3 | SS2 | SS1 | SSO |  |
|  | 0 | 0 | 0 | 0 | 0.01 ${ }_{\text {MCLK }}$ (0 ns) |
|  | 0 | 0 | 0 | 1 | $0.5 \mathrm{t}_{\text {MCLK }}(25 \mathrm{~ns})$ |
|  | 0 | 0 | 1 | 0 | $1.0 \mathrm{t}_{\text {MCLK }}(50 \mathrm{~ns})$ |
|  | 0 | 0 | 1 | 1 | $1.5 \mathrm{t}_{\text {MCLK }}(75 \mathrm{~ns}$ ) |
|  | 0 | 1 | 0 | 0 | $2.0 \mathrm{t}_{\text {MCLK }}(100 \mathrm{~ns})$ |
|  | 0 | 1 | 0 | 1 | $2.5 \mathrm{t}_{\text {MCLK }}(125 \mathrm{~ns})$ |
|  | 0 | 1 | 1 | 0 | $3.0 \mathrm{t}_{\text {MCLK }}(150 \mathrm{~ns})$ |
|  | 0 | 1 | 1 | 1 | $3.5 \mathrm{t}_{\text {MCLK }}(175 \mathrm{~ns})$ |
|  | 1 | 0 | 0 | 0 | $4.0 \mathrm{t}_{\text {MCLK }}(200 \mathrm{~ns})$ |
|  | 1 | 0 | 0 | 1 | $4.5 \mathrm{t}_{\text {MCLK }}(225 \mathrm{~ns})$ |
|  | 1 | 0 | 1 | 0 | $5.0 \mathrm{t}_{\text {MCLK }}(250 \mathrm{~ns})$ |
|  | 1 | 0 | 1 | 1 | $5.5 \mathrm{t}_{\text {MCLK }}(275 \mathrm{~ns})$ |
|  | 1 | 1 | 0 | 0 | $6.0 \mathrm{t}_{\text {MCLK }}(300 \mathrm{~ns})$ |
|  | 1 | 1 | 0 | 1 | $6.5 \mathrm{t}_{\text {MCLK }}(325 \mathrm{~ns})$ |
|  | 1 | 1 | 1 | 0 | $7.0 \mathrm{t}_{\text {MCLK }}(350 \mathrm{~ns})$ |
|  | 1 | 1 | 1 | 1 | 7.54 MCLK ( 375 ns ) |

Note: $\mathrm{t}_{\text {MCLK }}=1 / \mathrm{f}_{\text {MCLK }}=1$ MCLK period. Examples given in parenthesis are for $\mathrm{f}_{\text {MCLK }}=20 \mathrm{MHz}$ ( $\mathrm{t}_{\text {MCLK }}=50 \mathrm{~ns}$ ).



Note: $\mathrm{t}_{\text {MCLK }}=1 / \mathrm{f}_{\text {MCLK }}=1$ MCLK period. Examples given in parenthesis are for $\mathrm{f}_{\text {MCLK }}=20 \mathrm{MHz}\left(\mathrm{t}_{\text {MCLK }}=50 \mathrm{~ns}\right)$

| TABLE II. Configuration Register Parameters (Continued) |  |  |  |  |  |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| Parameter |  |  |  | Con | Bits |  | Result |
| Offset DAC | ODSIGN | VOS3 | VOS2 | VOS1 | VOSO |  | Offset (LSB) (typical) |
|  | 0 | 0 | 0 | 0 | 0 |  | 0.00 |
|  | 0 | 0 | 0 | 0 | 1 |  | -0.42 |
|  | 0 | 0 | 0 | 1 | 0 |  | -0.84 |
|  | 0 | 0 | 0 | 1 | 1 |  | -1.26 |
|  | 0 | 0 | 1 | 0 | 0 |  | -1.68 |
|  | 0 | 0 | 1 | 0 | 1 |  | -2.10 |
|  | 0 | 0 | 1 | 1 | 0 |  | -2.52 |
|  | 0 | 0 | 1 | 1 | 1 |  | -2.94 |
|  | 0 | 1 | 0 | 0 | 0 |  | -3.36 |
|  | 0 | 1 | 0 | 0 | 1 |  | -3.78 |
|  | 0 | 1 | 0 | 1 | 0 |  | -4.20 |
|  | 0 | 1 | 0 | 1 | 1 |  | -4.62 |
|  | 0 | 1 | 1 | 0 | 0 |  | -5.04 |
|  | 0 | 1 | 1 | 0 | 1 |  | -5.46 |
|  | 0 | 1 | 1 | 1 | 0 |  | -5.88 |
|  | 0 | 1 | 1 | 1 | 1 |  | -6.30 |
|  | 1 | 0 | 0 | 0 | 0 |  | 0.00 |
|  | 1 | 0 | 0 | 0 | 1 |  | +0.42 |
|  | 1 | 0 | 0 | 1 | 0 |  | +0.84 |
|  | 1 | 0 | 0 | 1 | 1 |  | +1.26 |
|  | 1 | 0 | 1 | 0 | 0 |  | +1.68 |
|  | 1 | 0 | 1 | 0 | 1 |  | +2.10 |
|  | 1 | 0 | 1 | 1 | 0 |  | +2.52 |
|  | 1 | 0 | 1 | 1 | 1 |  | +2.94 |
|  | 1 | 1 | 0 | 0 | 0 |  | +3.36 |
|  | 1 | 1 | 0 | 0 | 1 |  | +3.78 |
|  | 1 | 1 | 0 | 1 | 0 |  | +4.20 |
|  | 1 | 1 | 0 | 1 | 1 |  | +4.62 |
|  | 1 | 1 | 1 | 0 | 0 |  | +5.04 |
|  | 1 | 1 | 1 | 0 | 1 |  | $+5.46$ |
|  | 1 | 1 | 1 | 1 | 0 |  | +5.88 |
|  | 1 | 1 | 1 | 1 | 1 |  | +6.30 |

Note: $\mathrm{t}_{\text {MCLK }}=1 / \mathrm{f}_{\text {MCLK }}=1$ MCLK period. Examples given in parenthesis are for $\mathrm{f}_{\text {MCLK }}=20 \mathrm{MHz}$ ( $\mathrm{t}_{\text {MCLK }}=50 \mathrm{~ns}$ ).

## Block Diagram of LM9801-Based System



TL/H/12814-28
Note: Power supplies and bypass capacitors not shown for clarity.
FIGURE 1. LM9801 System Block Diagram

## Applications Information

### 1.0 THEORY OF OPERATION

The LM9801 removes errors from and digitizes a linear CCD pixel stream, while providing all the necessary clock signals to drive the CCD. Offset and gain errors for individual pixels are removed at the pixel rate. Offset errors are removed through correlated double sampling (CDS). Gain errors (which may come from any combination of PRNU, uneven illumination, $\cos ^{4}$ effect, RGB filter mismatch, etc.) are removed through the use of a 8 -bit programmable gain amplifier (PGA) in front of the ADC.

### 1.1 The Analog Signal Path <br> (See Block Diagram)

The analog output signal from the CCD is connected to the OS input of the LM9801 through a $0.01 \mu \mathrm{~F}$ (typical, see Section 4.2, Clamp Capacitor Selection) DC blocking capacitor. During the CCD's optical black pixel segment at the beginning of every line, this input is clamped to the REF OUT $_{\text {MID }}$ voltage (approximately 2.45 V ). This DC restore operation fixes the reference level of the CCD pixel stream at REF OUT ${ }_{\text {MID }}$.
The signal is then buffered and fed to a digitally-programmed 4-bit VGA (variable gain amplifier). The gain of the VGA is digitally programmable in 16 steps from 1V/V to $3 \mathrm{~V} / \mathrm{V}$. The VGA is used to compensate for peak white CCD outputs less than the 1.225 V full-scale required by the LM9801 for maximum dynamic range. When used with parallel output CCDs, the VGA can fine-tune the amplitude of the red, green, and blue signals. For a detailed explanation of the VGA, see Section 4.3.
The output of the VGA goes into the CDS (Correlated Double Sampling) stage, consisting of two sample/hold amplifiers: S/H Ref (Reference) and S/H Signal. The reference level of the signal is sampled and held by the S/H Ref circuit and the active pixel data is sampled and held by the $\mathrm{S} /$ H Signal circuit. The output of S/H Ref is subtracted from the S/H Signal output and amplified by 2. The full-scale signal range at this point is approximately $2.45 \mathrm{Vp}-\mathrm{p}$. CDS reduces or eliminates many sources of noise, including reset noise, flicker noise, and both high and low frequency pixel-to-pixel offset variation. For more information on the CDS stage, see Section 4.4.
At this point an offset voltage can be injected by the 5-bit (4 bits + sign) Offset DAC. This voltage is designed to compensate for any small fixed DC offset introduced by the CDS S/Hs and the $x 2$ amplifier. The LSB size of the DAC is approximately 0.42 ADC LSBs ( 4 mV ). The adjustment range is $\pm 6.3$ ADC LSBs. For a detailed explanation of the Offset DAC, see Section 4.6.
The next stage is the PGA. This is a programmable gain amplifier that changes the gain at the pixel rate to correct for gain errors due to PRNU, uneven illumination (such as $\cos ^{4}$ effect), RGB filter mismatch, etc. The gain adjustment range is 0 dB to $9 \mathrm{~dB}(1 \mathrm{~V} / \mathrm{V}$ to $3 \mathrm{~V} / \mathrm{V})$ with 8 bits of resolution. The gain data (correction coefficients) is provided on the CD0-CD7 bus. The gain may also be fixed at any value between 0 dB and 9 dB with the PGA Gain Coefficient configuration register. For additional information on the PGA, see Section 4.7.

An approximately 2 LSB ( 29 mV ) offset can be added at the output of the PGA stage if necessary to ensure that the offset is greater than zero. This eliminates the possibility of a negative offset clipping the darkest output pixels. For more information on the Offset Add Bit, see Section 4.8.
Finally, the output of the PGA is digitized by the ADC and made available on the DD0-DD7 bus (Section 4.9).
Three reference voltages are used throughout the signal path: the externally supplied REF IN $(1.225 \mathrm{~V})$, and the internally generated REF OUT MID ( 2.45 V ) and REF OUT HI (3.675V).

### 1.2 The CCD Clocking Signals

To maximize the flexibility of the LM9801, the CCD's $\phi 1$, $\phi 2$, RS, and TR pulses are internally generated, with a wide range of options, making these signals compatible with most commercial linear CCDs. In many cases, these output signals can drive the CCD clock inputs directly, with only series resistors (for slew rate control) between the LM9801's outputs and the CCD clock inputs.

### 1.3 The Digital Interface

There are three main sections to the digital interface of the LM9801: a serial interface to the Configuration Register, where all device programming is done, an 8 bit-wide input databus for gain correction coefficients with a synchronous clock output (CCLK), and an 8-bit output databus for the final pixel output data with a synchronous end of conversion output signal ( $\overline{\mathrm{EOC}}$ ) and an output enable input ( $\overline{\mathrm{RD}}$ ). Please note that the $\overline{\mathrm{CS}}$ input affects only the serial I/O-it has no effect on the output databus, input coefficient bus, or any other section of the LM9801.

### 2.0 DIGITAL INTERFACE

### 2.1 Reading and Writing to the Configuration Register

Communication with the Configuration Register is done through a standard MICROWIRETM serial interface. This interface is also compatible with the Motorola SPITM standard and is simple enough to easily be implemented in custom hardware if desired.
The serial interface timing is shown in Diagrams 13a-13b and Diagrams 15a-15d. Data is sent serially, LSB first. (Please note that some microcontrollers output data MSB first. When using these microcontrollers the bits in the configuration register are effectively reversed.) Input data is latched on the rising edge of SCLK, and output data changes on the falling edge of SCLK. $\overline{\mathrm{CS}}$ must be low to enable serial I/O.
If SCLK is only clocked when sending or receiving data from the LM9801, and held low at all other times, then $\overline{\mathrm{CS}}$ can be tied low permanently as shown in Diagrams 15a-15d. If SCLK is continuous, then $\overline{C S}$ must be used to determine the beginning and the end of a serial byte or word (see Diagrams 13a-13b). Note that CS must make its high-to-low and low-to-high transitions when SCLK is low, otherwise the internal bit counter may receive an erroneous pulse, causing an error in the write or read operation.
Data may be transmitted and received in two 8-bit bytes (typical with microcontroller interfaces) or one 16-bit word (for custom serial controllers).

## Applications Information (Continued)

The Configuration Register is programmed by sending a control byte to the serial port. This byte indicates whether this is a read or a write operation, and gives the 3 -bit address of the register bank to be read from or written to. If this is a read operation, the next 8 SCLKs will output the data at the requested location on the SDO pin. If this is a write operation, the data to be sent to the specified location should be clocked in on the SDI input during the next 8 SCLKs. Data is sent and received using the LSB (Least Significant Bit) first format.
For maximum system reliability, each configuration register location can be read back and verified after a write.
If the serial I/O to the configuration register falls out of sync for any reason, it can be reset by sending 8 or more SCLKs with $\overline{\text { CS }}$ held high.

### 2.2 Writing Correction Coefficient Data on the CD0-CD7 Bus

Correction coefficient data for each pixel is latched on the rising edge of the CCLK output signal (see Diagram 10). Note that there is a 3 pixel latency between when the coefficient data is latched and when the output data is available. As Diagram 2, Pixel Pipeline Timing Overview shows, coefficient data for pixel n is latched shortly before the output data for pixel $\mathrm{n}-2$ becomes available on the output databus (DD0-DD7). Note that there is no way to provide a correction coefficient for pixel 1 , the first pixel in the CCD array. This is not a problem since the first several pixels of the CCD are used for clamping.

### 2.3 Reading Output Data on the DD0-DD7 Bus

The corrected digital output data representing each pixel is available on the DDO-DD7 databus. The data is valid after the falling edge of the $\overline{E O C}$ output. The $\overline{\mathrm{RD}}$ input takes the databus in and out of TRI-STATE. $\overline{\mathrm{RD}}$ can be held low at all times if there are no other devices needing the bus, or it can be used to TRI-STATE the bus between pixels, allowing other devices access to the bus. Diagram 12, Data Timing (Output and Coefficient Data Sharing Same Bus), shows how EOC can be tied to $\overline{R D}$ to automatically multiplex between coefficient data and conversion data.

### 2.4 MCLK

This is the master clock input that controls the LM9801. The pixel conversion rate is fixed at $1 / 8$ of this frequency. Many of the timing parameters are also relative to the frequency of this clock.

### 2.5 SYNC

This input signals the beginning of a line. When SYNC goes high, the LM9801 generates a TR pulse, then begins converting pixels until the SYNC line is brought low again. Since there is no pixel counter in the LM9801, it will work with CCDs of any length.

### 3.0 DIGITAL CCD INTERFACE

### 3.1 Buffering $\phi 1, \phi 2$, RS, and TR

The LM9801 can drive the $\phi 1, \phi 2$, RS, and TR inputs of many CCDs directly, without the need for external buffers between the LM9801 and the CCD. Most linear CCDs designed for scanner applications require 0 V to 5 V signal swings into 20 pF to 500 pF input loading. Series resistors are typically inserted between the driver and the CCD to
control slew rate and isolate the driver from the large load capacitances. The values of these resistors are usually given in the CCD's datasheet.

### 4.0 ANALOG INTERFACE

### 4.1 Voltage Reference

The two REF IN pins should be connected to a $1.225 \mathrm{~V} \pm 2 \%$ reference voltage capable of sinking between 2 mA and 5 mA of current coming from the $500 \Omega-1400 \Omega$ resistor string between REF $\mathrm{OUT}_{\mathrm{HI}}$ and REF IN. The LM4041-1.2 1.225V bandgap reference is recommended for this application as shown in Figure 2. The inexpensive " $E$ " grade meets all the requirements of the application and is available in a TO-92 (LM4041EIZ-1.2) package as well as a SOT-23 package (LM4041EIM3-1.2) to minimize board space.
Due to the transient currents generated by the LM9801's ADC, PGA, and CDS circuitry, the REF IN pins, the REF OUT $_{\text {MID }}$ pin and the REF OUT ${ }_{H I}$ pin should all be bypassed to AGND with $0.1 \mu \mathrm{~F}$ monolithic capacitors


TL/H/12814-29
FIGURE 2. Voltage Reference Generation

### 4.2 Clamp Capacitor Selection

This section is very long because it is relatively complicated to explain, but the answer is short and simple: A clamp capacitor value of $0.01 \mu \mathrm{~F}$ should work in almost all applications. The rest of this section describes exactly how this value is selected.


TL/H/12814-30
FIGURE 3. OS Clamp Capacitor and Internal Clamp
The output signal of many CCDs rides on a large DC offset (typically 8 V to 10 V ) which is incompatible with the LM9801's 5V operation. To eliminate this offset without resorting to additional higher voltage components, the output

Applications Information (Continued)
of the CCD is AC coupled to the LM9801 through a DC blocking capacitor, $C_{\text {CLAMP }}$ (the CCD's DOS output is not used). The value of this capacitor is determined by the leakage current of the LM9801's OS input and the output impedance of the CCD. The leakage through the OS input determines how quickly the capacitor value will drift from the clamp value of REF OUTMID, which then determines how many pixels can be processed before the droop causes errors in the conversion ( $\pm 0.1 \mathrm{~V}$ is the recommended limit). The output impedance of the CCD determines how quickly the capacitor can be charged to the clamp value during the black reference period at the beginning of every line.
The minimum clamp capacitor value is determined by the maximum droop the LM9801 can tolerate while converting one CCD line. The following equation takes the maximum leakage current into the OS input, the maximum allowable droop ( 100 mV ), the number of pixels on the CCD, and the pixel conversion rate ( $\mathrm{f}_{\mathrm{MCLK}} / 8$ ) and provides the minimum clamp capacitor value:

$$
\begin{aligned}
\mathrm{C}_{\mathrm{CLAMP} \mathrm{MIN}} & =\frac{\mathrm{i}}{\mathrm{dV}} \mathrm{dt} \\
& =\frac{\text { leakage current }(\mathrm{A})}{\max \text { droop }(\mathrm{V})} \frac{\text { number of pixels }}{\text { conversion rate }(\mathrm{Hz})}
\end{aligned}
$$

For example, if the OS input leakage current is 20 nA worstcase, the CCD has 2700 active pixels, the conversion rate is 2.5 MHz ( $\mathrm{f}_{\mathrm{MCLK}}=20 \mathrm{MHz}$ ), and the max droop desired is 0.1 V , the minimum clamp capacitor value is:

$$
\begin{aligned}
\mathrm{C}_{\text {CLAMP MIN }} & =\frac{20 \mathrm{nA}}{0.1 \mathrm{~V}} \frac{2700}{2.5 \mathrm{MHz}} \\
& =216 \mathrm{pF}
\end{aligned}
$$

The maximum size of the clamp capacitor is determined by the amount of time available to charge it to the desired value during the optical black portion of the CCD output. The internal clamp is on for each pixel from the rising edge of the $\mathrm{S} / \mathrm{H}$ ref pulse to the falling edge of the $\mathrm{S} / \mathrm{H}$ signal pulse (see Diagrams 7 and 8). This time can be calculated using the values stored in the Sample Signal and Sample Reference configuration registers and the MCLK frequency. For normal CCDs:

$$
\mathrm{t}_{\mathrm{DARK}}(\mathrm{~s})=\frac{2+\mathrm{SS}-\mathrm{SR}}{2 \mathrm{f}_{\mathrm{MCLK}}(\mathrm{~Hz})}
$$

And for even/odd CCDs:

$$
\mathrm{t}_{\mathrm{DARK}}(\mathrm{~s})=\frac{18+\mathrm{SS}-\mathrm{SR}}{2 \mathrm{f}_{\mathrm{MCLK}}(\mathrm{~Hz})}
$$

Where SS is the value in the Sample Signal Position register ( $0-15$ ), SR is the value in the Sample Reference Position register $(0-14), f_{\text {MCLK }}$ is the MCLK frequency, and tDARK is the amount of time (per pixel) that the clamp is on.
The following equation takes the number of optical black pixels, the amount of time (per pixel) that the clamp is closed, the CCD's output impedance, and the desired accuracy of the final clamp voltage and provides the maximum clamp capacitor value that allows the clamp capacitor to settle to the desired accuracy within a single line:

$$
\begin{aligned}
\mathrm{C}_{\text {CLAMP MAX }} & =\frac{\mathrm{t}}{\mathrm{R}} \frac{1}{\ln (\text { accuracy })} \\
& =\frac{\mathrm{n}}{\mathrm{R}_{\text {OUT }}(\Omega)} \frac{t_{\text {DARK }}(\mathrm{s})}{\ln (\text { accuracy })}
\end{aligned}
$$

Where $\mathrm{n}=$ the number of optical black pixels, $\mathrm{t}_{\text {DARK }}$ is the amount of time (per pixel) that the clamp is on, ROUT is the output impedance of the CCD, and accuracy is the ratio of the worst-case initial capacitor voltage to the desired final capacitor voltage. For example, if a CCD has 18 black reference pixels, the output impedance of the CCD is $1500 \Omega$, the LM9801 is configured to clamp for 300 ns , the worst case initial voltage across the capacitor is 10 V , and the desired voltage after clamping is 0.1 V (accuracy $=10 / 0.1=100$ ), then:

$$
\begin{aligned}
\mathrm{C}_{\mathrm{CLAMP} \mathrm{MAX}} & =\frac{18}{1500 \Omega} \frac{300 \mathrm{~ns}}{\ln (100)} \\
& =514 \mathrm{pF}
\end{aligned}
$$

The final value for $\mathrm{C}_{\text {CLAMP }}$ should be less than or equal to CCLAMP MAX, but no less than C CLAMP MIN. A value of 470 pF will work in this example.
In some cases, depending primarily on the choice of CCD, $\mathrm{C}_{\text {CLAMP }}$ MAX may actually be less than the CLLAMP MIN, meaning that the capacitor cannot be charged $^{\text {Che }}$ to its final voltage during the black pixels at the beginning of a line and hold its voltage without drooping for the duration of that line. This is usually not a problem because in most applications the CCD is clocked continuously as soon as power is applied. In this case, a larger capacitor can be used (guaranteeing that the $\mathrm{C}_{\text {CLAMP }}$ MIN requirement is met), and the final clamp voltage is forced across the capacitor over multiple lines. This equation calculates how many lines are required before the capacitor settles to the desired accuracy:

$$
\text { lines }=\left(\frac{R_{\text {OUT }}}{n} \frac{C_{\text {CLAMP }}}{t_{\text {DARK }}}\right) \ln \left(\frac{\text { Initial Voltage }}{\text { Final Voltage }}\right)
$$

Using the values shown before and a clamp capacitor value of $0.01 \mu \mathrm{~F}$, this works out to be:

$$
\text { lines }=\left(\frac{1500 \Omega}{18} \frac{0.01 \mu \mathrm{~F}}{300 \mathrm{~ns}}\right) \ln \left(\frac{10 \mathrm{~V}}{0.1 \mathrm{~V}}\right)=12.8 \text { lines }
$$

At a 2.5 MHz conversion rate, this is about 14 ms .
In this example a $0.01 \mu \mathrm{~F}$ capacitor takes 14 ms after pow-er-up to charge to its final value, but its droop across all subsequent lines is now less than 2 mV (using the previous example's values). This wide margin is the reason a C ${ }_{C L A M P}$ value of $0.01 \mu \mathrm{~F}$ will work in most applications.

### 4.3 VGA

The LM9801 has a VGA (Variable Gain Amplifier) that can be used to increase the amplitude of the CCD signal prior to sampling, correction, and digitization. The gain of the VGA is 0 dB to 9 dB and is determined by the codes in the 4-bit VGA Gain register, as given by the equation:

$$
\text { Gain }_{V G A}(\mathrm{~dB})=\frac{\text { VGA code }}{16} 9.55
$$

This gain may be changed at the line rate (not the pixel rate) by writing to the configuration register. You can write to the configuration register to change the gain at any time, but if you write during a line, the remaining pixels of that line may be corrupted. It is best to change the gain after all active pixels have been read out or while SYNC is low.

## Applications Information (Continued)

### 4.4 Correlated Double Sampler (CDS)

Figure 4 shows the output stage of a typical CCD and the resulting output waveform:


## FIGURE 4. CDS

Capacitor C1 converts the electrons coming from the CCD's shift register to an analog voltage. The source follower output stage (Q2) buffers this voltage before it leaves the CCD. Q1 resets the voltage across capacitor C1 in between every pixel at intervals 2 and 5 . When Q1 is on, the output signal (OS) is at its maximum. After Q1 turns off (period 3), the OS level represents the residual voltage across C1 ( $\mathrm{V}_{\text {RESIDUAL }}$ ). $\mathrm{V}_{\text {RESIDUAL }}$ includes charge injection from Q1, thermal noise from the ON resistance of Q1, and other sources of error. When the shift register clock ( $\phi 1$ ) makes a low to high transition (period 4), the electrons from the next pixel flow into C 1 . The charge across C1 now contains the voltage proportional to the number of electrons plus $V_{\text {RESIDUAL }}$, an error term. If $O S$ is sampled at the end of period 3 and that voltage is subtracted from the OS at the end of period 4, the $\mathrm{V}_{\text {RESIDUAL }}$ term is canceled and the noise on the signal is reduced. ( $\left[\mathrm{V}_{\text {SIGNAL }}+\mathrm{V}_{\text {RESIDUAL }}\right]$ $-\mathrm{V}_{\text {RESIDUAL }}=\mathrm{V}_{\text {SIGNAL }}$ ). This is the principal of Correlated Double Sampling.
The LM9801 implements CDS with two switched-capacitor S/H amplifiers. The S/Hs acquire a signal within a 50 ns window which can be placed anywhere in the pixel period with 25 ns precision. See Diagrams 7 and 8 for more detailed timing information.

### 4.5 CIS Mode

The LM9801 provides some support for CIS (Contact Image Sensor) devices by offering a sampling mode for capturing positive going signals, as opposed to the CCD's negative going signal.


FIGURE 5. CIS vs CCD Output Signals
While CIS devices do not usually have a reference level with which to perform correlated double sampling, many have a very repeatable reset level which can be used as a black reference allowing the LM9801 to perform pseudo CDS on the signal. When the Signal Polarity bit is set to a zero, the LM9801 expects a positive going signal, typically from a CIS device. When the Signal Polarity bit is set to a one, the LM9801 expects a negative going signal, typically from a CCD sensor.

### 4.6 Offset DAC

The 4 bit plus sign Offset DAC is used to compensate for DC offsets due to the correlated double sampling stage. The offset can be corrected in 31 steps of 0.42 ADC LSB size between -6.3 and +6.3 LSBs. Note that the DAC comes betore the PGA, so any offset errors at this stage are multiplied by the gain of the PGA. The calibration procedure described in Section 5.0 demonstrates how to use the DAC to eliminate offset errors before scanning begins.
Note that this DAC is programmed during LM9801 calibration/configuration and is not meant to compensate for pixel-to-pixel CCD offset errors. CDS cancels the pixel-rate offset errors.

### 4.7 Programmable Gain Amplifier (PGA)

The PGA provides 8 bits of pixel-to-pixel gain correction over a 0 dB to $9 \mathrm{~dB}(\mathrm{x} 1$ to x 3 ) range. After the input signal is sampled and held by the CDS stage, it is amplified by the gain indicated by the data ("PGA Code") on the CD0-CD7 databus using the formula:

$$
\text { Gain }\left(\frac{V}{V}\right)=1+\frac{\text { PGA code }}{256} 1.95
$$

### 4.8 Offset Add Bit

In addition to the Offset DAC, there is a bit in the configuration register which, when set, adds a positive 2 LSB offset at the output of the PGA. This offset ensures that any offset between the output of the PGA and the ADC is positive, so that no dark level information is lost due to negative offsets. The calibration procedure described in Section 5.0 demonstrates how to set this bit.

## Applications Information (Continued)

### 4.9 ADC

The ADC converts the normalized analog output signal to an 8 -bit digital code. The $\overline{\mathrm{EOC}}$ output goes from high to low to indicate that a new conversion is ready. ADC data can be latched by external memory on the rising edge of EOC. The $\overline{\mathrm{RD}}$ input takes the ADC's output buffer in and out of TRI-STATE. $\overline{R D}$ may be tied to $\overline{E O C}$ in many applications, putting the data on the bus only when EOC is low, and allowing other data on the bus (such as CDO-CD7 correction data) at other times. In this way the output data and correction coefficient data can share the same databus (see Diagram 12).

### 5.0 CALIBRATION

Calibration of a CCD scanner is done to normalize the pixels of a linear CCD so that each pixel produces the same digital output code at the output of the scanner when presented with the same image light intensity. This intensity ranges from black (no light) to white (maximum light intensity). The CCD's analog output may have large pixel-to-pixel DC offsets (corresponding to errors on black signals) and pixel-topixel variations in their output voltage given the same white image (corresponding to errors on brighter signals). If these offsets are subtracted from each pixel, and each pixel is given its own gain setting to correct for different efficiencies, then these errors can be eliminated.
Ideally the digital output code for any pixel would be zero for a black image, and some code near fullscale for an image with maximum brightness. For an 8 -bit system like the LM9801, that code might be 250. This code will be called the Target Code.
The LM9801 eliminates these global and pixel-to-pixel offset and gain errors with its Correlated Double Sampling (CDS), Offset DACs, Variable Gain Amplifier, and pixel-rate Programmable Gain Amplifier. This section describes how to program the LM9801 and the coefficient RAM being used with it to eliminate these errors.
Calibration of a LM9801-based system requires 3 steps. The first, described in Section 5.1, Offset Calibration, takes a black image and normalizes the digital output code for each pixel to a code at or near 0 .
The second step, Section 5.2, Coarse Gain (VGA) Calibration, finds the optimum gain setting that places the output voltage of all the pixels within the 9 dB adjustment range of the PGA.
The final step, described in Section 5.3, PGA Correction Coefficients (Shading Calibration), describes how to calculate the gain required to normalize the output of each pixel to the desired output code (the Target code).

### 5.1 Offset Calibration

This procedure corrects for static offsets generated by the CCD and the LM9801. Because the LM9801 uses CDS to eliminate the pixel-to-pixel offset errors of the CCD, no pix-el-rate offset correction is required.
To use the Offset DAC and Offset Add bit for offset correction, the offset errors ( $\mathrm{V}_{\mathrm{OS} 1}$ and $\mathrm{V}_{\mathrm{OS} 2}$ ) must first be determined, as shown in Figure 6. This is done be measuring the voltage at the PGA output, using the ADC with a black image on the CCD (a black image can usually be created sim-


FIGURE 6. Offset Calibration
ply by turning off the scanner's illumination). If this voltage is known with a PGA gain of $1.00 \mathrm{~V} / \mathrm{V}(0 \mathrm{~dB})$ and $2.95 \mathrm{~V} / \mathrm{V}$ ( 9 dB ), then the offset errors ( $\mathrm{V}_{\mathrm{OS} 1}$ and $\mathrm{V}_{\mathrm{OS} 2}$ ) can be determined from the following two equations:

$$
\begin{aligned}
\mathrm{V}_{\mathrm{ADC} 1}= & 1\left(\mathrm{~V}_{\mathrm{OS} 1}+\mathrm{V}_{\mathrm{DAC} 1}\right)+\mathrm{V}_{\mathrm{OS} 2}+\mathrm{V}_{\mathrm{DAC} 2} \\
& (P G A \text { gain }=1) \\
\mathrm{V}_{\mathrm{ADC} 2}= & 2.95\left(\mathrm{~V}_{\mathrm{OS} 1}+\mathrm{V}_{\mathrm{DAC} 1}\right)+\mathrm{V}_{\mathrm{OS} 2}+\mathrm{V}_{\mathrm{DAC} 2} \\
& (P G A \text { gain }=2.95)
\end{aligned}
$$

Solving for $\mathrm{V}_{\mathrm{OS} 1}$ and $\mathrm{V}_{\mathrm{OS} 2}$ :

$$
\mathrm{V}_{\mathrm{OS} 1}=\left(\mathrm{V}_{\mathrm{ADC} 2}-\mathrm{V}_{\mathrm{ADC} 1}\right) / 1.95-\mathrm{V}_{\mathrm{DAC} 1}
$$

$$
\mathrm{V}_{\mathrm{OS} 2}=\left(2.95 \mathrm{~V}_{\mathrm{ADC} 1}-\mathrm{V}_{\mathrm{ADC} 2}\right) / 1.95-\mathrm{V}_{\mathrm{DAC} 2}
$$

These equations were used to produce this procedure for cancelling the LM9801's offset errors. Please note that all voltages and measurements are in units of ADC LSBs to simplify calibration.

1. Set the VGA Gain to $1 \mathrm{~V} / \mathrm{V}$ (VGA code $=0$ LSBs).
2. Set the Offset DAC $\left(V_{D A C 1}\right)$ to its maximum value ( +6.3 LSBs) to ensure the total offset is positive and therefore measurable by the ADC.
3. Set the Offset Add bit ( $V_{D A C 2}$ ) to 0 .
4. Set the PGA Gain to $1 \mathrm{~V} / \mathrm{V}(\mathrm{PGA}$ code $=0)$.
5. Digitize a black line.
6. Calculate the average (in ADC LSBs) of all the valid pixels in the black line and store that number as $\mathrm{V}_{\mathrm{ADC}} 1$.
7. Set the PGA Gain to $2.95 \mathrm{~V} / \mathrm{V}(\mathrm{PGA}$ code $=255)$.
8. Digitize a black line.
9. Calculate the average (in ADC LSBs) of all the valid pixels in the black line and store that number as $\mathrm{V}_{\text {ADC2 }}$.
10. Calculate $\mathrm{V}_{\mathrm{OS} 1}$ :
$\mathrm{V}_{\mathrm{OS} 1}=\left(\mathrm{V}_{\mathrm{ADC} 2}-\mathrm{V}_{\mathrm{ADC} 1}\right) / 1.95-6.3$
11. Program the Offset DAC register using the formula:

Offset DAC code $=-\left(\mathrm{V}_{\mathrm{OS} 1}\right)(15 / 6.3)$
$=\left(6.3+\left(\mathrm{V}_{\mathrm{ADC} 1}-\mathrm{V}_{\mathrm{ADC} 2}\right) / 1.95\right)(15 / 6.3)$
$=15+1.22\left(\mathrm{~V}_{\mathrm{ADC} 1}-\mathrm{V}_{\mathrm{ADC} 2}\right)$
(Note: This calculation can be done as
$15+39\left(\mathrm{~V}_{\mathrm{ADC} 1}-\mathrm{V}_{\mathrm{ADC} 2}\right) / 32$
for ease of programming in 8-bit microcontrollers)
12. If $3 \mathrm{~V}_{\mathrm{ADC} 1}>\mathrm{V}_{\mathrm{ADC} 2}$, then set the Offset Add bit to 0 . If $3 \mathrm{~V}_{\mathrm{ADC} 1}<\mathrm{V}_{\text {ADC2 }}$, set the Offset Add bit to 1 .
13. The final value of the offset present at the ADC input can be used for the shading calibration calculations. Calculate the final value of the ADC input offset (VOFFSET) using:

$$
\begin{aligned}
V_{\text {OFFSET }}= & \left(3 V_{\text {ADC1 }}-\mathrm{V}_{\text {ADC2 }}\right) / 2 \\
& \text { (if the Offset Add bit is } 0), \text { or } \\
V_{\text {OFFSET }}= & \left(3 V_{\text {ADC1 }}-\mathrm{V}_{\text {ADC2 }}\right) / 2+2 \\
& \text { (if the Offset Add bit is } 1)
\end{aligned}
$$

## Applications Information (Continued)

### 5.2 Coarse Gain Calibration

The LM9801's PGA corrects for up to 9 dB of varlation in the CCD output signal's white level intensity. That 9 dB range has to be centered inside the 9 dB window of correction as shown in Figure 7. The window's upper limit is determined by the Target code, and the lower limit by the Target code divided by 2.8 (this corresponds to the minimum gain range of the PGA). To allow proper calibration, the amplitude of all the pixels in the CCD should be inside this range when those pixels are scanning an image corresponding to the Target code. The placement of the pixels inside the 9 dB window can be controlled by any of three ways: changing the gain of the VGA, changing the integration time of the CCD, or changing the intensity of the light source.
In most designs, the output waveform of the CCD can be brought into the 9 dB correction range of the PGA by adjusting the gain of the VGA. This is the next step in system calibration.


TL/H/12814-34
FIGURE 7. CCD Input Signal In Range
Figure 8 is a flowchart of one technique to find the optimum VGA gain setting during calibration. Calibration begins with a VGA gain setting of $1 \mathrm{~V} / \mathrm{V}$ and increments the VGA gain until one of the four possible results occur. Result 1 is the desired outcome, where the signal falls into the range shown in Figure 7 and the VGA calibration has been successful.


FIGURE 8. VGA Calibration Flowchart

## Applications Information (Continued)

There are several conditions that can cause the VGA gain calibration routine to fail. Result 2, "Signal is too strong: Decrease light intensity or integration time" is shown in Figure 9. This condition indicates that the amplitude of one or more of the white pixels coming from the CCD is greater than the maximum input voltage that the LM9801 is capable of accepting (about $1.2 \mathrm{Vp}-\mathrm{p}$ ). In this case the amplitude of the analog CCD output must be reduced before it enters the LM9801's OS input to prevent clipping. This can be done by reducing the intensity of the light source or shortening the integration time of the CCD.


FIGURE 9. CCD Input Signal Too Strong
The second possible failure mode of the VGA calibration (Result 3) occurs if there is "Too much variation" in the amplitude of the pixels coming from the CCD (Figure 10). The LM9801 can correct for up to a 2.8 to 1 variation in pixel amplitude. If the variation is greater than this than it must be reduced before it can perform shading correction on all the pixels. Typically this is done by using a better light source that has more uniform illumination, higher quality lenses, or other opto-mechanical techniques to reduce variation across all the active pixels.


TL/H/12814-37
FIGURE 10. CCD Input Signal Range Too Wide


TL/H/12814-38
FIGURE 11. CCD Input Signal Too Weak

The final problem that can occur during VGA calibration (Result 4) is the "Signal too weak: increase light intensity or integration time" condition, shown in Figure 11. In this case, even with the VGA gain set to a maximum of 2.8 , the amplitude of one or more pixels is less than the minimum required for shading correction. The solution is to increase the intensity of the light source or lengthen the integration time of the CCD to increase the CCD's output amplitude.
To ensure that a scanner system is manufacturable, the result of the VGA calibration must always be State 1 . States 2 , 3 , and 4 must be eliminated either by ensuring that the total variation in light intensity (from all sources) from system to system to a maximum of 9 dB , or by being able to adjust the light source's intensity and/or the CCD's light integration time.

### 5.3 PGA Correction Coefficients (Shading Calibration)

Once the input signal has been centered inside the range the LM9801 can correct for, correction coefficients must be generated for each pixel to compensate for the gain error of that pixel.

1. Set Offset DAC and Add Bit as determined in Section 5.1.
2. Set the VGA gain to the value determined in Section 5.2.
3. Set the PGA gain to 0 dB .
4. Scan a reference line corresponding to all white or light grey and store it in memory.
5. Calculate the required gain correction coefficients for each pixel using the formula:
Correction Coefficient $_{\mathrm{n}}=\frac{256}{1.95}\left(\frac{\text { Target Code }}{\text { Uncorrected Code }} \mathrm{n}\right.$ -1$)$
Where Uncorrected Code $\mathbf{n}_{\mathbf{n}}$ is the ADC output code for pixel $n$ with the PGA gain $=0 \mathrm{~dB}$, Target Code is the number that corresponds to the desired output from the ADC with the given reference line input, and Correction Coefficient ${ }_{n}$ is the gain correction number that is sent to the CDO-CD7 correction databus to provide gain correction for pixel $n$ when digitizing a line with the LM9801's PGA gain correction operating.
If it is difficult or undesirable to do the division, subtraction, and multiplication operations shown above for every pixel, then a lookup table can be generated in advance that will return the Correction Coefficient for any Uncorrected Code. This table can be stored in ROM or RAM and can speed up the calibration process. The disadvantage of this technique is that the Target Code must be fixed when the table is generated, so only one Target Code can be used (unless multiple tables are generated).
All the Correction Coefficients must be stored and sent to the LM9801 through the CD0-CD7 databus for every line scanned.

## Applications Information (Continued)

### 6.0 POWER SUPPLY CONSIDERATIONS

### 6.1 General

The LM9801 should be powered by a single +5 V source (unless 3 V -compatible digital I/O is required-see Section 6.2). The analog supplies $\left(\mathrm{V}_{\mathrm{A}}\right)$ and the digital supplies ( $\mathrm{V}_{\mathrm{D}}$ and $\mathrm{V}_{\mathrm{D}(\mathrm{I} / \mathrm{O})}$ ) are brought out individually to allow separate bypassing for each supply input. They should not be powered by two or more different supplies.
In systems with separate analog and digital +5 V supplies, all the supply pins of the LM9801 should be powered by the analog +5 V supply. Each supply input should be bypassed to its respective ground with a $0.1 \mu \mathrm{~F}$ capacitor located as close as possible to the supply input pin. A single $10 \mu \mathrm{~F}$ tantalum capacitor should be placed near the $\mathrm{V}_{\mathrm{A}}$ supply pin to provide low frequency bypassing.
To minimize noise, keep the LM9801 and all analog components as far as possible from noise generators, such as switching power supplies and high frequency digital busses. If possible, isolate all the analog components and signals (OS, reference inputs and outputs, $\mathrm{V}_{\mathrm{A}}, \mathrm{AGND}$ ) on an analog ground plane, separate from the digital ground plane. The two ground planes should be tied together at a single point, preferably the point where the power supply enters the PCB.

### 6.2 3V Compatible Digital I/O

If 3 V digital I/O operation is desired, the $\mathrm{V}_{\mathrm{D}(\mathrm{I} / \mathrm{O})}$ pin may be powered by a separate $3 \mathrm{~V} \pm 10 \%$ or $3.3 \mathrm{~V} \pm 10 \%$ supply. In this case, all the digital I/O pins (CDO-CD7, CCLK, MCLK, DDO-DD7, $\bar{E} O C, \overline{R D}$, SYNC, $\overline{C S}$, SCLK, SDO, and SDI) will be 3 V compatible. The CCD clock signals ( $\phi 1, \phi 2$, $R S$, and TR) remain 5 V outputs, powered by $\mathrm{V}_{\mathrm{D}}$. In this case the $\mathrm{V}_{\mathrm{D}(I / O)}$ input should be bypassed to $\mathrm{DGND}_{(I / O)}$ with a parallel combination of a $0.1 \mu \mathrm{~F}$ capacitor and a $10 \mu \mathrm{~F}$ tantalum capacitor.

### 6.3 Power Down Mode

Setting the Power Down bit to a " 1 " puts the device in a low power standby mode. The CCD outputs ( $\phi 1, \phi 2$, RS, and TR) are pulled low and the analog sections are turned off to conserve power. The digital logic will continue to operate if MCLK continues and SYNC is held high, so for minimum power dissipation MCLK should be stopped when the LM9801 enters the Power Down mode. Recovery from Power Down typically takes $50 \mu$ s (the time required for the reference voltages to settle to 0.5 LSB accuracy).

### 7.0 COLOR

There are two primary ways to use the LM9801 in a color system with a triple output (RGB) CCD. The first is to use one LM9801 with an external multiplexer. This is the simplest solution. The second technique is to use one LM9801 per RGB color.

### 7.1 Parallel Output CCD, One LM9801

Figure 12 is an example of how to use a single LM9801 with a triple-output RGB CCD. In this case an entire line of red is digitized, followed by an entire line of green, then blue. This solution provides a $2.5 \mathrm{Mpixels} / \mathrm{sec}$ (for an effective 830k RGB pixels/sec after de-interleaving) pixel rate using a high performance triple output color CCD.
The Mux 1 multiplexer, located between the CCD's OS outputs and the LM9801's OS input, selects the color to be digitized according to the states of the A and B inputs (described below). The multiplexer's speed requirements are minimal because the mux switches at the line rate, not the pixel rate. Also, since the output of the mux goes into a high impedance, low-capacitance input, the ON resistance of the mux is not critical. The 74 HC 4052 is a good choice for this application.


FIGURE 12. Parallel Output CCD Application Circuit

## Applications Information (Continued)



FIGURE 13. Parallel Output CCD Timing

To maximize the integration time for the Red, Green, and Blue photodiodes, the transfer (TR) pulses should be staggered as shown in Figure 13. This is done by a demultiplexer (Mux 2) between the TR output of the LM9801 and the transfer gate inputs of the CCD. If the CCD's transfer gate input capacitance is relatively low (see the CCD datasheet for this specification and the requirements for TR pulse rise and fall time), then the other half of the 74 HC 4052 may be used to switch the TR pulses as shown. If the TR gate input capacitance is so large that the minimum TR rise and fall times can not be met because of the $200 \Omega$ max on resistance of the 74 HC 4052 's switches, then the 74 HC 4052 can not be used to multiplex the TR output and should be replaced with an active device such as the 74 HC 155 dual 2 -to-4 demultiplexer.
Two signals ( $A$ and $B$ ) must be generated to choose which color is going to be digitized and receives the TR pulse. These signals can be as simple as the output of a two bit counter that counts from 0 to $2(0,1,2,0,1,2$, etc.). This counter should be incremented after the end of the previous line and before the first transfer pulse of the next line. Also, since each color will need a different VGA gain, the appropriate VGA gain value for each color should be sent to the LM9801 during this time.

### 7.2 Parallel Output CCD, Three LM9801s

Figure 14 uses three LM9801s to achieve a 7.5 Mpixel/sec (2.5M RGB pixels/sec) pixel rate. The three LM9801s are synchronized by applying the same MCLK and SYNC signals to all three devices. One LM9801 provides the clock signals required for the CCD. Since the coefficient data for all three LM9801s will be latched simultaneously on the rising edge of CCLK, the correction coefficient bus must either be at least 24 bits wide ( 8 correction coefficient bits by 3 LM9801s) or run at a 7.5 MHz rate and be latched into a buffer between the correction coefficient databus and each LM9801. Similarly, the output data for all three LM9801s will be available simultaneously at the 3 output databusses. Since each LM9801 is dedicated to one color, the VGA gain does not change during line scan.


TL/H/12814-41
FIGURE 14. Parallel Output CCD, Three LM9801

## Applications Information (Continued)

### 8.0 A TYPICAL GREYSCALE APPLICATION

Figure 15 shows the interface between the LM9801 and a typical greyscale even/odd output CCD, the TCD1250. The interface for most other CCDs will be similar, the only difference being the values for the series resistors (if required).
The clamp capacitor value is determined as shown in Section 4.2. The resistor values are usually given in the CCD's datasheet. If the datasheet's requirement is given as a particular rise/fall time, the resistor can be chosen using the graph of $\phi 1, \phi 2$, RS and TR Rise Times Through a Series Resistance vs Load Capacitance graph in the Typical Performance Characteristics section. Given the required rise time and the input capacitance of the input being driven, the resistor value can be estimated from the graph.


FIGURE 15. Greyscale CCD Interface Example
These are the Configuration Register parameters recommended for use as a starting point for most even/odd CCDs:

Mode $=1$ (Even/Odd mode)*
RS Pulse Width $=0$ (1 MCLK)
RS Pulse Polarity $=0$ *
RS Pulse Position $=10$
Sample Reference Position $=14$
Sample Signal Position $=8$
$\phi 1 / \phi 2 /$ RS/TR Enable $=1 / 1 / 1 / 1$
TR Pulse Width $=0$
TR- $\phi 1$ Guardband $=0$
TR Polarity $=0$ *
Signal Polarity $=1$
Dummy Pixels $=2^{*}$
Optical Black Pixels $=5^{*}$
(*Value given in CCD datasheet)

The Mode is set to Even/Odd, RS Pulse Width is set to its minimum value, and RS polarity is positive. The timing, shown in Figure 16, is determined by the RS, SR, and SS registers. The RS pulse position (RS) is set to 10, dividing the pixel period so that the signal portion is available for the first 5 MCLKs following a $\phi 1$ clock edge and the black reference portion appears during the last 2 MCLKs (following the 1 MCLK wide reset pulse). Sample Reference (SR) is set to 14 , so it samples the black reference just before the next $\phi 1$ clock edge. Sample Signal (SS) is set to 8 , so it samples the black reference just before the next reset pulse. These values can be adjusted to account for differences in CCDs, CCD data delays, settling time, etc., but this is often not necessary.


TL/H/12814-43
FIGURE 16. Typical Even/Odd Timing
All 4 digital outputs ( $\phi 1, \phi 2$, RS, and TR) are enabled. The TR pulse width is set to the minimum, 20 MCLKs, as is the guardband between $\phi 1$ and TR. Either of these settings can be increased if necessary.
The TR polarity is positive, as is the RS polarity. Some CCDs may require one or both of these signals to be inverted, in which case the corresponding bit can be set to a " 1 ". If there is an inverting buffer between the LM9801 and the CCD, these bits may be used to correct the output polarity at the CCD. Note that if $\phi 1$ and $\phi 2$ are inverted, then $\overline{\phi 2}$ should be used as $\phi 1$ at the CCD, and $\overline{\phi 1}$ should be used as $\phi 2$ at the CCD (Figure 17).


TL/H/12814-44
FIGURE 17. $\phi 1$ and $\phi \mathbf{2}$ After Inversion
Since this is a CCD sensor, the Signal Polarity is set to a 1 (inverted) to match the CCD's output signal. The number of dummy pixels and optical black reference pixels are given in the CCD's datasheet. The dummy pixel register should be programmed with the number of dummy pixels in the CCD +1 (for example, if the CCD has 16 dummy pixels then the register should contain 17). The optical black reference register should be programmed with the number of optical black pixels in the CCD.

## Applications Information (Continued)

The PGA gain coefficient register and PGA Gain Source bit are used during calibration (see Section 5.0). The Power Down bit should be set to 0 for normal operation. The Offset Add bit is also programmed during calibration.
The VGA and Offset DAC bits are programmed during calibration (Section 5.0). The Test Mode bits should always be set to " 0 ".

### 9.0 TYPICAL CIS APPLICATION

Many CIS sensors (such as those made by Dyna Image Corporation) have only one clock input, a transfer signal, and an output signal that is referred to ground (Figure 18). Figure 19 shows the analog and digital circuitry required to connect a typical Dyna CIS to the LM9801.


TL/H/12814-46
FIGURE 19. Minimum CIS Interface
Because the CIS requires only one clock with a duty cycle of less than $50 \%$, the LM9801's RS output is used as the CIS's CLK source. $\phi 1$ and $\phi 2$ are not used. The $74 \mathrm{HC74}$ D flip-flop is used to lengthen the transfer pulse (SI, or "Shift In" on the CIS) so that it overlaps the first RS pulse and meets the timing requirement of the CIS (see Figure 20).

The final "trick" required to interface a CIS to the LM9801 is the generation of optical black pixels for the LM9801 to clamp to at the beginning of a line. Unlike CCDs, CIS devices do not have a sequence of optical black pixels at the beginning of a line-the first pixel out of a CIS is valid image data. There are several ways to create black pixels for the LM9801 to clamp to.


FIGURE 20. CIS Interface Digital Timing
The simplest solution is to physically place a light shield (black plastic, tape or metal) over the first 10 or so pixels. This reduces the voltage output of the CIS to nearly 0 V , which is adequate for the LM9801 to clamp to. This has the side effect of slightly reducing the number of active pixels available for image capture.
A second option is to artifically generate "black" pixels by holding the CLOCK input high for 10 or so RS pulses (Figure 21). This forces the output voltage to zero for the time that the CLOCK input is high, and only one active image pixel is lost. The BLACK signal could be generated by the ASIC/external logic that generates a pulse on the first rising edge of RS after the TR pulse.


FIGURE 21. Generating Artificial Black Pixels

## Applications Information (Continued)

Suggested timing for CIS devices is:
Mode $=0$ (Standard Mode)*
RS Pulse Width $=0$ (2 MCLKs)
RS Pulse Polarity $=0$ (or 1 if circuit of Figure 21 is
used)*
RS Pulse Position $=0$
Sample Reference Position $=2$
Sample Signal Position $=14$
$\phi 1 / \phi 2 /$ RS/TR Enable $=0 / 0 / 1 / 1$
TR Pulse Width $=0$
TR- $\phi 1$ Guardband $=0$
TR Polarity $=1^{*}$
Signal Polarity $=0$
Dummy Pixels $=2$
Optical Black Pixels $=10$
(*Value given in CCD datasheet)
As CIS sensors approach pixel rates of 1 MHz and above (corresponding to MCLK frequencies of 8 MHz and above), the voltage during the reset level becomes less stable, making it difficult to perform CDS on the output (Figure 22). The solution is to create the ground reference externally, shorting the LM9801's input to ground for half of the time using the $\phi 1$ clock, as shown in Figure 23.


TL/H/12814-49
FIGURE 22. High Speed CIS Waveforms


TL/H/12814-50
FIGURE 23. High Speed CIS Interface

### 10.0 HINTS AND COMMON SYSTEM DESIGN PROBLEMS

10.1 Reading and Writing to the Configuration Register

The Configuration Register sends and receives data LSB (Least Significant Byte) first. Some microcontrollers send out data MSB (Most Significant Byte) first. The order of the bits must be reversed to when using these microcontrollers. Note: Unlike the LM9800, the SYNC pin does not have to be held high to send or receive data to or from the Configuration Register.

### 10.2 Setting the Dummy and Optical Black Pixel

 RegistersThe minimum value in the Dummy Pixels register is 2 (a value of 0 or 1 will cause errors in the EOC and CCLK timing). Note that the value in this register should be equal to 1 plus the actual number of dummy pixels in the CCD. For example, if the CCD being used with the LM9801 has 12 dummy pixels, this register should be set to 13. The minimum number in the Optical Black Pixels register is 1.

### 10.3 Stretching the TR- $\phi 1$ Guardband

Some CCDs (Sony's ILX514, ILX518, and ILX524, for example) require a TR to $\phi 1$ guardband greater than the 100 ns (2 MCLKs) provided by the LM9801. The circuit shown in Figure 24 produces a $1 \mu \mathrm{~s} \phi$ ROG (transfer) pulse with a guardband between the end of the $\phi$ ROG pulse and the next edge of $\phi 1$. This is done by setting the LM9801's TR pulse width register to $2 \mu \mathrm{~s}$ and using the 74 HC 4538 to generate a $1 \mu$ s pulse inside that TR period to send to the CCD.


FIGURE 24. Stretching the TR- $\phi 1$ Guardband


Physical Dimensions inches (millimeters) unless otherwise noted


52-Pin Plastic Leaded Chip Carrier (PLCC)
Order Number LM9801CCV
NS Package Number V52A
LM9801 8-Bit Greyscale/24-Bit Color Linear CCD Sensor Processor

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)


52-Pin Thin Quad Flatpak Order Number LM9801CCVF NS Package Number VEG52A

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| :---: | :---: | :---: | :---: |

# Temperature Sensors 

- LM50 SOT23, Single Supply, Centigrade Temperature Sensor
- LM56 Dual Output Low Power Thermostat
- LM60 2.7V, SOT23, Single Supply, Centigrade Temperature Sensor
- LM75 Digital Temperature Sensor and Thermal Watchdog with Two-Wire Interface


| Absolute Maximum Ratings (Note 1$)$ |  |
| :--- | ---: |
| Supply Voltage | +12 V to -0.2 V |
| Output Voltage | $\left(+\mathrm{V}_{\mathrm{S}}+0.6 \mathrm{~V}\right)$ to -1.0 V |
| Output Current | 10 mA |
| Storage Temperature | $-65^{\circ} \mathrm{C}$ to $+150^{\circ} \mathrm{C}$ |
| Lead Temperature |  |
| SOT Package (Note 2): |  |
| Vapor Phase ( 60 seconds) |  |
| Infrared (15 seconds) | $215^{\circ} \mathrm{C}$ |
| TJMAX, Maximum Junction Temperature | $220^{\circ} \mathrm{C}$ |


| ESD Susceptibility (Note 3): |  |
| :--- | ---: |
| Human Body Model | 2000 V |
| Machine Model | 200 V |

Operating Ratings (Note 1)

| Specified Temperature Range: | $\mathrm{T}_{\text {MIN }}$ to $\mathrm{T}_{\text {MAX }}$ |
| :--- | ---: |
| LM50C | $-40^{\circ} \mathrm{C}$ to $+125^{\circ} \mathrm{C}$ |
| LM50B | $-25^{\circ} \mathrm{C}$ to $+100^{\circ} \mathrm{C}$ |
| Operating Temperature Range | $-40^{\circ} \mathrm{C}$ to $+150^{\circ} \mathrm{C}$ |
| $\theta_{\text {JA }}$ (Note 4) | $450^{\circ} \mathrm{C} / \mathrm{W}$ |
| Supply Voltage Range $\left(+\mathrm{V}_{\mathrm{S}}\right)$ | +4.5 V to +10 V |

Electrical Characteristics Unless otherwise noted, these specifications apply for $\mathrm{V}_{S}=+5 \mathrm{~V}_{\mathrm{DC}}$ and $\mathrm{I}_{\mathrm{LOAD}}=$ $+0.5 \mu \mathrm{~A}$, in the circuit of Figure 1. Boldface limits apply for the specified $\mathbf{T}_{\mathbf{A}}=\mathbf{T}_{\mathbf{J}}=\mathbf{T}_{\mathbf{M I N}}$ to $\mathbf{T}_{\text {MAX }}$; all other limits $\mathrm{T}_{\mathbf{A}}$ $=\mathrm{T}_{\mathrm{J}}=+25^{\circ} \mathrm{C}$, unless otherwise noted.

| Parameter | Conditions | LM50B |  | LM50C |  | Units (Limit) |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | Typical | Limit (Note 5) | Typical | Limit (Note 5) |  |
| Accuracy <br> (Note 6) | $\begin{aligned} & \mathrm{T}_{\mathrm{A}}=+25^{\circ} \mathrm{C} \\ & \mathrm{~T}_{\mathrm{A}}=\mathrm{T}_{\mathrm{MAX}} \\ & \mathrm{~T}_{\mathrm{A}}=\mathrm{T}_{\mathrm{MIN}} \\ & \hline \end{aligned}$ |  | $\begin{gathered} \pm 2.0 \\ \pm 3.0 \\ +3.0,-3.5 \\ \hline \end{gathered}$ |  | $\begin{aligned} & \pm 3.0 \\ & \pm 4.0 \\ & \pm 4.0 \\ & \hline \end{aligned}$ |  |
| Nonlinearity (Note 7) |  |  | $\pm 0.8$ |  | $\pm 0.8$ | ${ }^{\circ} \mathrm{C}$ (max) |
| Sensor Gain <br> (Average Slope) |  |  | $\begin{gathered} +9.7 \\ +10.3 \end{gathered}$ |  | $\begin{gathered} +9.7 \\ +10.3 \end{gathered}$ | $\mathrm{mV} /{ }^{\circ} \mathrm{C}(\mathrm{min})$ <br> $\mathrm{mV} /{ }^{\circ} \mathrm{C}$ (max) |
| Output Resistance |  | 2000 | 4000 | 2000 | 4000 | $\Omega$ (max) |
| Line Regulation (Note 8) | $+4.5 \mathrm{~V} \leq \mathrm{V}_{\mathrm{S}} \leq+10 \mathrm{~V}$ |  | $\begin{array}{r}  \pm 0.8 \\ \pm \mathbf{1 . 2} \\ \hline \end{array}$ |  | $\begin{array}{r}  \pm 0.8 \\ \pm \mathbf{1 . 2} \\ \hline \end{array}$ | mV/V (max) <br> mV/V (max) |
| Quiescent Current (Note 9) | $+4.5 \mathrm{~V} \leq \mathrm{V}_{\mathrm{S}} \leq+10 \mathrm{~V}$ |  | $\begin{aligned} & 130 \\ & \mathbf{1 8 0} \\ & \hline \end{aligned}$ |  | $\begin{aligned} & 130 \\ & \mathbf{1 8 0} \\ & \hline \end{aligned}$ | $\mu \mathrm{A}(\max )$ <br> $\mu \mathrm{A}$ (max) |
| Change of Quiescent Current (Note 8) | $+4.5 \mathrm{~V} \leq \mathrm{V}_{\mathrm{S}} \leq+10 \mathrm{~V}$ |  | 2.0 |  | 2.0 | $\mu \mathrm{A}$ (max) |
| Temperature Coefficient of Quiescent Current |  | +1.0 |  | +2.0 |  | $\mu \mathrm{A} /{ }^{\circ} \mathrm{C}$ |
| Long Term Stability (Note 10) | $\begin{gathered} \mathrm{T}_{J}=125^{\circ} \mathrm{C}, \text { for } \\ 1000 \text { hours } \end{gathered}$ | $\pm 0.08$ |  | $\pm 0.08$ |  | ${ }^{\circ} \mathrm{C}$ |

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. DC and AC electrical specifications do not apply when operating the device beyond its rated operating conditions.
Note 2: See AN-450 "Surface Mounting Methods and Their Effect on Product Reliability" or the section titled "Surface Mount" found in a current National Semiconductor Linear Data Book for other methods of soldering surface mount devices.
Note 3: Human body model, 100 pF discharged through a $1.5 \mathrm{k} \Omega$ resistor. Machine model, 200 pF discharged directly into each pin.
Note 4: Thermal resistance of the SOT-23 package is specified without a heat sink, junction to ambient.
Note 5: Limits are guaranteed to National's AOQL (Average Outgoing Quality Level).
Note 6: Accuracy is defined as the error between the output voltage and $10 \mathrm{mv} /{ }^{\circ} \mathrm{C}$ times the device's case temperature, at specified conditions of voltage, current, and temperature (expressed in ${ }^{\circ} \mathrm{C}$ ).
Note 7: Nonlinearity is defined as the deviation of the output-voltage-versus-temperature curve from the best-fit straight line, over the device's rated temperature range.
Note 8: Regulation is measured at constant junction temperature, using pulse testing with a low duty cycle. Changes in output due to heating effects can be computed by multiplying the internal dissipation by the thermal resistance.

Note 9: Quiescent current is defined in the circuit of Figure 1.
Note 10: For best long-term stability, any precision circuit will give best results if the unit is aged at a warm temperature, and/or temperature cycled for at least 46 hours before long-term life test begins. This is especially true when a small (Surface-Mount) part is wave-soldered; allow time for stress relaxation to occur. The majority of the drift will occur in the first 1000 hours at elevated temperatures. The drift after 1000 hours will not continue at the first 1000 hour rate.

## Typical Performance Characteristics

To generate these curves the LM50 was mounted to a printed circuit board as shown in Figure 2.


Thermal Response in Stirred Oil Bath with Heat Sink





Start-Up Response

$20 \mu \mathrm{~s} /$ DIVIIION





TL/H/12030-19
FIGURE 2. Printed Circuit Board Used for Heat Sink to Generate All Curves. $1 / 2^{\prime \prime}$ Square Printed Circuit Board with 2 oz. Foil or Similar

### 1.0 Mounting

The LM50 can be applied easily in the same way as other integrated-circuit temperature sensors. It can be glued or cemented to a surface and its temperature will be within about $0.2^{\circ} \mathrm{C}$ of the surface temperature.
This presumes that the ambient air temperature is almost the same as the surface temperature; if the air temperature were much higher or lower than the surface temperature, the actual temperature of the LM50 die would be at an intermediate temperature between the surface temperature and the air temperature.
To ensure good thermal conductivity the backside of the LM50 die is directly attached to the GND pin. The lands and traces to the LM50 will, of course, be part of the printed circuit board, which is the object whose temperature is being measured. These printed circuit board lands and traces will not cause the LM50s temperature to deviate from the desired temperature.
Alternatively, the LM50 can be mounted inside a sealed-end metal tube, and can then be dipped into a bath or screwed into a threaded hole in a tank. As with any IC, the LM50 and accompanying wiring and circuits must be kept insulated and dry, to avoid leakage and corrosion. This is especially true if the circuit may operate at cold temperatures where condensation can occur. Printed-circuit coatings and varnishes such as Humiseal and epoxy paints or dips are often used to ensure that moisture cannot corrode the LM50 or its connections.

| Temperature Rise of LM50 Due to Self-Heating |  |  |
| :--- | :---: | :---: |
| (Thermal Resistance, $\theta_{\text {JA) }}$ |  |  |
|  | SOT-23** | SOT-23 |
|  | no heat sink | small heat fin* |
| Still air | $450^{\circ} \mathrm{C} / \mathrm{W}$ | $260^{\circ} \mathrm{C} / \mathrm{W}$ |
| Moving air |  | $180^{\circ} \mathrm{C} / \mathrm{W}$ |

* Heat sink used is $1 / 2^{\prime \prime}$ square printed circuit board with 2 oz . foil with part attached as shown in Figure 2.
** Part soldered to 30 gauge wire.


### 2.0 Capacitive Loads



TL/H/12030-7
FIGURE 3. LM50 No Decoupling Required for Capacitive Load


FIGURE 4. LM50C with Filter for Noisy Environment
The LM50 handles capacitive loading very well. Without any special precautions, the LM50 can drive any capacitive load. The LM50 has a nominal $2 \mathrm{k} \Omega$ output impedance (as can be seen in the block diagram). The temperature coefficient of the output resistors is around $1300 \mathrm{ppm} /{ }^{\circ} \mathrm{C}$. Taking into account this temperature coefficient and the initial tolerance of the resistors the output impedance of the LM50 will not exceed $4 \mathrm{k} \Omega$. In an extremely noisy environment it may be necessary to add some filtering to minimize noise pickup. It is recommended that $0.1 \mu \mathrm{~F}$ be added from $\mathrm{V}_{\mathrm{IN}}$ to GND to bypass the power supply voltage, as shown in Figure 4. In a noisy environment it may be necessary to add a capacitor from the output to ground. A $1 \mu \mathrm{~F}$ output capacitor with the $4 \mathrm{k} \Omega$ output impedance will form a 40 Hz lowpass filter. Since the thermal time constant of the LM50 is much slower than the 25 ms time constant formed by the RC, the overall response time of the LM50 will not be significantly affected. For much larger capacitors this additional time lag will increase the overall response time of the LM50.


TL/H/12030-17
${ }^{*} \mathrm{R} 2 \approx 2 \mathrm{k}$ with a typical $1300 \mathrm{ppm} /{ }^{\circ} \mathrm{C}$ drift.
FIGURE 5. Block Diagram

### 3.0 Typical Applications



FIGURE 6. Centigrade Thermostat/Fan Controller
TL/H/12030-11


TL/H/12030-13
FIGURE 7. Temperature To Digital Converter (Serial Output) ( $+125^{\circ} \mathrm{C}$ Full Scale)


TL/H/12030-14
FIGURE 8. Temperature To Digital Converter (Parallel TRI-STATE ${ }^{\circledR}$ Outputs for Standard Data Bus to $\mu$ P Interface) ( $125^{\circ} \mathrm{C}$ Full Scale)


LM50B/LM50C SOT-23 Single-Supply Centigrade Temperature Sensor
Physical Dimensions inches (millimeters) unless otherwise noted

SOT-23 Molded Small Outline Transistor Package (M3)
Order Number LM50BIM3, or LM50CIM3
NS Package Number M03B
(JEDEC Registration TO-236AB)

## LIFE SUPPORT POLICY

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Applications

- Microprocessor Thermal Management
- Appliances
- Portable Battery Powered 3.0V or 5V Systems
- Fan Control
- Industrial Process Control
- HVAC Systems
- Remote Temperature Sensing
- Electronic System Protection


## Features

- Digital outputs support TTL logic levels
- Internal temperature sensor
- 2 internal comparators with hysteresis
- Internal voltage reference
- Future availability in 8-pin Mini-SO8 plastic package
- Currently Available in 8 -pin SO plastic package


## Key Specifications

- Power Supply Voltage
2.7V-10V
- Power Supply Current
$230 \mu \mathrm{~A}$ (max) $1.250 \mathrm{~V} \pm 1 \%(\max )$
- Hysteresis Temperature
- Internal Temperature Sensor Output Voltage $\quad\left(+6.20 \mathrm{mV} /{ }^{\circ} \mathrm{C} \times \mathrm{T}\right)+395 \mathrm{mV}$
- Temperature Trip Point Accuracy:

|  | LM56BIM | LM56CIM |
| :--- | :---: | :---: |
| $+25^{\circ} \mathrm{C}$ | $\pm 2^{\circ} \mathrm{C}$ (max) | $\pm 3^{\circ} \mathrm{C}$ (max) |
| $+25^{\circ} \mathrm{C}$ to $+85^{\circ} \mathrm{C}$ | $\pm 2^{\circ} \mathrm{C}$ (max) | $\pm 3^{\circ} \mathrm{C}$ (max) |
| $-40^{\circ} \mathrm{C}$ to $+125^{\circ} \mathrm{C}$ | $\pm 3^{\circ} \mathrm{C}$ (max) | $\pm 4^{\circ} \mathrm{C}$ (max) |

## Simplified Block Diagram and Connection Diagram



| Order Number | LM56BIM | LM56BIMX | LM56CIM | LM56CIMX | LM56BIMM* | LM56CIMM* |
| :--- | :---: | :---: | :---: | :---: | :---: | :---: |
| NS Package Number | M08A | M08A | M08A | M08A | NMMSO008* | NMMSO008* $^{*}$ |
| Transport Media | Bulk Rail | 2500 Units <br> Tape \& Reel | Bulk Rail | 2500 Units <br> Tape \& Reel |  |  |

*The Mini-SO8 package option is not available yet.


## Absolute Maximum Ratings (Note 1)

| Input Voltage | 12 V |
| :--- | ---: |
| Input Current at any pin (Note 2) | 5 mA |
| Package Input Current (Note 2) | 20 mA |
| Package Dissipation at $\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$ (Note 3) | 900 mW |
| ESD Susceptibility (Note 4) |  |
| $\quad$ Human Body Model | 1000 V |
| Machine Model | 200 V |


| Soldering Information |  |
| :---: | :---: |
| SO Package (Note 5): |  |
| Vapor Phase (60 seconds) | $215^{\circ} \mathrm{C}$ |
| Infrared (15 seconds) | $220^{\circ} \mathrm{C}$ |
| Storage Temperature | $-65^{\circ} \mathrm{C}$ to $+150^{\circ} \mathrm{C}$ |
| Operating Ratings (Note 1) |  |
| Operating Temperature Range | $\mathbf{T}_{\text {MIN }} \leq \mathrm{T}_{\text {A }} \leq \mathrm{T}_{\text {MAX }}$ |
| LM56BIM, LM56CIM | $-40^{\circ} \mathrm{C} \leq \mathrm{T}_{\mathrm{A}} \leq+125^{\circ} \mathrm{C}$ |
| Positive Supply Voltage ( $\mathrm{V}^{+}$) | +2.7 V to +10 V |
| Maximum $\mathrm{V}_{\text {OUT1 }}$ and $\mathrm{V}_{\text {OUT2 }}$ | $+10 \mathrm{~V}$ |

LM56 Electrical Characteristics The following specifications apply for $\mathrm{V}^{+}=2.7 \mathrm{~V}_{\mathrm{DC}}$, and $\mathrm{V}_{\mathrm{REF}}$ load current $=50 \mu \mathrm{~A}$ unless otherwise specified. Boldface limits apply for $\mathbf{T}_{\mathbf{A}}=\mathbf{T}_{\mathbf{J}}=\mathbf{T}_{\text {MIN }}$ to $\mathbf{T}_{\mathbf{M A X}}$; all other limits $\mathrm{T}_{\mathbf{A}}=\mathrm{T}_{J}$ $=25^{\circ} \mathrm{C}$ unless otherwise specified.

| Symbol | Parameter | Conditions | Typical (Note 6) | LM56BIM Limits (Note 7) | LM56CIM Limits (Note 7) | Units (Limits) |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| Temperature Sensor |  |  |  |  |  |  |
|  | Trip Point Accuracy (Includes $V_{\text {REF }}$, Comparator Offset, and Temperature Sensitivity errors) | $\begin{aligned} & +25^{\circ} \mathrm{C} \leq \mathrm{T}_{\mathrm{A}} \leq+85^{\circ} \mathrm{C} \\ & -40^{\circ} \mathrm{C} \leq \mathrm{T}_{\mathrm{A}} \leq+125^{\circ} \mathrm{C} \end{aligned}$ |  | $\begin{aligned} & \pm 2 \\ & \pm 2 \\ & \pm 3 \end{aligned}$ | $\begin{aligned} & \pm 3 \\ & \pm 3 \\ & \pm \mathbf{4} \end{aligned}$ |  |
|  | Trip Point Hysteresis | $\mathrm{T}_{\mathrm{A}}=-40^{\circ} \mathrm{C}$ | 4 | $\begin{aligned} & 3 \\ & 6 \end{aligned}$ | $\begin{aligned} & 3 \\ & 6 \end{aligned}$ | ${ }^{\circ} \mathrm{C}(\min )$ ${ }^{\circ} \mathrm{C}(\max )$ |
|  |  | $\mathrm{T}_{\mathrm{A}}=+25^{\circ} \mathrm{C}$ | 5 | $\begin{aligned} & 3.5 \\ & 6.5 \end{aligned}$ | $\begin{aligned} & 3.5 \\ & 6.5 \end{aligned}$ | ${ }^{\circ} \mathrm{C}$ (min) ${ }^{\circ} \mathrm{C}$ (max) |
|  |  | $\mathrm{T}_{\mathrm{A}}=+85^{\circ} \mathrm{C}$ | 6 | $\begin{aligned} & 4.5 \\ & 7.5 \\ & \hline \end{aligned}$ | $\begin{aligned} & 4.5 \\ & 7.5 \\ & \hline \end{aligned}$ | ${ }^{\circ} \mathrm{C}$ (min) ${ }^{\circ} \mathrm{C}$ (max) |
|  |  | $\mathrm{T}_{\mathrm{A}}=+125^{\circ} \mathrm{C}$ | 6 | $\begin{aligned} & 4 \\ & 8 \end{aligned}$ | $\begin{aligned} & 4 \\ & 8 \end{aligned}$ | ${ }^{\circ} \mathrm{C}(\min )$ <br> ${ }^{\circ} \mathrm{C}$ (max) |
|  | Internal Temperature Sensitivity |  | +6.20 |  |  | $\mathrm{mV} /{ }^{\circ} \mathrm{C}$ |
|  | Temperature Sensitivity Error |  |  | $\begin{aligned} & \pm 2 \\ & \pm 3 \\ & \hline \end{aligned}$ | $\begin{array}{r}  \pm 3 \\ \pm \mathbf{4} \\ \hline \end{array}$ | ${ }^{\circ} \mathrm{C}(\max )$ <br> ${ }^{\circ} \mathrm{C}$ (max) |
|  | Output Impedance | $-1 \mu \mathrm{~A} \leq \mathrm{I}_{\mathrm{L}} \leq+40 \mu \mathrm{~A}$ |  | 1500 | 1500 | $\Omega$ (max) |
|  | Line Regulation | $+3.0 \mathrm{~V} \leq \mathrm{V}^{+} \leq+10 \mathrm{~V}$ |  | $\pm 0.3$ | $\pm 0.3$ | $\mathrm{mV} / \mathrm{V}$ (max) |
|  |  | $+2.7 \mathrm{~V} \leq \mathrm{V}+\leq+3.3 \mathrm{~V}$ |  | $\pm 2.3$ | $\pm 2.3$ | mV (max) |
| $\mathbf{V}_{\mathbf{T} 1}$ and $\mathbf{V}_{\mathbf{T} 2}$ Analog Inputs |  |  |  |  |  |  |
| $\mathrm{I}_{\text {BIAS }}$ | Analog Input Bias Current |  | 150 | 300 | 300 | $n A$ (max) |
| $\mathrm{V}_{\text {IN }}$ | Analog Input Voltage Range |  | $\begin{gathered} \mathrm{V}^{+}-1 \\ \text { GND } \end{gathered}$ |  |  | $\begin{aligned} & \mathrm{V} \\ & \mathrm{~V} \end{aligned}$ |
| $\mathrm{V}_{\text {OS }}$ | Comparator Offset |  | 2 | 8 | 8 | mV (max) |
| $\mathrm{V}_{\text {REF }}$ Output |  |  |  |  |  |  |
| $\mathrm{V}_{\text {REF }}$ | $\mathrm{V}_{\text {REF }}$ Nominal |  | 1.250 V |  |  | V |
|  | $\mathrm{V}_{\text {REF }}$ Error |  |  | $\begin{gathered} \pm 1 \\ \pm \mathbf{1 2 . 5} \end{gathered}$ | $\begin{gathered} \pm 1 \\ \pm \mathbf{1 2 . 5} \end{gathered}$ | $\begin{gathered} \%(\max ) \\ m V(\max ) \end{gathered}$ |
| $\Delta \mathrm{V}_{\mathrm{REF}} / \Delta \mathrm{V}^{+}$ | Line Regulation | $\begin{aligned} & +3.0 \mathrm{~V} \leq \mathrm{V}^{+} \leq+10 \mathrm{~V} \\ & +2.7 \mathrm{~V} \leq \mathrm{V}^{+} \leq+3.3 \mathrm{~V} \end{aligned}$ | $\begin{aligned} & 0.13 \\ & 0.15 \end{aligned}$ | $\begin{aligned} & 0.20 \\ & 1.45 \end{aligned}$ | $\begin{aligned} & 0.20 \\ & 1.45 \end{aligned}$ | $\begin{gathered} \mathrm{mV} / \mathrm{V}(\max ) \\ \mathrm{mV}(\max ) \end{gathered}$ |
| $\Delta \mathrm{V}_{\text {REF }} / \Delta \mathrm{I}_{\mathrm{L}}$ | Load Regulation Sourcing | $+30 \mu \mathrm{~A} \leq \mathrm{I}_{\mathrm{L}} \leq+50 \mu \mathrm{~A}$ |  | 0.15 | 0.15 | $\mathrm{mV} / \mu \mathrm{A}$ (max) |

LM56 Electrical Characteristics The following specifications apply for $\mathrm{V}^{+}=2.7 \mathrm{~V}_{\mathrm{DC}}$, and $\mathrm{V}_{\text {REF }}$ load current $=50 \mu \mathrm{~A}$ unless otherwise specified. Boldface limits apply for $\mathbf{T}_{\mathbf{A}}=\mathbf{T}_{\mathbf{J}}=\mathbf{T}_{\mathbf{M I N}}$ to $\mathbf{T}_{\mathbf{M A X}}$; all other limits $\mathrm{T}_{\mathrm{A}}=\mathrm{T}_{\mathrm{J}}$ $=25^{\circ} \mathrm{C}$ unless otherwise specified. (Continued)

| Symbol | Parameter | Conditions | Typical (Note 6) | Limits (Note 7) | Units (Limits) |
| :---: | :---: | :---: | :---: | :---: | :---: |
| v+ Power Supply |  |  |  |  |  |
| Is | Supply Current | $\begin{aligned} & \mathrm{V}^{+}=+10 \mathrm{~V} \\ & \mathrm{~V}^{+}=+2.7 \mathrm{~V} \\ & \hline \end{aligned}$ |  | $\begin{aligned} & 230 \\ & 230 \end{aligned}$ | $\mu \mathrm{A}(\max )$ $\mu \mathrm{A}(\max )$ |
| Digital Output(s) |  |  |  |  |  |
| lout("1") | Logical "1" Output Leakage Current | $\mathrm{V}^{+}=+5.0 \mathrm{~V}$ |  | 1 | $\mu \mathrm{A}$ (max) |
| $\mathrm{V}_{\text {OUT ("0") }}$ | Logical "0" Output Voltage | lout $=+50 \mu \mathrm{~A}$ |  | 0.4 | $V$ (max) |

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional, but do not guarantee specific performance limits. For guaranteed specifications and test conditions, see the Electrical Characteristics. The guaranteed specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions.
Note 2: When the input voltage $\left(V_{1}\right)$ at any pin exceeds the power supply $\left(V_{1}<G N D\right.$ or $\left.V_{1}>V^{+}\right)$, the current at that pin should be limited to 5 mA . The 20 mA maximum package input current rating limits the number of pins that can safely exceed the power supplies with an input current of 5 mA to four.
Note 3: The maximum power dissipation must be derated at elevated temperatures and is dictated by $T_{J m a x}$ (maximum junction temperature), $\Theta_{J A}$ (junction to ambient thermal resistance) and $T_{A}$ (ambient temperature). The maximum allowable power dissipation at any temperature is $P_{D}=\left(T_{J m a x}-T_{A}\right) / \Theta_{J A}$ or the number given in the Absolute Maximum Ratings, whichever is lower. For this device, $\mathrm{T}_{\mathrm{Jmax}}=125^{\circ} \mathrm{C}$. For this device the typical thermal resistance ( $\Theta_{\mathrm{JA}}$ ) of the different package types when board mounted follow:

| Pacakge Type | $\Theta_{\mathrm{JA}}$ |
| :---: | :---: |
| M08A | $110^{\circ} \mathrm{C} / \mathrm{W}$ |

Note 4: The human body model is a 100 pF capacitor discharge through a $1.5 \mathrm{k} \Omega$ resistor into each pin. The machine model is a 200 pF capacitor discharged directly into each pin.
Note 5: See AN450 "Surface Mounting Methods and Their Effects on Product Reliability" or the section titled "Surface Mount" found in any post 1986 National Semiconductor Linear Data Book for other methods of soldering surface mount devices.
Note 6: Typicals are at $T_{J}=T_{A}=25^{\circ} \mathrm{C}$ and represent most likely parametric norm.
Note 7: Limits are guaranteed to National's AOQL (Average Outgoing Quality Level).

## Typical Performance Characteristics



Trip Point Hysteresis vs


TL/H/12893-7
Trip Point



Temperature Sensor Output Voltage vs Temperature


TL/H/12893-8
Comparator Bias Current vs Temperature


OUT1 and OUT2 Voltage Levels vs Load Current

Temperature Sensor Output Accuracy vs

TL/H/12893-9

OUT1 and OUT2 Leakage Current vs Temperature




TL/H/12893-14

Functional Description


### 1.0 PIN DESCRIPTION

$\mathrm{V}^{+} \quad$ This is the positive supply voltage pin. This pin should be bypassed with $0.1 \mu \mathrm{~F}$ capacitor to ground.
GND This is the ground pin.
$V_{\text {REF }} \quad$ This is the 1.250 V bandgap voltage reference output pin. In order to maintain trip point accuracy this pin should source a $50 \mu \mathrm{~A}$ load.
$V_{\text {TEMP }}$ This is the temperature sensor output pin.
OUT1 This is an open collector digital output. OUT1 is active LOW. It goes LOW when the temperature is greater than $\mathrm{T}_{1}$ and goes HIGH when the temperature drops below $\mathrm{T}_{1}-4^{\circ} \mathrm{C}$. This output is not intended to directly drive a fan motor.
OUT2 This is an open collector digital output. OUT2 is active LOW. It goes LOW when the temperature is greater than the $\mathrm{T}_{2}$ set point and goes HIGH when the temperature is less than $\mathrm{T}_{2}-4^{\circ} \mathrm{C}$. This output is not intended to directly drive a fan motor.
$\mathrm{V}_{\mathrm{T} 1} \quad$ This is the input pin for the temperature trip point voltage for OUT1.
$\mathrm{V}_{\mathrm{T} 2} \quad$ This is the input pin for the low temperature trip point voltage for OUT2.

$\mathrm{V}_{\mathrm{T} 1}=1.250 \mathrm{~V} \times(\mathrm{R} 1) /(\mathrm{R} 1+\mathrm{R} 2+\mathrm{R} 3)$
$\mathrm{V}_{\mathrm{T} 2}=1.250 \mathrm{~V} \times(\mathrm{R} 1+\mathrm{R} 2) /(\mathrm{R} 1+\mathrm{R} 2+\mathrm{R} 3)$
where:
$(\mathrm{R} 1+\mathrm{R} 2+\mathrm{R} 3)=27 \mathrm{k} \Omega$ and
$\mathrm{V}_{\mathrm{T} 1}$ or $\mathrm{T} 2=\left[6.20 \mathrm{mV} /{ }^{\circ} \mathrm{C} \times \mathrm{T}\right]+395 \mathrm{mV}$ therefore:
$\mathrm{R} 1=\mathrm{V}_{\mathrm{T} 1} /(1.25 \mathrm{~V}) \times 27 \mathrm{k} \Omega$
$\mathrm{R} 2=\left(\mathrm{V}_{T 2} /(1.25 \mathrm{~V}) \times 27 \mathrm{k}\right) \Omega-\mathrm{R} 1$
$R 3=27 k \Omega-R 1-R 2$

## Application Hints

### 2.0 LM56 TRIP POINT ACCURACY SPECIFICATION

For simplicity the following is an analysis of the trip point accuracy using the single output configuration show in Figure 2 with a set point of $82^{\circ} \mathrm{C}$.
Trip Point Error Voltage $=\mathrm{V}_{\text {TPE }}$,
Comparator Offset Error for $\mathrm{V}_{\text {T1E }}$
Temperature Sensor Error $=\mathrm{V}_{\text {TSE }}$
Reference Output Error $=\mathrm{V}_{\text {RE }}$


TL/H/12893-17
FIGURE 2. Single Output Configuration

1. $\mathrm{V}_{\mathrm{TPE}}= \pm \mathrm{V}_{\mathrm{T} 1 \mathrm{E}}-\mathrm{V}_{\mathrm{TSE}}+\mathrm{V}_{\mathrm{RE}}$

Where:
2. $\mathrm{V}_{\mathrm{T} 1 \mathrm{E}}= \pm 8 \mathrm{mV}$ (max)
3. $\mathrm{V}_{\mathrm{TSE}}=\left(6.20 \mathrm{mV} /{ }^{\circ} \mathrm{C}\right) \times\left( \pm 3^{\circ} \mathrm{C}\right)= \pm 18.6 \mathrm{mV}$
4. $\mathrm{V}_{\mathrm{RE}}=1.250 \mathrm{~V} \times( \pm 0.01) \mathrm{R} 2 /(\mathrm{R} 1+\mathrm{R} 2)$

Using Equations from page 1 of the datasheet
$\mathrm{V}_{\mathrm{T} 1}=1.25 \mathrm{~V} \times R 2 /(\mathrm{R} 1+\mathrm{R} 2)=\left(6.20 \mathrm{mV} /{ }^{\circ} \mathrm{C}\right)\left(82^{\circ} \mathrm{C}\right)+395 \mathrm{mV}$ Solving for R2/(R1 $+\mathrm{R} 2)=0.7227$
then,
5. $V_{R E}=1.250 \mathrm{~V} \times( \pm 0.01) R 2 /(R 1+R 2)=(0.0125) x$ $(0.7227)= \pm 9.03 \mathrm{mV}$
The individual errors do not add algebraically because, the odds of all the errors being at their extremes are rare. This is proven by the fact the specification for the trip point accuracy stated in the Electrical Characteristic for the temperature range of $-40^{\circ} \mathrm{C}$ to $+125^{\circ} \mathrm{C}$, for example, is specified at $\pm 3^{\circ} \mathrm{C}$ for the LM56BIM. Note this trip point error specification does not include any error introduced by the tolerance of the actual resistors used.
If the resistors have a $\pm 0.5 \%$ tolerance, an additional error of $\pm 0.4^{\circ} \mathrm{C}$ will be introduced. This error will increase to $\pm 0.8^{\circ} \mathrm{C}$ when both external resistors have a $\pm 1 \%$ tolerance.
3.0 BIAS CURRENT EFFECT ON TRIP POINT ACCURACY
Bias current for the comparator inputs is 300 nA (max) each, over the specified temperature range and will not introduce considerable error if the sum of the resistor values are kept to about $27 \mathrm{k} \Omega$ as shown in the typical application of Figure 1. This bias current of one comparator input will not flow if the temperature is well below the trip point level. As the temperature approaches trip point level the bias current will start to flow into the resistor network. When the temperature sensor output is equal to the trip point level the bias current


FIGURE 3. Simplified Schematic

## Application Hints (Continued)

will be 150 nA (max). Once the temperature is well above the trip point level the bias current will be 300 nA (max). Therefore, the first trip point will be affected by 150 nA of bias current. The leakage current is very small when the comparator input transistor of the different pair is off (see Figure 3).
The effect of the bias current on the first trip point can be defined by the following equations:

$$
\begin{aligned}
& \mathrm{K} 1=\frac{\mathrm{R} 1}{\mathrm{R} 1+\mathrm{R} 2+\mathrm{R} 3} \\
& \mathrm{~V}_{\mathrm{T} 1}=\mathrm{K} 1 \times \mathrm{V}_{\mathrm{REF}}+\mathrm{K} 1 \times(\mathrm{R} 2+\mathrm{R} 3) \times \frac{\mathrm{IB}}{2}
\end{aligned}
$$

where $I_{B}=300 n A$ (the maximum specified error).
The effect of the bias current on the second trip point can be defined by the following equations:

$$
\begin{aligned}
& \mathrm{K} 2=\frac{\mathrm{R} 1+\mathrm{R} 2}{\mathrm{R} 1+\mathrm{R} 2+\mathrm{R} 3} \\
& \mathrm{~V}_{\mathrm{T} 2}=\mathrm{K} 2 \times \mathrm{V}_{\mathrm{REF}}+\left(\mathrm{K} 1+\frac{\mathrm{K} 2}{2}\right) \times \mathrm{R} 3 \times \mathrm{I}_{\mathrm{B}}
\end{aligned}
$$

where $\mathrm{I}_{\mathrm{B}}=300 \mathrm{nA}$ (the maximum specified error).
The closer the two trip points are to each other the more significant the error is. Worst case would be when $\mathrm{V}_{\mathrm{T} 1}=$ $\mathrm{V}_{\mathrm{T} 2}=\mathrm{V}_{\mathrm{REF}} / 2$.

### 4.0 MOUNTING CONSIDERATIONS

The majority of the temperature that the LM56 is measuring is the temperature of its leads. Therefore, when the LM56 is placed on a printed circuit board, it is not sensing the temperature of the ambient air. It is actually sensing the temperature difference of the air and the lands and printed
circuit board that the leads are attached to. The most accurate temperature sensing is obtained when the ambient temperature is equivalent to the LM56's lead temperature.
As with any IC, the LM56 and accompanying wiring and circuits must be kept insulated and dry, to avoid leakage and corrosion. This is especially true if the cirucit may operate at cold temperatures where condensation can occur. Printed-circuit coatings and varnishes such as Humiseal and epoxy paints or dips are often used to ensure that moisture cannot corrode the LM56 or its connections.

## 5.0 $\mathrm{V}_{\text {REF }}$ AND $\mathrm{V}_{\text {TEMP }}$ CAPACTIVE LOADING

The LM56 $\mathrm{V}_{\text {REF }}$ and $\mathrm{V}_{\text {TEMP }}$ outputs handle capacitive loading well. Without any special precautions, these outputs can drive any capacitive load as shown in Figure 4.

### 6.0 NOISY ENVIRONMENTS

Over the specified temperature range the LM56 $\mathrm{V}_{\text {TEMP }}$ output has a maximum output impedance of $1500 \Omega$. In an extremely noisy environment it may be necessary to add some filtering to minimize noise pickup. It is recommended that $0.1 \mu \mathrm{~F}$ be added from $\mathrm{V}+$ to GND to bypass the power supply voltage, as shown in Figure 4. In a noisy environment it may be necessary to add a capacitor from the $\mathrm{V}_{\text {TEMP }}$ output to ground. A $1 \mu \mathrm{~F}$ output capacitor with the $1500 \Omega$ output impedance will form a 106 Hz lowpass filter. Since the thermal time constant of the $\mathrm{V}_{\text {TEMP }}$ output is much slower than the 9.4 ms time constant formed by the RC, the overall response time of the $\mathrm{V}_{\text {TEMP }}$ output will not be significantly affected. For much larger capacitors this additional time lag will increase the overall response time of the LM56.


FIGURE 4. Loading of $\mathrm{V}_{\text {REF }}$ and $\mathrm{V}_{\text {TEMP }}$

## Application Hints (Continued)

 7.0 APPLICATIONS CIRCUITS

FIGURE 5. Reducing Errors Caused by Bias Current
The circuit shown in Figure 5 will reduce the effective bias current error for $\mathrm{V}_{\mathrm{T} 2}$ as discussed in Section 3.0 to be equivalent to the error term of $V_{T 1}$. For this circuit the effect of the bias current on the first trip point can be defined by the following equations:

$$
\begin{aligned}
& K 1=\frac{R 1}{R 1+R 2} \\
& V_{T 1}=K 1 \times V_{R E F}+K 1 \times(R 2) \times \frac{I_{B}}{2}
\end{aligned}
$$

$$
\begin{aligned}
& K 2=\frac{R 3}{R 3+R 4} \\
& V_{T 1}=K 2 \times V_{R E F}+K 1 \times(R 4) \times \frac{I_{B}}{2}
\end{aligned}
$$

where $\mathrm{I}_{\mathrm{B}}=300 \mathrm{nA}$ (the maximum specified error).
The current shown in Figure 6 is a simple overtemperature detector for power devices. In this example, an audio power amplifier IC is bolted to a heat sink and an LM56 Celsius temperature sensor is mounted on a PC board that is bolted to the heat sink near the power amplifier. To ensure that the sensing element is at the same temperature as the heat sink, the sensor's leads are mounted to pads that have feed throughs to the back side of the PC board. Since the LM56 is sensing the temperature of the actual PC board the back side of the PC board also has large ground plane to help conduct the heat to the device. The comparator's output goes low if the heat sink temperature rises above a threshold set by R1, R2, and the voltage reference. This fault detection output from the comparator now can be used to turn on a cooling fan. The circuit as shown in design to turn the fan on when heat sink temperature exceeds about $80^{\circ} \mathrm{C}$, and to turn the fan off when the heat sink temperature falls below approximately $75^{\circ} \mathrm{C}$.
where $\mathrm{I}_{\mathrm{B}}=300 \mathrm{nA}$ (the maximum specified error).



## Physical Dimensions inches (millimeters) unless otherwise specified



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2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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| :---: | :---: | :---: | :---: |



| Absolute Maximum Ratings (Note 1) |  |  |  |
| :---: | :---: | :---: | :---: |
| Supply Voltage | +12 V to -0.2 V | Lead Temperature |  |
| Output Voltage $\quad\left(+\mathrm{V}_{S}\right.$ | $+\mathrm{V}_{\mathrm{S}}+0.6 \mathrm{~V}$ ) to -0.6 V | SOT Package (Note 4): |  |
| Output Current | 10 mA | Vapor Phase (60 seconds) | $+215^{\circ} \mathrm{C}$ |
| Input Current at any pin (Note 2) | 5 mA | Infrared (15 seconds) | $+220^{\circ} \mathrm{C}$ |
| Storage Temperature | $-65^{\circ} \mathrm{C}$ to $+150^{\circ} \mathrm{C}$ | Operating Ratings (Note 1) |  |
| Maximum Junction Temperature (TJMAX) $\quad+125^{\circ} \mathrm{C}$ ESD Susceptibility (Note 3): |  |  |  |
|  |  | Specified Temperature Range: | $\mathrm{T}_{\text {MIN }} \leq \mathbf{T}_{\mathbf{A}} \leq \mathrm{T}_{\text {MAX }}$ |
| Human Body Model | 800 V | LM60C | $-40^{\circ} \mathrm{C} \leq \mathrm{T}_{\mathrm{A}} \leq+125^{\circ} \mathrm{C}$ |
| Machine Model | 200 V | LM60B | $-25^{\circ} \mathrm{C} \leq \mathrm{T}_{\mathrm{A}} \leq+125^{\circ} \mathrm{C}$ |
|  |  | Supply Voltage Range ( $+\mathrm{V}_{\mathrm{s}}$ ) | +2.7 V to +10 V |
|  |  | Thermal Resistance, $\theta_{\text {JA }}$ (Note 5) | $450^{\circ} \mathrm{C} / \mathrm{W}$ |

Electrical Characteristics Unless otherwise noted, these specifications apply for $+\mathrm{V}_{\mathbf{S}}=+3.0 \mathrm{~V}_{\mathrm{DC}}$ and $I_{\text {LOAD }}=1 \mu \mathrm{~A}$. Boldface limits apply for $\mathbf{T}_{\mathbf{A}}=\mathbf{T}_{\mathbf{J}}=\mathbf{T}_{\text {MIN }}$ to $\mathbf{T}_{\mathbf{M A X}}$; all other limits $\mathrm{T}_{\mathbf{A}}=\mathrm{T}_{\mathrm{J}}=25^{\circ} \mathrm{C}$.

| Parameter | Conditions | Typical (Note 6) | LM60B | LM60C | Units (Limit) |
| :---: | :---: | :---: | :---: | :---: | :---: |
|  |  |  | Limits (Note 7) | Limits (Note 7) |  |
| Accuracy (Note 8) |  |  | $\begin{array}{r}  \pm 2.0 \\ \pm \mathbf{3 . 0} \\ \hline \end{array}$ | $\begin{array}{r}  \pm 3.0 \\ \pm \mathbf{4 . 0} \end{array}$ | ${ }^{\circ} \mathrm{C}$ (max) <br> ${ }^{\circ} \mathrm{C}$ (max) |
| Output Voltage at $0^{\circ} \mathrm{C}$ |  | + 424 |  |  | mV |
| Nonlinearity (Note 9) |  |  | $\pm 0.6$ | $\pm 0.8$ | ${ }^{\circ} \mathrm{C}$ (max) |
| Sensor Gain (Average Slope) |  | +6.25 | $\begin{array}{r} +6.06 \\ +6.44 \\ \hline \end{array}$ | $\begin{array}{r} +6.00 \\ +6.50 \\ \hline \end{array}$ | $\mathrm{mV} /{ }^{\circ} \mathrm{C}(\mathrm{min})$ <br> $\mathrm{mV} /{ }^{\circ} \mathrm{C}(\max )$ |
| Output Impedance |  |  | 800 | 800 | $\Omega$ (max) |
| Line Regulation (Note 10) | $+3.0 \mathrm{~V} \leq+\mathrm{V}_{\mathrm{S}} \leq+10 \mathrm{~V}$ |  | $\pm 0.3$ | $\pm 0.3$ | $\mathrm{mV} / \mathrm{V}$ (max) |
|  | $+2.7 \mathrm{~V} \leq+\mathrm{V}_{\mathrm{S}} \leq+3.3 \mathrm{~V}$ |  | $\pm 2.3$ | $\pm 2.3$ | mV (max) |
| Quiescent Current | $+2.7 \mathrm{~V} \leq+\mathrm{V}_{\mathrm{S}} \leq+10 \mathrm{~V}$ | 82 | $\begin{aligned} & 110 \\ & \mathbf{1 2 5} \\ & \hline \end{aligned}$ | $\begin{aligned} & 110 \\ & \mathbf{1 2 5} \\ & \hline \end{aligned}$ | $\mu \mathrm{A}$ (max) <br> $\mu \mathrm{A}$ (max) |
| Change of Quiescent Current | $+2.7 \mathrm{~V} \leq+\mathrm{V}_{\mathrm{S}} \leq+10 \mathrm{~V}$ |  | $\begin{array}{r}  \pm 5.0 \\ \pm \mathbf{2 0} \\ \hline \end{array}$ | $\begin{array}{r}  \pm 5.0 \\ \pm \mathbf{2 0} \\ \hline \end{array}$ | $\mu A$ (max) <br> $\mu \mathrm{A}(\max )$ |
| Temperature Coefficient of Quiescent Current |  | 0.2 |  |  | $\mu \mathrm{A} /{ }^{\circ} \mathrm{C}$ |
| Long Term Stability (Note 11) | $\begin{aligned} & T_{J}=T_{\text {MAX }}=+125^{\circ} \mathrm{C}, \text { for } \\ & 1000 \text { hours } \end{aligned}$ | $\pm 0.2$ |  |  | ${ }^{\circ} \mathrm{C}$ |

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional, but do not guarantee specific performance limits. For guaranteed specifications and test conditions, see the Electrical Characteristics. The guaranteed specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions.
Note 2: When the input voltage $\left(V_{1}\right)$ at any pin exceeds power supplies ( $\mathrm{V}_{\mathrm{l}}<\mathrm{GND}$ or $\mathrm{V}_{1}>+\mathrm{V}_{\mathrm{S}}$ ), the current at that pin should be limited to 5 mA .
Note 3: The human body model is a 100 pF capacitor discharged through a $1.5 \mathrm{k} \Omega$ resistor into each pin. The machine model is a 200 pF capacitor discharged directly into each pin.
Note 4: See AN-450 "Surface Mounting Methods and Their Effect on Product Reliability" or the section titled "Surface Mount" found in any post 1986 National Semiconductor Linear Data Book for other methods of soldering surface mount devices.
Note 5: The junction to ambient thermal resistance $\left(\theta_{\mathrm{JA}}\right)$ is specified without a heat sink in still air.
Note 6: Typicals are at $T_{J}=T_{A}=25^{\circ} \mathrm{C}$ and represent most likely parametric norm.
Note 7: Limits are guaranteed to National's AOQL (Average Outgoing Quality Level).
Note 8: Accuracy is defined as the error between the output voltage and $+6.25 \mathrm{mV} /{ }^{\circ} \mathrm{C}$ times the device's case temperature plus 424 mV , at specified conditions of voltage, current, and temperature (expressed in ${ }^{\circ} \mathrm{C}$ ).
Note 9: Nonlinearity is defined as the deviation of the output-voltage-versus-temperature curve from the best-fit straight line, over the device's rated temperature range.
Note 10: Regulation is measured at constant junction temperature, using pulse testing with a low duty cycle. Changes in output due to heating effects can be computed by multiplying the internal dissipation by the thermal resistance.
Note 11: For best long-term stability, any precision circuit will give best results if the unit is aged at a warm temperature, and/or temperature cycled for at least 46 hours before long-term life test begins. This is especially true when a small (Surface-Mount) part is wave-soldered; allow time for stress relaxation to occur. The majority of the drift will occur in the first 1000 hours at elevated temperatures. The drift after 1000 hours will not continue at the first 1000 hour rate.

## Typical Performance Characteristics

To generate these curves the LM60 was mounted to a printed circuit board as shown in Figure 2.



TL/H/12681-3


TL/H/12681-6


TL/H/12681-

$+V_{S}$ SUPPLY VOLTAGE $(V)$
TL/H/12681-12


TL/H/12681-4


TL/H/12681-7


L/H/12681-10

$5 \mu \mathrm{~s} / \mathrm{Div}$
TL/H/12681-13


TL/H/12681-5


TL/H/12681-8


TL/H/12681-11


TL/H/12681-1
figure 2. Printed Circuit Board Used for Heat Sink to Generate All Curves $1 / 2^{\prime \prime}$ Square Printed Circuit Board with 2 oz. Copper Foil or Similar.

### 1.0 Mounting

The LM60 can be applied easily in the same way as other integrated-circuit temperature sensors. It can be glued or cemented to a surface. The temperature that the LM60 is sensing will be within about $+0.1^{\circ} \mathrm{C}$ of the surface temperature that LM60's leads are attached to
This presumes that the ambient air temperature is almost the same as the surface temperature; if the air temperature were much higher or lower than the surface temperature, the actual temperature of the LM60 die would be at an intermediate temperature between the surface temperature and the air temperature.
To ensure good thermal conductivity the backside of the LM60 die is directly attached to the GND pin. The lands and traces to the LM60 will, of course, be part of the printed circuit board, which is the object whose temperature is being measured. These printed circuit board lands and traces will not cause the LM60's temperature to deviate from the desired temperature.
Alternatively, the LM60 can be mounted inside a sealed-end metal tube, and can then be dipped into a bath or screwed into a threaded hole in a tank. As with any IC, the LM60 and accompanying wiring and circuits must be kept insulated and dry, to avoid leakage and corrosion. This is especially true if the circuit may operate at cold temperatures where condensation can occur. Printed-circuit coatings and varnishes such as Humiseal and epoxy paints or dips are often used to ensure that moisture cannot corrode the LM60 or its connections.
The thermal resistance junction to ambient $\left(\theta_{\mathrm{JA}}\right)$ is the parameter used to calculate the rise of a device junction temperature due to the device power dissipation. For the LM60 the equation used to calculate the rise in the die temperature is as follows:

$$
\left.\mathrm{T}_{\mathrm{J}}=\mathrm{T}_{\mathrm{A}}+\theta_{\mathrm{JA}}\left[+\mathrm{V}_{\mathrm{S}} \mathrm{l}_{\mathrm{Q}}\right)+\left(+\mathrm{V}_{\mathrm{S}}-\mathrm{V}_{\mathrm{O}}\right) \mathrm{I}_{\mathrm{L}}\right]
$$

where $I_{Q}$ is the quiescent current and $I_{L}$ is the load current on the output.
The table shown in Figure 3 summarizes the rise in die temperature of the LM60 without any loading, and the thermal resistance for different conditions.

|  | SOT-23 <br> no heat sink** |  | SOT-23 <br> small heat fin* |  |
| :--- | :---: | :---: | :---: | :---: |
|  | $\theta_{\text {JA }}$ <br> $\left({ }^{\circ} \mathrm{C} / \mathrm{W}\right)$ | $\mathbf{T}_{\mathbf{J}}-\mathbf{T}_{\mathbf{A}}$ <br> $\left({ }^{\circ} \mathbf{C}\right)$ | $\theta_{\text {JA }}$ <br> $\left({ }^{\circ} \mathrm{C} / \mathrm{W}\right)$ | $\mathbf{T}_{\mathbf{J}}-\mathbf{T}_{\mathbf{A}}$ <br> $\left({ }^{\circ} \mathbf{C}\right)$ |
|  | 450 | 0.17 | 260 | 0.1 |
|  |  |  | 180 | 0.07 |

* Heat sink used is $1 / 2^{\prime \prime}$ square printed circuit board with 2 oz. foil with part attached as shown in Figure 2.
** Part soldered to 30 gauge wire
FIGURE 3. Temperature Rise of LM60 Due to Self-Heating and Thermal Resistance ( $\theta_{\mathrm{JA}}$ )


### 2.0 Capacitive Loads

The LM60 handles capacitive loading well. Without any special precautions, the LM60 can drive any capacitive load as shown in Figure 4. Over the specified temperature range the LM60 has a maximum output impedance of $800 \Omega$. In an extremely noisy environment it may be necessary to add some filtering to minimize noise pickup. It is recommended that $0.1 \mu \mathrm{~F}$ be added from $+\mathrm{V}_{\mathrm{S}}$ to GND to bypass the power supply voltage, as shown in Figure 5. In a noisy environment it may be necessary to add a capacitor from the output to ground. A $1 \mu \mathrm{~F}$ output capacitor with the $800 \Omega$ output impedance will form a 199 Hz lowpass filter. Since the thermal time constant of the LM60 is much slower than the 6.3 ms time constant formed by the RC, the overall response time of the LM60 will not be significantly affected. For much larger capacitors this additional time lag will increase the overall response time of the LM60.


TL/H/12681-15
FIGURE 4. LM60 No Decoupling Required for Capacitive Load


TL/H/12681-16
FIGURE 5. LM60 with Filter for Noisy Environment

### 2.0 Capacitive Loads (Continued)



TL/H/12681-17
FIGURE 6. Simplified Schematic

### 3.0 Applications Circuits




FIGURE 8. Conserving Power Dissipation with Shutdown
4.0 Recommended Solder Pads for SOT-23 Package


TL/H/12681-20


Physical Dimensions inches (millimeters) unless otherwise noted


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| :---: | :---: | :---: | :---: |




Absolute Maximum Ratings (Note 1)

| Supply Voltage | -0.3 V to 6.5 V |
| :--- | ---: |
| Voltage at any Pin | -0.3 V to $+\mathrm{V}_{\mathrm{S}}+0.3 \mathrm{~V}$ |
| Input Current at any Pin (Note 2) | 5 mA |
| Package Input Current (Note 2) | 20 mA |
| O.S. Output Sink Current | 10 mA |
| O.S. Output Voltage | 6.5 V |
| Storage Temperature | $-65^{\circ} \mathrm{C}$ to $+150^{\circ} \mathrm{C}$ |
| Soldering Information, Lead Temperature |  |
| SO Package (Note 3) |  |
| $\quad$ Vapor Phase (60 seconds) | $215^{\circ} \mathrm{C}$ |
| Infrared (15 seconds) | $220^{\circ} \mathrm{C}$ |

Temperature-to-Digital Converter Characteristics
Unless otherwise noted, these specifications apply for $+\mathrm{V}_{S}=+5 \mathrm{Vdc}$ for LM75CIM-5 and $+\mathrm{V}_{\mathrm{S}}=+3.3 \mathrm{Vdc}$ for LM75CIM-3 (Note 6). Boldface limits apply for $\mathbf{T}_{\mathbf{A}}=\mathbf{T}_{\mathbf{J}}=\mathbf{T}_{\mathbf{M I N}}$ to $\mathbf{T}_{\mathbf{M A X}}$; all other limits $\mathrm{T}_{\mathbf{A}}=\mathrm{T}_{\boldsymbol{J}}=+25^{\circ} \mathrm{C}$, unless otherwise noted.

| Parameter | Conditions | Typical (Note 12) | Limits (Note 7) | Units <br> (Limit) |
| :---: | :---: | :---: | :---: | :---: |
| Accuracy | $\begin{aligned} & \mathrm{T}_{\mathrm{A}}=-25^{\circ} \mathrm{C} \text { to }+100^{\circ} \mathrm{C} \\ & \mathrm{~T}_{\mathrm{A}}=-55^{\circ} \mathrm{C} \text { to }+125^{\circ} \mathrm{C} \end{aligned}$ |  | $\begin{array}{r}  \pm 2.0 \\ \pm \mathbf{3 . 0} \\ \hline \end{array}$ | ${ }^{\circ} \mathrm{C}$ (max) |
| Resolution |  | 9 |  | Bits |
| Temperature Conversion Time | (Note 8) | 100 |  | ms |
| Quiescent Current | ${ }^{12} \mathrm{C}$ Inactive ${ }^{2}{ }^{2} \mathrm{C}$ Active Shutdown Mode | $\begin{gathered} 0.25 \\ 1 \\ \hline \end{gathered}$ | 1.0 | $\begin{gathered} \mathrm{mA} \\ \mathrm{~mA}(\mathrm{max}) \\ \mu \mathrm{A} \\ \hline \end{gathered}$ |
| O.S. Output Saturation Voltage | $\begin{aligned} & \text { lout }=4.0 \mathrm{~mA} \\ & \text { (Note 9) } \end{aligned}$ |  | 0.8 | $V$ (max) |
| O.S. Delay | (Note 10) |  | $\begin{aligned} & 1 \\ & 6 \\ & \hline \end{aligned}$ | Conversions (min) Conversions (max) |
| TOS Default Temperature | (Note 11) | 80 |  | ${ }^{\circ} \mathrm{C}$ |
| THYST Default Temperature | (Note 11) | 75 |  | ${ }^{\circ} \mathrm{C}$ |

## Logic Electrical Characteristics

DIGITAL DC CHARACTERISTICS
Unless otherwise noted, these specifications apply for $+\mathrm{V}_{\mathrm{S}}=+5 \mathrm{Vdc}$. Boldface limits apply for $\mathbf{T}_{\mathbf{A}}=\mathbf{T}_{\mathbf{J}}=\mathbf{T}_{\text {MIN }}$ to $\mathbf{T}_{\text {MAX }}$; all other limits $\mathrm{T}_{\mathrm{A}}=\mathrm{T}_{\mathrm{J}}=+25^{\circ} \mathrm{C}$, unless otherwise noted.

| Symbol | Parameter | Conditions | Typical (Note 12) | Limits (Note 7) | Units (Limit) |
| :---: | :---: | :---: | :---: | :---: | :---: |
| $\mathrm{V}_{\mathrm{IN}(1)}$ | Logical "1" Input Voltage |  |  | $\begin{aligned} & +\mathbf{V}_{\mathbf{s}} \times \mathbf{0 . 7} \\ & +\mathbf{v}_{\mathbf{s}}+\mathbf{0 . 5} \\ & \hline \end{aligned}$ | $\begin{aligned} & V(\min ) \\ & \mathrm{V}(\max ) \end{aligned}$ |
| $\mathrm{V}_{\mathrm{IN}(0)}$ | Logical "0" Input Voltage |  |  | $\begin{gathered} -0.3 \\ +\mathbf{v}_{\mathbf{S}} \times 0.3 \\ \hline \end{gathered}$ | $V$ (min) <br> $V$ (max) |
| $1 \mathrm{IN}(1)$ | Logical "1" Input Current | $\mathrm{V}_{\mathrm{IN}}=5 \mathrm{~V}$ | 0.005 | 1.0 | $\mu \mathrm{A}$ (max) |
| $1 \mathrm{IN}(0)$ | Logical "0" Input Current | $\mathrm{V}_{\mathrm{IN}}=0 \mathrm{~V}$ | $-0.005$ | - 1.0 | $\mu \mathrm{A}$ (max) |
| $\mathrm{C}_{\text {IN }}$ | All Digital Inputs |  | 20 |  | pF |
| IOH | High Level Output Current | $\mathrm{V}_{\mathrm{OH}}=5 \mathrm{~V}$ |  | 100 | $\mu \mathrm{A}$ (max) |
| $\mathrm{V}_{\mathrm{OL}}$ | Low Level Output Voltage | $\mathrm{l}_{\mathrm{OL}}=3 \mathrm{~mA}$ |  | 0.4 | V (max) |
| $\mathrm{t}_{\mathrm{OF}}$ | Output Fall Time | $\begin{aligned} & \mathrm{C}_{\mathrm{L}}=400 \mathrm{pF} \\ & \mathrm{I}_{\mathrm{O}}=3 \mathrm{~mA} \end{aligned}$ |  | 250 | ns (max) |

## Logic Electrical Characteristics (Continued)

## ${ }^{2}{ }^{2} \mathrm{C}$ DIGITAL SWITCHING CHARACTERISTICS

Unless otherwise noted, these specifications apply for $+\mathrm{V}_{\mathrm{S}}=+5 \mathrm{Vdc}, \mathrm{C}_{\mathrm{L}}$ (load capacitance) on output lines $=80 \mathrm{pF}$ unless otherwise specified. Boldface limits apply for $\mathbf{T}_{\mathbf{A}}=\mathbf{T}_{\mathbf{J}}=\mathbf{T}_{\mathbf{M I N}}$ to $\mathbf{T}_{\mathbf{M A X}}$; all other limits $\mathrm{T}_{\mathbf{A}}=\mathrm{T}_{\mathbf{J}}=+25^{\circ} \mathrm{C}$, unless otherwise noted.
The switching characteristics of the LM75 fully meet or exceed the published specifications of the $1^{2} \mathrm{C}^{\circledR}$ bus. The following parameters are the timing relationships between SCL and SDA signals related to the LM75. They are not the $\mathrm{I}^{2} \mathrm{C}^{(8}$ bus specifications.

| Symbol | Parameter | Conditions | Typical <br> (Note 12) | Limits <br> (Note 7) | Units <br> (Limit) |
| :--- | :--- | :--- | :---: | :---: | :---: |
| $\mathrm{t}_{1}$ | SCL (Clock) Period |  |  | $\mathbf{2 . 5}$ | $\mu \mathrm{s}(\mathrm{min})$ |
| $\mathrm{t}_{2}$ | Data in Set-Up Time to SCL High |  |  | $\mathbf{1 0 0}$ | $\mathrm{ns}(\mathrm{min})$ |
| $\mathrm{t}_{3}$ | Data Out Stable after SCL Low |  |  | $\mathbf{0}$ | $\mathrm{ns}(\mathrm{min})$ |
| $\mathrm{t}_{4}$ | SDA Low Set-Up Time to SCL Low (Start Condition) |  |  | $\mathbf{1 0 0}$ | $\mathrm{ns}(\mathrm{min})$ |
| $\mathrm{t}_{5}$ | SDA High Hold Time after SCL High (Stop Condition) |  |  | $\mathbf{1 0 0}$ | $\mathrm{ns}(\mathrm{min})$ |



TL/H/12658-4
Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. DC and AC electrical specifications do not apply when operating the device beyond its rated operating conditions.
Note 2: When the input voltage $\left(V_{1}\right)$ at any pin exceeds the power supplies ( $V_{1}<G N D$ or $V_{1}>+V_{S}$ ) the current at that pin should be limited to 5 mA . The 20 mA maximum package input current rating limits the number of pins that can safely exceed the power supplies with an input current of 5 mA to four.
Note 3: See AN-450 "Surface Mounting Methods and Their Effect on Product Reliability" or the section titled "Surface Mount" found in a current National Semiconductor Linear Data Book for other methods of soldering surface mount devices.
Note 4: Human body model, 100 pF discharged through a $1.5 \mathrm{k} \Omega$ resistor. Machine model, 200 pF discharged directly into each pin.
Note 5: Thermal resistance of the SO-8 package is $200^{\circ} \mathrm{C} / \mathrm{W}$, junction-to-ambient when attached to a printed circuit board with 2 oz. foil as shown in Figure 3 .
Note 6: Both part numbers of the LM75 will operate properly over the $+\mathrm{V}_{\mathrm{S}}$ supply voltage range of 3 V to 5.5 V . The devices are tested and specified for rated accuracy at their nominal supply voltage. Accuracy will typically degrade $1^{\circ} \mathrm{C} / \mathrm{V}$ of variation in $+\mathrm{V}_{\mathrm{S}}$ as it varies from the nominal value. Note 7: Limits are guaranteed to National's AOQL (Average Outgoing Quality Level).
Note 8: This specification is provided only to indicate how often temperature data is updated. The LM75 can be read at any time without regard to conversion state (and will yield last conversion result). If a conversion is in process it will be interrupted and restarted after the end of the read.
Note 9: For best accuracy, minimize output loading. Higher sink currents can affect sensor accuracy with internal heating. This can cause an error of $0.64^{\circ} \mathrm{C}$ at full rated sink current and saturation voltage based on junction-to-ambient thermal resistance.
Note 10: O.S. Delay is user programmable up to 6 "over limit" conversions before O.S. is set to minimize false tripping in noisy environments.
Note 11: Default values set at power up.
Note 12: Typicals are at $\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$ and represent most likely parametric norm.

Electrical Characteristics (Continued)


FIGURE 2. Temperature-to-Digital Transfer Function (Non-linear scale for clarity)


TL/H/12658-6
FIGURE 3. Printed Circuit Board Used for Thermal Resistance Specifications

### 1.0 Functional Description

The LM75 temperature sensor incorporates a band-gap type temperature sensor and 9-bit ADC (Delta-Sigma Ana-log-to-Digital Converter). The temperature data output of the LM75 is available at all times via the $I^{2} \mathrm{C}^{\circledR}$ bus. If a conversion is in progress, it will be stopped and restarted after the read. A digital comparator is also incorporated that compares a series of readings, the number of which is user-selectable, to user-programmable setpoint and hysteresis values. The comparator trips the O.S. output line, which is programmable for mode and polarity.

### 1.1 O.S. OUTPUT, TOS AND THYST LIMITS

In Comparator mode the O.S. Output behaves like a thermostat. The output becomes active when temperature exceeds the TOS limit, and leaves the active state when the temperature drops below the THYST limit. In this mode the O.S. output can be used to turn a cooling fan on, initiate an emergency system shutdown, or reduce system clock speed. Shutdown mode does not reset O.S. state in a comparator mode.
In Interrupt mode exceeding ToS also makes O.S. active but O.S. will remain active indefinitely until reset by reading any register via the $I^{2} \mathrm{C}^{\circledR}$ interface. Once O.S. has been activated by crossing Tos, then reset, it can be activated again only by Temperature going below $\mathrm{T}_{\text {HYST. }}$. Again, it will remain active indefinitely until being reset by a read. Placing the LM75 in shutdown mode also resets the O.S. Output.

### 1.2 DEFAULT MODES

LM75 always powers up in a known state. LM75 power up default conditions are:

1. Comparator mode
2. $\mathrm{T}_{\mathrm{OS}}$ set to $80^{\circ} \mathrm{C}$
3. THYSt set to $75^{\circ} \mathrm{C}$
4. O.S. active low
5. Pointer set to " 00 "; Temperature Register

With these operating conditions LM75 can act as a standalone thermostat with the above temperature settings. Connection to an $\mathrm{I}^{2} \mathrm{C}^{\circledR}$ bus is not required.

## $\left.1.3\right|^{2}{ }^{\text {® }}{ }^{\circledR}$ BUS INTERFACE

The LM75 operates as a slave on the ${ }^{2} \mathrm{C}$ bus, so the SCL line is an input (no clock is generated by the LM75) and the SDA line is a bi-directional serial data path. According to ${ }^{2}{ }^{2}{ }^{\circledR}$ ® bus specifications, the LM75 has a 7-bit slave address. The four most significant bits of the slave address are hard wired inside the LM75 and are " 1001 ". The three least significant bits of the address are assigned to pins A2-A0, and are set by connecting these pins to ground for a low, (0); or to $+V_{S}$ for a high, (1).


TL/H/12658-7
*Note: These interrupt mode resets of O.S. occur only when LM75 is read or placed in shutdown. Otherwise, O.S. would remain active indefinitely for any event.
FIGURE 4. O.S. Output Temperature Response Diagram

### 1.0 Functional Description (Continued)

Therefore, the complete slave address is:

| 1 | 0 | 0 | 1 | A2 | A1 | A0 |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |

### 1.4 TEMPERATURE DATA FORMAT

Temperature data can be read from the Temperature, TOS Set Point, and THYST Set Point registers; and written to the TOS Set Point, and THYST Set Point registers. Temperature data is represented by a 9-bit, two's complement word with an LSB (Least Significant Bit) equal to $0.5^{\circ} \mathrm{C}$ :

| Temperature | Digital Output |  |
| :---: | :---: | :---: |
|  | Binary | Hex |
| $+125^{\circ} \mathrm{C}$ | 011111010 | 0FAh |
| $+25^{\circ} \mathrm{C}$ | 000110010 | 032 h |
| $+0.5^{\circ} \mathrm{C}$ | 000000001 | 001 h |
| $0^{\circ} \mathrm{C}$ | 000000000 | 000 h |
| $-0.5^{\circ} \mathrm{C}$ | 111111111 | 1 FFh |
| $-25^{\circ} \mathrm{C}$ | 111001110 | 1 CEh |
| $-55^{\circ} \mathrm{C}$ | 110010010 | 192 h |

### 1.5 SHUTDOWN MODE

Shutdown mode is enabled by setting the shutdown bit in the Configuration register via the $1^{2} \mathrm{C}^{\circledR}$ bus. Shutdown mode reduces power supply current to $1 \mu \mathrm{~A}$ typical. In Interrupt mode O.S. is reset if previously set and is undefined in Comparator mode during shutdown. The $I^{2} \mathrm{C}^{\circledR}$ interface remains active. Activity on the clock and data lines of the $\mathrm{I}^{2} \mathrm{C}^{\circledR}$ bus may slightly increase shutdown mode quiescent current. TOS, $T_{\text {HYST }}$, and Configuration registers can be read from and written to in shutdown mode.

### 1.6 FAULT QUEUE

A fault queue of up to 6 faults is provided to prevent false tripping of O.S. when the LM75 is used in noisy environments. The number of faults set in the queue must occur consecutively to set the O.S. output.

### 1.7 COMPARATOR/INTERRUPT MODE

As indicated in the O.S. Output Temperature Response Diagram, Figure 4, the events that trigger O.S. are identical for either Comparator or Interrupt mode. The most important difference is that in Interrupt mode the O.S. will remain set indefinitely once it has been set. To reset O.S. while in Interrupt mode, perform a read from any register in the LM75.
1.8 O.S. OUTPUT

The O.S. output is an open-drain output and does not have an internal pull-up. A "high" level will not be observed on this pin until pull-up current is provided from some external source, typically a pull-up resistor. Choice of resistor value depends on many system factors but, in general, the pull-up resistor should be as large as possible. This will minimize any errors due to internal heating of the LM75. The maximum resistance of the pull up, based on LM75 specification for High Level Output Current, to provide a 2V high level, is $30 \mathrm{k} \Omega$.
1.9 O.S. POLARITY

The O.S. output can be programmed via the configuration register to be either active low (default mode), or active high. In active low mode the O.S. output goes low when triggered exactly as shown on the O.S. Output Temperature Response Diagram, Figure 4. Active high simply inverts the polarity of the O.S. output.

### 1.0 Functional Description (Continued)

1.10 internal register structure


There are four data registers in the LM75, selected by the Pointer register. At power-up the Pointer is set to " 00 "; the location for the Temperature Register. The Pointer register latches whatever the last location it was set to. In Interrupt Mode, a read from the LM75, or placing the device in shutdown mode, resets the O.S. output. All registers are read and write, except the Temperature register which is read only.
A write to the LM75 will always include the address byte and the Pointer byte. A write to the Configuration register requires one data byte, and the TOS and $T_{\text {HYST }}$ registers require two data bytes.
Reading the LM75 can take place either of two ways: If the location latched in the Pointer is correct (most of the time it is expected that the Pointer will point to the Temperature register because it will be the data most frequently read from the LM75), then the read can simply consist of an address byte, followed by retrieving the corresponding number of data bytes. If the Pointer needs to be set, then an ad-
dress byte, pointer byte, repeat start, and another address byte will accomplish a read.
The first data byte is the most significant byte with most significant bit first, permitting only as much data as necessary to be read to determine temperature condition. For instance, if the first four bits of the temperature data indicates an overtemperature condition, the host processor could immediately take action to remedy the excessive temperatures. At the end of a read, the LM75 can accept either Acknowledge or No Acknowledge from the Master (No Acknowledge is typically used as a signal for the slave that the Master has read its last byte).
An inadvertent 8-bit read from a 16-bit register, with the D7 bit low, can cause the LM75 to stop in a state where the SDA line is held low as shown in Figure 5. This can prevent any further bus communication until at least 9 additional clock cycles have occurred. Alternatively, the master can issue clock cycles until SDA goes high, at which time issuing a "Stop" condition will reset the LM75.


FIGURE 5. Inadvertent 8-Bit Read from 16-Bit Register where D7 is Zero (" 0 ")

### 1.0 Functional Description (Continued)

1.11 POINTER REGISTER (Selects which registers will be read from or written to):

| P7 | P6 | P5 | P4 | P3 | P2 | P1 | P0 |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| 0 | 0 | 0 | 0 | 0 | 0 | Register <br> Select |  |

P0-P1: Register Select:

| P1 | P0 | Register |
| :---: | :---: | :--- |
| 0 | 0 | Temperature (Read only)(Power-up default) |
| 0 | 1 | Configuration (Read/Write) |
| 1 | 0 | THYST (Read/Write) |
| 1 | 1 | TOS (Read/Write) |

P2-P7: Must be kept zero.
1.12 TEMPERATURE REGISTER (Read Only):

| D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| MSB | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | LSB | X | X | X | X | X | X | X |

D0-D6: Undefined
D7-D15: Temperature Data. One LSB $=0.5^{\circ}$. Two's complement format.
1.13 CONFIGURATION REGISTER (Read/Write):

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| 0 | 0 | 0 | Fault Queue | O.S. <br> Polarity | Cmp/Int | Shutdown |  |

Power up default is with all bits "0" (zero).
D0: Shutdown: When set to 1 the LM75 goes to low power shutdown mode.
D1: Comparator/Interrupt mode: 0 is Comparator mode, 1 is Interrupt mode.
D2: O.S. Polarity: 0 is active low, 1 is active high. O.S. is an open-drain output under all conditions.
D3-D4: Fault Queue: Number of faults necessary to detect before setting O.S. output to avoid false tripping due to noise:

| D4 | D3 | Number of Faults |
| :---: | :---: | :--- |
| 0 | 0 | 1 (Power-up default) |
| 0 | 1 | 2 |
| 1 | 0 | 4 |
| 1 | 1 | 6 |

D5-D7: These bits are used for production testing and must be kept zero for normal operation.

### 1.0 Functional Description (Continued)

1.14 THYSt AND Tos REGISTER (Read/Write):

| D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| MSB | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | LSB | X | X | X | X | X | X | X |

D0-D6: Undefined
D7-D15: THYST Or TOS Trip Temperature Data. Power up default is $\mathrm{T}_{\mathrm{OS}}=80^{\circ} \mathrm{C}, \mathrm{T}_{\mathrm{HYST}}=75^{\circ} \mathrm{C}$.



### 3.0 Application Hints

The LM75 can be applied easily in the same way as other integrated-circuit temperature sensors. It can be glued or cemented to a surface and its temperature will be within about $0.2^{\circ} \mathrm{C}$ of the surface temperature.
This presumes that the ambient air temperature is almost the same as the surface temperature; if the air temperature were much higher or lower than the surface temperature, the actual temperature of the LM75 die would be at an intermediate temperature between the surface temperature and the air temperature.
The path of best thermal conductivity is between the die and the GND pin, upon which the die is mounted. The printedcircuit board lands and traces connecting to the LM75 will be the object whose temperature is being measured.

In probe type applications, the LM75 can be mounted inside a sealed-end metal tube, and can then be dipped into a bath or screwed into a threaded hole in a tank. As with any IC, the LM75 and accompanying wiring and circuits must be kept insulated and dry, to avoid leakage and corrosion. This is especially true if the circuit may operate at cold temperatures where condensation can occur. Printed-circuit coatings and varnishes such as Humiseal and epoxy paints or dips are often used to insure that moisture cannot corrode the LM75 or its connections.

## Typical Applications



When using the two-wire interface: program O.S. for active high and connect O.S. directly to Q2's gate
FIGURE 8. Simple Fan Controller, Interface Optional


FIGURE 9. Data Acquisition System with Temperature Input via ${ }^{2} \mathbf{C}^{\circledR}$ Bus

## Typical Applications (Continued)



FIGURE 11. Temperature Sensor with Loudmouth Alarm (Barking Watchdog)

Physical Dimensions inches (millimeters) unless otherwise noted


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| :---: | :---: | :---: | :---: |

## System Monitors

- LM78 Microprocessor System Hardware Monitor with $\mathrm{I}^{2} \mathrm{C}$ and ISA Interface
- LM79 LM78 Upgrate for Intel's Klamath Processor
September 1996


## General Description

The LM78 is a highly integrated Data Acquisition system for hardware monitoring of servers, Personal Computers, or virtually any microprocessor based system. In a PC, the LM78 can be used to monitor power supply voltages, temperatures, and fan speeds. Actual values for these inputs can be read at any time, and programmable WATCHDOGTM limits in the LM78 activate a fully programmable and maskable interrupt system with two outputs.
The LM78 has an on-chip temperature sensor, 5 positive analog inputs, two inverting inputs (for monitoring negative voltages), and an 8-bit ADC. An input is provided for the overtemperature outputs of additional temperature sensors and this is linked to the interrupt system. The LM78 provides inputs for three fan tachometer outputs. Additional inputs are provided for Chassis Intrusion detection circuits, VID monitor inputs, and chainable interrupt. The LM78 provides both ISA and Serial Bus interfaces. A 32-byte auto-increment RAM is provided for POST (Power On Self Test) code storage.

## Features

■ Temperature sensing

- 5 positive voltage inputs

■ 2 op amps for negative voltage monitoring

- 3 fan speed monitoring inputs
- Input for additional temperature sensors
- Chassis Intrusion Detector input
- WATCHDOG comparison of all monitored values
- POST code storage RAM
- ISA and $\mathrm{I}^{2} \mathrm{C}^{\circledR}$ Serial Bus interfaces


## Key Specifications

| - Voltage monitoring accuracy | $\pm 1 \%$ (max) |
| :--- | :--- |
| - Temperature Accuracy |  |
| $-10^{\circ} \mathrm{C}$ to $+100^{\circ} \mathrm{C}$ | $\pm 3^{\circ} \mathrm{C}$ (max) |

-100

- Supply Voltage

Operating: 1 mA typ Shutdown: $10 \mu \mathrm{~A}$ typ

- ADC Resolution

8 Bits

## Applications

■ System Hardware Monitoring for Servers and PCs

- Office Electronics

■ Electronic Test Equipment and Instrumentation

## Typical Application




Pin Description

| Pin Name(s) | Pin Numbers | Number of Pins | Type | Description |
| :---: | :---: | :---: | :---: | :---: |
| IORD\# | 1 | 1 | Digital Input | An active low standard ISA bus I/O Read Control. |
| IOWR\# | 2 | 1 | Digital Input | An active low standard ISA bus I/O Write Control. |
| SYSCLK | 3 | 1 | Digital Input | The reference clock for the ISA bus. Typically ranges from 4.167 MHz to 8.33 MHz. The minimum clock frequency this input can handle is 1 Hz . |
| D7-D0 | 4-11 | 8 | Digital I/O | Bi-directional ISA bus Data lines. DO corresponds to the low order bit, with D7 the high order bit. |
| $\mathrm{V}_{\mathrm{CC}}(+5 \mathrm{~V})$ | 12 | 1 | POWER | $+5 \mathrm{~V} \mathrm{~V}_{\mathrm{CC}}$ power. Bypass with the parallel combination of $10 \mu \mathrm{~F}$ (electolytic or tantalum) and $0.1 \mu \mathrm{~F}$ (ceramic) bypass capacitors. |
| GNDD | 13 | 1 | GROUND | Internally connected to all digital circuitry. |
| SMI_IN\# | 14 | 1 | Digital Input | Chainable SMI \# (System Management Interrupt) Input. This is an active low input that propagates the SMI\# signal to the SMI\# output of the LM78 via SMI \# Mask Register Bit 6 and SMI \# enable Bit 1 of the Configuration Register. |
| Chassis Intrusion | 15 | 1 | Digital I/O | An active high input from an external circuit which latches a Chassis Intrusion event. This line can go high without any clamping action regardless of the powered state of the LM78. The LM78 provides an internal open drain on this line, controlled by Bit 7 of NMI Mask Register 2 , to provide a minimum 20 ms reset of this line. |
| Power Switch Bypass\# | 16 | 1 | Digital Output | An active low output intended to drive an external P-channel power MOSFET for software power control. |
| FAN3-FAN1 | 17-19 | 3 | Digital Input | 0 V to +5 V amplitude fan tachometer input. |
| SCL | 20 | 1 | Digital Input | Serial Bus Clock. |
| SDA | 21 | 1 | Digital I/O | Serial Bus bidirectional Data. |
| RESET\# | 22 | 1 | Digital Output | Master Reset, 5 mA driver (open drain), active low output with a 20 ms minimum pulse width. Available when enabeld via Bit 7 in SMI\# Mask Register 2. |
| NTEST | 23 | 1 | Test Output | NAND Tree totem-pole output that provides board-level connectivity testing. Refer to Section 11.0 on NAND Tree testing. |
| GNDA | 24 | 1 | GROUND | Internally connected to all analog circuitry. The ground reference for all analog inputs. |
| -IN6 | 25 | 1 | Analog Input | Ground-referred inverting op amp input. Refer to Section 4.0, "ANALOG INPUTS". |
| FB6 | 26 | 1 | Analog Output | Output of inverting op amp for Input 6. Refer to section 4.0, "ANALOG INPUTS". |
| FB5 | 27 | 1 | Analog Output | Output of inverting op amp for Input 5. Refer to section 4.0, "ANALOG INPUTS". |
| -IN5 | 28 | 1 | Analog Input | Ground-referred inverting op amp input. Refer to Section 4.0, "ANALOG INPUTS". |
| IN4-IN0 | 29-33 | 1 | Analog Input | OV to 4.096V FSR Analog Inputs. |
| VID3-VID0 | 34-37 | 4 | Digital Input | Voltage Supply readouts from P6. This value is read in the VID/Fan Divisor Register. |
| BTI\# | 38 | 1 | Digital Input | Board Temperature Interrupt driven by O.S. outputs of additional temperature sensors such as LM75. Provides internal pull-up of $10 \mathrm{k} \Omega$. |
| NMI\# /IRQ\# | 39 | 1 | Digital Output | Non-Maskable Interrupt (open source)/Interrupt Request \# (open drain). The mode is selected with Bit 5 of the Configuration Register and the output is enabled when Bit 2 of the Configuration Register is set to 1 . The default state is disabled and IRQ\# mode. |

## Pin Description (Continued)

| Pin Name(s) | Pin <br> Numbers | Number <br> of Pins | Type | Description |
| :--- | :---: | :---: | :---: | :--- |
| SMI\# | 40 | 1 | Digital Output | System Management Interrupt (open drain). This output is enabled when <br> Bit 1 in the Configuration Register is set to 1. The default state is disabled. |
| A2-A0 | $41-43$ | 3 | Digital Input | The three lowest order bits of the 16-bit ISA Address Bus. A0 corresponds <br> to the lowest order bit. |
| CS\# | 44 | 1 | Digital Input | Chip Select input from an external decoder which decodes high order <br> address bits on the ISA Address Bus. This is an active low input. |
| TOTAL PINS |  | 44 |  |  |

\# Indicates Active Low ("Not")


| The following specifications apply for $+4.25 \mathrm{~V}_{\mathrm{DC}} \leq \mathrm{V}_{\mathrm{CC}} \leq+5.75 \mathrm{~V}_{\mathrm{DC}}$, $\mathrm{f}_{\text {SYSCLK }}=8.33 \mathrm{MHz}, \mathrm{R}_{\mathrm{S}}=25 \Omega$, unless otherwise specified. Boldface limits apply for $\mathbf{T}_{\mathbf{A}}=\mathbf{T}_{\mathbf{J}}=\mathbf{T}_{\mathbf{M I N}}$ to $\mathbf{T}_{\mathbf{M A X}}$; all other limits $\mathrm{T}_{\mathbf{A}}=\mathrm{T}_{\mathrm{J}}=25^{\circ} \mathrm{C}$ (Note 7). |  |  |  |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: |
| Symbol | Parameter | Conditions | Typical (Note 8) | Limits (Note 9) | Units (Limits) |
| FAN RPM-TO-DIGITAL CONVERTER |  |  |  |  |  |
|  | Accuracy | $\begin{aligned} & +25^{\circ} \mathrm{C} \leq \mathrm{T}_{\mathrm{A}} \leq+75^{\circ} \mathrm{C} \\ & -10^{\circ} \mathrm{C} \leq \mathrm{T}_{\mathrm{A}} \leq+100^{\circ} \mathrm{C} \end{aligned}$ |  | $\begin{gathered} \pm 6 \\ \pm \mathbf{1 2} \end{gathered}$ | \% (max) <br> \% (max) |
|  | Full-scale Count |  |  | 255 | (max) |
|  | FAN1 and FAN2 Nominal Input | Divisor = 1, Fan Count = 153 (Note 12) | 8800 |  | RPM |
|  | RPM (See Section 6.0) | Divisor $=2$, Fan Count $=153$ (Note 12) | 4400 |  | RPM |
|  |  | Divisor $=3$, Fan Count $=153$ (Note 12) | 2200 |  | RPM |
|  |  | Divisor = 4, Fan Count = 153 (Note 12) | 1100 |  | RPM |
|  | FAN3 Design Nominal Input RPM | Fan Count = 153 (Note 12) | 4400 |  | RPM |
|  | Internal Clock Frequency | $+25^{\circ} \mathrm{C} \leq \mathrm{T}_{\mathrm{A}} \leq+75^{\circ} \mathrm{C}$ | 22.5 | $\begin{aligned} & 21.1 \\ & 23.9 \end{aligned}$ | $\begin{aligned} & \mathrm{kHz}(\min ) \\ & \mathrm{kHz}(\max ) \end{aligned}$ |
|  |  | $-10^{\circ} \mathrm{C} \leq \mathrm{T}_{\mathrm{A}} \leq+100^{\circ} \mathrm{C}$ | 22.5 | $\begin{aligned} & 19.8 \\ & 25.2 \end{aligned}$ | $\mathrm{kHz}(\min )$ <br> kHz (max) |
| DIGITAL OUTPUTS (Power Switch Bypass \#, NTEST, NMI/IRQ\#) |  |  |  |  |  |
| $\mathrm{V}_{\text {OUT(1) }}$ | Logical "1" Output Voltage | $\mathrm{I}_{\text {OUT }}= \pm 5.0 \mathrm{~mA}$ |  | 2.4 | $V$ (min) |
| $\mathrm{V}_{\text {OUT(0) }}$ | Logical "0" Output Voltage | $\mathrm{I}_{\text {OUT }}= \pm 5.0 \mathrm{~mA}$ |  | 0.4 | $V$ (max) |
| ISA D0-D7 DIGITAL OUTPUTS |  |  |  |  |  |
| $\mathrm{V}_{\text {OUT(1) }}$ | Logical "1" Output Voltage | $\mathrm{I}_{\text {OUT }}= \pm 12.0 \mathrm{~mA}$ |  | 2.4 | $V(\min )$ |
| $\mathrm{V}_{\text {OUT(0) }}$ | Logical "0" Output Voltage | $\mathrm{I}_{\text {OUT }}= \pm 12.0 \mathrm{~mA}$ |  | 0.4 | $V$ (max) |
| Iout | TRI-STATE ${ }^{\text {® }}$ Output Current | $\begin{aligned} & \mathrm{V}_{\text {OUT }}=0 \mathrm{~V}_{\mathrm{DC}} \\ & \mathrm{~V}_{\text {OUT }}=+5.0 \mathrm{~V}_{\mathrm{DC}} \end{aligned}$ | $\begin{gathered} 0.005 \\ -0.005 \end{gathered}$ | $\begin{gathered} 1 \\ -1 \\ \hline \end{gathered}$ | $\mu \mathrm{A}$ (max) <br> $\mu \mathrm{A}$ (min) |
| OPEN DRAIN DIGITAL OUTPUTS (SDA, RESET \#, SMI \#, Chassis Intrusion) |  |  |  |  |  |
| $\mathrm{V}_{\text {OUT(0) }}$ | Logical "0" Output Voltage | $\mathrm{I}_{\text {OUT }}=-5.0 \mathrm{~mA}$ |  | 0.4 | V (min) |
| IOH | High Level Output Current | $\mathrm{V}_{\text {OUT }}=+5.0 \mathrm{~V}_{\mathrm{DC}}$ | 0.1 | 100 | $\mu \mathrm{A}$ (max) |
|  | RESET\# and Chassis Intrusion Pulse Width |  | 45 | 20 | ms (min) |
| DIGITAL INPUTS: SMI_IN \#, VID0-VID3, BTI\#, CS \#, A0, A1, A2, Mode Control and interface Inputs (IORD \#, IOWR \#, SYSCLK), Data Lines (D0-D7), Chassis Intrusion, and Tach Pulse Logic Inputs (FAN1, FAN2, FAN3) |  |  |  |  |  |
| $\mathrm{V}_{\mathrm{IN}(1)}$ | Logical "1" Input Voltage |  |  | 2.0 | $V(\min )$ |
| $\mathrm{V}_{\text {IN }}(0)$ | Logical "0" Input Voltage |  |  | 0.8 | $V$ (max) |
| SERIAL BUS DIGITAL INPUTS (SCL, SDA) |  |  |  |  |  |
| $\mathrm{V}_{\text {IN(1) }}$ | Logical "1" Input Voltage |  |  | $0.7 \times V_{\text {cc }}$ | $V$ (min) |
| $\mathrm{V}_{\text {IN }(0)}$ | Logical "0" Input Voltage |  |  | $\mathbf{0 . 3} \times \mathbf{V}_{\text {cc }}$ | $V$ (max) |
| ALL DIGITAL INPUTS EXCEPT FOR BTI\# |  |  |  |  |  |
| $1 \mathrm{IN}(1)$ | Logical "1" Input Current | $\mathrm{V}_{\mathrm{IN}}=5.0 \mathrm{~V}_{\mathrm{DC}}$ | -0.005 | -1 | $\mu \mathrm{A}(\mathrm{min})$ |
| $1 \mathrm{IN}(0)$ | Logical "0"' Input Current | $\mathrm{V}_{\mathrm{IN}}=0 \mathrm{~V}_{\mathrm{DC}}$ | 0.005 | 1 | $\mu \mathrm{A}$ (max) |
| $\mathrm{C}_{\mathrm{IN}}$ | Digital Input Capacitance |  | 20 |  | pF |


| DC Electrical Characteristics (Continued) <br> The following specifications apply for $+4.25 \mathrm{~V}_{\mathrm{DC}} \leq \mathrm{V}_{\mathrm{CC}} \leq+5.75 \mathrm{~V}_{\mathrm{DC}}$, $\mathrm{f}_{\mathrm{SYSCLK}}=8.33 \mathrm{MHz}, \mathrm{R}_{\mathrm{S}}=25 \Omega$, unless otherwise specified. Boldface limits apply for $\mathbf{T}_{\mathbf{A}}=\mathbf{T}_{\mathbf{J}}=\mathbf{T}_{\mathbf{M I N}}$ to $\mathbf{T}_{\mathbf{M A X}}$; all other limits $\mathrm{T}_{\mathrm{A}}=\mathrm{T}_{\mathbf{J}}=25^{\circ} \mathrm{C}$ (Note 7). |  |  |  |  |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| Symbol | Parameter | Conditions | Typical (Note 8) |  |  | Units (Limits) |
| BIT\# DIGITAL INPUT |  |  |  |  |  |  |
| $1 \mathrm{IN}(1)$ | Logical "1" Input Current | $\mathrm{V}_{\mathrm{IN}}=5.0 \mathrm{~V}_{\mathrm{DC}}$ | 1 |  |  | $\mu \mathrm{A}$ (max) |
| $1 \mathrm{IN}(0)$ | Logical "0" Input Current | $\mathrm{V}_{\mathrm{IN}}=0 \mathrm{~V}_{\mathrm{DC}}$ | -500 |  |  | $\mu \mathrm{A}$ (max) |
| $\mathrm{Cl}_{\mathrm{IN}}$ | Digital Input Capacitance |  | 20 |  |  | pF |
| AC Electrical Characteristics <br> The following specifications apply for $+4.25 \mathrm{~V}_{\mathrm{DC}} \leq \mathrm{V}_{\mathrm{CC}} \leq+5.75 \mathrm{~V}_{\mathrm{DC}}$ unless otherwise specified. Boldface limits apply for $\mathbf{T}_{\mathbf{A}}=\mathbf{T}_{\mathbf{J}}=\mathbf{T}_{\mathbf{M I N}}$ to $\mathbf{T}_{\mathbf{M A X}}$; all other limits $\mathrm{T}_{\mathrm{A}}=\mathrm{T}_{\mathrm{J}}=25^{\circ} \mathrm{C}$ (Note 13). |  |  |  |  |  |  |
| Symbol | Parame |  | Conditions | Typical (Note 8) | Limits (Note 9) | Units (Limits) |
| ISA TIMING CHARACTERISTICS |  |  |  |  |  |  |
| $\mathrm{f}_{\text {SYSCLK }}$ | System Clock (SYSCLK) | equency |  | 8.33 |  | MHz |
| $\mathrm{t}_{\text {CS }}$ (setup) | CS \# Active to IORD \# /I | Active |  |  | 10 | ns (min) |
| $\mathrm{t}_{\text {CS }}$ (hold) | IORD\# /IOWR \# Inactive | Inactive |  |  | 10 | ns (min) |
| $t_{\text {SA }}$ (setup) | Address Valid to IORD\# | Active |  |  | 30 | ns (min) |
| tsA (hold) | IORD \# /IOWR \# Inactive | ess Invalid |  |  | 10 | ns (min) |
| ISA WRITE TIMING |  |  |  |  |  |  |
| tsDWR (setup) | Data Valid to IOWR \# Ac |  |  |  | 5 | ns (min) |
| $t_{\text {SDWR }}$ (hold) | IOWR \# Inactive to Data |  |  |  | 5 | ns (min) |
| $t_{\text {WR }}$ (setup) | IOWR \# Active to Rising | SYSCLK |  |  | 20 | ns (min) |
|  |  |  <br> SA Bus Write T | Timing Diagram | $t_{\text {SA }}$ (hold) <br> (hold) |  | TL/H/12873-4 |



AC Electrical Characteristics (Continued)
The following specifications apply for $+4.25 \mathrm{~V}_{\mathrm{DC}} \leq \mathrm{V}_{\mathrm{CC}} \leq+5.75 \mathrm{~V}_{\mathrm{DC}}$ unless otherwise specified. Boldface limits apply for $\mathbf{T}_{\mathbf{A}}=\mathbf{T}_{\mathbf{J}}=\mathbf{T}_{\text {MIN }}$ to $\mathbf{T}_{\text {MAX }}$; all other limits $\mathrm{T}_{\mathrm{A}}=\mathrm{T}_{\mathrm{J}}=25^{\circ} \mathrm{C}$ (Note 13).

| Symbol | Parameter | Conditions | Typical <br> (Note 8) | Limits <br> (Note 9) | Units <br> (Limits) |
| :---: | :---: | :---: | :---: | :---: | :---: |

SERIAL BUS TIMING CHARACTERISTICS

| $t_{1}$ | SCL (Clock) Period |  |  | $\mathbf{2 . 5}$ | $\mu \mathrm{S}(\mathrm{min})$ |
| :---: | :--- | :--- | :--- | :---: | :---: |
| $\mathrm{t}_{2}$ | Data In Setup Time to SCL High |  |  | $\mathbf{1 0 0}$ | $\mathrm{ns}(\mathrm{min})$ |
| $\mathrm{t}_{3}$ | Data Out Stable After SCL Low |  |  | $\mathbf{0}$ | $\mathrm{ns}(\mathrm{min})$ |
| $\mathrm{t}_{4}$ | SDA Low Setup Time to SCL Low (start) |  |  | $\mathbf{1 0 0}$ | $\mathrm{ns}(\mathrm{min})$ |
| $\mathrm{t}_{5}$ | SDA High Hold Time After SCL High (stop) |  |  | $\mathbf{1 0 0}$ | $\mathrm{ns}(\mathrm{min})$ |



FIGURE 3. Serial Bus Timing Diagram
Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional, but do not guarantee specific performance limits. For guaranteed specifications and test conditions, see the Electrical Characteristics. The guaranteed specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions.
Note 2: All voltages are measured with respect to GND, unless otherwise specified
Note 3: When the input voltage $\left(\mathrm{V}_{\mathrm{IN}}\right)$ at any pin exceeds the power supplies ( $\mathrm{V}_{\mathrm{IN}}<\left(\mathrm{GNDD}\right.$ or GNDA ) or $\mathrm{V}_{\mathrm{IN}}>\mathrm{V}_{\mathrm{CC}}$ ), the current at that pin should be limited to 5 mA . The 20 mA maximum package input current rating limits the number of pins that can safely exceed the power supplies with an input current of 5 mA to four.
Note 4: The maximum power dissipation must be derated at elevated temperatures and is dictated by $T_{J m a x}, \Theta_{J A}$ and the ambient temperature, $T_{A}$. The maximum allowable power dissipation at any temperature is $P_{D}=\left(T_{J} \max -T_{A}\right) / \Theta_{J A}$.
Note 5: The human body model is a 100 pF capacitor discharged through a $1.5 \mathrm{k} \Omega$ resistor into each pin. The machine model is a 200 pF capacitor discharged directly into each pin.
Note 6: See the section titled "Surface Mount" found in any post 1986 National Semiconductor Linear Data Book for other methods of soldering surface mount devices.

## AC Electrical Characteristics (Continued)

Note 7: Each input and output is protected by a nominal 6.5 V breakdown voltage zener diode to GND; as shown below, input voltage magnitude up to 0.3 V above $\mathrm{V}_{\mathrm{CC}}$ or 0.3 V below GND will not damage the LM78. There are parasitic diodes that exist between the inputs and the power supply rails. Errors in the ADC conversion can occur if these diodes are forward biased by more than 50 mV . As an example, if $\mathrm{V}_{\mathrm{CC}}$ is $4.50 \mathrm{~V}_{\mathrm{DC}}$, input voltage must be $\leq 4.55 \mathrm{~V}_{\mathrm{DC}}$, to ensure accurate conversions.

*An x indicates that the diode exists.

| Pin Name | D1 | D2 | D3 |
| :--- | :---: | :---: | :---: |
| IORD\# |  |  | x |
| IOWR\# |  |  | x |
| SYSCLK |  |  | x |
| D0-D7 | x | x | x |
| SMI_IN \# |  |  | x |
| Chassis Intrusion |  | x | x |
| Power Switch Bypass\# | x | x | x |
| FAN1-FAN3 |  |  | x |
| SCL |  |  | x |
| SDA |  | x | x |
| RESET\# |  | x | x |
| NTEST | x | x | x |


| Pin Name | D1 | D2 | D3 |
| :--- | :---: | :---: | :---: |
| -IN6 |  | x | x |
| FB6 | x | x | x |
| FB5 | x | x | x |
| -IN5 |  | x | x |
| IN4-IN0 | x | x | x |
| VID3-VID0 | x | x | x |
| BTI\# | x |  | x |
| NMI\#/IRQ\# | x | x | x |
| SMI\# |  | x | x |
| A0-A2 |  |  | x |
| CS\# |  |  | x |

## FIGURE 4. ESD Protection Input Structure

Note 8: Typicals are at $\mathrm{T}_{J}=\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$ and represent most likely parametric norm.
Note 9: Limits are guaranteed to National's AOQL (Average Outgoing Quality Level).
Note 10: TUE (Total Unadjusted Error) includes Offset, Gain and Linearity errors of the ADC and any error introduced by the amplifiers as shown in the circuit of Figure 13.
Note 11: Total Monitoring Cycle Time includes temperature conversion, 7 analog input voltage conversions and 3 tachometer readings. Each temperature and input voltage conversion takes 100 ms typical and 112 ms maximum. Fan tachometer readings take 20 ms typical, at 4400 rpm , and 200 ms max.
Note 12: The total fan count is based on 2 pulses per revolution of the fan tachometer output.
Note 13: Timing specifications are tested at the TTL logic levels, $\mathrm{V}_{\mathrm{IL}}=0.4 \mathrm{~V}$ for a falling edge and $\mathrm{V}_{\mathrm{IH}}=2.4 \mathrm{~V}$ for a rising edge. TRI-STATE output voltage is forced to 1.4 V .

## Test Circuit



FIGURE 5. Digital Output Load Circuitry

## Functional Description

### 1.0 GENERAL DESCRIPTION

The LM78 provides 7 analog inputs, a temperature sensor, a Delta-Sigma ADC (Analog-to-Digital Converter), 3 fan speed counters, WATCHDOG registers, and a variety of inputs and outputs on a single chip. Interfaces are provided for both the ISA parallel bus or Serial Bus. The LM78 performs power supply, temperature, and fan monitoring for personal computers.
The LM78 continuously converts analog inputs to 8-bit digital words with a 16 mV LSB (Least Significant Bit) weighting, yielding input ranges of from OV to 4.096 V . The two negative analog inputs provide inverting op amps, with their noninverting input referred to ground. With additional external feedback components, these inputs provide measurements of negative voltages (such as -5 V and -12 V power supplies). The analog inputs are useful for monitoring several power supplies present in a typical computer. Temperature is converted to an 8-bit two's-complement digital word with a $1^{\circ} \mathrm{C}$ LSB.
Fan inputs measure the period of tachometer pulses from the fans, providing a higher count for lower fan speeds. The fan inputs are digital inputs with an acceptable range of OV to 5 V and a transition level of approximately 1.4 V . Full scale fan counts are 255 (8-bit counter) and this represents a stopped or very slow fan. Nominal speeds, based on a count of 153, are programmable from 1100 to 8800 RPM on FAN1 and FAN2, with FAN3 fixed at 4400 RPM. Signal conditioning circuitry is included to accommodate slow rise and fall times.
The LM78 provides a number of internal registers, as detailed in Figure 6. These include:

Configuration Register: Provides control and configuration.
Interrupt Status Registers: Two registers to provide status of each WATCHDOG limit or Interrupt event.
Interrupt Mask Registers: Allows masking of individual Interrupt sources, as well as separate masking for each of both hardware Interrupt outputs.
VID/Fan Divisor Registers: A register to read the status of the VID input lines. The high bits of this register contain the divisor bits for FAN1 and FAN2 inputs.
Serial Bus Address Register: Contains the Serial Bus address. At power on it assumes the default value of 0101101 binary, and can be altered via the ISA or Serial Bus interface.
POST RAM: FIFO RAM to store up to 32 bytes of 8 -bit POST codes. Overflow of the POST RAM will set an Interrupt. The POST RAM, located at base address xOh and x 4 h , allows for easy decoding to address 80 h and 84h, the normal addresses for outputting of POST codes. Interrupt will only be set when writing to port xOh or x 4 h . The POST RAM can be read via ports 85 h and 86 h .
Value RAM: The monitoring results: temperature, voltages, fan counts, and WATCHDOG limits are all contained in the Value RAM. The Value RAM consists of a total of 64 bytes. The first 11 bytes are all of the results, the next 19 bytes are the WATCHDOG limits, and are located at $20 \mathrm{~h}-3 \mathrm{Fh}$, including two unused bytes in the upper locations. The next 32 bytes, located at 60h-7Fh, mirror the first 32 bytes with identical contents. The only
difference in the upper bytes are that they auto-increment the LM78 Internal Address Register when read from or written to via the ISA bus (auto-increment is not available for Serial Bus communications).
When the LM78 is started, it cycles through each measurement in sequence, and it continuously loops through the sequence approximately once every second. Each measured value is compared to values stored in WATCHDOG, or Limit registers. When the measured value violates the programmed limit the LM78 will set a corresponding Interrupt in the Interrupt Status Registers. Two hardware Interrupt lines, SMI\# and NMI/IRQ\#, are fully programmable with separate masking of each Interrupt source, and masking of each output. In addition, the Configuration Register has control bits to enable or disable the hardware Interrupts. Additional digital inputs are provided for chaining of SMI\# (System Management Interrupt), outputs of multiple external LM75 temperature sensors via the BTI\# (Board Temperature Interrupt) input, and a Chassis Intrusion input. The Chassis Intrusion input is designed to accept an active high signal from an external circuit that latches when the case is removed from the computer.

### 2.0 INTERFACE

The LM78 only decodes the three lowest address bits on the ISA bus. Referring to the ISA bus timing diagrams in Figure 1 and Figure 2, the Chip Select Input, CS\#, should be taken low by external address decoder circuitry to access the LM78. The LM78 decodes the following base addresses:
-Port xOh: Power On Self Test codes from ISA bus.
-Port x4h: Power On Self Test codes from ISA bus.
-Port x5h: The LM78s Internal Address Register
-Port x6h: Data Register
IORD\# is the standard ISA bus signal that indicates to the LM78 that it may drive data on to the ISA data bus.
IOWR \# is the standard ISA command to the LM78 that it may latch data from the ISA bus.
SYSCLK is the standard ISA SYSCLK, typically 8.33 MHz. This clock is used only for timing of the ISA interface of the LM78. All other clock functions within LM78 such as the ADC and fan counters are done with a separate asynchronous internal clock.
A typical application designed to utilize the POST RAM would decode the LM78 to the address space starting at 80h, which is where POST codes are output to. Otherwise, the LM78 can be decoded into a different desired address space.
To communicate with an LM78 Register, first write the address of that Register to Port x5h. Read or write data from or to that register via Port x6h. A write will take IOWR \# low, while a read will take IORD\# low.
If the Serial Bus Interface and ISA bus interface are used simultaneously there is the possibility of collision. To prevent this from occurring in applications where both interfaces are used, read port $\times 5 \mathrm{~h}$ and if the Most Significant Bit, D7, is high, ISA communication is limited to reading port $\times 5 \mathrm{~h}$ only until this bit is low. A Serial Bus communication occurring while ISA is active will not be a problem, since even a single bit of Serial Bus communication requires 10 microseconds, in comparison to less than a microsecond for an entire ISA communication.


## Functional Description (Continued)

### 2.1 Internal Registers of the LM78

TABLE I. The internal registers and their corresponding internal LM78 address is as follows:

| Register | LM78 Internal Hex <br> Address <br> (This is the data to be written to Port x5h) | Power on Value | Notes |
| :---: | :---: | :---: | :---: |
| Configuration Register | 40h | 00001000 |  |
| Interrupt Status Register 1 | 41h | 00000000 | Auto-increment to the address of Interrupt Status Register 2 after a read or write to Port x6h. |
| Interrupt Status Register 2 | 42h | 00000000 |  |
| SMI\# Mask Register 1 | 43h | 00000000 | Auto-increment to the address of SMI\# Mask Register 2 after a read or write to Port x6h. |
| SMI\# Mask Register 2 | 44h | 00000000 |  |
| NMI Mask Register 1 | 45h | 00000000 | Auto-increment to the address of NMI Mask Register 2 after a read or write to Port x6h. |
| NMI Mask Register 2 | 46h | 01000000 |  |
| VID/Fan Divisor Register | 47h | 0101XXXX | The first four bits set the divisor for Fan Counters 1 and 2. The lower four bits reflect the state of the VID inputs. |
| Serial Bus Address Register | 48h | 00101101 |  |
| POST RAM | 00h-1Fh |  | Auto-increment when written to from Port x0h or $x 4$ h. Auto-increment after a read or write to Port x 6 h , with a separate pointer. Auto-incrementing stops when address 1Fh is reached. |
| Value RAM | 20h-3Fh |  |  |
| Value RAM | 60h-7Fh |  | Auto-increment after a read or write to Port x6h. Auto-incrementing stops when address 7Fh is reached. |

## A typical communication with the LM78 would consist

 of:1. Write to Port $x 5 \mathrm{~h}$ the LM78 Internal Address (from column 2 above) of the desired register. Alternatively, when both ISA and Serial Bus interfaces are used, the first step in a communication may be to read Port $x 5 \mathrm{~h}$ to ascertain the state of the Busy bit to avoid contention with an Serial Bus communication.
2. Read or write the corresponding registers data with reads/writes from Port x6h.
The LM78 Internal Address latches, and does not have to be written if it is already pointing at the desired register. The LM78 Internal Address Register is read/write (Bit 7 is read only).

Functional Description (Continued)

(a) Serial Bus Write to the Internal Address Register followed by the Data Byte

(b) Serial Bus Write to the Internal Address Register Only

(c) Serial Bus Read from a Register with the Internal Address Register Preset to Desired Location

FIGURE 7. Serial Bus Timing

## Functional Description (Continued)

### 2.2 Serial Bus Interface

When using the Serial Bus Interface a write will always consist of the LM78 Serial Bus Interface Address byte, followed by the Internal Address Register byte, then the data byte. There are two cases for a read:

1. If the Internal Address Register is known to be at the desired Address, simply read the LM78 with the Serial Bus Interface Address byte, followed by the data byte read from the LM78.
2. If the Internal Address Register value is unknown, write to the LM78 with the Serial Bus Interface Address byte, followed by the Internal Address Register byte. Then restart the Serial Communication with a Read consisting of the Serial Bus Interface Address byte, followed by the data byte read from the LM78.
In all other respects the LM78 functions identically for Serial Bus communications as it does for ISA communications. Auto-Increment does not operate. When writing to or reading from a Register which Auto-Increments with ISA communications, the Register must be manually incremented for Serial Bus communications.
The default power on Serial Bus address for the LM78 is: 0101101 binary. This address can be changed by writing any desired value to the Serial Bus address register, which can be done either via the ISA or Serial Bus. During and Serial Bus communication on the BUSY bit (bit 7) in the address register at x 5 h will be high, and any ISA activity in that situation should be limited to reading port $x 5 h$ only.
All of these communications are depicted in the Serial Bus Interface Timing Diagrams as shown in Figure 7.

### 3.0 USING THE LM78

### 3.1 Power On

When power is first applied, the LM78 performs a "power on reset" on several of its registers. The power on condition of registers in shown in Table I. Registers whose power on values are not shown have power on conditions that are indeterminate (this includes the value RAM and WATCHDOG limits). The ADC is inactive. In most applications, usually the first action after power on would be to write WATCHDOG limits into the Value RAM.

### 3.2 Resets

Configuration Register INITIALIZATION accomplishes the same function as power on reset. The POST RAM, Value RAM conversion results, and Value RAM WATCHDOG limits are not Reset and will be indeterminate immediately after power on. If the Value RAM contains valid conversion results and/or Value RAM WATCHDOG limits have been previously set, they will not be affected by a Configuration Register INITIALIZATION. Power on reset, or Configuration Register INITIALIZATION, clear or initialize the following registers (the initialized values are shown on Table I):

Configuration Register
Interrupt Status Register 1
Interrupt Status Register 2
SMI\# Mask Register 1
SMI\# Mask Register 2

NMI Mask Register 1
NMI Mask Register 2
VID/Fan Divisor Register
Serial Bus Address Register (Power on reset only, not reset by Configuration Register INITIALIZATION)
Configuration Register INITIALIZATION is accomplished by setting Bit 7 of the Configuration Register high. This bit automatically clears after being set.

### 3.3 Using the Configuration Register

The Configuration Register provides all control over the LM78. At power on, the ADC is stopped and INT__Clear is asserted, clearing the SMI\# and NMI/IRQ\# hardwire outputs. The Configuration Register starts and stops the LM78, enables and disables interrupt outputs and modes, and provides the Reset function described in Section 3.2.
Bit 0 of the Configuration Register controls the monitoring loop of the LM78. Setting Bit 0 low stops the LM78 monitoring loop and puts the LM78 in shutdown mode, reducing power consumption. ISA and Serial Bus communication is possible with any register in the LM78 although activity on these lines will increase shutdown current, up to as much as maximum rated supply current, while the activity takes place. Taking Bit 0 high starts the monitoring loop, described in more detail subsequently.
Bit 1 of the Configuration Register enables the SMI\# Interrupt hardwire output when this bit is taken high. Similarly, Bit 2 of the Configuration Register enables the NMI/IRQ\# Interrupt hardwire output when taken high. The NMI/IRQ\# mode is determined by Bit 5 in the Configuration Register. When Bit 5 is low the output is an active low IRQ\# output. Taking Bit 5 high inverts this output to provide an active high NMI output.
The Power Switch Bypass\# provides an active low at the Power Switch Bypass\# output when set high. This is intended for use in software power control by activating an external power control MOSFET.

### 3.4 Starting Conversion

The monitoring function (Analog inputs, temperature, and fan speeds) in the LM78 is started by writing to the Configuration Register and setting INT__Clear (Bit 3), low, and Start (bit 0), high. The LM78 then performs a "round-robin" monitoring of all analog inputs, temperature, and fan speed inputs approximately once a second. The sequence of items being monitored corresponds to locations in the Value RAM and is:

1. Temperature
2. INO
3. IN1
4. IN2
5. IN3
6. IN4
7. -IN5
8. -IN6
9. Fan 1
10. Fan 2
11. Fan 3

## Functional Description (Continued)

### 3.5 Reading Conversion Results

The conversion results are available in the Value RAM. Conversions can be read at any time and will provide the result of the last conversion. Because the ADC stops, and starts a new conversion whenever it is read, reads of any single value should not be done more often then once every 120 ms . When reading all values, allow at least 1.5 seconds between reading groups of values. Reading more frequently than once every 1.5 seconds can also prevent complete updates of Interrupt Status Registers and Interrupt Output's.
A typical sequence of events upon power on of the LM78 would consist of:

1. Set WATCHDOG Limits
2. Set Interrupt Masks
3. Start the LM78 monitoring process

### 4.0 ANALOG INPUTS

The 8 -bit ADC has a 16 mV LSB, yielding a 0 V to 4.08 V (4.096-1LSB) input range. This is true for all analog inputs. In PC monitoring applications these inputs would most often be connected to power supplies. The 2.5 V and 3.3 V supplies can be directly connected to the inputs. The 5 V and 12 V inputs should be attenuated with external resistors to any desired value within the input range.
A typical application, such as is shown in Figure 8, might select the input voltage divider to provide 3 V at the analog inputs of the LM78. This is sufficiently high for good resolution of the voltage, yet leaves headroom for upward excursions from the supply of about $25 \%$. To simplify the process of resistor selection, set the value of R2 first. Select a value for R2 between $10 \mathrm{k} \Omega$ and $100 \mathrm{k} \Omega$. This is low enough to avoid errors due to input leakage currents yet high enough to both protect the inputs under overdrive conditions as well as minimize loading of the source. Then select R1 to provide a 3 V input according to:

$$
R 1=R 2\left(\frac{V_{S}}{V_{I N}}-1\right)
$$

The negative inputs provide inverting op amps with non-inverting inputs connected to ground. The output of these op amps are designed to drive the input of the LM78 and their associated feedback loops. Avoid heavy loading, long lines, and capacitive loading of greater than 100 pF with these op amps. The optimum feedback resistor (resistor from Feedback to -IN pin ) value is approximately $60 \mathrm{k} \Omega$, based on the op amp nominal output current rating of $50 \mu \mathrm{~A}$ at an output voltage of 3 V . Locate the feedback resistors as close as possible to the LM78. The recommended range for $R_{I N}$ is from $30 \mathrm{k} \Omega$ to $300 \mathrm{k} \Omega$.
Select $R_{I N}$ according to:

$$
R_{\text {IN }}=\frac{V_{S} \times R_{F}}{V_{F E E D B A C K}}
$$

The analog inputs have internal diodes that clamp inputs exceeding the power supply and ground. Exceeding any analog input has no detrimental effect on other channels. The input diodes will also clamp voltages appearing at the inputs of an un-powered LM78. External resistors should be included to limit input currents to the values given in the ABSO-

LUTE MAXIMUM RATINGS for Input Current At Any Pin. Inputs with the attenuator networks will usually meet these requirements. If it is possible for inputs without attenuators (such as the 2.5 V or 3.3 V supplies) to be turned on while LM78 is powered off, additional resistors of about $10 \mathrm{k} \Omega$ should be added in series with the inputs to limit the input current.

### 5.0 LAYOUT AND GROUNDING

Analog inputs will provide best accuracy when referred to the AGND pin. A separate, low-impedance ground plane for analog ground, which provides a ground point for the voltage dividers and analog components, will provide best performance but is not mandatory. Analog components such as voltage dividers and feedback resistors should be located physically as close as possible to the LM78.
The power supply bypass, the parallel combination of $10 \mu \mathrm{~F}$ (electrolytic or tantalum) and $0.1 \mu \mathrm{~F}$ (ceramic) bypass capacitors connected between pin 12 and ground, should also be located as close as possible to the LM78.

### 6.0 FAN INPUTS

Inputs are provided for signals from fans equipped with tachometer outputs. These are logic-level inputs with an approximate threshold of 1.4 V . Signal conditioning in the LM78 accommodates the slow rise and fall times typical of fan tachometer outputs. The maximum input signal range is 0 to $\mathrm{V}_{\mathrm{CC}}$. In the event these inputs are supplied from fan outputs which exceed 0 to $\mathrm{V}_{\mathrm{CC}}$, either resistive division or diode clamping must be included to keep inputs within an acceptable range, as shown in Figure 9. R2 is selected so that it does not develop excessive voltage due to input leakage. R1 is selected based on R2 to provide a minimum input of 2 V and a maximum of $\mathrm{V}_{\mathrm{CC}}$. R1 should be as low as possible to provide the maximum possible input up to $V_{C C}$ for best noise immunity. Alternatively, use a shunt reference or zener diode to clamp the input level.
If fans can be powered while the power to the LM78 is off, the LM78 inputs will provide diode clamping. Limit input current to the Input Current at Any Pin specification shown in the ABSOLUTE MAXIMUM RATINGS section. In most cases, open collector outputs with pull-up resistors inherently limit this current. If this maximum current could be exceeded, either a larger pull up resistor should be used or resistors connected in series with the fan inputs.
The Fan Inputs gate an internal 22.5 kHz oscillator for one period of the Fan signal into an 8 -bit counter (maximum count $=255$ ). The default divisor, located in the VID/Fan Divisor Register, is set to 2 (choices are 1, 2, 4, and 8) providing a nominal count of 153 for a 4400 rpm fan with two pulses per revolution. Typical practice is to consider $70 \%$ of normal RPM a fan failure, at which point the count will be 219 .
Determine the fan count according to:

$$
\text { Count }=\frac{1.35 \times 10^{6}}{\text { RPM } \times \text { Divisor }}
$$

Note that Fan 1 and Fan 2 Divisors are programmable via the VID/Fan Divisor Register. Fan 3 is not adjustable, and its Divisor is always set to 2.

Functional Description (Continued)

| Voltage Measurements $\left(\mathbf{V}_{\mathbf{S}}\right)$ | $\mathbf{R 1}$ or $\mathbf{R}_{\mathbf{I N}}$ | R2 or $\mathbf{R}_{\mathbf{F}}$ | Voltage at Analog Inputs |
| :---: | :---: | :---: | :---: |
| +2.50 V | 0 | NONE | +2.50 V |
| +3.30 V | 0 | NONE | +3.30 V |
| +5 V | $6.8 \mathrm{k} \Omega$ | $10 \mathrm{k} \Omega$ | +2.98 V |
| +12 V | $30 \mathrm{k} \Omega$ | $10 \mathrm{k} \Omega$ | +3.00 V |
| -12 V | $240 \mathrm{k} \Omega$ | $60 \mathrm{k} \Omega$ | +3.00 V |
| -5 V | $100 \mathrm{k} \Omega$ | $60 \mathrm{k} \Omega$ | +3.00 V |



TL/H/12873-13
FIGURE 8. Input Examples. Resistor Values Shown Provide Approximately 3V at the Analog Inputs


## Functional Description (Continued)

7.0 TEMPERATURE MEASUREMENT SYSTEM

The LM78 bandgap type temperature sensor and ADC perform 8 -bit two's-complement conversions of the tempera-
ture. A digital comparator is also incorporated that compares the readings to the user-programmable Overtemperature setpoint and Hysteresis values.


FIGURE 10. Temperature-to-Digital Transfer Function (Non-Linear Scale for Clarity)

## Functional Description (Continued)

### 7.1 Temperature Interrupts

The normal mode for temperature interrupts in the LM78 is an "Interrupt"mode operating in the following way: Exceeding $\mathrm{T}_{\mathrm{O}}$ causes an interrupt that will remain active indefinitely until reset by reading Interrupt Status Register 1. Once an interrupt event has occurred by crossing $T_{\text {OII }}$, then reset, an interrupt will only occur again by the temperature going below THYST. Again, it will remain active indefinitely until being reset by reading Interrupt Status Register 1.

*Note: Interrupt resets occur only when interrupt Status Register 1 is read. (a) Interrupt Mode

A "Comparator" mode for temperature interrupts can be made available by setting the $\mathrm{T}_{\mathrm{HYST}}$ limit to $127^{\circ} \mathrm{C}$. This results in a simple "thermostat" type of function where an interrupt will be set whenever the temperature exceeds the TOI limit. Reading Interrupt Status Register 1 will clear the interrupt as usual, but the interrupt will set again after the completion of another measurement cycle. It will remain set until the temperature goes below the $\mathrm{T}_{\mathrm{O}}$ limit (allow up to two measurement cycles for clearing after descending below $\mathrm{T}_{\mathrm{O}}$ while in Comparator mode).


Interrupt resets occur when Interrupt Status Register 1 is read but will set again when monitoring cycle continues (as long as temperature exceeds $\left.\mathrm{T}_{\mathrm{OI}}\right)$. When temperature descends below $\mathrm{T}_{\mathrm{OI}}$ allow up to two monitoring loops before the Temperature Interrupt resets.
(b) Comparator Mode

FIGURE 11. Temperature Interrupt Response Diagram

## Functional Description (Continued)

### 7.2 Temperature Data Format

Temperature data can be read from the Temperature, $\mathrm{T}_{\mathrm{O}}$ Set Point, and $T_{\text {HYST }}$ Set Point registers; and written to the $\mathrm{T}_{\text {OI }}$ Set Point, and $\mathrm{T}_{\text {HYST }}$ Set Point registers. Temperature data is represented by an 8-bit, two's complement word with an LSB (Least Significant Bit) equal to $1.0^{\circ} \mathrm{C}$ :

| Temperature | Digital Output |  |
| :---: | :---: | :---: |
|  | Binary | Hex |
| $+125^{\circ} \mathrm{C}$ | 01111101 | 7 Dh |
| $+25^{\circ} \mathrm{C}$ | 00011001 | 19 h |
| $+1.0^{\circ} \mathrm{C}$ | 00000001 | 01 h |
| $+0^{\circ} \mathrm{C}$ | 00000000 | 00 h |
| $-1.0^{\circ} \mathrm{C}$ | 11111111 | FFh |
| $-25^{\circ} \mathrm{C}$ | 11100111 | E7h |
| $-55^{\circ} \mathrm{C}$ | 11001001 | C 9 h |

### 8.0 THE LM78 INTERRUPT STRUCTURE

Figure 12 depicts the Interrupt Structure of the LM78. The LM78 can generate Interrupts as a result of each of its internal WATCHDOG registers on the analog, temperature, and fan inputs. Overflow of the POST RAM (greater than 32 bytes written to POST RAM) will also cause an Interrupt.
External Interrupts can come from the following three sources. While the labels suggest a specific type or source of Interrupt, these labels are not restrictions of their usage, and they could come from any desired source:
BTI\#: This is an active low Interrupt intended to come from the O.S. output of LM75 temperature sensors. The LM75 O.S. output goes active when its temperature exceeds a programmed threshold. Up to 8 LM75's can be connected to a single Serial Bus bus with their O.S. output's wire or'd to the BTI\# input of the LM78. If the temperature of any LM75 exceeds its programmed limit, it drives BTI\# low. This generates an Interrupt to notify the host of a possible overtemperature condition. Provides an internal pull-up of $10 \mathrm{k} \Omega$.

Chassis Intrusion: This is an active high interrupt from any type of device that detects and captures chassis intrusion violations. This could be accomplished mechanically, optically, or electrically, and circuitry external to the LM78 is expected to latch the event. The design of the LM78 allows this input to go high even with no power applied to the LM78, and no clamping or other interference with the line will occur. This line can also be pulled low for at least 20 ms by the LM78 to reset a typical Chassis Intrusion circuit. Accomplish this reset by setting Bit 7 of NMI Mask Register 2 high. The bit in the Register is self-clearing.
SMI_IN \#: This active low Interrupt merely provides a way to chain the SMI\# Interrupt from other devices through the LM78 to the processor.
All Interrupts are indicated in the two Interrupt Status Registers. The NMI/IRQ\# and SMI\# outputs have individual mask registers, and individual masks for each Interrupt. As described in Section 3.3, these two hardware Interrupt lines can also be enabled/disabled in the Configuration Register. The Configuration Register is also used to set the mode of the NMI/IRQ\# Interrupt line.

### 8.1 Interrupt Clearing

Reading the Interrupt Status Register will output the contents of the Register, and reset the Register. A subsequent read done before the analog "round-robin" monitoring loop is complete will indicate a cleared Register. Allow at least 1.5 seconds to allow all Registers to be updated between reads. In summary, the Interrupt Status Register clears upon being read, and requires at least 1.5 seconds to be updated. When the Interrupt Status Register clears, the hardware interrupt line will also clear until the Registers are updated by the monitoring loop.
The hardware Interrupt lines are cleared with the INT__Clear bit, which is Bit 3 of the Configuration Register. When this bit is high, the LM78 monitoring loop will stop. It will resume when the bit is low.


## Functional Description (Continued)

### 9.0 RESET\# AND Power Switch Bypass\# OUTPUTS

In PC applications the Power Switch Bypass\# provides a gate drive signal to an external P-channel MOSFET power switch. This external MOSFET then would keep power turned on regardless of the state of front panel power switches when software power control is used. In any given application this signal is not limited to the function described by its label. For example, since the LM78 incorporates temperature sensing, the Power Switch Bypass\# output could also be utilized to control power to a cooling fan. Take Power Switch Bypass\# active low by setting Bit 6 in the Configuration Register high.
RESET\# is intended to provide a master reset to devices connected to this line. SMI\# Mask Register 2, Bit 7, must be set high to enable this function. Setting Bit 4 in the Configuration Register high outputs a least 20 ms low on this line, at the end of which Bit 4 in the Configuration Register automatically clears. Again, the label for this pin is only its suggested use. In applications where the RESET \# capability is not needed it can be used for any type of digital control that requires a 20 ms active low open drain output.

### 10.0 POST RAM

The POST RAM is located at address $x 0 h$ and $x 4 h$, which typical address decoders will decode to 80 h or 84 h , where the BIOS will output Power On Self Test codes. A write to the POST RAM auto-increments the internal pointer of the LM78. Up to 32 bytes may be stored. An excess of 32 bytes will generate an Interrupt and stop incrementing.
The POST RAM is read as like any other register at Ports x 5 h and x 6 h , with the POST RAM located at the LM78 Internal Address from 00h to 1Fh. Reading the POST RAM via $x 6 h$ will also auto-increment, but this is a separate pointer than the one used for ports 80 h and 84 h .

### 11.0 NAND TREE TESTS

A NAND tree is provided in the LM78 for Automated Test Equipment (ATE) board level connectivity testing. NAND
tree tests are accomplished in either power on reset or Configuration Register reset state, with the Start Bit, Bit 0 of the Configuration Register low, and the INT__Clear (Bit 3) high. In this mode, forcing the SMI\# output low takes all pins except Power Switch Bypass \#, RESET \#, -IN5, -IN6, VCC, GNDA, and GNDD to a high impedance (either TRI-STATE or open drain) state. All high impedance pins can be taken to 0 and $V_{C C}$ to accomplish NAND tree tests.
To perform a NAND tree test all pins included in the NAND tree should be driven to 1 . Each individual pin (excluding the aforementioned exceptions) can be toggled and the resulting toggle observed on the NTEST pin. Allow for a typical propagation delay of 200 ns .
12.0 FAN MANUFACTURERS

Manufacturers of cooling fans with tachometer outputs are listed below:
NMB Tech
9730 Independence Ave.
Chatsworth, California 91311
818 341-3355
818 341-8207

| Model Number | Frame Size | Airflow CFM |
| :---: | :---: | :---: |
| $\mathbf{2 4 0 8 N L}$ | 2.36 in sq. $\times 0.79$ in <br> $(60 \mathrm{~mm}$ sq. $\times 20 \mathrm{~mm})$ | $9-16$ |
| $\mathbf{2 4 1 0 M L}$ | 2.36 in sq. $\times 0.98$ in <br> $(60 \mathrm{~mm}$ sq. $\times 25 \mathrm{~mm})$ | $14-25$ |
| $\mathbf{3 1 0 8 N L}$ | $3.15 \mathrm{in} \mathrm{sq}. \times 0.79 \mathrm{in}$ <br> $(80 \mathrm{~mm}$ sq. $\times 20 \mathrm{~mm})$ | $25-42$ |
| $\mathbf{3 1 1 0 K L}$ | $3.15 \mathrm{in} \mathrm{sq} \times$.0.98 in <br> $(80 \mathrm{~mm}$ sq. $\times 25 \mathrm{~mm})$ | $25-40$ |

Mechatronics Inc.
P.O. Box 20

Merrer Island, WA 98040
800 453-4569
Various sizes available with tach output option.
Sanyo Denki/Keymarc Electronics
2310 205th, Suite 101
Torrance, CA 90501
310 212-7724
109P Series.

## Functional Description (Continued)

### 13.0 REGISTERS AND RAM

13.1 Address Register (Port $\times 5 \mathrm{~h}$ )

The main register is the ADDRESS Register located at Port x 5 h . The bit designations are as follows:

| Bit | Name | Read/Write | Description |  |  |  |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| 6-0 | Address Pointer | Read/Write | Address of RAM and Registers. See the tables below for detail. |  |  |  |  |  |
| 7 | Busy | Read Only | A one indicates the device is busy because of a Serial Bus transaction or another ISA bus transaction. With checking this bit, multiple ISA drivers can use LM78 without interfering with each other or a Serial Bus driver. <br> It is the user's responsibility not to have a Serial Bus and ISA bus operations at the same time. <br> This bit is: <br> Set: with a write to Port $x 5 h$ or when a Serial Bus transaction is in progress. <br> Reset: with a write or read from Port $\times 6 \mathrm{~h}$ if it is set by a write to Port x 5 h , or when the Serial Bus transaction is finished. |  |  |  |  |  |
| Bit 7 |  | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
| Busy <br> (Power On default 0) |  | Address Pointer (Power On default 00h) |  |  |  |  |  |  |
|  |  | A6 | A5 | A4 | A3 | A2 | A1 | A0 |


| Address Pointer Index (A6-A0) |  |  |  |
| :--- | :--- | :--- | :--- |
| Registers and RAM | A6-A0 in Hex | Power On Value of Registers: <br> $<7: 0>$ in Binary | Notes |
| Configuration Register | 40 h | 00001000 | Auto-increment to the address of Interrupt <br> Status Register 2 after a read or write to Port <br> x6h. |
| Interrupt Status Register 1 | 41 h | 00000000 | Auto-increment to the address of SMI \# Mask <br> Register 2 after a read or write to Port x6h. |
| Interrupt Status Register 2 | 42 h | 00000000 |  |
| SMI \# Mask Register 1 | 43 h | 00000000 | Auto-increment to the address of NMI Mask <br> Register 2 after a read or write to Port x6h. |
| SMI\# Mask Register 2 | 44 h | 00000000 | 00000000 |
| NMI Mask Register 1 | 45 h | 01000000 | $<7: 4>=0101 ;$ <br> $<3: 0>=$ VID3-VID0 |
| NMI Mask Register 2 | 46 h | $<6: 0>=0101101 ;$ <br> $<7>=0$ | Auto-increment to the next location after a read <br> or write to Port x6h and stop at 1Fh. |
| VID/Fan Divisor Register | 47 h |  |  |
| Serial Bus Address Register | 48 h | Auto-increment to the next location after a read <br> or write to Port x6h and stop at 7Fh. |  |
| POST RAM | $00-1 \mathrm{Fh}$ | $20-3 F h$ | $60-7 \mathrm{Fh}$ |
| Value RAM |  |  |  |

## Functional Description (Continued)

13.2 Data Register (Port x6h)

Power on default $\langle 7: 0\rangle=00 \mathrm{~h}$

| Bit | Name | Read/Write | Description |
| :---: | :--- | :--- | :--- |
| $7-0$ | Data | Read/Write | Data to be read from or to be written to RAM and Register. |

13.3 Configuration Register-Address 40h

Power on default $\langle 7: 0\rangle=00001000$ binary

| Bit | Name | Read/Write | Description |
| :---: | :--- | :--- | :--- |
| 0 | Start | Read/Write | A one enables startup of monitoring operations, a zero puts the part in standby mode. <br> Note: The outputs of Interrupt pins will not be cleared if the user writes a zero to this <br> location after an interrupt has occurred unlike "INT_Clear" bit. |
| 1 | SMI\# Enable | Read/Write | A one enables the SMI\# Interrupt output. |
| 2 | NMI/IRQ\# Enable | Read/Write | A one enables the NMI/IRQ\# Interrupt output. |
| 3 | INT_Clear | Read/Write | A one disables the SMI\# and NMI/IRQ\# outputs without affecting the contents of <br> Interrupt Status Registers. The device will stop monitoring. It will resume upon clearing <br> of this bit. |
| 4 | RESET\# | Read/Write | A one outputs at least a 20 ms active low reset signal at RESET\# if <7> $=1$ in SMI\# <br> Mask Register 2. This bit is cleared once the pulse has gone inactive. |
| 5 | NMI/IRQ\# Select | Read/Write | A one selects NMI, and a zero selects IRQ\#. |
| 6 | Power Switch <br> Bypass\# | Read/Write | A one in this bit drives a zero on Power Switch Bypass\# pin. |
| 7 | INITIALIZATION | Read/Write | A one restores power on default value to all registers except the Serial Bus Address <br> register. This bit clears itself since the power on default is zero. |

13.4 Interrupt Status Register 1—Address 41h

Power on default $\langle 7: 0\rangle=00 \mathrm{~h}$

| Bit | Name | Read/Write |  |
| :---: | :--- | :--- | :--- |
| 0 | IN0 | Read Only | A one indicates a High or Low limit has been exceeded. |
| 1 | IN1 | Read Only | A one indicates a High or Low limit has been exceeded. |
| 2 | IN2 | Read Only | A one indicates a High or Low limit has been exceeded. |
| 3 | IN3 | Read Only | A one indicates a High or Low limit has been exceeded. |
| 4 | Temperature | Read Only | A one indicates a High or Low limit has been exceeded. |
| 5 | BTI\# | Read Only | A one indicates an interrupt has occurred from the Board Temperature Interrupt (BTI\#) input <br> (O.S. output of multiple LM75 chips). |
| 6 | FAN1 | Read Only | A one indicates the fan count limit has been exceeded. |
| 7 | FAN2 | Read Only | A one indicates the fan count limit has been exceeded. |

Functional Description (Continued)
13.5 Interrupt Status Register 2—Address 42h

Power on default <7:0> $=00 \mathrm{~h}$

| Bit | Name | Read/Write |  |
| :---: | :--- | :--- | :--- |
| 0 | IN4 | Read Only | A one indicates a High or Low limit has been exceeded. |
| 1 | -IN5 | Read Only | A one indicates a High or Low limit has been exceeded. |
| 2 | -IN6 | Read Only | A one indicates a High or Low limit has been exceeded. |
| 3 | FAN3 | Read Only | A one indicates the fan count limit has been exceeded. |
| 4 | Chassis Intrusion | Read Only | A one indicates Chassis Intrusion has gone high. |
| 5 | FIFO Overflow | Read Only | A one indicates an overflow in FIFO (POST RAM) i.e. 32nd location in FIFO has been <br> written via Port xOh or x4h. |
| 6 | SMI_IN\# | Read Only | A one indicates SMI__IN\# has gone low. |
| 7 | Reserved | Read Only |  |

13.6 SMI \# Mask Register 1—Address 43h

Power on default $\langle 7: 0\rangle=00 \mathrm{~h}$

| Bit | Name | Read/Write | Description |
| :---: | :--- | :--- | :--- |
| 0 | IN0 | Read/Write | A one disables the corresponding interrupt status bit for SMI\# interrupt. |
| 1 | IN1 | Read/Write | A one disables the corresponding interrupt status bit for SMI\# interrupt. |
| 2 | IN2 | Read/Write | A one disables the corresponding interrupt status bit for SMI\# interrupt. |
| 3 | IN3 | Read/Write | A one disables the corresponding interrupt status bit for SMI\# interrupt. |
| 4 | Temperature | Read/Write | A one disables the corresponding interrupt status bit for SMI\# interrupt. |
| 5 | BTI\# | Read/Write | A one disables the corresponding interrupt status bit for SMI\# interrupt. |
| 6 | FAN1 | Read/Write | A one disables the corresponding interrupt status bit for SMI\# interrupt. |
| 7 | FAN2 | Read/Write | A one disables the corresponding interrupt status bit for SMI\# interrupt. |

## Functional Description (Continued)

13.7 SMI \# Mask Register 2—Address 44h

Power on default $\langle 7: 0\rangle=00 \mathrm{~h}$

| Bit | Name | Read/Write | Description |
| :---: | :--- | :--- | :--- |
| 0 | IN4 | Read/Write | A one disables the corresponding interrupt status bit for SMI \# interrupt. |
| 1 | -IN5 | Read/Write | A one disables the corresponding interrupt status bit for SMI \# interrupt. |
| 2 | -IN6 | Read/Write | A one disables the corresponding interrupt status bit for SMI \# interrupt. |
| 3 | FAN3 | Read/Write | A one disables the corresponding interrupt status bit for SMI\# interrupt. |
| 4 | Chassis Intrusion | Read/Write | A one disables the corresponding interrupt status bit for SMI \# interrupt. |
| 5 | FIFO Overflow | Read/Write | A one disables the corresponding interrupt status bit for SMI \# interrupt. |
| 6 | SMI_IN\# | Read/Write | A one disables the corresponding interrupt status bit for SMI \# interrupt. |
| 7 | RESET\# Enable | Read/Write | $<7>=1$ in SMI \# Mask Register 2 enables the RESET\# in the Configuration Register. |

13.8 NMI Mask Register 1—Address 45h

Power on default <7:0> $=00 \mathrm{~h}$

| Bit | Name | Read/Write | Description |
| :---: | :--- | :--- | :--- |
| 0 | IN0 | Read/Write | A one disables the corresponding interrupt status bit for NMI/IRQ\# interrupt. |
| 1 | IN1 | Read/Write | A one disables the corresponding interrupt status bit for NMI/IRQ\# interrupt. |
| 2 | IN2 | Read/Write | A one disables the corresponding interrupt status bit for NMI/IRQ\# interrupt. |
| 3 | IN3 | Read/Write | A one disables the corresponding interrupt status bit for NMI/IRQ\# interrupt. |
| 4 | Temperature | Read/Write | A one disables the corresponding interrupt status bit for NMI/IRQ\# interrupt. |
| 5 | BTI\# | Read/Write | A one disables the corresponding interrupt status bit for NMI/IRQ\# interrupt. |
| 6 | FAN1 | Read/Write | A one disables the corresponding interrupt status bit for NMI/IRQ\# interrupt. |
| 7 | FAN2 | Read/Write | A one disables the corresponding interrupt status bit for NMI/IRQ\# interrupt. |

Functional Description (Continued)
13.9 NMI Mask Register 2—Address 46h

Power on <7:0> $=01000000$ binary

| Bit | Name | Read/Write | Description |
| :---: | :--- | :--- | :--- |
| 0 | IN4 | Read/Write | A one disables the corresponding interrupt status bit for NMI/IRQ\# interrupt. |
| 1 | -IN5 | Read/Write | A one disables the corresponding interrupt status bit for NMI/IRQ\# interrupt. |
| 2 | -IN6 | Read/Write | A one disables the corresponding interrupt status bit for NMI/IRQ\# interrupt. |
| 3 | FAN3 | Read/Write | A one disables the corresponding interrupt status bit for NMI/IRQ\# interrupt. |
| 4 | Chassis Intrusion | Read/Write | A one disables the corresponding interrupt status bit for NMI/IRQ\# interrupt. |
| 5 | FIFO Overflow | Read/Write | A one disables the corresponding interrupt status bit for NMI/IRQ\# interrupt. |
| 6 | SMI_IN\# | Read/Write | A one disables the corresponding interrupt status bit for NMI/IRQ\# interrupt. <br> Note: The Power on default is $\mathbf{1}$ for this bit. |
| 7 | Chassis Clear | Read/Write | A one outputs a minimum 20 ms active low pulse on the Chassis Intrusion pin. The <br> register bit self clears after the pulse has been output. |

13.10 VID/Fan Divisor Register—Address 47h

Power on $-<7: 4>$ is 0101, and $<3: 0>$ is mapped to VID $<3: 0>$

| Bit | Name | Read/Write | Description |
| :---: | :---: | :---: | :---: |
| 3-0 | VID <3:0> | Read Only | The VID $<3$ :0> inputs |
| 5-4 | FAN1 RPM Control | Read/Write | FAN1 Speed Control. $\begin{aligned} & <5: 4>=00-\text { divide by } 1 ; \\ & <5: 4>=01-\text { divide by } 2 ; \\ & <5: 4>=10-\text { divide by } 4 ; \\ & <5: 4>=11 \text { - divide by } 8 . \end{aligned}$ |
| 7-6 | FAN2 RPM Control | Read/Write | FAN2 Speed Control. $\begin{aligned} & <7: 6>=00-\text { divide by } 1 ; \\ & <7: 6>=01 \text { - divide by } 2 ; \\ & <7: 6>=10-\text { divide by } 4 ; \\ & <7: 6>=11 \text { - divide by } 8 . \end{aligned}$ |

13.11 Serial Bus Address Register—Address 48h

Power on default Serial Bus address $\langle 6: 0\rangle=0101101$ and $<7\rangle=0$ binary

| Bit | Name | Read/Write |  | Description |
| :---: | :--- | :--- | :--- | :--- |
| $6-0$ | Serial Bus Address | Read/Write | Serial Bus address $\langle 6: 0\rangle$ |  |
| 7 | Reserved | Read Only |  |  |

## Functional Description (Continued)

13.12 POST RAM—Address 00 h -1Fh

The address pointer for the POST RAM auto-increments when written to at Port x0h or x 4 h . Once the address pointer reaches 1Fh, a FIFO overflow interrupt will be generated and the FIFO will stop incrementing. Normal reads via Port $x 5 \mathrm{~h}$ and x 6 h auto-increment a separate pointer, and will not cause a FIFO overflow interrupt.

| Address A6-A0 | Address A6-A0 with Auto-Increment | Description |
| :---: | :---: | :---: |
| 20h | 60h | INO reading |
| 21h | 61h | IN1 reading |
| 22h | 62h | IN2 reading |
| 23h | 63h | IN3 reading |
| 24h | 64h | IN4 reading |
| 25h | 65h | -IN5 reading |
| 26h | 66h | -IN6 reading |
| 27h | 67h | Temperature reading |
| 28h | 68h | FAN1 reading <br> Note: This location stores the number of counts of the internal clock per revolution. |
| 29h | 69h | FAN2 reading <br> Note: This location stores the number of counts of the internal clock per revolution. |
| 2 Ah | 6Ah | FAN3 reading <br> Note: This location stores the number of counts of the internal clock per revolution. |
| 2Bh | 6Bh | INO High Limit |
| 2Ch | 6Ch | INO Low Limit |
| 2Dh | 6Dh | IN1 High Limit |
| 2Eh | 6Eh | IN1 Low Limit |
| 2Fh | 6Fh | IN2 High Limit |
| 30h | 70h | IN2 Low Limit |
| 31 h | 71h | IN3 High Limit |
| 32h | 72h | IN3 Low Limit |
| 33h | 73h | IN4 High Limit |
| 34h | 74h | IN4 Low Limit |
| 35h | 75h | -IN5 High Limit |
| 36h | 76h | -IN5 Low Limit |
| 37h | 77h | -IN6 High Limit |
| 38h | 78h | -IN6 Low Limit |
| 39h | 79h | Over Temperature Limit (High) |
| 3Ah | 7Ah | Temperature Hysteresis Limit (Low) |
| 3 Bh | 7Bh | FAN1 Fan Count Limit <br> Note: It is the number of counts of the internal clock for the Low Limit of the fan speed. |

## Functional Description (Continued)

13.13 Value RAM—Address 20h-3Fh or 60h-7Fh (auto-increment) (Continued)

| Address A6-A0 | Address A6-A0 <br> with Auto-Increment | Description |
| :---: | :---: | :--- |
| 3 Ch | 7 Ch | FAN2 Fan Count Limit <br> Note: It is the number of counts of the internal clock for the Low Limit of the fan <br> speed. |
| 3 Dh | 7 Dh | FAN3 Fan Count Limit <br> Note: It is the number of counts of the internal clock for the Low Limit of the fan <br> speed. |
| $3 E-3 F h$ | RE-7Fh | Reserved |

Setting all ones to the high limits for voltages and fans (0111 1111 binary for temperature) means interrupts will never be generated except the case when voltages go below the low limits.
Note: For the high limits of the voltages, the device is doing a greater than comparison. For the low limits, however, it is doing a less than or equal comparison.

## Typical Application



FIGURE 13. In this PC application the LM78 monitors temperature, fan speed for 3 fans, and 7 power supply voltages. It also monitors the O.S. Output of up to 8 LM75 digital temperature sensors as well as an optical chassis intrusion detector.

Physical Dimensions inches (millimeters) unless otherwise noted


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| :---: | :---: | :---: | :---: |

## LM79 Microprocessor System Hardware Monitor

## General Description

The LM79 is a highly integrated Data Acquisition system for hardware monitoring of servers, Personal Computers, or virtually any microprocessor based system. In a PC, the LM79 can be used to monitor power supply voltages, temperatures, and fan speeds. Actual values for these inputs can be read at any time, and programmable WATCHDOG limits in the LM79 activate a fully programmable and maskable interrupt system with two outputs.
The LM79 has an on-chip temperature sensor, 5 positive analog inputs, two inverting inputs (for monitoring negative voltages), and an 8-bit ADC. An input is provided for the overtemperature outputs of additional temperature sensors and this is linked to the interrupt system. The LM79 provides inputs for three fan tachometer outputs. Additional inputs are provided for Chassis Intrusion detection circuits, VID monitor inputs, and chainable interrupt. The LM79 provides both ISA and Serial Bus interfaces. A 32-byte auto-increment RAM is provided for POST (Power On Self Test) code storage.
Compared to LM78, the LM79 has the following differences:

Features

- Temperature sensing
- 5 positive voltage inputs
- 2 op amps for negative voltage monitoring
- 3 fan speed monitoring inputs
$\square$ Input for additional temperature sensors
- Chassis Intrusion Detector input

WATCHDOG comparison of all monitored values

- POST code storage RAM
$\square$ ISA and $I^{2} \mathrm{C}^{\circledR}$ Serial Bus interfaces
Provides VID0 - VID4
Key Specifications
- Voltage monitoring accuracy
$\pm 1 \%$ (max)
- Temperature Accuracy $-10^{\circ} \mathrm{C}$ to $+100^{\circ} \mathrm{C}$
$\pm 3^{\circ} \mathrm{C}$ (max)
Supply Voltage
Supply Current
Operating: 1 mA typ
Shutdown: $10 \mu \mathrm{~A}$ typ
- ADC Resolution

8 Bits

## Applications

$\square$ System Hardware Monitoring for Servers and PCs

- Office Electronics
- Electronic Test Equipment and Instrumentation
- an additional VID input pin
- an additional register for device identification
- open drain Power Switch Bypass\# Output



## Ordering Information

| $\begin{array}{c}\text { Temperature Range } \\ -10^{\circ} \mathbf{C} \leq \mathrm{T}_{A} \leq+100^{\circ} \mathrm{C}\end{array}$ | Package |
| :---: | :---: |
| LM79CCVF | VGZ44A |

## Connection Diagram



## Block Diagram



## Pin Description

| Pin Name(s) | Pin Numbers | Number of Pins | Type | Description |
| :---: | :---: | :---: | :---: | :---: |
| IORD\# | 1 | 1 | Digital Input | An active low standard ISA bus I/O Read Control. |
| IOWR\# | 2 | 1 | Digital Input | An active low standard ISA bus I/O Write Control. |
| SYSCLK | 3 | 1 | Digital Input | The reference clock for the ISA bus. Typically ranges from 4.167 MHz to 8.33 MHz . The minimum clock frequency this input can handle is 1 Hz . |
| D7-D0 | 4-11 | 8 | Digital I/O | Bi-directional ISA bus Data lines. D0 corresponds to the low order bit, with D7 the high order bit. |
| $\mathrm{V}_{\mathrm{CC}}(+5 \mathrm{~V})$ | 12 | 1 | POWER | $+5 \mathrm{~V} \mathrm{~V}_{\text {cc }}$ power. Bypass with the parallel combination of $10 \mu \mathrm{~F}$ (electrolytic or tantalum) and $0.1 \mu \mathrm{~F}$ (ceramic) bypass capacitors. |
| GNDD | 13 | 1 | GROUND | Internally connected to all digital circuitry. |
| SMI_IN\# | 14 | 1 | Digital Input | Chainable SMI\# (System Management Interrupt) Input. This is an active low input that propagates the SMI\# signal to the SMI\# output of the LM79 via SMI\# Mask Register Bit 6 and SMI\# enable Bit 1 of the Configuration Register. |
| Chassis Intrusion | 15 | 1 | Digital I/O | An active high input from an external circuit which latches a Chassis Intrusion event. This line can go high without any clamping action regardless of the powered state of the LM79. The LM79 provides an internal open drain on this line, controlled by Bit 7 of NMI Mask Register 2, to provide a minimum 20 ms reset of this line. |
| Power <br> Switch Bypass\# | 16 | 1 | Digital Output | An active low open drain output intended to drive an external P-channel power MOSFET for software power control. |
| FAN3-FAN1 | 17-19 | 3 | Digital Input | 0 to +5 V amplitude fan tachometer input. |
| SCL | 20 | 1 | Digital Input | Serial Bus Clock. |
| SDA | 21 | 1 | Digital I/O | Serial Bus bidirectional Data. |
| RESET\# | 22 | 1 | Digital Output | Master Reset, 5 mA driver (open drain), active low output with a 20 ms minimum pulse width. Available when enabled via Bit 7 in SMI\# Mask Register 2. |
| VID4/NTEST | 23 | 1 | Digital Input/Test Output | By default an input for the VID4 voltage supply readout from the P6. Can be programed as a Totem-pole output that allows NAND Tree board-level connectivity testing. Refer to Section 11.0 on NAND Tree testing. |
| GNDA | 24 | 1 | GROUND | Internally connected to all analog circuitry. The ground reference for all analog inputs. |
| -IN6 | 25 | 1 | Analog Input | Ground-referred inverting op amp input. Refer toSection 4.0, "ANALOG INPUTS". |
| FB6 | 26 | 1 | Analog Output | Output of inverting op amp for Input 6. Refer to Section 4.0, "ANALOG INPUTS". |
| FB5 | 27 | 1 | Analog Output | Output of inverting op amp for Input 5. Refer to Section 4.0, "ANALOG INPUTS". |
| -IN5 | 28 | 1 | Analog Input | Ground-referred inverting op amp input. Refer to Section 4.0, "ANALOG INPUTS". |
| IN4-IN0 | 29-33 | 1 | Analog Input | 0 to 4.096 V FSR Analog Inputs. |
| VID3-VID0 | 34-37 | 4 | Digital Input | Voltage Supply readouts from P6. This value is read in the VID/Fan Divisor Register. |
| BTI\# | 38 | 1 | Digital Input | Board Temperature Interrupt driven by O.S. outputs of additional temperature sensors such as LM75. Provides internal pull-up of $10 \mathrm{k} \Omega$. |
| NMI\#/IRQ\# | 39 | 1 | Digital Output | Non-Maskable Interrupt (open source)/Interrupt Request\# (open drain). The mode is selected with Bit 5 of the Configuration Register and the output is enabled when Bit 2 of the Configuration Register is set to 1 . The default state is disabled and IRQ\# mode. |
| SMI\# | 40 | 1 | Digital Output | System Management Interrupt (open drain). This output is enabled when Bit 1 in the Configuration Register is set to 1 . The default state is disabled. If this pin is taken low before the first write to the configuration register the NTEST mode will be enabled (See Section 11.0 or NAND Tree testing). |
| A2-A0 | 41-43 | 3 | Digital Input | The three lowest order bits of the 16-bit ISA Address Bus. A0 corresponds to the lowest order bit. |
| CS\# | 44 | 1 | Digital Input | Chip Select input from an external decoder which decodes high order address bits on the ISA Address Bus. This is an active low input. |
| TOTAL PINS |  | 44 |  |  |



Operating Ratings (Notes 1 \& 2)

| Operating Temperature Range |  |
| :---: | :---: |
| LM79 | $-55^{\circ} \mathrm{C} \leq \mathrm{T}_{\mathrm{A}} \leq+125$ |
| Specified Temperature Range | $\mathrm{T}_{\text {MIN }} \leq \mathrm{T}_{\mathrm{A}} \leq \mathrm{T}_{\mathrm{M}}$ |
| LM79 | $-10^{\circ} \mathrm{C} \leq \mathrm{T}_{\mathrm{A}} \leq+100$ |
| Junction to Ambient Thermal Resistance ( $\Theta_{\mathrm{JA}}$ (Note 4)) |  |
| NS Package ID: VGZ44A | $62^{\circ} \mathrm{C}$ |
| upply Voltage( $\mathrm{V}_{\mathrm{CC}}$ ) | +4.25 V to +5.75 |
| Ground Difference (\|GNDD-GNDA|) | $\leq 100$ |
| $\mathrm{V}_{\text {IN }}$ Voltage Range | -0.05 V to $\mathrm{V}_{\mathrm{CC}}+0.05$ |

## DC Electrical Characteristics

The following specifications apply for $+4.25 \mathrm{~V}_{\mathrm{DC}} \leq \mathrm{V}_{\mathrm{CC}} \leq+5.75 \mathrm{~V}_{\mathrm{DC}}, \mathrm{f}_{\mathrm{SYSCLK}}=8.33 \mathrm{MHz}, \mathrm{R}_{\mathrm{S}}=25 \Omega$, unless otherwise specified. Boldface limits apply for $\mathrm{T}_{\mathrm{A}}=\mathrm{T}_{\mathbf{J}}=\mathrm{T}_{\text {MIN }}$ to $\mathrm{T}_{\mathrm{MAX}}$; all other limits $\mathrm{T}_{\mathrm{A}}=\mathrm{T}_{\mathrm{J}}=25^{\circ} \mathrm{C}$. (Note 7)

| Symbol | Parameter | Conditions | Typical <br> (Note 8) | Limits <br> (Note 9) | Units <br> (Limits) |
| :---: | :---: | :---: | :---: | :---: | :---: |

Power Supply Characteristics

| $\mathrm{I}_{\mathrm{CC}}$ | Supply Current | Interface Inactive | 1.0 | 2 | $\mathrm{mA}(\mathrm{max})$ |
| :---: | :--- | :--- | :---: | :---: | :---: |
|  |  | Shutdown Mode | 10 |  | $\mu \mathrm{~A}$ |

Temperature-to-Digital Converter Characteristics

|  | Accuracy | $-10^{\circ} \mathrm{C} \leq \mathrm{T}_{\mathrm{A}} \leq+100^{\circ} \mathrm{C}$ |  | $\pm \mathbf{3}$ | ${ }^{\circ} \mathrm{C}(\max )$ |
| :--- | :--- | :--- | :--- | :---: | :---: |
|  | Resolution |  |  | $\mathbf{1}$ | ${ }^{\circ} \mathrm{C}(\mathrm{min})$ |

Analog-to-Digital Converter Characteristics

|  | Resolution (8 bits with full-scale at 4.096V) |  | 16 |  | mV |
| :---: | :--- | :--- | :---: | :---: | :---: |
| TUE | Total Unadjusted Error | (Note 10) |  | $\pm \mathbf{1}$ | \%(max) |
| DNL | Differential Non-Linearity |  |  | $\pm \mathbf{1}$ | LSB |
| PSS | Power Supply Sensitivity |  | $\pm 1$ |  | $\% / V$ |
| $\mathrm{t}_{\mathrm{C}}$ | Total Monitoring Cycle Time | (Note 11) | 1.0 | $\mathbf{1 . 5}$ | $\sec (\max )$ |

Op Amp Characteristics

|  | Output Current (Sourcing) |  | 50 |  | $\mu \mathrm{~A}$ |
| :--- | :--- | :--- | :---: | :---: | :---: |
|  | Input Offset Voltage | $\mathrm{I}_{\text {Out }}=50 \mu \mathrm{~A}$ | $\pm 1$ |  | mV |
|  | Input Bias Current |  | $\pm 0.1$ |  | nA |
|  | PSRR |  | 60 |  | dB |
|  | DC Open Loop Gain |  | 70 |  | dB |

Multiplexer/ADC Input Characteristics

|  | On Resistance |  | 400 | 2000 | $\Omega$ (max) |
| :--- | :--- | :---: | :---: | :---: | :---: |
|  | Off Channel Leakage Current |  | $\pm 0.1$ |  | nA |
|  | Input Current (On Channel Leakage Current) |  | $\pm 0.1$ |  | nA |

## DC Electrical Characteristics

 (Continued)The following specifications apply for $+4.25 \mathrm{~V}_{\mathrm{DC}} \leq \mathrm{V}_{\mathrm{CC}} \leq+5.75 \mathrm{~V}_{\mathrm{DC}}, \mathrm{f}_{\mathrm{SYSCLK}}=8.33 \mathrm{MHz}, \mathrm{R}_{\mathrm{s}}=25 \Omega$, unless otherwise specified. Boldface limits apply for $\mathrm{T}_{\mathrm{A}}=\mathrm{T}_{\mathrm{J}}=\mathrm{T}_{\text {MIN }}$ to $\mathrm{T}_{\text {MAX }}$; all other limits $\mathrm{T}_{\mathrm{A}}=\mathrm{T}_{\mathrm{J}}=25^{\circ} \mathrm{C}$. (Note 7)

| Symbol | Parameter | Conditions | Typical <br> (Note 8) | Limits <br> (Note 9) | Units <br> (Limits) |
| :---: | :---: | :---: | :---: | :---: | :---: |

## Fan RPM-to-Digital Converter

|  | Accuracy | $\begin{aligned} & +25^{\circ} \mathrm{C} \leq \mathrm{T}_{\mathrm{A}} \leq+75^{\circ} \mathrm{C} \\ & -10^{\circ} \mathrm{C} \leq \mathrm{T}_{\mathrm{A}} \leq+100^{\circ} \mathrm{C} \end{aligned}$ |  | $\begin{gathered} \pm 6 \\ \pm 12 \end{gathered}$ | \% (max) <br> \% (max) |
| :---: | :---: | :---: | :---: | :---: | :---: |
|  | Full-scale Count |  |  | 255 | (max) |
|  | FAN1 and FAN2 Nominal Input RPM (See Section 6.0) | Divisor = 1, Fan Count = 153 (Note 12) | 8800 |  | RPM |
|  |  | Divisor $=2$, Fan Count $=153$ (Note 12) | 4400 |  | RPM |
|  |  | Divisor $=4$, Fan Count $=153$ (Note 12) | 2200 |  | RPM |
|  |  | Divisor $=8$, Fan Count $=153$ (Note 12) | 1100 |  | RPM |
|  | FAN3 Design Nominal Input RPM | Fan Count = 153 (Note 12) | 4400 |  | RPM |
|  | Internal Clock Frequency | $+25^{\circ} \mathrm{C} \leq \mathrm{T}_{\mathrm{A}} \leq+75^{\circ} \mathrm{C}$ | 22.5 | $\begin{aligned} & \hline 21.1 \\ & 23.9 \end{aligned}$ | kHz (min) <br> kHz (max) |
|  |  | $-10^{\circ} \mathrm{C} \leq \mathrm{T}_{\mathrm{A}} \leq+100^{\circ} \mathrm{C}$ | 22.5 | $\begin{aligned} & 19.8 \\ & 25.2 \end{aligned}$ | $\mathrm{kHz}(\min )$ <br> kHz (max) |
| Digital Outputs (VID4/NTEST, NMI/IRQ\#) |  |  |  |  |  |
| $\mathrm{V}_{\text {OUT(1) }}$ | Logical "1" Output Voltage | $\mathrm{I}_{\text {OUT }}= \pm 5.0 \mathrm{~mA}$ |  | 2.4 | V (min) |
| $V_{\text {OUT(0) }}$ | Logical "0" Output Voltage | $\mathrm{I}_{\text {OUT }}= \pm 5.0 \mathrm{~mA}$ |  | 0.4 | $V$ (max) |
| ISA D0-D7 Digital Outputs |  |  |  |  |  |
| $\mathrm{V}_{\text {OUT(1) }}$ | Logical "1" Output Voltage | $\mathrm{I}_{\text {OUT }}= \pm 12.0 \mathrm{~mA}$ |  | 2.4 | $V$ (min) |
| $\mathrm{V}_{\text {OUT(0) }}$ | Logical "0" Output Voltage | $\mathrm{I}_{\text {OUT }}= \pm 12.0 \mathrm{~mA}$ |  | 0.4 | $V$ (max) |
| Iout | TRI-STATE Output Current | $\begin{aligned} & \mathrm{V}_{\text {OUT }}=0 \mathrm{~V}_{\mathrm{DC}} \\ & \mathrm{~V}_{\text {OUT }}=\mathrm{V}_{\mathrm{CC}}=+5.0 \mathrm{~V}_{\mathrm{DC}} \end{aligned}$ | $\begin{gathered} 0.005 \\ -0.005 \end{gathered}$ | $\begin{gathered} 1 \\ -1 \end{gathered}$ | $\mu \mathrm{A}$ (max) $\mu \mathrm{A}(\min )$ |

Open Drain Digital Outputs (Power Switch Bypass\#, SDA, RESET\#, SMI\#, Chassis Intrusion)

| $\mathrm{V}_{\mathrm{OUT}(0)}$ | Logical "0" Output Voltage | $\mathrm{I}_{\mathrm{OUT}}=-5.0 \mathrm{~mA}$ |  | $\mathbf{0 . 4}$ | $\mathrm{~V}(\mathrm{~min})$ |
| :---: | :--- | :--- | :---: | :---: | :---: |
| $\mathrm{I}_{\mathrm{OH}}$ | High Level Output Current | $\mathrm{V}_{\mathrm{OUT}}=\mathrm{V}_{\mathrm{CC}}=+5.0 \mathrm{~V}_{\mathrm{DC}}$ | 0.1 | $\mathbf{1 0 0}$ | $\mu \mathrm{~A}(\mathrm{max})$ |
|  | RESET\# andChassis Intrusion <br> Pulse Width |  | 45 | $\mathbf{2 0}$ | $\mathrm{~ms}(\mathrm{~min})$ |

Digital Inputs: SMI_IN\#, VID0-VID3, VID4/NTEST, BTI\#, CS\#, A0, A1, A2, Mode Control and Interface Inputs (IORD\#, IOWR\#, SYSCLK), Data Lines (D0-D7), Chassis Intrusion, and Tach Pulse Logic Inputs (Fan1, Fan2, Fan3)


All Digital Inputs Except for BTI\#

| $\mathrm{I}_{\mathbb{N}(1)}$ | Logical "1" Input Current | $\mathrm{V}_{\mathbb{I N}}=\mathrm{V}_{\mathrm{CC}}=+5.0 \mathrm{~V}_{\mathrm{DC}}$ | -0.005 | $\mathbf{- 1}$ | $\mu \mathrm{~A}(\mathrm{~min})$ |
| :---: | :--- | :--- | :---: | :---: | :---: |
| $\mathrm{I}_{\mathbb{N}(0)}$ | Logical "0" Input Current | $\mathrm{V}_{\mathbb{I N}}=0 \mathrm{~V}_{\mathrm{DC}}$ | 0.005 | $\mathbf{1}$ | $\mu \mathrm{~A}(\mathrm{max})$ |
| $\mathrm{C}_{\mathbb{N}}$ | Digital Input Capacitance |  | 20 |  | pF |


| DC Electrical Characteristics (Continued) |  |  |  |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: |
| The following specifications apply for $+4.25 \mathrm{~V}_{\mathrm{DC}} \leq \mathrm{V}_{\mathrm{CC}} \leq+5.75 \mathrm{~V}_{\mathrm{DC}}, \mathrm{f}_{\mathrm{SYSCLK}}=8.33 \mathrm{MHz}, \mathrm{R}_{\mathrm{S}}=25 \Omega$, unless otherwise specified. Boldface limits apply for $\mathrm{T}_{\mathrm{A}}=\mathrm{T}_{\mathrm{J}}=\mathrm{T}_{\text {MIN }}$ to $\mathrm{T}_{\text {MAX }}$; all other limits $\mathrm{T}_{\mathrm{A}}=\mathrm{T}_{\mathrm{J}}=25^{\circ} \mathrm{C}$. (Note 7) |  |  |  |  |  |
| Symbol | Parameter | Conditions | Typical (Note 8) | Limits (Note 9) | Units (Limits) |
| BTI\# Digital Input |  |  |  |  |  |
| $\mathrm{I}_{\text {(1) }}$ | Logical "1" Input Current | $\mathrm{V}_{1 \mathrm{~N}}=\mathrm{V}_{\mathrm{CC}}=+5.0 \mathrm{~V}_{\text {DC }}$ | 1 | 10 | $\mu \mathrm{A}$ (max) |
| $\mathrm{I}_{\text {IN(0) }}$ | Logical "0" Input Current | $\mathrm{V}_{\mathrm{IN}}=0 \mathrm{~V}_{\mathrm{DC}}$ | - 500 | -2000 | $\mu \mathrm{A}$ (max) |
| $\mathrm{C}_{\text {IN }}$ | Digital Input Capacitance |  | 20 |  | pF |

## AC Electrical Characteristics

The following specifications apply for $+4.25 \mathrm{~V}_{\mathrm{DC}} \leq \mathrm{V}_{\mathrm{CC}} \leq+5.75 \mathrm{~V}_{\mathrm{DC}}$ unless otherwise specified. Boldface limits apply for $\mathrm{T}_{\mathrm{A}}=$ $\mathbf{T}_{\mathbf{J}}=\mathrm{T}_{\text {MIN }}$ to $\mathrm{T}_{\text {MAX }}$; all other limits $\mathrm{T}_{\mathrm{A}}=\mathrm{T}_{\mathrm{J}}=25^{\circ} \mathrm{C}$. (Note 13)

| Symbol | Parameter | Conditions | Typical <br> (Note 8) | Limits <br> (Note 9) | Units <br> (Limits) |
| :---: | :---: | :---: | :---: | :---: | :---: |

ISA Timing Characteristics



Figure 1. ISA Bus Write Timing Diagram


Figure 2. ISA Bus Read Timing Diagram

## AC Electrical Characteristics (Continued)

The following specifications apply for $+4.25 \mathrm{~V}_{\mathrm{DC}} \leq \mathrm{V}_{C C} \leq+5.75 \mathrm{~V}_{\mathrm{DC}}$ unless otherwise specified. Boldface limits apply for $\mathrm{T}_{\mathrm{A}}=$ $\mathrm{T}_{\mathrm{J}}=\mathrm{T}_{\text {MIN }}$ to $\mathrm{T}_{\text {MAX }}$; all other limits $\mathrm{T}_{\mathrm{A}}=\mathrm{T}_{\mathrm{J}}=25^{\circ} \mathrm{C}$. (Note 13)

| Symbol | Parameter | Conditions | Typical <br> (Note 8) | Limits <br> (Note 9) | Units <br> (Limits) |
| :---: | :---: | :---: | :---: | :---: | :---: |

Serial Bus Timing Characteristics

| $t_{1}$ | SCL (Clock) Period |  | $\mathbf{2 . 5}$ | $\mu \mathrm{s}(\mathrm{min})$ |
| :---: | :--- | :--- | :--- | :---: |
| $\mathrm{t}_{2}$ | Data In Setup Time to SCL High |  |  | $\mathbf{1 0 0}$ |
| $\mathrm{t}_{3}$ | Data Out Stable After SCL Low |  | $\mathrm{ns}(\mathrm{min})$ |  |
| $\mathrm{t}_{4}$ | SDA Low Setup Time to SCL Low <br> (start) |  | $\mathbf{0}$ | $\mathrm{ns}(\mathrm{min})$ |
| $\mathrm{t}_{5}$ | SDA High Hold Time After SCL High <br> $($ stop $)$ |  | $\mathbf{1 0 0}$ | $\mathrm{ns}(\mathrm{min})$ |



Figure 3. Serial Bus Timing Diagram

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional, but do not guarantee specific performance limits. For guaranteed specifications and test conditions, see the Electrical Characteristics. The guaranteed specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions.
Note 2: All voltages are measured with respect to GND, unless otherwise specified
Note 3: When the input voltage $\left(\mathrm{V}_{\mathbb{I N}}\right)$ at any pin exceeds the power supplies $\left(\mathrm{V}_{\mathbb{I N}}<(\mathrm{GNDD}\right.$ or GNDA$)$ or $\left.\mathrm{V}_{\mathbb{I N}}>\mathrm{V}_{\mathrm{CC}}\right)$, the current at that pin should be limited to 5 mA . The 20 mA maximum package input current rating limits the number of pins that can safely exceed the power supplies with an input current of 5 mA to four.
Note 4: The maximum power dissipation must be derated at elevated temperatures and is dictated by $\mathrm{T}_{\mathrm{J}} \mathrm{max}, \Theta_{\mathrm{JA}}$ and the ambient temperature, $\mathrm{T}_{\mathrm{A}}$. The maximum allowable power dissipation at any temperature is $\mathrm{P}_{\mathrm{D}}=\left(\mathrm{T}_{\mathrm{J} m a x}-\mathrm{T}_{\mathrm{A}}\right) / \Theta_{\mathrm{JA}}$.
Note 5: The human body model is a 100 pF capacitor discharged through a $1.5 \mathrm{k} \Omega$ resistor into each pin. The machine model is a 200 pF capacitor discharged directly into each pin.
Note 6: See the section titled "Surface Mount" found in any post 1986 National Semiconductor Linear Data Book for other methods of soldering surface mount devices.
Note 7: Each input and output is protected by a nominal 6.5 V breakdown voltage zener diode to GND ; as shown below, input voltage magnitude up to 0.3 V above $\mathrm{V}_{\mathrm{CC}}$ or 0.3 V below GND will not damage the LM79. There are parasitic diodes that exist between the inputs and the power supply rails. Errors in the ADC conversion can occur if these diodes are forward biased by more than 50 mV . As an example, if $\mathrm{V}_{\mathrm{CC}}$ is $4.50 \mathrm{~V}_{\mathrm{DC}}$, input voltage must be $\leq 4.55 \mathrm{~V}_{\mathrm{DC}}$, to ensure accurate conversions.

*An x indicates that the diode exists.

| Pin Name | D 1 | D 2 | D 3 |
| :---: | :---: | :---: | :---: |
| IORD\# |  |  | x |
| IOWR\# |  |  | x |
| SYSCLK |  |  | x |
| D0-D7 | x | x | x |
| SMI_IN\# |  |  | x |
| Chassis Intrusion |  | x | x |
| Power Switch Bypass\# |  | x | x |
| Fan1-Fan3 |  |  | x |
| SCL |  |  | x |
| SDA |  | x | x |
| RESET\# |  | x | x |
| VID4/NTEST | x | x | x |


| Pin Name | D1 | D2 | D3 |
| :---: | :---: | :---: | :---: |
| -IN6 |  | x | x |
| FB6 | x | x | x |
| FB5 | x | x | x |
| -IN5 |  | x | x |
| IN4-IN0 | x | x | x |
| VID3-VID0 | x | x | x |
| BTI\# | x |  | x |
| NMI\#/IRQ\# | x | x | x |
| SMI\# |  | x | x |
| A0-A2 |  |  | x |
| CS\# |  |  | x |

Figure 4. ESD Protection Input Structure

Note 8: Typicals are at $\mathrm{T}_{\mathrm{J}}=\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$ and represent most likely parametric norm.
Note 9: Limits are guaranteed to National's AOQL (Average Outgoing Quality Level).
Note 10: TUE (Total Unadjusted Error) includes Offset, Gain and Linearity errors of the ADC and any error introduced by the amplifiers as shown in the circuit of Figure 11.
Note 11: Total Monitoring Cycle Time includes temperature conversion, 7 analog input voltage conversions and 3 tachometer readings. Each temperature and input voltage conversion takes 100 ms typical and 112 ms maximum. Fan tachometer readings take 20 ms typical, at 4400 rpm , and 200 ms max.

Note 12: The total fan count is based on 2 pulses per revolution of the fan tachometer output.
Note 13: Timing specifications are tested at the TTL logic levels, $\mathrm{V}_{\mathrm{IL}}=0.4 \mathrm{~V}$ for a falling edge and $\mathrm{V}_{\mathrm{IH}}=2.4 \mathrm{~V}$ for a rising edge. TRI-STATE output voltage is forced to 1.4 V .

## Test Circuit



Figure 5. Digital Output Load Circuitry

## Functional Description

### 1.0 GENERAL DESCRIPTION

The LM79 provides 7 analog inputs, a temperature sensor, a Delta-Sigma ADC (Analog-to-Digital Converter), 3 fan speed counters, WATCHDOG registers, and a variety of inputs and outputs on a single chip. Interfaces are provided for both the ISA parallel bus or Serial Bus. The LM79 performs power supply, temperature, and fan monitoring for personal computers.
The LM79 continuously converts analog inputs to 8-bit digital words with a 16 mV LSB (Least Significant Bit) weighting, yielding input ranges of from 0 to 4.096 volts. The two negative analog inputs provide inverting op amps, with their noninverting input referred to ground. With additional external feedback components, these inputs provide measurements of negative voltages (such as -5 and -12 volt power supplies). The analog inputs are useful for monitoring several power supplies present in a typical computer. Temperature is converted to an 8 -bit two's-complement digital word with a 1 ${ }^{\circ} \mathrm{C}$ LSB.
Fan inputs measure the period of tachometer pulses from the fans, providing a higher count for lower fan speeds. The fan inputs are digital inputs with an acceptable range of 0 to 5 volts and a transition level of approximately 1.4 volts. Full scale fan counts are 255 ( 8 -bit counter) and this represents a stopped or very slow fan. Nominal speeds, based on a count of 153, are programmable from 1100 to 8800 RPM on FAN1 and FAN2, with FAN3 fixed at 4400 RPM. Signal conditioning circuitry is included to accommodate slow rise and fall times.
The LM79 provides a number of internal registers, as detailed in Figure 6. These include:

Configuration Register: Provides control and configuration.
Interrupt Status Registers: Two registers to provide status of each WATCHDOG limit or Interrupt event.
Interrupt Mask Registers: Allows masking of individual Interrupt sources, as well as separate masking for each of both hardware Interrupt outputs.
VID/Fan Divisor Registers: A register to read the status of the VIDO-VID3 input lines. The high bits of this register contain the divisor bits for FAN1 and FAN2 inputs.
Serial Bus Address Register: Contains the Serial Bus address. At power on it assumes the default value of 0101101 binary, and can be altered via the ISA or Serial Bus interface.
VID4/Device ID Register: The state of VID4 is reflected in this register. The identity of the device being used can be determined by reading the state of D7 of this register. An LM79 would be identified when D7 is high.
POST RAM: FIFO RAM to store up to 32 bytes of 8 -bit POST codes. Overflow of the POST RAM will set an Interrupt. The POST RAM, located at base address x0h and x 4 h , allows for easy decoding to address 80 h and 84h, the normal addresses for outputting of POST codes. Interrupt will only be set when writing to port x 0 h or x 4 h . The POST RAM can be read via ports 85 h and 86 h .
Value RAM: The monitoring results: temperature, voltages, fan counts, and WATCHDOG limits are all contained in the Value RAM. The Value RAM consists of a
total of 64 bytes. The first 11 bytes are all of the results, the next 19 bytes are the WATCHDOG limits, and are located at $20 \mathrm{~h}-3 \mathrm{Fh}$, including two unused bytes in the upper locations. The next 32 bytes, located at 60h-7Fh, mirror the first 32 bytes with identical contents. The only difference in the upper bytes are that they auto-increment the LM79 Internal Address Register when read from or written to via the ISA bus (auto-increment is not available for Serial Bus communications).
When the LM79 is started, it cycles through each measurement in sequence, and it continuously loops through the sequence approximately once every second. Each measured value is compared to values stored in WATCHDOG, or Limit registers. When the measured value violates the programmed limit the LM79 will set a corresponding Interrupt in the Interrupt Status Registers. Two hardware Interrupt lines, SMI\# and NMI//RQ\#, are fully programmable with separate masking of each Interrupt source, and masking of each output. In addition, the Configuration Register has control bits to enable or disable the hardware Interrupts.
Additional digital inputs are provided for chaining of SMI\# (System Management Interrupt), outputs of multiple external LM75 temperature sensors via the BTI\# (Board Temperature Interrupt) input, and a Chassis Intrusion input. The Chassis Intrusion input is designed to accept an active high signal from an external circuit that latches when the case is removed from the computer.

### 2.0 INTERFACE

The LM79 only decodes the three lowest address bits on the ISA bus. Referring to the ISA bus timing diagrams in Figure 1. and Figure 2., the Chip Select Input, CS\#, should be taken low by external address decoder circuitry to access the LM79. The LM79 decodes the following base addresses:
-Port xOh: Power On Self Test codes from ISA bus.
-Port x4h: Power On Self Test codes from ISA bus.
-Port x5h: The LM79's Internal Address Register
-Port x6h: Data Register
IORD\# is the standard ISA bus signal that indicates to the LM79 that it may drive data on to the ISA data bus.
IOWR\# is the standard ISA command to the LM79 that it may latch data from the ISA bus.
SYSCLK is the standard ISA SYSCLK, typically 8.33 MHz . This clock is used only for timing of the ISA interface of the LM79. All other clock functions within LM79 such as the ADC and fan counters are done with a separate asynchronous internal clock.
A typical application designed to utilize the POST RAM would decode the LM79 to the address space starting at 80 h , which is where POST codes are output to. Otherwise, the LM79 can be decoded into any desired address space.
To communicate with an LM79 Register, first write the address of that Register to Port $\times 5 \mathrm{~h}$. Read or write data from or to that register via Port x6h. A write will take IOWR\# low, while a read will take IORD\# low.
If the Serial Bus Interface and ISA bus interface are used simultaneously there is the possibility of collision. To prevent this from occurring in applications where both interfaces are used, read port $\times 5 \mathrm{~h}$ and if the Most Significant Bit, D7, is high, ISA communication is limited to reading port x5h only until this

Functional Description (Continued)


Figure 6. LM79 Register Structure

## Functional Description (Continued)

bit is low. A Serial Bus communication occurring while ISA is active will not be a problem, since even a single bit of Serial Bus communication requires 10 microseconds, in comparison to less than a microsecond for an entire ISA communication.

### 2.1 Internal Registers of the LM79

Table 1. The internal registers and their corresponding internal LM79 address is as follows:

| Register | LM79 Internal Hex Address <br> (This is the data to be written to Port x5h) | Power on Value | Notes |
| :---: | :---: | :---: | :---: |
| Configuration Register | 40h | 00001000 |  |
| Interrupt Status Register 1 | 41h | 00000000 | Auto-increment to the address of Interrupt Status Register 2 after a read or write to Port x6h. |
| Interrupt Status Register 2 | 42h | 00000000 |  |
| SMI\# Mask Register 1 | 43h | 00000000 | Auto-increment to the address of SMI\# Mask Register 2 after a read or write to Port x6h. |
| SMI\# Mask Register 2 | 44h | 00000000 |  |
| NMI Mask Register 1 | 45h | 00000000 | Auto-increment to the address of NMI Mask Register 2 after a read or write to Port x6h. |
| NMI Mask Register 2 | 46h | 01000000 |  |
| VID/Fan Divisor Register | 47h | 0101 XXXX | The first four bits set the divisor for Fan Counters 1 and 2. The lower four bits reflect the state of the VIDOVID3 inputs. |
| Serial Bus Address Register | 48h | 00101101 |  |
| VID4/Device ID Register | 49h | 1000 000X | D7 identifies this devices as the LM79. D0 reflects the state of VID4. |
| POST RAM | 00h-1Fh |  | Auto-increment when written to from Port $x 0 h$ or $x 4 h$. Autoincrement after a read or write to Port x6h, with a separate pointer. Autoincrementing stops when address 1 Fh is reached. |
| Value RAM | 20h-3Fh |  |  |
| Value RAM | 60h-7Fh |  | Auto-increment after a read or write to Port x6h. Autoincrementing stops when address 7Fh is reached. |

Functional Description (Continued)

(a) Serial Bus Write to the Internal Address Register followed by the Data Byte

(b) Serial Bus Write to the Internal Address Register only.

(c) Serial Bus Read from a Register with the Internal Address Register preset to desired location.

Figure 7. Serial Bus Timing

## Functional Description (Continued)

## A typical communication with the LM79 would consist of:

1. Write to Port x5h the LM79 Internal Address (from column 2 above) of the desired register. Alternatively, when both ISA and Serial Bus interfaces are used, the first step in a communication may be to read Port x5h to ascertain the state of the Busy bit to avoid contention with an Serial Bus communication.
2. Read or write the corresponding registers data with reads/writes from Port x6h.
The LM79 Internal Address latches, and does not have to be written if it is already pointing at the desired register. The LM79 Internal Address Register is read/write (Bit 7 is read only).

### 2.2 Serial Bus Interface

When using the Serial Bus Interface a write will always consist of the LM79 Serial Bus Interface Address byte, followed by the Internal Address Register byte, then the data byte. There are two cases for a read:

1. If the Internal Address Register is known to be at the desired Address, simply read the LM79 with the Serial Bus Interface Address byte, followed by the data byte read from the LM79.
2. If the Internal Address Register value is unknown, write to the LM79 with the Serial Bus Interface Address byte, followed by the Internal Address Register byte. Then restart the Serial Communication with a Read consisting of the Serial Bus Interface Address byte, followed by the data byte read from the LM79.
In all other respects the LM79 functions identically for Serial Bus communications as it does for ISA communications. AutoIncrement does not operate. When writing to or reading from a Register which Auto-Increments with ISA communications, the Register must be manually incremented for Serial Bus communications.
The default power on Serial Bus address for the LM79 is: 0101101 binary. This address can be changed by writing any desired value to the Serial Bus address register, which can be done either via the ISA or Serial Bus. During and Serial Bus communication the BUSY bit (Bit 7) in the address register at $\times 5 \mathrm{~h}$ will be high, and any ISA activity in that situation should be limited to reading port $\times 5 \mathrm{~h}$ only.
All of these communications are depicted in the Serial Bus Interface Timing Diagrams as shown in Figure 7.

### 3.0 USING THE LM79

### 3.1 Power On

When power is first applied, the LM79 performs a "power on reset" on several of its registers. The power on condition of registers is shown in Table 1. Registers whose power on values are not shown have power on conditions that are indeterminate (this includes the value RAM and WATCHDOG limits). The ADC is inactive. In most applications, usually the first action after power on would be to write WATCHDOG limits into the Value RAM.

### 3.2 Resets

Configuration Register INITIALIZATION accomplishes the same function as power on reset. The POST RAM, Value RAM conversion results, and Value RAM WATCHDOG limits are not Reset and will be indeterminate immediately after power on. If the Value RAM contains valid conversion results and/or Value RAM WATCHDOG limits have been previously set, they will not be affected by a Configuration Register INITIALIZATION. Power on reset, or Configuration Register INITIALIZATION, clear or initialize the following registers (the initialized values are shown in Table 1):

Configuration Register
Interrupt Status Register 1
Interrupt Status Register 2
SMI\# Mask Register 1
SMI\# Mask Register 2
NMI Mask Register 1
NMI Mask Register 2
VID/Fan Divisor Register

## VID4/Device ID Register

Serial Bus Address Register (Power on reset only, not reset by Configuration Register INITIALIZATION)
Configuration Register INITIALIZATION is accomplished by setting Bit 7 of the Configuration Register high. This Bit automatically clears after being set.

### 3.3 Using the Configuration Register

The Configuration Register provides all control over the LM79. At power on, the ADC is stopped and INT_Clear is asserted, clearing the SMI\# and NMI/IRQ\# hardwire outputs. The Configuration Register starts and stops the LM79, enables and disables Interrupt outputs and modes, and provides the Reset function described in 3.2.
Bit 0 of the Configuration Register controls the monitoring loop of the LM79. Setting Bit 0 low stops the LM79 monitoring loop and puts the LM79 in shutdown mode, reducing power consumption. ISA and Serial Bus communication is possible with any register in the LM79 although activity on these lines will increase shutdown current, up to as much as maximum rated supply current, while the activity takes place. Taking Bit 0 high starts the monitoring loop, described in more detail subsequently.
Bit 1 of the Configuration Register enables the SMI\# Interrupt hardwire output when this bit is taken high. Similarly, Bit 2 of the Configuration Register enables the NMI/IRQ\# Interrupt hardwire output when taken high. The NMI/IRQ\# mode is determined by Bit 5 in the Configuration Register. When Bit 5 is low the output is an active low IRQ\# output. Taking Bit 5 high inverts this output to provide an active high NMI output.
The Power Switch Bypass\# provides an active low open drain at the Power Switch Bypass\# output when set high. This is intended for use in software power control by activating an external power control MOSFET.

## Functional Description (Continued)

### 3.4 Starting Conversion

The monitoring function (Analog inputs, temperature, and fan speeds) in the LM79 is started by writing to the Configuration Register and setting INT_Clear (Bit 3), low, and Start (Bit 0), high. The LM79 then performs a "round-robin" monitoring of all analog inputs, temperature, and fan speed inputs approximately once a second. The sequence of items being monitored corresponds to locations in the Value RAM and is:

1. Temperature
2. INO
3. IN1
4. IN2
5. IN3
6. IN4
7. -IN5
8.     - IN6
9. Fan 1
10. Fan 2
11. Fan 3

### 3.5 Reading Conversion Results

The conversion results are available in the Value RAM. Conversions can be read at any time and will provide the result of the last conversion. Because the ADC stops, and starts a new conversion whenever it is read, reads of any single value should not be done more often than once every 120 ms . When reading all values, allow at least 1.5 seconds between reading groups of values. Reading more frequently than once every 1.5 seconds can also prevent complete updates of Interrupt Status Registers and Interrupt Outputs.
A typical sequence of events upon power on of the LM79 would consist of:

## 1. Set WATCHDOG Limits.

2. Set Interrupt Masks
3. Start the LM79 monitoring process

### 4.0 ANALOG INPUTS

The 8 -bit ADC has a 16 mV LSB, yielding a 0 to 4.08 volt (4.096-1LSB) input range. This is true for all analog inputs. In PC monitoring applications these inputs would most often be connected to power supplies. The 2.5 and 3.3 volt supplies can be directly connected to the inputs. The 5 and 12 volt inputs should be attenuated with external resistors to any desired value within the input range.
A typical application, such as is shown in Figure 8., might select the input voltage divider to provide 3 volts at the analog inputs of the LM79. This is sufficiently high for good resolution of the voltage, yet leaves headroom for upward excursions from the supply of about $25 \%$. To simplify the process of resistor selection, set the value of R2 first. Select a value for R2 between $10 \mathrm{k} \Omega$ and $100 \mathrm{k} \Omega$ This is low enough to avoid
errors due to input leakage currents yet high enough to both protect the inputs under overdrive conditions as well as minimize loading of the source. Then select R1 to provide a 3 volt input according to:
$R 1=R 2\left(\frac{V_{S}}{V_{I N}}-1\right)$

| Voltage Measurement $\left(\mathrm{V}_{\mathrm{S}}\right)$ | R1 or $\mathrm{R}_{\mathrm{IN}}$ | R2 or $\mathrm{R}_{\mathrm{F}}$ | Voltage at Analog Inputs |
| :---: | :---: | :---: | :---: |
| +2.50 V | 0 | NONE | +2.50 V |
| +3.30 V | 0 | NONE | +3.30 V |
| +5 V | $6.8 \mathrm{k} \Omega$ | $10 \mathrm{k} \Omega$ | +2.98 V |
| +12 V | $30 \mathrm{k} \Omega$ | $10 \mathrm{k} \Omega$ | +3.00 V |
| -12 V | $240 \mathrm{k} \Omega$ | $60 \mathrm{k} \Omega$ | +3.00 V |
| -5 V | $100 \mathrm{k} \Omega$ | $60 \mathrm{k} \Omega$ | +3.00 V |



Figure 8. Input examples. Resistor values shown provide approximately 3 V at the analog inputs
The negative inputs provide inverting op amps with noninverting inputs connected to ground. The output of these op amps are designed to drive the input of the LM79 and their associated feedback loops. Avoid heavy loading, long lines, and capacitive loading of greater than 100 pF with these op amps. The optimum feedback resistor (resistor from Feedback to -IN pin) value is approximately $60 \mathrm{k} \Omega$, based on the op amp nominal output current rating of $50 \mu \mathrm{~A}$ at an output voltage of 3 V . Locate the feedback resistors as close as possible to the LM79. The recommended range for $\mathrm{R}_{\mathrm{IN}}$ is from $30 \mathrm{k} \Omega$ to 300 $\mathrm{k} \Omega$.
Select $\mathrm{R}_{\mathrm{IN}}$ according to:
$R_{I N}=\frac{V_{S} \times R_{F}}{V_{F E E D B A C K}}$
The analog inputs have internal diodes that clamp inputs exceeding the power supply and ground. Exceeding any analog input has no detrimental effect on other channels. The input diodes will also clamp voltages appearing at the inputs of an un-powered LM79. External resistors should be included to limit input currents to the values given in the ABSOLUTE MAXIMUM RATINGS for Input Current At Any Pin. Inputs with the attenuator networks will usually meet these requirements. If it is possible for inputs without attenuators (such as the 2.5 or 3.3 volt supplies) to be turned on while LM79 is powered off, additional resistors of about $10 \mathrm{k} \Omega$ should be added in series with the inputs to limit the input current.

Functional Description (Continued)


Figure 9. Alternatives for fan inputs.

Counts are based on 2 pulses per revolution tachometer outputs.

| RPM | Time per revolution | Counts for "Divide by 2" <br> (default) in decimal | Comments |
| :--- | :--- | :--- | :--- |
| 4400 | 13.64 ms | 153 counts | Typical RPM |
| 3080 | 19.48 ms | 219 counts | $70 \%$ RPM |
| 2640 | 22.73 ms | 255 counts (maximum <br> counts) | $60 \%$ RPM |


| Mode <br> Select | Nominal <br> RPM | Time per revolution | Counts for the <br> given speed in <br> decimal | 70\% RPM | Time per revolution for <br> 70\% RPM |
| :--- | :--- | :--- | :--- | :--- | :--- |
| Divide by 1 | 8800 | 6.82 ms | 153 | 6160 | 9.74 ms |
| Divide by 2 | 4400 | 13.64 ms | 153 | 3080 | 19.48 ms |
| Divide by 4 | 2200 | 27.27 ms | 153 | 770 | 38.96 ms |
| Divide by 8 | 1100 | 54.54 ms | 153 | 77.92 ms |  |

$1.35 \times 10^{6}$
Count =
RPM x Divisor

## Functional Description (Continued)

### 5.0 LAYOUT AND GROUNDING

Analog inputs will provide best accuracy when referred to the AGND pin. A separate, low-impedance ground plane for analog ground, which provides a ground point for the voltage dividers and analog components, will provide best performance but is not mandatory. Analog components such as voltage dividers and feedback resistors should be located physically as close as possible to the LM79.
The power supply bypass, the parallel combination of $10 \mu \mathrm{~F}$ (electrolytic or tantalum) and $0.1 \mu \mathrm{~F}$ (ceramic) bypass capacitors connected between pin 12 and ground, should also be located as close as possible to the LM79.

### 6.0 FAN INPUTS

Inputs are provided for signals from fans equipped with tachometer outputs. These are logic-level inputs with an approximate threshold of 1.4 volts. Signal conditioning in the LM79 accommodates the slow rise and fall times typical of fan tachometer outputs. The maximum input signal range is 0 to $\mathrm{V}_{\mathrm{cc}}$. In the event these inputs are supplied from fan outputs which exceed 0 to $\mathrm{V}_{\mathrm{C}}$, either resistive division or diode clamping must be included to keep inputs within an acceptable range, as shown in Figure 9. R2 is selected so that it does not develop excessive voltage due to input leakage. R1 is selected based on R2 to provide a minimum input of 2 volts and a maximum of $\mathrm{V}_{\mathrm{CC}}$. R1 should be as low as possible to provide the maximum possible input up to $\mathrm{V}_{\mathrm{CC}}$ for best noise immunity. Alternatively, use a shunt reference or zener diode to clamp the input level.

If fans can be powered while the power to the LM79 is off, the LM79 inputs will provide diode clamping. Limit input current to the Input Current at Any Pin specification shown in the ABSOLUTE MAXIMUM RATINGS section. In most cases, open collector outputs with pull-up resistors inherently limit this current. If this maximum current could be exceeded, either a larger pullup resistor should be used or resistors connected in series with the fan inputs.

The Fan Inputs gate an internal 22.5 kHz oscillator for one period of the Fan signal into an 8 -bit counter (maximum count $=255)$. The default divisor, located in the VID/Fan Divisor Register, is set to 2 (choices are 1, 2, 4, and 8) providing a nominal count of 153 for a 4400 rpm fan with two pulses per revolution. Typical practice is to consider 70\% of normal RPM a fan failure, at which point the count will be 219.
Determine the fan count according to:

## $1.35 \times 10^{6}$ <br> Count = <br> RPM $\times$ Divisor

Note that Fan 1 and Fan 2 Divisors are programmable via the VID/Fan Divisor Register. Fan 3 is not adjustable, and its Divisor is always set to 2.

### 7.0 TEMPERATURE MEASUREMENT SYSTEM

The LM79 bandgap type temperature sensor and ADC perform 8 -bit two's-complement conversions of the temperature. A digital comparator is also incorporated that


Figure 10. Temperature-to-Digital transfer Function (Non-linear scale for clarity)

## Functional Description (Continued)

compares the readings to the user-programmable Overtemperature setpoint and Hysteresis values.

### 7.1 Temperature Interrupts

The normal mode for temperature interrupts in the LM79 is an "Interrupt" mode operating in the following way: Exceeding $\mathrm{T}_{\mathrm{O}}$ causes an Interrupt that will remain active indefinitely until reset by reading Interrupt Status Register 1. Once an Interrupt event has occurred by crossing $\mathrm{T}_{\mathrm{OI}}$, then reset, an Interrupt will only occur again by the temperature going below $\mathrm{T}_{\text {HYST }}$. Again, it will remain active indefinitely until being reset by reading Interrupt Status Register 1.

A "Comparator" mode for temperature interrupts can be made available by setting the $\mathrm{T}_{\text {HYST }}$ limit to $127^{\circ} \mathrm{C}$. This results in a simple "thermostat" type of function where an Interrupt will be set whenever the temperature exceeds the $T_{0 I}$ limit. Reading Interrupt Status Register 1 will clear the Interrupt as usual, but the Interrupt will set again after the completion of another measurement cycle. It will remain set until the temperature goes below the $T_{\mathrm{O}}$ limit (allow up to two measurement cycles for clearing after descending below $\mathrm{T}_{\mathrm{O}}$ while in Comparator mode).

### 7.2 Temperature Data Format

Temperature data can be read from the Temperature, $T_{\text {OI }}$ Set Point, and $T_{\text {HYST }}$ Set Point registers; and written to the $T_{\text {OI }}$ Set Point, and $\mathrm{T}_{\text {HYST }}$ Set Point registers. Temperature data is
represented by an 8-bit, two's complement word with an LSB (Least Significant Bit) equal to $1.0^{\circ} \mathrm{C}$ :

| Temperature | Digital Output |  |
| :---: | :---: | :---: |
|  | Binary | Hex |
| $+125^{\circ} \mathrm{C}$ | 01111101 | 7 Dh |
| $+25^{\circ} \mathrm{C}$ | 00011001 | 19 h |
| $+1.0^{\circ} \mathrm{C}$ | 00000001 | 01 h |
| $0^{\circ} \mathrm{C}$ | 00000000 | 00 h |
| $-1.0^{\circ} \mathrm{C}$ | 11111111 | FFh |
| $-25^{\circ} \mathrm{C}$ | 11100111 | E 7 h |
| $-55^{\circ} \mathrm{C}$ | 11001001 | C 9 h |

$\mathrm{T}_{\text {HYST }}=+127^{\circ} \mathrm{C}$

b) Comparator Mode. Interrupt resets occur when Interrupt Status Register 1 is read but will set again when monitoring cycle continues (as long as temperature exceeds $\mathrm{T}_{\mathrm{OI}}$ ). When temperature descends below $\mathrm{T}_{\mathrm{O}}$ allow up to two monitoring loops before the Temperature Interrupt resets.

Figure 9. Temperature Interrupt Response Diagram

## Functional Description (Continued)



Figure 10. Interrupt Structure

### 8.0 THE LM79 INTERRUPT STRUCTURE

Figure 10. depicts the Interrupt Structure of the LM79. The LM79 can generate Interrupts as a result of each of its internal WATCHDOG registers on the analog, temperature, and fan inputs. Overflow of the POST RAM (greater than 32 bytes written to POST RAM) will also cause an Interrupt.
External Interrupts can come from the following three sources. While the labels suggest a specific type or source of Interrupt, these labels are not restrictions of their usage, and they could come from any desired source:
BTI\#: This is an active low Interrupt intended to come from the O.S. output of LM75 temperature sensors. The LM75 O.S. output goes active when its temperature exceeds a programmed threshold. Up to 8 LM75's can be connected to a single Serial Bus bus with their O.S. output's wire or'd to the BTI\# input of the LM79. If the temperature of any LM75 exceeds its programmed limit, it drives BTI\# low. This generates an Interrupt to notify the host of a possible overtemperature condition. Provides an internal pull-up of $10 \mathrm{k} \Omega$.

Chassis Intrusion: This is an active high interrupt from any type of device that detects and captures chassis intrusion violations. This could be accomplished mechanically, optically, or electrically, and circuitry external to the LM79 is expected to latch the event. The design of the LM79 allows this input to go high even with no power applied to the LM79, and no clamping or other interference with the line will occur. This line can also be pulled low for at least 20 ms by the LM79 to reset a typical Chassis Intrusion circuit. Accomplish this reset by setting Bit 7 of NMI Mask Register 2 high. The bit in the Register is self-clearing.
SMI_IN\#: This active low Interrupt merely provides a way to chain the SMI\# Interrupt from other devices through the LM79 to the processor.
All Interrupts are indicated in the two Interrupt Status Registers. The NMI/IRQ\# and SMI\# outputs have individual mask registers, and individual masks for each Interrupt. As described in Section 3.3, these two hardware Interrupt lines

## Functional Description (Continued)

can also be enabled/disabled in the Configuration Register. The Configuration Register is also used to set the mode of the NMI/IRQ\# Interrupt line.

### 8.1 Interrupt Clearing

Reading the Interrupt Status Register will output the contents of the Register, and reset the Register. A subsequent read done before the analog "round-robin" monitoring loop is complete will indicate a cleared Register. Allow at least 1.5 seconds to allow all Registers to be updated between reads In summary, the Interrupt Status Register clears upon being read, and requires at least 1.5 seconds to be updated. When the Interrupt Status Register clears, the hardware interrupt line will also clear until the Registers are updated by the monitoring loop.

The hardware Interrupt lines are cleared with the INT_Clear bit, which is Bit 3 of the Configuration Register. When this bit is high, the LM79 monitoring loop will stop. It will resume when the bit is low.

### 9.0 RESET\# AND Power Switch Bypass\# OUTPUTS

In PC applications the open drain Power Switch Bypass\# provides a gate drive signal to an external P-channel MOSFET power switch. This external MOSFET then would keep power turned on regardless of the state of front panel power switches when software power control is used. In any given application this signal is not limited to the function described by its label. For example, since the LM79 incorporates temperature sensing, the Power Switch Bypass\# output could also be utilized to control power to a cooling fan. Take Power Switch Bypass\# active low by setting Bit 6 in the Configuration Register high.
RESET\# is intended to provide a master reset to devices connected to this line. SMI\# Mask Register 2, Bit 7, must be set high to enable this function. Setting Bit 4 in the Configuration Register high outputs a least 20 ms low on this line, at the end of which Bit 4 in the Configuration Register automatically clears. Again, the label for this pin is only its suggested use. In applications where the RESET\# capability is not needed it can be used for any type of digital control that requires a 20 ms active low open drain output.

### 10.0 POST RAM

The POST RAM is located at address $x 0 h$ and $x 4 h$, which typical address decoders will decode to 80 h or 84 h , where the BIOS will output Power On Self Test codes. A write to the POST RAM auto-increments the internal pointer of the LM79. Up to 32 bytes may be stored. An excess of 32 bytes will generate an Interrupt and stop incrementing

The POST RAM is read as like any other register at ports $\times 5 \mathrm{~h}$ and $x 6 h$, with the POST RAM located at the LM79 Internal Address from 00h to 1Fh. Reading the POST RAM via x6h will also auto-increment, but this is a separate pointer than the one used for ports 80 h and 84 h .

### 11.0 NAND TREE TESTS

A NAND tree is provided in the LM79 for Automated Test Equipment (ATE) board level connectivity testing. NAND tree tests are accomplished in power on reset with the Configuration Register in the reset state (Start Bit (Bit 0) low, and the INT_Clear (Bit 3) high). In this mode, forcing the SMI\# output low before the first write to Configuration Register takes all pins except Power Switch Bypass\#, RESET\#, -IN5, IN6, $\mathrm{V}_{\mathrm{CC}}$, GNDA, and GNDD to a high impedance (either TRISTATE or open drain) state. A write to the Configuration Register disables this mode. All high impedance pins can be taken to 0 and $V_{C C}$ to accomplish NAND tree tests.
To perform a NAND tree test all pins included in the NAND tree should be driven to 1 . Each individual pin (excluding the aforementioned exceptions) can be toggled and the resulting toggle observed on the VID4/NTEST pin. Allow for a typical propagation delay of 200 ns .

### 12.0 FAN MANUFACTURERS

Manufacturers of cooling fans with tachometer outputs are listed below:

NMB Tech
9730 Independence Ave.
Chatsworth, California 91311
818-341-3355
818 341-8207

| Model Number | Frame Size | Airflow CFM |
| :---: | :---: | :---: |
| 2408NL | 2.36 in sq. $\times 0.79$ in ( 60 mm sq. $X 20 \mathrm{~mm}$ ) | 9-16 |
| 2410ML | 2.36 in sq. $X 0.98$ in ( 60 mm sq. $X 25 \mathrm{~mm}$ ) | 14-25 |
| 3108NL | 3.15 in sq. $X 0.79$ in ( 80 mm sq. X 20 mm ) | 25-42 |
| 3110KL | 3.15 in sq. $\times 0.98$ in ( 80 mm sq. X 25 mm ) | 25-40 |

Mechatronis Inc.
P.O. Box 20

Mercer Island, WA 98040
800-453-4569
Various sizes available with tach output option.

Sanyo Denki/Keymarc Electronics
2310 205th, Suite 101
Torrance, CA 9050
310-212-7724
109P Series

Functional Description (Continued)
13.0 Registers and RAM
13.1 Address Register (Port x5h)

The main register is the ADDRESS Register located at Port $x 5 h$. The bit designations are as follows:

| BIT | Name | Read/Write | Description |
| :--- | :--- | :--- | :--- |
| 6-0 | Address Pointer | Read/Write | Address of RAM and Registers. See the tables below for detail. |
| 7 | Busy | Read Only | A one indicates the device is busy because of an Serial Bus transaction or <br> another ISA bus transaction. With checking this bit, multiple ISA drivers can <br> use LM79 without interfering with each other or a Serial Bus driver. <br> It is the user's responsibility not to have a Serial Bus and ISA bus operations at <br> the same time. <br> This bit is: <br> Set: with a write to Port x5h or when a Serial Bus transaction is in progress. <br> Reset: with a write or read from Port x6h if it is set by a write to Port x5h, or <br> when the Serial Bus transaction is finished. |


| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| Busy <br> (ower On <br> default 0) | A6 | A5 | Address Pointer (Power On default 00h) |  |  |  |  |

Address Pointer Index (A6-A0)

| Registers and RAM | A6 - A0 in <br> hex | Power On Value of <br> Registers: <7:0> in <br> binary | Notes |
| :--- | :--- | :--- | :--- |
| Configuration Register | 40 h | 00001000 |  |
| Interrupt Status Register 1 | 41 h | 00000000 | Auto-increment to the address of Interrupt Status <br> Register 2 after a read or write to Port x6h. |
| Interrupt Status Register 2 | 42 h | 00000000 | Auto-increment to the address of SMI\# Mask <br> Register 2 after a read or write to Port x6h. |
| SMI\# Mask Register 1 | 43 h | 00000000 | Auto-increment to the address of NMI Mask Register <br> 2 after a read or write to Port x6h. |
| SMI\# Mask Register 2 | 44 h | 00000000 | 00000000 |

## Functional Description (Continued)

| Registers and RAM | A6 - A0 in <br> hex | Power On Value of <br> Registers: $<7: 0>$ in <br> binary | Notes |
| :--- | :--- | :--- | :--- |
| POST RAM | $00-1$ Fh |  | Auto-increment to the next location after a read or <br> write to Port x6h and stop at 1Fh. |
| Value RAM | $20-3$ Fh |  |  |
| Value RAM | $60-7 \mathrm{Fh}$ |  | Auto-increment to the next location after a read or <br> write to Port x6h and stop at 7Fh. |

### 13.2 Data Register (Port x6h)

power on default <7:0> $=00 \mathrm{~h}$

| BIT | Name | Read/Write | Description |
| :--- | :--- | :--- | :--- |
| $7-0$ | Data | Read/Write | Data to be read from or to be written to RAM and Register. |

### 13.3 Configuration Register - Address 40h

Power on default <7:0> = 00001000 binary

| BIT | Name | Read/Write | Description |
| :--- | :--- | :--- | :--- |
| 0 | Start | Read/Write | A one enables startup of monitoring operations, a zero puts the part in <br> standby mode. <br> Note:The outputs of Interrupt pins will not be cleared if the user writes a zero <br> to this location after an interrupt has occurred unlike "INT_Clear" bit. |
| 1 | SMI\# enable | Read/Write | A one enables the SMI\# Interrupt output |
| 2 | NMI/IRQ\# <br> enable | Read/Write | A one enables the NMI/IRQ\# Interrupt output |
| 3 | INT_Clear | Read/Write | A one disables the SMI\# and NMI/IRQ\# outputs without affecting the <br> contents of Interrupt Status Registers. The device will stop monitoring. It will <br> resume upon clearing of this bit. |
| 4 | RESET\# | Read/Write | A one outputs at least a 20 ms active low reset signal at RESET\# if $<7>=1$ in <br> SMI\# Mask Register 2. This bit is cleared once the pulse has gone inactive. |
| 5 | NMI/IRQ\# select | Read/Write | A one selects NMI, and a zero selects IRQ\#. |
| 6 | Power Switch <br> Bypass\# | Read/Write | A one in this bit drives a zero on Power Switch Bypass\# pin. |
| 7 | INITIALIZATION | Read/Write | A one restores power on default value to all registers except the Serial Bus <br> Address register. This bit clears itself since the power on default is zero. |

### 13.4 Interrupt Status Register 1 - Address 41h

power on default <7:0> $=00 \mathrm{~h}$

| BIT | Name | Read/Write | Description |
| :--- | :--- | :--- | :--- |
| 0 | IN0 | Read Only | A one indicates a High or Low limit has been exceeded. |
| 1 | IN1 | Read Only | A one indicates a High or Low limit has been exceeded. |
| 2 | IN2 | Read Only | A one indicates a High or Low limit has been exceeded. |
| 3 | IN3 | Read Only | A one indicates a High or Low Limit has been exceeded. |
| 22 |  |  |  |

Functional Description (Continued)

| BIT | Name | Read/Write | Description |
| :--- | :--- | :--- | :--- |
| 4 | Temperature | Read Only | A one indicates a High or Low limit has been exceeded. |
| 5 | BTI\# | Read Only | A one indicates an interrupt has occurred from the Board Temperature <br> Interrupt (BTI\#) input (O.S. output of multiple LM75 chips). |
| 6 | FAN1 | Read Only | A one indicates the fan count limit has been exceeded. |
| 7 | FAN2 | Read Only | A one indicates the fan count limit has been exceeded. |

### 13.5 Interrupt Status Register 2 - Address 42h

power on default <7:0> $=00 \mathrm{~h}$

| BIT | Name | Read/Write | Description |
| :--- | :--- | :--- | :--- |
| 0 | IN4 | Read Only | A one indicates a High or Low limit has been exceeded. |
| 1 | -IN5 | Read Only | A one indicates a High or Low limit has been exceeded. |
| 2 | -IN6 | Read Only | A one indicates a High or Low limit has been exceeded. |
| 3 | FAN3 | Read Only | A one indicates the fan count limit has been exceeded. |
| 4 | Chassis <br> Intrusion | Read Only | A one indicates Chassis Intrusion has gone high. |
| 5 | FIFO Overflow | Read Only | A one indicates an overflow in FIFO (POST RAM) i.e. 32nd location in FIFO <br> has been written via Port xOh or x4h. |
| 6 | SMI_IN\# | Read Only | A one indicates SMI_IN\# has gone low. |
| 7 | Reserved | Read Only |  |

### 13.6 SMI\# Mask Register 1 - Address 43h

power on default <7:0> $=00 \mathrm{~h}$

| BIT | Name | Read/Write | Description |
| :--- | :--- | :--- | :--- |
| 0 | IN0 | Read/Write | A one disables the corresponding interrupt status bit for SMI\# interrupt. |
| 1 | IN1 | Read/Write | A one disables the corresponding interrupt status bit for SMI\# interrupt. |
| 2 | IN2 | Read/Write | A one disables the corresponding interrupt status bit for SMI\# interrupt. |
| 3 | IN3 | Read/Write | A one disables the corresponding interrupt status bit for SMI\# interrupt. |
| 4 | Temperature | Read/Write | A one disables the corresponding interrupt status bit for SMI\# interrupt. |
| 5 | BTI\# | Read/Write | A one disables the corresponding interrupt status bit for SMI\# interrupt. |
| 6 | FAN1 | Read/Write | A one disables the corresponding interrupt status bit for SMI\# interrupt. |
| 7 | FAN2 | Read/Write | A one disables the corresponding interrupt status bit for SMI\# interrupt. |

## Functional Description (Continued)

### 13.7 SMI\# Mask Register 2 - Address 44h

power on default $\langle 7: 0\rangle=00 \mathrm{~h}$

| Bit | Name | Read/Write | Description |
| :--- | :--- | :--- | :--- |
| 0 | IN4 | Read/Write | A one disables the corresponding interrupt status bit for SMI\# interrupt. |
| 1 | -IN5 | Read/Write | A one disables the corresponding interrupt status bit for SMI\# interrupt. |
| 2 | -IN6 | Read/Write | A one disables the corresponding interrupt status bit for SMI\# interrupt. |
| 3 | FAN3 | Read/Write | A one disables the corresponding interrupt status bit for SMI\# interrupt. |
| 4 | Chassis <br> Intrusion | Read/Write | A one disables the corresponding interrupt status bit for SMI\# interrupt. |
| 5 | FIFO Overflow | Read/Write | A one disables the corresponding interrupt status bit for SMI\# interrupt. |
| 6 | SMI_IN\# | Read/Write | A one disables the corresponding interrupt status bit for SMI\# interrupt. |
| 7 | RESET\# Enable | Read/Write | $<7>=1$ in SMI\# Mask Register 2 enables the RESET\# in the Configuration <br> Register. |

13.8 NMI Mask Register 1 - Address 45h

Power on default <7:0> = 00h

| BIT | Name | Read/Write | Description |
| :--- | :--- | :--- | :--- |
| 0 | IN0 | Read/Write | A one disables the corresponding interrupt status bit for NMI/IRQ\# interrupt. |
| 1 | IN1 | Read/Write | A one disables the corresponding interrupt status bit for NMI/IRQ\# interrupt. |
| 2 | IN2 | Read/Write | A one disables the corresponding interrupt status bit for NMI/IRQ\# interrupt. |
| 3 | IN3 | Read/Write | A one disables the corresponding interrupt status bit for NMI/IRQ\# interrupt. |
| 4 | Temperature | Read/Write | A one disables the corresponding interrupt status bit for NMI/IRQ\# interrupt. |
| 5 | BTI\# | Read/Write | A one disables the corresponding interrupt status bit for NMI/IRQ\# interrupt. |
| 6 | FAN1 | Read/Write | A one disables the corresponding interrupt status bit for NMI/IRQ\# interrupt. |
| 7 | FAN2 | Read/Write | A one disables the corresponding interrupt status bit for NMI/IRQ\# interrupt. |

## Functional Description (Continued)

13.9 NMI Mask Register 2 - Address 46h

Power on <7:0> = 01000000 binary

| BIT | Name | Read/Write | Description |
| :--- | :--- | :--- | :--- |
| 0 | IN4 | Read/Write | A one disables the corresponding interrupt status bit for NMI/IRQ\# interrupt. |
| 1 | -IN5 | Read/Write | A one disables the corresponding interrupt status bit for NMI/IRQ\# interrupt. |
| 2 | -IN6 | Read/Write | A one disables the corresponding interrupt status bit for NMI/IRQ\# interrupt. |
| 3 | FAN3 | Read/Write | A one disables the corresponding interrupt status bit for NMI/IRQ\# interrupt. |
| 4 | Chassis <br> Intrusion | Read/Write | A one disables the corresponding interrupt status bit for NMI/IRQ\# interrupt. |
| 5 | FIFO Overflow | Read/Write | A one disables the corresponding interrupt status bit for NMI/IRQ\# interrupt. |
| 6 | SMI_IN\# | Read/Write | A one disables the corresponding interrupt status bit for NMI/IRQ\# interrupt. <br> Note: The Power on default is $\mathbf{1}$ for this bit. |
| 7 | Chassis Clear | Read/Write | A one outputs a minimum 20 ms active low pulse on the Chassis Intrusion <br> pin. The register bit self clears after the pulse has been output. |

13.10 VID/Fan Divisor Register - Address 47h

Power on - <7:4> is 0101 binary, and <3:0> is mapped to VID <3:0>

| BIT | Name | Read/Write | Description |
| :--- | :--- | :--- | :--- |
| $3-0$ | VID <3:0> | Read Only | The VID <3:0> inputs |
| $5-4$ | FAN1 RPM <br> control | Read/Write | FAN1 Speed Control. <br> $<5: 4>=00-$ divide by 1; <br> $<5: 4>=01-$-divide by 2; <br> $<5: 4>=10-$ divide by 4; <br> $<5: 4>=11-$ divide by 8. |
| $7-6$ | FAN2 RPM <br> control | Read/Write | FAN2 Speed Control. <br> $<7: 6>=00-$ divide by 1; <br> $<7: 6>=01-$ divide by 2; <br> $<7: 6>=10-$ divide by 4; <br> $<7: 6>=11-$ divide by 8. |

## Functional Description (Continued)

13.11 Serial Bus Address Register - Address 48h

Power on Serial Bus address <6:0> = 0101101 and $<7>=0$ binary

| BIT | Name | Read/Write | Description |
| :--- | :--- | :--- | :--- |
| $6-0$ | Serial Bus <br> Address | Read/Write | Serial Bus address $<6: 0>$ |
| 7 | Reserved | Read only |  |

13.12 VID4/Device ID Register - Address 49h

Power on Device ID <7:1>=1000000 binary and <0>=VID4

| BIT | Name | Read/Write | Description |
| :--- | :--- | :--- | :--- |
| $7-1$ | Device ID | Read Only | LM79 device identification. The LM78 has $<7>=0$. |
| 0 | VID4 | Read Only | VID4 input |

13.13 POST RAM - Address 00h - 1Fh

The address pointer for the POST RAM auto-increments when written to at Port x0h or x 4 h . Once the address pointer reaches 1Fh, a FIFO overflow interrupt will be generated and the FIFO will stop incrementing. Normal reads via port $x 5 \mathrm{~h}$ and x 6 h auto-increment a separate pointer, and will not cause a FIFO overflow interrupt.

Functional Description (Continued)
13.14 Value RAM - Address 20 h - $\mathbf{3 F h}$ or $\mathbf{6 0 h} \mathbf{- 7 F h}$ (auto-increment)

| Address A6- A0 | Address A6 - A0 with autoincrement | Description |
| :---: | :---: | :---: |
| 20h | 60h | INO reading |
| 21h | 61h | IN1 reading |
| 22h | 62h | IN2 reading |
| 23h | 63h | IN3 reading |
| 24h | 64h | IN4 reading |
| 25h | 65h | -IN5 reading |
| 26h | 66h | -IN6 reading |
| 27h | 67h | Temperature reading |
| 28h | 68h | FAN1 reading <br> Note: This location stores the number of counts of the internal clock per revolution. |
| 29h | 69h | FAN2 reading <br> Note:This location stores the number of counts of the internal clock per revolution. |
| 2Ah | 6Ah | FAN3 reading <br> Note:This location stores the number of counts of the internal clock per revolution. |
| 2Bh | 6Bh | IN0 High Limit |
| 2Ch | 6Ch | INO Low Limit |
| 2Dh | 6Dh | IN1 High Limit |
| 2Eh | 6Eh | IN1 Low Limit |
| 2Fh | 6Fh | IN2 High Limit |
| 30h | 70h | IN2 Low Limit |
| 31 h | 71h | IN3 High Limit |
| 32h | 72h | IN3 Low Limit |
| 33h | 73h | IN4 High Limit |
| 34h | 74h | IN4 Low Limit |
| 35h | 75h | -IN5 High Limit |
| 36h | 76h | -IN5 Low Limit |
| 37h | 77h | -IN6 High Limit |
| 38h | 78h | -IN6 Low Limit |
| 39h | 79h | Over Temperature Limit (High) |

## Functional Description (Continued)

| Address A6- A0 | Address A6 - A0 with auto- <br> increment | Description |
| :--- | :--- | :--- |
| 3Ah | 7Ah | Temperature Hysteresis Limit (Low) |
| $3 B h$ | 7Bh | FAN1 Fan Count Limit <br> Note It is the number of counts of the internal clock for the Low <br> Limit of the fan speed. |
| 3Ch | 7Ch | FAN2 Fan Count Limit <br> Note: It is the number of counts of the internal clock for the Low <br> Limit of the fan speed. |
| 3Dh | 7Dh | FAN3 Fan Count Limit <br> Note: It is the number of counts of the internal clock for the Low <br> Limit of the fan speed. |
| 3E -3Fh | $7 \mathrm{E}-7 \mathrm{Fh}$ | Reserved |

Setting all ones to the high limits for voltages and fans (0111 1111 binary for temperature) means interrupts will never be generated except the case when voltages go below the low limits.

Note:
For the high limits of the voltages, the device is doing a greater than comparison. For the low limits, however, it is doing a less than or equal comparison.

## Typical Application



Figure 11. In this PC application the LM79 monitors temperature, fan speed for 3 fans, and 7 power supply voltages. It also monitors the O.S. Output of up to 8 LM75 digital temperature sensors as well as an optical chassis intrusion detector.

## Physical Dimensions inches (millimeters)



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[^0]:    Transistor Count
    MTBF (based on limited test data)

[^1]:    Transistor Count
    MTBF (based on limited test data)

[^2]:    - Capacitance across $\mathbf{R}_{\mathrm{f}}$
    - Do not place a capacitor across $R_{f}$
    - Keep traces connecting $R_{f}$ separated and as short as possible
    - Capacitive Loads
    - Place a small resistor ( $20-50 \Omega$ ) between the output and $\mathrm{C}_{\mathrm{L}}$
    - Long traces and/or lead lengths between $\mathbf{R}_{\mathrm{f}}$ and the CLC5523

[^3]:    $\dagger$ Patent Number 5,382,918.

[^4]:    $\mathrm{C}_{\mathrm{IN}}-470 \mu \mathrm{~F}, 50 \mathrm{~V}$, Aluminum Electrolytic Panasonic, "HFQ Series"
    COUT $-220 \mu \mathrm{~F}, 35 \mathrm{~V}$ Aluminum Electrolytic Panasonic, "HFQ Series"
    D1 -5A, 40V Schottky Rectifier, 1N5825

    - $47 \mu \mathrm{H}, \mathrm{L} 39$, Renco, Through Hole
    - $1 \mathrm{k} \Omega, 1 \%$
    -Use formula in Design Procedure
    FF - See Figure 4.

[^5]:    $\dagger$ Patent Number 5,382,918.
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[^6]:    $\dagger$ Patent Number 5,382,918.

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