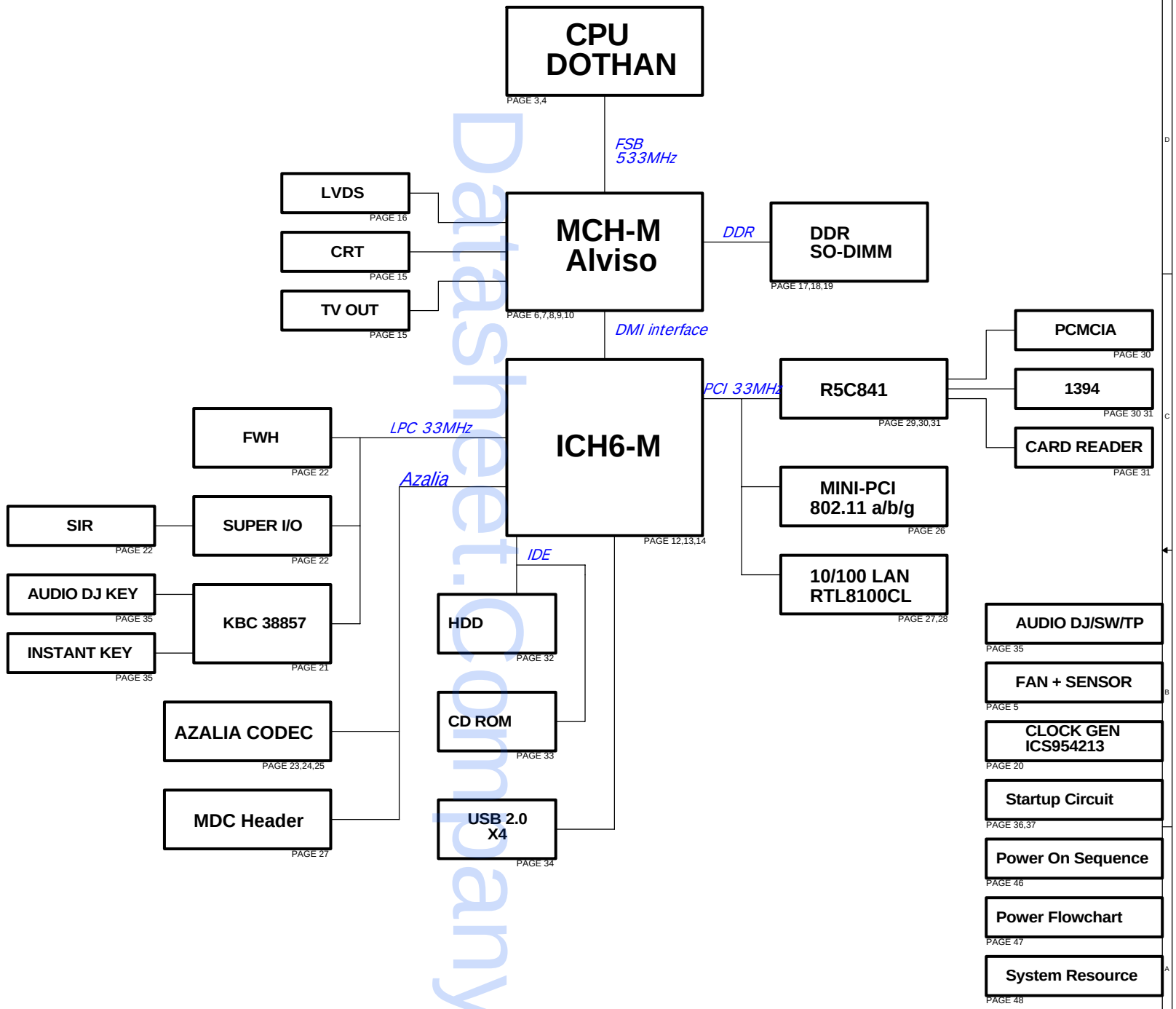
A3E CONTEXT



Title : BLOCK DIAGRAM

Engineer: Quan-Tai Lin

ASUSTeK COMPUTER INC

Size	Project Name	Rev
Custom	A3E	2.2

Date: Thursday, May 05, 2005 Sheet 1 of 51

REVISION LIST

R1.0 2005/01/10

POWER INTERFACE

SIGNALS	TYPE	POWER
PM_PSI#	O	+VCCP
VR_VID[5:0]	O	+VCCP
VRON	O	+3.3V
PM_DPRSLPVR	O	+3.3V
CPU_STP#	O	+3.3V
RST_BTN#	O	+3.3V
CLK_EN#	I	+3.3V
DELAY_VR_PWRGD	I	+3.3V
OTP_RESET#	I	+3.3V
SHUT_DOWN#	I	+3.3V
BAT_LEARN	I	+3.3V
BAT_LLOW#_OC	I	+3.3V
BAT_IN#_OC	I	+3.3V
CHG_EN#	I	+3.3V
CHG_FULL_OC	I	+3.3V
CHG_LED_UP	I	+3.3V
SMCLK_BAT1	IO	+3.3V
SMDATA_BAT1	IO	+3.3V
SUSB#	O	+3.3V
SUSC#	O	+3.3V
1.8V_PWRGD	I	+3.3V
1.5VS_PWRGD	I	+3.3V
VSUS_ON	O	+3.3V
ACIN_OC	I	+3.3V
ACIN#	I	AC_BAT_SYS
+3VA	PWR	+3.3V
+5VA	PWR	+5V
+5VLCM	PWR	+5VLCM
A/D_DOCK_IN	PWR	DC
AC_BAT_SYS	PWR	DC

POWER PLANE

POWER	VOLTAGE	CURRENT
+VCORE	0.7 - 1.77V	27A
+VCCP	1.05 - 1.2V	3.95A
+VCC_GMCH	1.05V	4.12A
+0.9VS	1.25V	0.85A
+1.5VS	1.5V	4.33A
+1.5V	1.5V	300 mA
~~+1.5VSUS~~	~~1.5V~~	~~270 mA~~
+2.5V	2.5V	6.68A
+2.5VS	2.5V	0.3 A
+3VS	3.3V	1.732A
+3V	3.3V	1.515A
+3VSUS	3.3V	540 mA
+5VS	5V	4.1A
+5V	5V	0.5A
+5VSUS	5V	0.5A
+12V	12V	0.25A
+12VS	12V	0.25A

IMPEDENCE

Single-Ended

27.4 OHM WIDTH

TOP/BOT 18 mils

37.5 OHM WIDTH

TOP/BOT 11 mils
IN1/IN2 9.5 mils

50 OHM WIDTH

TOP/BOT 6 mils
IN1/IN2 5 mils

55 OHM WIDTH

TOP/BOT 5.5 mils
IN1/IN2 4.5 mils

75 OHM WIDTH

TOP/BOT 4 mils
IN1/IN3 3.5 mils

Differential

85 OHM WIDTH/SPACE

TOP/BOT 5.5 mils/ 4 mils
IN1/IN2 4.5 mils/ 4 mils

90 OHM WIDTH/SPACE

TOP/BOT 5.5 mils/ 5 mils
IN1/IN2 4.5 mils/ 5 mils

100 OHM WIDTH/SPACE

TOP/BOT 6 mils/ 11 mils
IN1/IN2 5 mils/ 12 mils

110 OHM WIDTH/SPACE

TOP/BOT 5 mils/ 13 mils
IN1/IN2 4 mils/ 12 mils

PCI INTERFACE

PCI_REQ#

MINIPCI	PCI_REQ#3
10/100	PCI_REQ#2
CB&1394	PCI_REQ#1

IDSEL

MINIPCI	PCI_AD19
10/100	PCI_AD16
CB&1394	PCI_AD17

PCB STACK-UP

PCB THICKNESS: 1.6 mm

L1 TOP
L2 GND
L3 IN1
L4 IN2
L5 GND
L6 BOT

PAGE 38

```
SIGNAL  IN:   VR_VID[0..5]
              PM_DPRSLPVR
              STP_CPU#
              PM_PSI#
              CPU_VRON
              MCH_OK
        OUT:  DELAY_VR_PWRGD
              CLK_PWR_GD#

POWER   IN:   AC_BAT_SYS
              +5VO
              +3VO
        OUT:  +VCORE
```

PAGE 39

```
SIGNAL   IN:  SUSC#_PWR
              VSUS_ON

POWER    IN:  AC_BAT_SYS

         OUT: +12VO
              +3VO
              +5VO
```

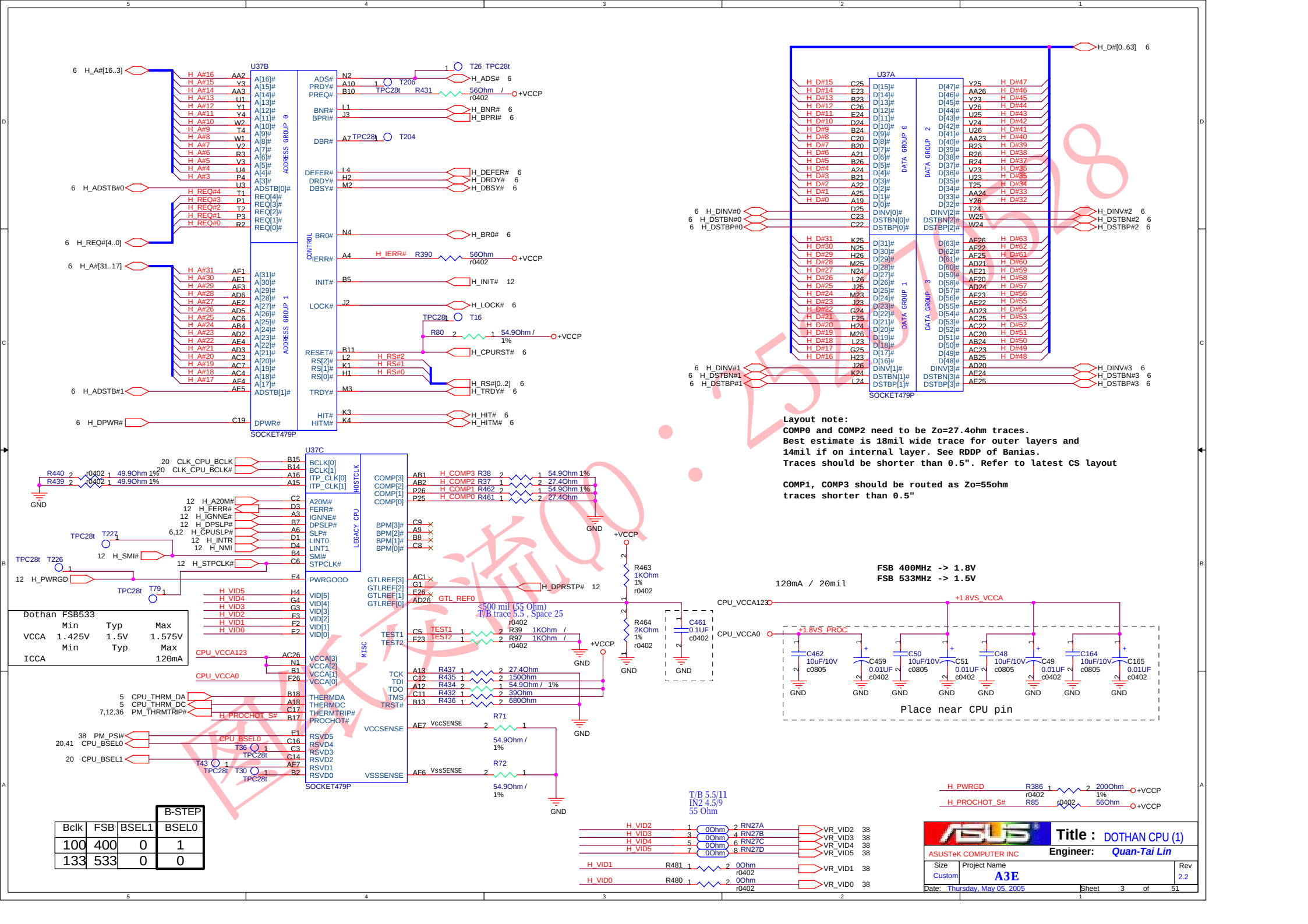
PAGE 40

```
SIGNAL  IN: SUSB#_PWR
            SUSC#_PWR
            CPU_VRON

POWER   IN: AC_BAT_SYS
            +5VO

       OUT: +1.8V
            +1.5VS
            +2.5VS
            +VCC_GMCH_CORE
            +5VALWAYS
            +3VALWAYS
            +VCCP
```

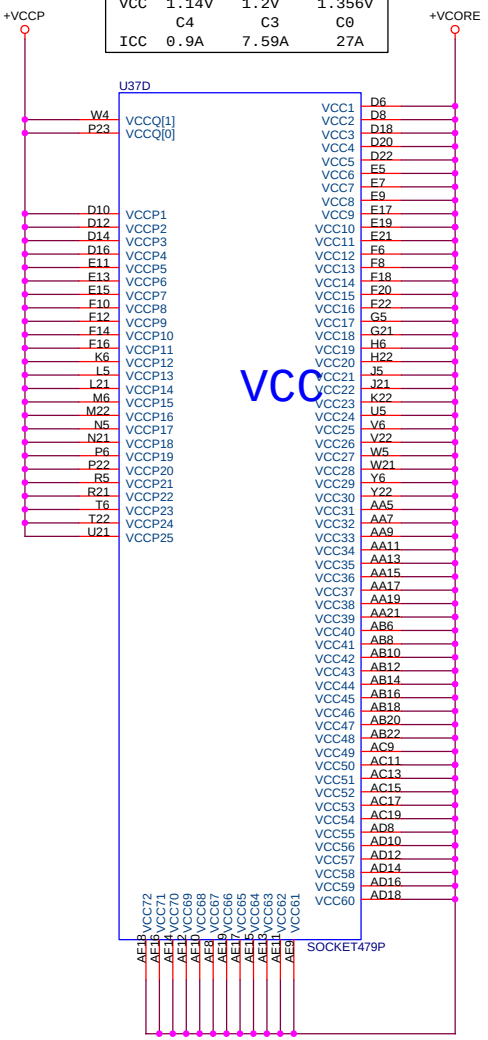
PAGE 41

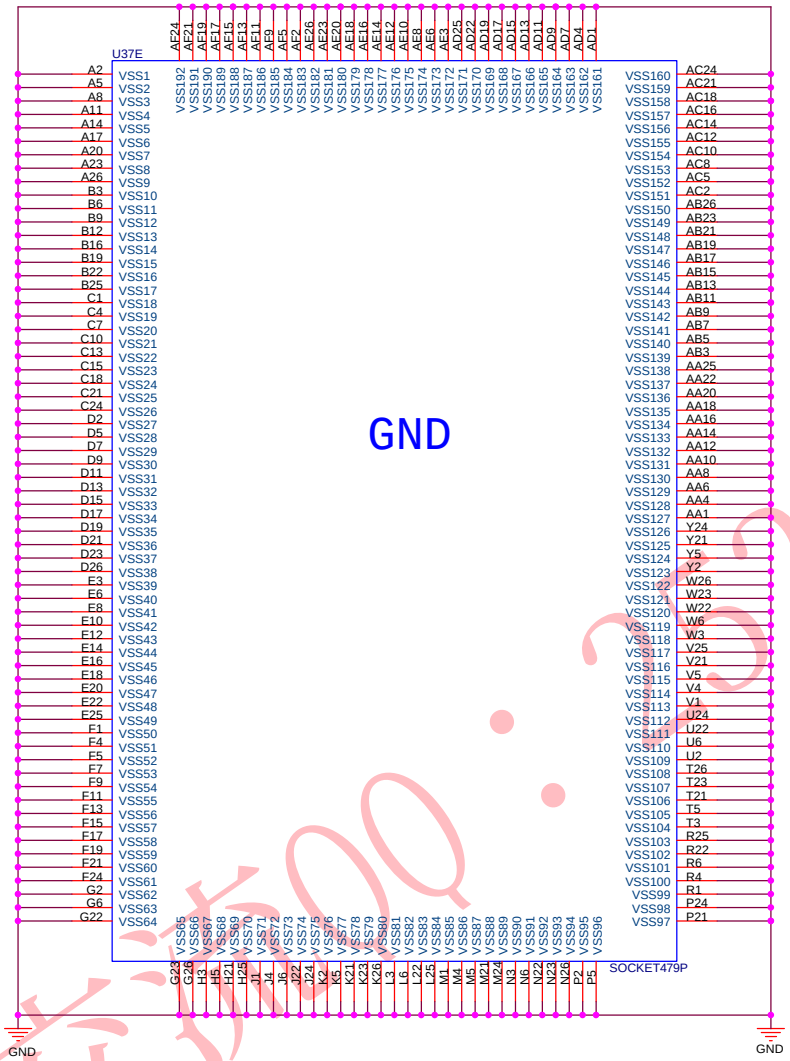
```
SIGNAL  IN: SUSB#_PWR

POWER   IN: +3V
            +1.8V

       OUT: +0.9VS
```

ASUSTeK COMPUTER INC	Title : REVISION LIST	
	Engineer: Quan-Tai Lin	
Size: Custom	Project Name: A3E	Rev: 2.2
Date: Thursday, May 05, 2005	Sheet 2 of 51	


U37B
ADDRESS GROUP 0
ADDRESS GROUP 1
CONTROL
SOCKET479P
U37A
DATA GROUP 0
DATA GROUP 1
DATA GROUP 2
DATA GROUP 3
SOCKET479P
U37C
HOSTCLK
LEGACY CPU
MISC
SOCKET479P
Layout note:
COMP0 and COMP2 need to be Zo=27.4ohm traces.
Best estimate is 18mil wide trace for outer layers and
14mil if on internal layer. See RDDP of Banias.
Traces should be shorter than 0.5". Refer to latest CS layout
COMP1, COMP3 should be routed as Zo=55ohm
traces shorter than 0.5"
FSB 400MHz -> 1.8V
FSB 533MHz -> 1.5V
120mA / 20mil
Place near CPU pin
Dothan FSB533
Min Typ Max
VCCA 1.425V 1.5V 1.575V
Min Typ Max
ICCA 120mA
Bclk FSB BSEL1 B-STEP BSEL0
100 400 0 1
133 533 0 0
Title : DOTHAN CPU (1)
ASUSTeK COMPUTER INC
Engineer: Quan-Tai Lin
Size Custom
Project Name A3E
Rev 2.2
Date: Thursday, May 05, 2005
Sheet 3 of 51

Dothan FSB533	LFM	TYP	HFM
VCC	1.14V	1.2V	1.356V
	C4	C3	C0
ICC	0.9A	7.59A	27A



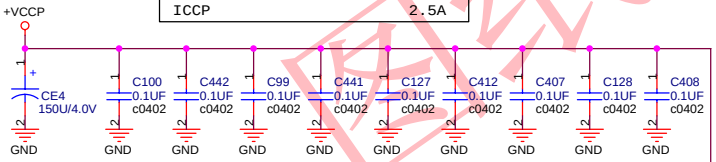


MOBILE DOTHAN VID TABLE

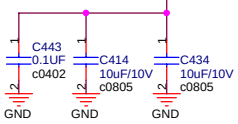
VID[5..0]	Voltage	VID[5..0]	Voltage
0 0 0 0 0 0	1.708V	1 0 0 0 0 0	1.196V
0 0 0 0 0 1	1.692V	1 0 0 0 0 1	1.180V
0 0 0 0 1 0	1.676V	1 0 0 0 1 0	1.164V
0 0 0 0 1 1	1.660V	1 0 0 0 1 1	1.148V
0 0 0 1 0 0	1.644V	1 0 0 1 0 0	1.132V
0 0 0 1 0 1	1.628V	1 0 0 1 0 1	1.116V
0 0 0 1 1 0	1.612V	1 0 0 1 1 0	1.100V
0 0 0 1 1 1	1.596V	1 0 0 1 1 1	1.084V
0 0 1 0 0 0	1.580V	1 0 1 0 0 0	1.068V
0 0 1 0 0 1	1.564V	1 0 1 0 0 1	1.052V
0 0 1 0 1 0	1.548V	1 0 1 0 1 0	1.036V
0 0 1 0 1 1	1.532V	1 0 1 0 1 1	1.020V
0 0 1 1 0 0	1.516V	1 0 1 1 0 0	1.004V
0 0 1 1 0 1	1.500V	1 0 1 1 0 1	0.988V
0 0 1 1 1 0	1.484V	1 0 1 1 1 0	0.972V
0 0 1 1 1 1	1.468V	1 0 1 1 1 1	0.956V
0 1 0 0 0 0	1.452V	1 1 0 0 0 0	0.940V
0 1 0 0 0 1	1.436V	1 1 0 0 0 1	0.924V
0 1 0 0 1 0	1.420V	1 1 0 0 1 0	0.908V
0 1 0 0 1 1	1.404V	1 1 0 0 1 1	0.892V
0 1 0 1 0 0	1.388V	1 1 0 1 0 0	0.876V
0 1 0 1 0 1	1.372V	1 1 0 1 0 1	0.860V
0 1 0 1 1 0	1.356V	1 1 0 1 1 0	0.844V
0 1 0 1 1 1	1.340V	1 1 0 1 1 1	0.828V
0 1 1 0 0 0	1.324V	1 1 1 0 0 0	0.812V
0 1 1 0 0 1	1.308V	1 1 1 0 0 1	0.796V
0 1 1 0 1 0	1.292V	1 1 1 0 1 0	0.780V
0 1 1 0 1 1	1.276V	1 1 1 0 1 1	0.764V
0 1 1 1 0 0	1.260V	1 1 1 1 0 0	0.748V
0 1 1 1 0 1	1.244V	1 1 1 1 0 1	0.732V
0 1 1 1 1 0	1.228V	1 1 1 1 1 0	0.716V
0 1 1 1 1 1	1.212V	1 1 1 1 1 1	0.700V

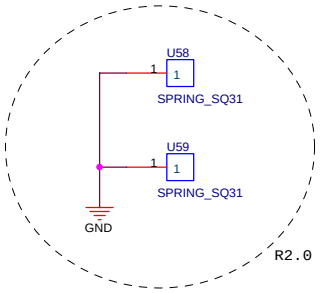
1.0V - 1.2V(+/- 5%)
S0-S1M: 2.5
A(CPU,MCH,ICH)

Dothan FSB533	Min	Typ	Max
VCCP	0.997V	1.05V	1.102V
	Min	Typ	Max
ICCP			2.5A



+VCCP (CPU) Decoupling Capacitor
(Place near CPU)





R2.0 For EMI

Title : DOTHAN CPU (2)		
ASUSTeK COMPUTER INC	Engineer: Quan-Tai Lin	
Size: Custom	Project Name: A3E	Rev: 2.2
Date: Thursday, May 05, 2005	Sheet 4 of 51	

Fan Speed Control

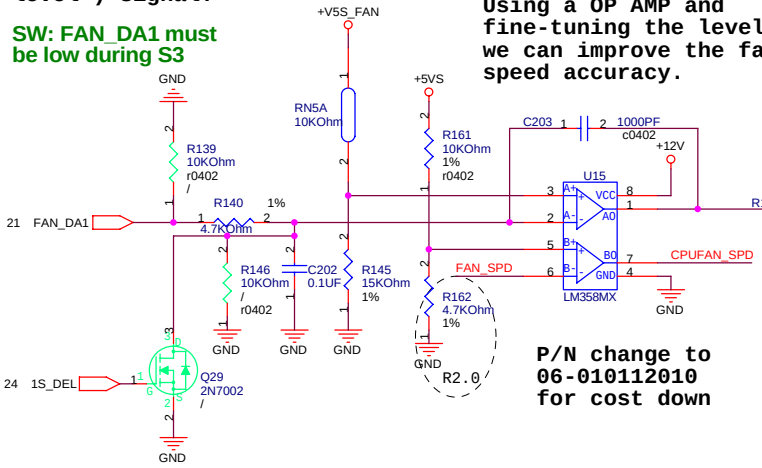
KBC will issue a analog (a voltage level) signal.

SW: FAN_DA1 must be low during S3

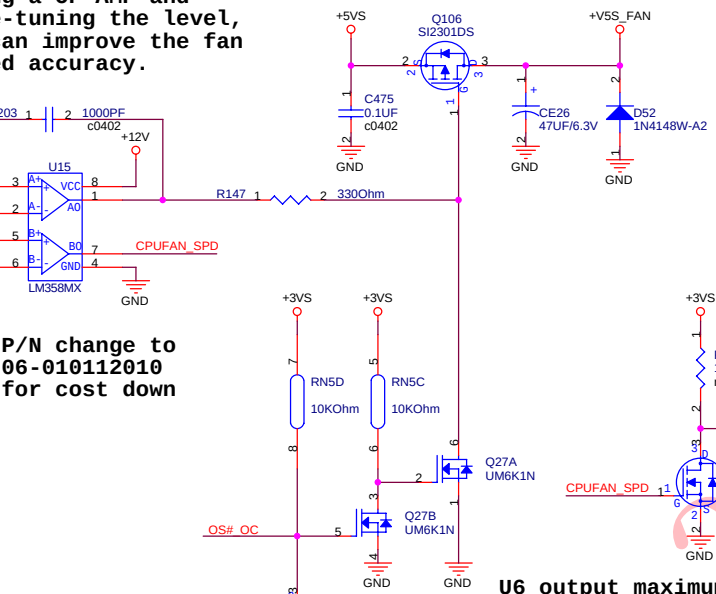
Using a OP AMP and fine-tuning the level, we can improve the fan speed accuracy.

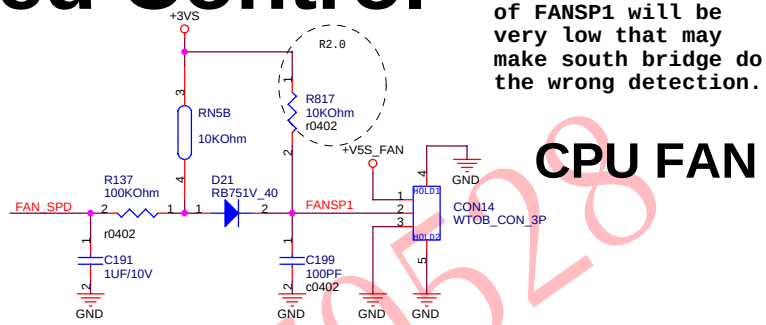
When fan speed is very slow, after RC integrator the level of FANSP1 will be very low that may make south bridge do the wrong detection.

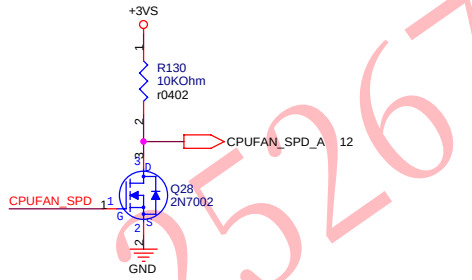
CPU FAN



P/N change to 06-010112010 for cost down







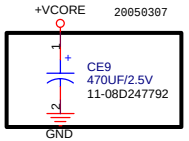
CPU FAN will be forced on:
1) Thermal Sensor Over-temperture
2) PROCHOT asserted(CPU)
3) WATCHDOG asserted(KBC)

U6 output maximum will be 10.5V (VCC-1.5V) which will damage sourth bridge. Add a MOS to tansfer it to +3V level.

Route H_THERMDA and H_THERMDC on the same layer

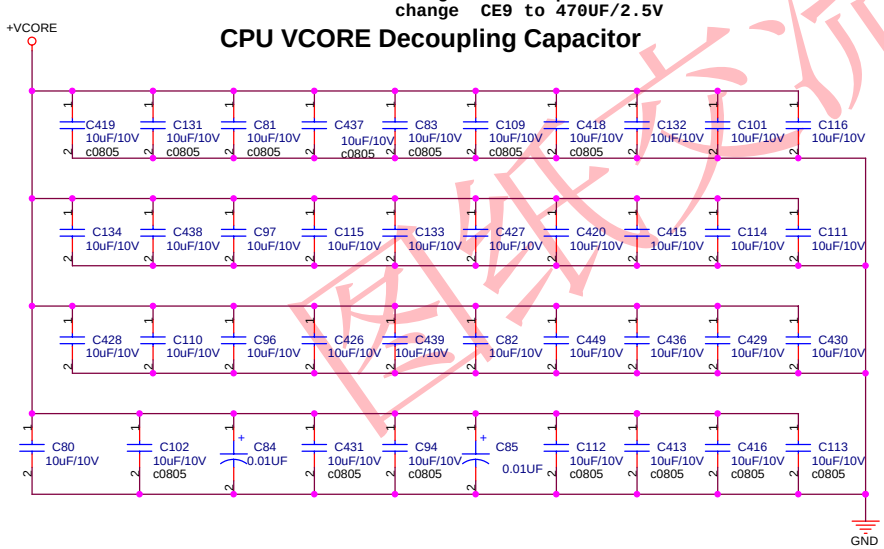
----------OTHER SIGNALS
12 mils
==========GND
10 mils
=========H_THERMDA(10 mils)
10 mils
=========H_THERMDC(10 mils)
10 mils
=========GND
12 mils
----------OTHER SIGNALS

Avoid BPSB,Power



Change CE10 to power and change CE9 to 470UF/2.5V

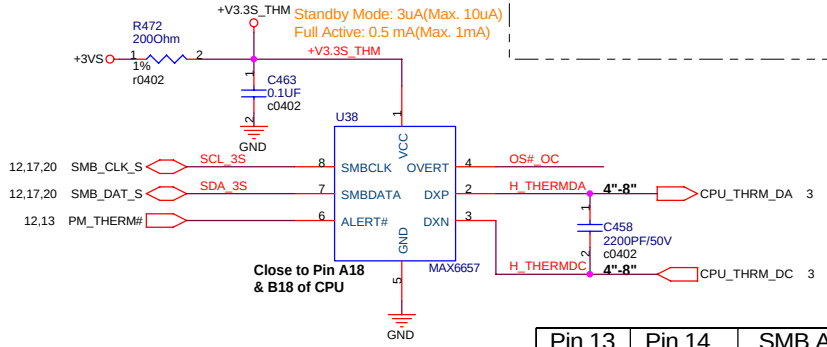
CPU VCORE Decoupling Capacitor



Mid Frequency Decoupling (Place around Processor)

High Frequency Decoupling (Place underneath Processor) using 10uF/6.3V X5R

+VCORE Bulk Decoupling



Pin 13	Pin 14	SMB Addr
1	X	5C **
0	1	5A
0	0	58

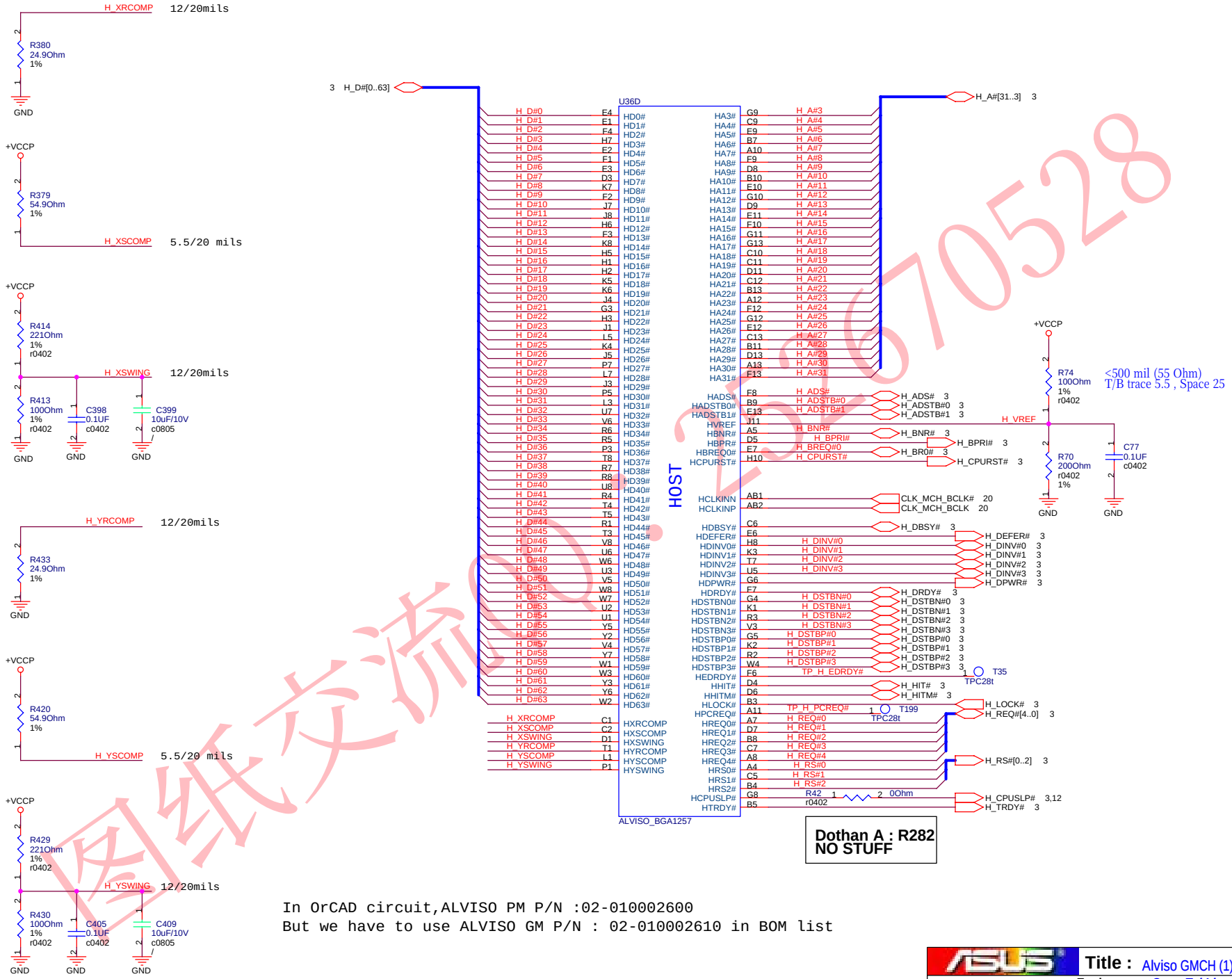
Four 200 uF are located in IMVP4

Title : THER-SENSOR,FAN

ASUSTeK COMPUTER INC Engineer: Quan-Tai Lin

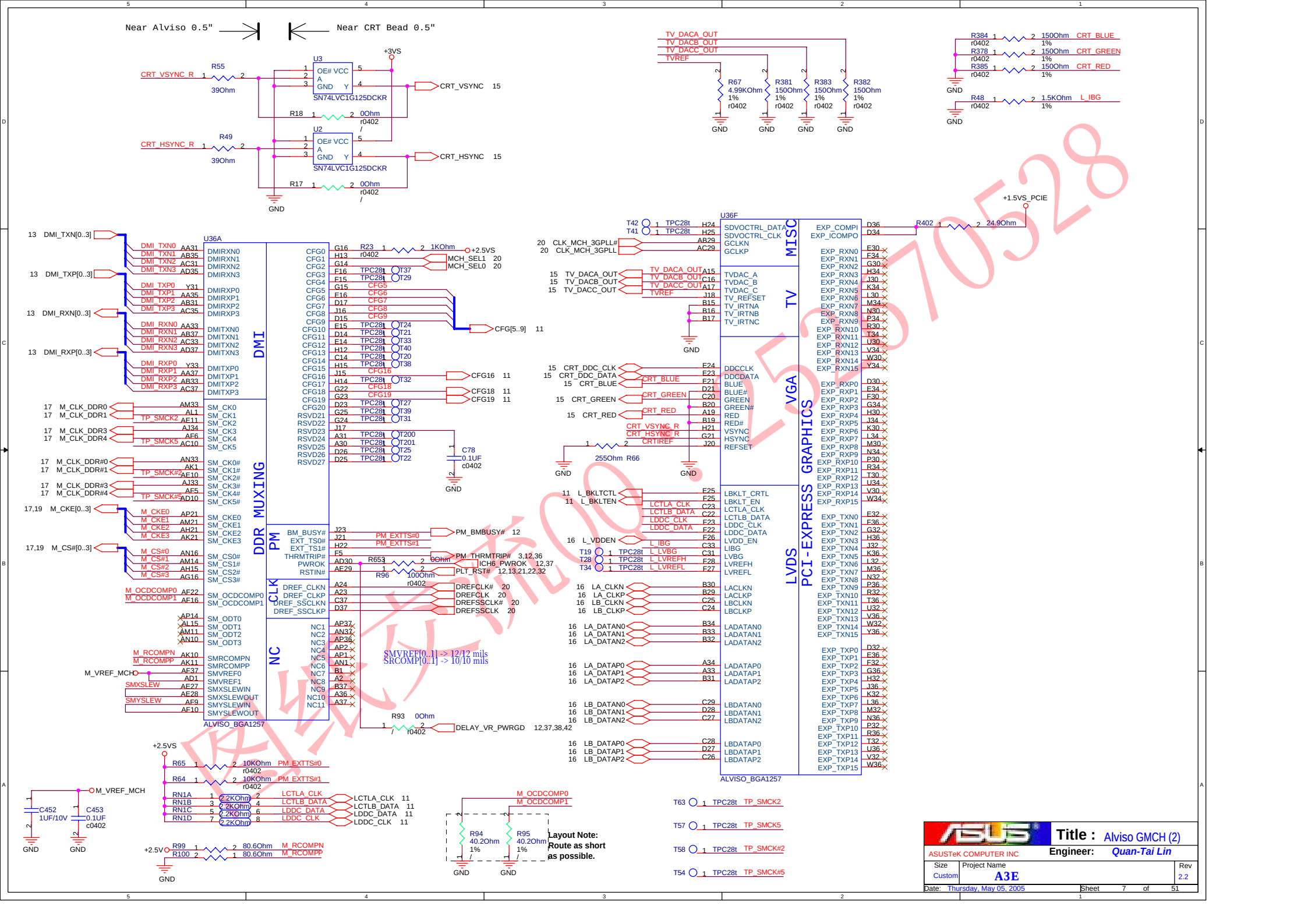
Size	Project Name	Rev
Custom	A3E	2.2

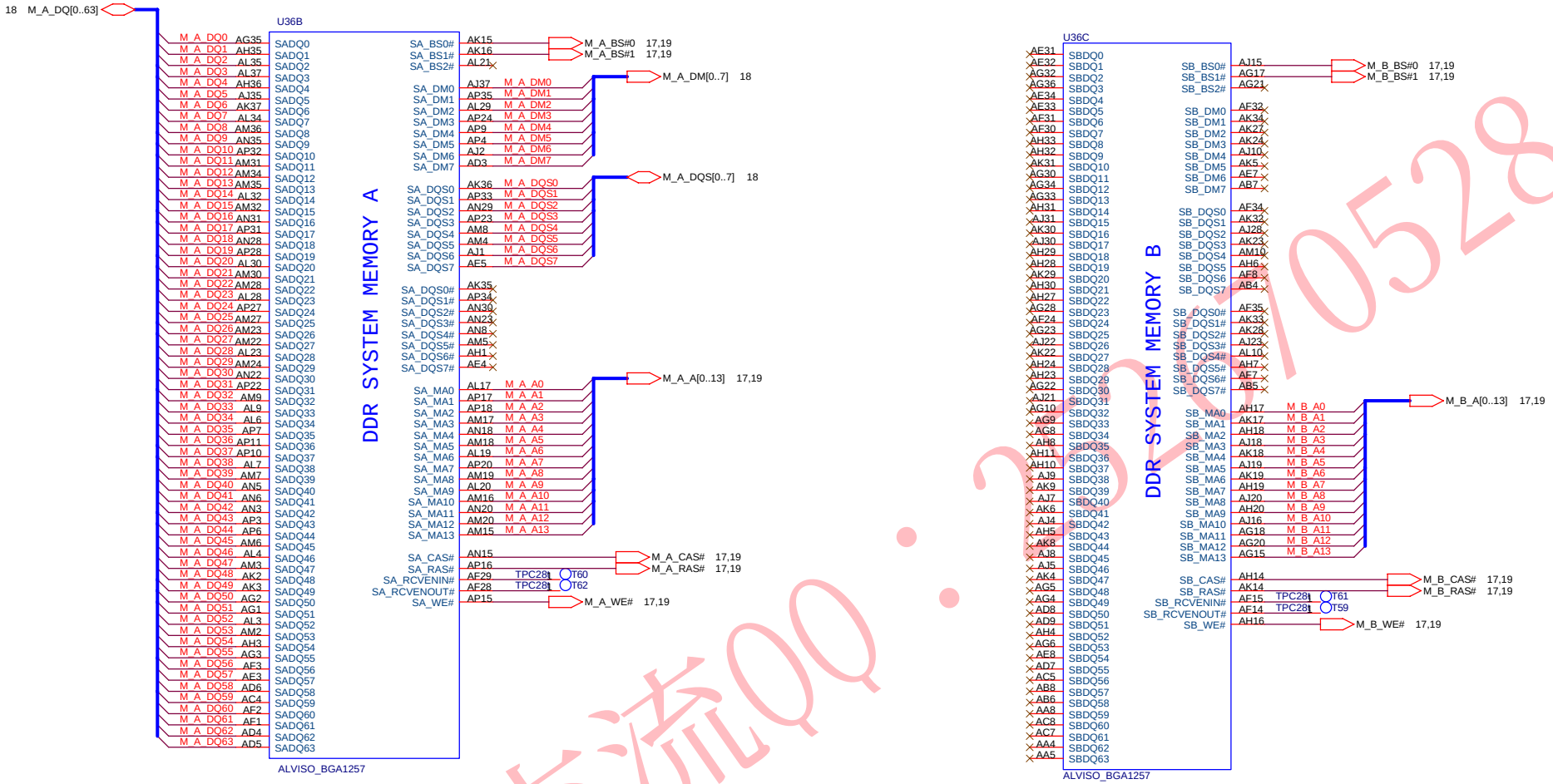
Date: Thursday, May 05, 2005 Sheet 5 of 51



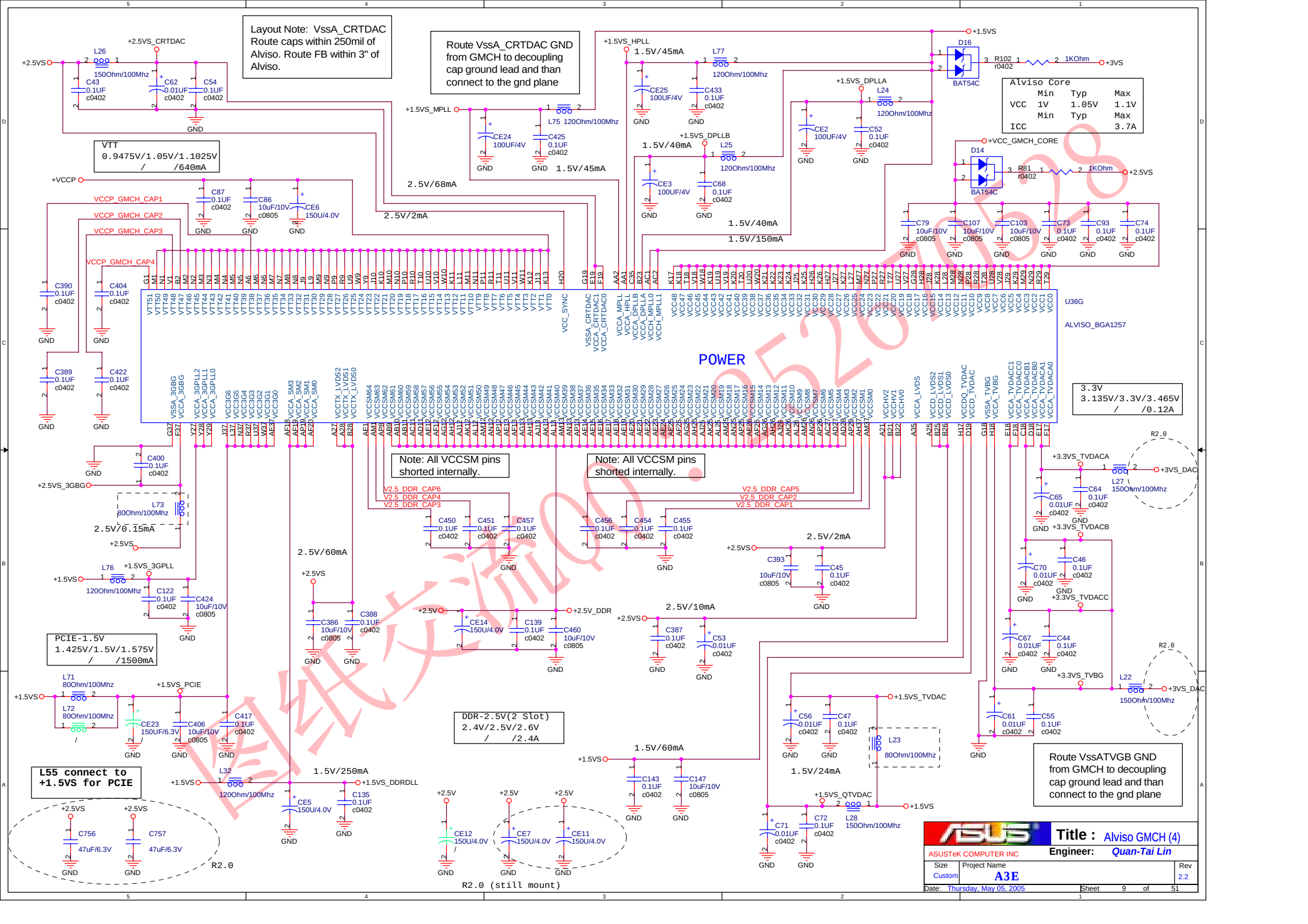
In OrCAD circuit,ALVISO PM P/N :02-010002600
But we have to use ALVISO GM P/N : 02-010002610 in BOM list

Title : Alviso GMCH (1)		
ASUSTeK COMPUTER INC	Engineer: Quan-Tai Lin	
Size: Custom	Project Name: A3E	Rev: 2.2
Date: Thursday, May 05, 2005	Sheet 6 of 51	


Near Alviso 0.5"
Near CRT Bead 0.5"
U3
SN74LVC1G125DCKR
U2
SN74LVC1G125DCKR
CRT_VSYNC_R
CRT_HSYNC_R
R55
R49
R18
R17
39Ohm
0Ohm
r0402
+3VS
GND
CRT_VSYNC 15
CRT_HSYNC 15
TV_DACA_OUT
TV_DACB_OUT
TV_DACC_OUT
TVREF
R67 4.99KOhm 1% r0402
R381 150Ohm 1% r0402
R383 150Ohm 1% r0402
R382 150Ohm 1% r0402
R384 150Ohm 1% CRT_BLUE
R378 150Ohm 1% CRT_GREEN
R385 150Ohm 1% CRT_RED
R48 1.5KOhm 1% L_IBG
U36A
DMI
DDR MUXING
PM
CLK
NC
ALVISO_BGA1257
DMI_TXN[0..3]
DMI_TXP[0..3]
DMI_RXN[0..3]
DMI_RXP[0..3]
M_CLK_DDR0
M_CLK_DDR1
M_CLK_DDR3
M_CLK_DDR4
M_CLK_DDR#0
M_CLK_DDR#1
M_CLK_DDR#3
M_CLK_DDR#4
M_CKE[0..3]
M_CS#[0..3]
M_OCDCOMP0
M_OCDCOMP1
M_RCOMPN
M_RCOMPP
M_VREF_MCH
SMXSLEW
SMYSLEW
CFG[5..9] 11
CFG16 11
CFG18 11
CFG19 11
C78 0.1UF c0402
PM_BMBUSY# 12
PM_THRMTRIP# 3,12,36
ICH6_PWROK 12,37
PLT_RST# 12,13,21,22,32
DREFCLK# 20
DREFCLK 20
DREFSSCLK# 20
DREFSSCLK 20
SMVREF[0..1] -> 12/12 mils
SRCOMP[0..1] -> 10/10 mils
R93 0Ohm
DELAY_VR_PWRGD 12,37,38,42
MISC
TV
VGA
GRAPHICS
LVDS
PCI-EXPRESS
U36F
ALVISO_BGA1257
+1.5VS_PCIE
R402 24.9Ohm
CLK_MCH_3GPLL#
CLK_MCH_3GPLL
SDVOCTRL_DATA
SDVOCTRL_CLK
GCLKN
GCLKP
TVDAC_A
TVDAC_B
TVDAC_C
TV_REFSET
TV_IRTNA
TV_IRTNB
TV_IRTNC
DDCCLK
DDCDATA
BLUE
BLUE#
GREEN
GREEN#
RED
RED#
VSYNC
HSYNC
REFSET
CRTREF
255Ohm R66
LBKLT_CRTL
LBKLT_EN
LCTLA_CLK
LCTLB_DATA
LDDC_CLK
LDDC_DATA
LVDD_EN
LIBG
LVBG
LVREFH
LVREFL
L_VDDEN
L_LVBG
L_LVREFH
L_LVREFL
LACLKN
LACLKP
LBCLKN
LBCLKP
LADATAN0
LADATAN1
LADATAN2
LADATAP0
LADATAP1
LADATAP2
LBDATAN0
LBDATAN1
LBDATAN2
LBDATAP0
LBDATAP1
LBDATAP2
EXP_COMPI
EXP_ICOMPO
EXP_RXN0
EXP_RXN1
EXP_RXN2
EXP_RXN3
EXP_RXN4
EXP_RXN5
EXP_RXN6
EXP_RXN7
EXP_RXN8
EXP_RXN9
EXP_RXN10
EXP_RXN11
EXP_RXN12
EXP_RXN13
EXP_RXN14
EXP_RXN15
EXP_RXP0
EXP_RXP1
EXP_RXP2
EXP_RXP3
EXP_RXP4
EXP_RXP5
EXP_RXP6
EXP_RXP7
EXP_RXP8
EXP_RXP9
EXP_RXP10
EXP_RXP11
EXP_RXP12
EXP_RXP13
EXP_RXP14
EXP_RXP15
EXP_TXN0
EXP_TXN1
EXP_TXN2
EXP_TXN3
EXP_TXN4
EXP_TXN5
EXP_TXN6
EXP_TXN7
EXP_TXN8
EXP_TXN9
EXP_TXN10
EXP_TXN11
EXP_TXN12
EXP_TXN13
EXP_TXN14
EXP_TXN15
EXP_TXP0
EXP_TXP1
EXP_TXP2
EXP_TXP3
EXP_TXP4
EXP_TXP5
EXP_TXP6
EXP_TXP7
EXP_TXP8
EXP_TXP9
EXP_TXP10
EXP_TXP11
EXP_TXP12
EXP_TXP13
EXP_TXP14
EXP_TXP15
T42 TPC28t H24
T41 TPC28t H25
TV_DACA_OUT A15
TV_DACB_OUT C16
TV_DACC_OUT A17
TVREF J18
CRT_DDC_CLK E24
CRT_DDC_DATA E23
CRT_BLUE E21
CRT_GREEN D21
CRT_RED C20
CRT_VSYNC_R B20
CRT_HSYNC_R A19
CRTIREF H21
L_BKLTCTL G21
L_BKLTEN J20
L_IBG E25
L_LVBG F25
L_LVREFH C23
L_LVREFL C22
T19 TPC28t
T28 TPC28t
T34 TPC28t
LA_CLKN B30
LA_CLKP B29
LB_CLKN C25
LB_CLKP C24
LA_DATAN0 B34
LA_DATAN1 B33
LA_DATAN2 B32
LA_DATAP0 A34
LA_DATAP1 A33
LA_DATAP2 B31
LB_DATAN0 C29
LB_DATAN1 D28
LB_DATAN2 C27
LB_DATAP0 C28
LB_DATAP1 D27
LB_DATAP2 C26
R65 10KOhm PM_EXTTS#0
R64 10KOhm PM_EXTTS#1
RN1A 2.2KOhm LCTLA_CLK
RN1B 2.2KOhm LCTLB_DATA
RN1C 2.2KOhm LDDC_DATA
RN1D 2.2KOhm LDDC_CLK
C452 1UF/10V
C453 0.1UF c0402
R99 80.6Ohm M_RCOMPN
R100 80.6Ohm M_RCOMPP
R94 40.2Ohm 1%
R95 40.2Ohm 1%
Layout Note: Route as short as possible.
T63 TPC28t TP_SMCK2
T57 TPC28t TP_SMCK5
T58 TPC28t TP_SMCK#2
T54 TPC28t TP_SMCK#5
Title : Alviso GMCH (2)
ASUSTeK COMPUTER INC
Engineer: Quan-Tai Lin
Size Custom
Project Name A3E
Rev 2.2
Date: Thursday, May 05, 2005
Sheet 7 of 51



ASUSTeK COMPUTER INC	Title : Alviso GMCH (3)	
	Engineer: Quan-Tai Lin	
Size: Custom	Project Name: A3E	Rev: 2.2
Date: Thursday, May 05, 2005	Sheet 8 of 51	

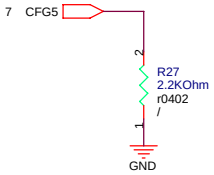

Layout Note: VssA_CRTDAC Route caps within 250mil of Alviso. Route FB within 3" of Alviso.
Route VssA_CRTDAC GND from GMCH to decoupling cap ground lead and than connect to the gnd plane
Alviso Core
Min Typ Max
VCC 1V 1.05V 1.1V
Min Typ Max
ICC 3.7A
VTT
0.9475V/1.05V/1.1025V
/ /640mA
POWER
U36G
ALVISO_BGA1257
3.3V
3.135V/3.3V/3.465V
/ /0.12A
Note: All VCCSM pins shorted internally.
Note: All VCCSM pins shorted internally.
PCIE-1.5V
1.425V/1.5V/1.575V
/ /1500mA
DDR-2.5V(2 Slot)
2.4V/2.5V/2.6V
/ /2.4A
L55 connect to +1.5VS for PCIE
Route VssATVGB GND from GMCH to decoupling cap ground lead and than connect to the gnd plane
R2.0
R2.0 (still mount)
Title : Alviso GMCH (4)
ASUSTeK COMPUTER INC
Engineer: Quan-Tai Lin
Size Custom
Project Name A3E
Rev 2.2
Date: Thursday, May 05, 2005
Sheet 9 of 51

ASUSTeK COMPUTER INC	Title : Alviso GMCH (5)	
	Engineer: Quan-Tai Lin	
Size: Custom	Project Name: A3E	Rev: 2.2
Date: Thursday, May 05, 2005	Sheet 10 of 51	

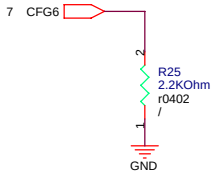
CFG[2:0] are HVCMOS (+2.5VS)
CFG[17..3] have internal pullup resistors. /AGTL+(VCCP)/
CFG[19..18] have internal pulldown resistors./HVCMOS(+2.5VS)/
SDVOCRTL_DATA has internal pulldown resistors.

SDVOCRTL_DATA :
LOW = No SDVO device present (Default)

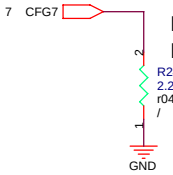
CFG5 : LOW = DMI X 2
HIGH = DMI X 4 (Default)



CFG6 : LOW = DDR2 SDRAM
HIGH = DDR SDRAM (Default)

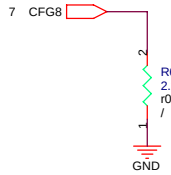


CFG7 : CPU STRAP



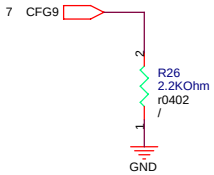
LOW = Mobile Prescott
HIGH = Dothan CPU (Default)

CFG8 : PCI-X POWER Saving

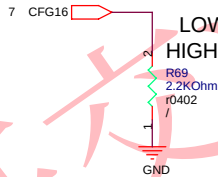


LOW = PCI-X POWER Saving
HIGH (Default)

CFG9 : PCIE GRAPHIC LANE
LOW = REVERSE LANE
HIGH = NORMAL OPERATION (Default)

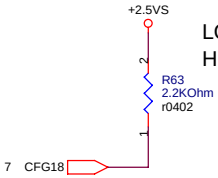


CFG16 : FSB DYNAMIC ODT



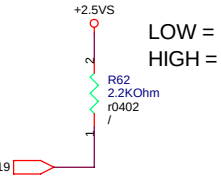
LOW = Dynamic ODT Disabled
HIGH = Dynamic ODT Enabled (Default)

CFG18 : VCC SELECT

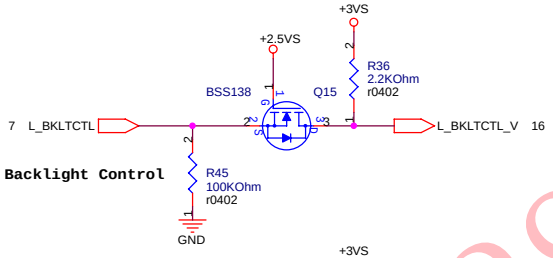


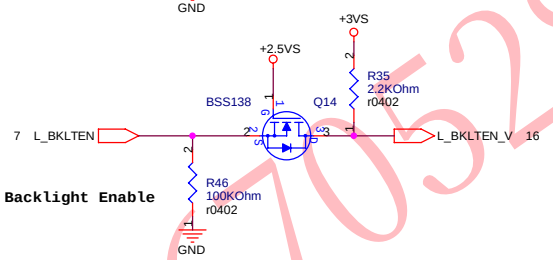
LOW = 1.05V (Default)
HIGH = 1.5V

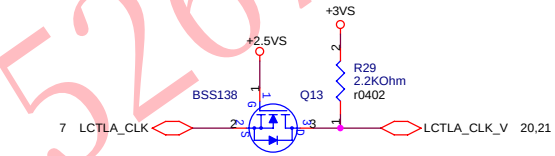
CFG19 : VTT SELECT

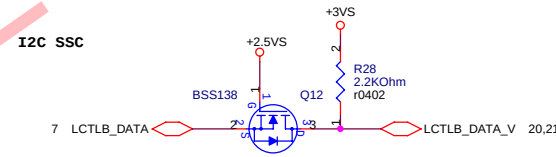


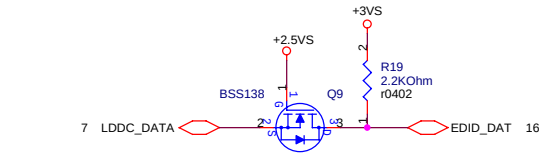
LOW = 1.05V (Default)
HIGH = 1.2V

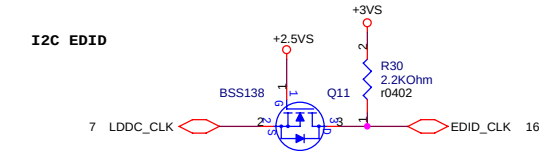












ASUSTeK COMPUTER INC	Title : GMCH Strapping	
	Engineer: Quan-Tai Lin	
Size: Custom	Project Name: A3E	Rev: 2.2
Date: Thursday, May 05, 2005	Sheet 11 of 51	

ICH6-M from 02-010002500 change to 02-010004402 on bom list

Unused SATA pin
- Connect RX, RBIAS, CLK to GND
- Leave TX, LED# as NC

PLACE WITHIN 500mils of ICH6 ball

H_CPUSLP# R193 : B STEP NO STUFF
H_DPRSTP# R231 : A STEP NO STUFF

INTERNAL PULL-DOWN
PULL-UP : NO REBOOT

INTERNAL PULL-UP
PULL-DOWN : RESERVED

TP_3 INTERNAL PULL-UP
PULL-DOWN : PCI
Express Port chain test

DELAY 18~25ms

Battery(RTC) P/N:07-016202032

* 56 within 1" from the ICH6-M pins
* 75 W pull-up to VCCP within 2"
from the series resistor

Title : ICH6_M (1)
ASUSTeK COMPUTER INC
Engineer: Quan-Tai Lin
Size: Custom
Project Name: A3E
Rev: 2.2
Date: Thursday, May 05, 2005
Sheet 12 of 51

PLT_RST#
ICH6,Alviso/KBC/FWH/HDD

U20A

ICH6_M

U20B

ICH6_M

PLACE within 500 mils of ICH.

PLACE within 500 mils of ICH.
5.5mil/8mil

INTERNAL PULL-DOWN SIGNALS :
AC_BITCLK , AC_RST# , AC_SDIN[2:0] , AC_SDOUT , AC_SYNC , DPSLPVR , LAN_CLK , PDD[7] , SDD[7] , PDDREQ , SDDREQ , SPKR , USB[7:0][P,N]

INTERNAL PULL-UP SIGNALS :
EE_DIN , EE_DOUT , GNT[B:A]# , GNT[5]# , GPIO[17:16] , LAD[3:0]# , LDRQ[1:0] , LAN_RXD[2:0] , PME# , PWRBTN#

(USB 4 for CAMERA)
(USB 5 for WLAN)

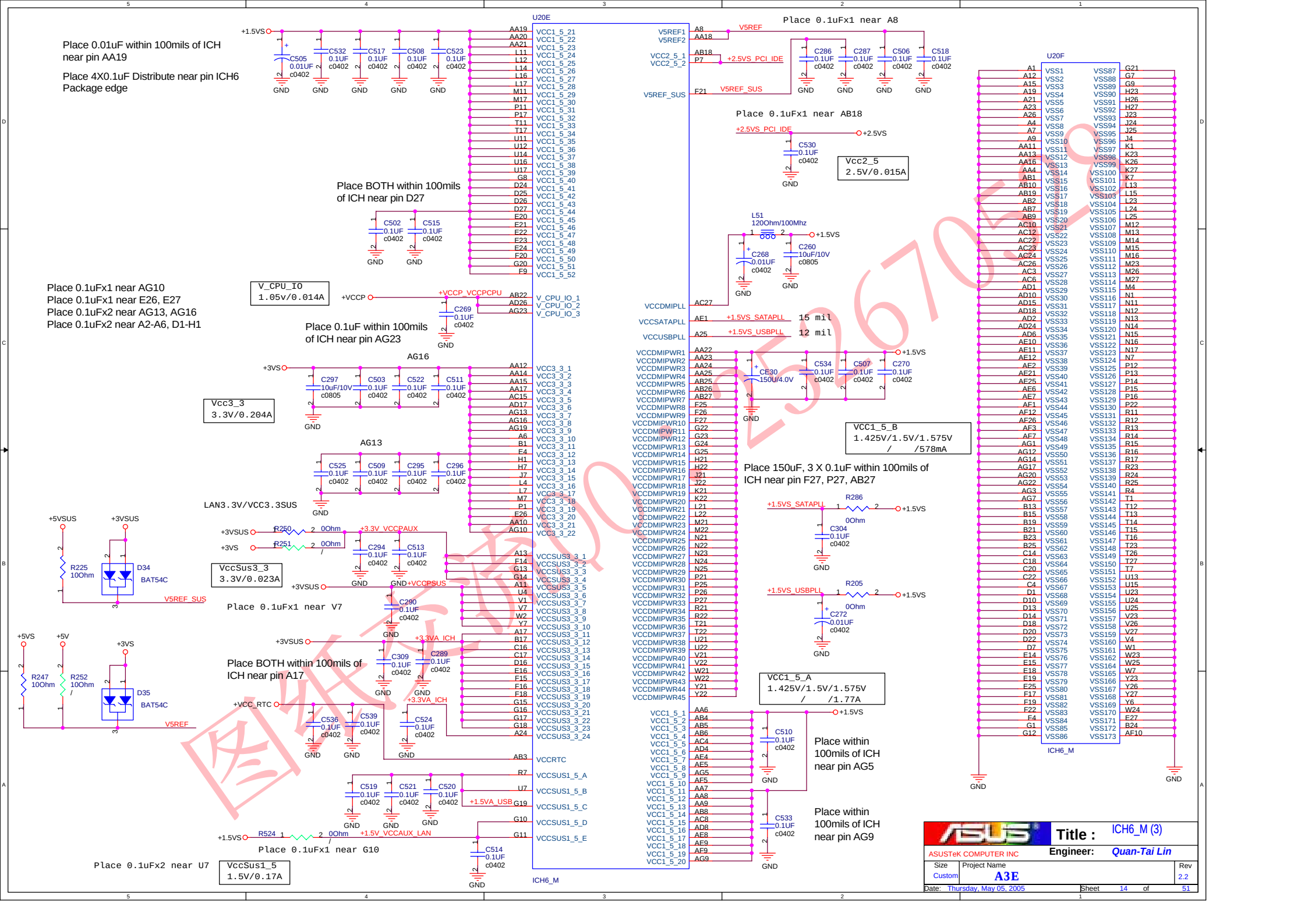
PCB_VID 0 1 2
MB V1.0 0 0 0

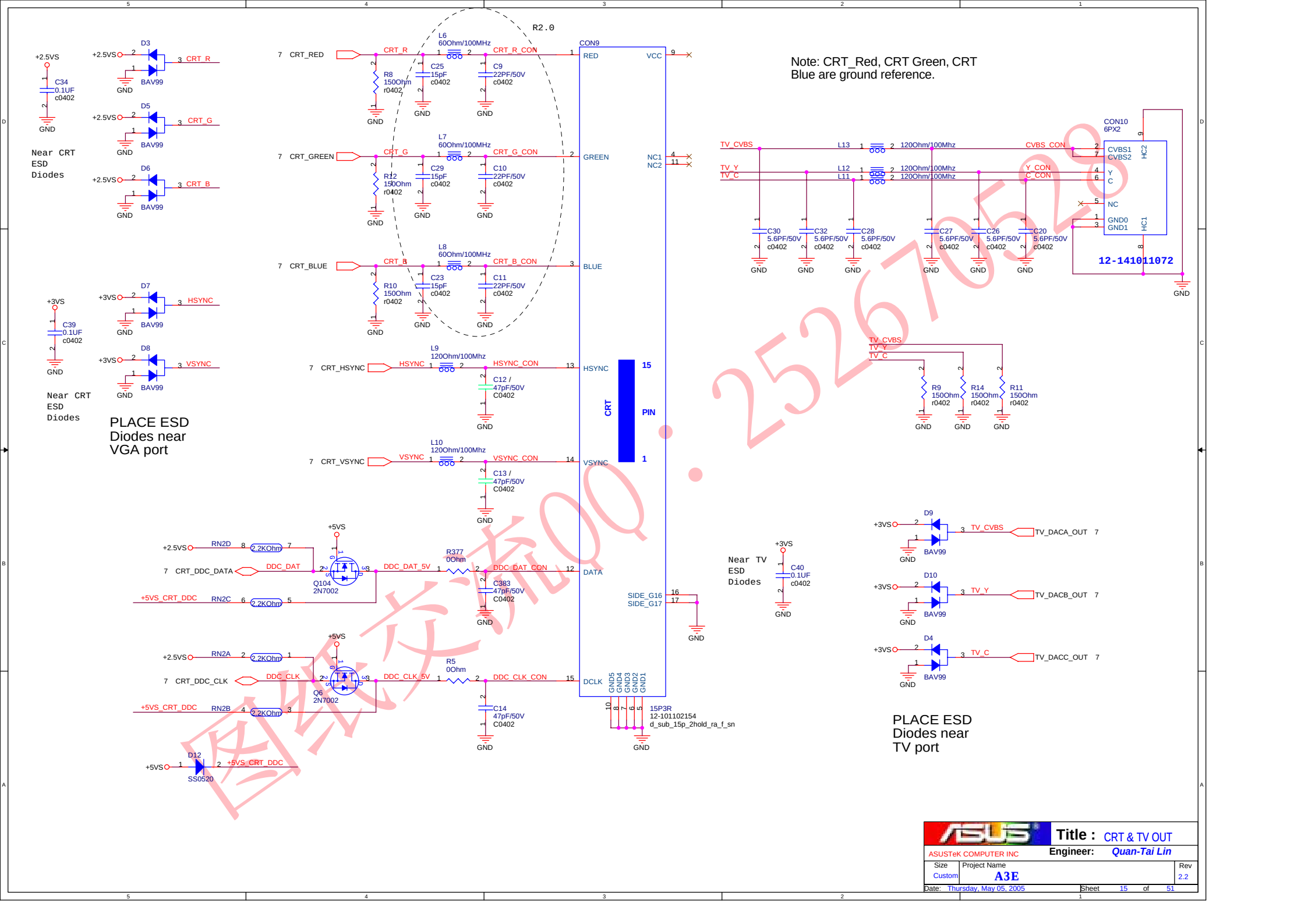
PCB_VID3 : PROJECT CODE

INTERNAL PULL-UP
PULL-DOWN : Boot BIOS destination select

INTERNAL PULL-UP
PULL-DOWN :TOP-BLOCK SWAP

Title :	ICH6_M (2)
ASUSTeK COMPUTER INC	Engineer: Quan-Tai Lin
Size: Custom	Project Name: A3E
Rev: 2.2	
Date: Thursday, May 05, 2005	Sheet 13 of 51


Place 0.01uF within 100mils of ICH near pin AA19
Place 4X0.1uF Distribute near pin ICH6 Package edge
Place BOTH within 100mils of ICH near pin D27
Place 0.1uFx1 near AG10
Place 0.1uFx1 near E26, E27
Place 0.1uFx2 near AG13, AG16
Place 0.1uFx2 near A2-A6, D1-H1
Place 0.1uF within 100mils of ICH near pin AG23
AG16
AG13
LAN3.3V/VCC3.3SUS
Place 0.1uFx1 near V7
Place BOTH within 100mils of ICH near pin A17
Place 0.1uFx1 near G10
Place 0.1uFx2 near U7
Place 0.1uFx1 near A8
Place 0.1uFx1 near AB18
Place 150uF, 3 X 0.1uF within 100mils of ICH near pin F27, P27, AB27
Place within 100mils of ICH near pin AG5
Place within 100mils of ICH near pin AG9
V_CPU_IO 1.05v/0.014A
Vcc3_3 3.3V/0.204A
VccSus3_3 3.3V/0.023A
VccSus1_5 1.5V/0.17A
Vcc2_5 2.5V/0.015A
VCC1_5_B 1.425V/1.5V/1.575V / /578mA
VCC1_5_A 1.425V/1.5V/1.575V / /1.77A
U20E
U20F
ICH6_M
Title : ICH6_M (3)
ASUSTeK COMPUTER INC
Engineer: Quan-Tai Lin
Size Custom
Project Name A3E
Rev 2.2
Date: Thursday, May 05, 2005
Sheet 14 of 51

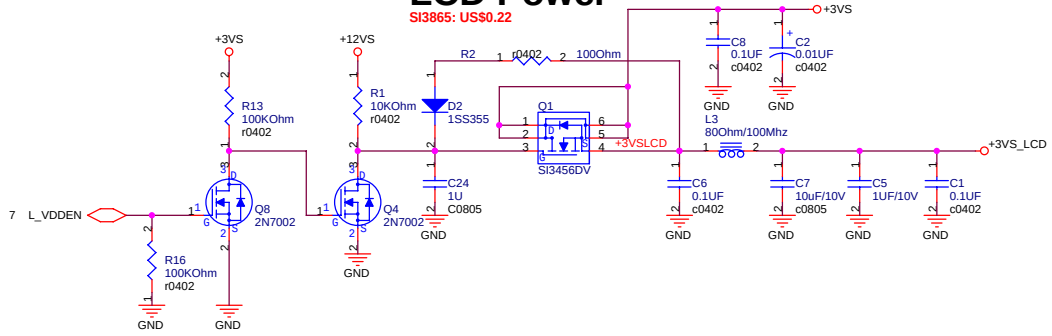

R2.0
Note: CRT_Red, CRT Green, CRT Blue are ground reference.
Near CRT ESD Diodes
Near CRT ESD Diodes
PLACE ESD Diodes near VGA port
Near TV ESD Diodes
PLACE ESD Diodes near TV port
CON9
CRT
PIN
15P3R
12-101102154
d_sub_15p_2hold_ra_f_sn
CON10
6PX2
12-141011072
Title : CRT & TV OUT
ASUSTeK COMPUTER INC
Engineer: Quan-Tai Lin
Size: Custom
Project Name: A3E
Rev: 2.2
Date: Thursday, May 05, 2005
Sheet 15 of 51

LCD Backlight Control

3V-3.6V
Full Active: 410 mA(Max. 500 mA)
3-3.6V
S0-S1M:410 mA(500 mA Max.)

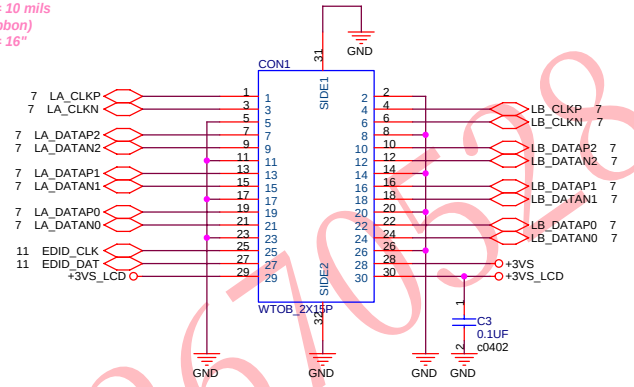
LCD Power

SI3865: US$0.22



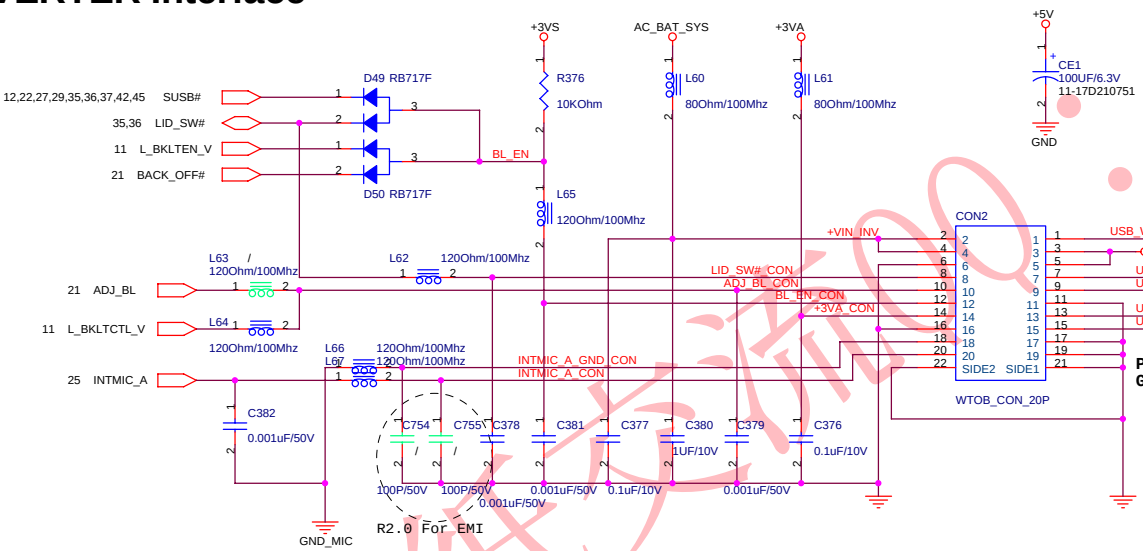
Cable Requirement:
Impedence: 100 ohm +/- 10%
Length Mismatch <= 10 mils
Twisted Pair(Not Ribbon)
Maximum Length <= 16"

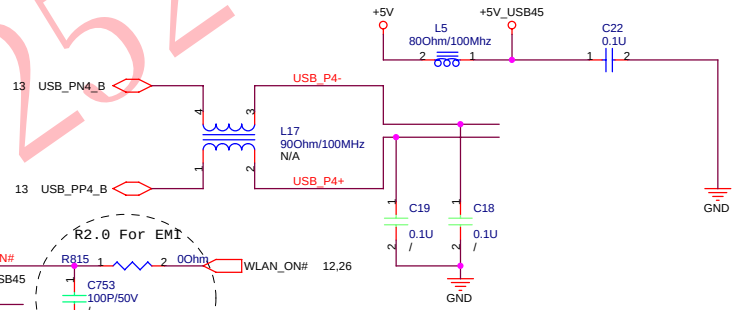
LCD LVDS Interface



CON1 P/N on BOM List : 12-17001030A

INVERTER Interface

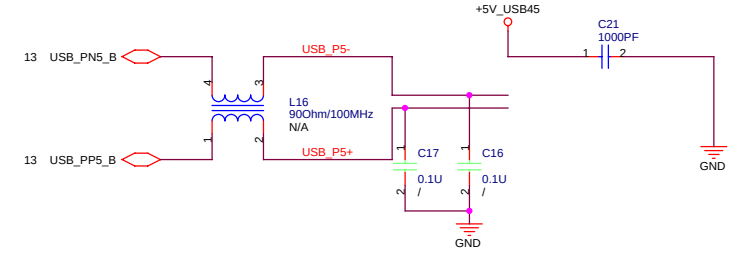




R2.0 For EMI
R815 0Ohm
WLAN_ON# 12,26
C753 100P/50V

USB PORT 4 for CAMERA

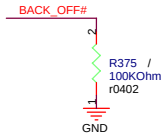
Pin 19 : Add a USB 2.0 Shielding GND cable to USB module.



USB PORT 5 for WLAN

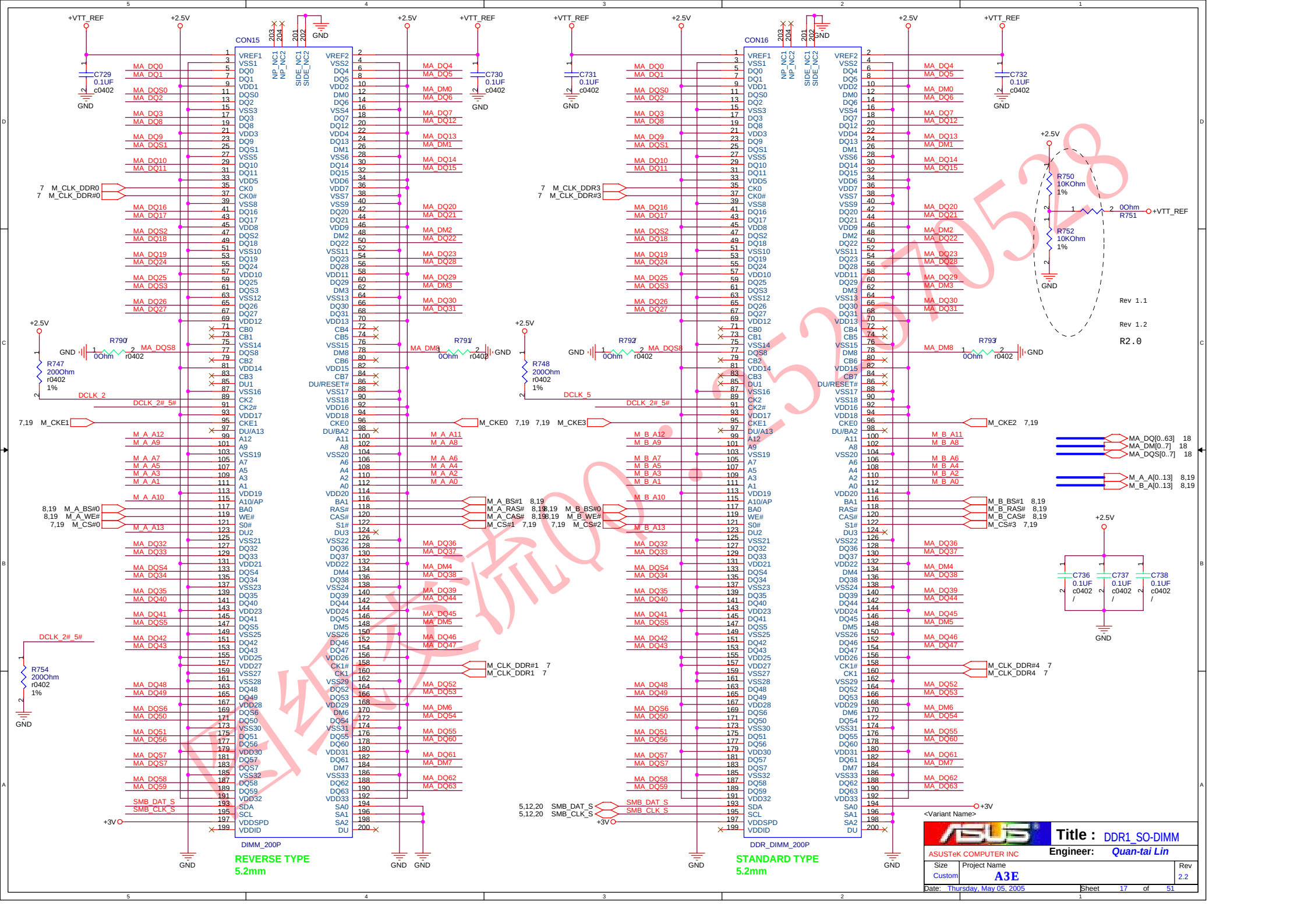
BIOS
ADJ_BL: KBC output D/A signal (adjust voltage level) to adjust Back light.

BIOS
BACK_OFF#:When user push "Fn+F7" button, BIOS active this pin to turn off back light.



700Vrms@5 mArms
(Min. 3 mArms)6 mArms(Max. 6.5 mArms)

ASUSTeK COMPUTER INC	Title : LVDS & INVERTER	
	Engineer: Quan-Tai Lin	
Size: Custom	Project Name: A3E	Rev: 2.2
Date: Thursday, May 05, 2005	Sheet 16 of 51	


CON15
CON16
DIMM_200P
DDR_DIMM_200P
REVERSE TYPE
5.2mm
STANDARD TYPE
5.2mm
+VTT_REF
+2.5V
+3V
GND
M_CLK_DDR0
M_CLK_DDR#0
M_CLK_DDR3
M_CLK_DDR#3
M_CKE0
M_CKE1
M_CKE2
M_CKE3
DCLK_2
DCLK_2#
DCLK_5
DCLK_5#
R747 200Ohm r0402 1%
R748 200Ohm r0402 1%
R754 200Ohm r0402 1%
R750 10KOhm 1%
R751 0Ohm
R752 10KOhm 1%
C729 0.1UF c0402
C730 0.1UF c0402
C731 0.1UF c0402
C732 0.1UF c0402
C736 0.1UF c0402
C737 0.1UF c0402
C738 0.1UF c0402
Rev 1.1
Rev 1.2
R2.0
Title : DDR1_SO-DIMM
ASUSTeK COMPUTER INC
Engineer: Quan-tai Lin
Size: Custom
Project Name: A3E
Rev: 2.2
Date: Thursday, May 05, 2005
Sheet 17 of 51

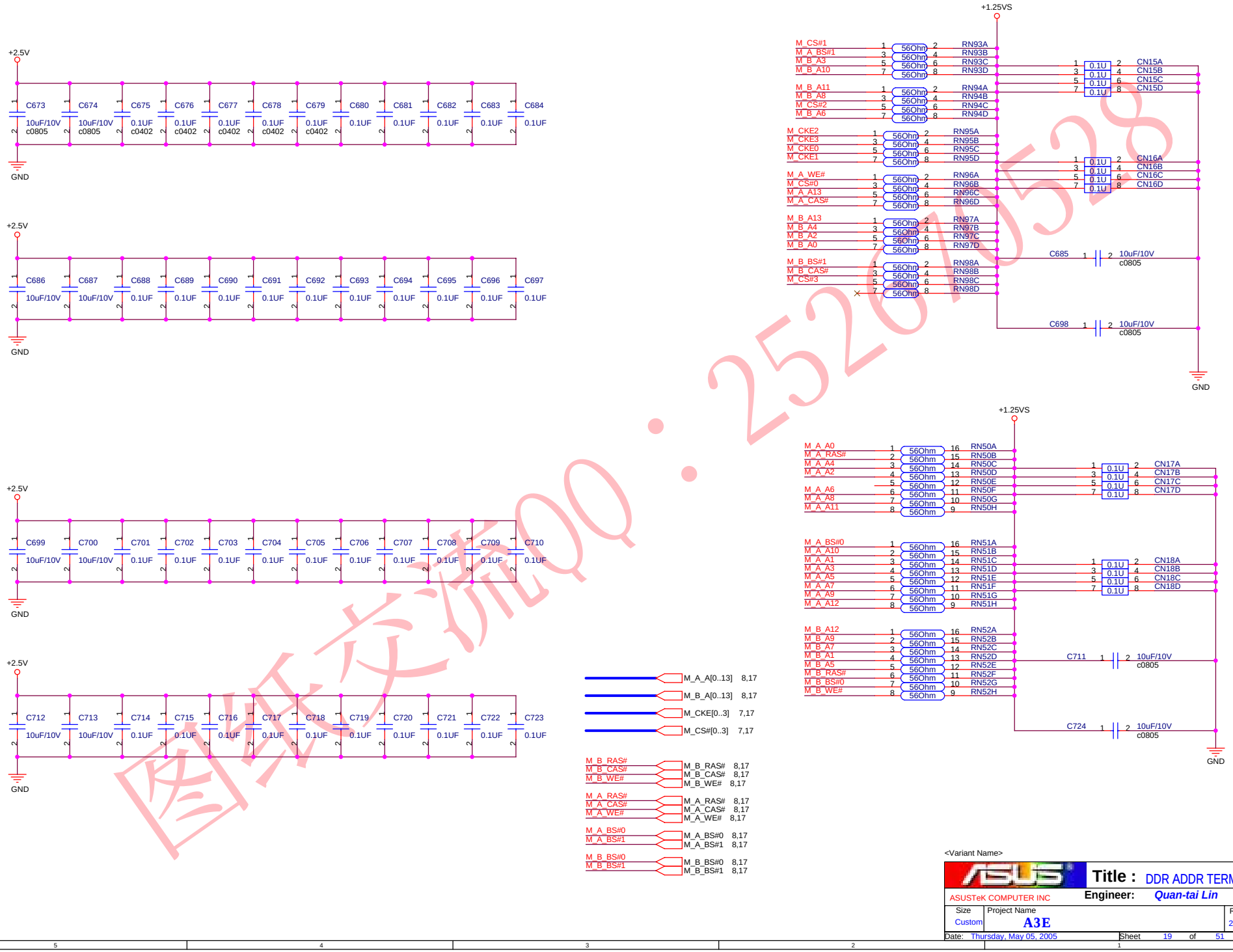
<Variant Name>

Title DDR DATA TERMINATION

ASUSTeK COMPUTER INC Engineer: Quan-tai Lin

Size	Project Name	Rev
Custom	A3E	2.2

Date: Thursday, May 05, 2005 Sheet 18 of 51



<Variant Name>

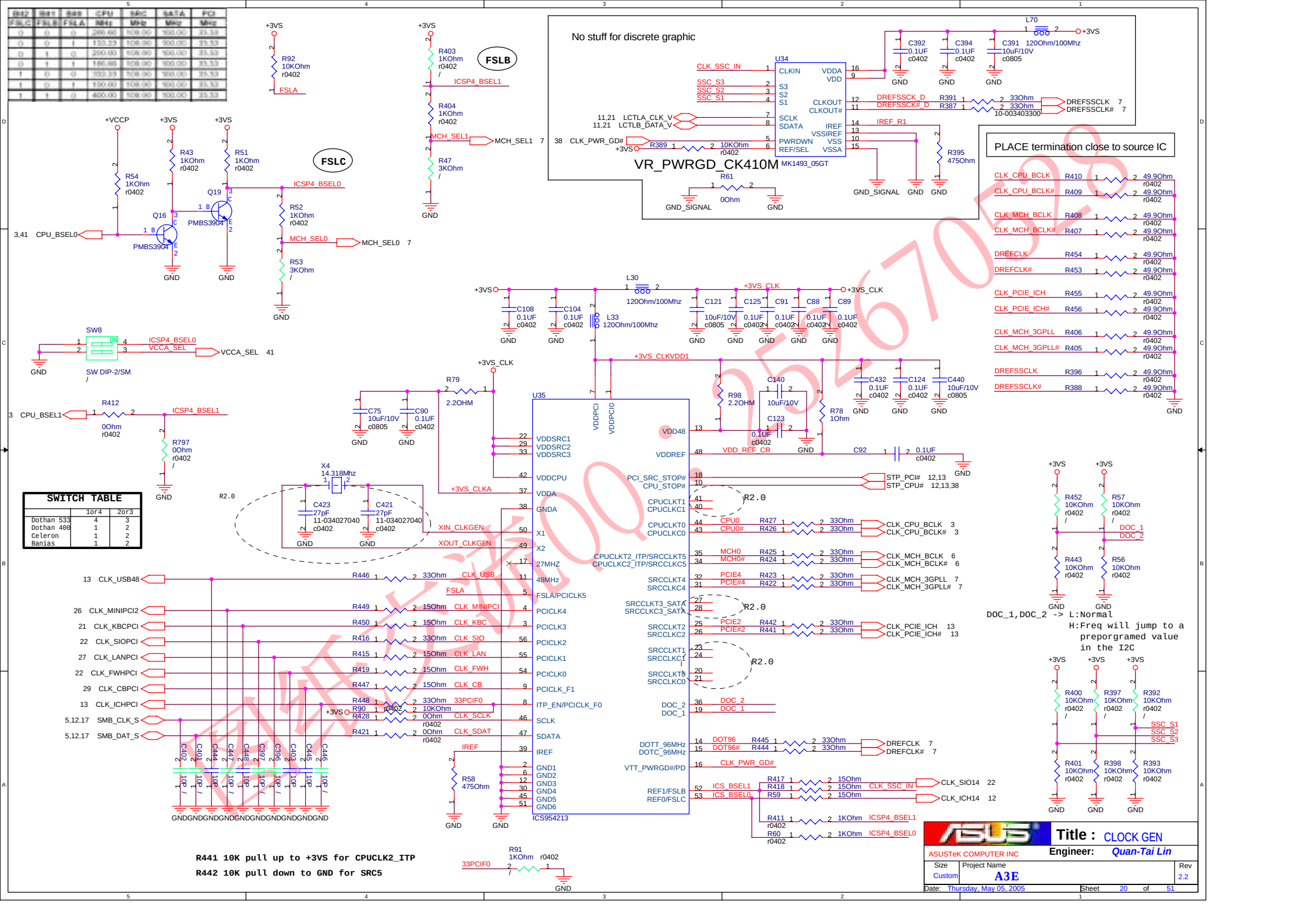
Title : DDR ADDR TERM

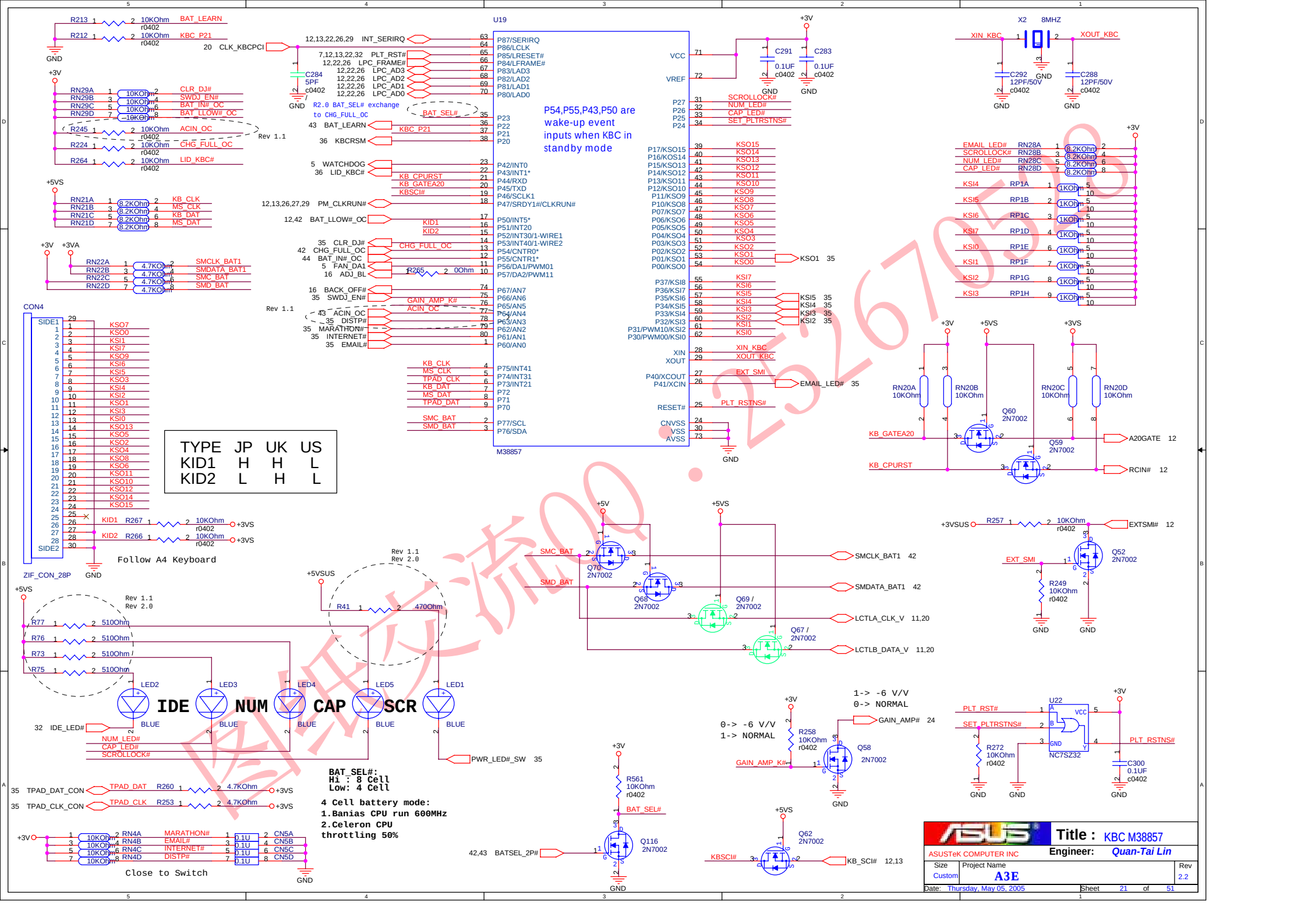
ASUSTeK COMPUTER INC

Engineer: Quan-tai Lin

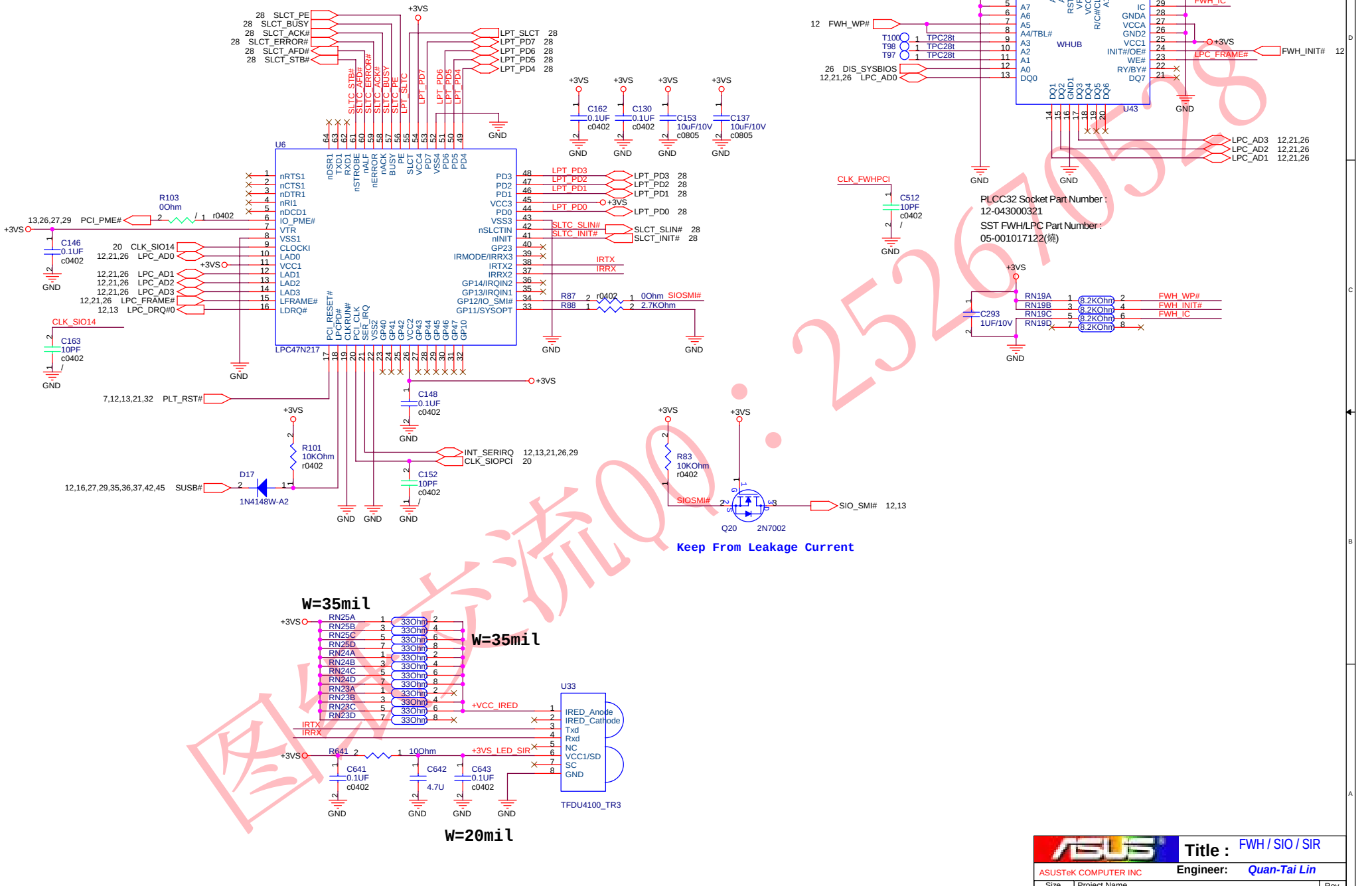
Size	Project Name	Rev
Custom	A3E	2.2

Date: Thursday, May 05, 2005 Sheet 19 of 51


No stuff for discrete graphic
VR_PWRGD_CK410M
MK1493_05GT
PLACE termination close to source IC
SWITCH TABLE
1or4 2or3
Dothan 533 4 3
Dothan 400 1 2
Celeron 1 2
Banias 1 2
R441 10K pull up to +3VS for CPUCLK2_ITP
R442 10K pull down to GND for SRC5
DOC_1,DOC_2 -> L:Normal
H:Freq will jump to a preporgramed value in the I2C
ICS954213
Title : CLOCK GEN
ASUSTeK COMPUTER INC
Engineer: Quan-Tai Lin
Project Name A3E
Rev 2.2
Date: Thursday, May 05, 2005
Sheet 20 of 51


U19
M38857
P54,P55,P43,P50 are wake-up event inputs when KBC in standby mode
R2.0 BAT_SEL# exchange to CHG_FULL_OC
Rev 1.1
CON4
ZIF_CON_28P
Follow A4 Keyboard
TYPE JP UK US
KID1 H H L
KID2 L H L
IDE NUM CAP SCR
LED1
LED2
LED3
LED4
LED5
BAT_SEL#:
Hi : 8 Cell
Low: 4 Cell
4 Cell battery mode:
1.Banias CPU run 600MHz
2.Celeron CPU
throttling 50%
Close to Switch
X2 8MHZ
Q58 2N7002
Q59 2N7002
Q60 2N7002
Q62 2N7002
Q68 2N7002
Q69 / 2N7002
Q70 2N7002
Q67 / 2N7002
Q52 2N7002
Q116 2N7002
NC7SZ32
Title : KBC M38857
ASUSTeK COMPUTER INC
Engineer: Quan-Tai Lin
Project Name A3E
Size Custom
Rev 2.2
Date: Thursday, May 05, 2005
Sheet 21 of 51

Super I/O



PLCC32 Socket Part Number :
12-043000321
SST FWH/LPC Part Number :
05-001017122(燒)

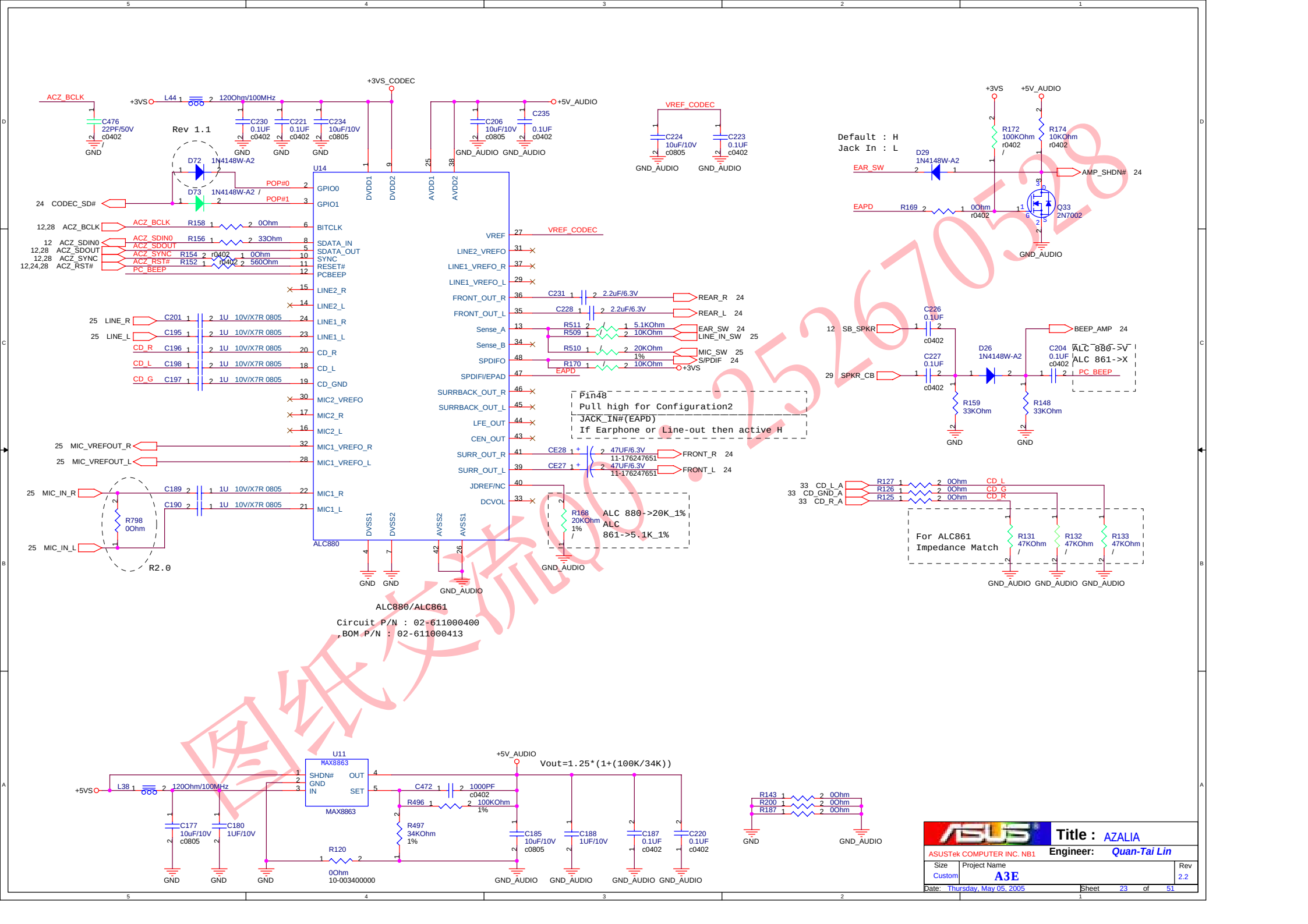
Keep From Leakage Current

W=35mil

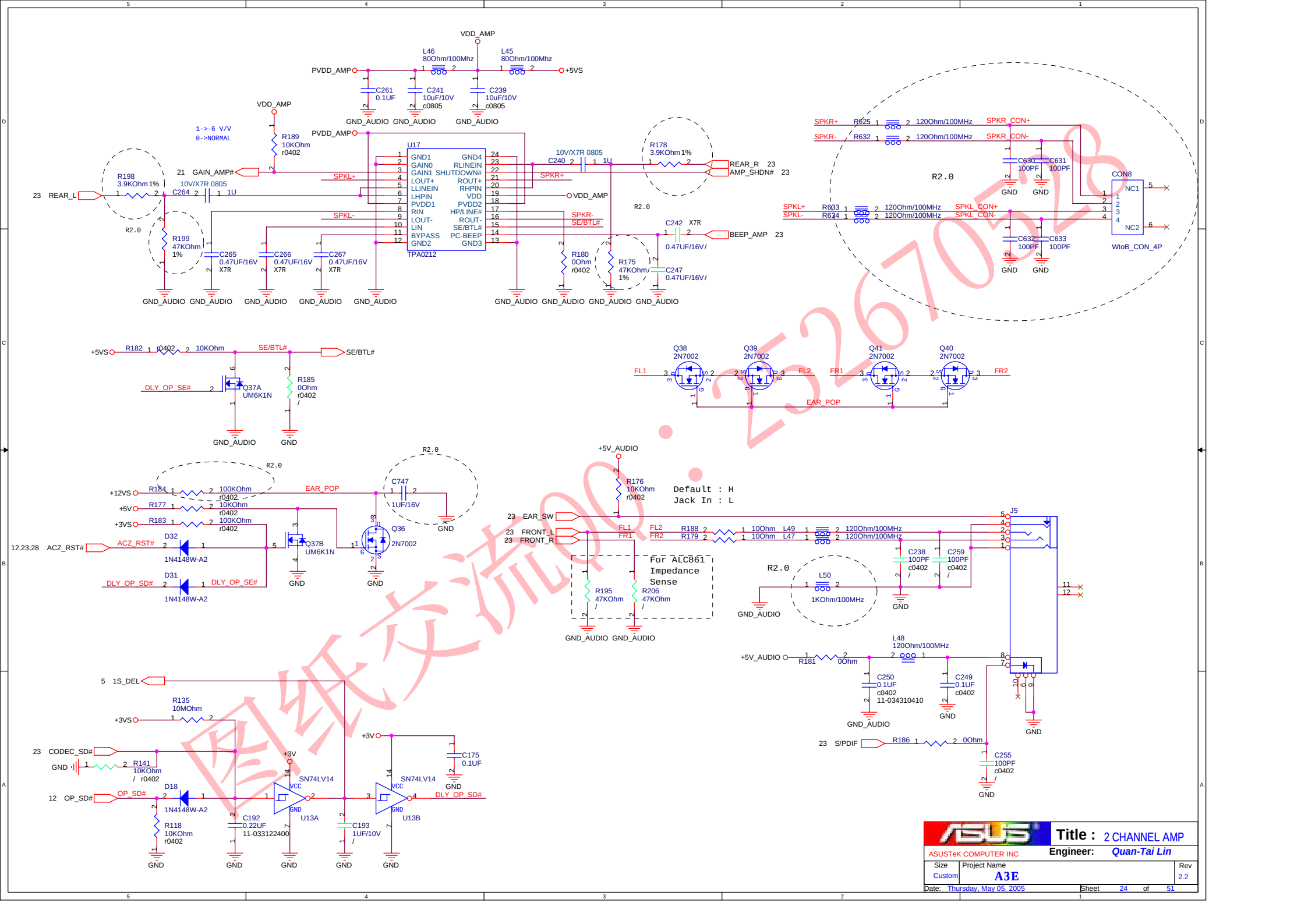
W=35mil

W=20mil

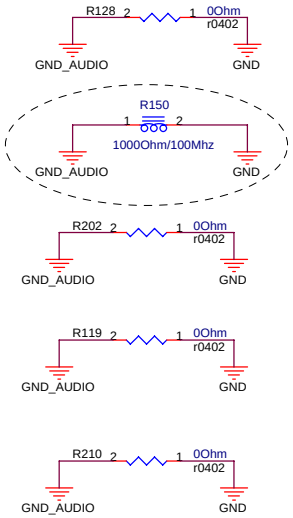
ASUSTeK COMPUTER INC	Title : FWH / SIO / SIR	
	Engineer: Quan-Tai Lin	
Size: Custom	Project Name: A3E	Rev: 2.2
Date: Thursday, May 05, 2005	Sheet 22 of 51	



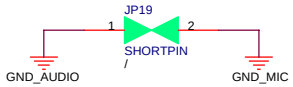
Title : AZALIA		
ASUSTek COMPUTER INC. NB1	Engineer: Quan-Tai Lin	
Size: Custom	Project Name: A3E	Rev: 2.2
Date: Thursday, May 05, 2005	Sheet 23 of 51	

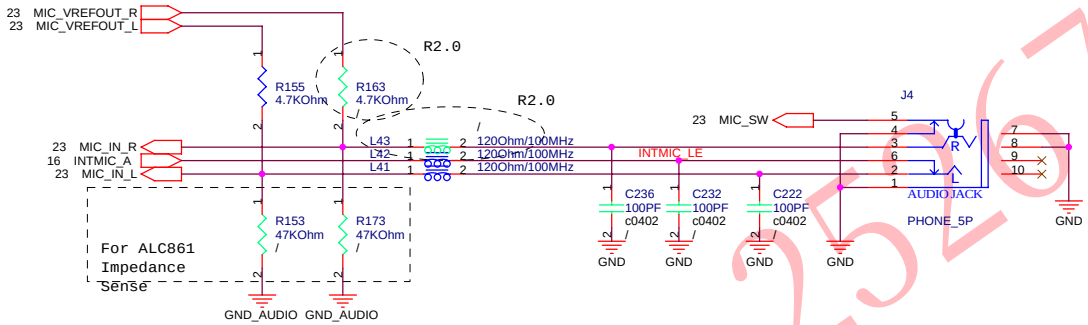


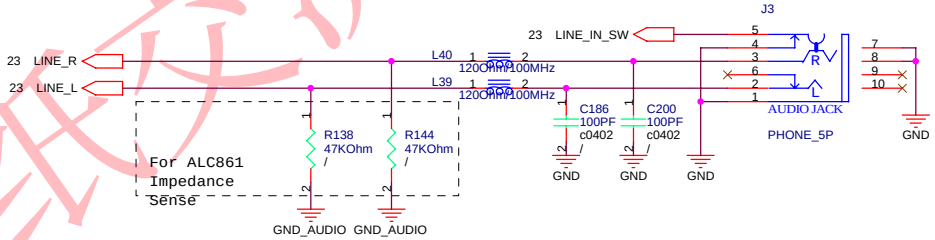
ASUSTeK COMPUTER INC	Title : 2 CHANNEL AMP	
	Engineer: Quan-Tai Lin	
Size: Custom	Project Name: A3E	Rev: 2.2
Date: Thursday, May 05, 2005	Sheet 24 of 51	



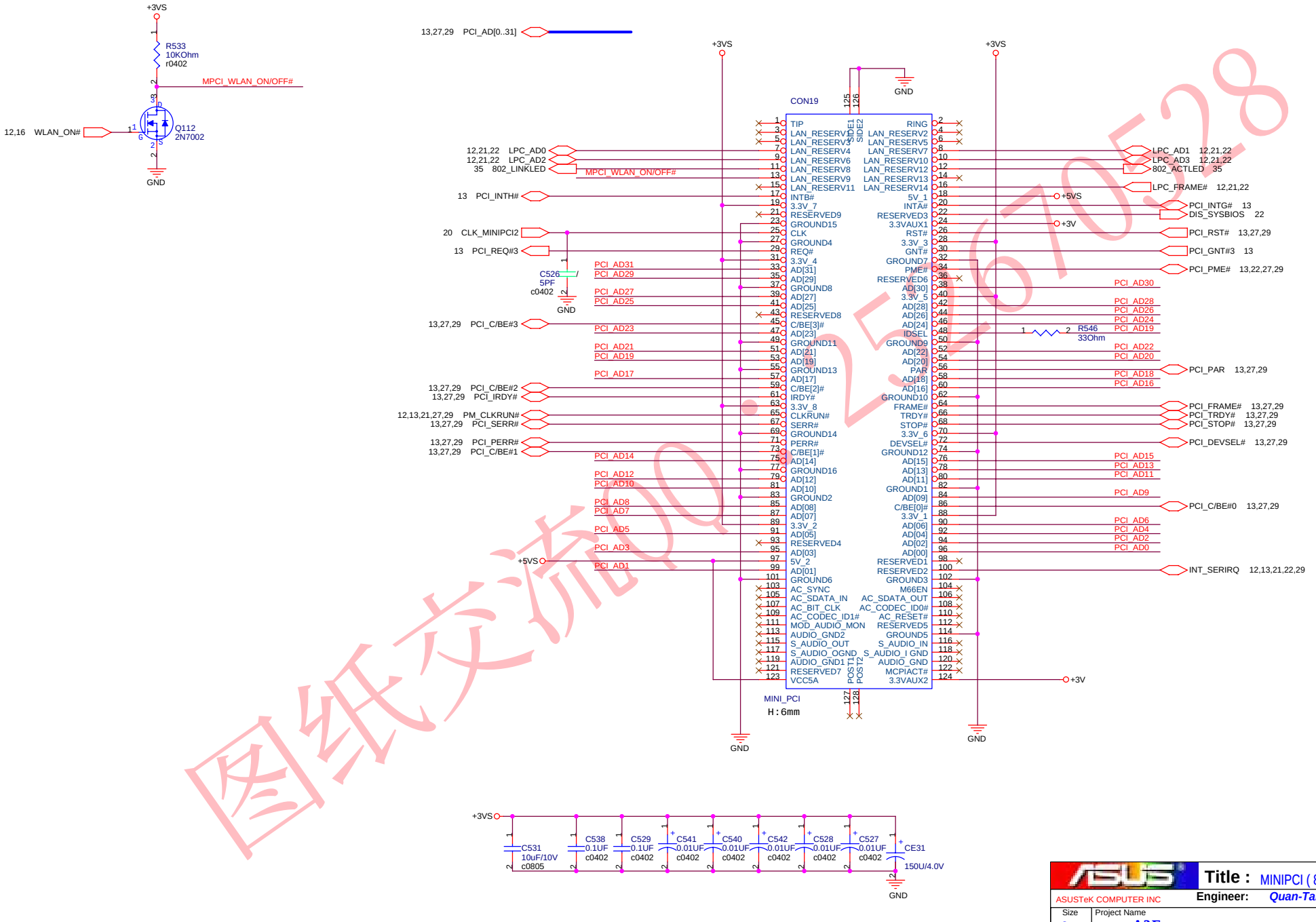
INTMIC_A:GND_AUDIO
: W/P/X = 12/5/15mils

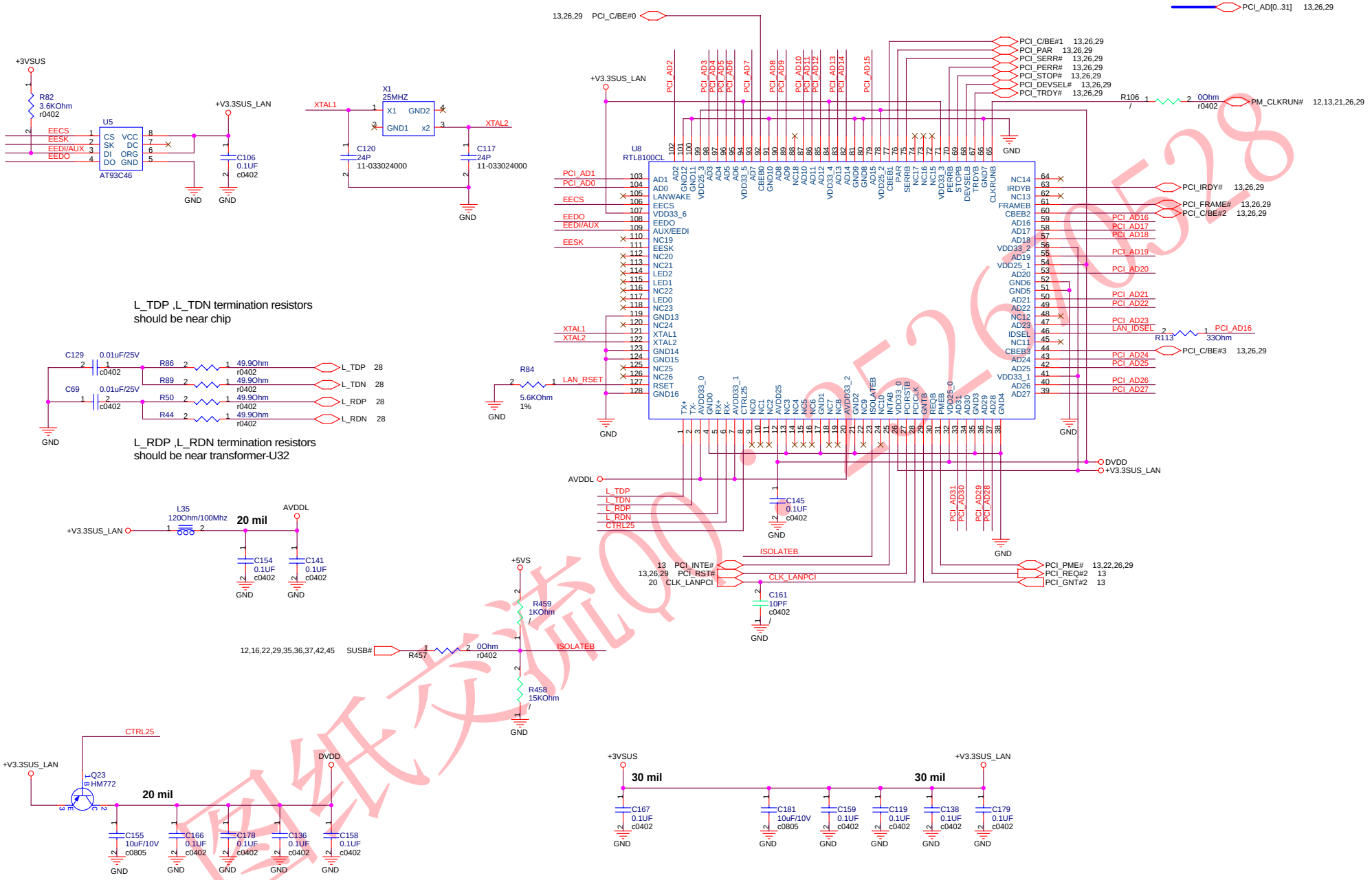






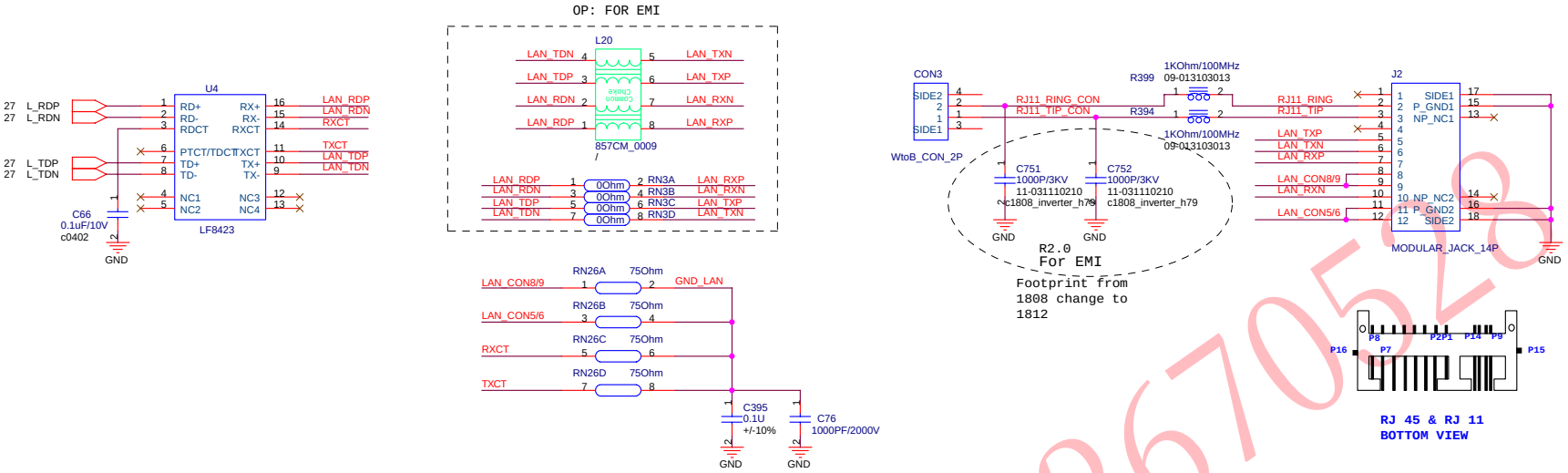
ASUSTeK COMPUTER INC	Title : MIC / Line-IN Jack	
	Engineer: Quan-Tai Lin	
Size: Custom	Project Name: A3E	Rev: 2.2
Date: Thursday, May 05, 2005	Sheet 25 of 51	



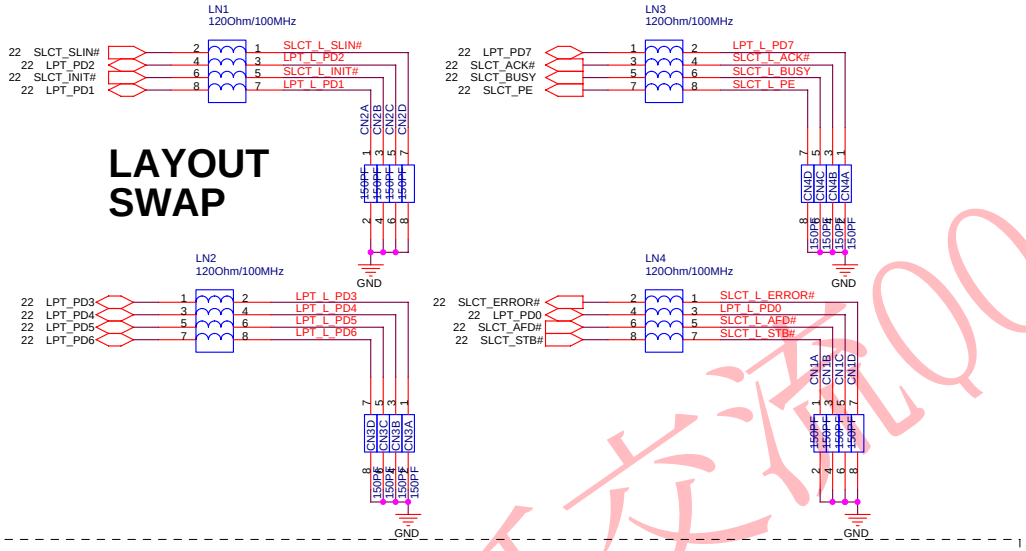


ASUSTeK COMPUTER INC	Title : 10/100 LAN RTL8100CL	
	Engineer: Quan-Tai Lin	
Size: Custom	Project Name: A3E	Rev: 2.2
Date: Thursday, May 05, 2005	Sheet 27 of 51	

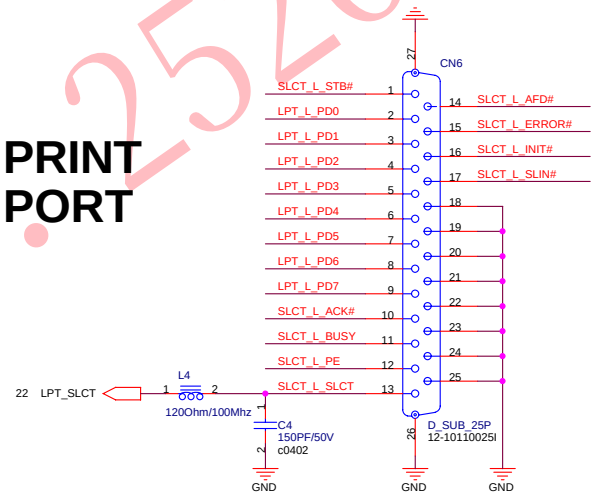
LAN PORT



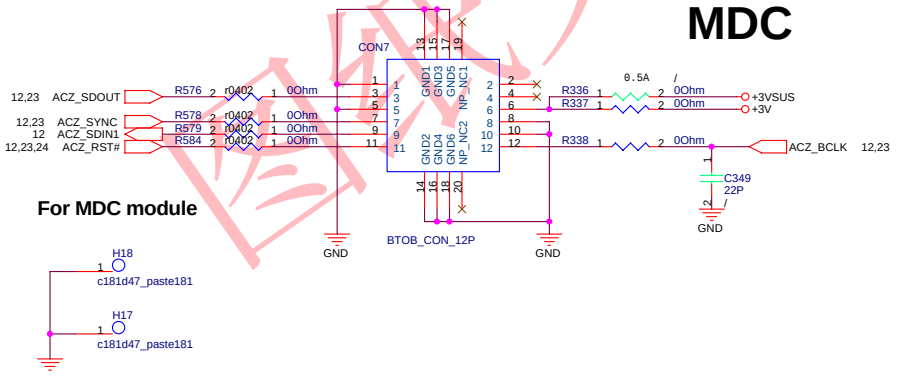
LAYOUT SWAP

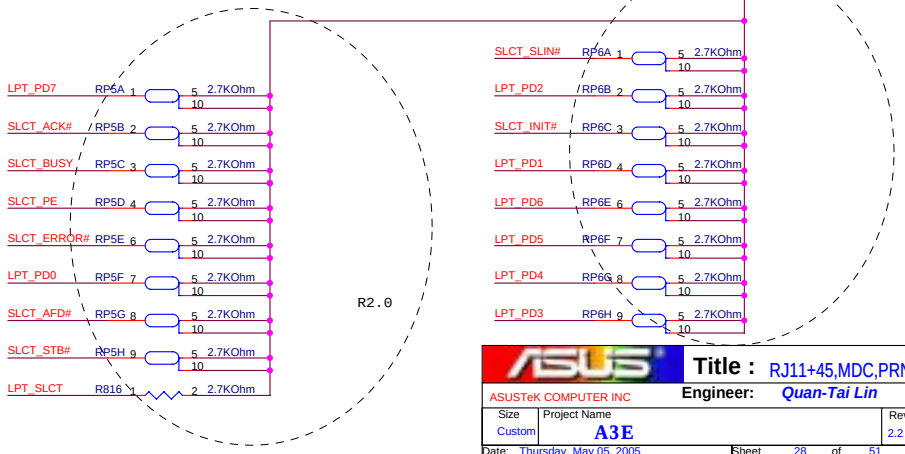


PRINT PORT

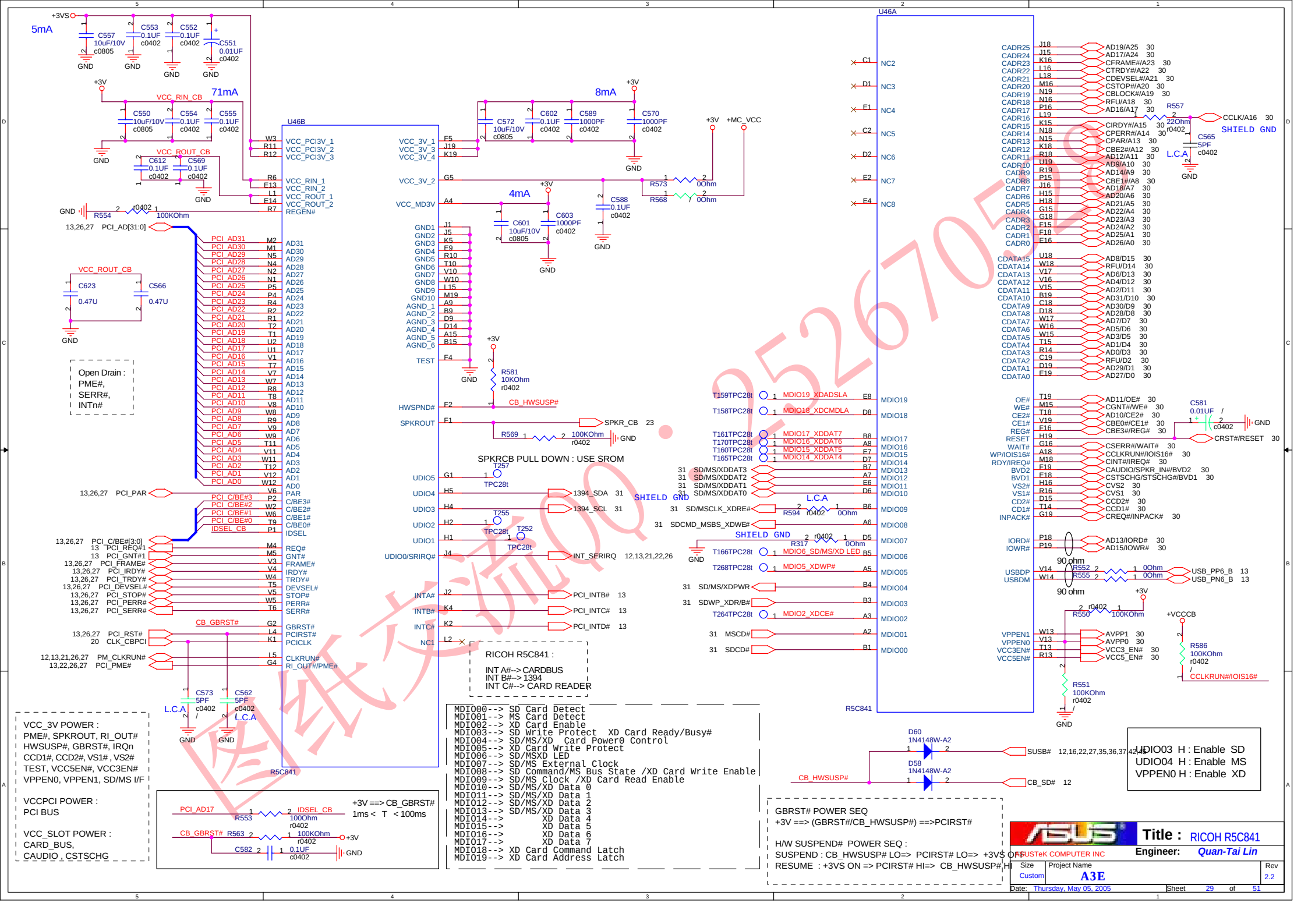


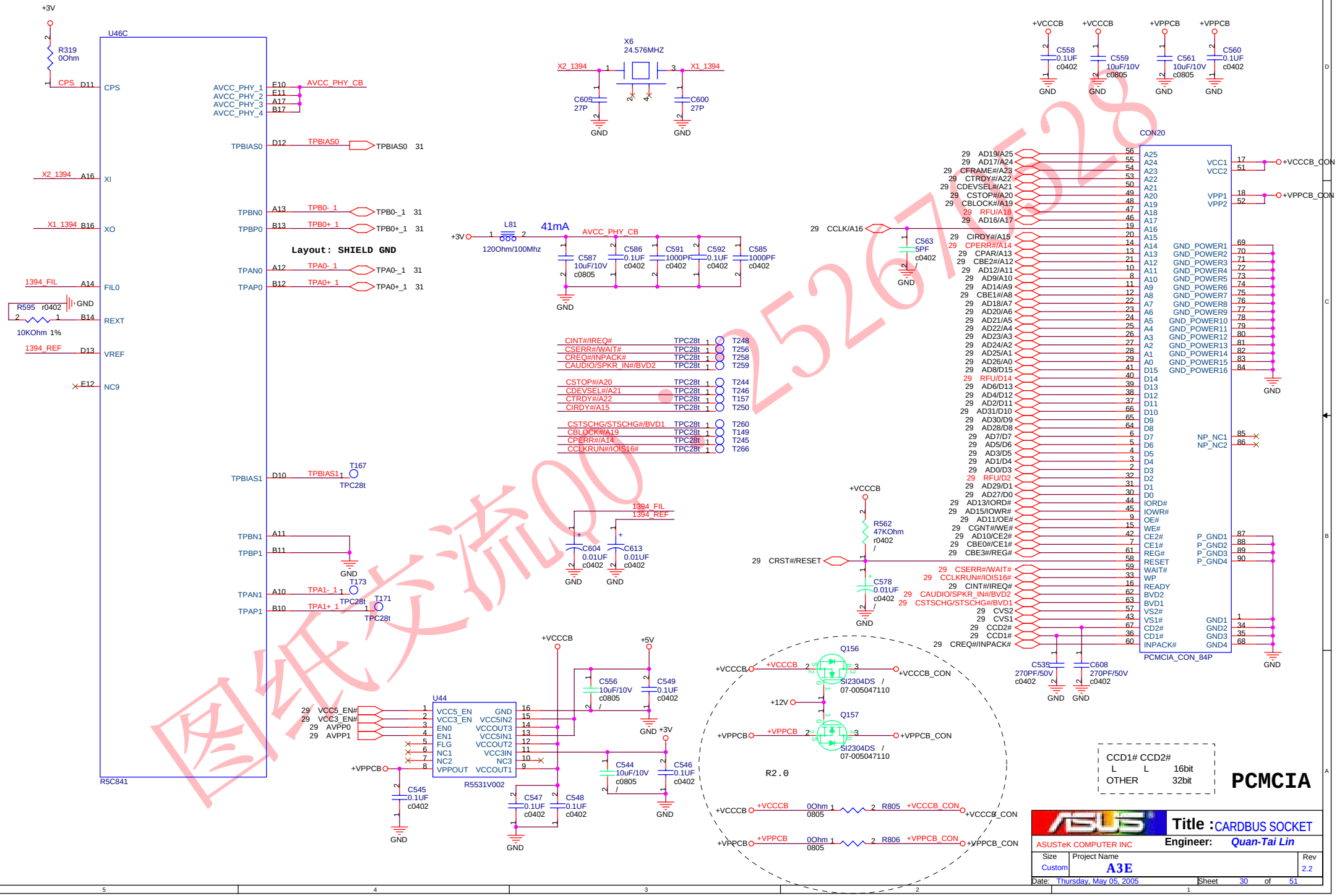
MDC

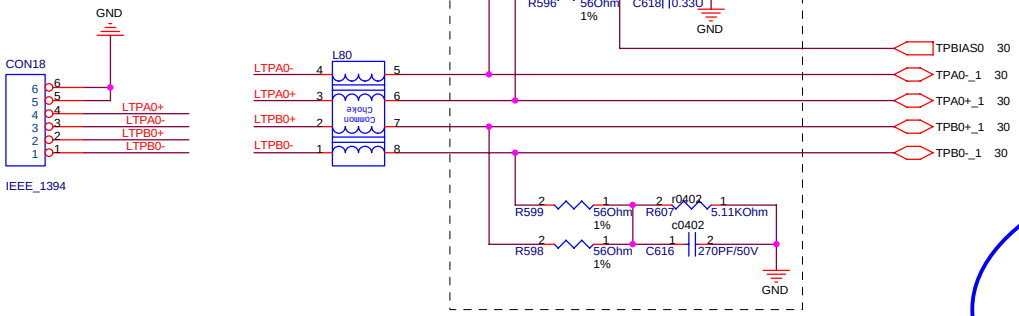




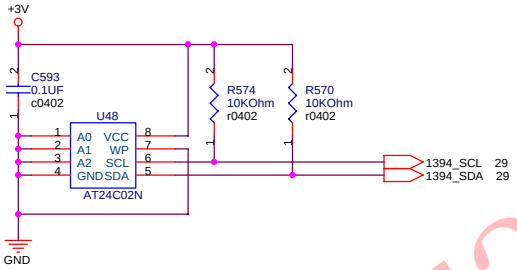
ASUSTeK COMPUTER INC	Title : RJ11+45,MDC,PRN	
	Engineer: Quan-Tai Lin	
Size: Custom	Project Name: A3E	Rev: 2.2
Date: Thursday, May 05, 2005	Sheet 28 of 51	

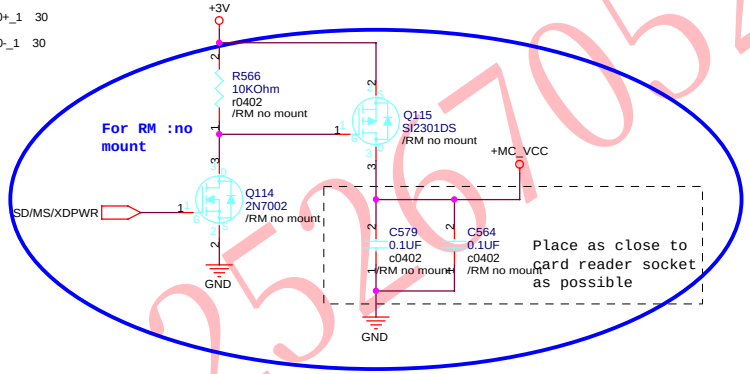

5mA
71mA
8mA
4mA
U46B
U46A
R5C841
SHIELD GND
L.C.A
SPKRCB PULL DOWN : USE SROM
Open Drain : PME#, SERR#, INTn#
RICOH R5C841 :
INT A#--> CARDBUS
INT B#--> 1394
INT C#--> CARD READER
VCC_3V POWER : PME#, SPKROUT, RI_OUT# HWSUSP#, GBRST#, IRQn CCD1#, CCD2#, VS1# , VS2# TEST, VCC5EN#, VCC3EN# VPPEN0, VPPEN1, SD/MS I/F
VCCPCI POWER : PCI BUS
VCC_SLOT POWER : CARD_BUS, CAUDIO , CSTSCHG
+3V ==> CB_GBRST# 1ms < T < 100ms
MDIO00--> SD Card Detect
MDIO01--> MS Card Detect
MDIO02--> XD Card Enable
MDIO03--> SD Write Protect XD Card Ready/Busy#
MDIO04--> SD/MS/XD Card Power0 Control
MDIO05--> XD Card Write Protect
MDIO06--> SD/MSXD LED
MDIO07--> SD/MS External Clock
MDIO08--> SD Command/MS Bus State /XD Card Write Enable
MDIO09--> SD/MS Clock /XD Card Read Enable
MDIO10--> SD/MS/XD Data 0
MDIO11--> SD/MS/XD Data 1
MDIO12--> SD/MS/XD Data 2
MDIO13--> SD/MS/XD Data 3
MDIO14--> XD Data 4
MDIO15--> XD Data 5
MDIO16--> XD Data 6
MDIO17--> XD Data 7
MDIO18--> XD Card Command Latch
MDIO19--> XD Card Address Latch
GBRST# POWER SEQ
+3V ==> (GBRST#/CB_HWSUSP#) ==>PCIRST#
H/W SUSPEND# POWER SEQ :
SUSPEND : CB_HWSUSP# LO=> PCIRST# LO=> +3VS OFF
RESUME : +3VS ON => PCIRST# HI=> CB_HWSUSP# HI
UDIO03 H : Enable SD
UDIO04 H : Enable MS
VPPEN0 H : Enable XD
Title : RICOH R5C841
Engineer: Quan-Tai Lin
ASUSTeK COMPUTER INC
Size Custom
Project Name A3E
Rev 2.2
Date: Thursday, May 05, 2005
Sheet 29 of 51

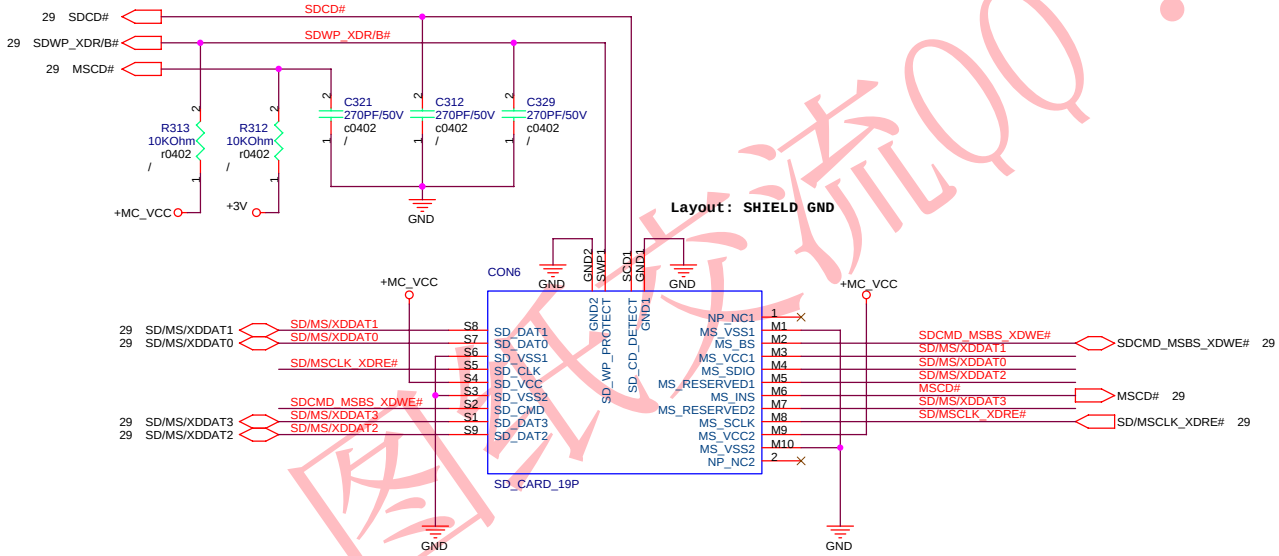




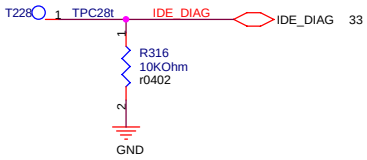
1.CLOSE TO R5C841
2.The area is as compact as possible,length < 10 mm
3.TPA Pair and TPB pair mismatch < 2.5mm
4.No via recommend , maxmium is one.
5.Total length < 50 mm
6.Differential impedance is 110+/- 6 ohm
7.TPA Pair trace or TPB pair trace mismatch < 1.25mm



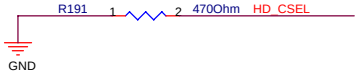


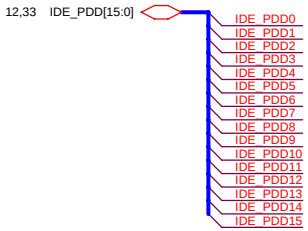


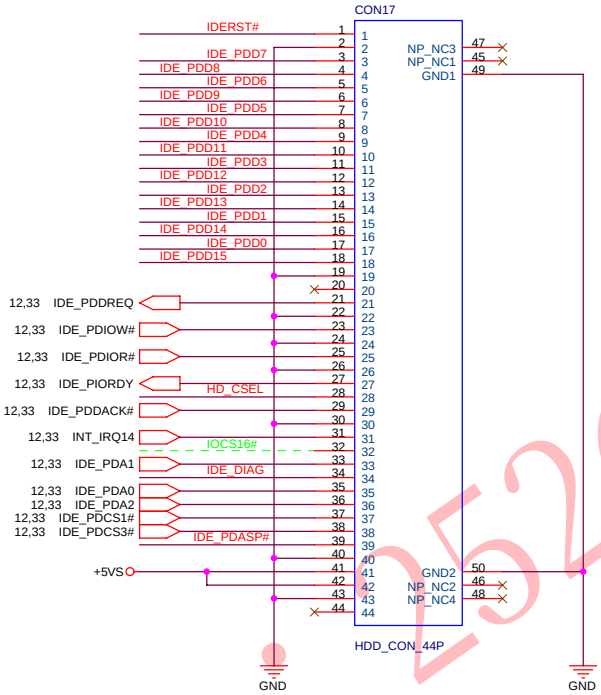
ASUSTeK COMPUTER INC	Title : 1394 & 3 IN 1 CON	
	Engineer: Quan-Tai Lin	
Size: Custom	Project Name: A3E	Rev: 2.2
Date: Thursday, May 05, 2005	Sheet 31 of 51	

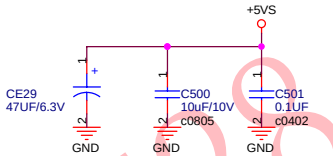


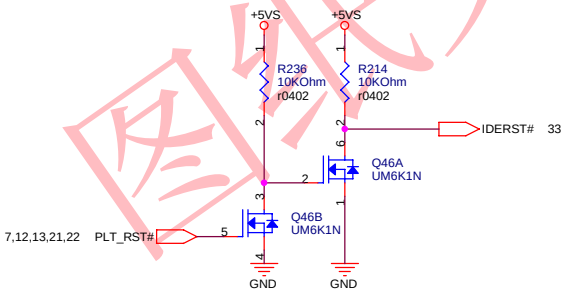
HD_CSEL : Pull-Down, HDD as Master

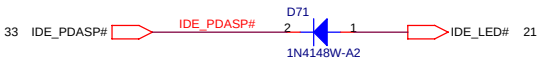












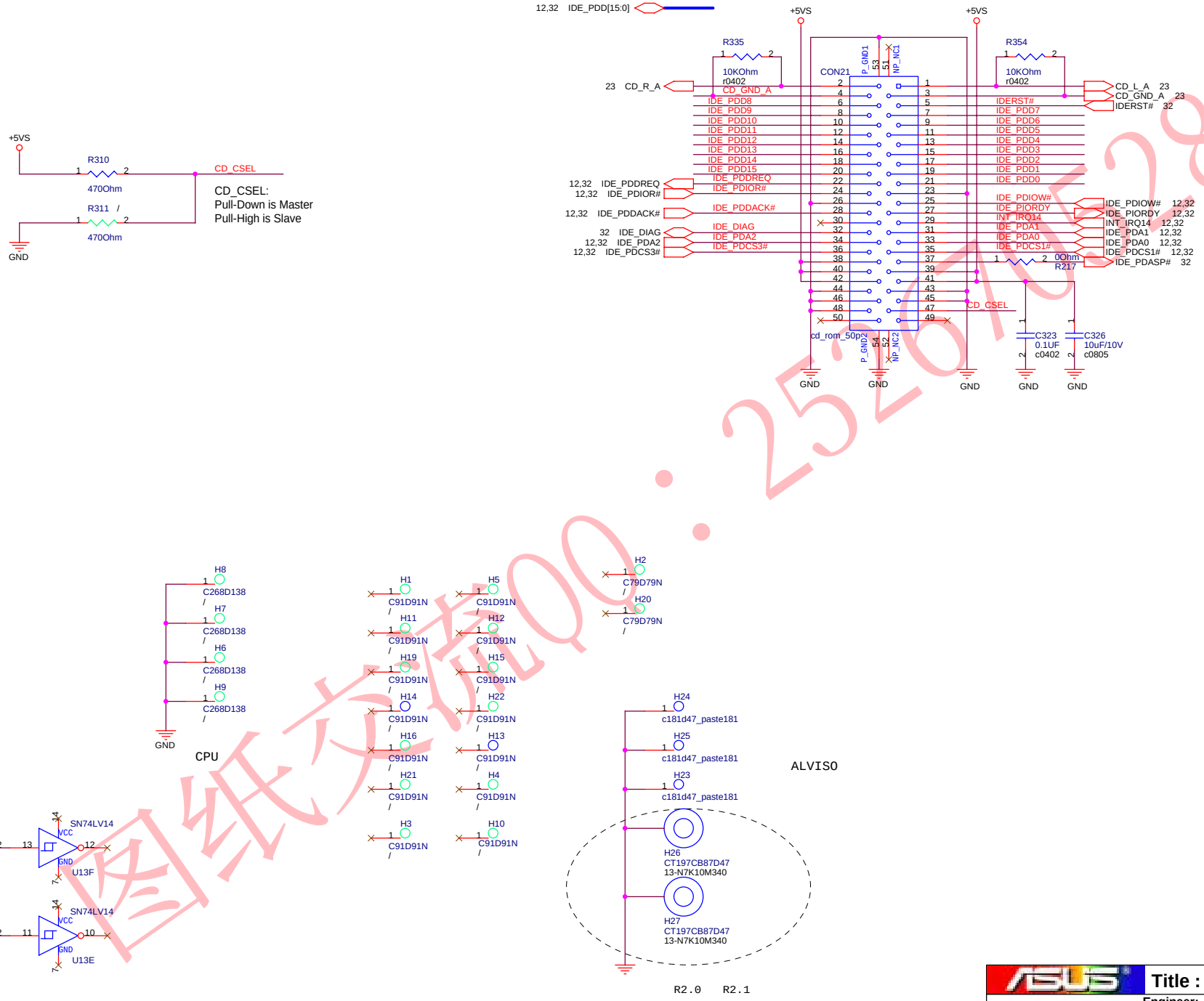
Title : HDD CONNECTOR

ASUSTeK COMPUTER INC

Engineer: Quan-Tai Lin

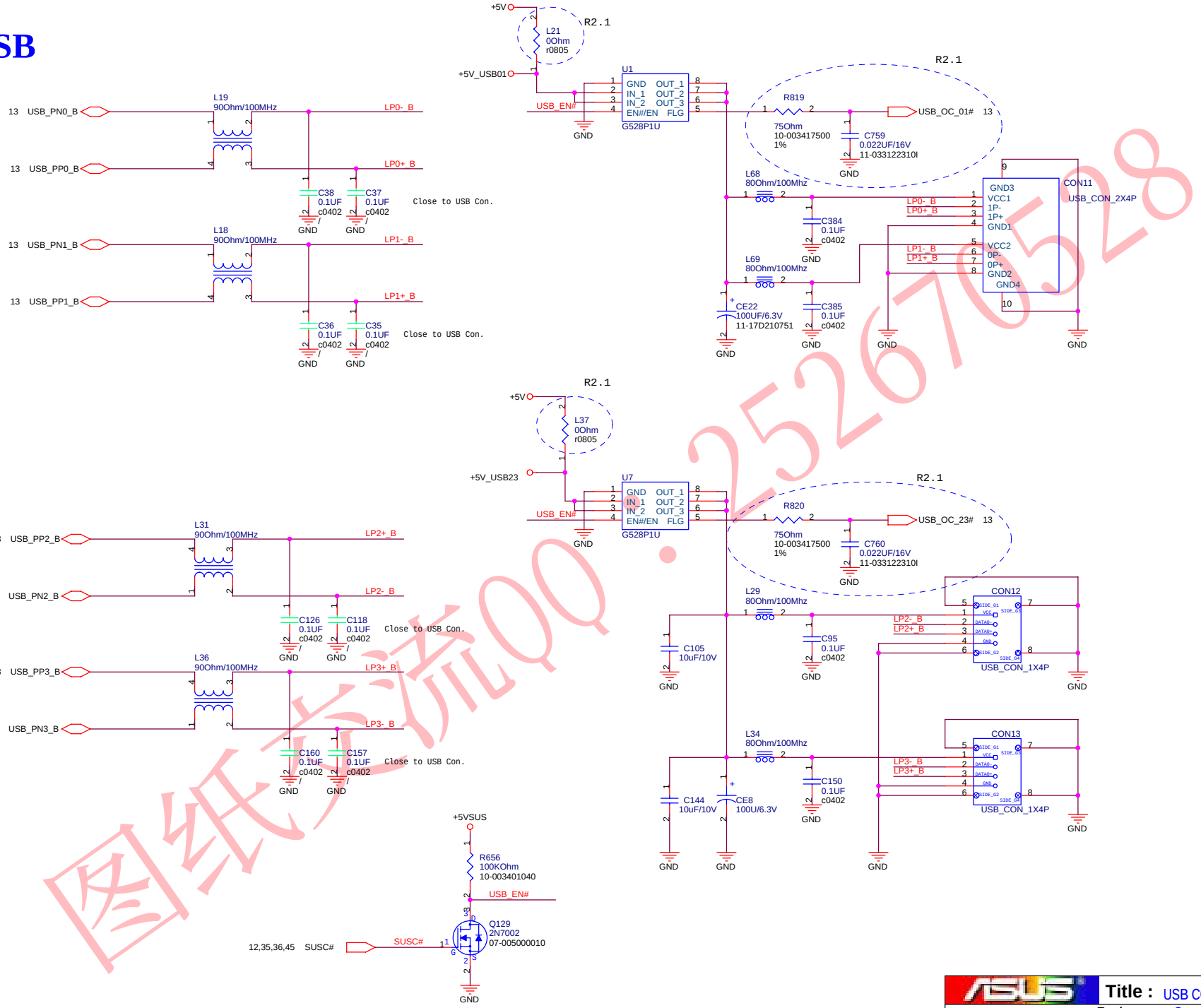
Size	Project Name	Rev
Custom	A3E	2.2

Date: Thursday, May 05, 2005 Sheet 32 of 51

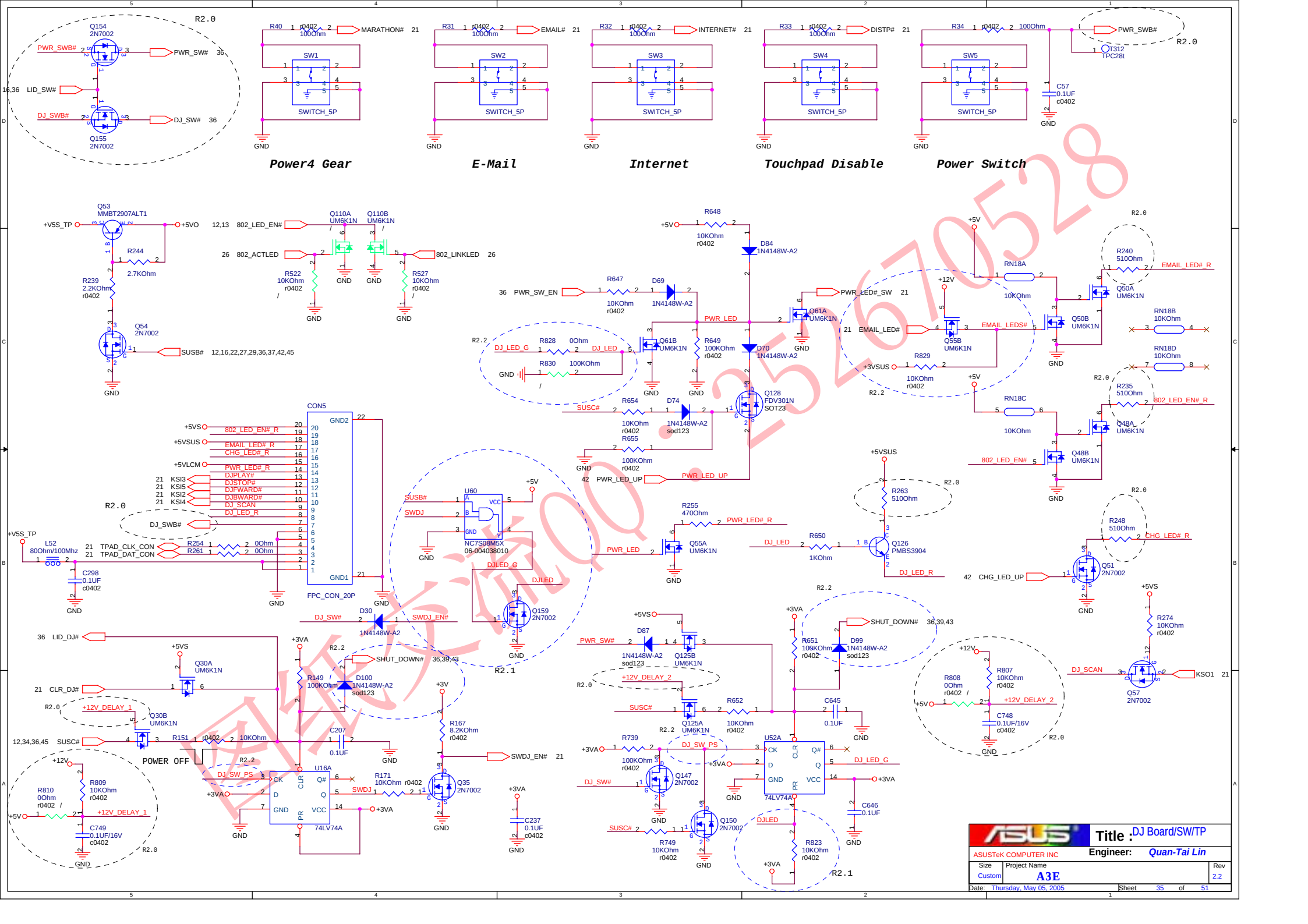


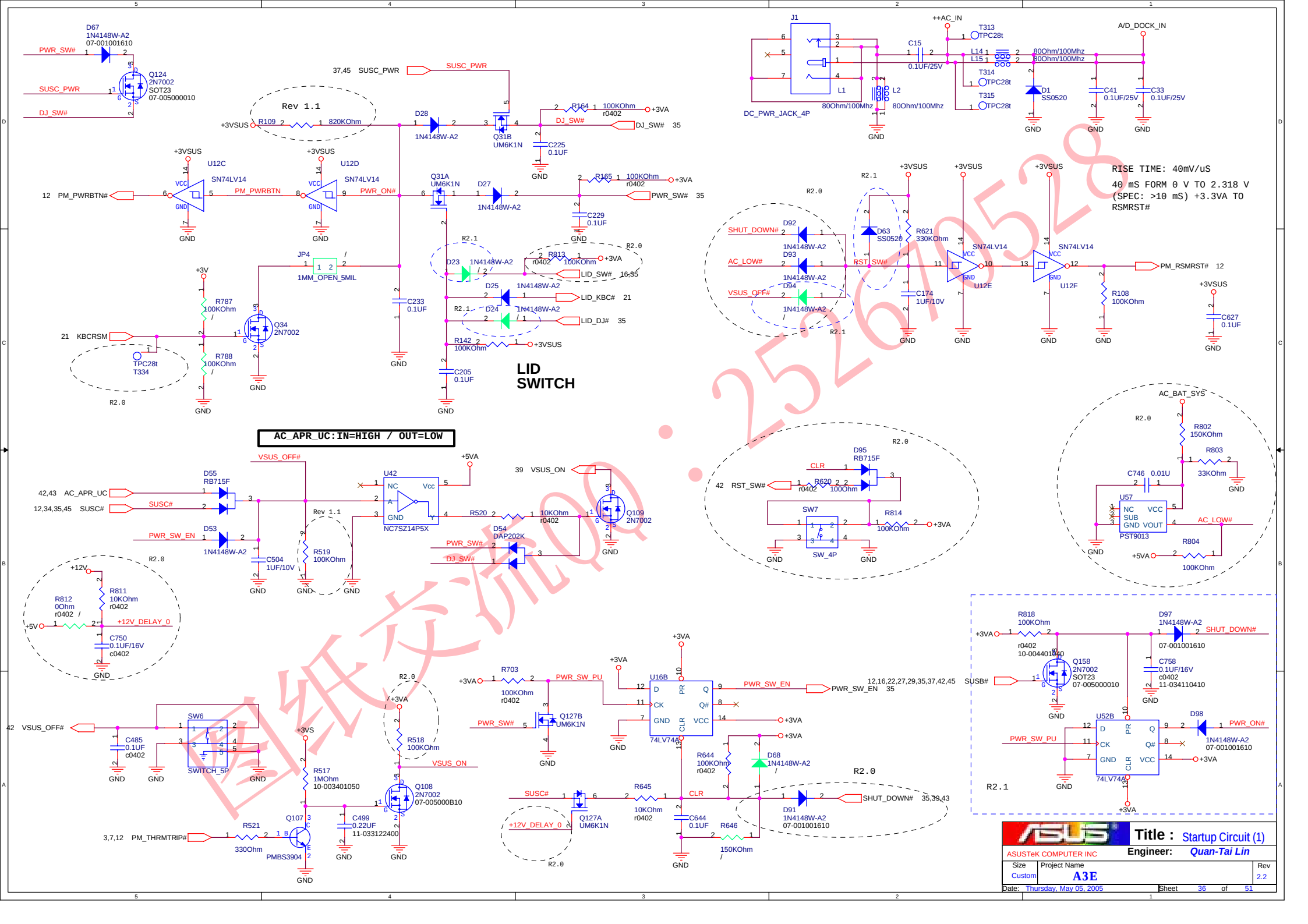
ASUSTeK COMPUTER INC	Title : CDROM	
	Engineer: Quan-Tai Lin	
Size: Custom	Project Name: A3E	Rev: 2.2
Date: Thursday, May 05, 2005	Sheet 33 of 51	

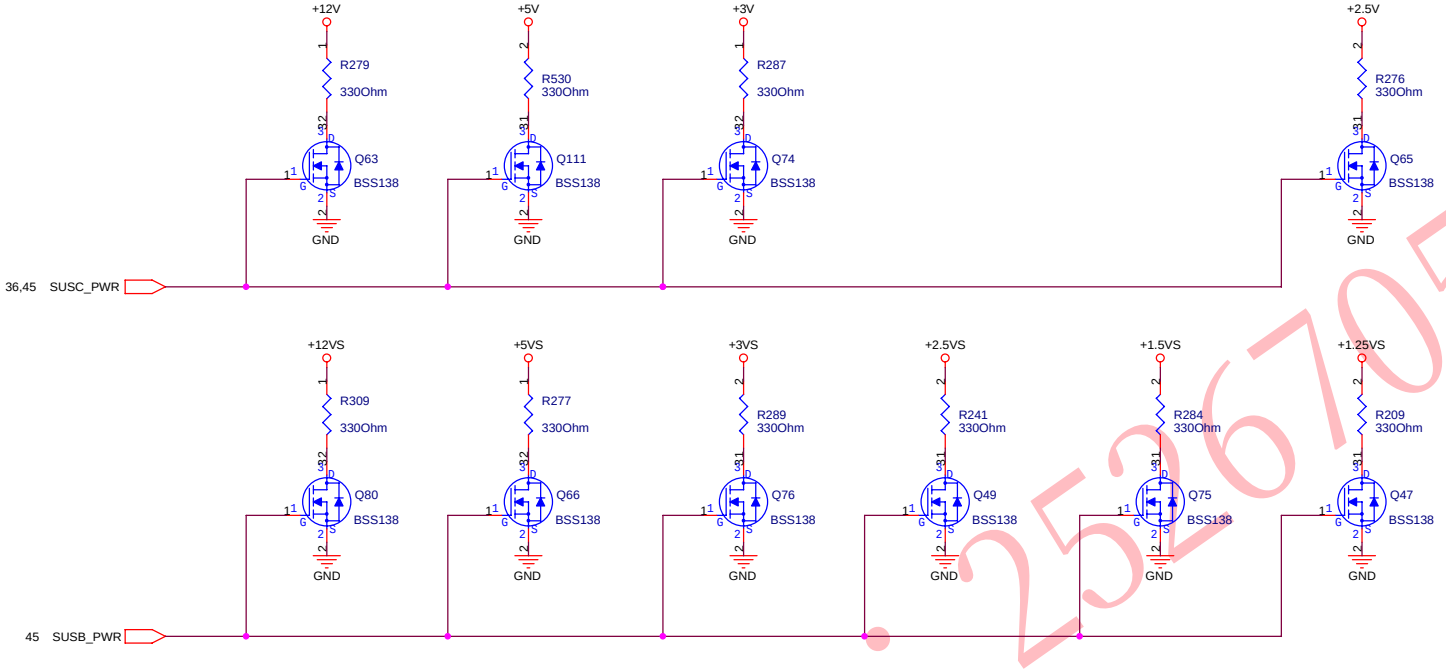
USB



ASUSTeK COMPUTER INC	Title : USB CONN	
	Engineer: Quan-Tai Lin	
Size: Custom	Project Name: A3E	Rev: 2.2
Date: Thursday, May 05, 2005	Sheet 34 of 51	

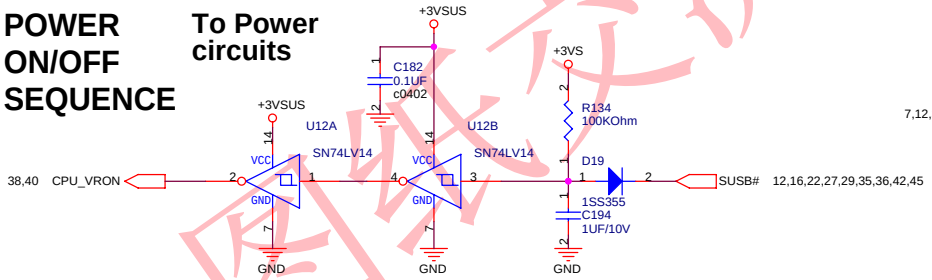

Power4 Gear
E-Mail
Internet
Touchpad Disable
Power Switch
POWER OFF
FPC_CON_20P
Title : DJ Board/SW/TP
ASUSTeK COMPUTER INC
Engineer: Quan-Tai Lin
Project Name A3E
Rev 2.2
Date: Thursday, May 05, 2005
Sheet 35 of 51

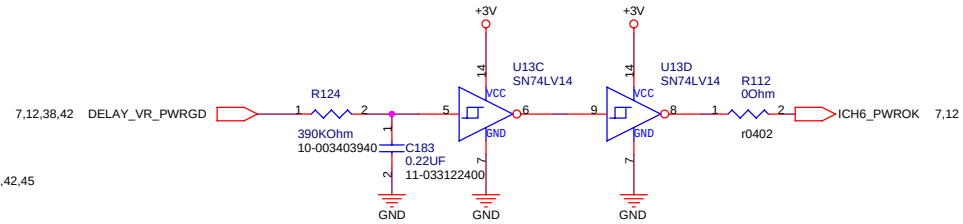

LID SWITCH
AC_APR_UC:IN=HIGH / OUT=LOW
RISE TIME: 40mV/uS
40 mS FORM 0 V TO 2.318 V
(SPEC: >10 mS) +3.3VA TO
RSMRST#
Title : Startup Circuit (1)
ASUSTeK COMPUTER INC
Engineer: Quan-Tai Lin
Size Custom
Project Name A3E
Rev 2.2
Date: Thursday, May 05, 2005
Sheet 36 of 51



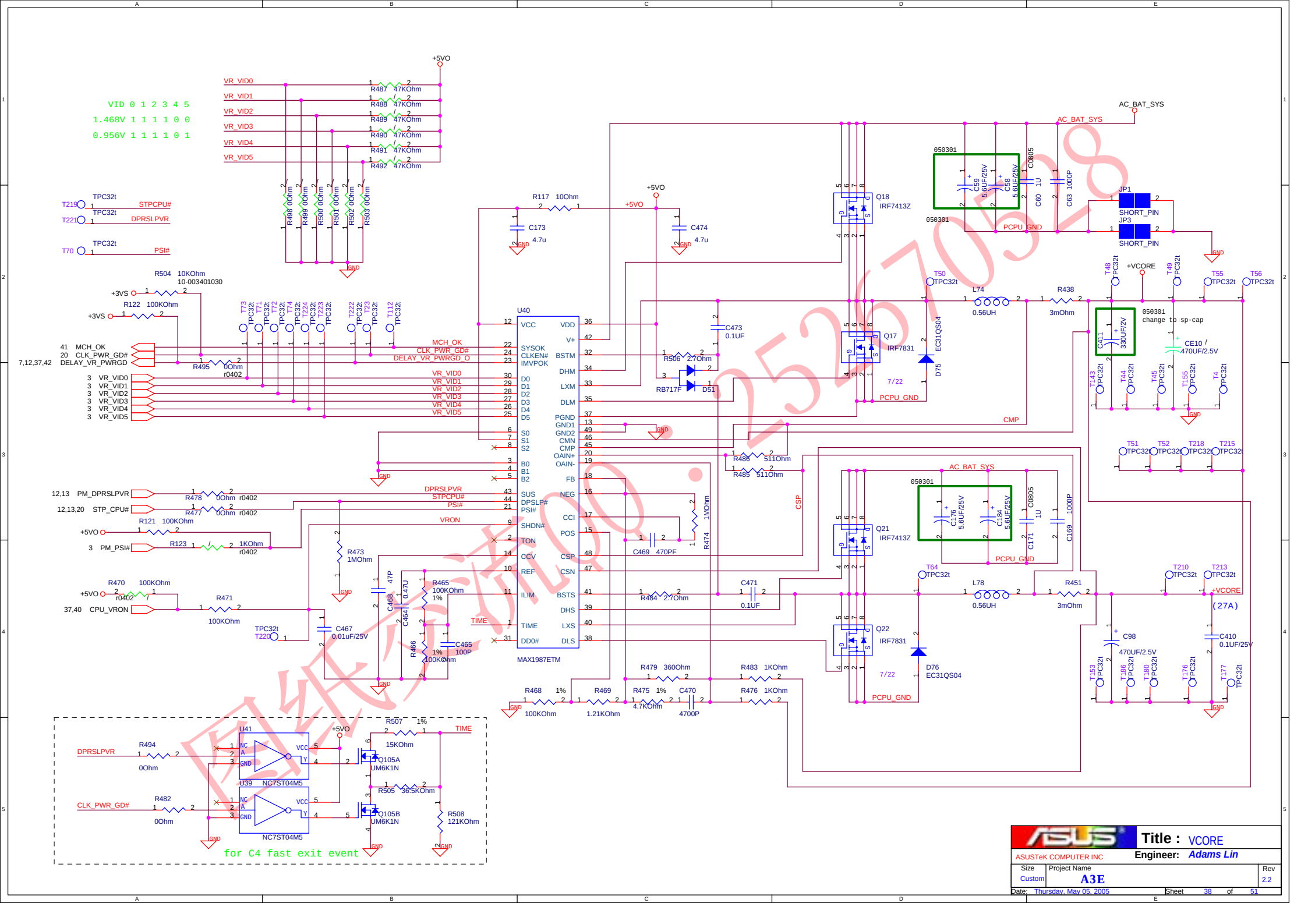
POWER ON/OFF SEQUENCE

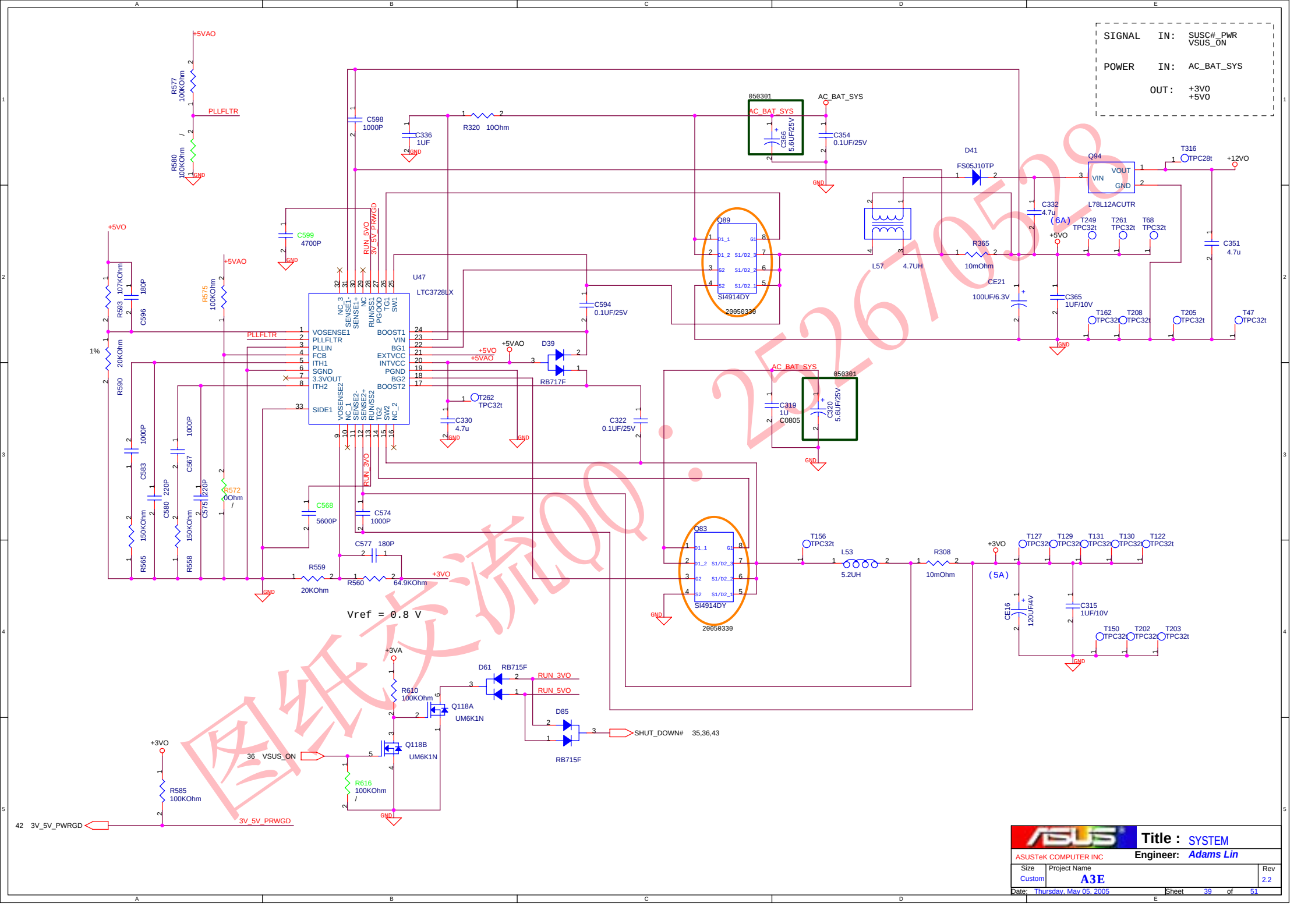
To Power circuits

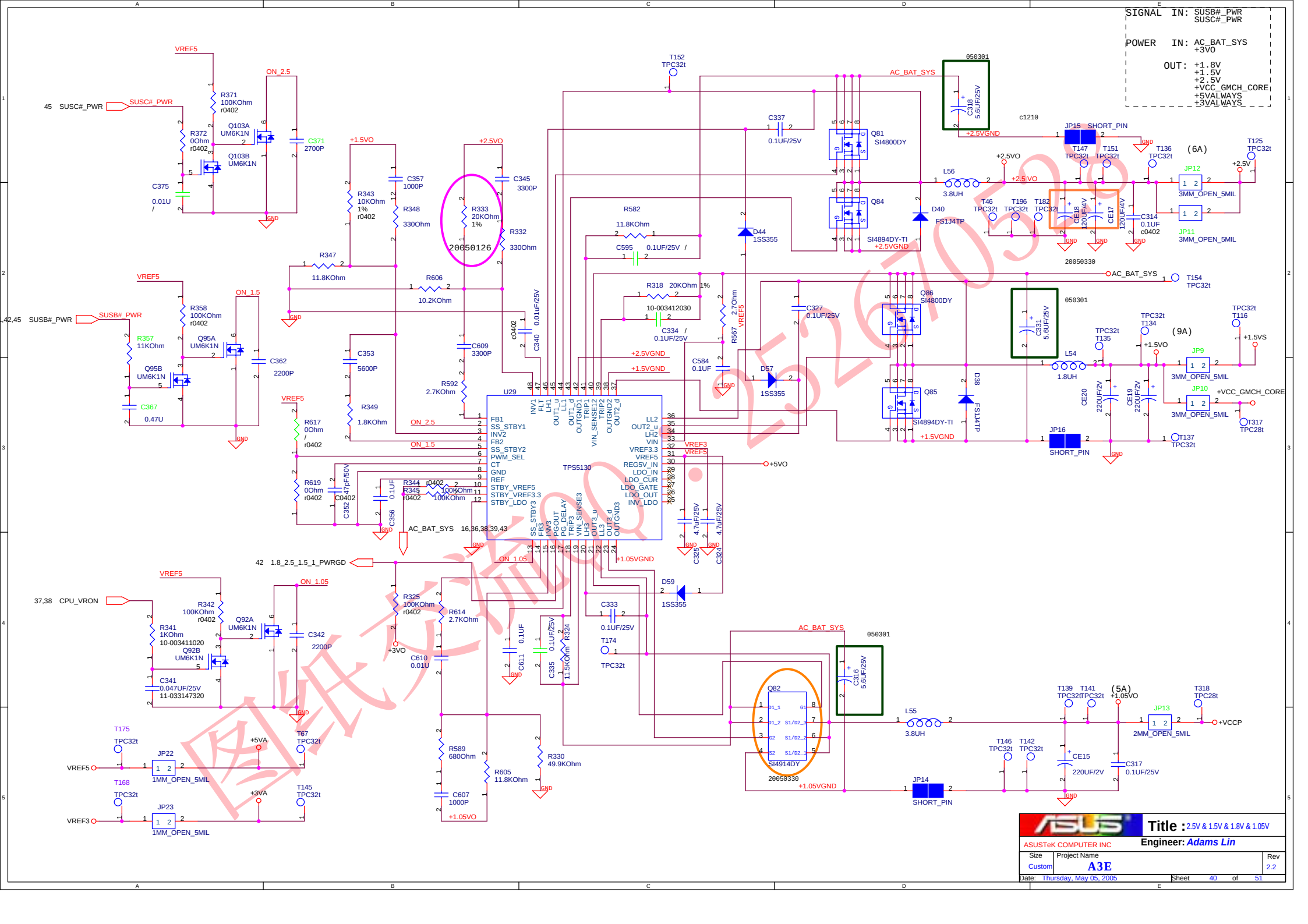




ASUSTeK COMPUTER INC	Title : Startup Circuit (2)	
	Engineer: Quan-Tai Lin	
Size: Custom	Project Name: A3E	Rev: 2.2
Date: Thursday, May 05, 2005	Sheet 37 of 51	


VID 0 1 2 3 4 5
1.468V 1 1 1 1 0 0
0.956V 1 1 1 1 0 1
MAX1987ETM
U40
for C4 fast exit event
AC_BAT_SYS
+5VO
+VCORE
PCPU_GND
CMP
CSP
TIME
Title : VCORE
ASUSTeK COMPUTER INC
Engineer: Adams Lin
Size: Custom
Project Name: A3E
Rev: 2.2
Date: Thursday, May 05, 2005
Sheet 38 of 51


SIGNAL IN: SUSC#_PWR
VSUS_ON
POWER IN: AC_BAT_SYS
OUT: +3VO
+5VO
U47
LTC3728LX
SI4914DY
20050330
Vref = 0.8 V
SHUT_DOWN# 35,36,43
3V_5V_PWRGD
Title : SYSTEM
ASUSTeK COMPUTER INC
Engineer: Adams Lin
Project Name A3E
Date: Thursday, May 05, 2005
Sheet 39 of 51


SIGNAL IN: SUSB#_PWR
SUSC#_PWR
POWER IN: AC_BAT_SYS
+3VO
OUT: +1.8V
+1.5V
+2.5V
+VCC_GMCH_CORE
+5VALWAYS
+3VALWAYS
TPS5130
U29
SI4800DY
SI4894DY-TI
SI4914DY
FS1J4TP
1SS355
20050126
20050330
SHORT_PIN
2MM_OPEN_5MIL
3MM_OPEN_5MIL
1MM_OPEN_5MIL
ASUSTeK COMPUTER INC
Engineer: Adams Lin
Title : 2.5V & 1.5V & 1.8V & 1.05V
Size Custom
Project Name A3E
Rev 2.2
Date: Thursday, May 05, 2005
Sheet 40 of 51

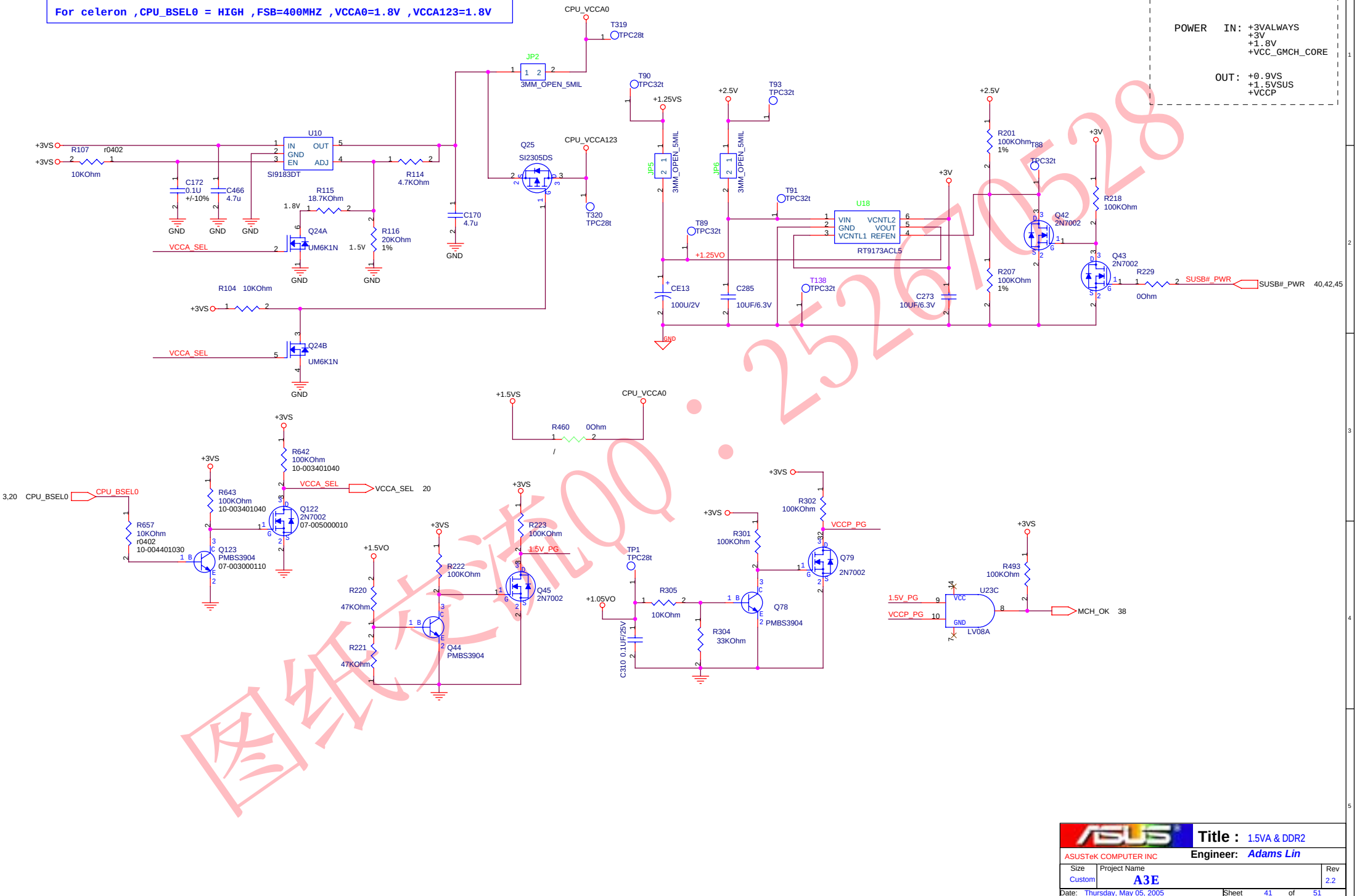
For Duthon ,CPU_BSEL0 = LOW ,FSB=533MHZ ,VCCA0=1.5V ,VCCA123=0V

For celeron ,CPU_BSEL0 = HIGH ,FSB=400MHZ ,VCCA0=1.8V ,VCCA123=1.8V

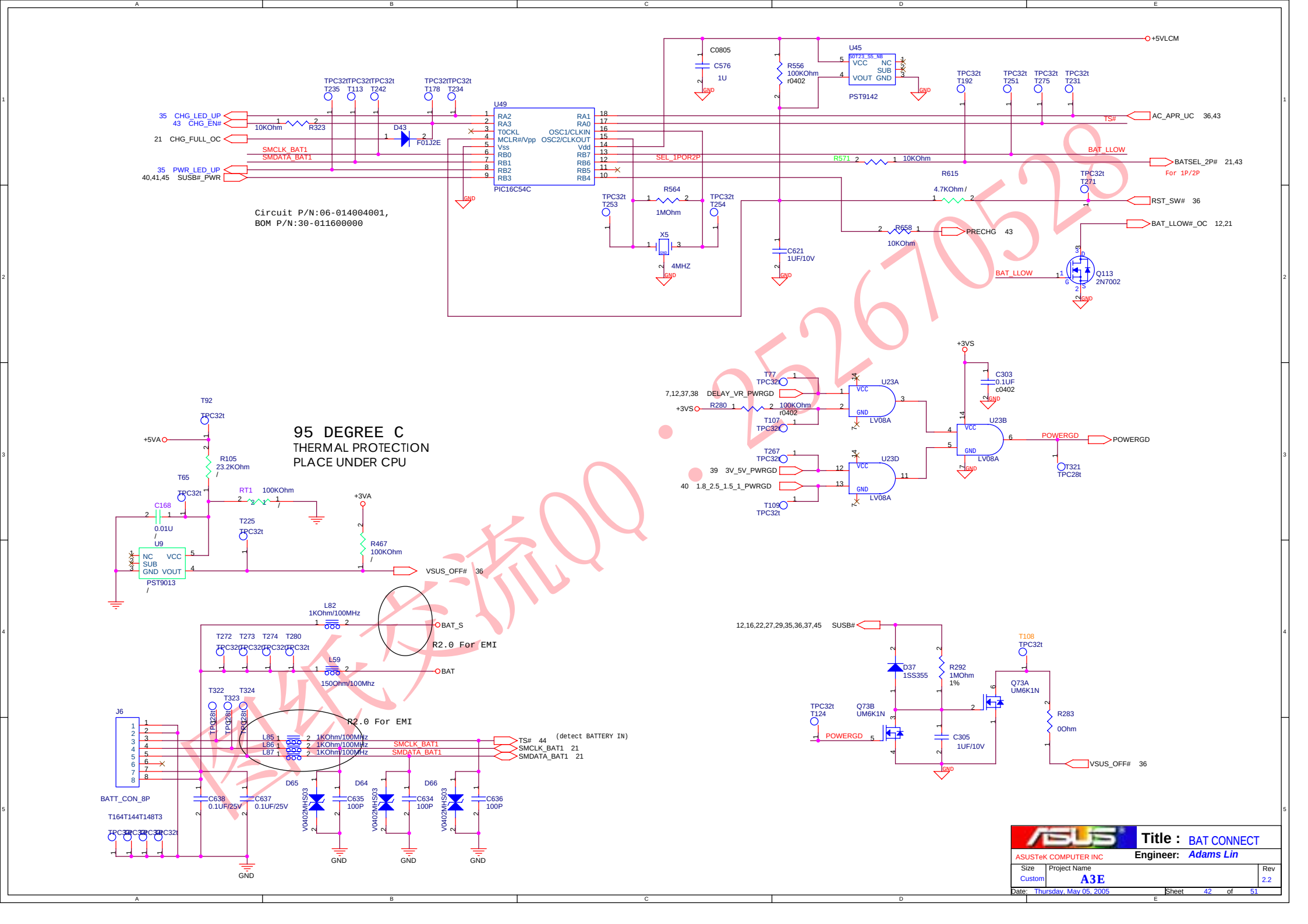
SIGNAL IN: SUSB#_PWR
CPU_VRON

POWER IN: +3VALWAYS
+3V
+1.8V
+VCC_GMCH_CORE

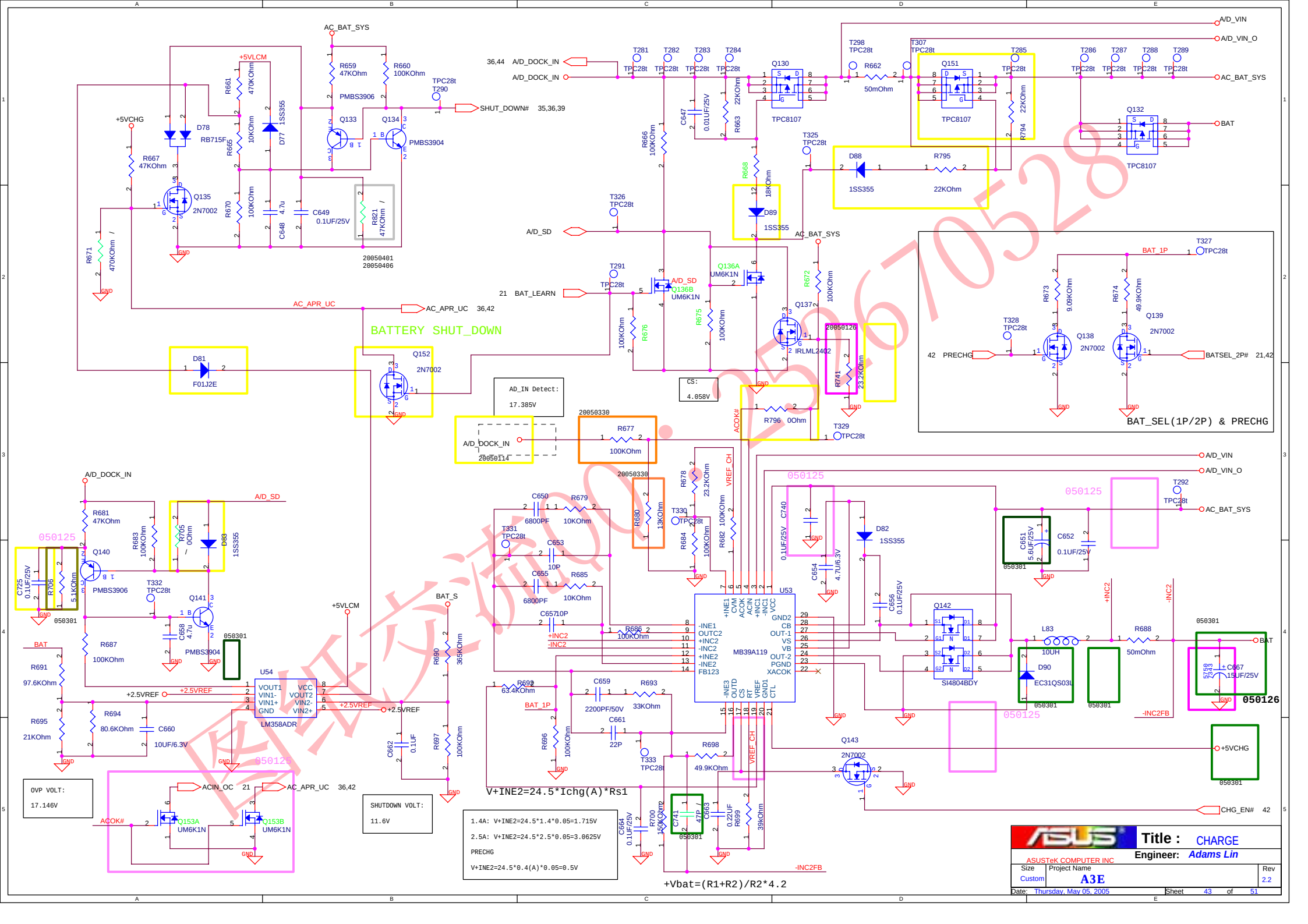
OUT: +0.9VS
+1.5VSUS
+VCCP

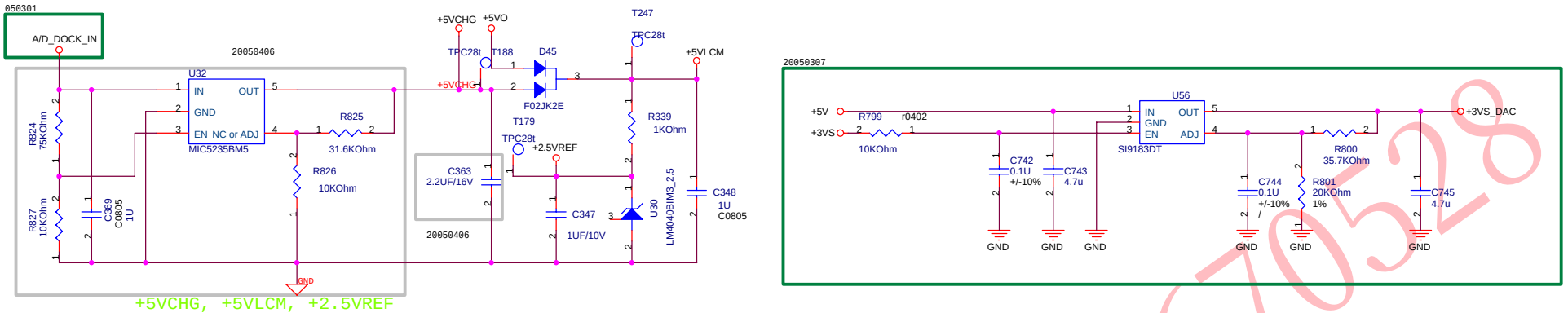


Title : 1.5VA & DDR2		
ASUSTeK COMPUTER INC	Engineer: Adams Lin	
Size: Custom	Project Name: A3E	Rev: 2.2
Date: Thursday, May 05, 2005	Sheet 41 of 51	

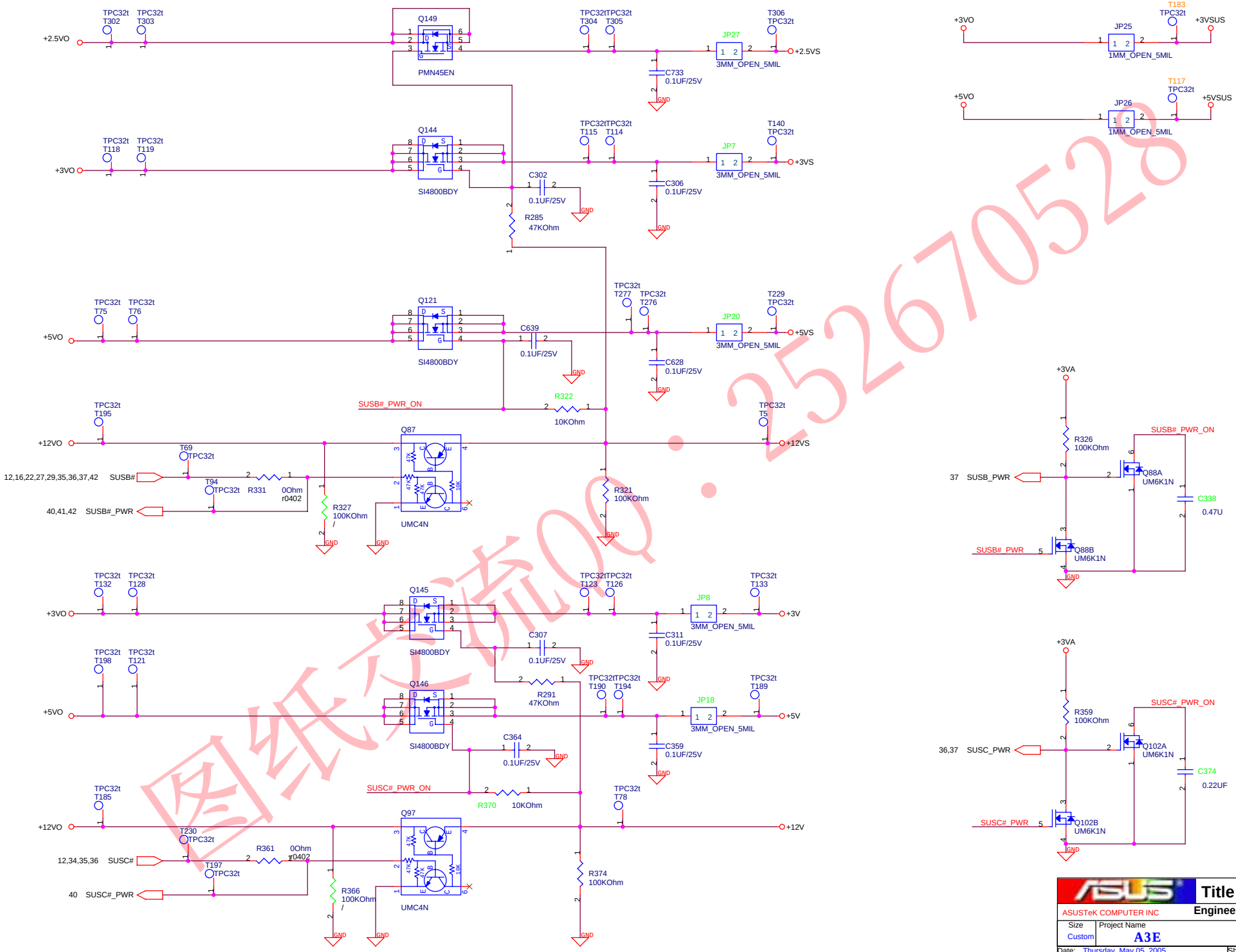


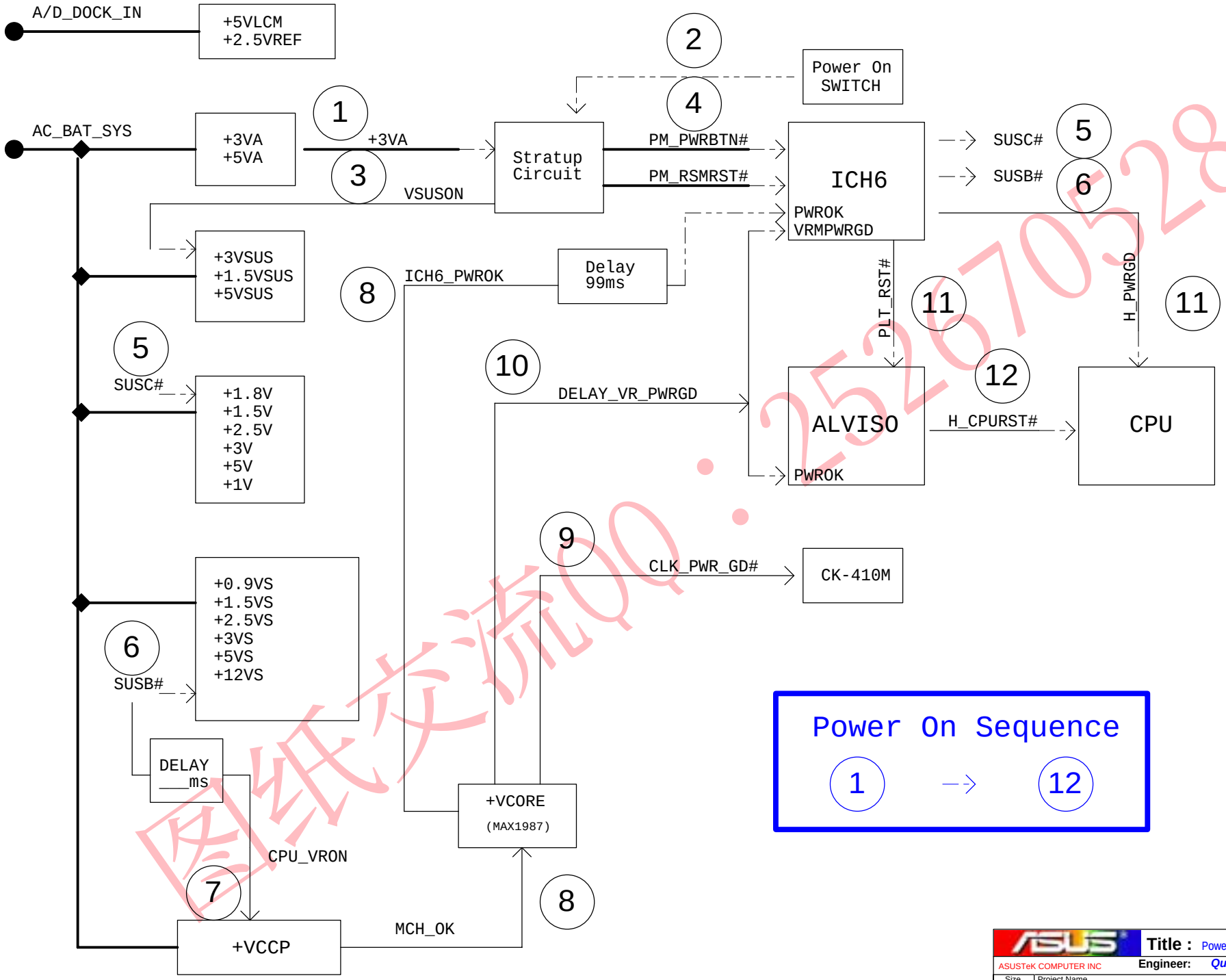
ASUSTeK COMPUTER INC	Title : BAT CONNECT	
	Engineer: Adams Lin	
Size: Custom	Project Name: A3E	Rev: 2.2
Date: Thursday, May 05, 2005	Sheet 42 of 51	


AC_BAT_SYS
+5VLCM
+5VCHG
D78
RB715F
D77
1SS355
R659
47KOhm
R660
100KOhm
PMBS3906
Q133
Q134
PMBS3904
TPC28t
T290
SHUT_DOWN# 35,36,39
R661
470KOhm
R665
10KOhm
R667
47KOhm
Q135
2N7002
R670
100KOhm
C648
4.7u
C649
0.1UF/25V
R821
47KOhm
R671
470KOhm
20050401
20050406
AC_APR_UC
AC_APR_UC 36,42
BATTERY SHUT_DOWN
D81
F01J2E
Q152
2N7002
A/D_DOCK_IN
36,44 A/D_DOCK_IN
T281
T282
T283
T284
Q130
TPC8107
C647
0.01UF/25V
22KOhm
R663
R666
100KOhm
R668
18KOhm
D89
1SS355
T325
T326
A/D_SD
T291
21 BAT_LEARN
Q136A
UM6K1N
Q136B
UM6K1N
R672
100KOhm
R675
100KOhm
R676
100KOhm
Q137
IRLML2402
20050126
R741
23.2KOhm
ACOK#
R796 0Ohm
T329
AD_IN Detect:
17.385V
A/D_DOCK_IN
20050114
CS:
4.058V
20050330
R677
100KOhm
T298
T307
R662
50mOhm
Q151
T285
T286
T287
T288
T289
R794
22KOhm
Q132
BAT
D88
1SS355
R795
22KOhm
A/D_VIN
A/D_VIN_O
AC_BAT_SYS
T327
BAT_1P
R673
9.09KOhm
R674
49.9KOhm
Q139
2N7002
T328
Q138
2N7002
42 PRECHG
BATSEL_2P# 21,42
BAT_SEL(1P/2P) & PRECHG
050125
A/D_DOCK_IN
A/D_SD
R681
47KOhm
R683
100KOhm
R705
0Ohm
D83
1SS355
Q140
PMBS3906
C725
0.1UF/25V
R706
5.1KOhm
050301
T332
Q141
PMBS3904
C658
4.7u
R687
100KOhm
BAT
R691
97.6KOhm
R695
21KOhm
R694
80.6KOhm
C660
10UF/6.3V
+2.5VREF
U54
LM358ADR
VOUT1
VIN1-
VIN1+
GND
VCC
VOUT2
VIN2-
VIN2+
+5VLCM
BAT_S
R690
365KOhm
R697
100KOhm
C662
0.1UF
ACIN_OC 21
AC_APR_UC 36,42
Q153A
UM6K1N
Q153B
UM6K1N
OVP VOLT:
17.146V
SHUTDOWN VOLT:
11.6V
C650
6800PF
R679
10KOhm
T331
C653
10P
C655
6800PF
R685
10KOhm
C65710P
+INC2
-INC2
R686
100KOhm
R692
63.4KOhm
C659
2200PF/50V
R693
33KOhm
C661
22P
T333
BAT_1P
R696
100KOhm
R698
49.9KOhm
C741
47P
C663
0.22UF
R699
39KOhm
C664
0.1UF/25V
R700
150KOhm
V+INE2=24.5*Ichg(A)*Rs1
1.4A: V+INE2=24.5*1.4*0.05=1.715V
2.5A: V+INE2=24.5*2.5*0.05=3.0625V
PRECHG
V+INE2=24.5*0.4(A)*0.05=0.5V
+Vbat=(R1+R2)/R2*4.2
R678
23.2KOhm
R680
13KOhm
R682
100KOhm
R684
100KOhm
VREF_CH
T330
C740
0.1UF/25V
C654
4.7U/6.3V
D82
1SS355
C651
5.6UF/25V
C652
0.1UF/25V
C656
0.1UF/25V
T292
AC_BAT_SYS
U53
MB39A119
+INE1
CVM
ACOK
ACIN
+INC1
-INC1
VCC
GND2
CB
OUT-1
VS
VB
OUT-2
PGND
XACOK
-INE1
OUTC2
+INC2
-INC2
+INE2
-INE2
FB123
-INE3
OUTD
CS
RT
VREF
GND1
CTL
Q142
SI4804BDY
L83
10UH
D90
EC31QS03L
R688
50mOhm
+INC2
-INC2
-INC2FB
C667
15UF/25V
050126
+5VCHG
CHG_EN# 42
Title : CHARGE
Engineer: Adams Lin
ASUSTeK COMPUTER INC
Size Custom
Project Name A3E
Rev 2.2
Date: Thursday, May 05, 2005
Sheet 43 of 51

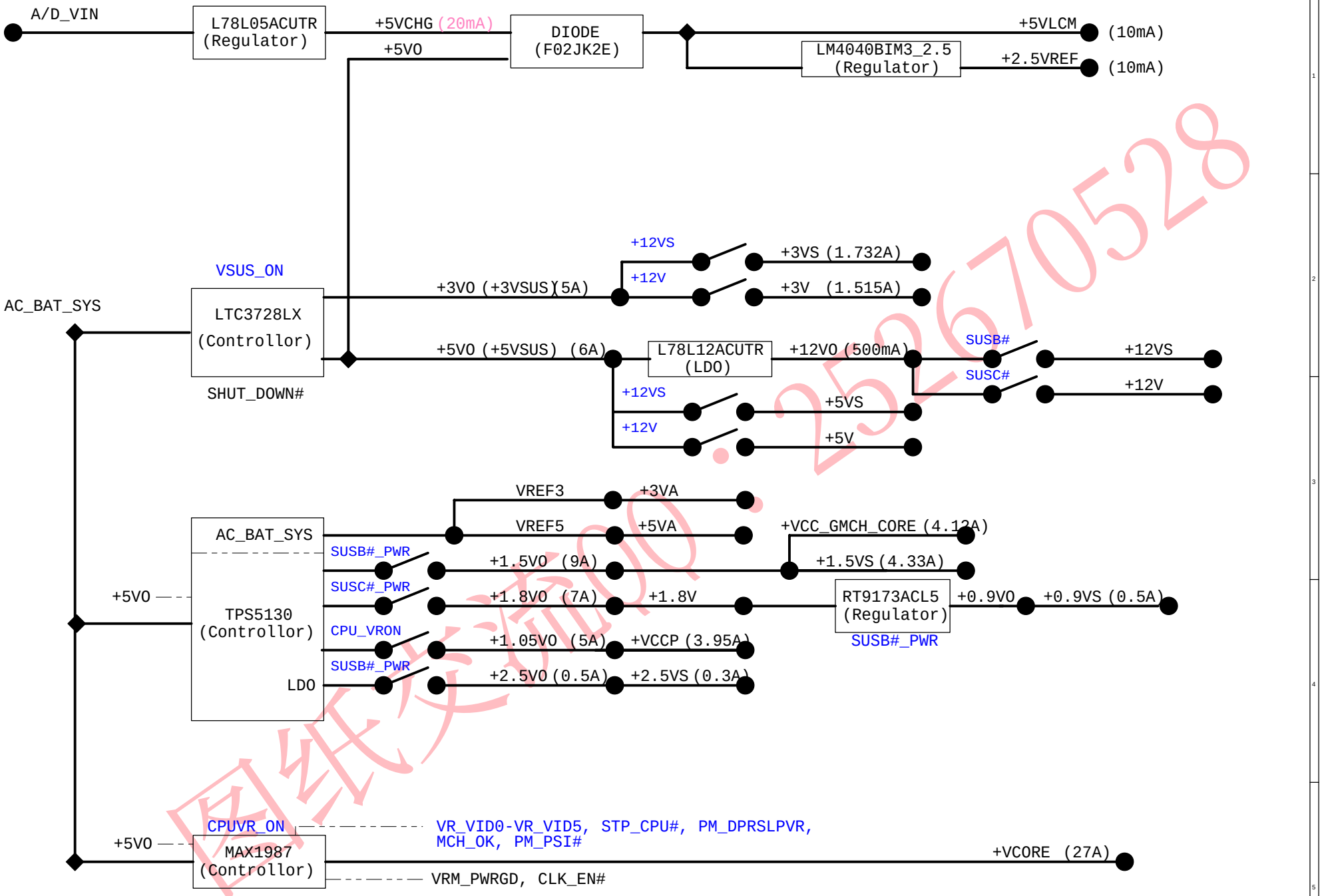


ASUSTeK COMPUTER INC	Title : BATLOW/SD#	
	Engineer: Adams Lin	
Size: Custom	Project Name: A3E	Rev: 2.2
Date: Thursday, May 05, 2005	Sheet 44 of 51	





ASUSTeK COMPUTER INC	Title : Power On Sequence		
	Engineer: Quan-Tai Lin		
Size: Custom	Project Name: A3E		Rev: 2.2
Date: Thursday, May 05, 2005	Sheet 46 of 51		



ASUSTeK COMPUTER INC	Title : POWER FLOWCHART	
	Engineer: Quan-Tai Lin	
Size: Custom	Project Name: A3E	Rev: 2.2
Date: Thursday, May 05, 2005	Sheet 47 of 51	

PCI Device	IDSEL#	REQ/GNT#	Interrupts
10/100 RTL8100CL	AD16	2	E
CARD READER	AD17	1	B
CARDBUS	AD17	1	C
1394	AD17	1	D
MINIPCI (802.11a/b/g)	AD19	3	G,H

SM-Bus Device	SM-Bus Address
Clock Generator	1101001x (D2)
SO-DIMM 0	1010000x (A0)
SO-DIMM 1	1010001x (A2)
Thermal Sensor	0101110x (5C)
PIC	1001001x (92)

ICH6-M GPIO	A5V	Note	Volt
GPI 0			+3VS
GPI 1			+3VS
GPI 2			+3VS
GPI 3			+3VS
GPI 4			+3VS
GPI 5			
GPI 7			+3VS
GPI 8	EXTSMI#		+3VSUS
GPI 11	LID_ICH#		+3VSUS
GPI 12	KB_SCI#		+3VSUS
GPI 13	SIO_SMI#		+3VSUS
GPI 14			+3VSUS
GPI 15			+3VSUS
GPO 16			
GPO 17			
GPO 19	PWRLED_1HZ		+3VS
GPO 21	BACK_OFF#		+3VS
GPO 23	FWH_WP#		+3VS
GPO 24	802_LED_EN#		+3VSUS
GPI 26	SATA_DET#0	Unused pull-up to Vcc3_3	+3VS
GPI 27			+3VSUS
GPI 28			+3VSUS
GPI 29	PCB_ID2	Default : 0	+3VS
GPI 30	PCB_ID0	Default : 0	+3VS
GPI 31	PCB_ID1	Default : 0	+3VS
GPI 33	CPUFAN_SPD_A		+3VS
GPO 34	WLAN_ON#		+3VS
GPI 40	PANEL_ID0		+3VS
GPI 41	PANEL_ID1		+3VS
GPO 48			
GPO 49			
GPIO 25	CB_SD#	Diode	+3V

KBC GPIO	A5V	Note
P23(Pin 35)	CHG_FULL_OC	
P22(Pin 36)	BAT_LEARN	
P21(Pin 37)	KBC_P21	
P20(Pin 38)	KBCRSM	
P42(Pin 23)	WATCHDOG	
P43(Pin 22)	OP_SD#	POSTCode前拉Low,ACPI前拉High,ACPI後放掉
P44(Pin 21)	KB_CPURST	
P45(Pin 20)	KB_GATEA20	
P46(Pin 19)	KBCSCI	
P47(Pin 18)	PM_CLKRUN#	
P50(Pin 17)	BAT_LLOW#_OC	
P51(Pin 16)	KID1	
P52(Pin 15)	KID2	
P53(Pin 14)	CLR_DJ#	
P54(Pin 13)	BAT_SEL#	
P55(Pin 12)	BAT1_IN#_OC	
P56(Pin 11)	FAN_DA1	
P57(Pin 10)	ADJ_BL	
P67(Pin 74)	DJ_LED#	
P66(Pin 75)	SWDJ_EN#	
P65(Pin 76)	GAIN_AMP_K#	0->6 V/V 1->NORMAL
P64(Pin 77)	ACIN_OC	
P63(Pin 78)	DISTP#	
P62(Pin 79)	MARATHON#	
P61(Pin 80)	INTERNET#	
P60(Pin 1)	EMAIL#	
P75(Pin 4)	KB_CLK	
P74(Pin 5)	MS_CLK	
P73(Pin 6)	TPAD_CLK	
P72(Pin 7)	KB_DAT	
P71(Pin 8)	MS_DAT	
P70(Pin 9)	TPAD_DAT	
P77(Pin 2)	SMC_BAT	
P76(Pin 3)	SMD_BAT	
P27(Pin 31)	SCROLL_LED#	
P26(Pin 32)	NUM_LED#	
P25(Pin 33)	CAP_LED#	
P24(Pin 34)	SET_PLTRSTNS#	
P40(Pin 27)	EXT_SMI	
P41(Pin 26)	EMAIL_LED#	

Title : System Resource

ASUSTeK COMPUTER INC Engineer: Quan-Tai Lin

Size	Project Name	Rev
Custom	A3E	2.2

Date: Thursday, May 05, 2005 Sheet 48 of 51

Rev.	Data	Description
1.0	05' 01/06	Initial release
2005/01/21-1140		R735.R736.R750.R752 footprint change to 0603
		JP28 for CMOS clear renames to JRST1 and no mount U19.77 signal changes to ACIN_OC and R245 still mount R73.R75.R76.R77 value change to 470ohm and R41 is 330ohm R519 value changes to 100Kohm
2005/01/24-1035		Add SW8 ,R797 but no mount
2005/01/26-0945		R109 value changes to 820Kohm D72 mount
2005/02/01-1300		R735.R736.R750.R752 tolerance change to 1%
2005/02/21-1300		Add test point :T309(+Vcc_RTC).T310(+RTCBAT).T311(R545.2). T312(PWR_SW#).T313.T314.T315(++AC_IN)
2005/03/01-1130		Add R798 to connect signal MIC_IN_R and MIC_IN_L R163. L43 no mount Add Q154 .Q155 to let LID_SW# to control PWR_SWB# and DJ_SWB# to be on or off Add D91 to connect to SHUT_DOWN# signal
2005/03/04-1600		U19.13 exchange to U19.35 (BAT_SEL# exchange to CHG_FULL_OC) GPIO29=PCB_ID0,GPIO30=PCB_ID1,GPIO31=PCB_ID2 PCB_ID0=1,PCB_ID1=0,PCB_ID2=0
2005/03/07-1500		R518 change to 100Kohm to prevent from +3VA sinking too much current Change CE10 to power and change CE9 to 470UF/2.5V L27.2 and L22.2 change to +3VS_DAC
2005/03/08-0950		Add D92.D93.D94,U57,C746,R802.R803.R804 to prevent from abnormal shut down in startup circuit Change R41 value to 470ohm,R77.R75.R76.R73.R240.R235.R248.R263 to 510ohm Change R184 to 100Kohm and add C747 1uF/10V Add T334 to R788.1 for KBCRSM signal
2005/03/10-1128		Colay Q156, R805and Q157,R806 for keep from PCMCIA device current leakage Q125,Q30,Q127 turn on voltage change to a RC delay +12V Add R811.C750.R812 for +12V_DELAY_0 signal Add R809.C749.R810 for +12V_DELAY_1 signal Add R807.C748.R808 for +12V_DELAY_2 signal
2005/03/11-1120		Add C751.C752 for EMI(P.28) Add C754.C755 100PF for EMI(P.16) Add C753 100PF. R815 0ohm for EMI(P.16) Add U58.U59 for EMI(P.4) Add R813 to pull up LID_SW# to +3VA Add D95.R814 to make RESET button (SW7) function to be ok
2005/03/14-1040		Delete T53.T207.T217.T214.T211.T212.T209.T216 Add C756.C757 47UF/6.3V 1206 to +2.5VS on page 9 Add D96.RP5.RP6.R816 and pull to +5VS for LPT C751.C752 footprint change to 1812_h71 Add H26.H27
2005/03/15-2050		Add R817 10Kohm to pull high to +3VS on page 5

Rev.	Data	Description
2005/03/16-1600		R178.R198 value change to 3.9Kohm 1% C630.C631.C632.C633 still mount C751.C752 still mount R625.R632.R633.R634 change to 120ohm/100MHz bead R175.R199 still mount L50.R150 change to 1Kohm/100MHz bead L6.L7.L8 change to 60ohm /100MHz bead R162 change value to 4.7Kohm 1% CE9 change to 470UF/2.5V
		Rev 2.1
2005/03/29-1710		Add D63 back and D94 is no mount
2005/04/01-1228		Add U52B,D98,D97,R818,C758,Q158 for start up circuit D23.D24 no mount Add R819.C759 between U1.5 (FLG) and USB_OC_01# Add R820.C760 between U7.5 (FLG) and USB_OC_23# C751.C752 footprint changes to C1808_inverter_h79
2005/04/06		L21.L37 change to 0ohm resistance (0805) Add U60.R822.R823.Q159 for LED signal

ASUSTeK COMPUTER INC

Title : History-EE(1)

Engineer: Quan-Tai Lin

Size	Project Name	Rev
A3	A3E	2.2

Date: Thursday, May 05, 2005 Sheet 49 of 51

Rev.	Data	Description
		For RM:
	2005/01/24-1035	Page 31 no mount : R566,Q114,Q115,C579,C564 Page 20 no mount : R54,R43,Q16,Q19,R412 Page 41 no mount : R657,R643,Q122,Q123 Mount SW8 ,R797 Add SWITCH TABLE for CPU frequency select

Rev.	Data	Description

ASUSTeK COMPUTER INC	Title : History-EE(2)	
	Engineer: Quan-Tai Lin	
Size: Custom	Project Name: A3E	Rev: 2.2
Date: Thursday, May 05, 2005	Sheet 50 of 51	

Rev.	Data	Description
1.0	05' 01/06	Initial release
2005/01/21-1200		Add 22Kohm R794.R795 , P-MOS Q151 , diode D88.D89
2005/01/21-1200		Add capacitor C739,resistor R796,N-MOS Q152,diode D90
2005/01/21-1200		R677 value is from 110Kohm to 107Kohm and R677.1 connect to A/D_DOCK_IN
2005/01/21-1200		R680 value is from 14Kohm to 13.7Kohm and D81 changes to F01J2E
2005/01/21-1200		D83 mount and R705 no mount and R725 mount
2005/01/26-0945		R333 value changes to 20Kohm
2005/01/26-0945		Add Q153 for ACIN_OC and AC_APR_UC signals and delete D90
2005/01/26-0945		Change U53.18 and U53.19 for signal VREF_CH
2005/01/26-0945		Delete JP24 and add a cap C740 0.1UF
2005/01/26-0945		C725 still mount and R706 no mount
2005/01/26-0945		R741 value changes to 23.2K ohm
2005/01/26-1250		C666 changes to connect to L83.2
2005/01/28-1200		C666 no mount
2005/02/21-1300		Add test point : T316(+12VO).T317(+VCC_GMCH_CORE).T318(+VCCP). T319(CPU_VCCA0).T320(CPU_VCCA123).T322(R631.1).T323(R630.1). T324(R629.1).T321(POWERGD).T329(R796.2).T326(A/D_SD).T325(D88.2). T332(C658.1).T330(R684.2).T333(C661.1).T327(BAT_1P).T331(C653.2). T328(PRECHG)
2005/03/01-1800		Change C59, C58, C176, C184, C366, C320, C318, C331, C316, C651 to POSCAP 5.6UF/25V Add D90 for Charger noise(P. 43) Remove C666, R705, R689 Change r706 to 5.1Kohm Change U53 Pin 21 connector to +5VCHG Change U32 Pin 1 connector to A/D_DOCK_IN Change C441 to 330UF/2V SP-CAP Change C98 to 470UF/2.5V POSCAP Add C741 47PF/50V with R700(P.43) Change C667 to 15UF/2.5V POSCAP
2005/03/30-1124		Change R677 to 100Kohm Change R680 to 13Kohm Change CE17,CE18 to 220UF/4V Mount R283 Change Q82, Q83, Q89 to SI4914
2005/04/01-1640		Change CE17,CE18 to 120UF/4V Add R821 47Kohm for boot issue

Rev.	Data	Description
2005/04/06-1524		Change U32 to MIC5235BM5 Add R824=75K, R827=10K, R825=31.6K, R826=10K Change C363 to 2.2UF/16V Change R821 to unmount

ASUSTeK COMPUTER INC	Title : History-PWR	
	Engineer: Quan-Tai Lin	
Size: Custom	Project Name: A3E	Rev: 2.2
Date: Thursday, May 05, 2005	Sheet 51 of 51	