CD54/74AC74, CD54/74ACT74

Data sheet acquired from Harris Semiconductor
SCHS231C

September 1998 - Revised June 2002

Dual D-Type Flip-Flop with Set and Reset Positive-Edge-Triggered

Features

- **Buffered Inputs**
- **Typical Propagation Delay (AC00)**
  - **4.9ns at V_{CC} = 5V, T_A = 25^oC, C_L = 50pF**
- **Exceeds 2kV ESD Protection MIL-STD-883, Method 3015**
- **SCR-Lachup-Resistant CMOS Process and Circuit Design**
- **Speed of Bipolar FAST™/AS/S with Significantly Reduced Power Consumption**
- **Balanced Propagation Delays**
- **AC Types Feature 1.5V to 5.5V Operation and Balanced Noise Immunity at 30% of the Supply**
- **±24mA Output Drive Current**
  - **Fanout to 15 FAST™ ICs**
  - **Drives 50Ω Transmission Lines**

Description

The 'AC74 and 'ACT74 dual D-type, positive edge triggered flip-flops use ADVANCED CMOS technology. These flip-flops have independent DATA, $\overline{SET}$, $\overline{RESET}$, and CLOCK inputs and Q and $\overline{Q}$ outputs. The logic level present at the data input is transferred to the output during the positive going transition of the clock pulse. $\overline{SET}$ and $\overline{RESET}$ are independent of the clock and are accomplished by a low level at the appropriate input.

Ordering Information

PART NUMBER	TEMP. RANGE (^oC)	PACKAGE
CD54AC74F3A	-55 to 125	14 Ld CERDIP
CD74AC74E	0 to 70, -40 to 85, -55 to 125	14 Ld PDIP
CD74AC74EX	0 to 70, -40 to 85, -55 to 125	14 Ld PDIP
CD74AC74M	0 to 70, -40 to 85, -55 to 125	14 Ld SOIC
CD54ACT74F3A	-55 to 125	14 Ld CERDIP
CD74ACT74E	0 to 70, -40 to 85, -55 to 125	14 Ld PDIP
CD74ACT74EX	0 to 70, -40 to 85, -55 to 125	14 Ld PDIP
CD74ACT74M	0 to 70, -40 to 85, -55 to 125	14 Ld SOIC

NOTES:

1. When ordering, use the entire part number. Add the suffix 96 to obtain the variant in the tape and reel.
2. Wafer and die for this part number is available which meets all electrical specifications. Please contact your local TI sales office or customer service for ordering information.

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.

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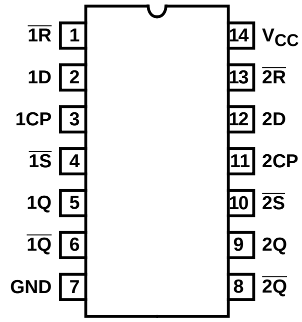
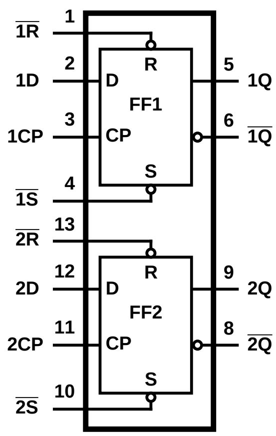
Pinout

CD54AC74, CD54ACT74
(CERDIP)
CD74AC74, CD74ACT74
(PDIP, SOIC)
TOP VIEW



Functional Diagram



TRUTH TABLE

INPUTS				OUTPUTS	
$\overline{SET}$	$\overline{RESET}$	CP	D	Q	$\overline{Q}$
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	H (Note 5)	H (Note 5)
H	H	↑	H	H	L
H	H	↑	L	L	H
H	H	L	X	Q0	$\overline{Q0}$

NOTES:

3. H = High level (steady state), L = Low level (steady state), X = Don't care, ↑ = Transition from Low to High level.
4. Q0 = the level of Q before the indicated input conditions were established.
5. This configuration is nonstable, that is, it will not persist when set and reset inputs return to their inactive (high) level.

Absolute Maximum Ratings

DC Supply Voltage, V_{CC} . . . . -0.5V to 6V
DC Input Diode Current, I_{IK}
For V_I < -0.5V or V_I > V_{CC} + 0.5V . . . .±20mA
DC Output Diode Current, I_{OK}
For V_O < -0.5V or V_O > V_{CC} + 0.5V . . . .±50mA
DC Output Source or Sink Current per Output Pin, I_O
For V_O > -0.5V or V_O < V_{CC} + 0.5V . . . .±50mA
DC V_{CC} or Ground Current, $I_{CC\ or}\ I_{GND}$ (Note 6) . . . .±100mA

Operating Conditions

Temperature Range, T_A . . . . -55°C to 125°C
Supply Voltage Range, V_{CC} (Note 7)
AC Types. . . . . .1.5V to 5.5V
ACT Types . . . . .4.5V to 5.5V
DC Input or Output Voltage, V_I, V_O . . . . 0V to V_{CC}
Input Rise and Fall Slew Rate, dt/dv
AC Types, 1.5V to 3V . . . . 50ns (Max)
AC Types, 3.6V to 5.5V. . . . . 20ns (Max)
ACT Types, 4.5V to 5.5V. . . . . 10ns (Max)

Thermal Information

Thermal Resistance (Typical, Note 8) θ_{JA} (°C/W)
PDIP Package 90
SOIC Package 175
Maximum Junction Temperature (Plastic Package) . . . . 150°C
Maximum Storage Temperature Range . . . .-65°C to 150°C
Maximum Lead Temperature (Soldering 10s) . . . . 300°C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTES:

6. For up to 4 outputs per device, add ±25mA for each additional output.
7. Unless otherwise specified, all voltages are referenced to ground.
8. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

DC Electrical Specifications

PARAMETER	SYMBOL	TEST CONDITIONS V_I (V)	TEST CONDITIONS I_O (mA)	V_{CC} (V)	25°C MIN	25°C MAX	-40°C TO 85°C MIN	-40°C TO 85°C MAX	-55°C TO 125°C MIN	-55°C TO 125°C MAX	UNITS
AC TYPES											
High Level Input Voltage	V_{IH}	-	-	1.5	1.2	-	1.2	-	1.2	-	V
				3	2.1	-	2.1	-	2.1	-	V
				5.5	3.85	-	3.85	-	3.85	-	V
Low Level Input Voltage	V_{IL}	-	-	1.5	-	0.3	-	0.3	-	0.3	V
				3	-	0.9	-	0.9	-	0.9	V
				5.5	-	1.65	-	1.65	-	1.65	V
High Level Output Voltage	V_{OH}	V_{IH} or V_{IL}	-0.05	1.5	1.4	-	1.4	-	1.4	-	V
			-0.05	3	2.9	-	2.9	-	2.9	-	V
			-0.05	4.5	4.4	-	4.4	-	4.4	-	V
			-4	3	2.58	-	2.48	-	2.4	-	V
			-24	4.5	3.94	-	3.8	-	3.7	-	V
			-75 (Note 9, 10)	5.5	-	-	3.85	-	-	-	V
			-50 (Note 9, 10)	5.5	-	-	-	-	3.85	-	V

DC Electrical Specifications (Continued)

PARAMETER	SYMBOL	TEST CONDITIONS V_I (V)	TEST CONDITIONS I_O (mA)	V_{CC} (V)	25°C MIN	25°C MAX	-40°C TO 85°C MIN	-40°C TO 85°C MAX	-55°C TO 125°C MIN	-55°C TO 125°C MAX	UNITS
Low Level Output Voltage	V_{OL}	V_{IH} or V_{IL}	0.05	1.5	-	0.1	-	0.1	-	0.1	V
			0.05	3	-	0.1	-	0.1	-	0.1	V
			0.05	4.5	-	0.1	-	0.1	-	0.1	V
			12	3	-	0.36	-	0.44	-	0.5	V
			24	4.5	-	0.36	-	0.44	-	0.5	V
			75 (Note 9, 10)	5.5	-	-	-	1.65	-	-	V
			50 (Note 9, 10)	5.5	-	-	-	-	-	1.65	V
Input Leakage Current	I_I	V_{CC} or GND	-	5.5	-	±0.1	-	±1	-	±1	µA
Quiescent Supply Current, FF	I_{CC}	V_{CC} or GND	0	5.5	-	4	-	40	-	80	µA
ACT TYPES											
High Level Input Voltage	V_{IH}	-	-	4.5 to 5.5	2	-	2	-	2	-	V
Low Level Input Voltage	V_{IL}	-	-	4.5 to 5.5	-	0.8	-	0.8	-	0.8	V
High Level Output Voltage	V_{OH}	V_{IH} or V_{IL}	-0.05	4.5	4.4	-	4.4	-	4.4	-	V
			-24	4.5	3.94	-	3.8	-	3.7	-	V
			-75 (Note 9, 10)	5.5	-	-	3.85	-	-	-	V
			-50 (Note 9, 10)	5.5	-	-	-	-	3.85	-	V
Low Level Output Voltage	V_{OL}	V_{IH} or V_{IL}	0.05	4.5	-	0.1	-	0.1	-	0.1	V
			24	4.5	-	0.36	-	0.44	-	0.5	V
			75 (Note 9, 10)	5.5	-	-	-	1.65	-	-	V
			50 (Note 9, 10)	5.5	-	-	-	-	-	1.65	V
Input Leakage Current	I_I	V_{CC} or GND	-	5.5	-	±0.1	-	±1	-	±1	µA
Quiescent Supply Current, FF	I_{CC}	V_{CC} or GND	0	5.5	-	4	-	40	-	80	µA
Additional Supply Current per Input Pin TTL Inputs High 1 Unit Load	ΔI_{CC}	V_{CC} -2.1	-	4.5 to 5.5	-	2.4	-	2.8	-	3	mA

NOTES:

9. Test one output at a time for a 1-second maximum duration. Measurement is made by forcing current and measuring voltage to minimize power dissipation.
10. Test verifies a minimum 50Ω transmission-line-drive capability at 85°C, 75Ω at 125°C.

ACT Input Load Table

INPUT	UNIT LOAD
D	0.53
$\overline{R}$, $\overline{S}$	0.58
CP	1

NOTE: Unit load is ΔI_{CC} limit specified in DC Electrical Specifications Table, e.g., 2.4mA max at 25°C.

Prerequisite For Switching Function

PARAMETER	SYMBOL	V_{CC} (V)	-40°C TO 85°C		-55°C TO 125°C		UNITS
			MIN	MAX	MIN	MAX	
AC TYPES							
Data to CP Setup Time	t_{SU}	1.5	39	-	44	-	ns
		3.3 (Note 11)	4.3	-	4.9	-	ns
		5 (Note 12)	3.1	-	3.5	-	ns
Hold Time	t_H	1.5	0	-	0	-	ns
		3.3	0	-	0	-	ns
		5	0	-	0	-	ns
Removal Time, $\overline{R}$, $\overline{S}$ to CP	t_{REM}	1.5	30	-	34	-	ns
		3.3	4.1	-	4.7	-	ns
		5	2.4	-	2.7	-	ns
Pulse Width, $\overline{R}$, $\overline{S}$	t_W	1.5	44	-	50	-	ns
		3.3	4.9	-	5.6	-	ns
		5	3.5	-	4	-	ns
Pulse Width, CP	t_W	1.5	49	-	56	-	ns
		3.3	5.5	-	6.3	-	ns
		5	3.9	-	4.5	-	ns
CP Frequency	f_{MAX}	1.5	10	-	9	-	MHz
		3.3	90	-	79	-	MHz
		5	125	-	110	-	MHz
ACT TYPES							
Data to CP Setup Time	t_{SU}	5 (Note 12)	3.5	-	4	-	ns
Hold Time	t_H	5	0	-	0	-	ns
Removal Time, $\overline{R}$, $\overline{S}$ to CP	t_{REM}	5	2.4	-	2.7	-	ns
Pulse Width, $\overline{R}$, $\overline{S}$	t_W	5	4.4	-	5	-	ns
Pulse Width, CP	t_W	5	5	-	5.7	-	ns
CP Frequency	f_{MAX}	5	97	-	85	-	MHz

NOTES:

11. 3.3V Min at 3.6V.
12. 5V Min at 4.5V.

Switching Specifications Input t_r, t_f = 3ns, C_L = 50pF (Worst Case)

PARAMETER	SYMBOL	V_{CC} (V)	-40°C TO 85°C			-55°C TO 125°C			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
AC TYPES									
Propagation Delay, CP to Q, $\overline{Q}$	t_{PLH}, t_{PHL}	1.5	-	-	114	-	-	125	ns
		3.3 (Note 14)	3.6	-	12.7	3.5	-	14	ns
		5 (Note 15)	2.6	-	9.1	2.5	-	10	ns

Switching Specifications Input t_r, t_f = 3ns, C_L = 50pF (Worst Case) **(Continued)**

PARAMETER	SYMBOL	V_{CC} (V)	-40°C TO 85°C			-55°C TO 125°C			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
Propagation Delay, $\overline{R}$, $\overline{S}$ to Q, $\overline{Q}$	t_{PLH}	1.5	-	-	120	-	-	132	ns
		3.3	3.8	-	13.4	3.7	-	14.7	ns
		5	2.7	-	9.5	2.6	-	10.5	ns
	t_{PHL}	1.5	-	-	131	-	-	144	ns
		3.3	4.1	-	14.6	4	-	16.1	ns
		5	3	-	10.4	2.9	-	11.5	ns
Input Capacitance	C_I	-	-	-	10	-	-	10	pF
Power Dissipation Capacitance	C_{PD} (Note 16)	-	-	55	-	-	55	-	pF
ACT TYPES									
Propagation Delay, CP to Q, $\overline{Q}$	t_{PHL} t_{PLH}	5 (Note 15)	2.5	-	8.6	2.4	-	9.5	ns
Propagation Delay, $\overline{R}$, $\overline{S}$ to Q, $\overline{Q}$	t_{PLH}	5	3	-	10.5	2.9	-	11.5	ns
	t_{PHL}	5	3.2	-	11.4	3.1	-	12.5	ns
Input Capacitance	C_I	-	-	-	10	-	-	10	pF
Power Dissipation Capacitance	C_{PD} (Note 16)	-	-	55	-	-	55	-	pF

NOTES:

13. Limits tested 100%.
14. 3.3V Min at 3.6V, Max at 3V.
15. 5V Min at 5.5V, Max at 4.5V.
16. C_{PD} is used to determine the dynamic power consumption per flip-flop.
    $P_D = C_{PD}V_{CC}^2 f_i + \Sigma (C_L V_{CC}^2 f_o) + V_{CC} \Delta I_{CC}$ where f_i = input frequency, f_o = output frequency, C_L = output load capacitance, V_{CC} = supply voltage.

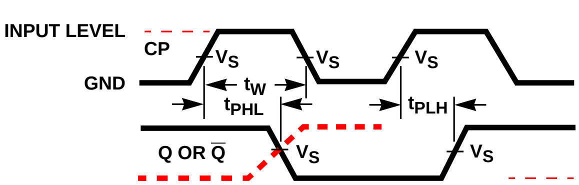


FIGURE 1.

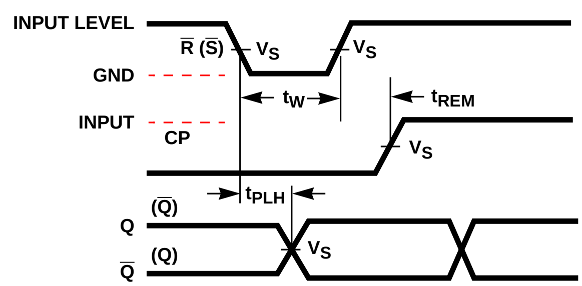


FIGURE 2.

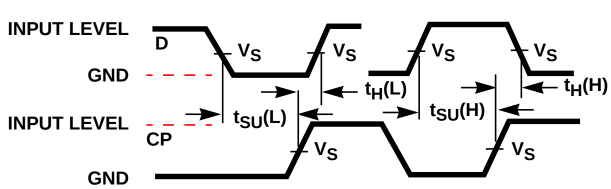
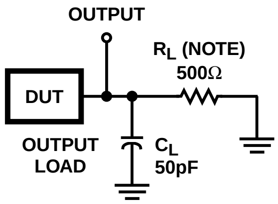


FIGURE 3.



NOTE: For AC Series Only: When V_{CC} = 1.5V, R_L = 1kΩ.

	AC	ACT
Input Level	V_{CC}	3V
Input Switching Voltage, V_S	0.5 V_{CC}	1.5V
Output Switching Voltage, V_S	0.5 V_{CC}	0.5 V_{CC}

FIGURE 4. PROPAGATION DELAY TIMES

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