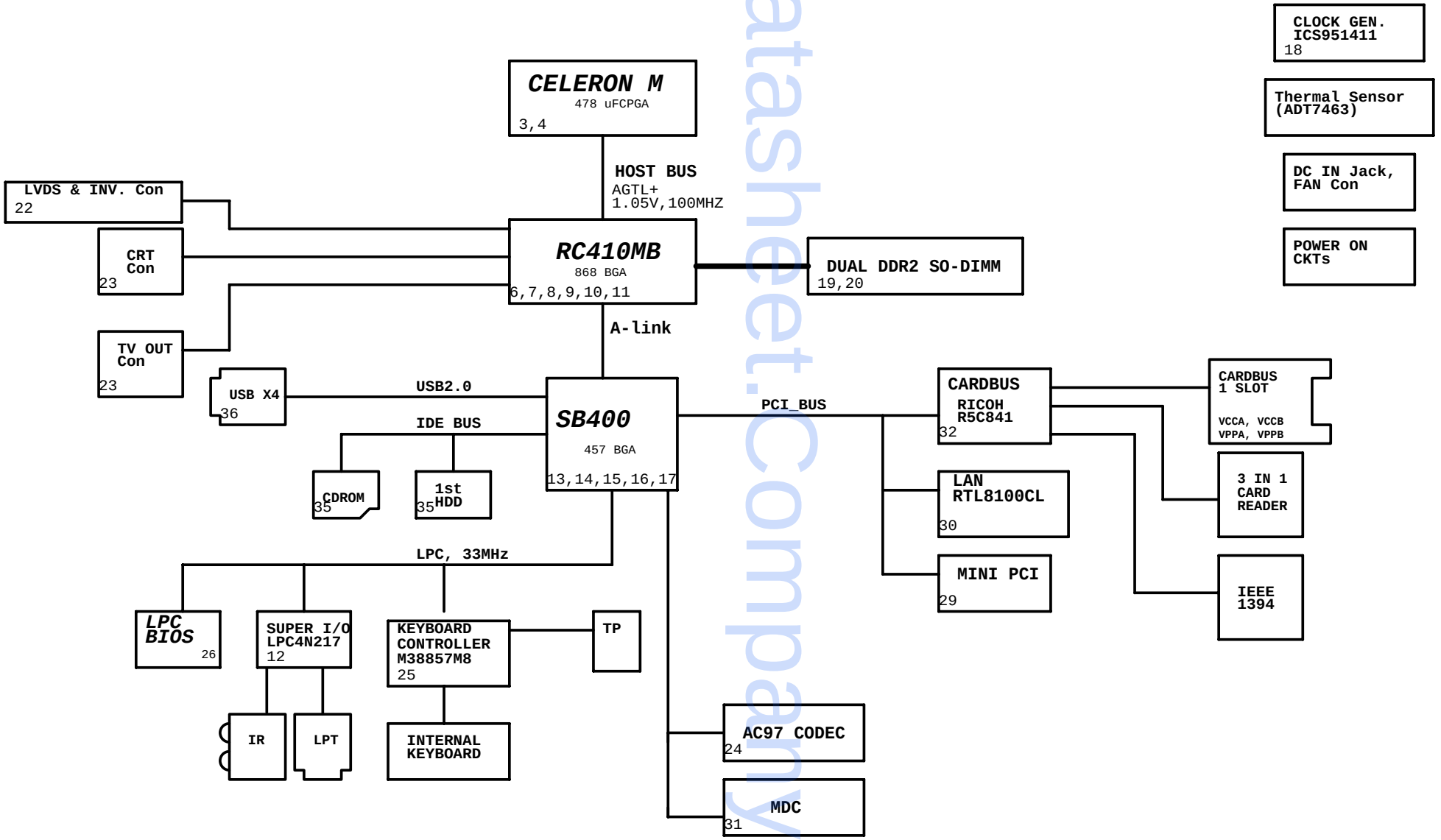
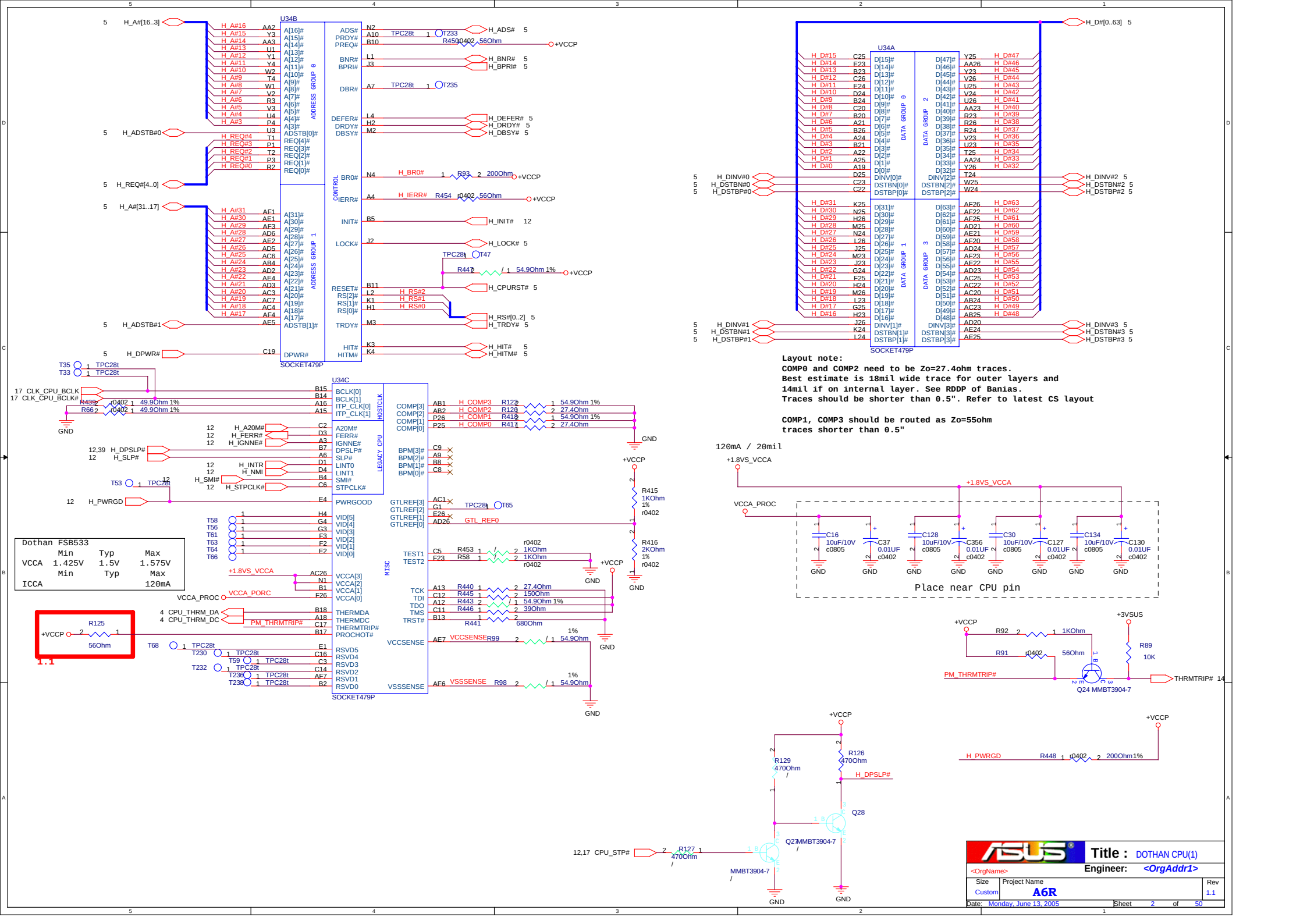
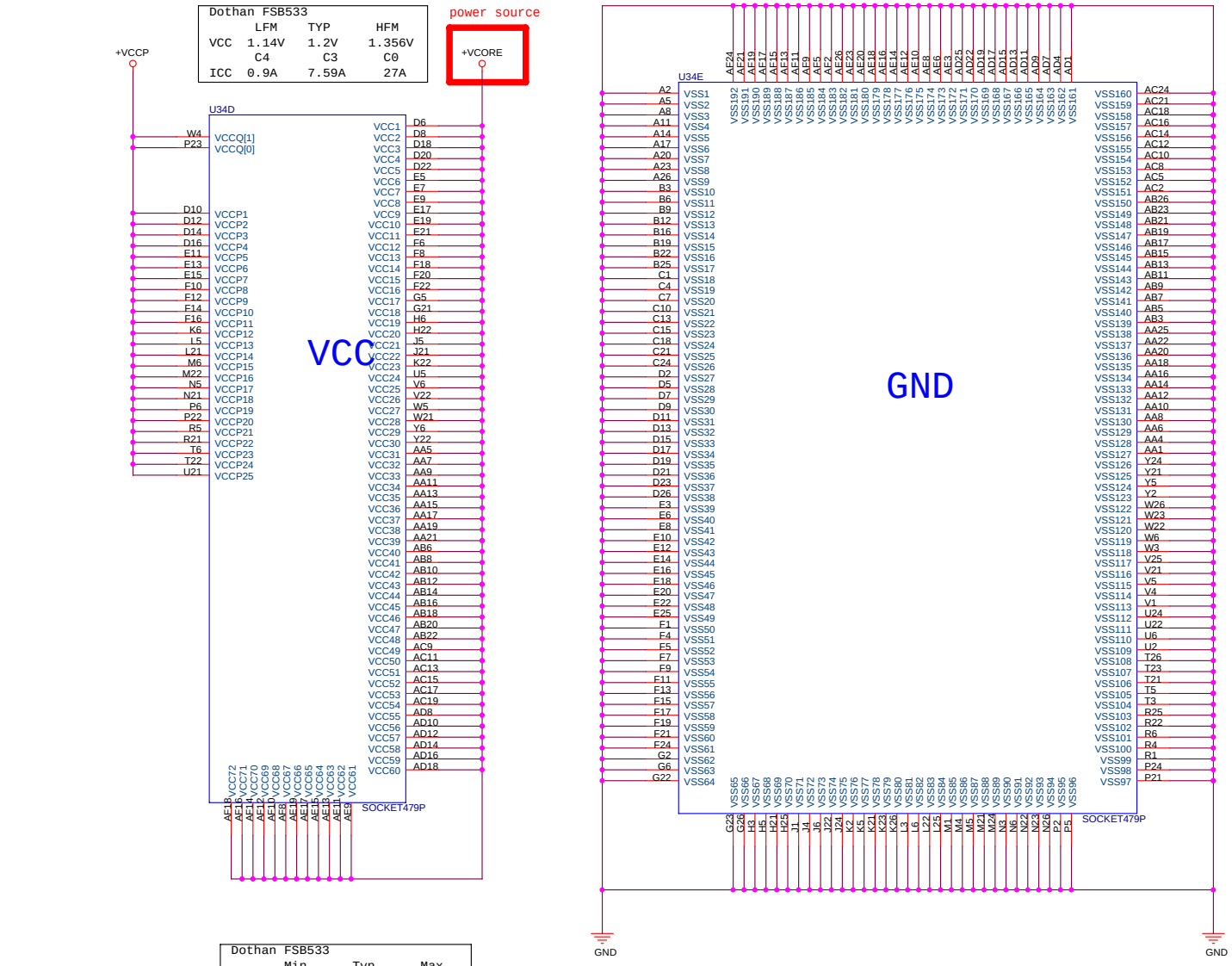
CELERON/RC410MB/IXP400 BLOCK DIAGRAM



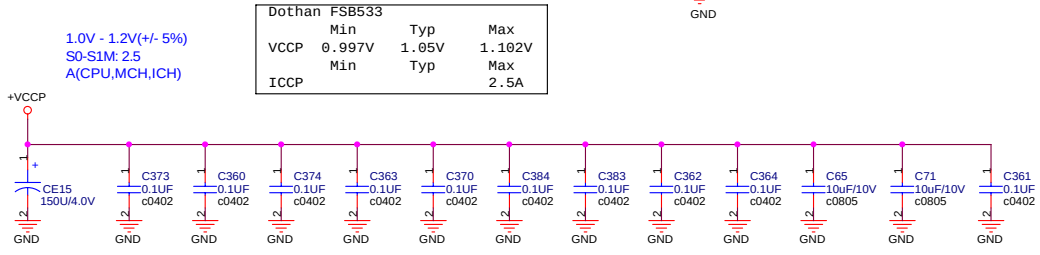
ASUS	Title : BLOCK DIAGRAM	
<OrgName>	Engineer: <OrgAddr1>	
Size: Custom	Project Name: A6R	Rev: 1.1
Date: Monday, June 13, 2005	Sheet 1 of 50	


U34B
SOCKET479P
U34C
SOCKET479P
U34A
SOCKET479P
Layout note:
COMP0 and COMP2 need to be Zo=27.4ohm traces.
Best estimate is 18mil wide trace for outer layers and
14mil if on internal layer. See RDDP of Banias.
Traces should be shorter than 0.5". Refer to latest CS layout
COMP1, COMP3 should be routed as Zo=55ohm
traces shorter than 0.5"
120mA / 20mil
Place near CPU pin
Dothan FSB533
Min Typ Max
VCCA 1.425V 1.5V 1.575V
Min Typ Max
ICCA 120mA
1.1
Q24 MMBT3904-7
Q27 MMBT3904-7
Q28
MMBT3904-7
Title : DOTHAN CPU(1)
Engineer: <OrgAddr1>
<OrgName>
Size Custom
Project Name A6R
Rev 1.1
Date: Monday, June 13, 2005
Sheet 2 of 50



MOBILE DOTHAN VID TABLE

VID[5..0]	Voltage	VID[5..0]	Voltage
000000	1.708V	100000	1.196V
000001	1.692V	100001	1.180V
000010	1.676V	100010	1.164V
000011	1.660V	100011	1.148V
000100	1.644V	100100	1.132V
000101	1.628V	100101	1.116V
000110	1.612V	100110	1.100V
000111	1.596V	100111	1.084V
001000	1.580V	101000	1.068V
001001	1.564V	101001	1.052V
001010	1.548V	101010	1.036V
001011	1.532V	101011	1.020V
001100	1.516V	101100	1.004V
001101	1.500V	101101	0.988V
001110	1.484V	101110	0.972V
001111	1.468V	101111	0.956V
010000	1.452V	110000	0.940V
010001	1.436V	110001	0.924V
010010	1.420V	110010	0.908V
010011	1.404V	110011	0.892V
010100	1.388V	110100	0.876V
010101	1.372V	110101	0.860V
010110	1.356V	110110	0.844V
010111	1.340V	110111	0.828V
011000	1.324V	111000	0.812V
011001	1.308V	111001	0.796V
011010	1.292V	111010	0.780V
011011	1.276V	111011	0.764V
011100	1.260V	111100	0.748V
011101	1.244V	111101	0.732V
011110	1.228V	111110	0.716V
011111	1.212V	111111	0.700V

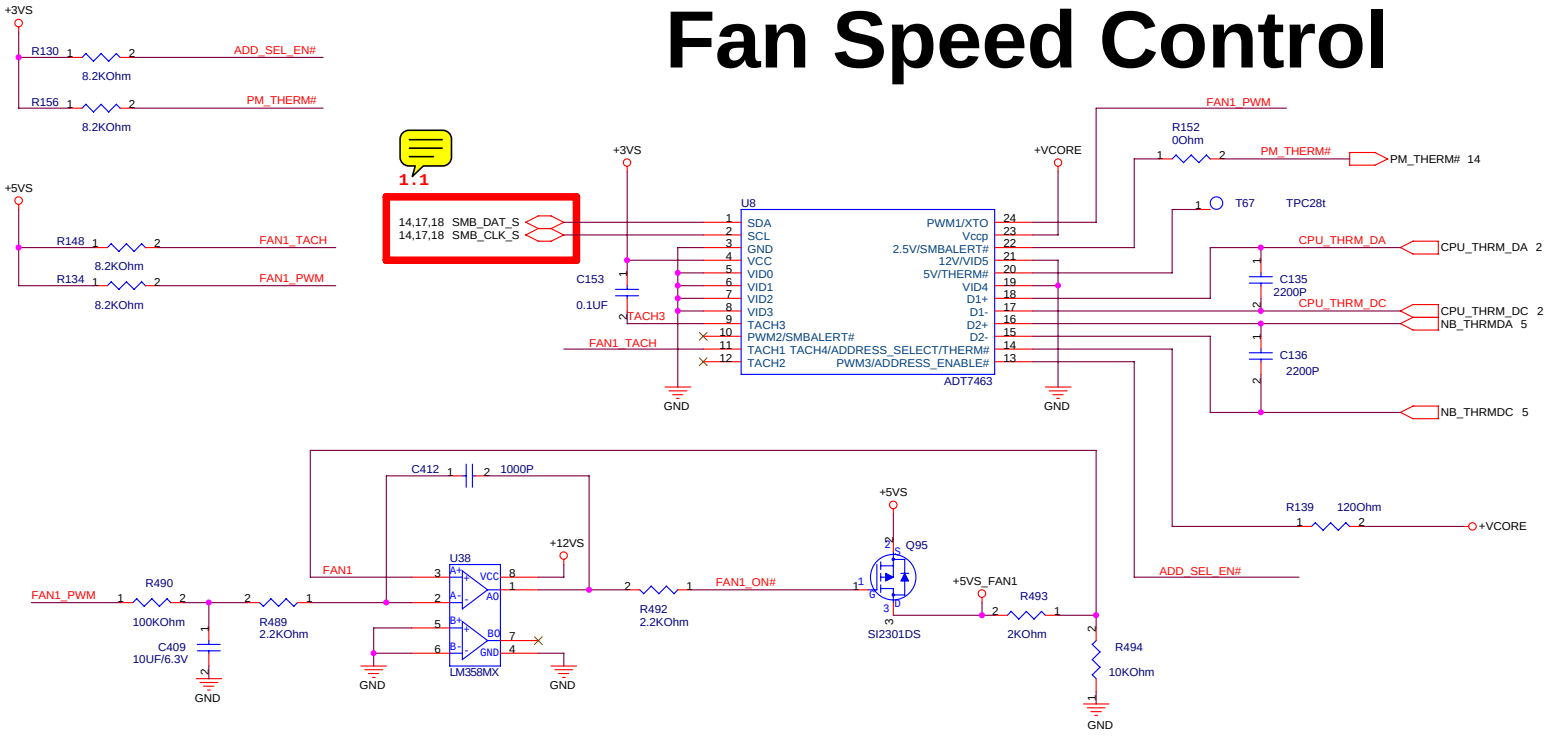


+VCCP (CPU) Decoupling Capacitor
(Place near CPU)

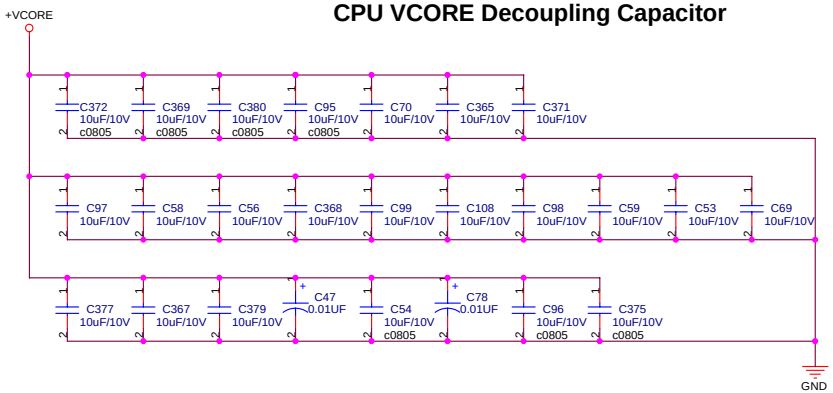
ASUS	Title : DOTHAN CPU(2)	
<OrgName>	Engineer: <OrgAddr1>	
Size: Custom	Project Name: A6R	Rev: 1.1
Date: Monday, June 13, 2005	Sheet 3 of 50	

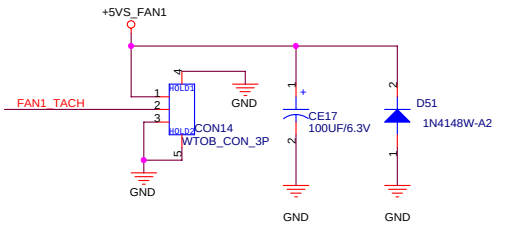
Fan Speed Control

Pin 13	Pin 14	SMB Addr
1	X	5C **
0	1	5A
0	0	58

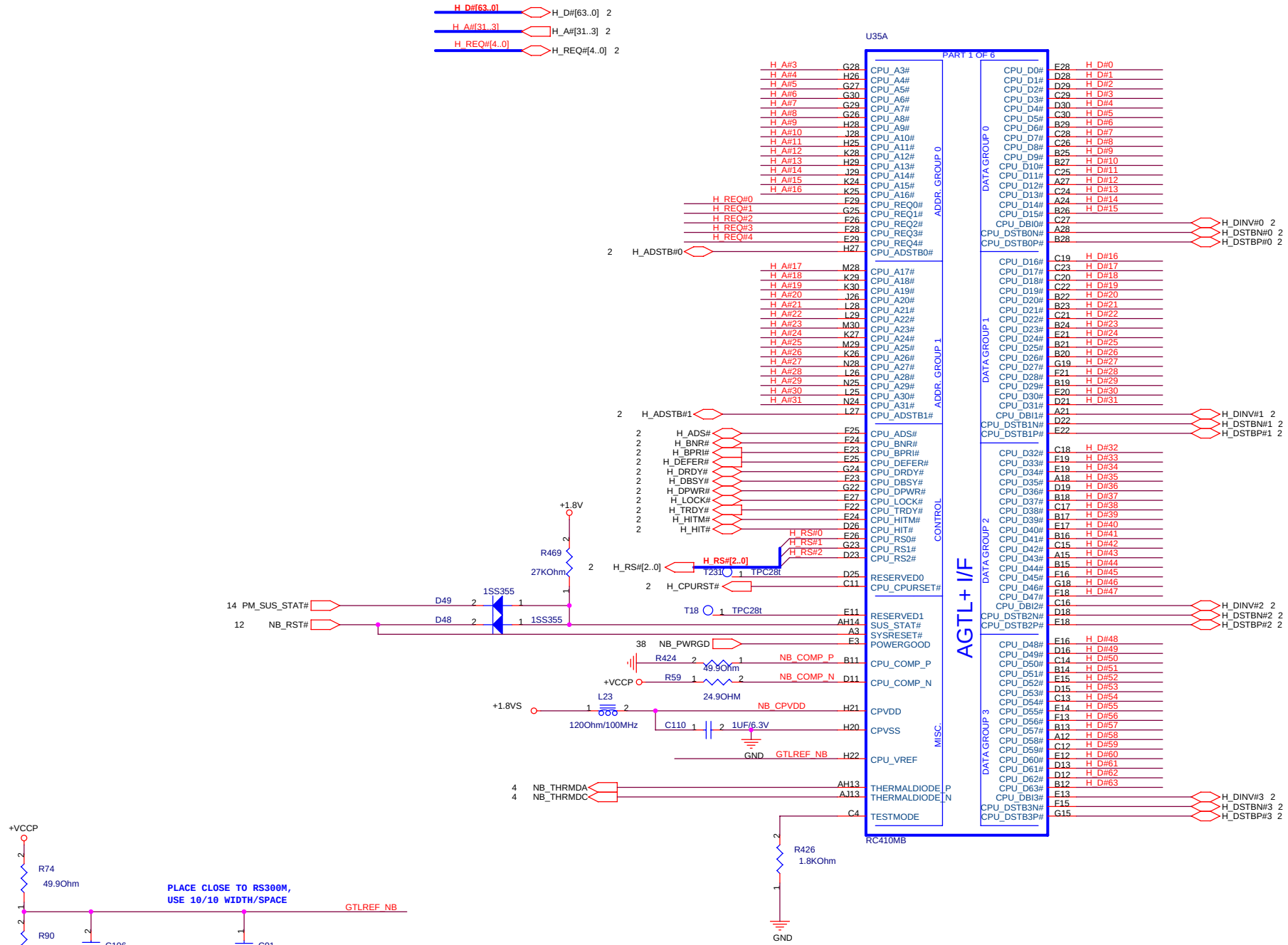


CPU VCORE Decoupling Capacitor

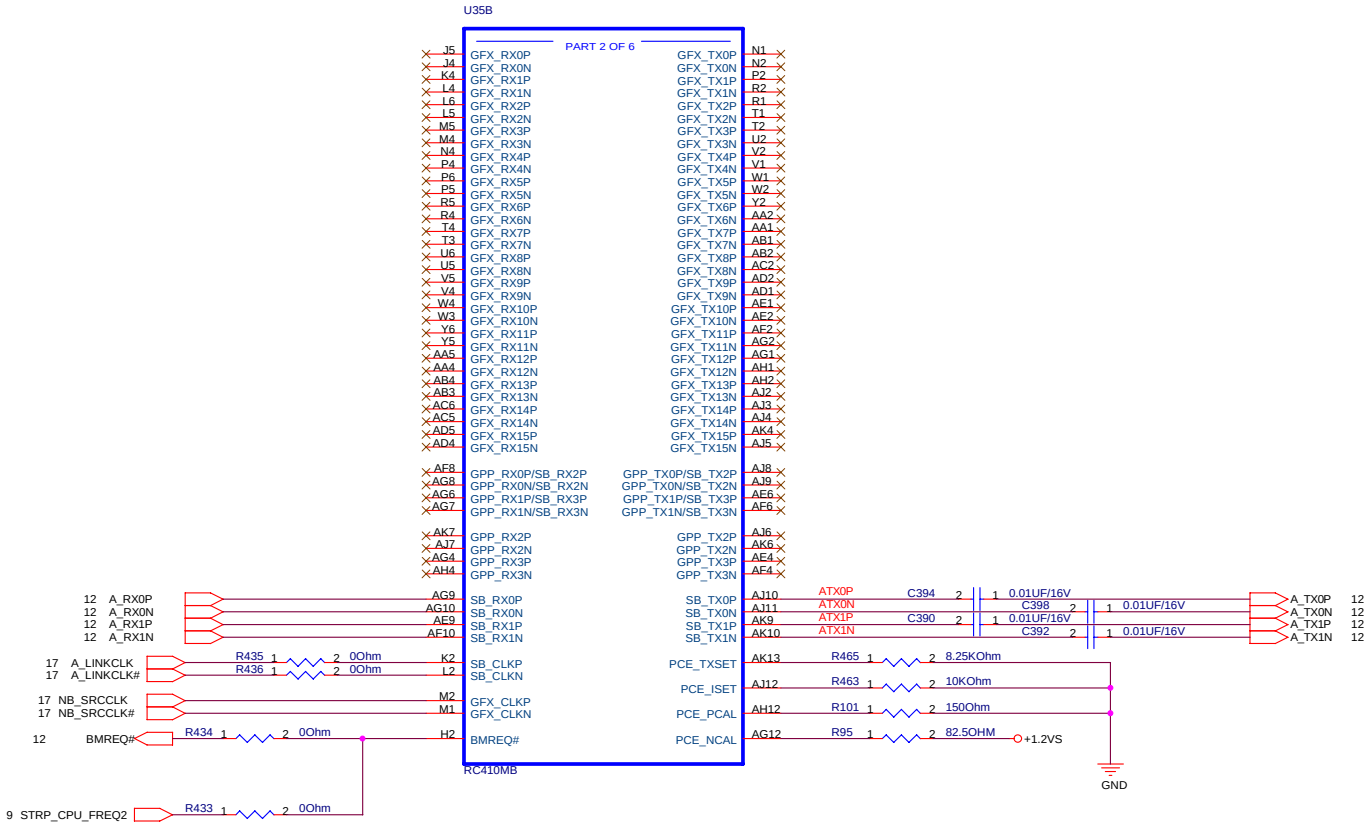




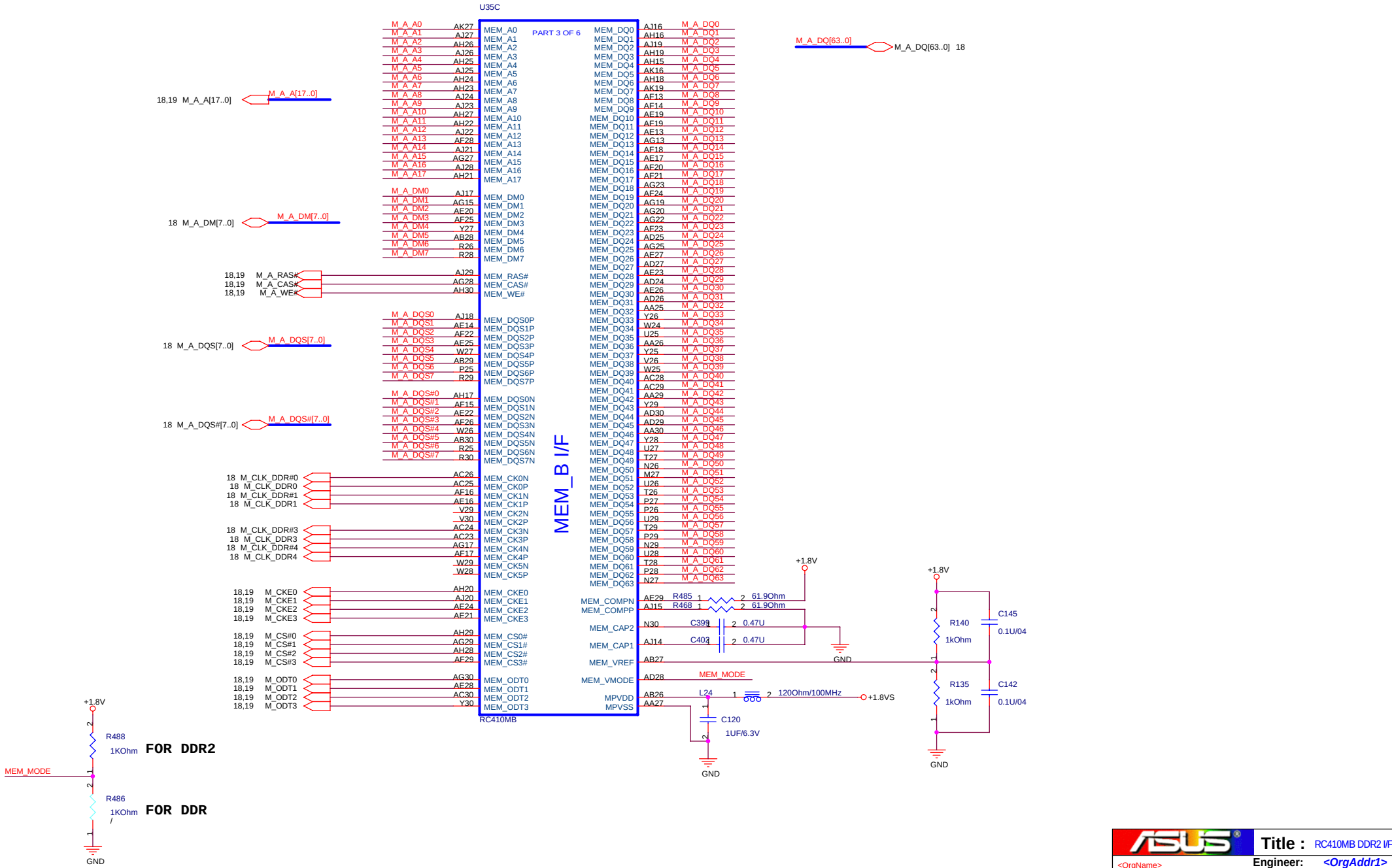
ASUS	Title : THERMAL SERSOR,FAN		
<OrgName>	Engineer: <OrgAddr1>		
Size: Custom	Project Name: A6R		Rev: 1.1
Date: Monday, June 13, 2005	Sheet 4 of 50		



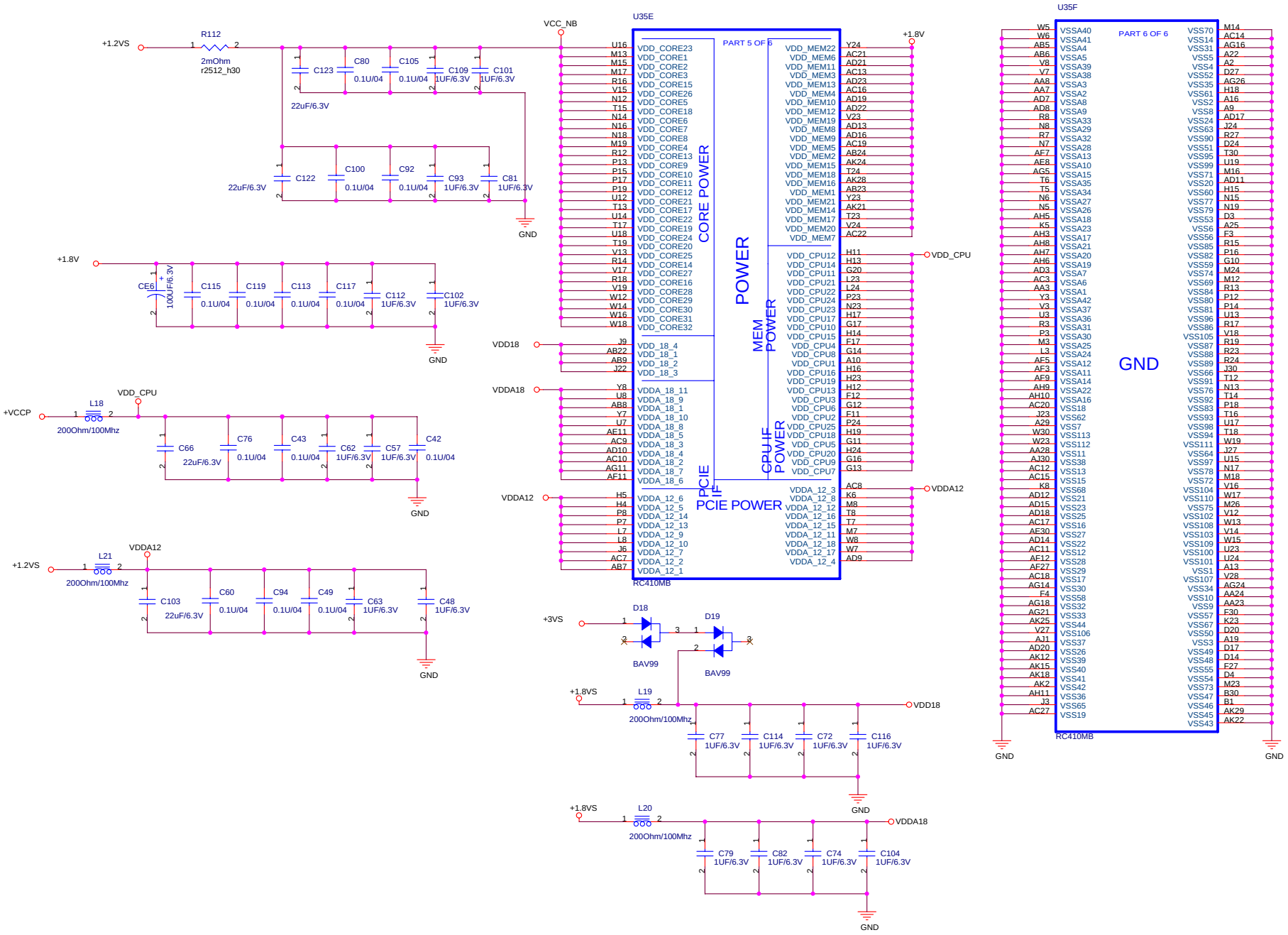
Title :	RC410MB AGTL I/F(1)
<OrgName>	Engineer: <OrgAddr1>
Size: Custom	Project Name: A6R
Rev: 1.1	
Date: Monday, June 13, 2005	Sheet 5 of 50



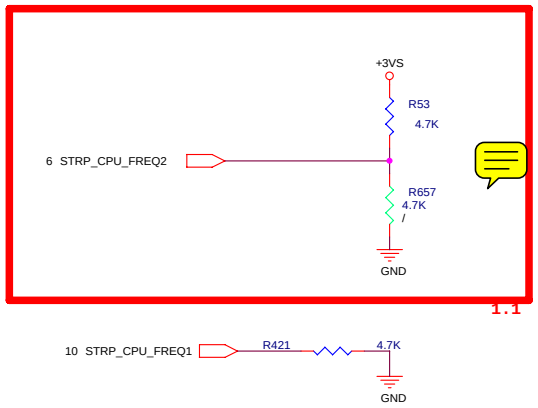
ASUS	Title : RC410MB PCIE & A-Link(2)	
<OrgName>	Engineer: <OrgAddr1>	
Size: Custom	Project Name: A6R	Rev: 1.1
Date: Monday, June 13, 2005	Sheet 6 of 50	



ASUS	Title : RC410MB DDR2 I/F (3)		
<OrgName>	Engineer: <OrgAddr1>		
Size: Custom	Project Name: A6R		Rev: 1.1
Date: Monday, June 13, 2005	Sheet 7 of 50		



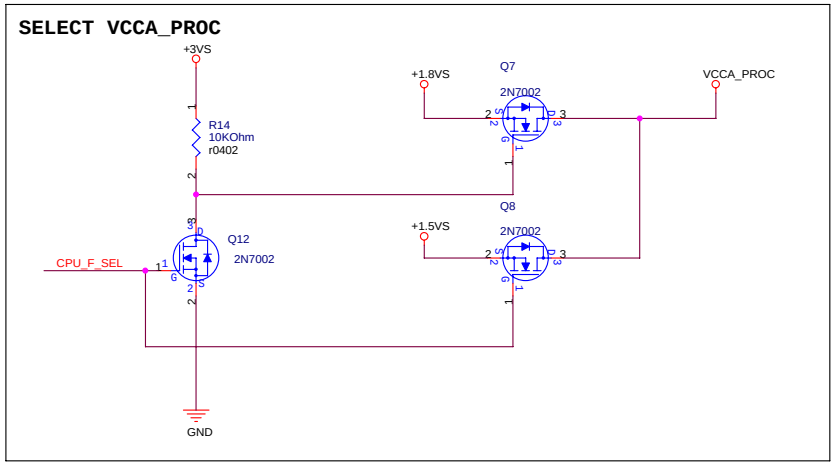
ASUS	Title : RC410MB POWER (4)		
<OrgName>	Engineer: <OrgAddr1>		
Size: Custom	Project Name: A6R		Rev: 1.1
Date: Monday, June 13, 2005	Sheet 8 of 50		

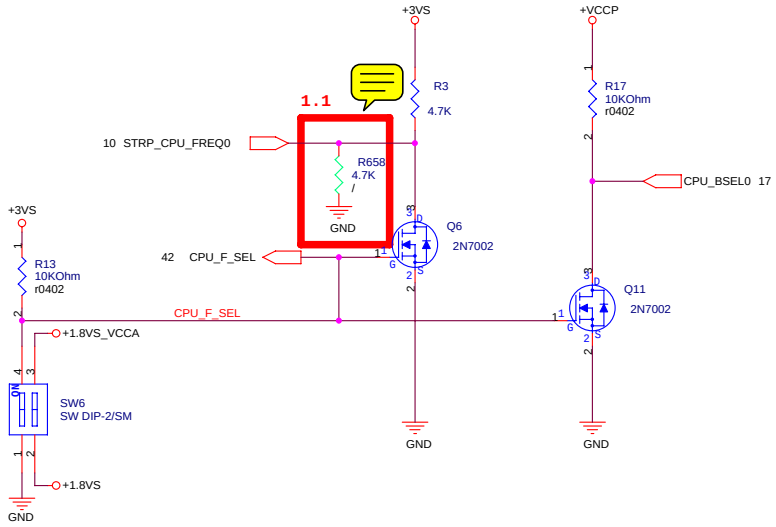


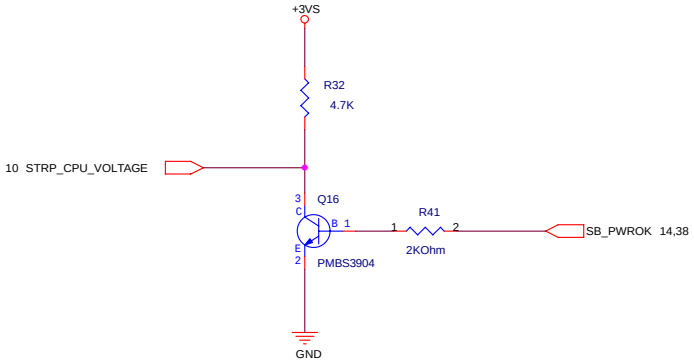
FSB	STRP_CPU_FREQ2	STRP_CPU_FREQ1	STRP_CPU_FREQ0
100MHZ	1	0	1
133MHZ	1	0	0
133MHZ	1	1	0
133MHZ	1	1	1
100MHZ	0	0	0
133MHZ	0	0	1
133MHZ	0	1	0
133MHZ	0	1	1

DEFAULT: 101

Note1: For A11, 100M and 133M need to strap at 101or 001 .
Note2: A12 changed 101 to be 100MHZ instead of 133MHZ in A11 ASIC.





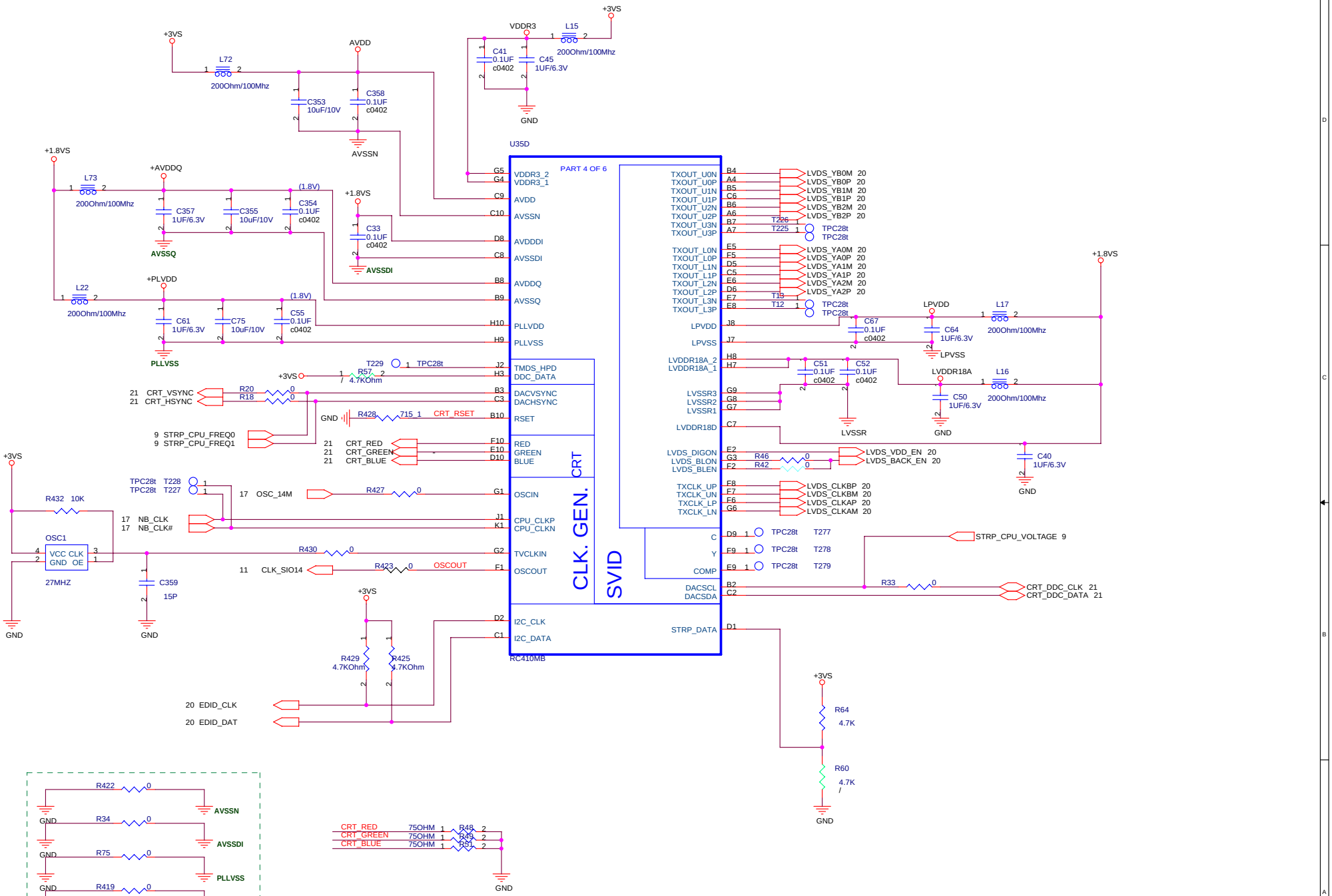


CELERON M
100

SW8
ON: CPU_F_SEL=0 FSB100MHz VCCA_PROC=1.8V
OFF: CPU_F_SEL=1 FSB133MHz VCCA_PROC=1.5V

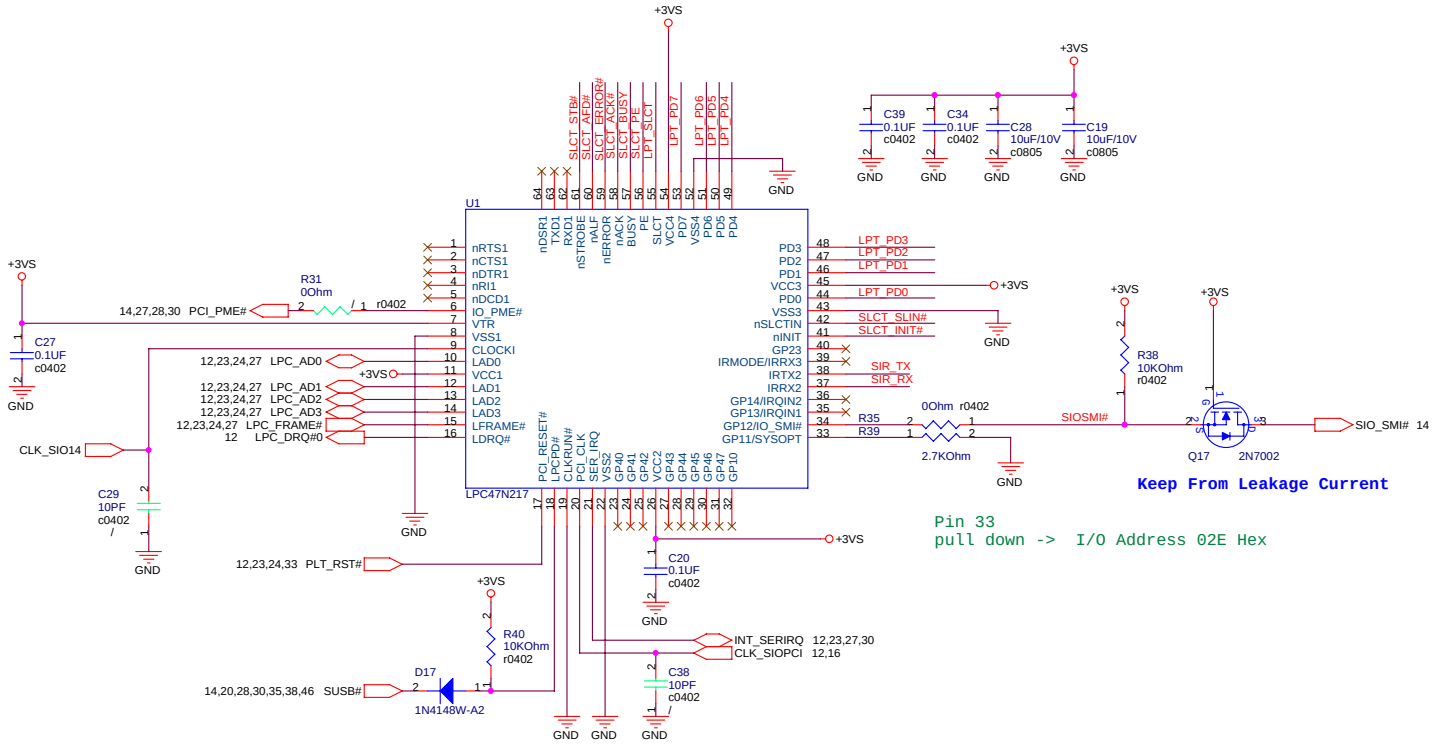
STRP_CPU_VOLTAGE: CPU VCC
0: MOBILE CPU
1: DESKTOP CPU
DEFAULT:0

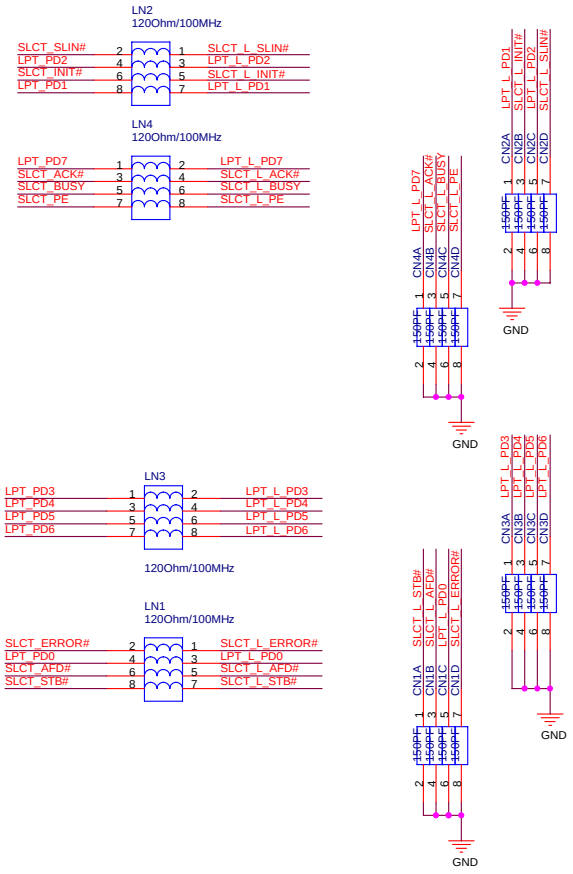
ASUS	Title : FSB SELECTION	
<OrgName>	Engineer: <OrgAddr1>	
Size: Custom	Project Name: A6R	Rev: 1.1
Date: Monday, June 13, 2005	Sheet 9 of 50	



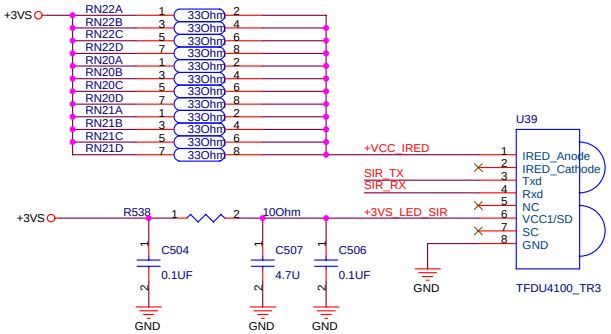
ASUS	Title : RC410MB VIDEO I/F (6)		
<OrgName>	Engineer: <OrgAddr1>		
Size: Custom	Project Name: A6R		Rev: 1.1
Date: Monday, June 13, 2005	Sheet 10 of 50		

Super I/O

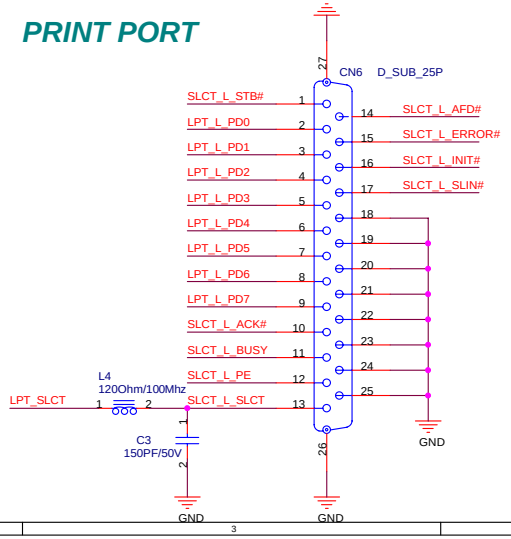


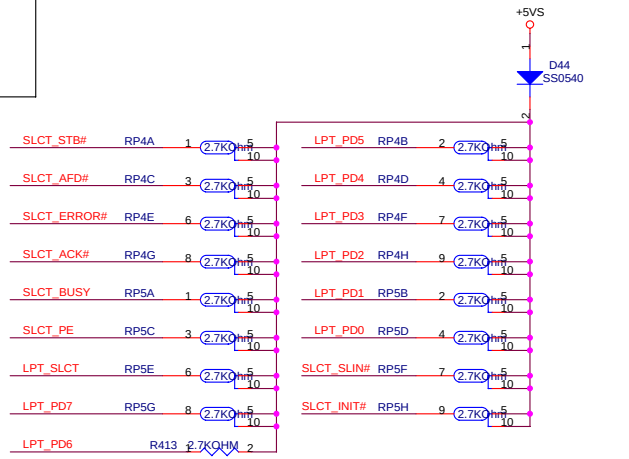


SIR



PRINT PORT



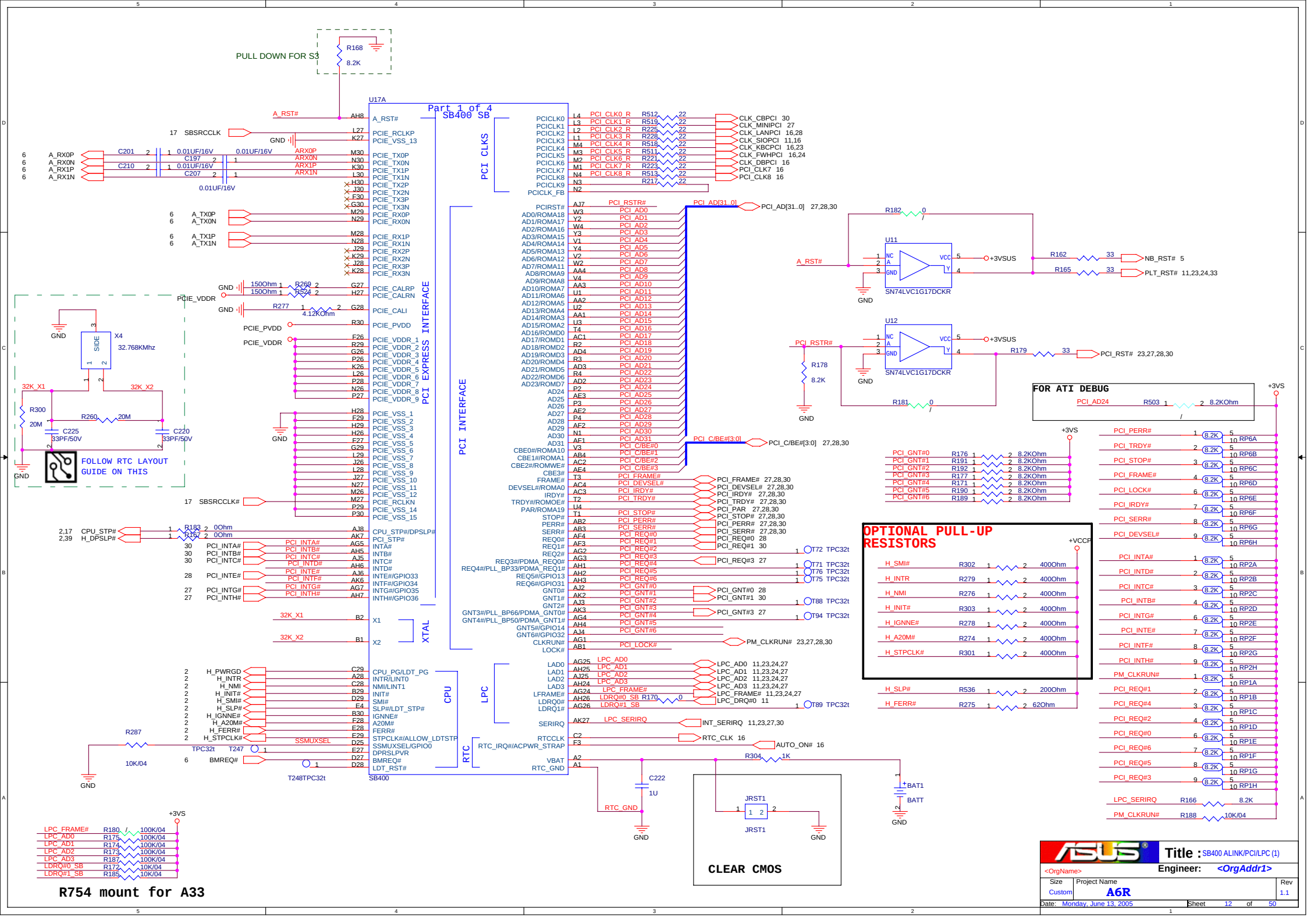


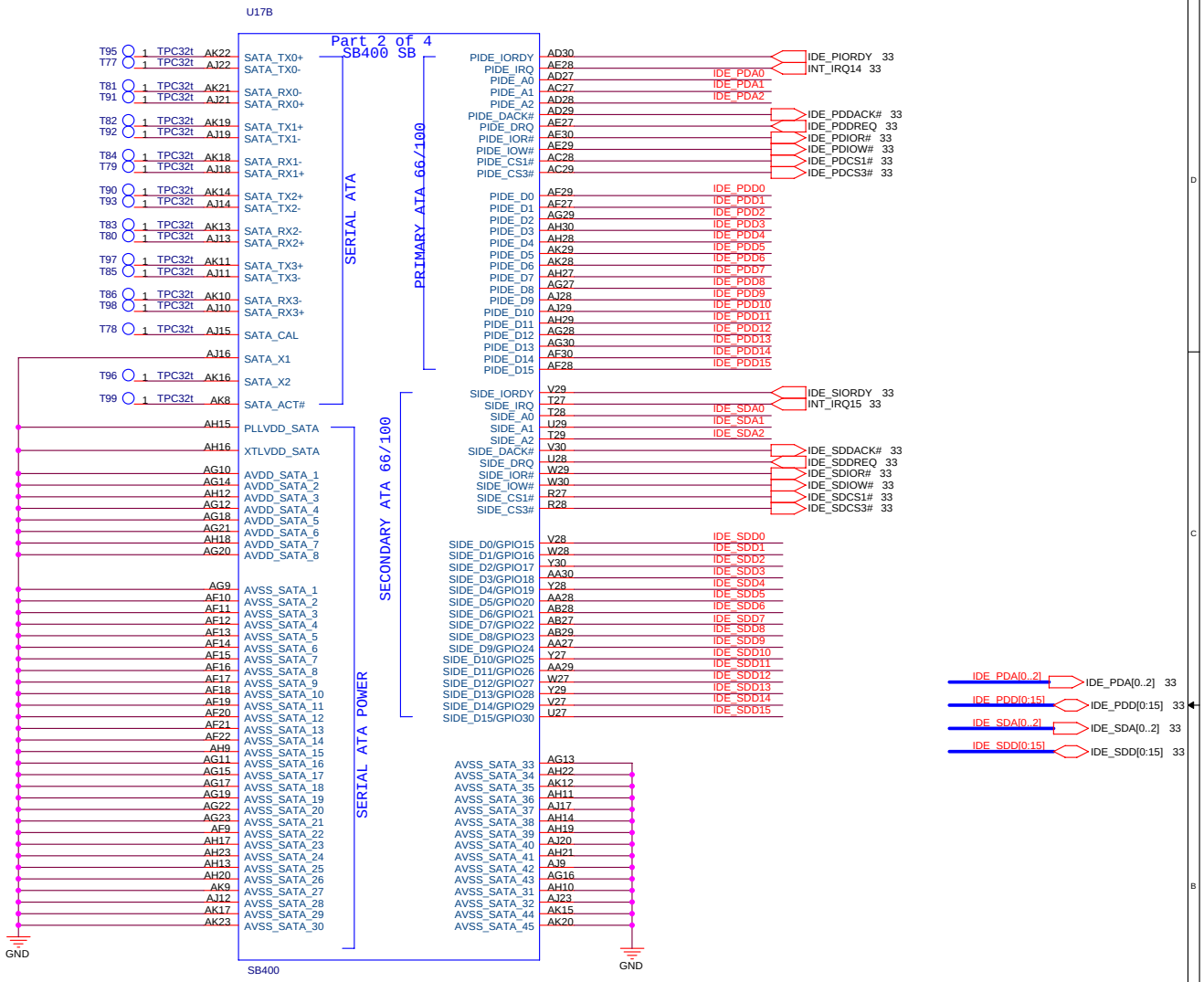
Title : SIO & SIR & PRINTER PORT

<OrgName> Engineer: <OrgAddr1>

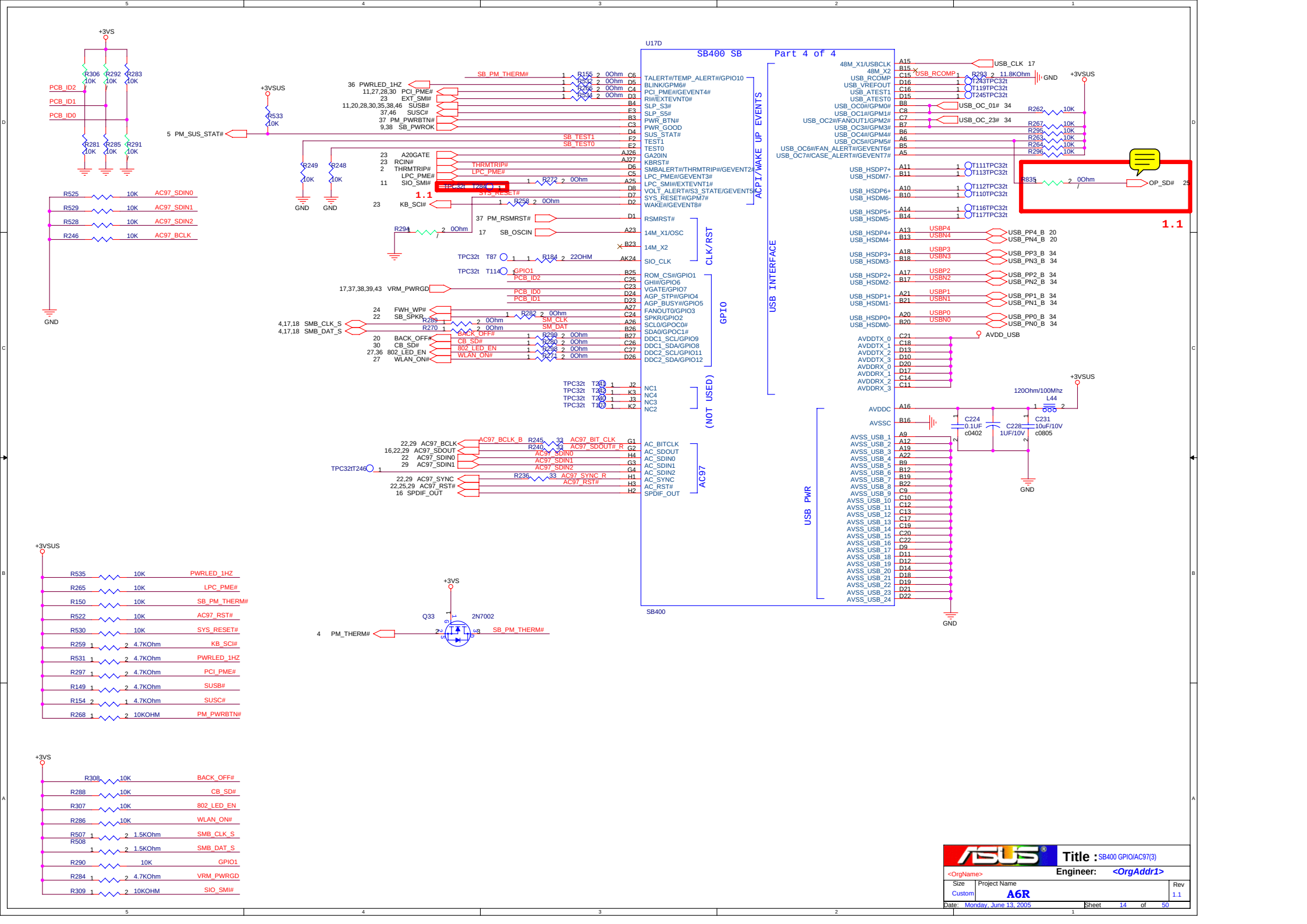
Size	Project Name	Rev
Custom	A6R	1.1

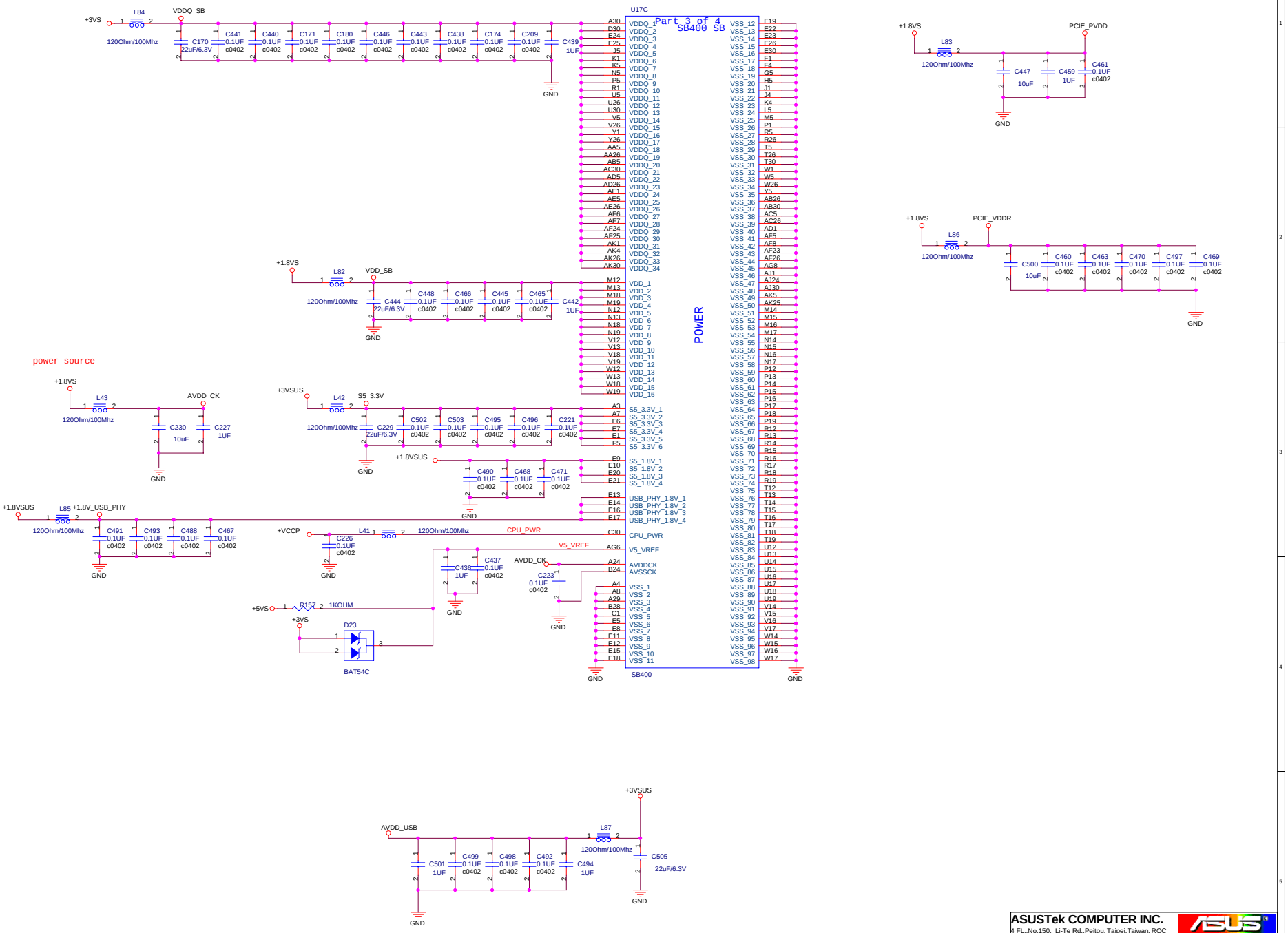
Date: Monday, June 13, 2005 Sheet 11 of 50


PULL DOWN FOR S3
R168
8.2K
U17A
Part 1 of 4
SB400 SB
A_RST#
SBSRCCLK
A_RX0P
A_RX0N
A_RX1P
A_RX1N
A_TX0P
A_TX0N
A_TX1P
A_TX1N
0.01UF/16V
PCIE_VDDR
PCIE_PVDD
150Ohm
4.12KOhm
PCIE_CALRP
PCIE_CALRN
PCIE_CALI
PCIE_VDDR_1
PCIE_VDDR_2
PCIE_VDDR_3
PCIE_VDDR_4
PCIE_VDDR_5
PCIE_VDDR_6
PCIE_VDDR_7
PCIE_VDDR_8
PCIE_VDDR_9
PCIE_VSS_1
PCIE_VSS_2
PCIE_VSS_3
PCIE_VSS_4
PCIE_VSS_5
PCIE_VSS_6
PCIE_VSS_7
PCIE_VSS_8
PCIE_VSS_9
PCIE_VSS_10
PCIE_VSS_11
PCIE_VSS_12
PCIE_RCLKN
PCIE_VSS_14
PCIE_VSS_15
PCIE EXPRESS INTERFACE
X4
32.768KMhz
SIDE
32K_X1
32K_X2
R300
20M
R260
C225
C220
33PF/50V
FOLLOW RTC LAYOUT
GUIDE ON THIS
CPU_STP#
H_DPSLP#
CPU_STP#/DPSLP#
PCI_STP#
PCI_INTA#
PCI_INTB#
PCI_INTC#
PCI_INTD#
PCI_INTE#
PCI_INTF#
PCI_INTG#
PCI_INTH#
INTA#
INTB#
INTC#
INTD#
INTE#/GPIO33
INTF#/GPIO34
INTG#/GPIO35
INTH#/GPIO36
XTAL
CPU
H_PWRGD
H_INTR
H_NMI
H_INIT#
H_SMI#
H_SLP#
H_IGNNE#
H_A20M#
H_FERR#
H_STPCLK#
SSMUXSEL
BMREQ#
R287
10K/04
T247
T248TPC32t
SB400
PCI INTERFACE
PCI CLKS
PCICLK0
PCICLK1
PCICLK2
PCICLK3
PCICLK4
PCICLK5
PCICLK6
PCICLK7
PCICLK8
PCICLK9
PCICLK_FB
PCI_CLK0_R
PCI_CLK1_R
PCI_CLK2_R
PCI_CLK3_R
PCI_CLK4_R
PCI_CLK5_R
PCI_CLK6_R
PCI_CLK7_R
PCI_CLK8_R
CLK_CBPCI 30
CLK_MINIPCI 27
CLK_LANPCI 16,28
CLK_SIOPCI 11,16
CLK_KBCPCI 16,23
CLK_FWHPCI 16,24
CLK_DBPCI 16
PCI_CLK7 16
PCI_CLK8 16
PCIRST#
PCI_RSTR#
PCI_AD[31..0]
PCI_C/BE#[3:0]
PCI_FRAME#
PCI_DEVSEL#
PCI_IRDY#
PCI_TRDY#
PCI_STOP#
PCI_PAR
PCI_PERR#
PCI_SERR#
PCI_REQ#0
PCI_REQ#1
PCI_REQ#2
PCI_REQ#3
PCI_REQ#4
PCI_REQ#5
PCI_REQ#6
PCI_GNT#0
PCI_GNT#1
PCI_GNT#2
PCI_GNT#3
PCI_GNT#4
PCI_GNT#5
PCI_GNT#6
PCI_LOCK#
PM_CLKRUN# 23,27,28,30
LPC
LAD0
LAD1
LAD2
LAD3
LFRAME#
LDRQ0#
LDRQ1#
SERIRQ
LPC_AD0
LPC_AD1
LPC_AD2
LPC_AD3
LPC_FRAME#
LDRQ#0_SB
LDRQ#1_SB
INT_SERIRQ 11,23,27,30
RTC
RTCCLK
RTC_IRQ#/ACPWR_STRAP
VBAT
RTC_GND
RTC_CLK 16
AUTO_ON# 16
C222
1U
R304
1K
BAT1
BATT
JRST1
CLEAR CMOS
U11
U12
SN74LVC1G17DCKR
+3VSUS
NB_RST# 5
PLT_RST# 11,23,24,33
PCI_RST# 23,27,28,30
R178
8.2K
FOR ATI DEBUG
PCI_AD24
R503
8.2KOhm
OPTIONAL PULL-UP
RESISTORS
+VCCP
H_SMI#
H_INTR
H_NMI
H_INIT#
H_IGNNE#
H_A20M#
H_STPCLK#
400Ohm
H_SLP#
H_FERR#
200Ohm
62Ohm
8.2KOhm
RP6A
RP6B
RP6C
RP6D
RP6E
RP6F
RP6G
RP6H
RP2A
RP2B
RP2C
RP2D
RP2E
RP2F
RP2G
RP2H
RP1A
RP1B
RP1C
RP1D
RP1E
RP1F
RP1G
RP1H
LPC_FRAME#
LPC_AD0
LPC_AD1
LPC_AD2
LPC_AD3
LDRQ#0_SB
LDRQ#1_SB
100K/04
10K/04
R754 mount for A33
Title : SB400 ALINK/PCI/LPC (1)
Engineer: <OrgAddr1>
<OrgName>
Project Name
A6R
Size
Custom
Rev
1.1
Date: Monday, June 13, 2005
Sheet 12 of 50



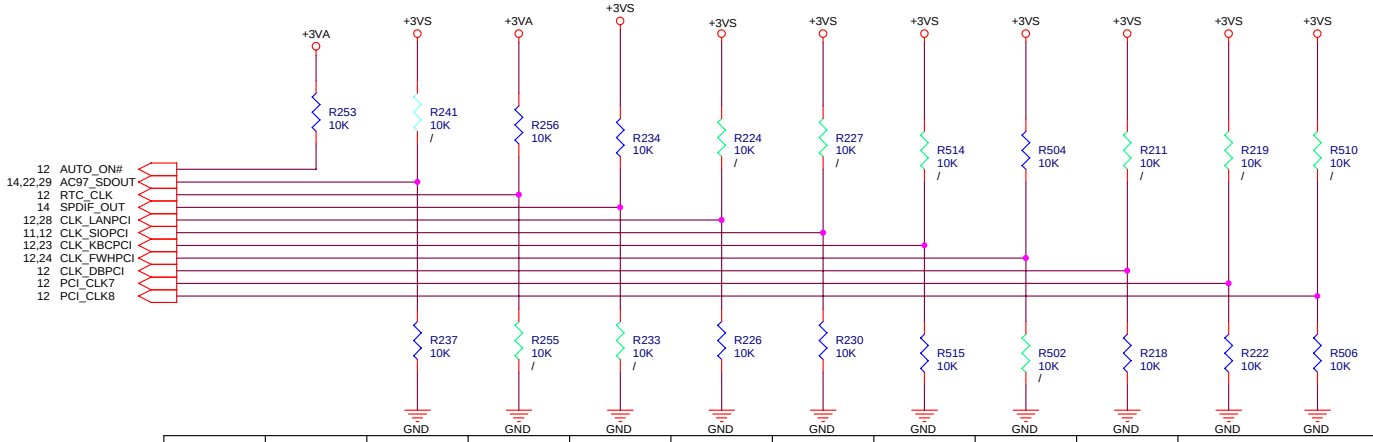
<OrgName>	Title : SB400 IDE/USB/MII (2)	
	Engineer: <OrgAddr1>	
Size: Custom	Project Name: A6R	Rev: 1.1
Date: Monday, June 13, 2005	Sheet 13 of 50	


U17D
SB400 SB
Part 4 of 4
SB400
ACPI/WAKE UP EVENTS
USB INTERFACE
CLK/RST
GPIO
(NOT USED)
AC97
USB PWR
TALERT#/TEMP_ALERT#/GPIO10
BLINK/GPM6#
PCI_PME#/GEVENT4#
RI#/EXTEVNT0#
SLP_S3#
SLP_S5#
PWR_BTN#
PWR_GOOD
SUS_STAT#
TEST1
TEST0
GA20IN
KBRST#
SMBALERT#/THRMTRIP#/GEVENT2#
LPC_PME#/GEVENT3#
LPC_SMI#/EXTEVNT1#
VOLT_ALERT#/S3_STATE/GEVENT5#
SYS_RESET#/GPM7#
WAKE#/GEVENT8#
RSMRST#
14M_X1/OSC
14M_X2
SIO_CLK
ROM_CS#/GPIO1
GHI#/GPIO6
VGATE/GPIO7
AGP_STP#/GPIO4
AGP_BUSY#/GPIO5
FANOUT0/GPIO3
SPKR/GPIO2
SCL0/GPOC0#
SDA0/GPOC1#
DDC1_SCL/GPIO9
DDC1_SDA/GPIO8
DDC2_SCL/GPIO11
DDC2_SDA/GPIO12
NC1
NC4
NC3
NC2
AC_BITCLK
AC_SDOUT
AC_SDIN0
AC_SDIN1
AC_SDIN2
AC_SYNC
AC_RST#
SPDIF_OUT
48M_X1/USBCLK
48M_X2
USB_RCOMP
USB_VREFOUT
USB_ATEST1
USB_ATEST0
USB_OC0#/GPM0#
USB_OC1#/GPM1#
USB_OC2#/FANOUT1/GPM2#
USB_OC3#/GPM3#
USB_OC4#/GPM4#
USB_OC5#/GPM5#
USB_OC6#/FAN_ALERT#/GEVENT6#
USB_OC7#/CASE_ALERT#/GEVENT7#
USB_HSDP7+
USB_HSDM7-
USB_HSDP6+
USB_HSDM6-
USB_HSDP5+
USB_HSDM5-
USB_HSDP4+
USB_HSDM4-
USB_HSDP3+
USB_HSDM3-
USB_HSDP2+
USB_HSDM2-
USB_HSDP1+
USB_HSDM1-
USB_HSDP0+
USB_HSDM0-
AVDDTX_0
AVDDTX_1
AVDDTX_2
AVDDTX_3
AVDDRX_0
AVDDRX_1
AVDDRX_2
AVDDRX_3
AVDDC
AVSSC
AVSS_USB_1
AVSS_USB_2
AVSS_USB_3
AVSS_USB_4
AVSS_USB_5
AVSS_USB_6
AVSS_USB_7
AVSS_USB_8
AVSS_USB_9
AVSS_USB_10
AVSS_USB_11
AVSS_USB_12
AVSS_USB_13
AVSS_USB_14
AVSS_USB_15
AVSS_USB_16
AVSS_USB_17
AVSS_USB_18
AVSS_USB_19
AVSS_USB_20
AVSS_USB_21
AVSS_USB_22
AVSS_USB_23
AVSS_USB_24
+3VS
+3VSUS
GND
PCB_ID2
PCB_ID1
PCB_ID0
R306 10K
R292 10K
R283 10K
R281 10K
R285 10K
R291 10K
R533 10K
5 PM_SUS_STAT#
SB_TEST1
SB_TEST0
R249 10K
R248 10K
SB_PM_THERM#
36 PWRLED_1HZ
11,27,28,30 PCI_PME#
23 EXT_SMI#
11,20,28,30,35,38,46 SUSB#
37,46 SUSC#
37 PM_PWRBTN#
9,38 SB_PWROK
R155 0Ohm
R252 0Ohm
R266 0Ohm
R534 0Ohm
23 A20GATE
23 RCIN#
2 THRMTRIP#
LPC_PME#
11 SIO_SMI#
THRMTRIP#
LPC_PME#
R272 0Ohm
SYS_RESET#
1.1
23 KB_SCI#
R258 0Ohm
37 PM_RSMRST#
R294 0Ohm
17 SB_OSCIN
TPC32t T87
R184 22OHM
TPC32t T114
GPIO1
PCB_ID2
17,37,38,39,43 VRM_PWRGD
PCB_ID0
PCB_ID1
24 FWH_WP#
22 SB_SPKR
R282 0Ohm
4,17,18 SMB_CLK_S
4,17,18 SMB_DAT_S
R289 0Ohm
R270 0Ohm
SM_CLK
SM_DAT
20 BACK_OFF#
30 CB_SD#
27,36 802_LED_EN
27 WLAN_ON#
R299 0Ohm
R260 0Ohm
R298 0Ohm
R271 0Ohm
TPC32t T245
TPC32t T246
TPC32t T247
TPC32t T107
22,29 AC97_BCLK
16,22,29 AC97_SDOUT
22 AC97_SDIN0
29 AC97_SDIN1
TPC32tT246
22,29 AC97_SYNC
22,25,29 AC97_RST#
16 SPDIF_OUT
AC97_BCLK_B
R245 33
R240 33
AC97_BIT_CLK
AC97_SDOUT#_R
AC97_SDIN0
AC97_SDIN1
AC97_SDIN2
R236 33
AC97_SYNC_R
AC97_RST#
Q33
2N7002
4 PM_THERM#
SB_PM_THERM#
USB_CLK 17
R293 11.8KOhm
T243TPC32t
T119TPC32t
T245TPC32t
USB_OC_01# 34
USB_OC_23# 34
R262 10K
R267 10K
R295 10K
R263 10K
R264 10K
R296 10K
T111TPC32t
T113TPC32t
T112TPC32t
T110TPC32t
T116TPC32t
T117TPC32t
R835 0Ohm
OP_SD# 25
1.1
USBP4
USBN4
USB_PP4_B 20
USB_PN4_B 20
USBP3
USBN3
USB_PP3_B 34
USB_PN3_B 34
USBP2
USBN2
USB_PP2_B 34
USB_PN2_B 34
USBP1
USBN1
USB_PP1_B 34
USB_PN1_B 34
USBP0
USBN0
USB_PP0_B 34
USB_PN0_B 34
AVDD_USB
120Ohm/100Mhz
L44
C224 0.1UF c0402
C228 1UF/10V
C231 10uF/10V c0805
R525 10K AC97_SDIN0
R529 10K AC97_SDIN1
R528 10K AC97_SDIN2
R246 10K AC97_BCLK
R535 10K PWRLED_1HZ
R265 10K LPC_PME#
R150 10K SB_PM_THERM#
R522 10K AC97_RST#
R530 10K SYS_RESET#
R259 4.7KOhm KB_SCI#
R531 4.7KOhm PWRLED_1HZ
R297 4.7KOhm PCI_PME#
R149 4.7KOhm SUSB#
R154 4.7KOhm SUSC#
R268 10KOHM PM_PWRBTN#
R308 10K BACK_OFF#
R288 10K CB_SD#
R307 10K 802_LED_EN
R286 10K WLAN_ON#
R507 1.5KOhm SMB_CLK_S
R508 1.5KOhm SMB_DAT_S
R290 10K GPIO1
R284 4.7KOhm VRM_PWRGD
R309 10KOHM SIO_SMI#
Title : SB400 GPIO/AC97(3)
Engineer: <OrgAddr1>
<OrgName>
Size Custom
Project Name A6R
Rev 1.1
Date: Monday, June 13, 2005
Sheet 14 of 50



ASUSTek COMPUTER INC.		
4 FL.,No.150, Li-Te Rd.,Peitou, Taipei,Taiwan, ROC		
Title: SB400 PWR/DECOUPLING(4)		
Size: Custom	Document Number: A6R	Rev: 1.1
Date: Monday, June 13, 2005	Sheet 15 of 50	

REQUIRED STRAPS



	AUTO_ON#	AC_SDOUT	RTC_CLK	SPDIF_OUT	CLK_LANPCI	CLK_SIOPCI	CLK_KBCPCI	CLK_FWHPCI	CLK_DBPCI	PCI_CLK7 PCI_CLK8
PULL HIGH	MANUAL PWR ON	USE DEBUG STRAPS	INTERNAL RTC	SIO 24MHz	SEE NOTE1	USB PHY PWRDOWN DISABLE	USE USB PLL	SEE NOTE2	CPU I/F = K8	ROM TYPE H,H = PCI ROM H,L = LPC ROM I DEFAULT LPC Address Mapped below 1M L,H = LPC ROM II LPC Address Mapped to top 4G L,L = FWH ROM
PULL LOW	AUTO PWR ON	IGNORE DEBUG STRAPS	EXTERNAL RTC (NOT SUPPORTED W/ IT8712)	SIO 48MHz		USB PHY PWRDOWN ENABLE	BYPASS USB PLL		CPU I/F = P4	

NOTE

1. USB CLK STRAPPING CHANGE

	A21,A22,A23	A31 AND NEWER
10K PULL UP	OSC/CLOCK BUFFER	CRYSTAL PAD
10K PULL DOWN	CRYSTAL PAD	OSC/CLOCK BUFFER

2. 14MHz CLOCK TYPE STRAPPING

	A11~A31	A32 AND ABOVE
	14MHz CLOCK PAD IS CRYSTAL PAD	PCIE COMMON MODE SETTING
10K PULL UP	CLOCK INPUT BUFFER	PCIE CM_SET LOW
10K PULL DOWN	CRYSTAL PAD	PCIE CM_SET HIGH

ASUS

Title : SB400 STRAPS(5)

<OrgName> Engineer: <OrgAddr1>

Size	Project Name	Rev
Custom	A6R	1.1

Date: Monday, June 13, 2005 Sheet 16 of 50

PLACE termination close to source IC

CPU_CLK R107 49.9Ohm r0402
CPU_CLK# R102 49.9Ohm r0402
NB_CLK R96 49.9Ohm r0402
NB_CLK# R94 49.9Ohm r0402
A_LINKCLK R87 49.9Ohm r0402
A_LINKCLK# R79 49.9Ohm r0402
SBSRCCLK R444 49.9Ohm r0402
SBSRCCLK# R442 49.9Ohm r0402
NB_SRCCLK R76 49.9Ohm r0402
NB_SRCCLK# R70 49.9Ohm r0402
GND

+3VS
L29 120Ohm/100Mhz
CLK_VDD
C140 22uF/6.3V
C141 0.1U
C397 0.1U
C388 0.1U
C391 0.1U
C376 0.1U
C381 0.1U
C125 0.1U
L25 120Ohm/100Mhz
CLK_VDD_USB
C129 0.1U
GND

CLK_VDD
CLK_VDD_USB
U6
VDDCPU 45
VDDSRC3 35
VDDATI 32
VDDSRC2 21
VDDSRC1 14
VDD48 3
VDDPCI 51
VDDREF 56
GNDCPU 44
GNDSRC4 36
GNDATI 31
GNDSRC3 26
GNDSRC2 20
GNDPCI 49
GNDSRC1 15
GND2 55
GND1 5
X2 2
X1 1
VTTPWR_GD/PD# 6
SCLK 7
SDATA 8
IREF 37
ICS951417A

X2 14.318MHZ
C133 47pF/50V C0402
C132 47pF/50V C0402
XIN_CLKGEN
XOUT_CLKGEN
R114 0Ohm
14,37,38,39,43 VRM_PWRGD
4,14,18 SMB_CLK_S
4,14,18 SMB_DAT_S
R449 475Ohm

VDDA
L28 120Ohm/100Mhz
+3VS
C107 0.1U
C139 22uF/6.3V
GND

VDDA 39
GNDA 38
CPUCLKT0 47
CPUCLKC0 46
CPUCLKT1 43
CPUCLKC1 42
CPUCLKT2_ITP 41
CPUCLKC2_ITP 40
CPU_STOP# 48
CPUCLKT0 R106 33Ohm CPU_CLK
CPUCLKC0 R103 33Ohm CPU_CLK#
CPUCLKT1 R104 33Ohm NB_CLK
CPUCLKC1 R97 33Ohm NB_CLK#
R455 33Ohm T237
R452 33Ohm T234
CPUSTOP# R108 0Ohm
CLK_CPU_BCLK 2
CLK_CPU_BCLK# 2
NB_CLK 10
NB_CLK# 10
CPU_STP# 2,12

SRCCLKT0 34
SRCCLKC0 33
SRCCLKT3 24
SRCCLKC3 25
SRCCLKT4 22
SRCCLKC4 23
SRCCLKT5 18
SRCCLKC5 19
SRCCLKT6 16
SRCCLKC6 17
SRCCLKT7 12
SRCCLKC7 13
SRCCLKT0 R88 33Ohm A_LINKCLK
SRCCLKC0 R80 33Ohm A_LINKCLK#
SRCCLKT3 R78 33Ohm SBSRCCLK
SRCCLKC3 R72 33Ohm SBSRCCLK#
T42 T43 T48 T49 T52 T51 T54 T55
R105 33Ohm
R100 33Ohm
A_LINKCLK 6
A_LINKCLK# 6
SBSRCCLK 12
SBSRCCLK# 12

ATIGCLKT0 30
ATIGCLKC0 29
ATIGCLKT1 27
ATIGCLKC1 28
ATIGCLKT0 R77 33Ohm /
ATIGCLKC0 R71 33Ohm /
R68 33Ohm T28
R67 33Ohm T27
NB_SRCCLK
NB_SRCCLK#
NB_SRCCLK 6
NB_SRCCLK# 6

CLKREQA# 10
DOC/CLKREQB# 11
CK410#/PCICLK0 50
DOCEN/USB_48MHz 4
RESET# 9
R459 0Ohm /
R457 0Ohm /
R113 33Ohm
USB_48MHZ R117 33Ohm
R656 33Ohm T280
USB_CLK 14
1.1

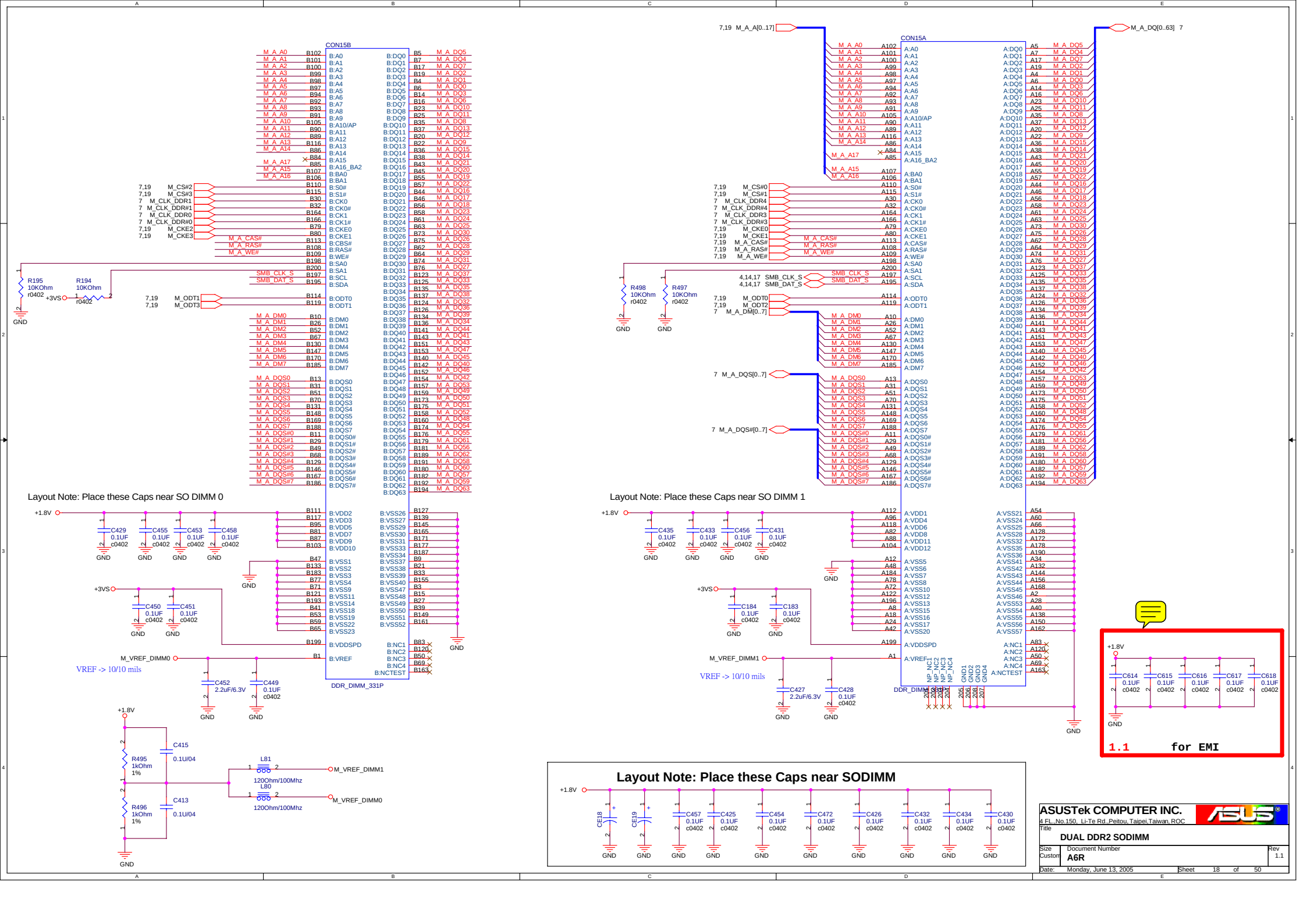
FSLB/REF1 53
FSLA/REF0 54
FSLC/REF2 52
FS_C
R115 4.7KOhm
R123 4.7KOhm
GND
CLK_VDD
1.1

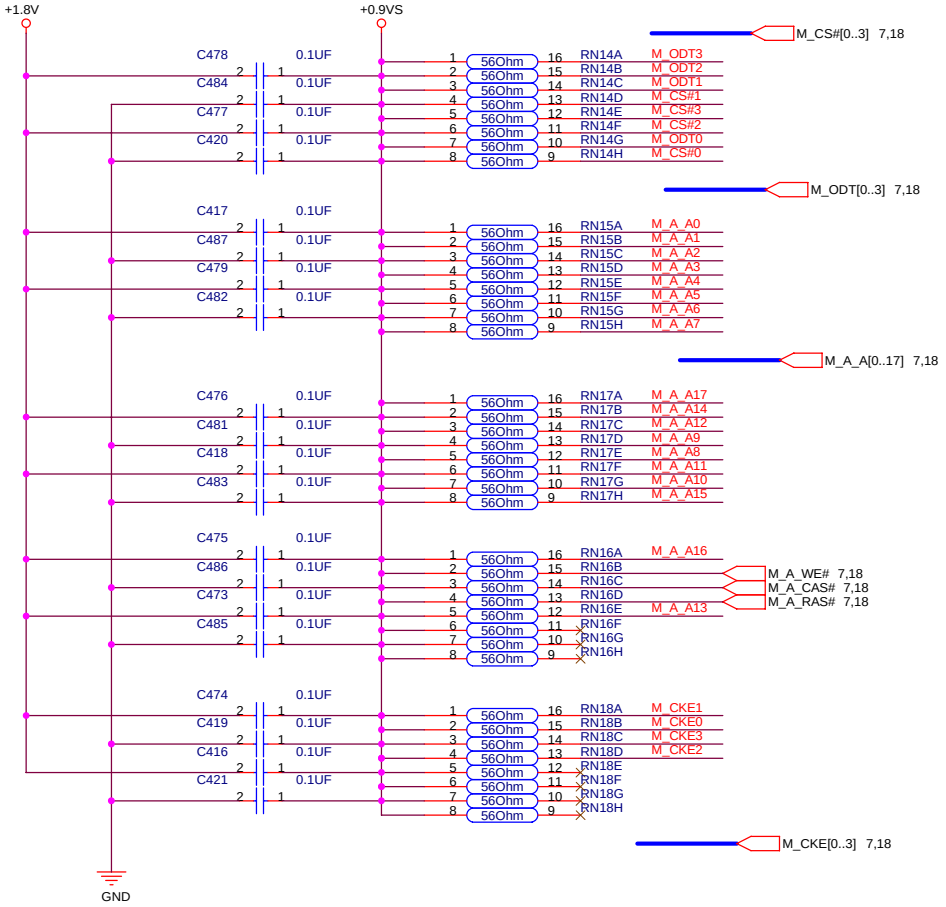
R116 33Ohm AC97_OSCIN 22
R128 33Ohm OSC_14M 10

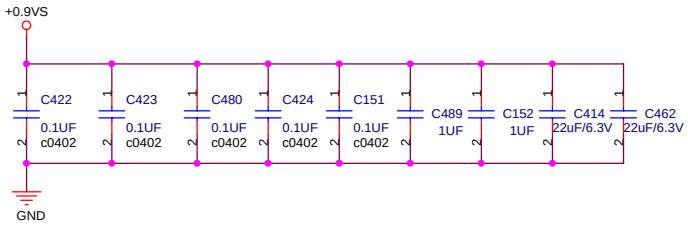
R110 4.7KOhm CPU_BSEL0 9
1.1

R111 33Ohm SB_OSCIN 14

Title : CLOCK GENERATOR		
<OrgName>	Engineer: <OrgAddr1>	
Size: Custom	Project Name: A6R	Rev: 1.1
Date: Monday, June 13, 2005	Sheet 17 of 50	


CON15B
CON15A
DDR_DIMM_331P
DDR_DIMM_200P
Layout Note: Place these Caps near SO DIMM 0
Layout Note: Place these Caps near SO DIMM 1
VREF -> 10/10 mils
VREF -> 10/10 mils
Layout Note: Place these Caps near SODIMM
1.1 for EMI
ASUSTek COMPUTER INC.
4 FL.,No.150, Li-Te Rd.,Peitou, Taipei,Taiwan, ROC
DUAL DDR2 SODIMM
A6R
Monday, June 13, 2005
Sheet 18 of 50





Title : DDR2 TERMINATION

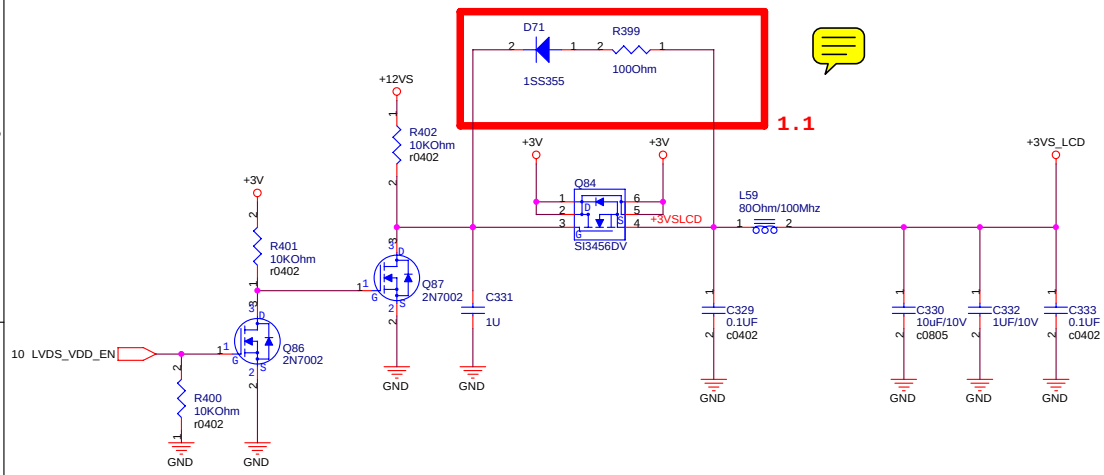
<OrgName> Engineer: <OrgAddr1>

Size	Project Name	Rev
Custom	A6R	1.1

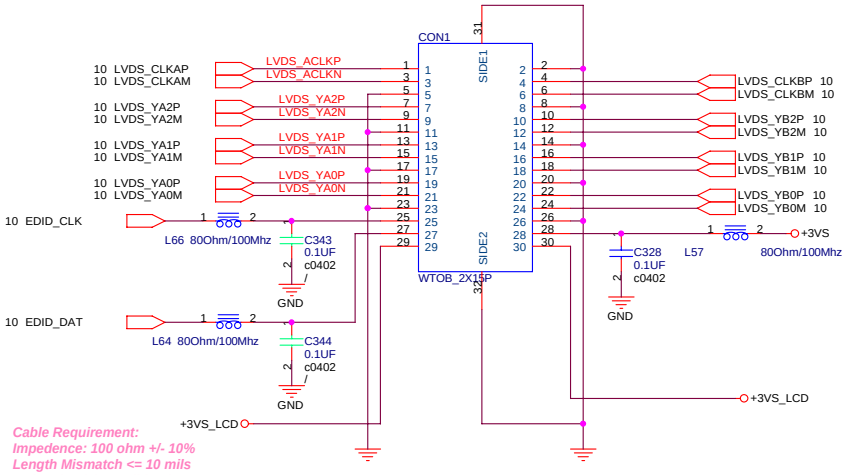
Date: Monday, June 13, 2005 Sheet 19 of 50

LCD Power

3V-3.6V
Full Active: 410 mA(Max. 500 mA)



LCD LVDS Interface

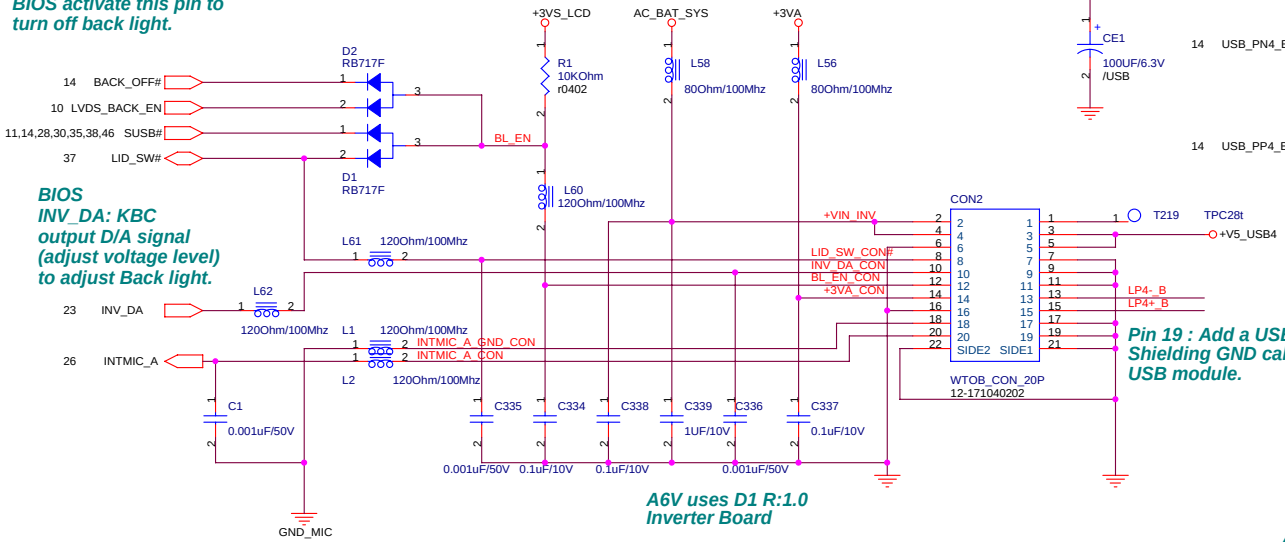


Cable Requirement:
Impedence: 100 ohm +/- 10%
Length Mismatch <= 10 mils
Twisted Pair(Not Ribbon)
Maximum Length <= 16"

INVERTER Interface

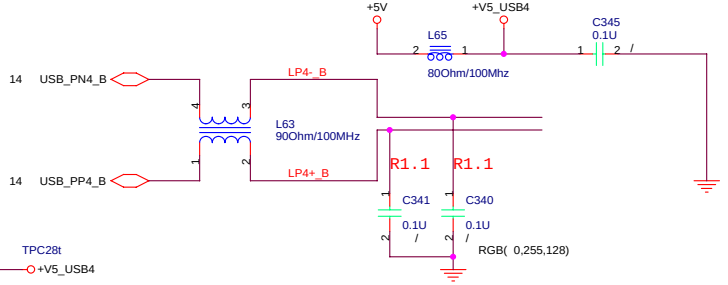
BIOS
BACK_OFF#: When user pushs "Fn+F7" button, BIOS activate this pin to turn off back light.

BIOS
INV_DA: KBC output D/A signal (adjust voltage level) to adjust Back light.



A6V uses D1 R:1.0 Inverter Board

Pin 19 : Add a USB 2.0 Shielding GND cable to USB module.



USB PORT 4 for USB CAMERA

A6V doesn't support USB WLAN function!

ASUS

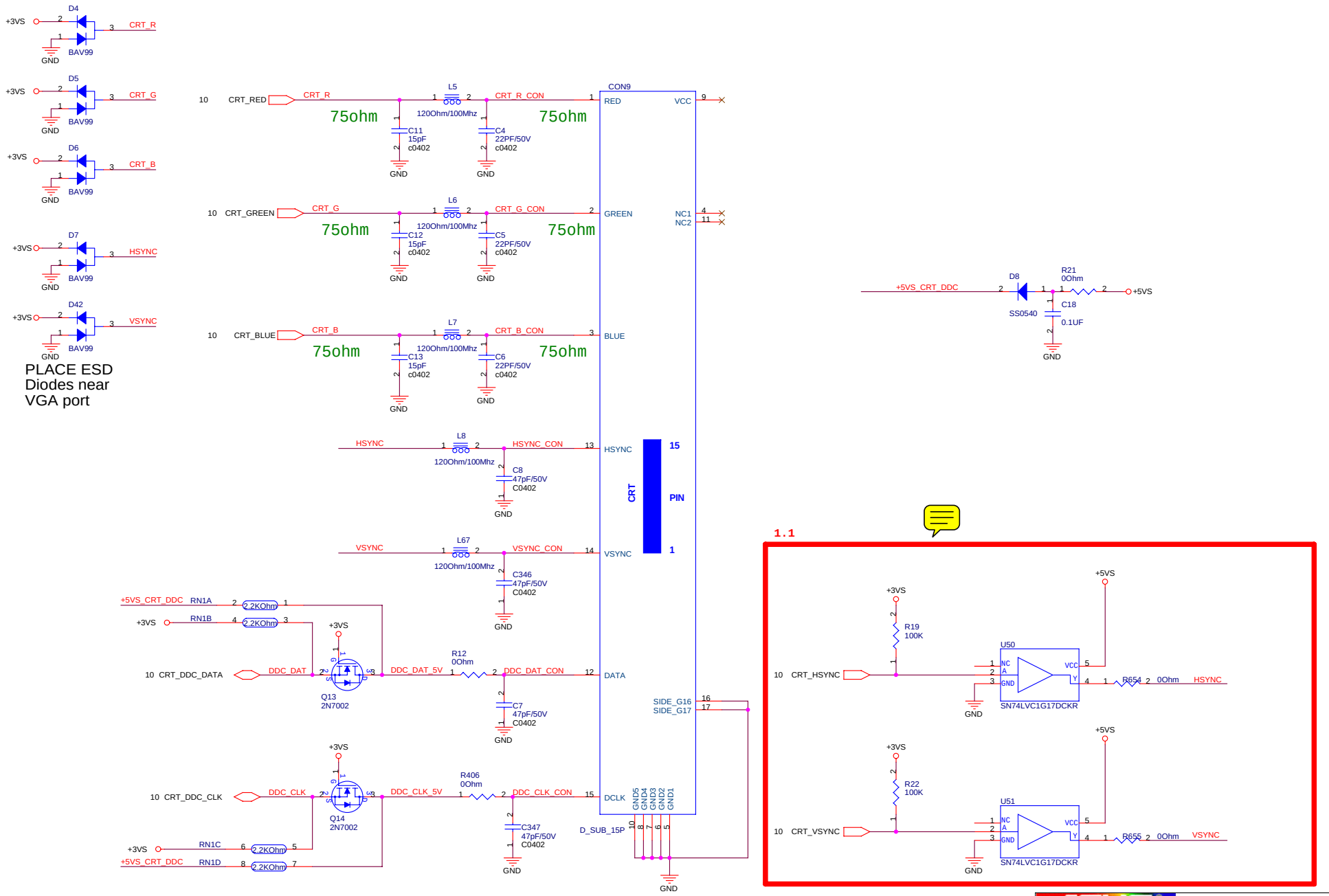
Title : LVDS & INVERTER (CAMERA)

<OrgName>

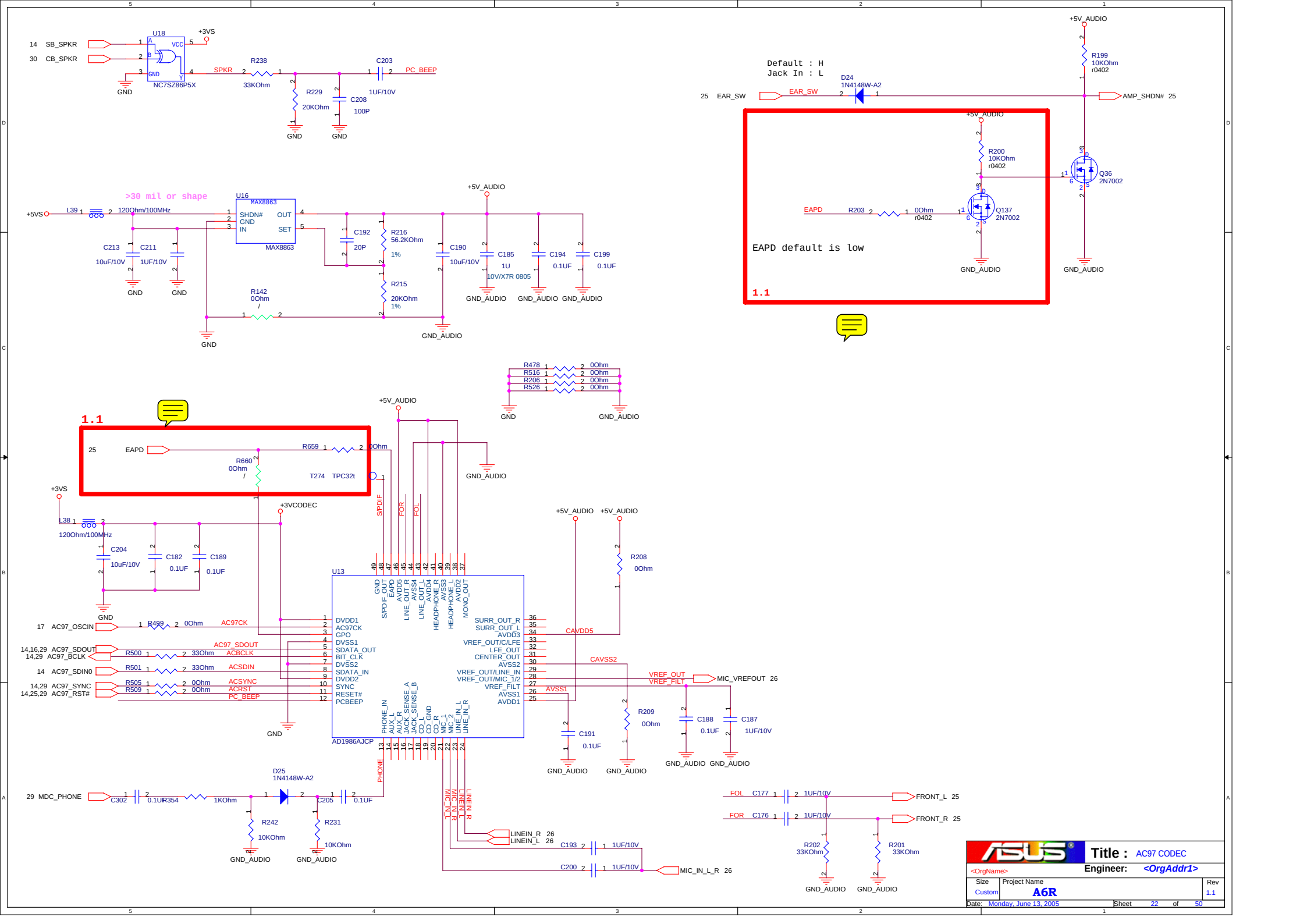
Engineer: *<OrgAddr1>*

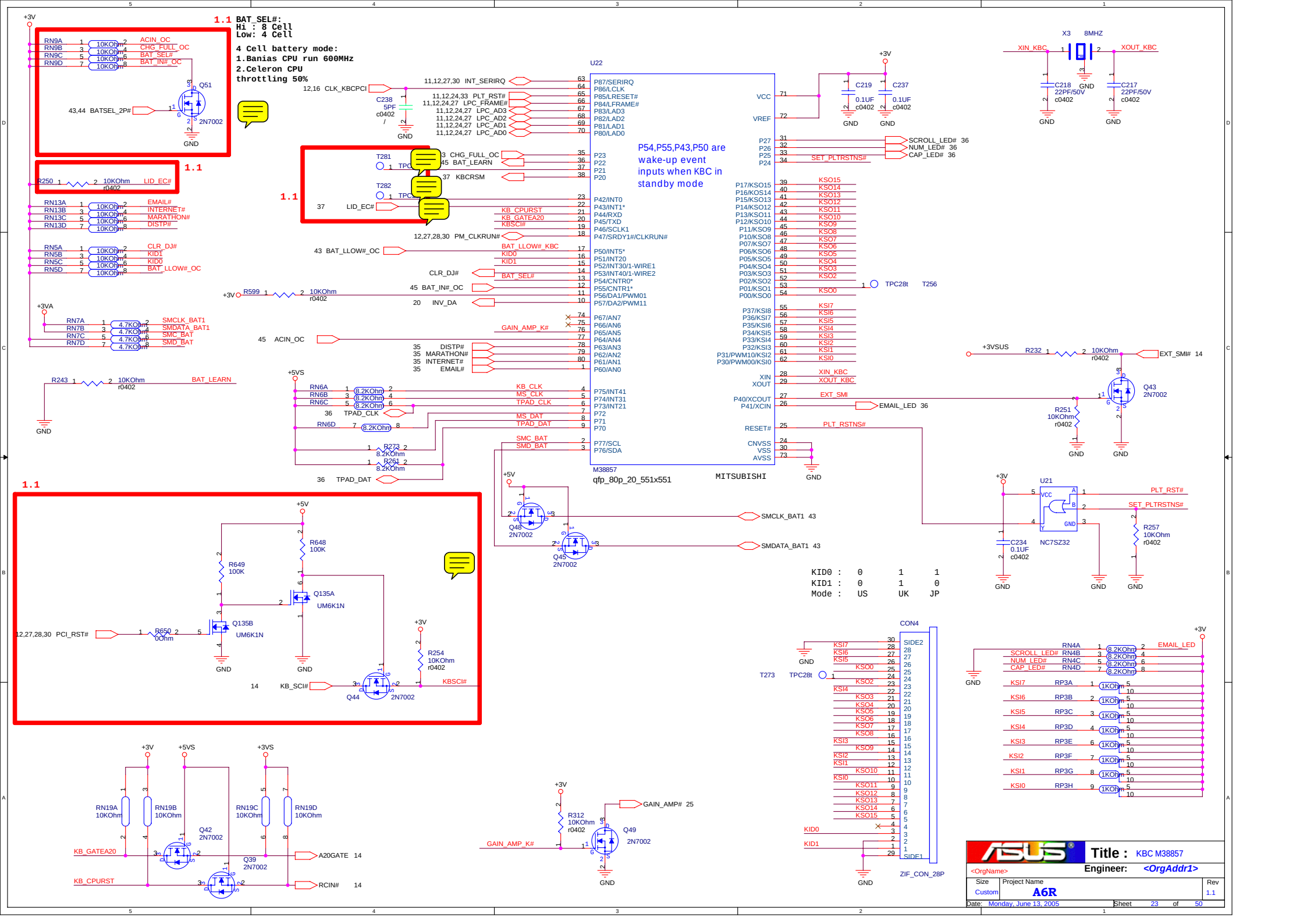
Size	Project Name	Rev
Custom	A6R	1.1

Date: Monday, June 13, 2005 Sheet 20 of 50

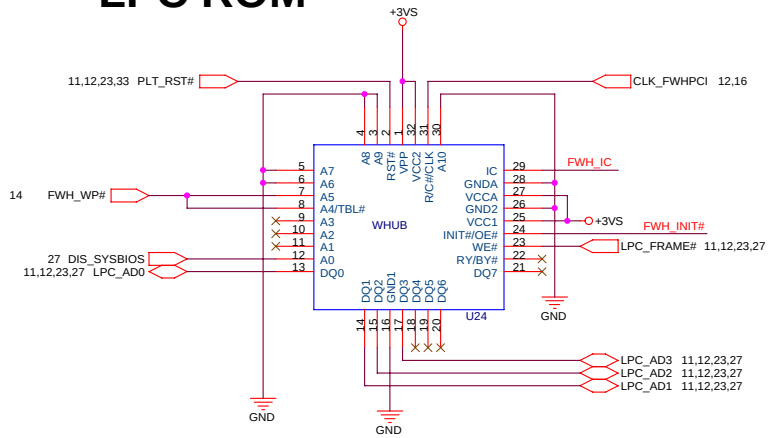


Title : TV , CRT CONNECTOR		
<OrgName>	Engineer: <OrgAddr1>	
Size: Custom	Project Name: A6R	Rev: 1.1
Date: Monday, June 13, 2005	Sheet 21 of 50	

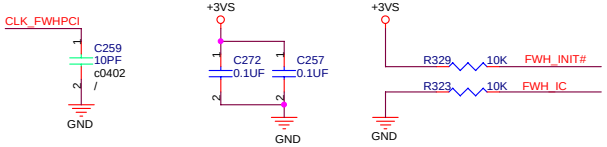

14 SB_SPKR
30 CB_SPKR
U18
NC7SZ86P5X
+3VS
GND
SPKR
R238
33KOhm
R229
20KOhm
C208
100P
C203
1UF/10V
PC_BEEP
>30 mil or shape
+5VS
L39
120Ohm/100MHz
U16
MAX8863
SHDN#
GND
IN
OUT
SET
C213
10uF/10V
C211
1UF/10V
C192
20P
R216
56.2KOhm
1%
R215
20KOhm
1%
R142
0Ohm
C190
10uF/10V
C185
1U
10V/X7R 0805
C194
0.1UF
C199
0.1UF
+5V_AUDIO
GND_AUDIO
Default : H
Jack In : L
25 EAR_SW
D24
1N4148W-A2
R199
10KOhm
r0402
AMP_SHDN# 25
R200
10KOhm
r0402
Q36
2N7002
EAPD
R203
0Ohm
Q137
2N7002
EAPD default is low
1.1
R478
R516
R206
R526
0Ohm
25 EAPD
R659
R660
0Ohm
T274 TPC32t
+3VCODEC
L38
120Ohm/100MHz
C204
10uF/10V
C182
0.1UF
C189
0.1UF
U13
AD1986AJCP
SPDIF
FOR
FOL
17 AC97_OSCIN
R499
AC97CK
14,16,29 AC97_SDOUT
14,29 AC97_BCLK
R500
33Ohm
ACBCLK
AC97_SDOUT
14 AC97_SDIN0
R501
ACSDIN
14,29 AC97_SYNC
14,25,29 AC97_RST#
R505
R509
ACSYNC
ACRST
PC_BEEP
DVDD1
AC97CK
GPO
DVSS1
SDATA_OUT
BIT_CLK
DVSS2
SDATA_IN
DVDD2
SYNC
RESET#
PCBEEP
SURR_OUT_R
SURR_OUT_L
AVDD3
VREF_OUT/C/LFE
LFE_OUT
CENTER_OUT
AVSS2
VREF_OUT/LINE_IN
VREF_OUT/MIC_1/2
VREF_FILT
AVSS1
AVDD1
CAVDD5
CAVSS2
AVSS1
R208
0Ohm
R209
0Ohm
C191
0.1UF
C188
0.1UF
C187
1UF/10V
VREF_OUT
VREF_FILT
MIC_VREFOUT 26
PHONE_IN
AUX_L
AUX_R
JACK_SENSE_A
JACK_SENSE_B
CD_L_GND
CD_R
MIC_1
MIC_2
LINE_IN_L
LINE_IN_R
PHONE
29 MDC_PHONE
C302
0.1UF
R354
1KOhm
D25
1N4148W-A2
C205
0.1UF
R242
10KOhm
R231
10KOhm
MIC_IN_L
MIC_IN_R
LINEIN_L
LINEIN_R
LINEIN_R 26
LINEIN_L 26
C193
1UF/10V
C200
1UF/10V
MIC_IN_L_R 26
FOL C177
FOR C176
1UF/10V
FRONT_L 25
FRONT_R 25
R202
33KOhm
R201
33KOhm
Title : AC97 CODEC
<OrgName>
Engineer: <OrgAddr1>
Size Custom
Project Name A6R
Rev 1.1
Date: Monday, June 13, 2005
Sheet 22 of 50


1.1 BAT_SEL#:
Hi : 8 Cell
Low: 4 Cell
4 Cell battery mode:
1.Banias CPU run 600MHz
2.Celeron CPU
throttling 50%
P54,P55,P43,P50 are wake-up event inputs when KBC in standby mode
U22
M38857
qfp_80p_20_551x551
MITSUBISHI
X3 8MHZ
U21
NC7SZ32
CON4
ZIF_CON_28P
KID0 : 0 1 1
KID1 : 0 1 0
Mode : US UK JP
Title : KBC M38857
Engineer: <OrgAddr1>
A6R
Monday, June 13, 2005

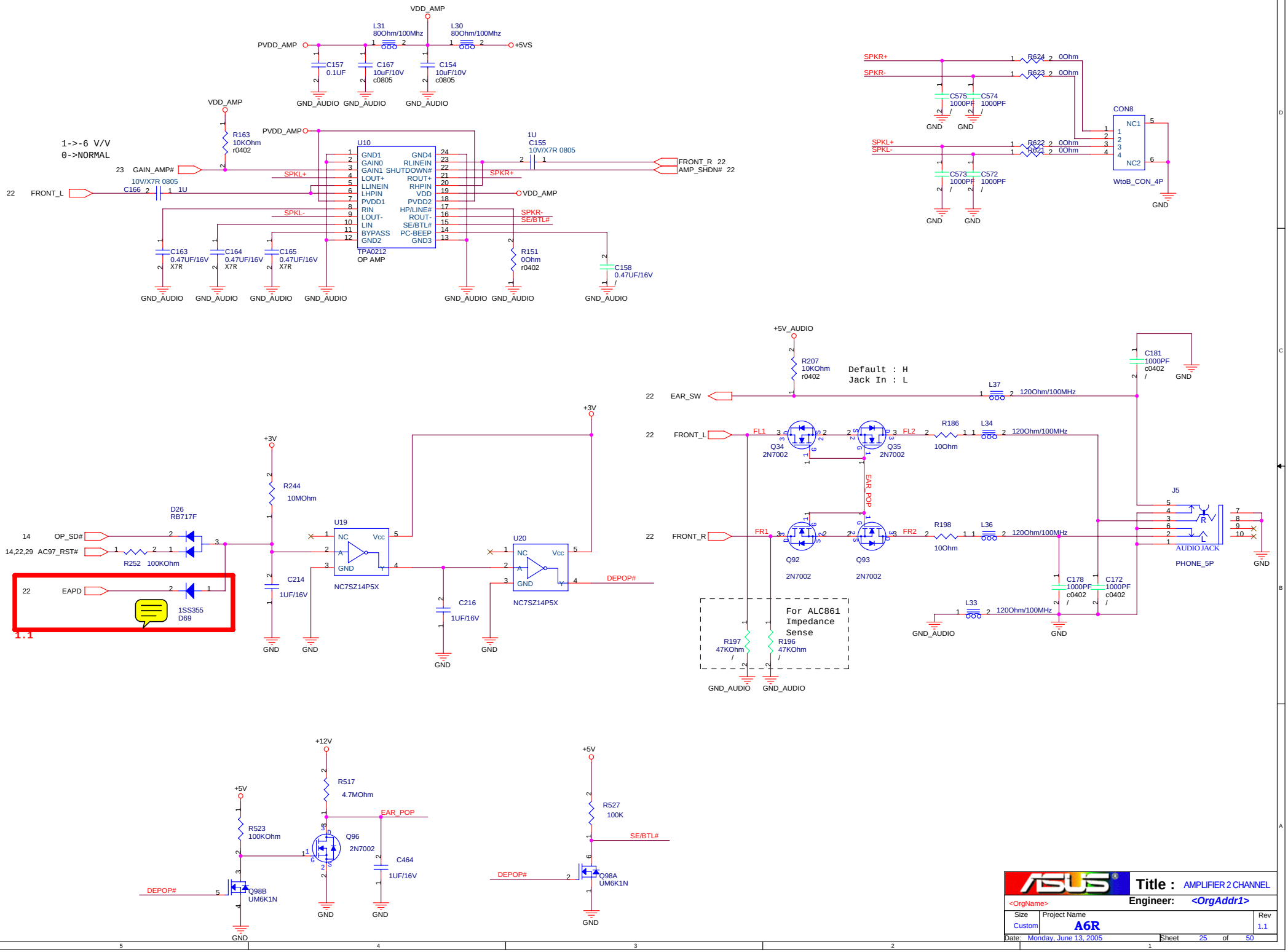
LPC ROM



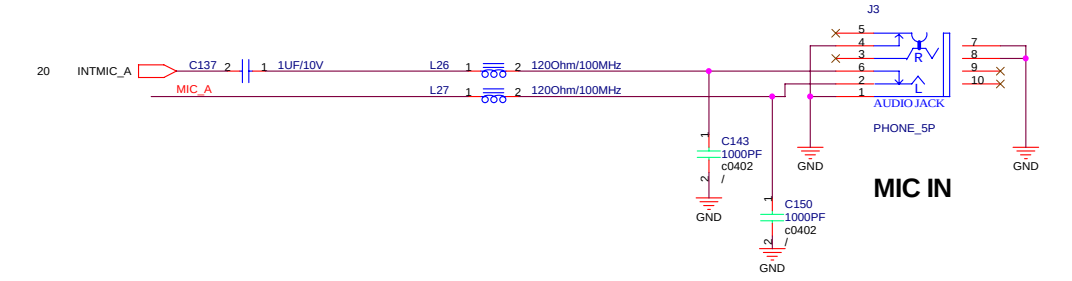
PLCC32 Socket Part Number :
12-043000321
SST FWH/LPC Part Number :
05-001017122(燒)

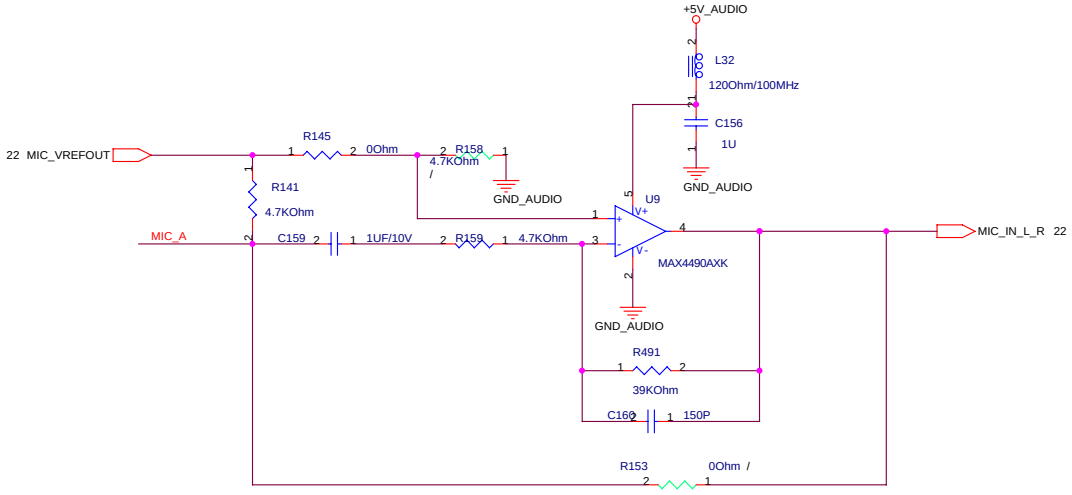


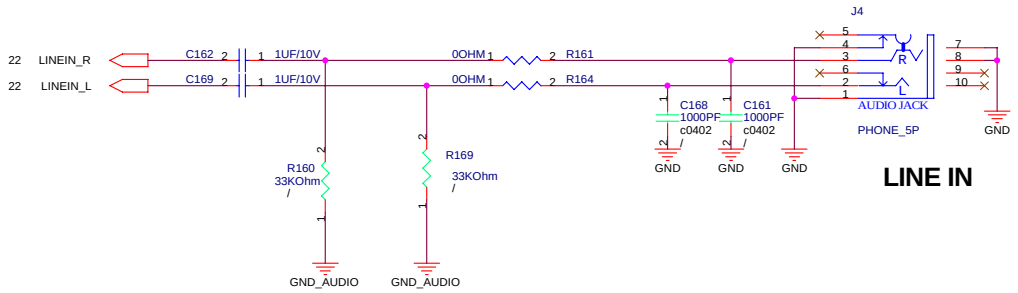
Title : FWH			
<OrgName>	Engineer: <OrgAddr1>		
Size: Custom	Project Name: A6R		Rev: 1.1
Date: Monday, June 13, 2005	Sheet 24 of 50		

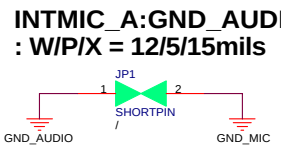


ASUS	Title :	AMPLIFIER 2 CHANNEL
<OrgName>	Engineer:	<OrgAddr1>
Size: Custom	Project Name: A6R	Rev: 1.1
Date: Monday, June 13, 2005	Sheet 25 of 50	

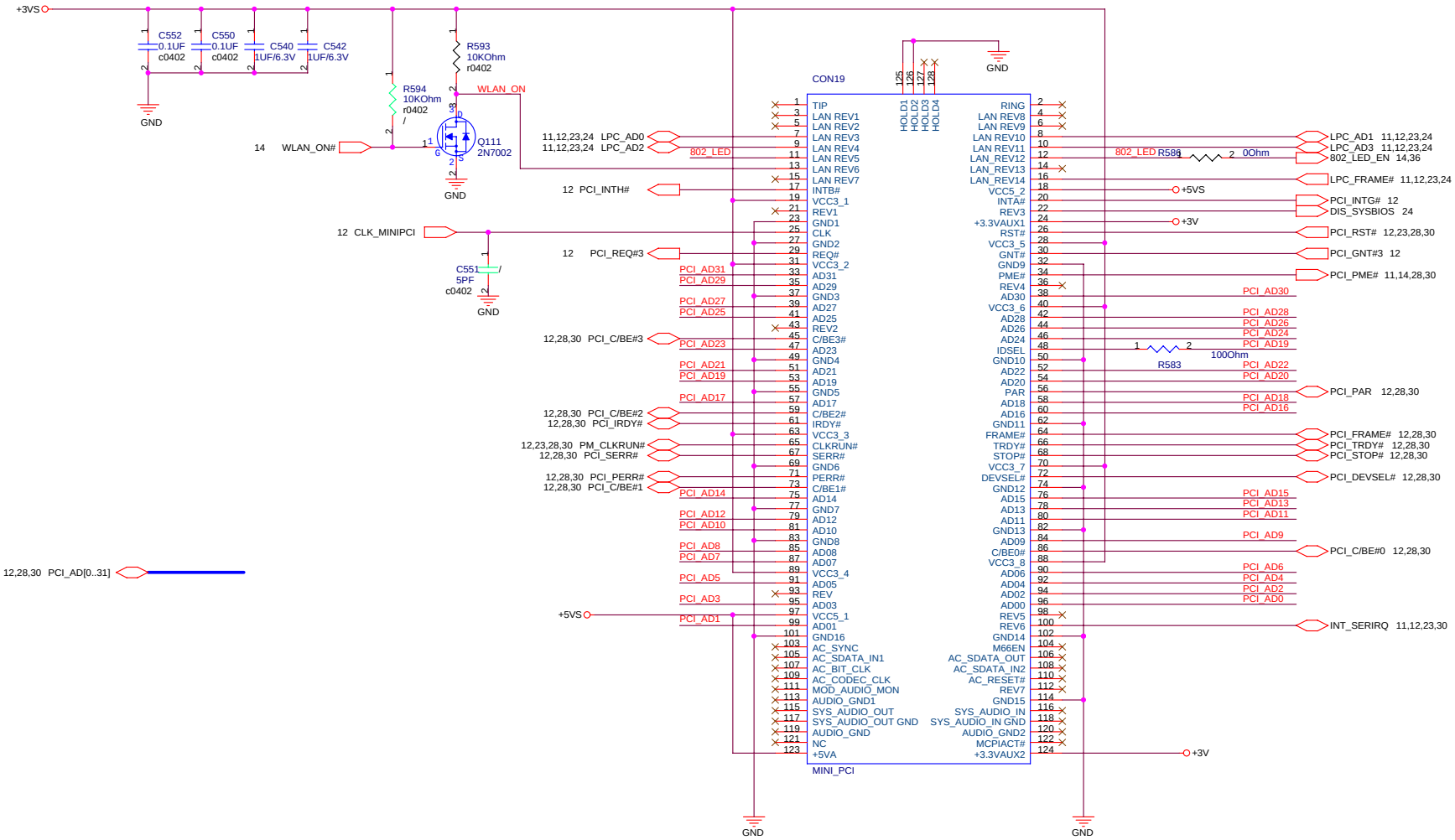




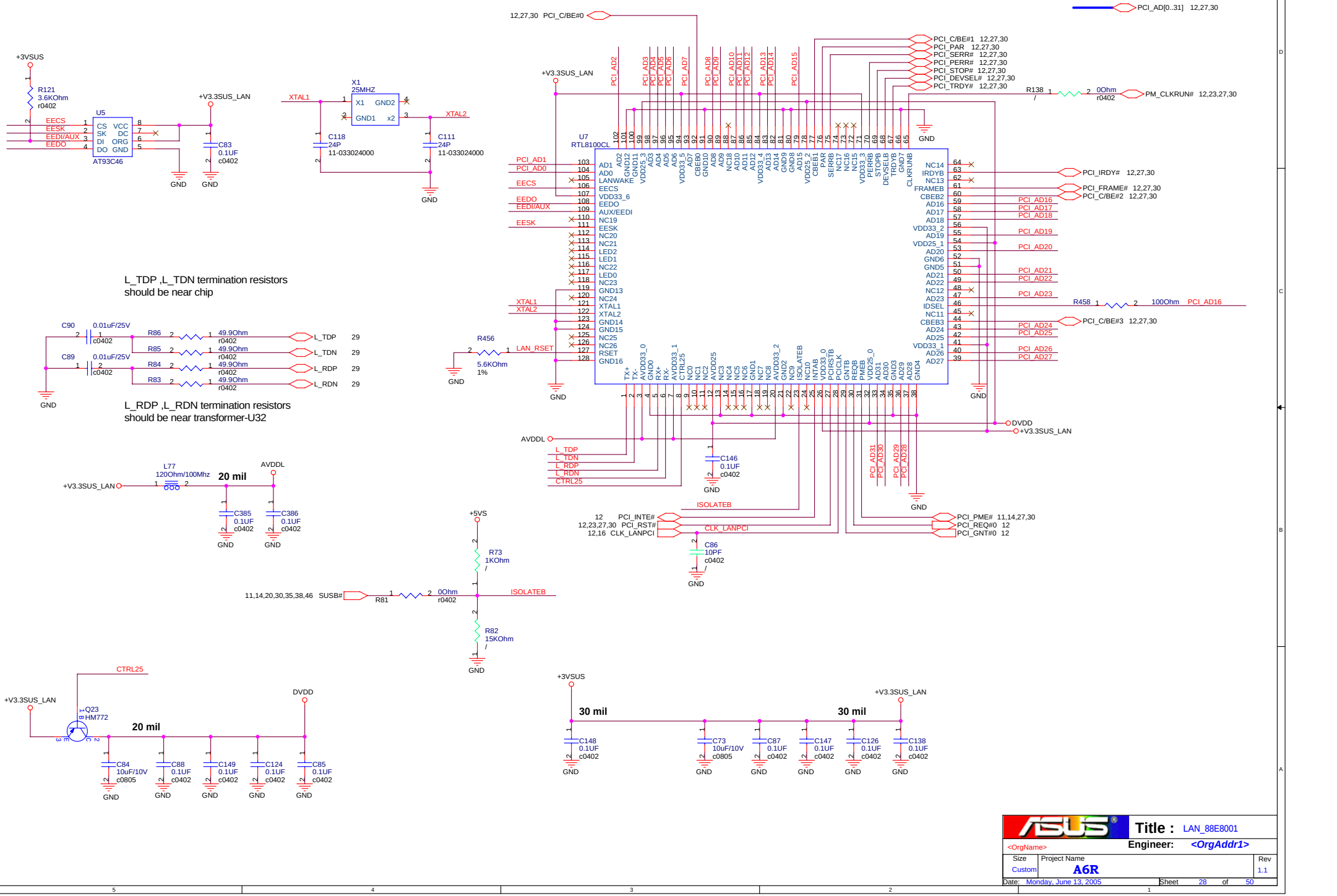




ASUS	Title : MIC,LINE-IN JACK	
<OrgName>	Engineer: <OrgAddr1>	
Size: Custom	Project Name: A6R	Rev: 1.1
Date: Monday, June 13, 2005	Sheet 26 of 50	



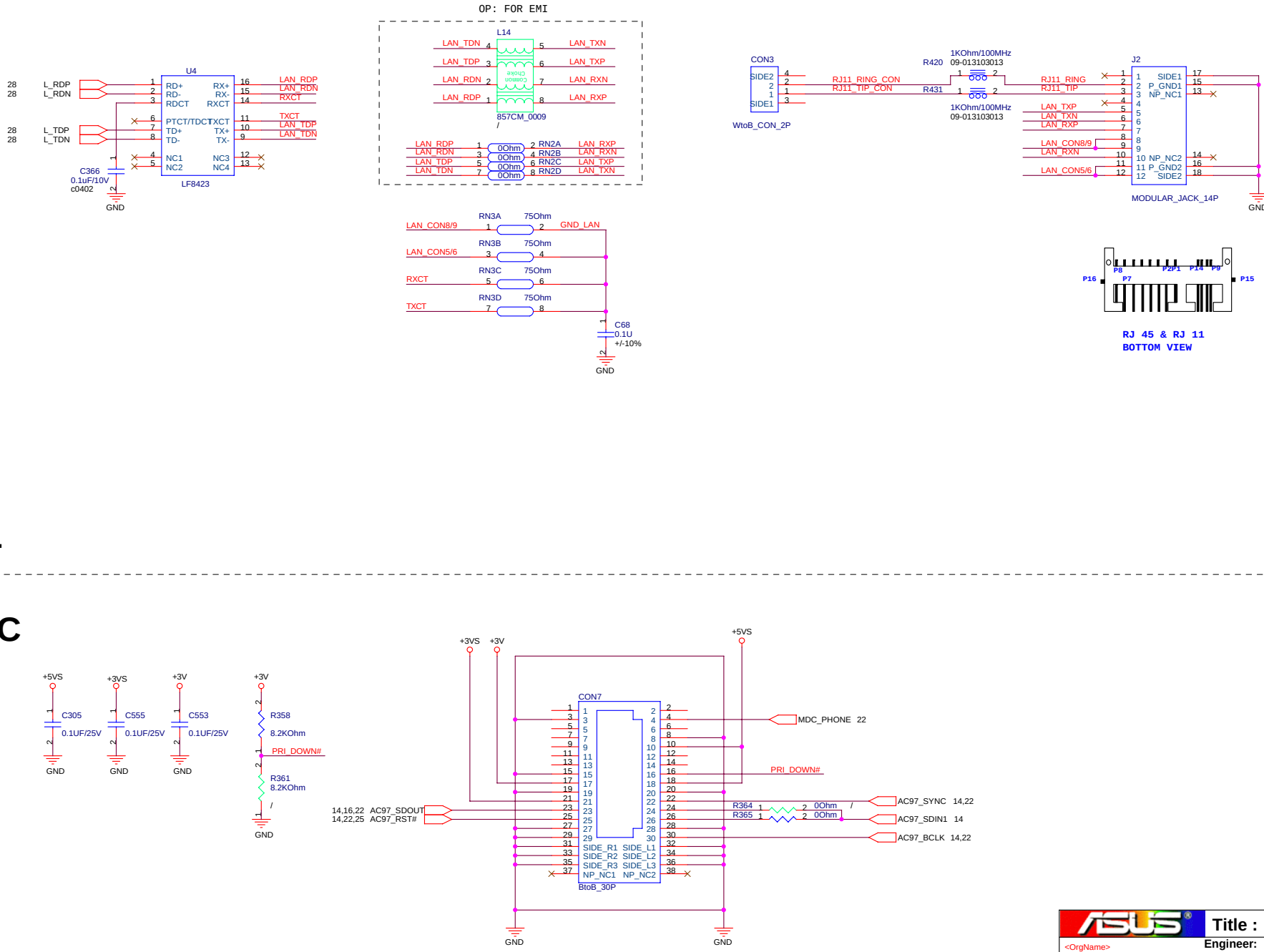
Title : MINIPCI_WIRELESS		
<OrgName>	Engineer: <OrgAddr1>	
Size: Custom	Project Name: A6R	Rev: 1.1
Date: Monday, June 13, 2005	Sheet 27 of 50	



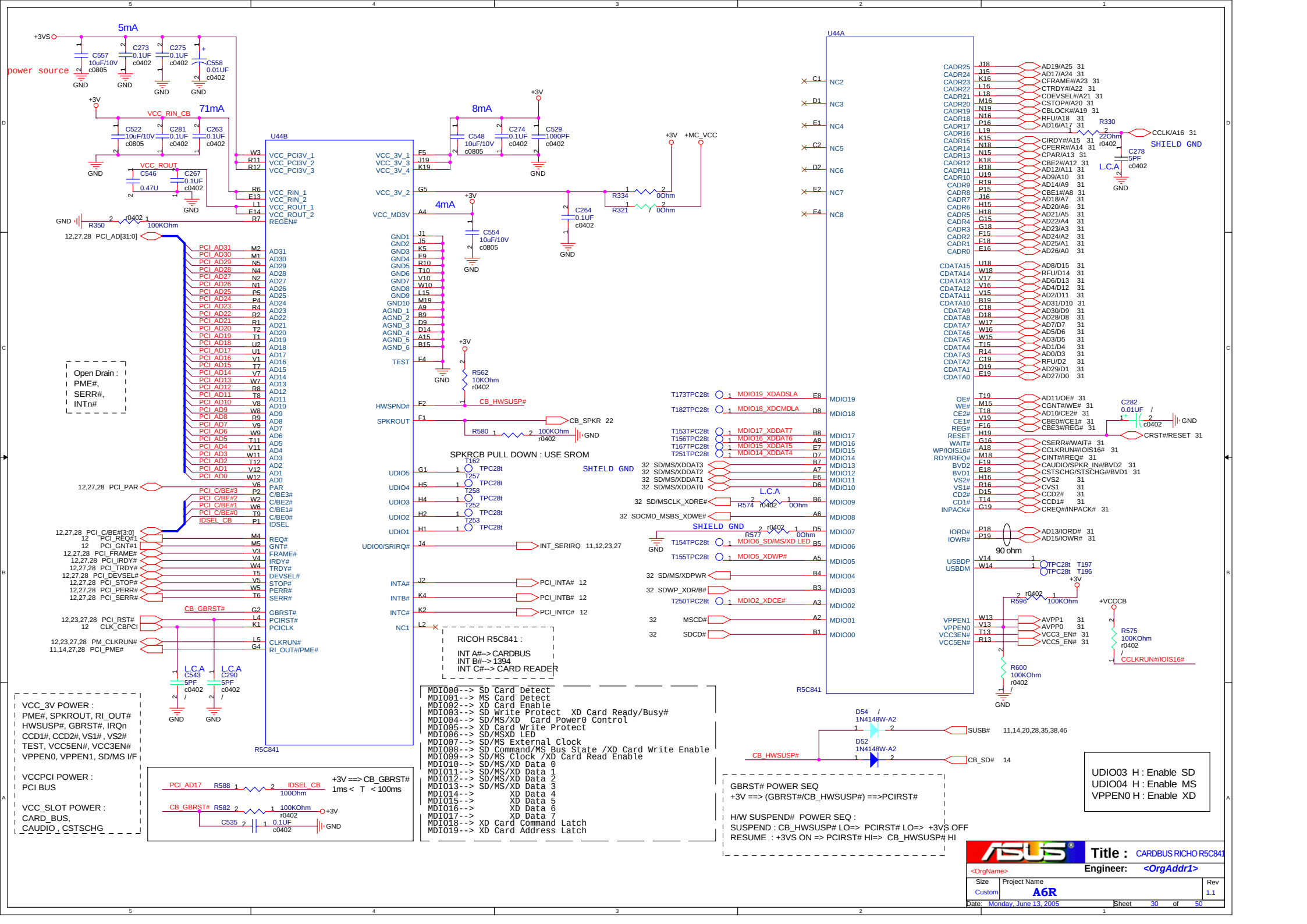
<OrgName>	Title : LAN_88E8001		
	Engineer: <OrgAddr1>		
Size: Custom	Project Name: A6R		Rev: 1.1
Date: Monday, June 13, 2005	Sheet 28 of 50		

LAN PORT

MDC



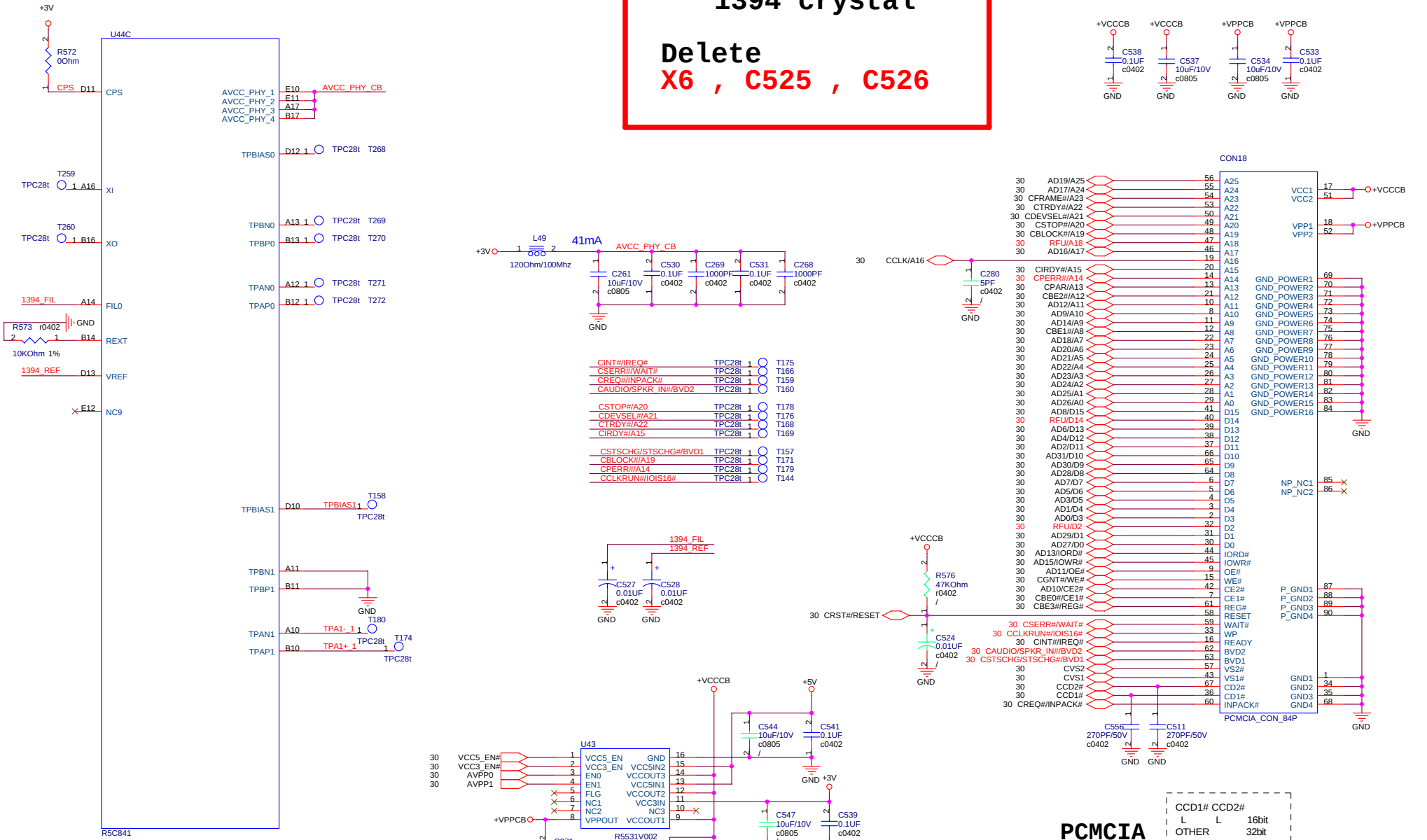
Title : RJ11+45 & MDC		
<OrgName>	Engineer: <OrgAddr1>	
Size: Custom	Project Name: A6R	Rev: 1.1
Date: Monday, June 13, 2005	Sheet 29 of 50	


5mA
power source
+3VS
C557 10uF/10V c0805
C273 0.1UF c0402
C275 0.1UF c0402
C558 0.01UF c0402
GND
71mA
VCC_RIN_CB
C522 10uF/10V c0805
C281 0.1UF c0402
C263 0.1UF c0402
VCC_ROUT
C546 0.47U
C267 0.1UF c0402
R350 100KOhm
12,27,28 PCI_AD[31:0]
PCI_AD31 PCI_AD30 PCI_AD29 PCI_AD28 PCI_AD27 PCI_AD26 PCI_AD25 PCI_AD24 PCI_AD23 PCI_AD22 PCI_AD21 PCI_AD20 PCI_AD19 PCI_AD18 PCI_AD17 PCI_AD16 PCI_AD15 PCI_AD14 PCI_AD13 PCI_AD12 PCI_AD11 PCI_AD10 PCI_AD9 PCI_AD8 PCI_AD7 PCI_AD6 PCI_AD5 PCI_AD4 PCI_AD3 PCI_AD2 PCI_AD1 PCI_AD0
12,27,28 PCI_PAR
PCI_C/BE#3 PCI_C/BE#2 PCI_C/BE#1 PCI_C/BE#0 IDSEL_CB
12,27,28 PCI_C/BE#[3:0]
12 PCI_REQ#1
12 PCI_GNT#1
12,27,28 PCI_FRAME#
12,27,28 PCI_IRDY#
12,27,28 PCI_TRDY#
12,27,28 PCI_DEVSEL#
12,27,28 PCI_STOP#
12,27,28 PCI_PERR#
12,27,28 PCI_SERR#
CB_GBRST#
12,23,27,28 PCI_RST#
12 CLK_CBPCI
12,23,27,28 PM_CLKRUN#
11,14,27,28 PCI_PME#
L.C.A C543 5PF c0402
L.C.A C290 5PF c0402
U44B
VCC_PCI3V_1 VCC_PCI3V_2 VCC_PCI3V_3
VCC_RIN_1 VCC_RIN_2 VCC_ROUT_1 VCC_ROUT_2 REGEN#
AD31 AD30 AD29 AD28 AD27 AD26 AD25 AD24 AD23 AD22 AD21 AD20 AD19 AD18 AD17 AD16 AD15 AD14 AD13 AD12 AD11 AD10 AD9 AD8 AD7 AD6 AD5 AD4 AD3 AD2 AD1 AD0
PAR C/BE3# C/BE2# C/BE1# C/BE0# IDSEL
REQ# GNT# FRAME# IRDY# TRDY# DEVSEL# STOP# PERR# SERR#
GBRST# PCIRST# PCICLK
CLKRUN# RI_OUT#/PME#
R5C841
VCC_3V_1 VCC_3V_3 VCC_3V_4
VCC_3V_2
VCC_MD3V
GND1 GND2 GND3 GND4 GND5 GND6 GND7 GND8 GND9 GND10
AGND_1 AGND_2 AGND_3 AGND_4 AGND_5 AGND_6
TEST
HWSPND#
SPKROUT
UDIO5 UDIO4 UDIO3 UDIO2 UDIO1
UDIO0/SRIRQ#
INTA# INTB# INTC#
NC1
8mA
C548 10uF/10V c0805
C274 0.1UF c0402
C529 1000PF c0402
4mA
C554 10uF/10V c0805
C264 0.1UF c0402
+MC_VCC
R334 0Ohm
R321 0Ohm
R562 10KOhm r0402
CB_HWSUSP#
R580 100KOhm r0402
CB_SPKR 22
SPKRCB PULL DOWN : USE SROM
T162 T257 T258 T252 T253 TPC28t
INT_SERIRQ 11,12,23,27
PCI_INTA# 12
PCI_INTB# 12
PCI_INTC# 12
Open Drain : PME#, SERR#, INTn#
RICOH R5C841 :
INT A#--> CARDBUS
INT B#--> 1394
INT C#--> CARD READER
U44A
NC1 NC2 NC3 NC4 NC5 NC6 NC7 NC8
MDIO19 MDIO18 MDIO17 MDIO16 MDIO15 MDIO14 MDIO13 MDIO12 MDIO11 MDIO10 MDIO09 MDIO08 MDIO07 MDIO06 MDIO05 MDIO04 MDIO03 MDIO02 MDIO01 MDIO00
T173TPC28t MDIO19_XDADSLA
T182TPC28t MDIO18_XDCMDLA
T153TPC28t MDIO17_XDDAT7
T156TPC28t MDIO16_XDDAT6
T167TPC28t MDIO15_XDDAT5
T251TPC28t MDIO14_XDDAT4
SHIELD GND
32 SD/MS/XDDAT3
32 SD/MS/XDDAT2
32 SD/MS/XDDAT1
32 SD/MS/XDDAT0
L.C.A
32 SD/MSCLK_XDRE#
R574 r0402 0Ohm
32 SDCMD_MSBS_XDWE#
SHIELD GND
R577 r0402 0Ohm
MDIO6_SD/MS/XD LED
T154TPC28t
T155TPC28t MDIO5_XDWP#
32 SD/MS/XDPWR
32 SDWP_XDR/B#
T250TPC28t MDIO2_XDCE#
32 MSCD#
32 SDCD#
R5C841
CADR25 CADR24 CADR23 CADR22 CADR21 CADR20 CADR19 CADR18 CADR17 CADR16 CADR15 CADR14 CADR13 CADR12 CADR11 CADR10 CADR9 CADR8 CADR7 CADR6 CADR5 CADR4 CADR3 CADR2 CADR1 CADR0
AD19/A25 AD17/A24 CFRAME#/A23 CTRDY#/A22 CDEVSEL#/A21 CSTOP#/A20 CBLOCK#/A19 RFU/A18 AD16/A17
R330 22Ohm r0402
CCLK/A16
SHIELD GND
C278 5PF c0402
L.C.A
CIRDY#/A15 CPERR#/A14 CPAR/A13 CBE2#/A12 AD12/A11 AD9/A10 AD14/A9 CBE1#/A8 AD18/A7 AD20/A6 AD21/A5 AD22/A4 AD23/A3 AD24/A2 AD25/A1 AD26/A0
CDATA15 CDATA14 CDATA13 CDATA12 CDATA11 CDATA10 CDATA9 CDATA8 CDATA7 CDATA6 CDATA5 CDATA4 CDATA3 CDATA2 CDATA1 CDATA0
AD8/D15 RFU/D14 AD6/D13 AD4/D12 AD2/D11 AD31/D10 AD30/D9 AD28/D8 AD7/D7 AD5/D6 AD3/D5 AD1/D4 AD0/D3 RFU/D2 AD29/D1 AD27/D0
OE# WE# CE2# CE1# REG# RESET WAIT# WP/IOIS16# RDY/IREQ# BVD2 BVD1 VS2# VS1# CD2# CD1# INPACK#
AD11/OE# CGNT#/WE# AD10/CE2# CBE0#/CE1# CBE3#/REG# CRST#/RESET
C282 0.01UF c0402
CSERR#/WAIT# CCLKRUN#/IOIS16# CINT#/IREQ# CAUDIO/SPKR_IN#/BVD2 CSTSCHG/STSCHG#/BVD1 CVS2 CVS1 CCD2# CCD1# CREQ#/INPACK#
IORD# IOWR#
AD13/IORD# AD15/IOWR#
90 ohm
USBDP USBDM
TPC28t T197 TPC28t T196
R596 r0402 100KOhm
+VCCCB
VPPEN1 VPPEN0 VCC3EN# VCC5EN#
AVPP1 AVPP0 VCC3_EN# VCC5_EN#
R575 100KOhm r0402
CCLKRUN#/IOIS16#
R600 100KOhm r0402
D54 1N4148W-A2
D52 1N4148W-A2
SUSB# 11,14,20,28,35,38,46
CB_SD# 14
CB_HWSUSP#
VCC_3V POWER :
PME#, SPKROUT, RI_OUT#
HWSUSP#, GBRST#, IRQn
CCD1#, CCD2#, VS1# , VS2#
TEST, VCC5EN#, VCC3EN#
VPPEN0, VPPEN1, SD/MS I/F
VCCPCI POWER :
PCI BUS
VCC_SLOT POWER :
CARD_BUS,
CAUDIO , CSTSCHG
PCI_AD17 R588 IDSEL_CB 100Ohm
CB_GBRST# R582 100KOhm r0402 +3V
C535 0.1UF c0402 GND
+3V ==> CB_GBRST#
1ms < T < 100ms
MDIO00--> SD Card Detect
MDIO01--> MS Card Detect
MDIO02--> XD Card Enable
MDIO03--> SD Write Protect XD Card Ready/Busy#
MDIO04--> SD/MS/XD Card Power0 Control
MDIO05--> XD Card Write Protect
MDIO06--> SD/MSXD LED
MDIO07--> SD/MS External Clock
MDIO08--> SD Command/MS Bus State /XD Card Write Enable
MDIO09--> SD/MS Clock /XD Card Read Enable
MDIO10--> SD/MS/XD Data 0
MDIO11--> SD/MS/XD Data 1
MDIO12--> SD/MS/XD Data 2
MDIO13--> SD/MS/XD Data 3
MDIO14--> XD Data 4
MDIO15--> XD Data 5
MDIO16--> XD Data 6
MDIO17--> XD Data 7
MDIO18--> XD Card Command Latch
MDIO19--> XD Card Address Latch
GBRST# POWER SEQ
+3V ==> (GBRST#/CB_HWSUSP#) ==>PCIRST#
H/W SUSPEND# POWER SEQ :
SUSPEND : CB_HWSUSP# LO=> PCIRST# LO=> +3VS OFF
RESUME : +3VS ON => PCIRST# HI=> CB_HWSUSP# HI
UDIO03 H : Enable SD
UDIO04 H : Enable MS
VPPEN0 H : Enable XD
Title : CARDBUS RICHO R5C841
<OrgName>
Engineer: <OrgAddr1>
Size Custom
Project Name A6R
Rev 1.1
Date: Monday, June 13, 2005
Sheet 30 of 50

1.1

1394 crystal

Delete
X6 , C525 , C526



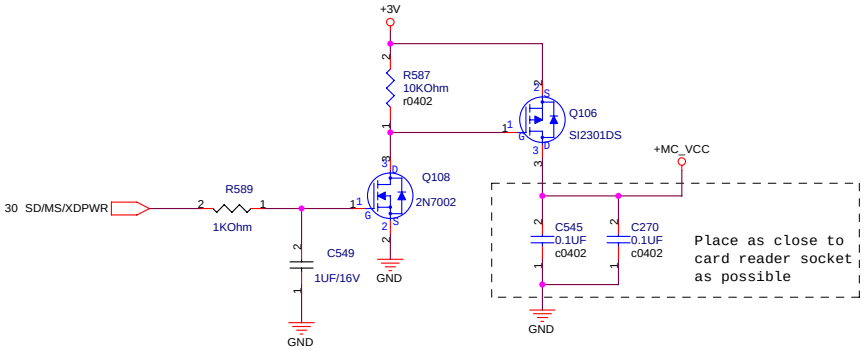
ASUS	Title : PCMCIA SOCKET	
<OrgName>	Engineer: <OrgAddr1>	
Size: Custom	Project Name: A6R	Rev: 1.1
Date: Monday, June 13, 2005	Sheet 31 of 50	

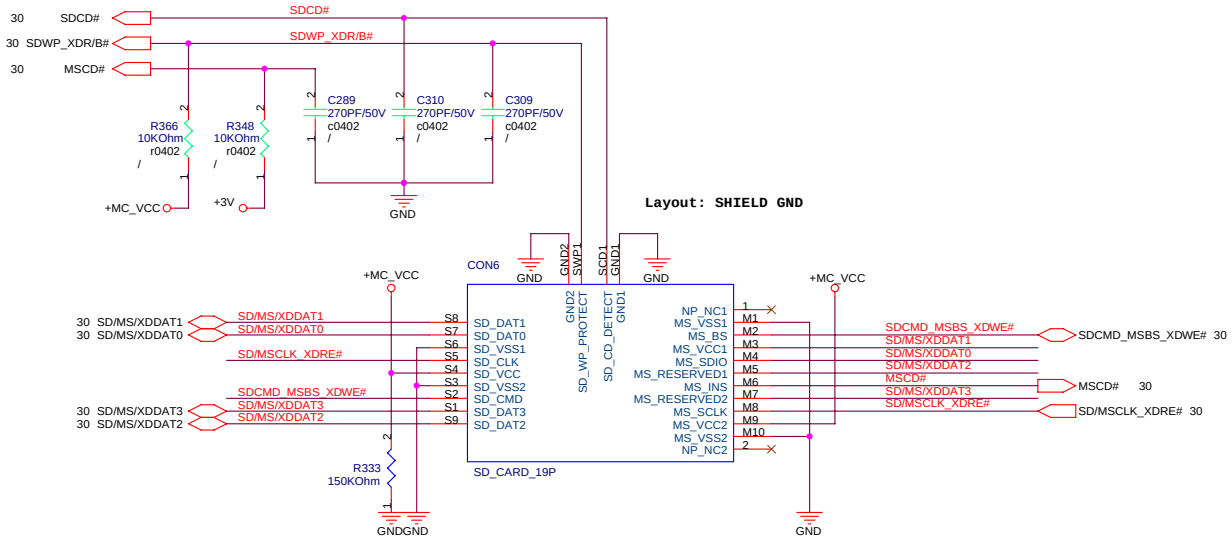
1394 CON

Delete

CON17 , L40 , R568 , R569
R570 , R571 , R566 , C518
C520 , C52

U42 , C532 , R579 , R584

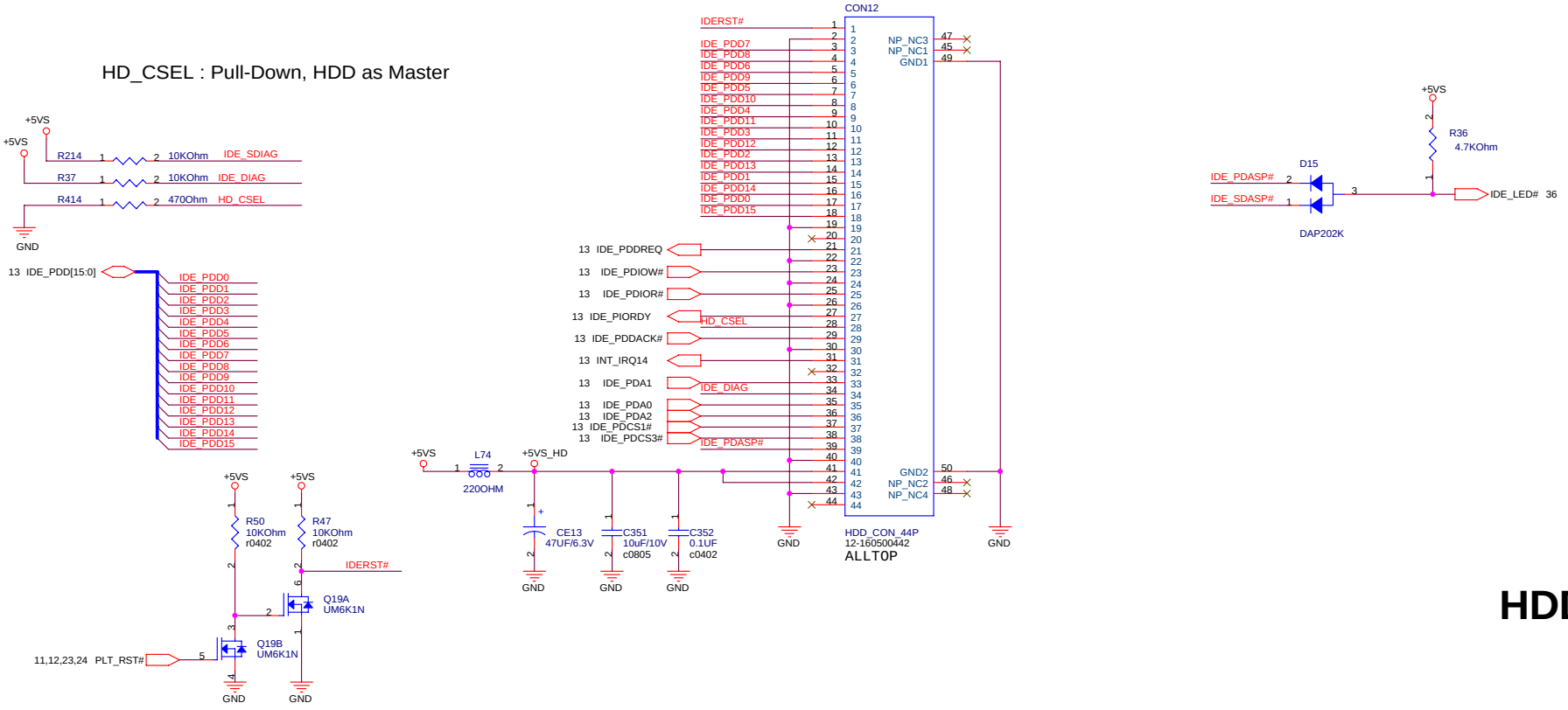




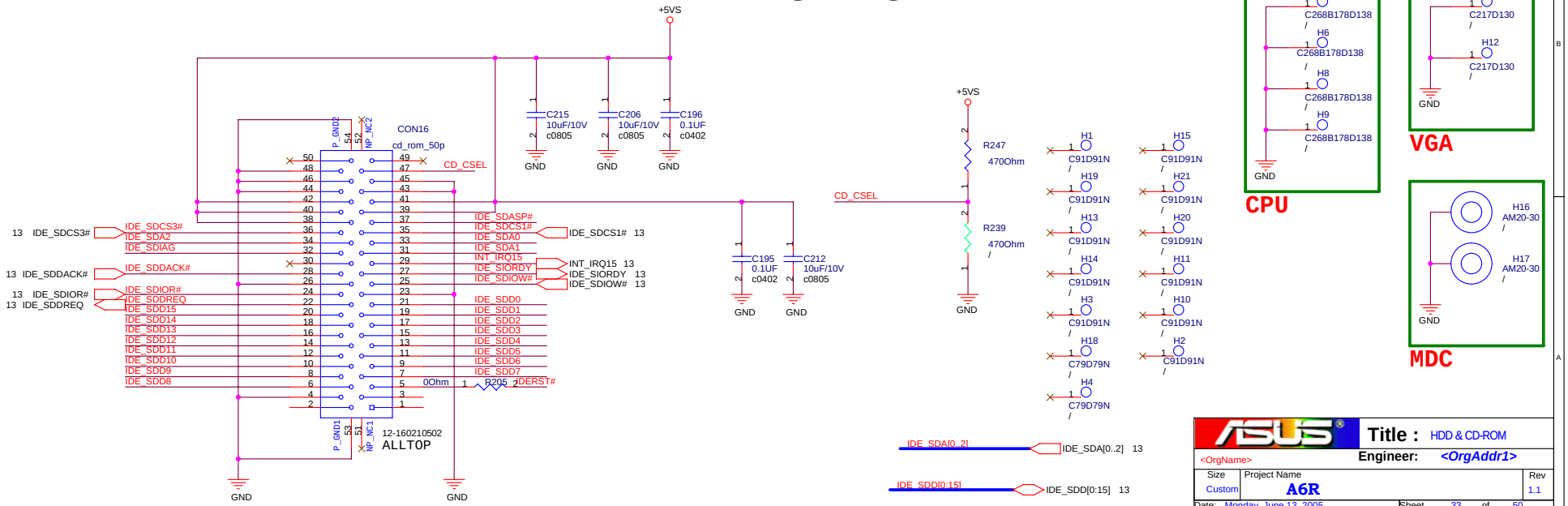
ASUS	Title : IEEE 1394 & 4 IN 1 CON		
<OrgName>	Engineer: <OrgAddr1>		
Size: Custom	Project Name: A6R		Rev: 1.1
Date: Monday, June 13, 2005	Sheet 32 of 50		

HDD

HD_CSEL : Pull-Down, HDD as Master

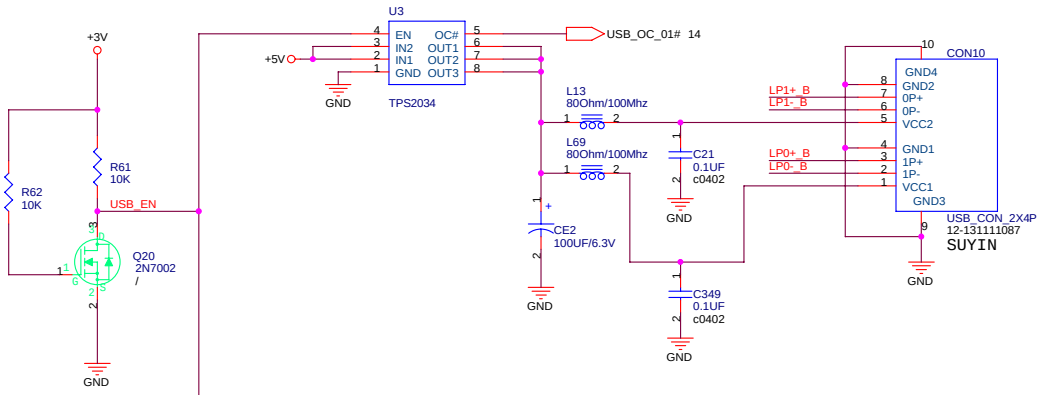


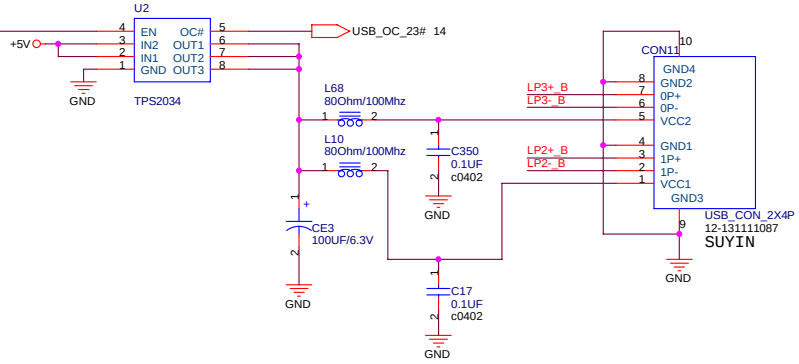
CD-ROM

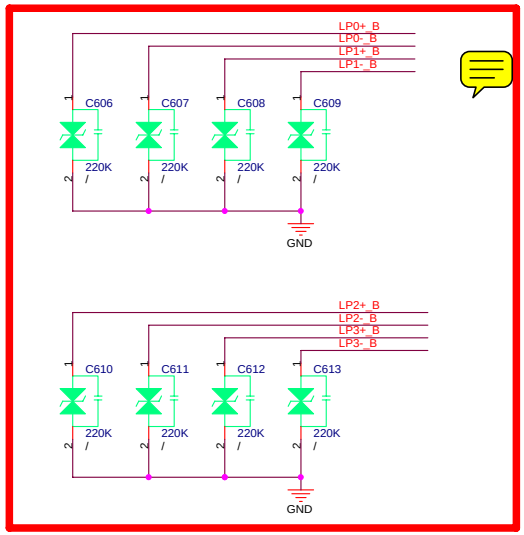


ASUS	Title : HDD & CD-ROM	
<OrgName>	Engineer: <OrgAddr1>	
Size: Custom	Project Name: A6R	Rev: 1.1
Date: Monday, June 13, 2005	Sheet 33 of 50	

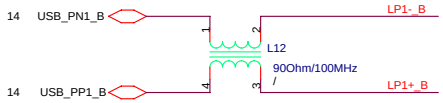
USB

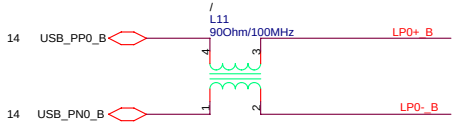


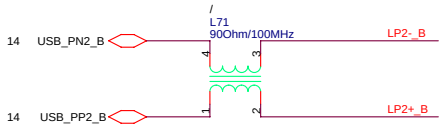


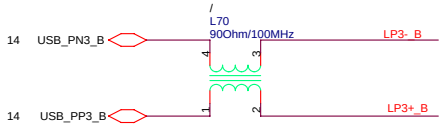


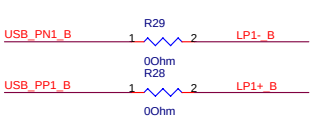
1.1

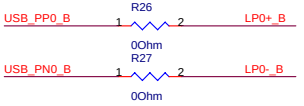


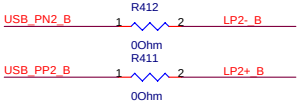


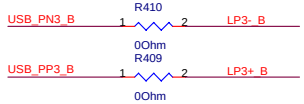






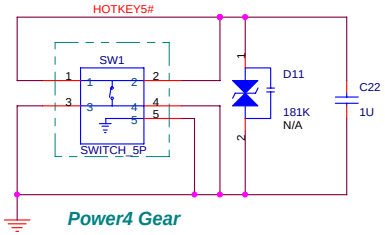




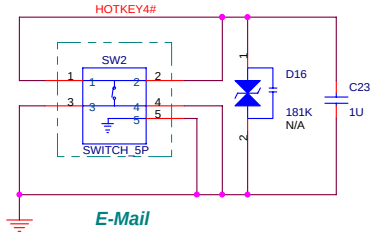


ASUS	Title : USB	
<OrgName>	Engineer: <OrgAddr1>	
Size: Custom	Project Name: A6R	Rev: 1.1
Date: Monday, June 13, 2005	Sheet 34 of 50	

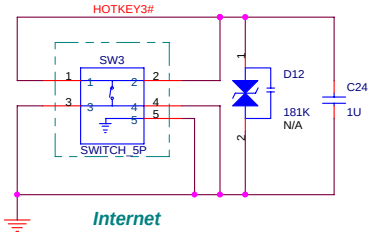
FUNCTION KEY



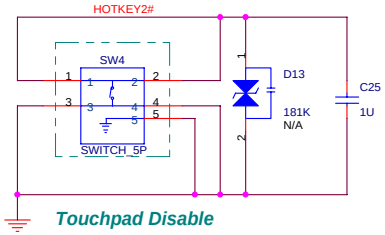
Power4 Gear



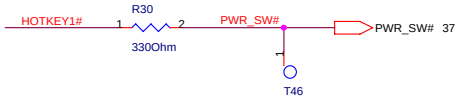
E-Mail

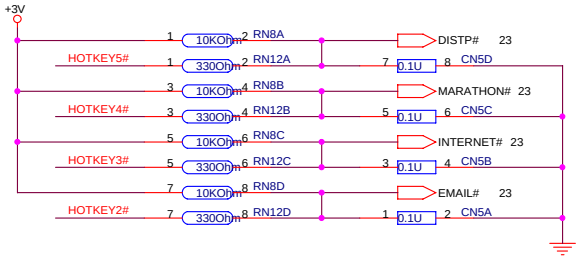


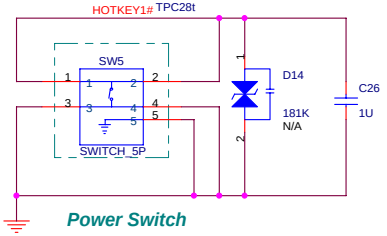
Internet



Touchpad Disable

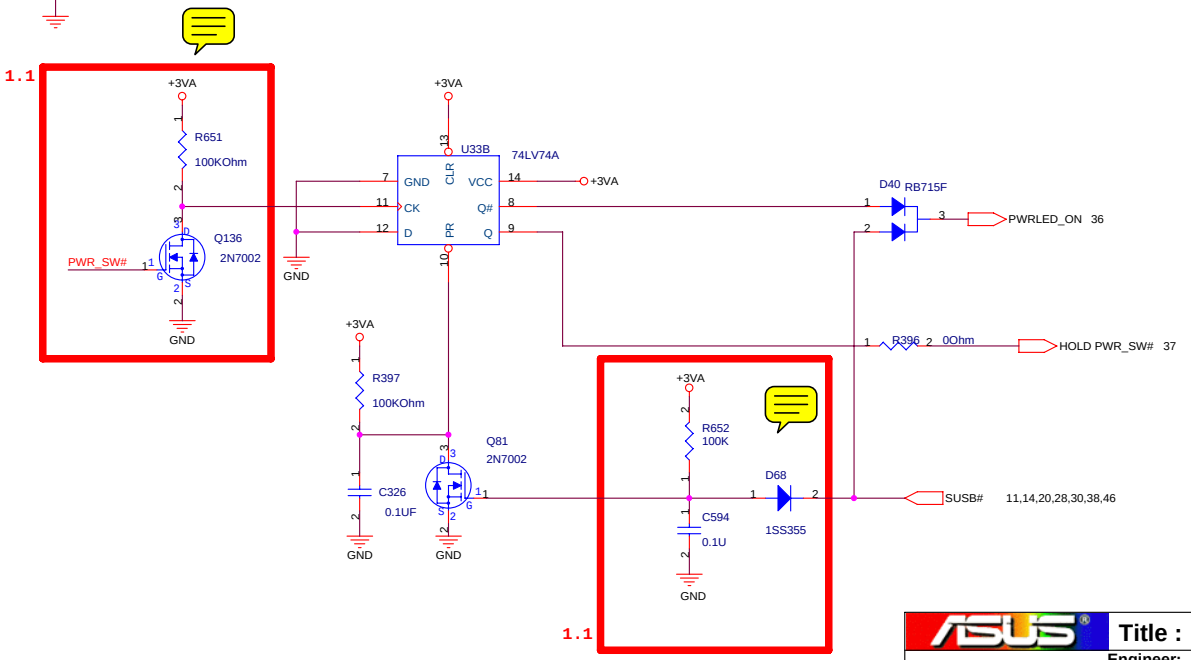


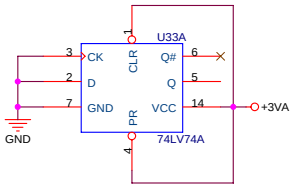




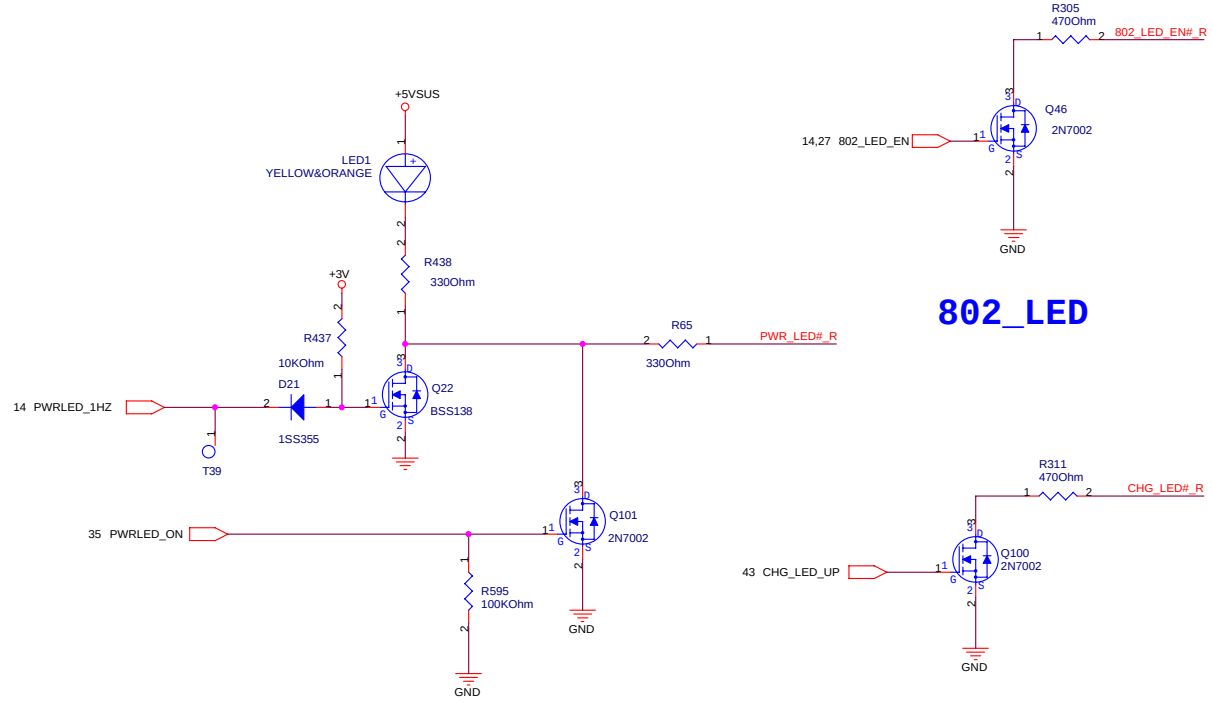
Power Switch

Uses 5-pin switch to improve ESD margin.

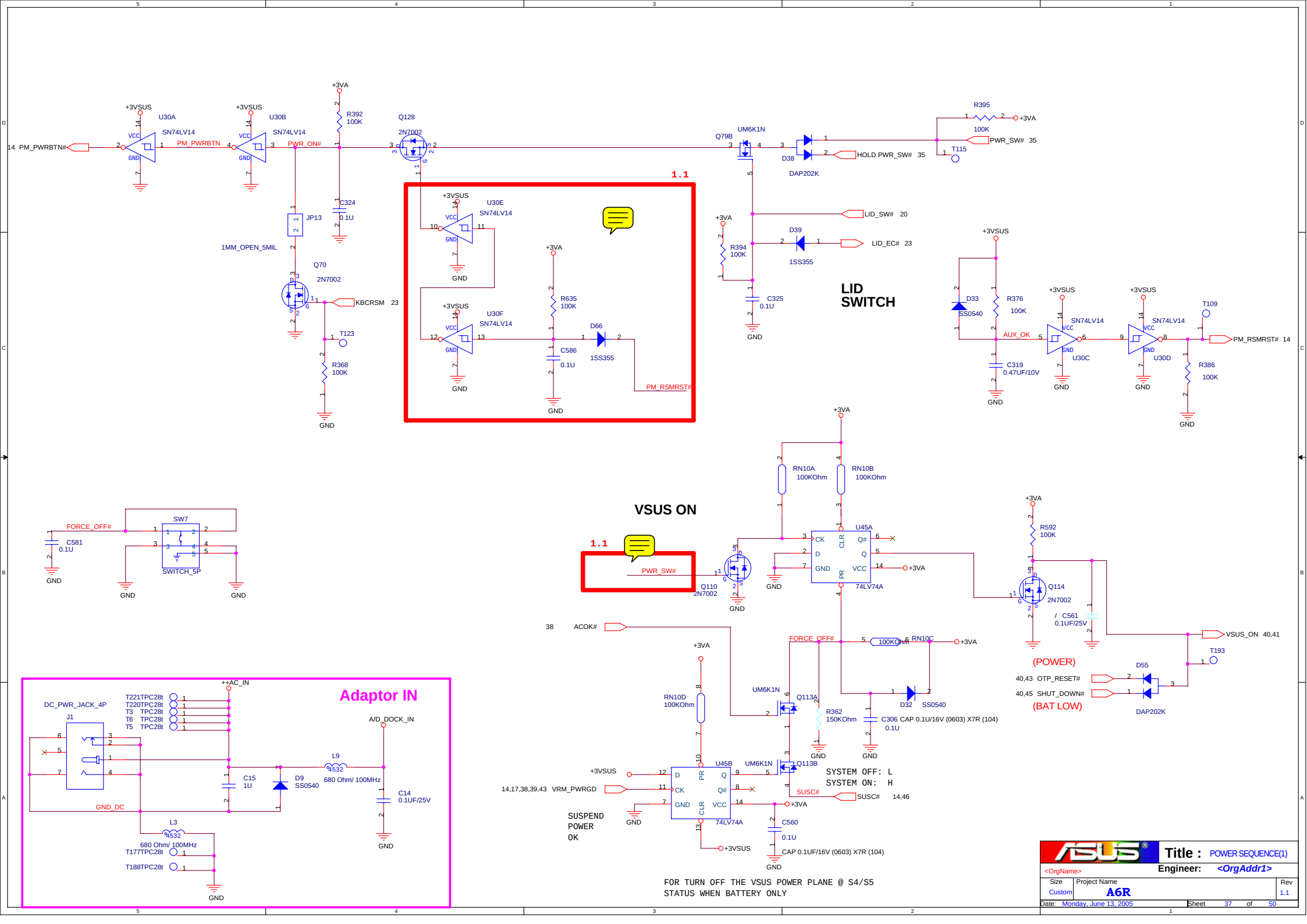


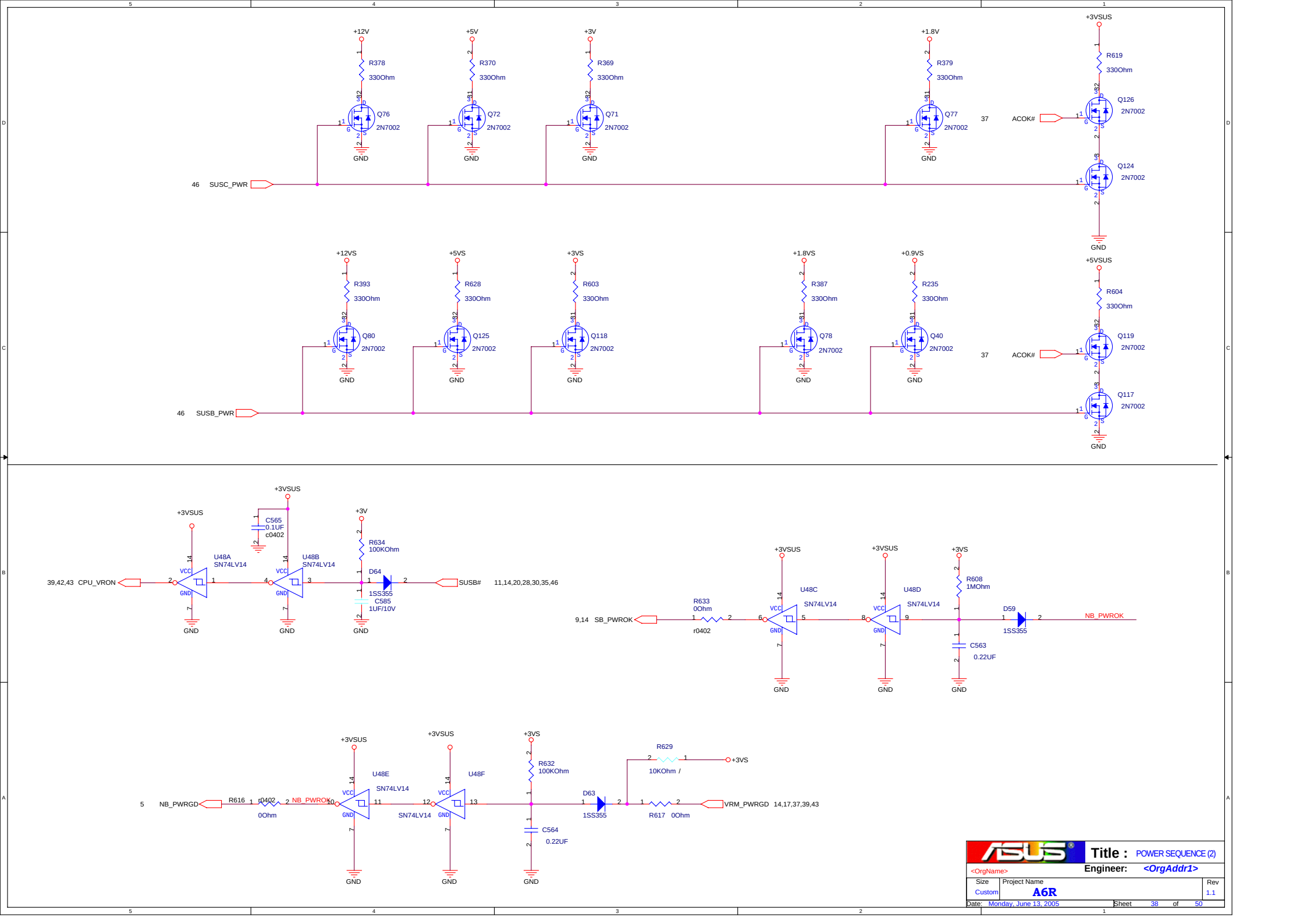


ASUS	Title : FUNCTION KEY & DJ	
<OrgName>	Engineer: <OrgAddr1>	
Size: Custom	Project Name: A6R	Rev: 1.1
Date: Monday, June 13, 2005	Sheet 35 of 50	

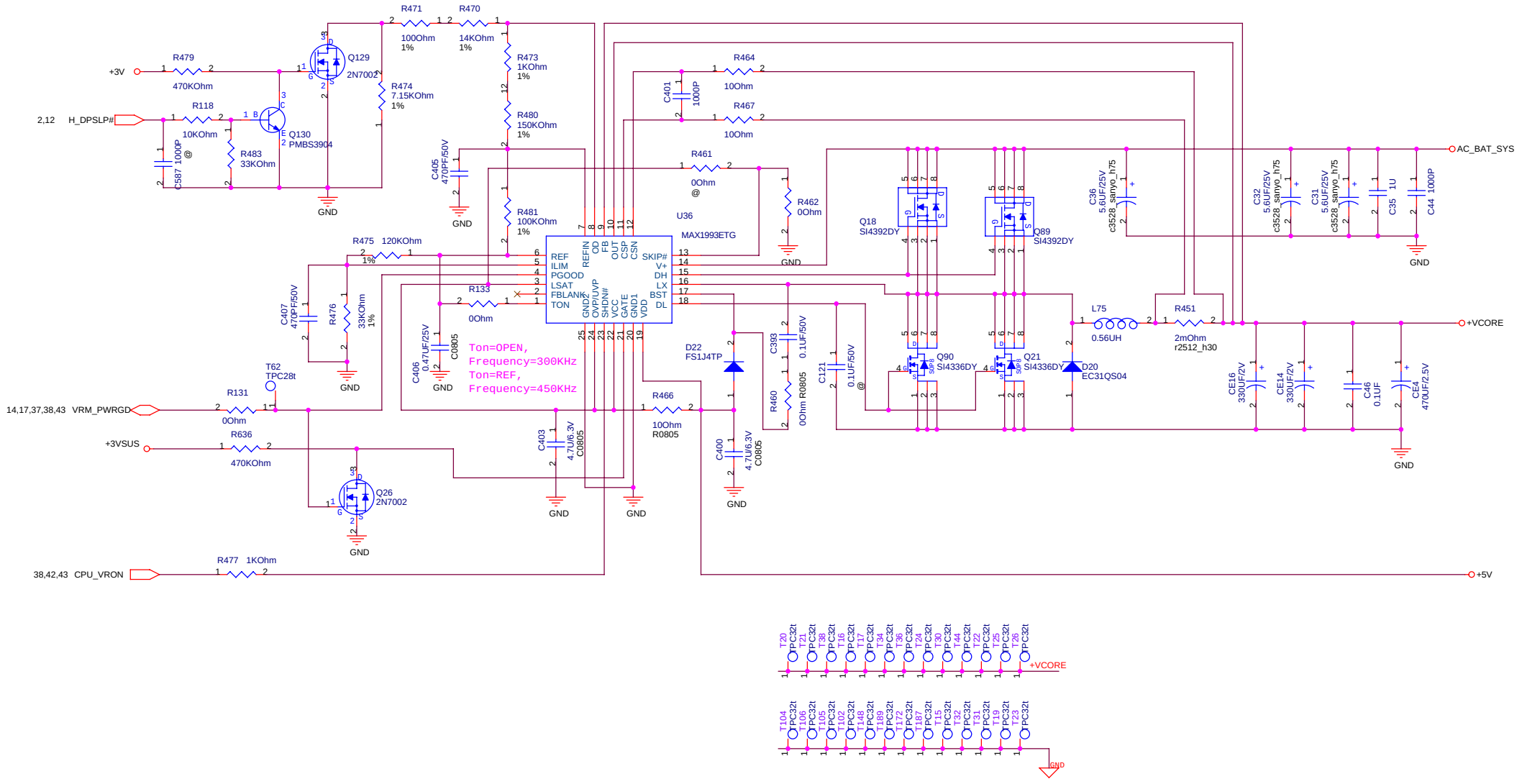


ASUS	Title : LED	
<OrgName>	Engineer: <OrgAddr1>	
Size: Custom	Project Name: A6R	Rev: 1.1
Date: Monday, June 13, 2005	Sheet 36 of 50	

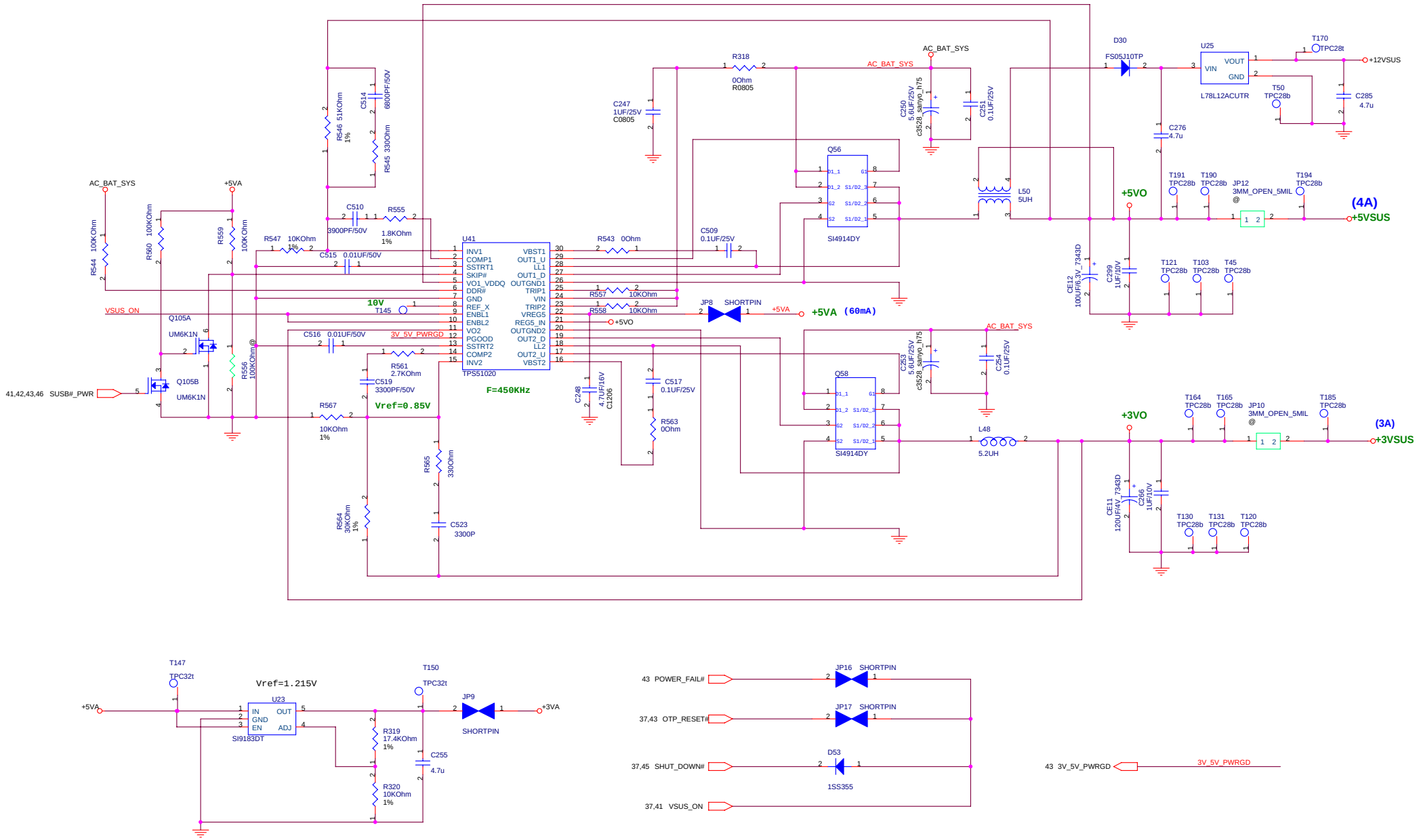

14 PM_PWRBTN#
U30A
SN74LV14
PM_PWRBTN
U30B
PWR_ON#
R392 100K
Q128
2N7002
C324 0.1U
JP13
1MM_OPEN_5MIL
Q70
2N7002
KBCRSM 23
T123
R368 100K
GND
1.1
U30E
U30F
R635 100K
D66
1SS355
C586 0.1U
PM_RSMRST#
Q79B
UM6K1N
D38
DAP202K
HOLD PWR_SW# 35
R395 100K
PWR_SW# 35
T115
LID_SW# 20
LID_EC# 23
D39
1SS355
R394 100K
C325 0.1U
LID SWITCH
D33
SS0540
R376 100K
AUX_OK
C319 0.47UF/10V
U30C
U30D
T109
R386 100K
PM_RSMRST# 14
FORCE_OFF#
SW7
SWITCH_5P
C581 0.1U
VSUS ON
PWR_SW#
Q110
2N7002
RN10A 100KOhm
RN10B 100KOhm
U45A
74LV74A
R592 100K
Q114
2N7002
/ C561 0.1UF/25V
VSUS_ON 40,41
T193
(POWER)
40,43 OTP_RESET#
40,45 SHUT_DOWN#
(BAT LOW)
D55
DAP202K
38 ACOK#
RN10C 100KOhm
RN10D 100KOhm
Q113A
Q113B
UM6K1N
R362 150KOhm
C306 CAP 0.1U/16V (0603) X7R (104) 0.1U
D32 SS0540
U45B
14,17,38,39,43 VRM_PWRGD
SUSC#
SUSC# 14,46
SYSTEM OFF: L
SYSTEM ON: H
SUSPEND POWER OK
C560 0.1U
CAP 0.1UF/16V (0603) X7R (104)
FOR TURN OFF THE VSUS POWER PLANE @ S4/S5
STATUS WHEN BATTERY ONLY
Adaptor IN
++AC_IN
DC_PWR_JACK_4P
J1
T221TPC28t
T220TPC28t
T3 TPC28t
T6 TPC28t
T5 TPC28t
C15 1U
D9 SS0540
L9 680 Ohm/ 100MHz
A/D_DOCK_IN
C14 0.1UF/25V
GND_DC
L3 680 Ohm/ 100MHz
T177TPC28t
T188TPC28t
Title : POWER SEQUENCE(1)
Engineer: <OrgAddr1>
<OrgName>
Size Custom
Project Name A6R
Rev 1.1
Date: Monday, June 13, 2005
Sheet 37 of 50



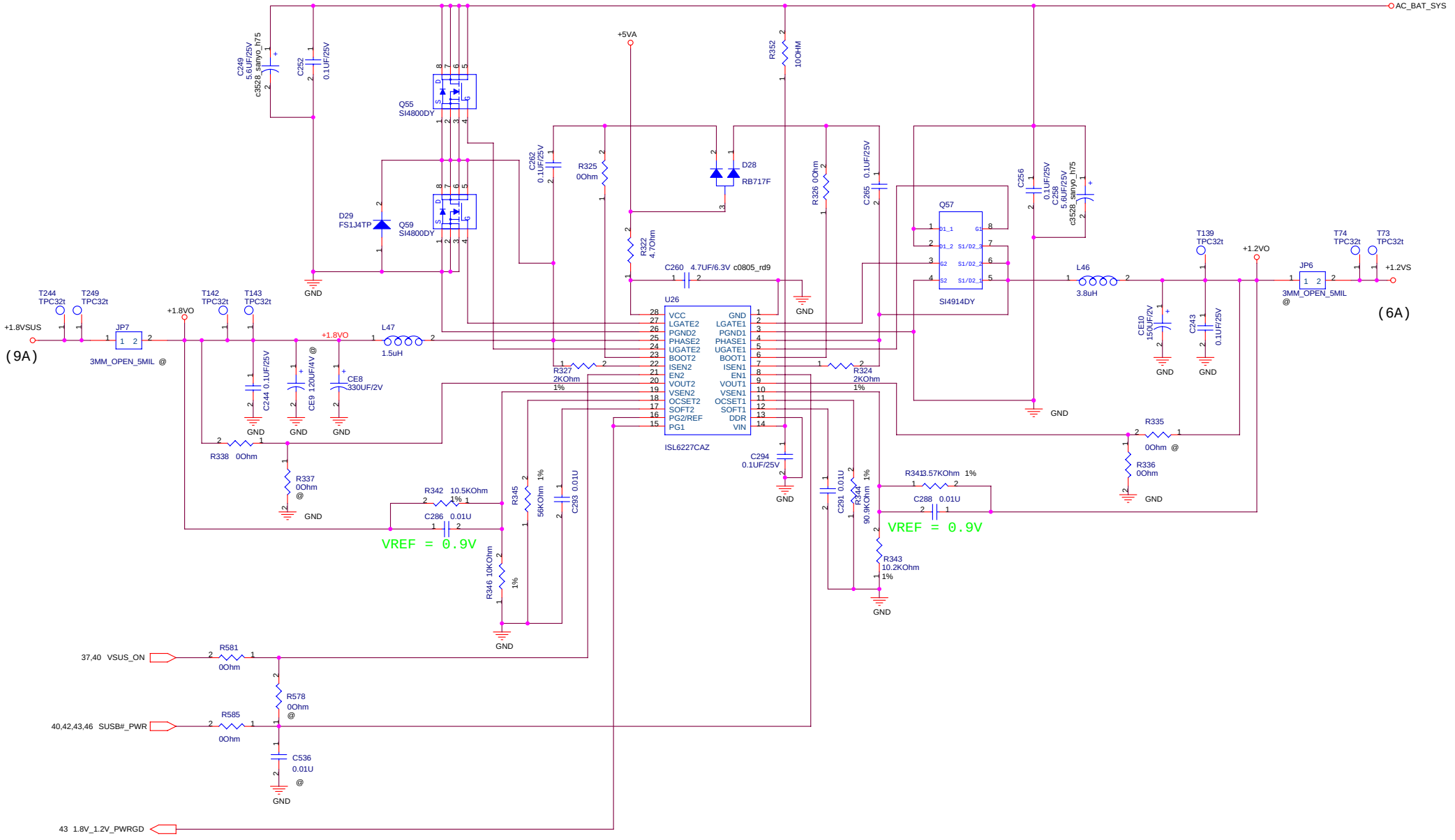
<OrgName>	Title : POWER SEQUENCE (2)	
	Engineer: <OrgAddr1>	
Size: Custom	Project Name: A6R	Rev: 1.1
Date: Monday, June 13, 2005	Sheet 38 of 50	



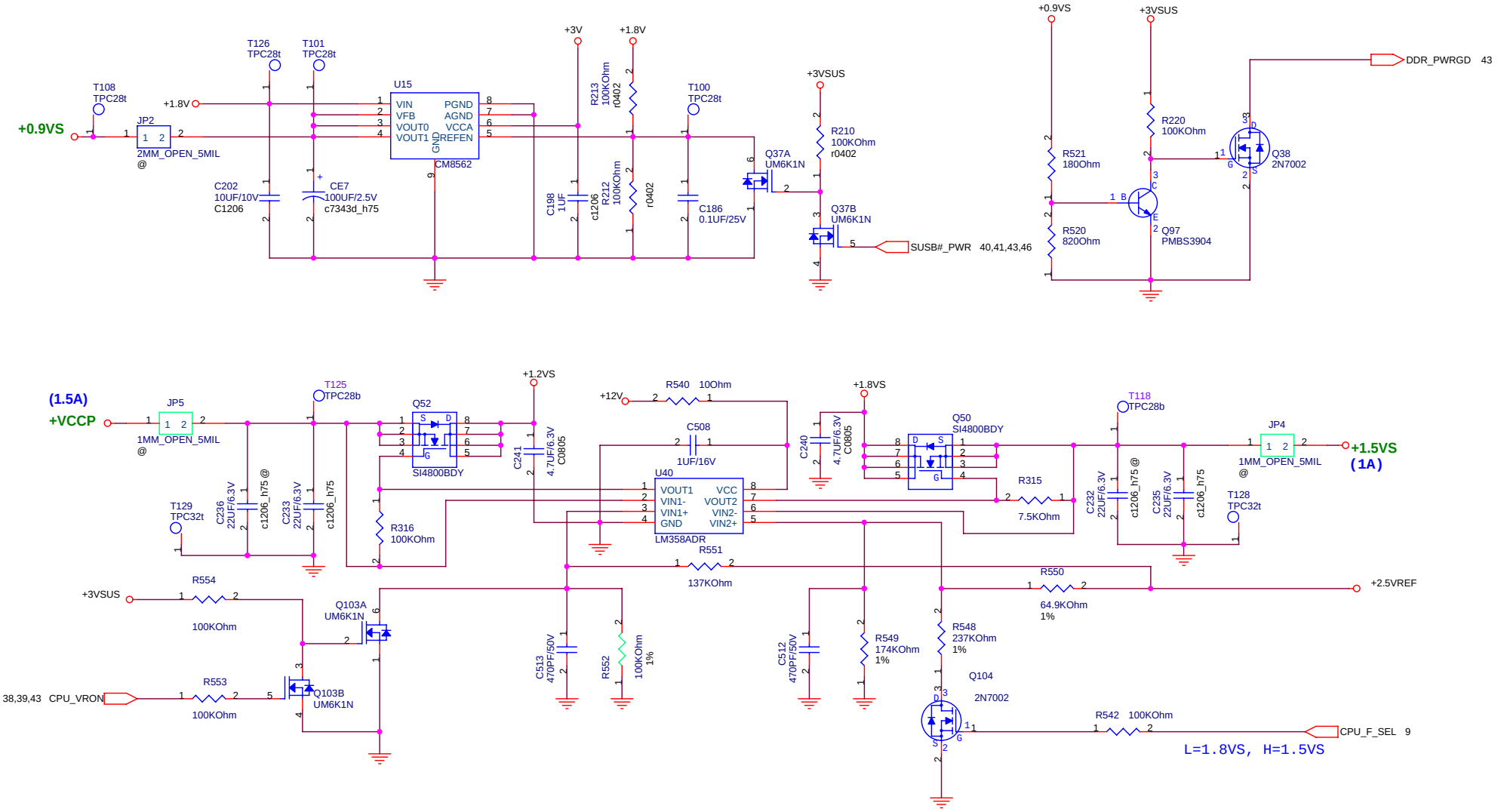
ASUS	Title : VCORE	
<OrgName>	Engineer: <OrgAddr1>	
Size: Custom	Project Name: A6R	Rev: 1.1
Date: Monday, June 13, 2005	Sheet 39 of 50	



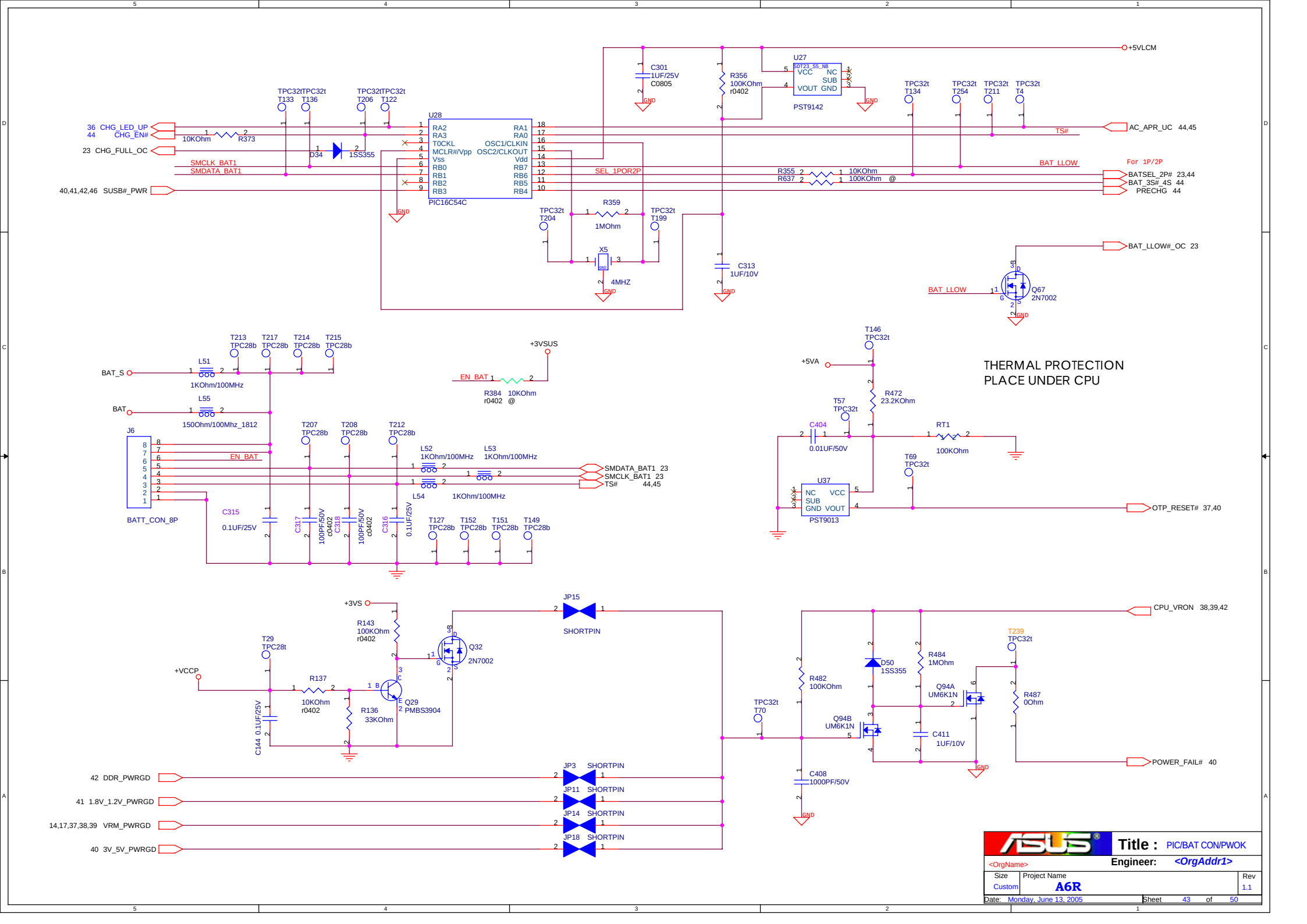
ASUS	Title :	SYSTEM_+5VA & +3VA
<OrgName>	Engineer:	<OrgAddr1>
Size: Custom	Project Name: A6R	Rev: 1.1
Date: Monday, June 13, 2005	Sheet 40 of 50	

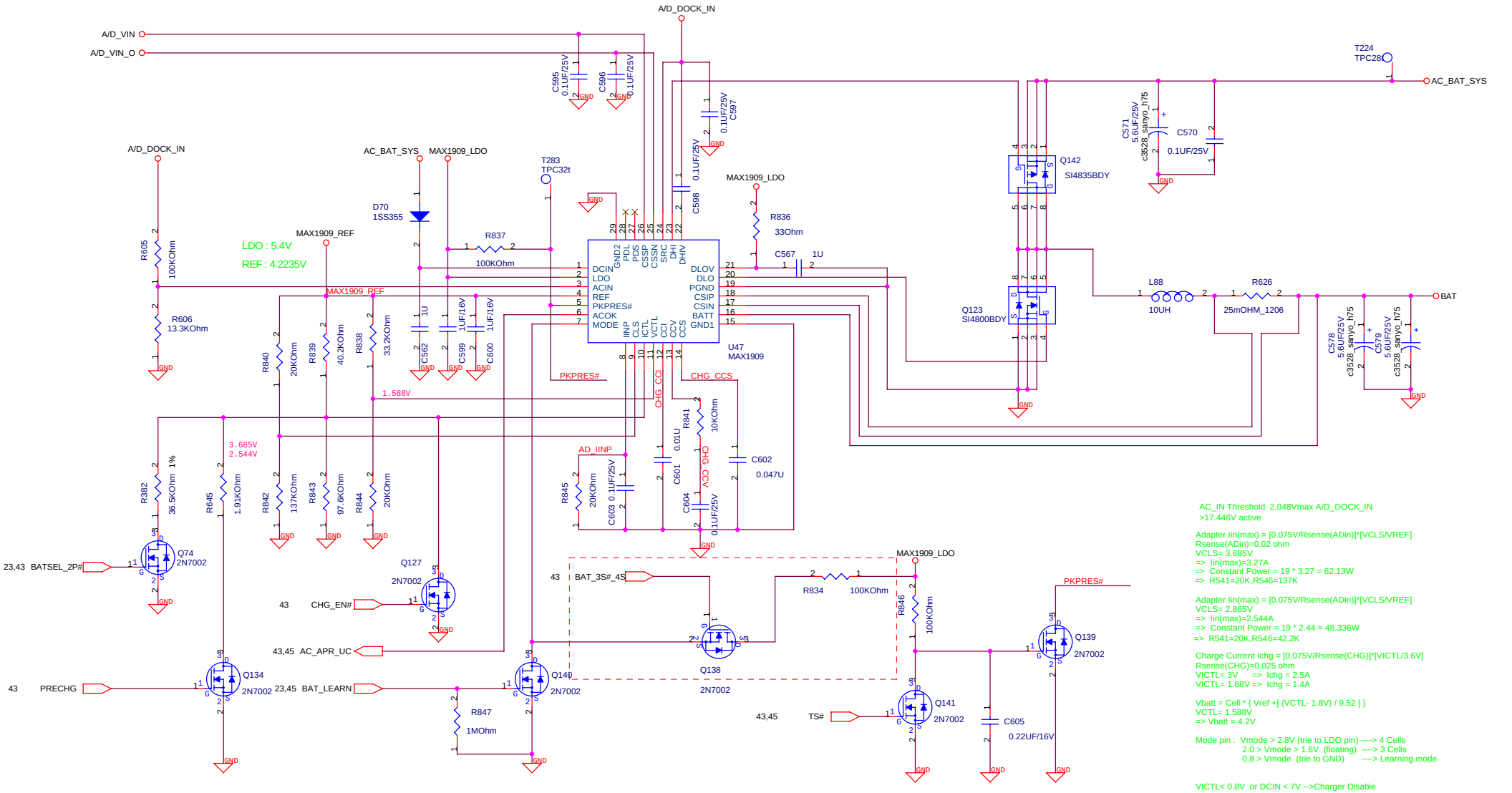


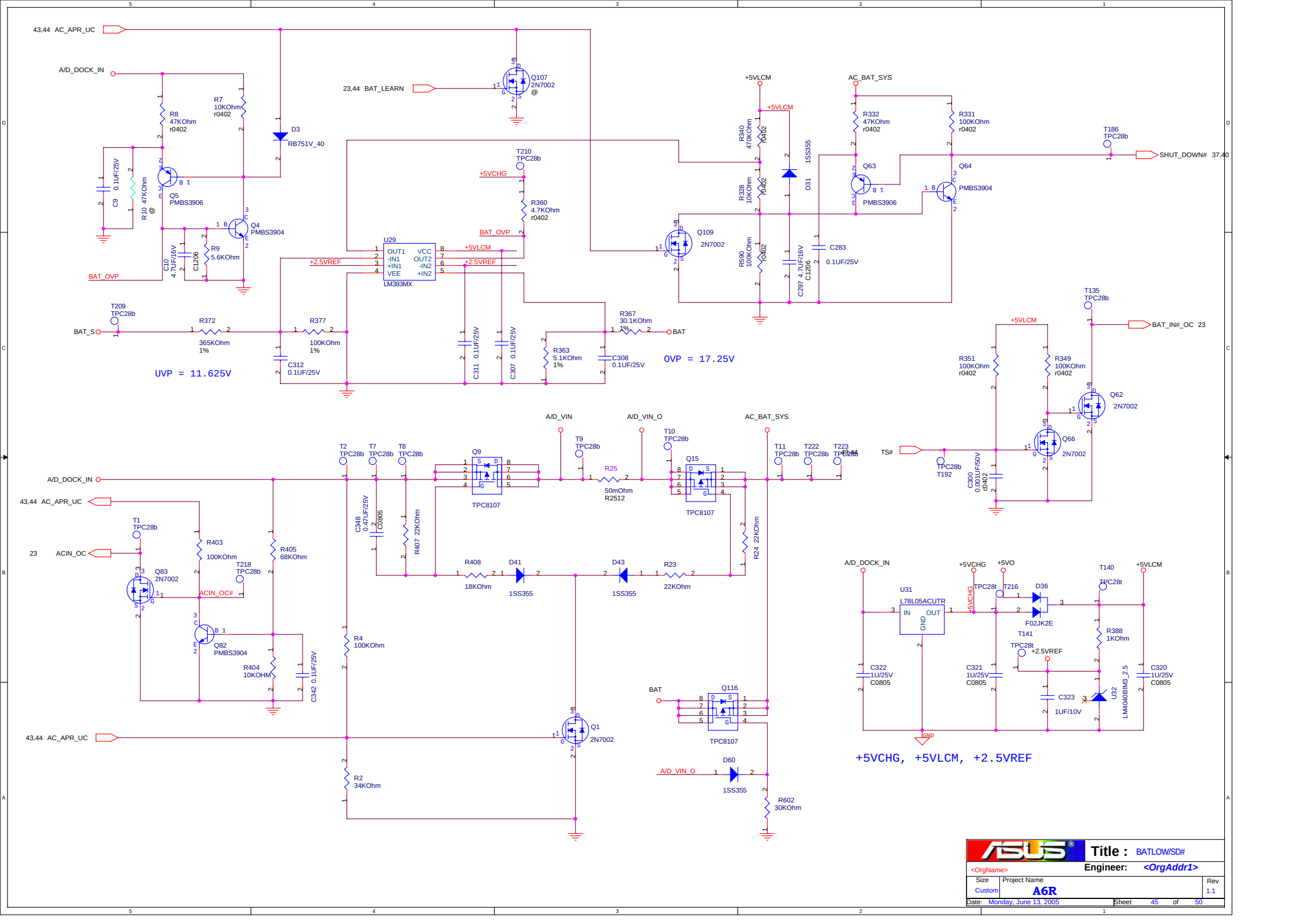
ASUS	Title : 1.8V&1.2VS		
<OrgName>	Engineer: <OrgAddr1>		
Size: Custom	Project Name: A6R		Rev: 1.1
Date: Monday, June 13, 2005	Sheet 41 of 50		



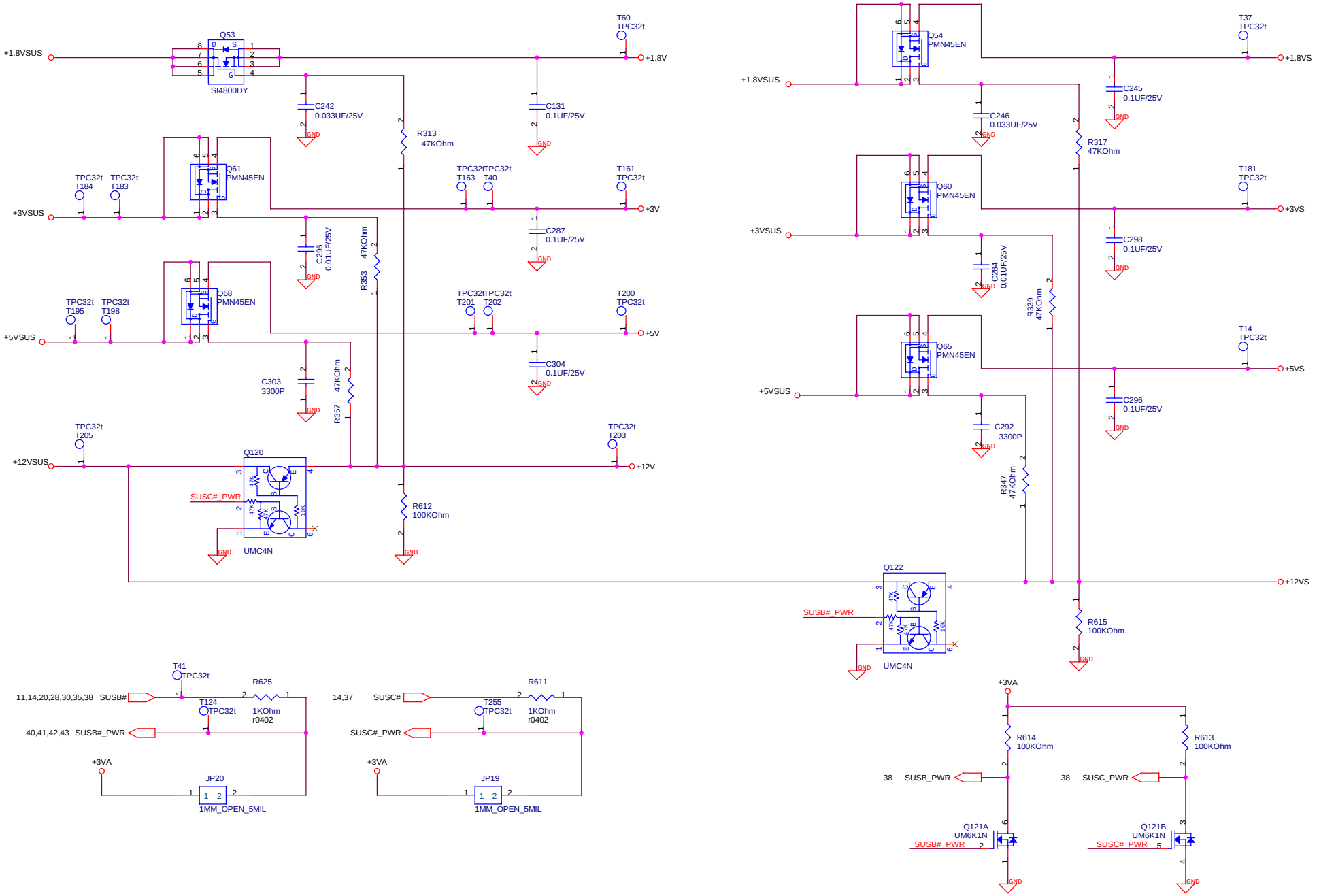
Title : 1.05VA & +0.9VS		
<OrgName>	Engineer: <OrgAddr1>	
Size: B	Project Name: A6R	Rev: 1.1
Date: Monday, June 13, 2005	Sheet 42 of 50	


+5VLCM
C301
1UF/25V
C0805
R356
100KOhm
r0402
U27
PST9142
TPC32t T134
TPC32t T254
TPC32t T211
TPC32t T4
36 CHG_LED_UP
44 CHG_EN#
10KOhm
R373
23 CHG_FULL_OC
D34
1SS355
SMCLK_BAT1
SMDATA_BAT1
40,41,42,46 SUSB#_PWR
U28
PIC16C54C
TS#
AC_APR_UC 44,45
BAT_LLOW
For 1P/2P
SEL_1POR2P
R355 10KOhm
R637 100KOhm @
BATSEL_2P# 23,44
BAT_3S#_4S 44
PRECHG 44
R359
1MOhm
X5
4MHZ
C313
1UF/10V
BAT_LLOW#_OC 23
Q67
2N7002
BAT_S
L51
1KOhm/100MHz
BAT
L55
150Ohm/100Mhz_1812
J6
BATT_CON_8P
EN_BAT
+3VSUS
R384 10KOhm
r0402 @
L52 1KOhm/100MHz
L53 1KOhm/100MHz
L54 1KOhm/100MHz
SMDATA_BAT1 23
SMCLK_BAT1 23
TS# 44,45
C315
0.1UF/25V
C317 100PF/50V c0402
C318 100PF/50V c0402
C316 0.1UF/25V
T127 TPC28b
T152 TPC28b
T151 TPC28b
T149 TPC28b
THERMAL PROTECTION
PLACE UNDER CPU
+5VA
R472
23.2KOhm
C404
0.01UF/50V
RT1
100KOhm
T57 TPC32t
T69 TPC32t
U37
PST9013
OTP_RESET# 37,40
+3VS
R143
100KOhm
r0402
Q32
2N7002
JP15
SHORTPIN
T29 TPC28t
+VCCP
R137
10KOhm
r0402
R136
33KOhm
Q29
PMBS3904
C144 0.1UF/25V
42 DDR_PWRGD
41 1.8V_1.2V_PWRGD
14,17,37,38,39 VRM_PWRGD
40 3V_5V_PWRGD
JP3 SHORTPIN
JP11 SHORTPIN
JP14 SHORTPIN
JP18 SHORTPIN
TPC32t T70
R482
100KOhm
D50
1SS355
R484
1MOhm
Q94A
UM6K1N
Q94B
UM6K1N
C411
1UF/10V
C408
1000PF/50V
T239 TPC32t
R487
0Ohm
CPU_VRON 38,39,42
POWER_FAIL# 40
Title : PIC/BAT CON/PWOK
<OrgName>
Engineer: <OrgAddr1>
Size Custom
Project Name A6R
Rev 1.1
Date: Monday, June 13, 2005
Sheet 43 of 50

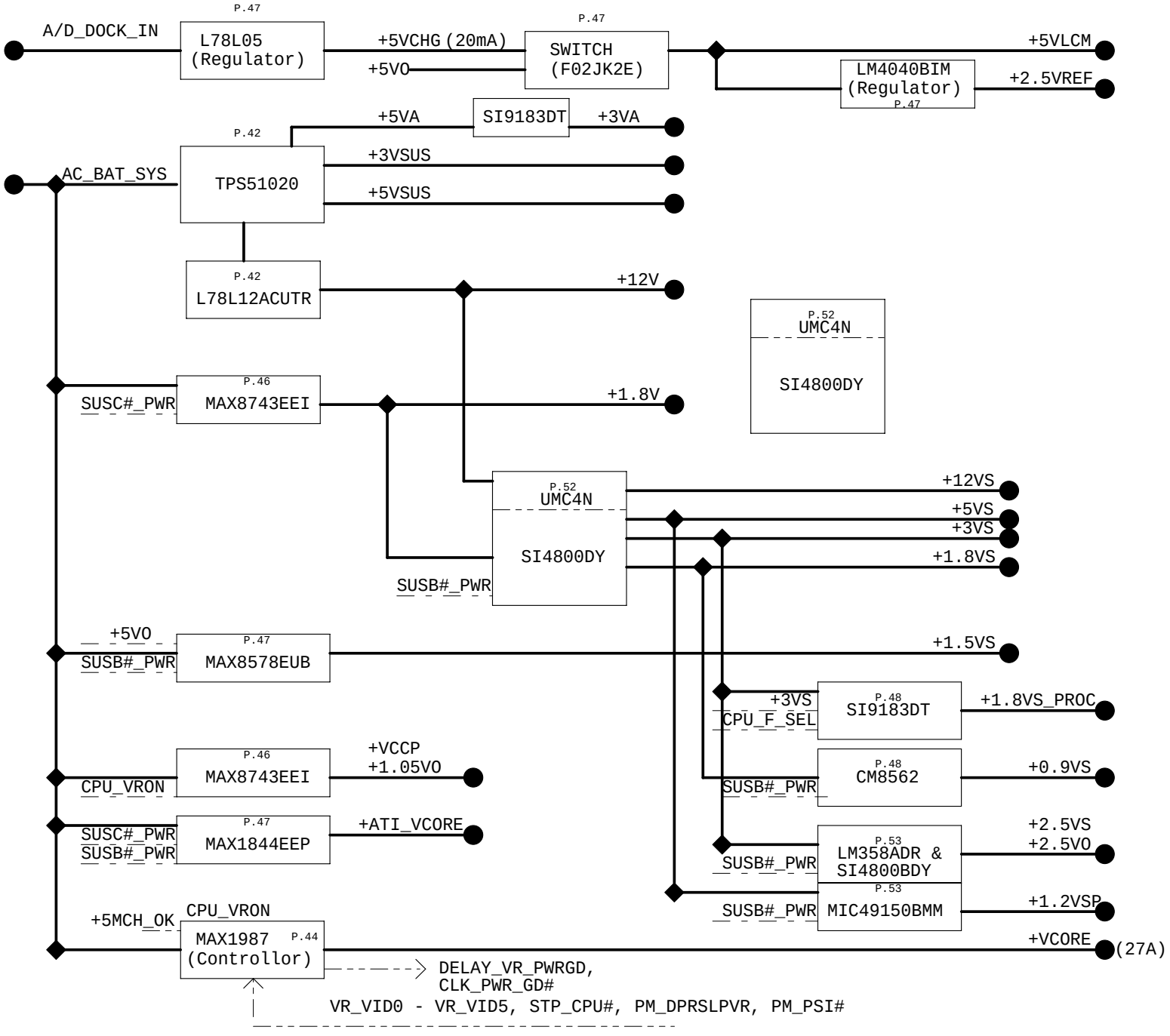

A/D_VIN
A/D_VIN_O
A/D_DOCK_IN
C595 0.1UF/25V
C596 0.1UF/25V
C597 0.1UF/25V
C598 0.1UF/25V
T224 TPC28
AC_BAT_SYS
C571 5.6UF/25V c3528_sanyo_h75
C570 0.1UF/25V
Q142 SI4835BDY
AC_BAT_SYS
MAX1909_LDO
T283 TPC32t
D70 1SS355
R837 100KOhm
MAX1909_REF
LDO : 5.4V
REF : 4.2235V
R836 33Ohm
C567 1U
R605 100KOhm
R606 13.3KOhm
MAX1909_REF
DCIN
LDO
ACIN
REF
PKPRES#
ACOK
MODE
GND2
PDL
PDS
CSSP
CSSN
SRC
DHI
DHV
DLOV
DLO
PGND
CSIP
CSIN
BATT
GND1
U47 MAX1909
Q123 SI4800BDY
L88 10UH
R626 25mOHM_1206
BAT
C578 5.6UF/25V c3528_sanyo_h75
C579 5.6UF/25V c3528_sanyo_h75
R840 20KOhm
R839 40.2KOhm
R838 33.2KOhm
C562 1U
C599 1UF/16V
C600 1UF/16V
1.588V
PKPRES#
CHG_CCI
CHG_CCS
R841 10KOhm
C601 0.01U
C602 0.047U
CHG_CCV
C604 0.1UF/25V
AD_IINP
R845 20KOhm
C603 0.1UF/25V
3.685V
2.544V
R382 36.5KOhm 1%
R645 1.91KOhm
R842 137KOhm
R843 97.6KOhm
R844 20KOhm
23,43 BATSEL_2P#
Q74 2N7002
Q127 2N7002
43 CHG_EN#
43,45 AC_APR_UC
43 PRECHG
Q134 2N7002
23,45 BAT_LEARN
Q140 2N7002
R847 1MOhm
43 BAT_3S#_4S
MAX1909_LDO
R834 100KOhm
R846 100KOhm
Q138 2N7002
PKPRES#
Q139 2N7002
43,45 TS#
Q141 2N7002
C605 0.22UF/16V
AC_IN Threshold 2.048Vmax A/D_DOCK_IN
>17.446V active
Adapter Iin(max) = [0.075V/Rsense(ADin)]*[VCLS/VREF]
Rsense(ADin)=0.02 ohm
VCLS= 3.685V
=> Iin(max)=3.27A
=> Constant Power = 19 * 3.27 = 62.13W
=> R541=20K,R546=137K
Adapter Iin(max) = [0.075V/Rsense(ADin)]*[VCLS/VREF]
VCLS= 2.865V
=> Iin(max)=2.544A
=> Constant Power = 19 * 2.44 = 48.336W
=> R541=20K,R546=42.2K
Charge Current Ichg = [0.075V/Rsense(CHG)]*[VICTL/3.6V]
Rsense(CHG)=0.025 ohm
VICTL= 3V => Ichg = 2.5A
VICTL= 1.68V => Ichg = 1.4A
Vbatt = Cell * { Vref +[(VCTL- 1.8V) / 9.52] }
VCTL= 1.588V
=> Vbatt = 4.2V
Mode pin : Vmode > 2.8V (trie to LDO pin) ----> 4 Cells
2.0 > Vmode > 1.6V (floating) ----> 3 Cells
0.8 > Vmode (trie to GND) ----> Learning mode
VICTL< 0.8V or DCIN < 7V -->Charger Disable
Title : CHARGE
<OrgName>
Engineer: <OrgAddr1>
Size Custom
Project Name A6R
Rev 1.1
Date: Monday, June 13, 2005
Sheet 44 of 50



ASUS	Title : BATLOW/SD#	
<OrgName>	Engineer: <OrgAddr1>	
Size: Custom	Project Name: A6R	Rev: 1.1
Date: Monday, June 13, 2005	Sheet 45 of 50	



<OrgName>	Title : LOAD SWITCH	
	Engineer: <OrgAddr1>	
Size: Custom	Project Name: A6R	Rev: 1.1
Date: Monday, June 13, 2005	Sheet 46 of 50	



ASUS	Title : POWER BLOCK DIAGRAM		
<OrgName>	Engineer: <OrgAddr1>		
Size: Custom	Project Name: A6R		Rev: 1.1
Date: Monday, June 13, 2005	Sheet 47 of 50		

PCI Device	IDSEL#	REQ/GNT#	Interrupts
10/100 LAN	AD16	0	E
CARD READER	AD17	1	C
CARDBUS	AD17	1	A
1394	AD17	1	B
MINIPCI (802.11a/b/g)	AD19	3	G,H

SM-Bus Device	SM-Bus Address
Clock Generator	1101001x (D2)
SO-DIMM 0	1010000x (A0)
SO-DIMM 1	1010001x (A2)
Thermal Sensor	0101110x (5C)
PIC	1001001x (92)

SB400 GPIO TABLE

GPIO	TYPE	POWER DOMAIN	FUNCTION
GPIO 0	I/OD	S0	
GPIO 1	I/O	S0	
GPIO 2	I/O	S0	SB_SPKR
GPIO 3	I/O	S0	FWH_WP#
GPIO 4	I/O	S0	PCB_ID0
GPIO 5	I/O	S0	PCB_ID1
GPIO 6	I/OD	S0	PCB_ID2
GPIO 7	I/O	S0	VRM_PWRGD
GPIO 8	I/O	S0	CB_SD#
GPIO 9	I/O	S0	BACK_OFF#
GPIO 10	I/O	S5	SB_PM_THERM#
GPIO 11	I/O	S0	802_LED_EN
GPIO 12	I/O	S0	WLAN_ON#
GPIO 13	I/O	S0	
GPIO 14	I/O	S0	PCI_GNT#5
GPIO 31	I/O	S0	
GPIO 32	I/O	S0	PCI_GNT#6
GPIO 33	I/O	S0	PCI_INTE#
GPIO 34	I/O	S0	PCI_INTF#
GPIO 35	I/O	S0	PCI_INTG#
GPIO 36	I/O	S0	PCI_INTH#
GPM 0	I	S5	
GPM 1	I	S5	
GPM 2	I/O	S5	
GPM 3	I	S5	
GPM 4	I	S5	
GPM 5	I	S5	
GPM 6	I/OD	S5	PWRLED_1HZ
GPM 7	I	S5	SYS_RESET#
GEVENT 0	I	S5	
GEVENT 1	I	S0	
GEVENT 2	I	S5	THRMTRIP#
GEVENT 3	I	S5	LPC_PME#
GEVENT 4	I	S5	PCI_PME#
GEVENT 5	I	S5	H_PROCHOT#
GEVENT 6	I	S5	
GEVENT 7	I	S5	
GEVENT 8			KB_SCI
EXTEVENT#0			EXT_SMI#
EXTEVENT#1			SIO_SMI#

KBC GPIO	W1V	Note
P23(Pin 35)	CHG_FULL_OC	
P22(Pin 36)	BAT_LEARN	
P21(Pin 37)	LID_EC#	
P20(Pin 38)	KBCRSM	
P42(Pin 23)		
P43(Pin 22)	OP_SD#	
P44(Pin 21)	KB_CPURST	
P45(Pin 20)	KB_GATEA20	
P46(Pin 19)	KBCSCI#	
P47(Pin 18)	PM_CLKRUN#	
P50(Pin 17)	BAT_LLOW#_OC	
P51(Pin 16)	KID0	
P52(Pin 15)	KID1	
P53(Pin 14)	CLR_DJ#	
P54(Pin 13)	BAT_SEL#	
P55(Pin 12)	BAT1_IN#_OC	
P56(Pin 11)		
P57(Pin 10)	INV_DA	
P67(Pin 74)	DJ_LED#	
P66(Pin 75)	SWDJ_EN#	
P65(Pin 76)	GAIN_AMP_K#	0->-6 V/V 1->NORMAL
P64(Pin 77)	ACIN_OC	
P63(Pin 78)	DISTP#	
P62(Pin 79)	MARATHON#	
P61(Pin 80)	INTERNET#	
P60(Pin 1)	EMAIL#	
P75(Pin 4)	KB_CLK	
P74(Pin 5)	MS_CLK	
P73(Pin 6)	TPAD_CLK	
P72(Pin 7)	KB_DAT	
P71(Pin 8)	MS_DAT	
P70(Pin 9)	TPAD_DAT	
P77(Pin 2)	SMC_BAT	
P76(Pin 3)	SMD_BAT	
P27(Pin 31)	SCROLL_LED#	
P26(Pin 32)	NUM_LED#	
P25(Pin 33)	CAP_LED#	
P24(Pin 34)	SET_PLTRSTNS#	
P40(Pin 27)	EXT_SMI	
P41(Pin 26)	EMAIL_LED#	

ASUS

Title : SYSTEM RESOURCE

<OrgName>

Engineer: <OrgAddr1>

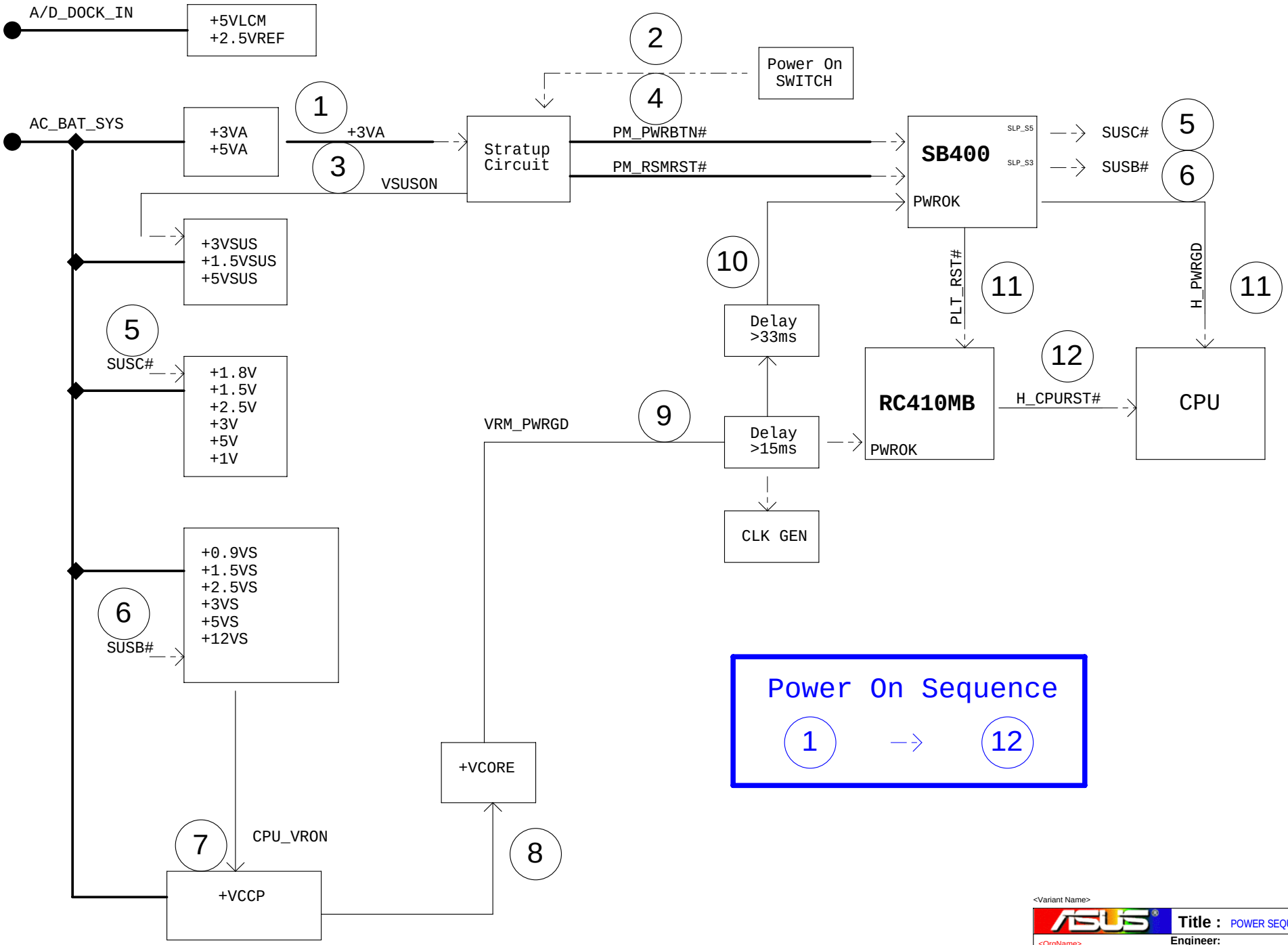
Size	Project Name	Rev
Custom	A6R	1.1

Date: Monday, June 13, 2005 Sheet 48 of 50

Rev	Date	Description
1.0	05/03/01	1. Initial release.

Rev	Date	Description

ASUS	Title :	HISTORY
<OrgName>	Engineer:	*<OrgAddr1>*
Size: Custom	Project Name: **A6R**	Rev: 1.1
Date: Monday, June 13, 2005	Sheet 49 of 50	



<Variant Name>

Title : POWER SEQUENCY

<OrgName>

Engineer:

Size	Project Name	Rev
Custom	A6R	1.1

Date: Monday, June 13, 2005 Sheet 50 of 50