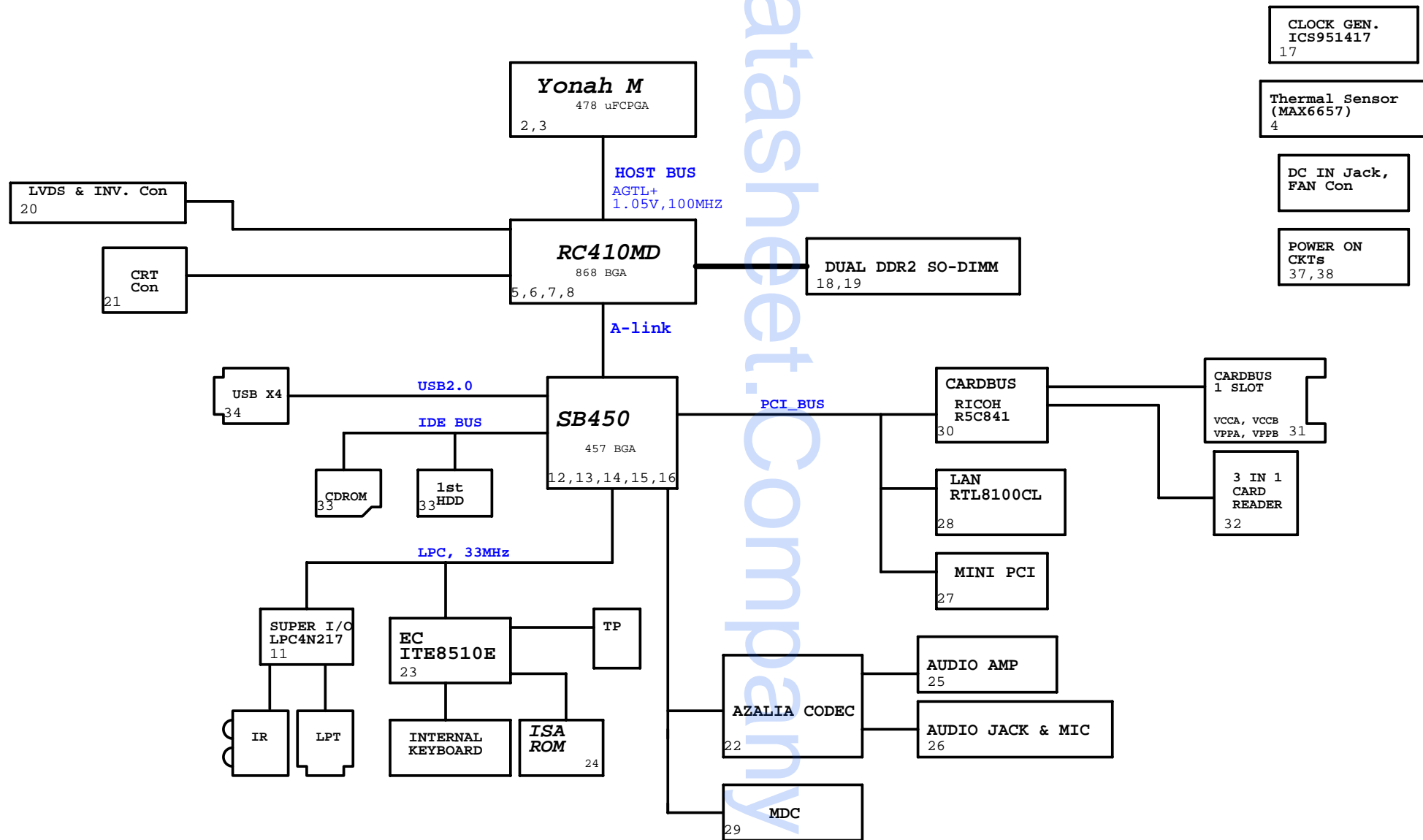
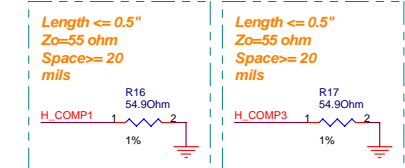
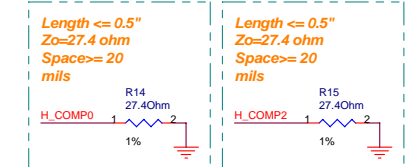
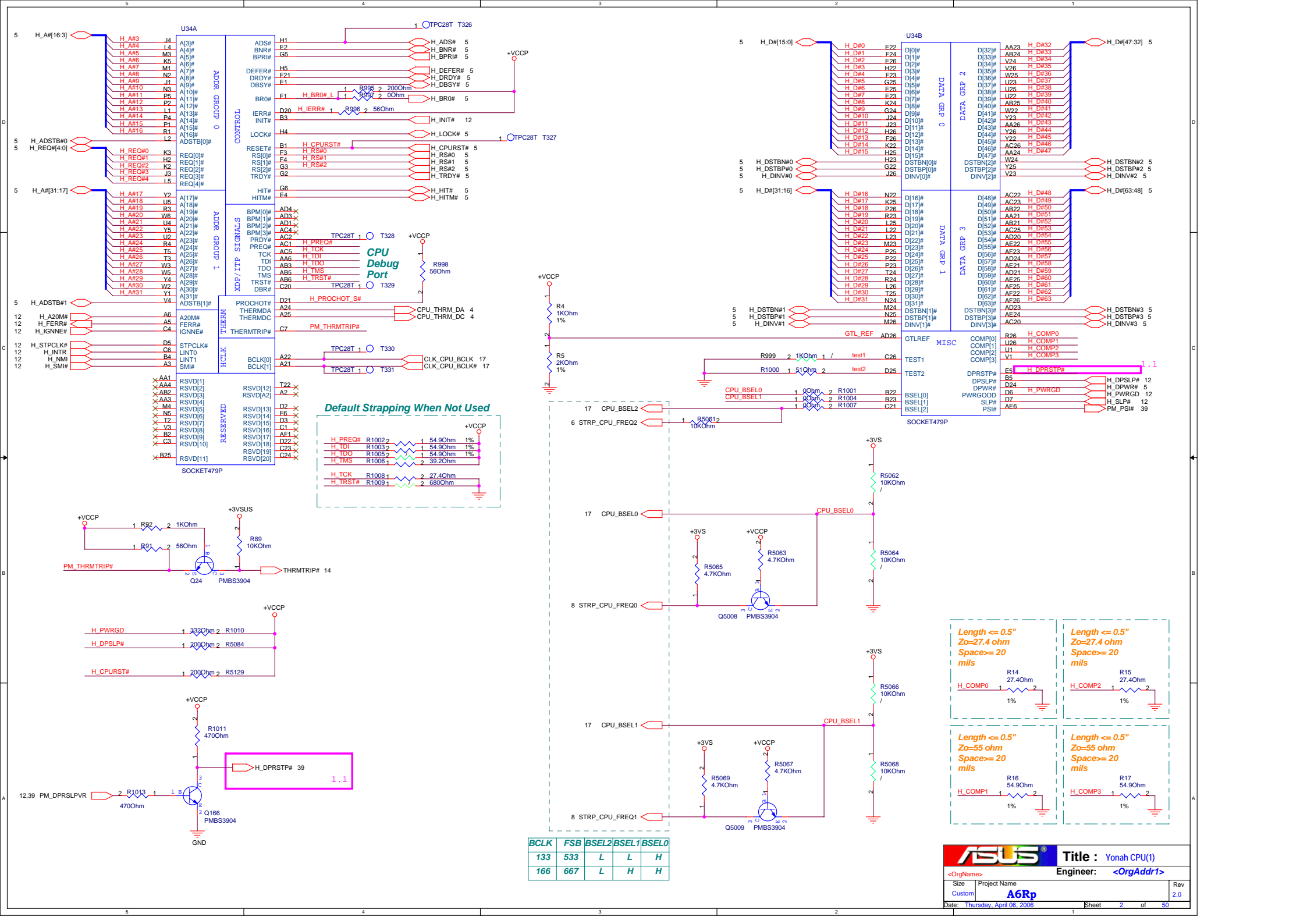
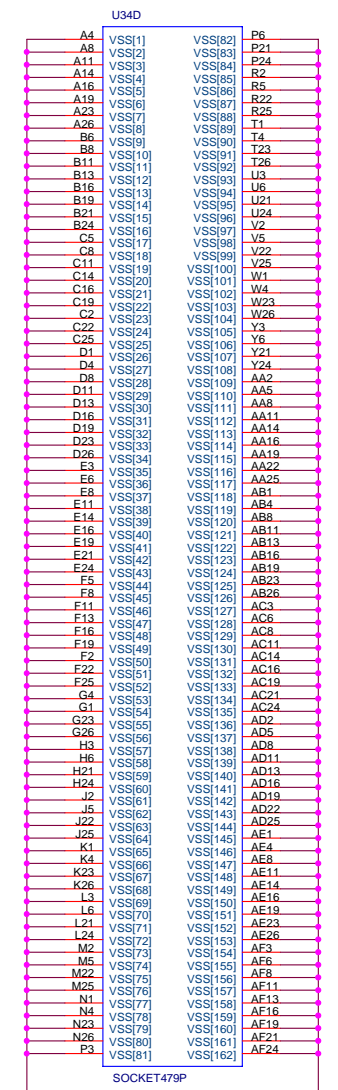
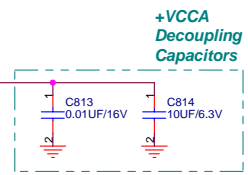
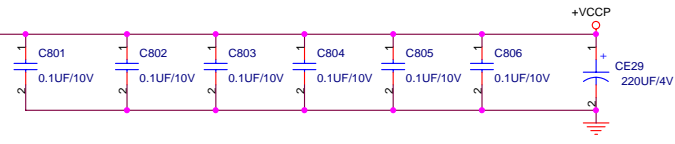
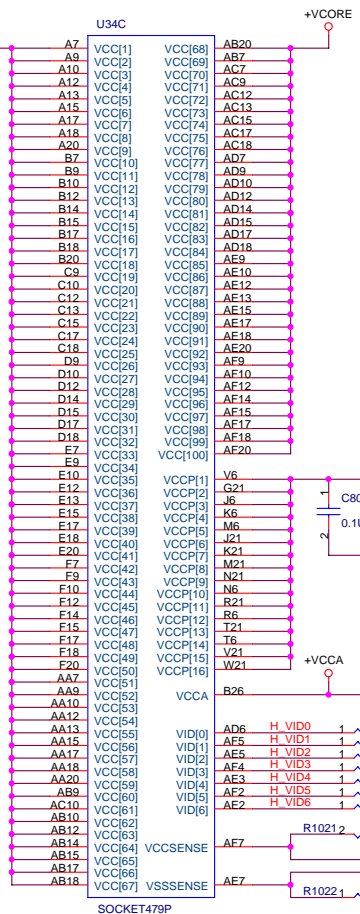
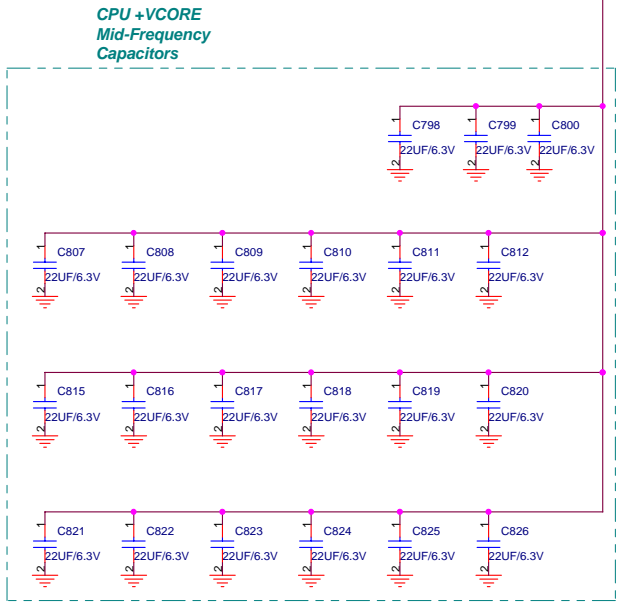
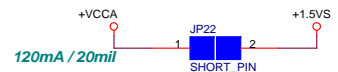
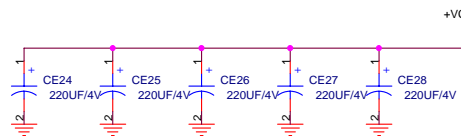


Yonah/RC410MD/IXP450 BLOCK DIAGRAM





BCLK	FSB	BSEL2	BSEL1	BSEL0
133	533	L	L	H
166	667	L	H	H



+VCCORE Low-Freq Capacitor
 Intel: 330UF *6
 ATI: 330UF *6
 R1F: 330UF *4
 A7J: 330UF *5

+VCCORE Mid-Frequency Capacitor
 Intel: 22UF *32
 ATI: 10UF *26
 R1F: 22UF *16
 A7J: 22UF*29 use 19
 A6RF: 22UF*21 use 21

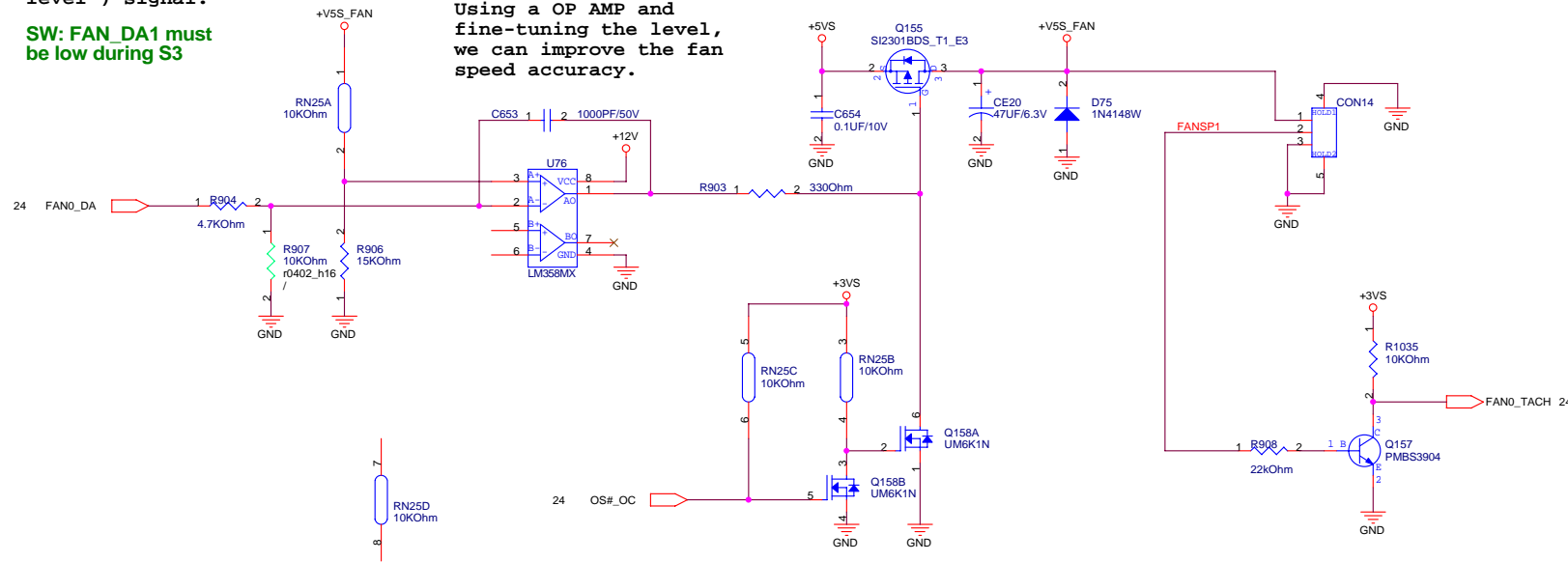
+VCCP Decoupling Capacitor
 Intel: 270UF *1, 0.1UF *6
 R1F: 220UF *1, 0.1UF *4
 A7J: 220UF *1, 0.1UF *6
 A6RF: 220UF *1, 0.1UF *6

Fan Speed Control

KBC will issue a analog (a voltage level) signal.

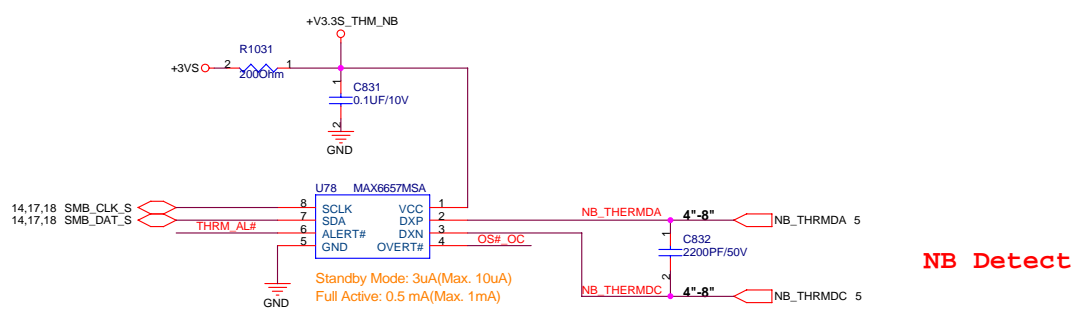
SW: FAN_DA1 must be low during S3

Using a OP AMP and fine-tuning the level, we can improve the fan speed accuracy.

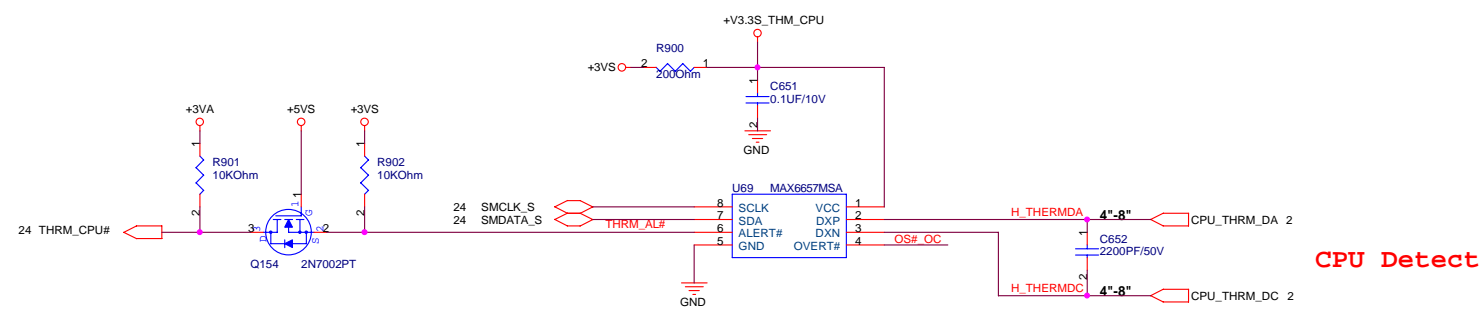


Route H_THERMDA and H_THERMDC on the same layer

- OTHER SIGNALS
 - 12 mils
 - =====GND
 - 10 mils
 - =====H_THERMDA(10 mils)
 - 10 mils
 - =====H_THERMDC(10 mils)
 - 10 mils
 - =====GND
 - 12 mils
 - OTHER SIGNALS
- Avoid BPSB,Power

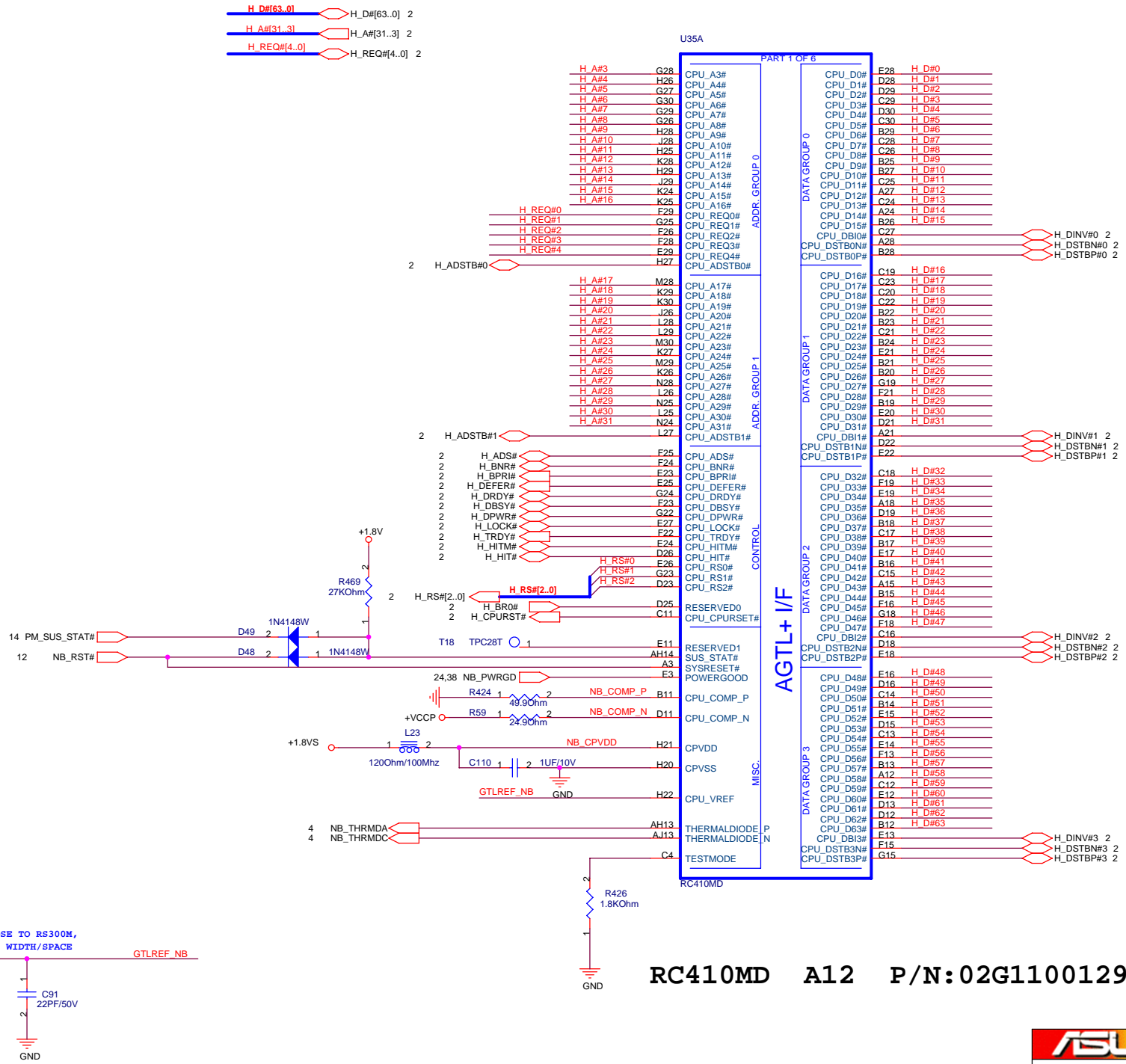


NB Detect



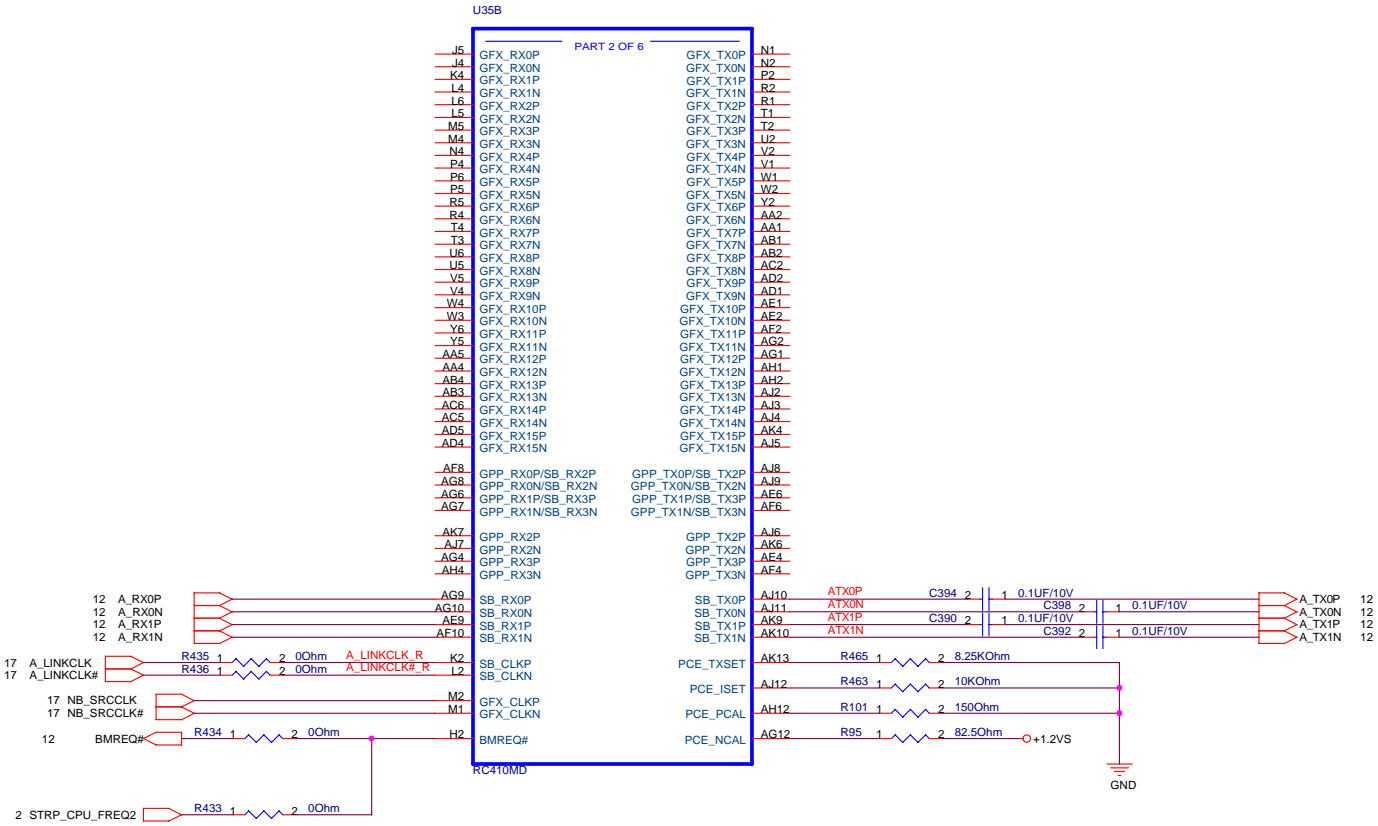
CPU Detect

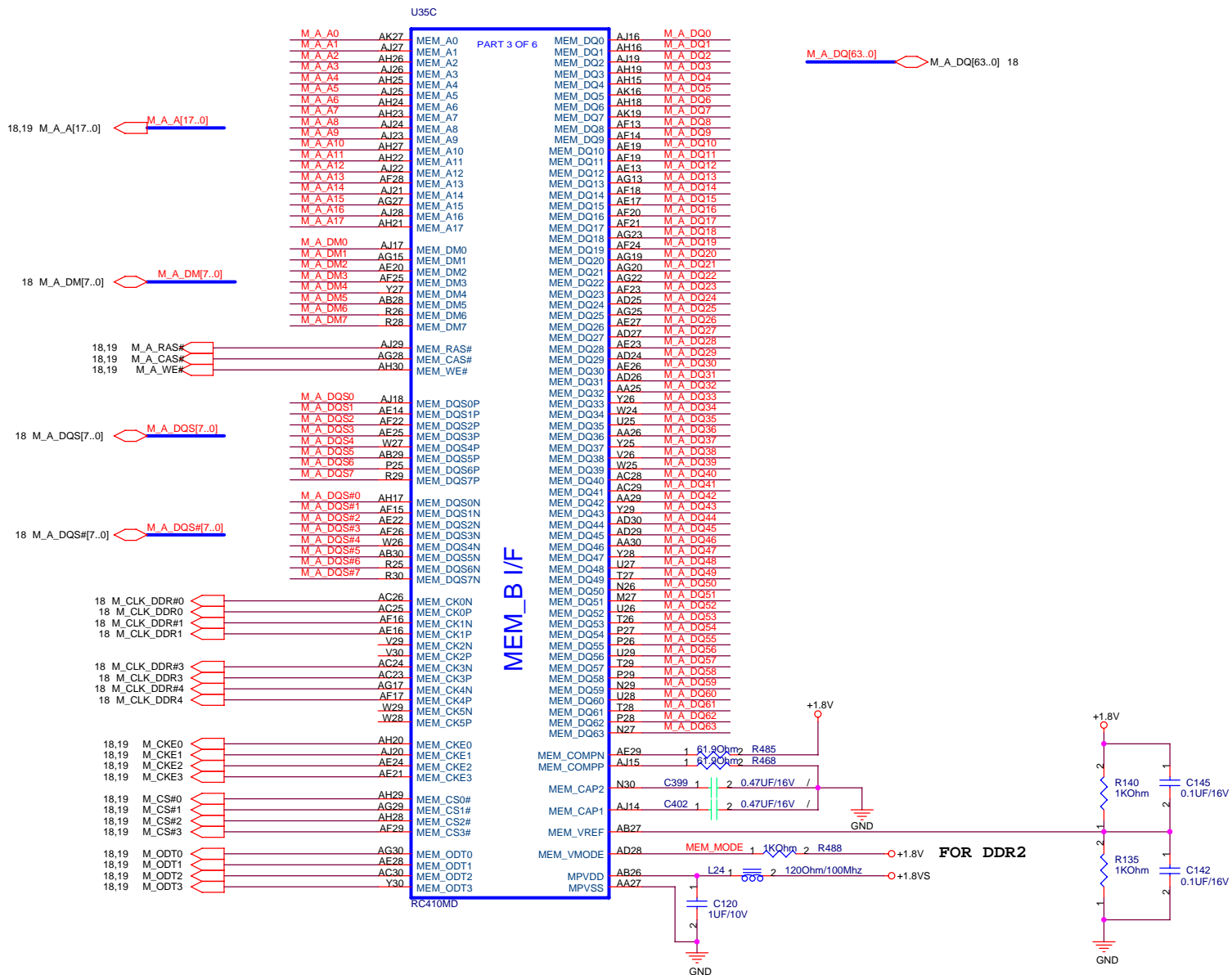
		Title : THERMAL SENSOR,FAN	
<OrgName>		Engineer: <OrgAddr1>	
Size	Project Name		Rev
Custom	A6Rp		2.0
Date: Thursday, April 06, 2006		Sheet 4 of 50	

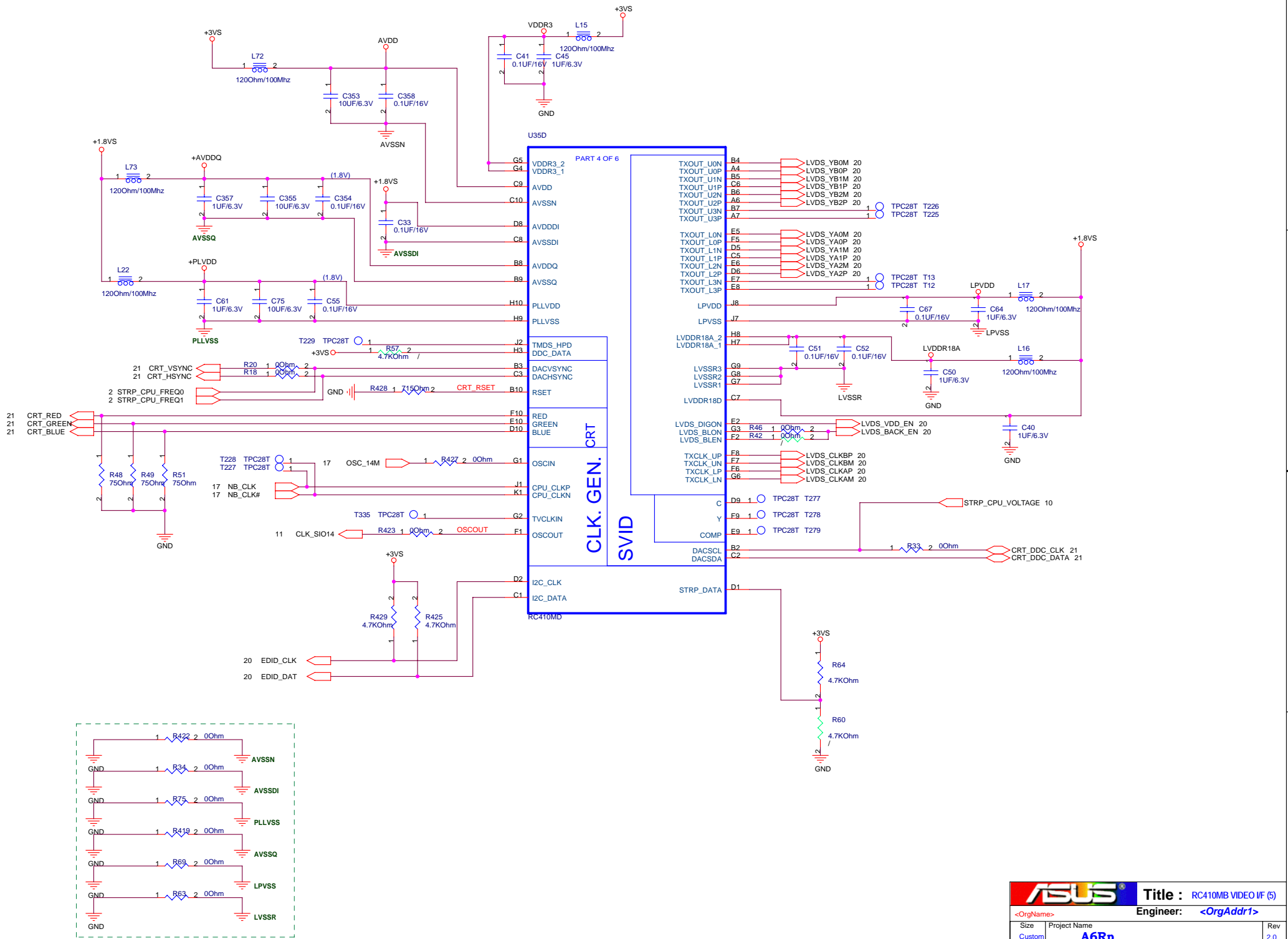


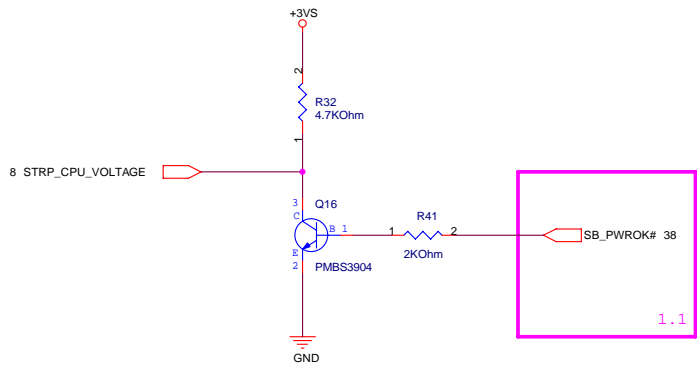
RC410MD A12 P/N:02G110012910

		Title : RC410MD AGTL I/F(1)	
<OrgName>		Engineer: <OrgAddr1>	
Size	Project Name		
Custom	A6Rp		
Date: Thursday, April 06, 2006	Sheet 5 of 50	Rev 2.0	





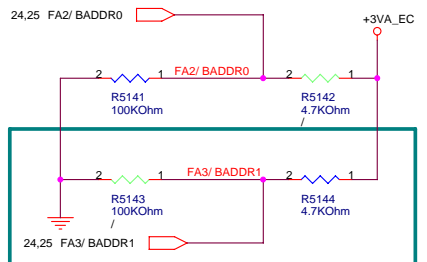




STRP_CPU_VOLTAGE: CPU VCC
0: MOBILE CPU
1: DESKTOP CPU
DEFAULT:0

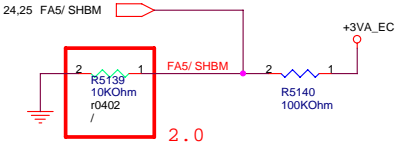
1.1

FA2/ BADDR0 & FA3/ BADDR1
00: PNPCNG Access Register Pair Are 002Eh and 002Fh
10: PNPCNG Access Register Pair Are 004Eh and 004Fh
01: PNPCNG Access Register Pair Are Determined by EC Domain Registers SWCBALR and SWCBAHR.
11: Reserved



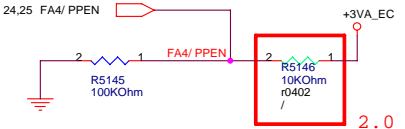
Note: Sampled at VSTBY Power Up Reset

FA5/ SHBM
0: Disable Shared Memory with Host BIOS
1: Enable Shared Memory with Host BIOS



2.0

FA4/ PPEN
0: Normal
1: KBS Interface Pins Are Switched to Parallel Port Interface for In-System Programming

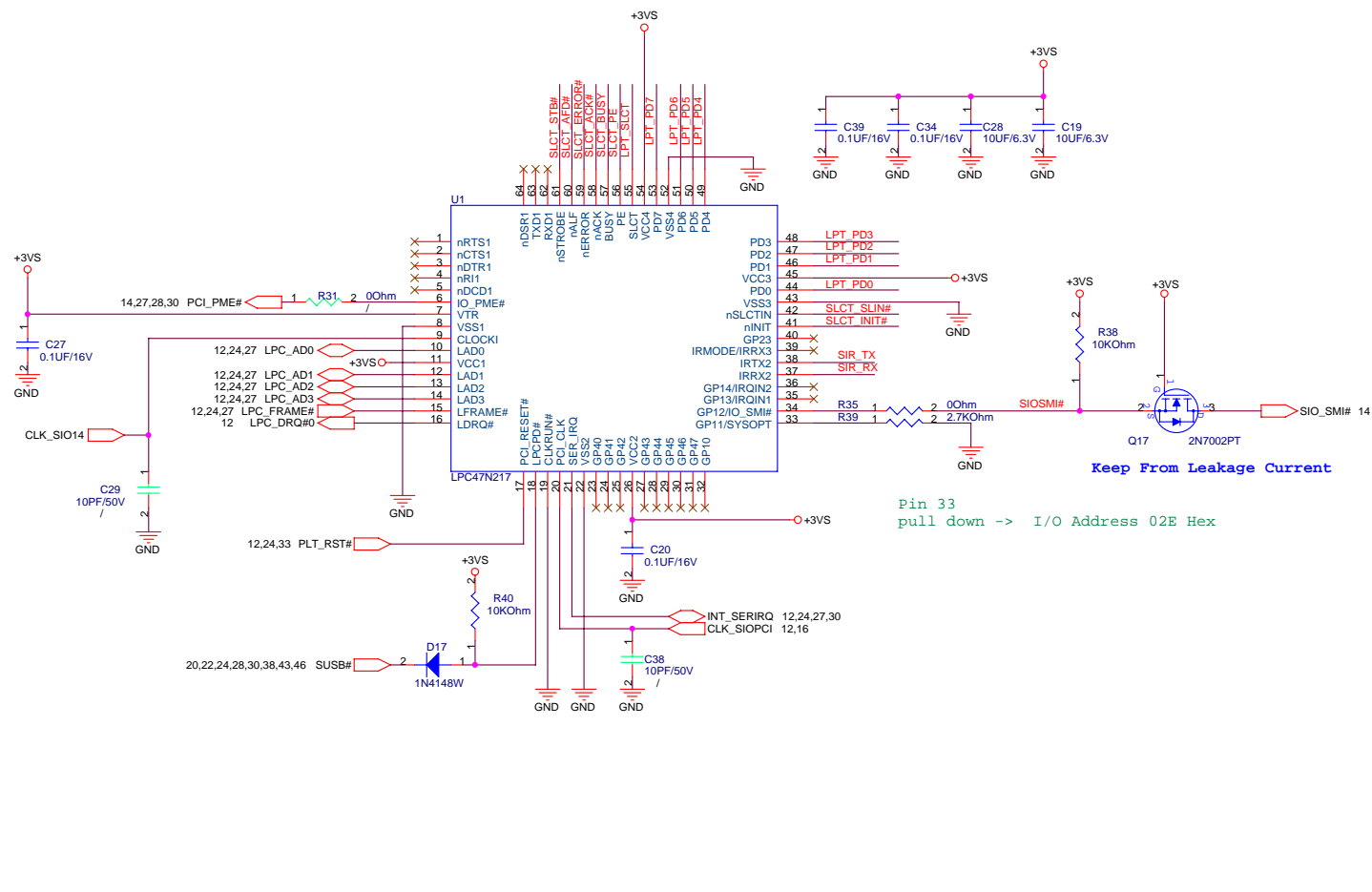


2.0

1.1

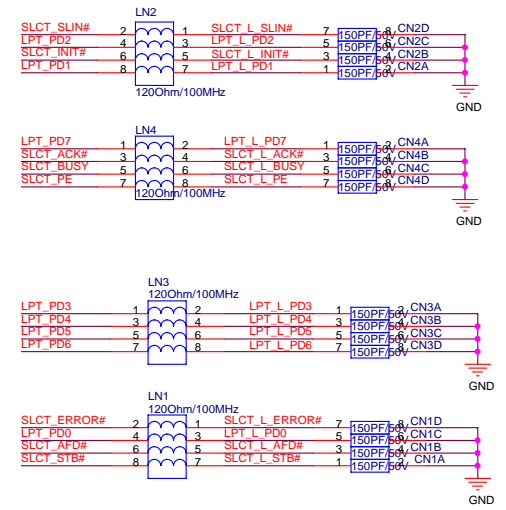
EC Hardware Strapping

Super I/O

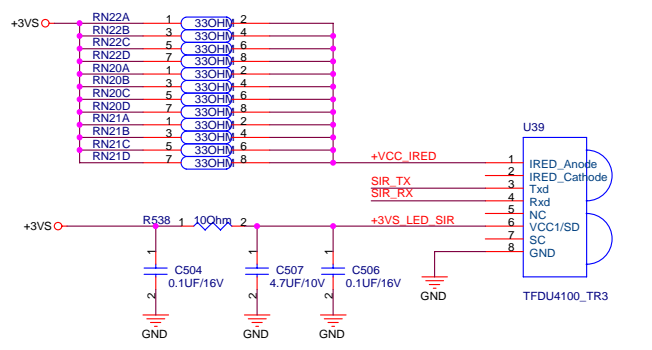


Pin 33 pull down -> I/O Address 02E Hex

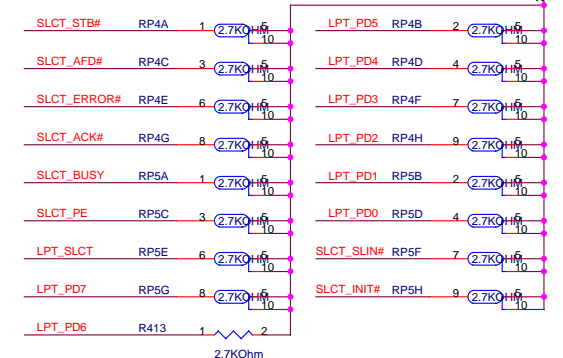
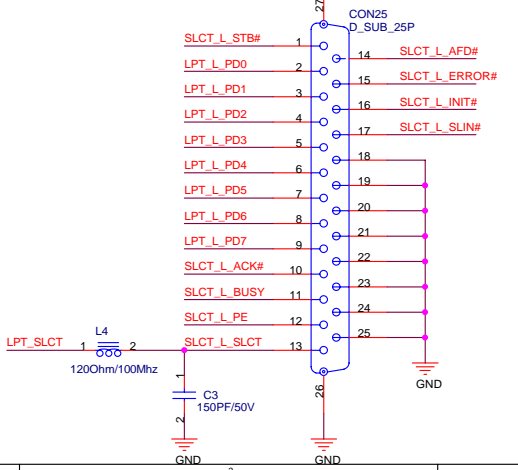
Keep From Leakage Current

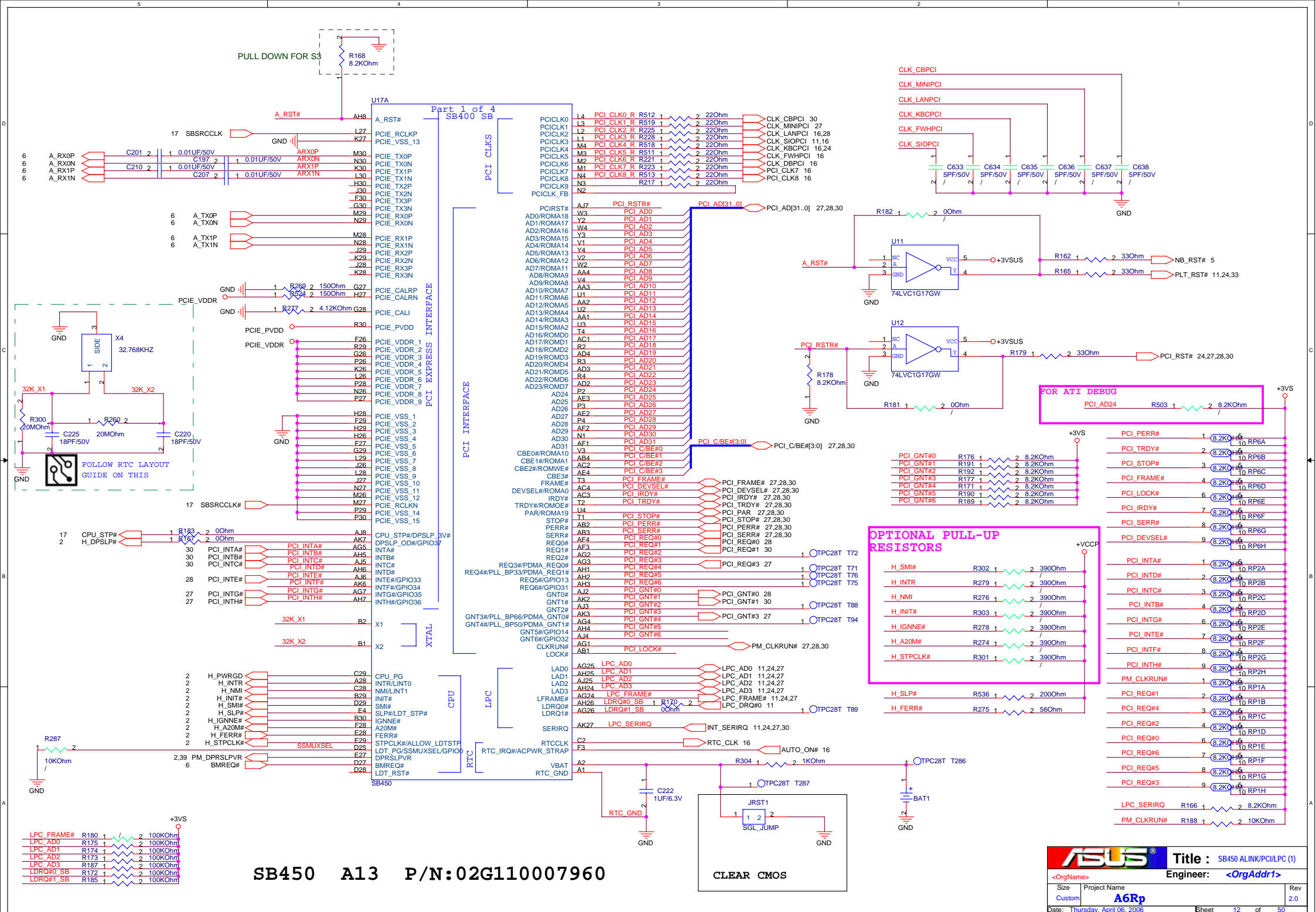


SIR



PRINT PORT

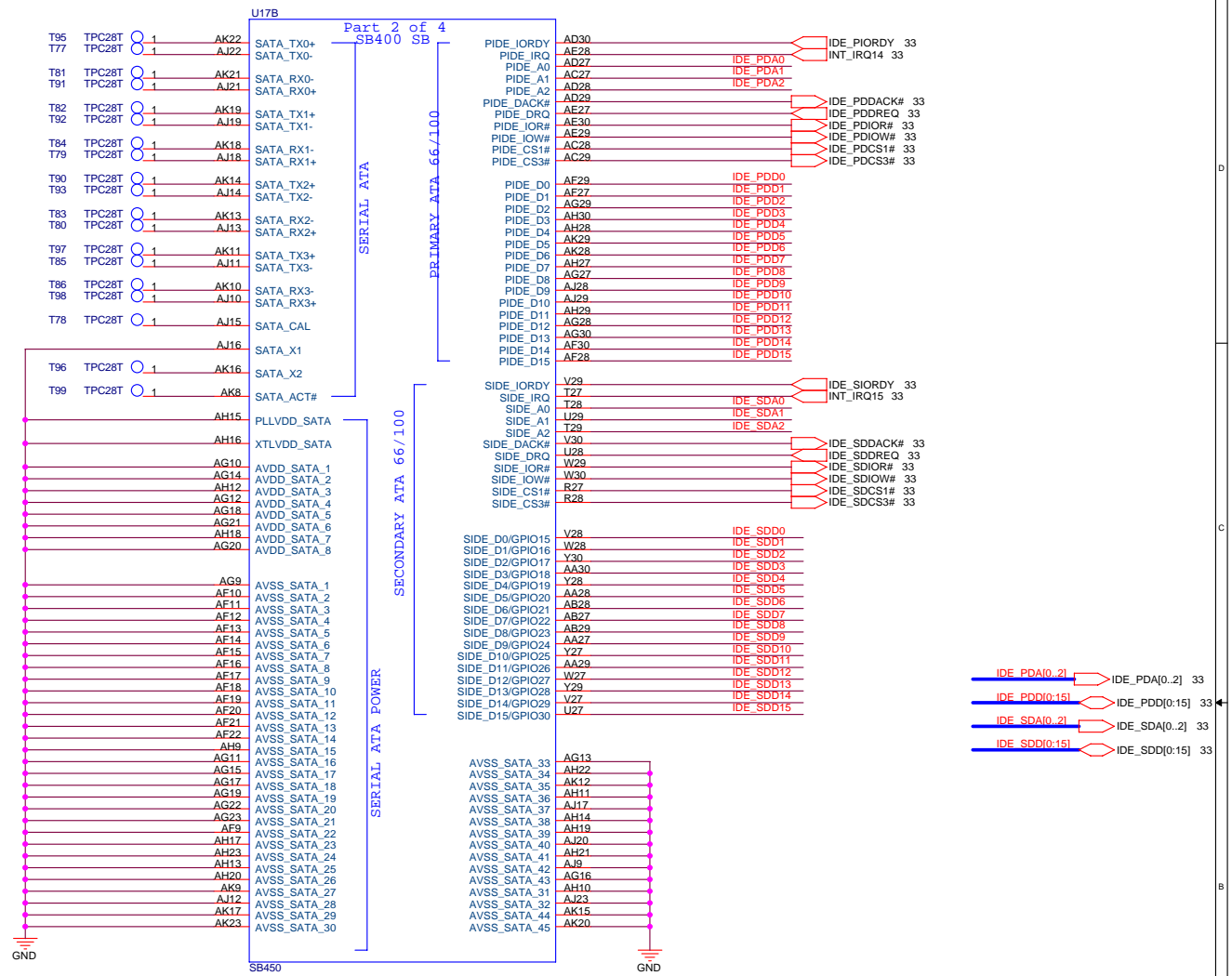


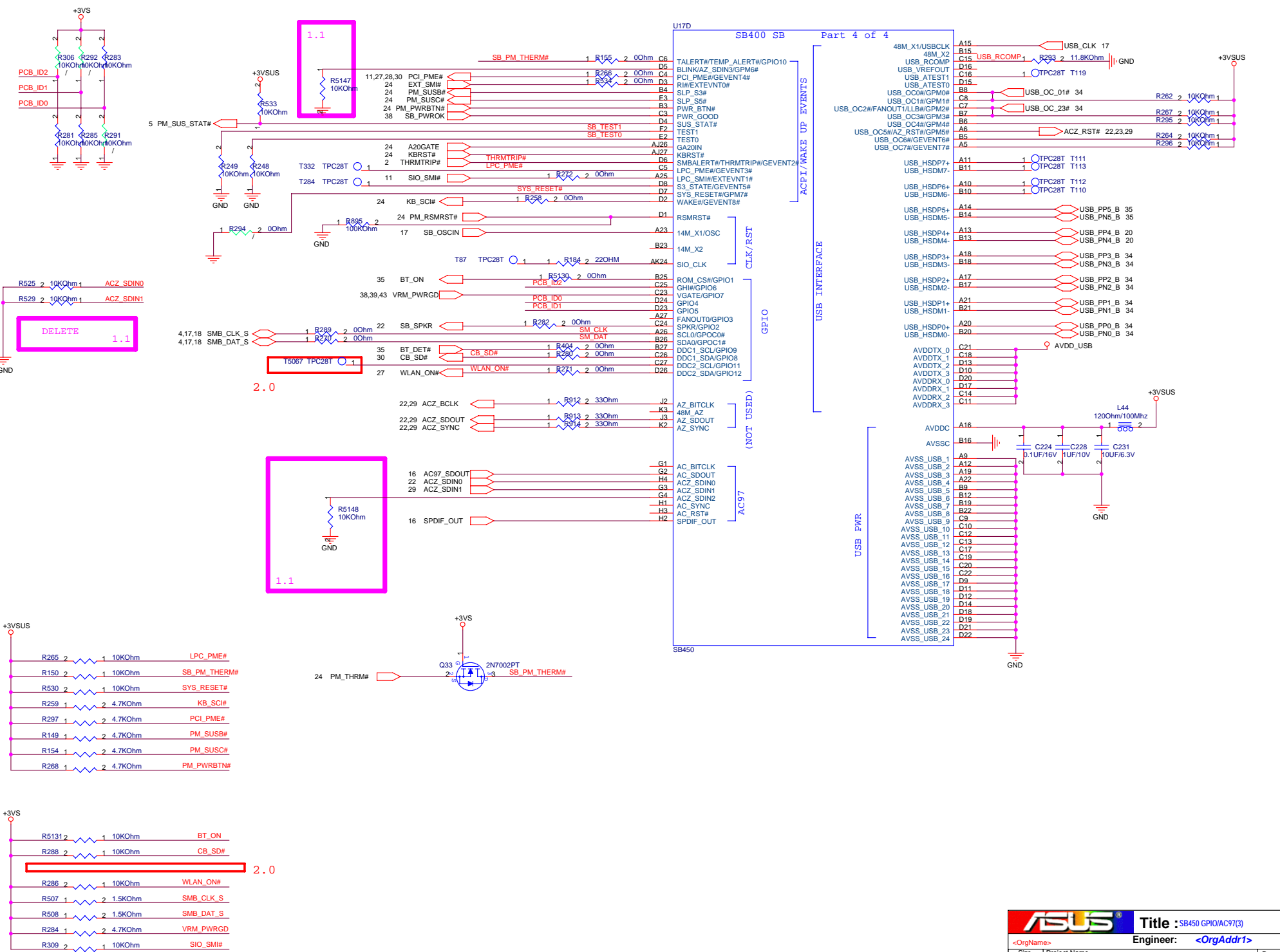


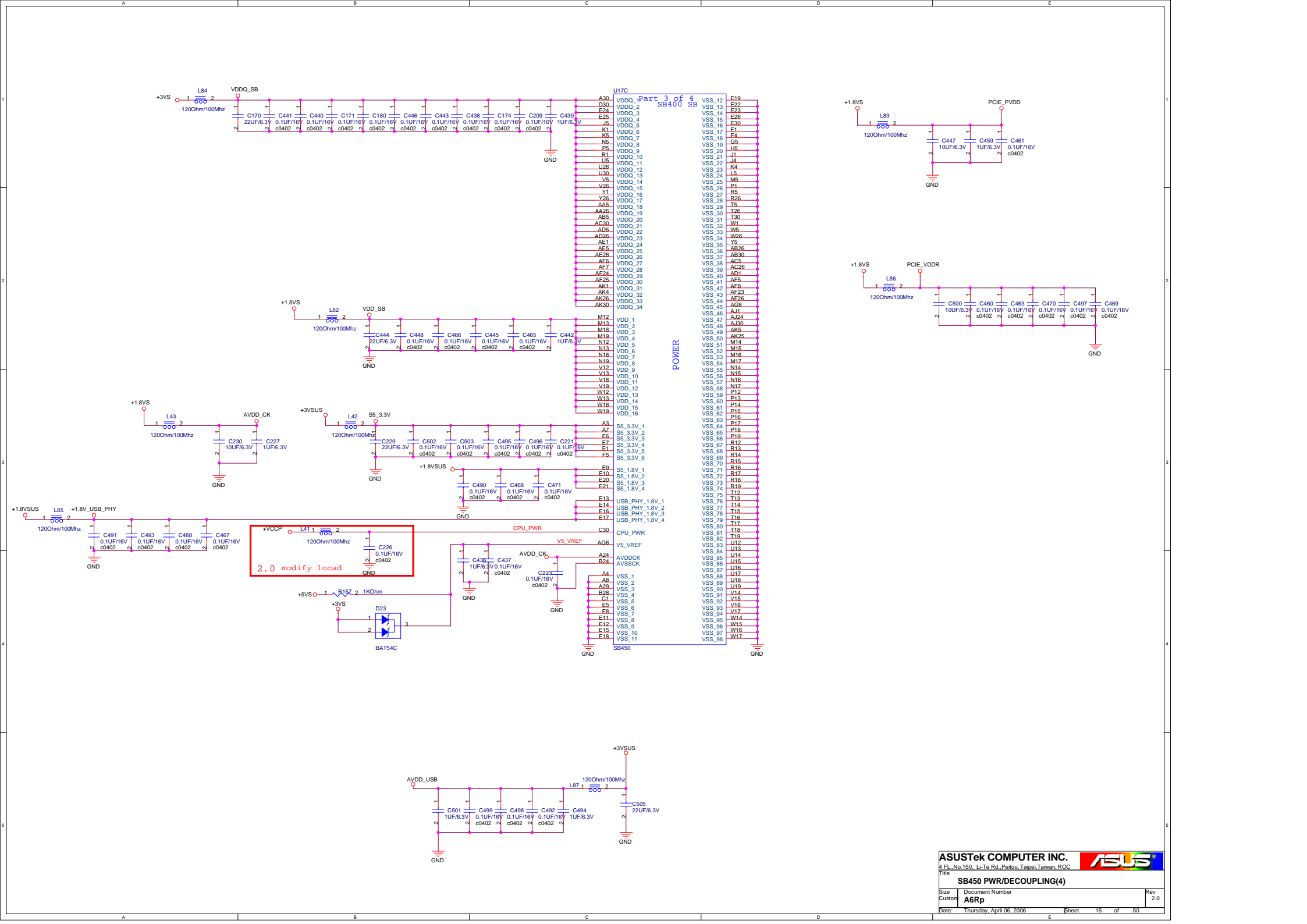
SB450 A13 P/N:02G110007960

CLEAR CMOS

ASUS Title : SB450 ALINK/PCI/LPC (1)
 Engineer : <OrgAddr1>
 Size Project Name
 Custom A6Rp
 Date: Thursday, April 06, 2006 Sheet 12 of 50







U17C

Part 3 of 4 SB400 SB

A30	VDDQ_12
D30	VDDQ_2
E24	VDDQ_3
E25	VDDQ_4
J6	VDDQ_5
K1	VDDQ_6
K5	VDDQ_7
N5	VDDQ_8
P5	VDDQ_9
R1	VDDQ_10
U5	VDDQ_11
U26	VDDQ_12
U30	VDDQ_13
V5	VDDQ_14
V26	VDDQ_15
Y1	VDDQ_16
Y26	VDDQ_17
AA5	VDDQ_18
AA26	VDDQ_19
AB5	VDDQ_20
AC30	VDDQ_21
AD5	VDDQ_22
AD26	VDDQ_23
AE1	VDDQ_24
AE5	VDDQ_25
AE26	VDDQ_26
AF6	VDDQ_27
AF7	VDDQ_28
AF24	VDDQ_29
AF25	VDDQ_30
AK1	VDDQ_31
AK4	VDDQ_32
AK26	VDDQ_33
AK30	VDDQ_34

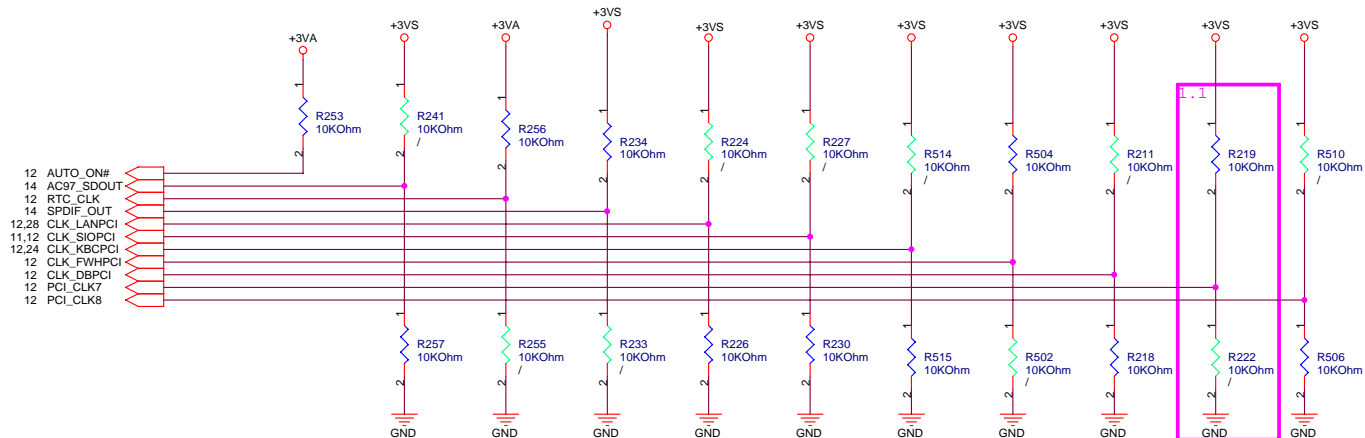
M12	VDD_1
M13	VDD_2
M18	VDD_3
M19	VDD_4
N12	VDD_5
N13	VDD_6
N18	VDD_7
N19	VDD_8
N42	VDD_9
V13	VDD_10
V18	VDD_11
V49	VDD_12
W12	VDD_13
W13	VDD_14
W18	VDD_15
W19	VDD_16

A3	S5_3.3V_1
A7	S5_3.3V_2
E6	S5_3.3V_3
E7	S5_3.3V_4
E1	S5_3.3V_5
F5	S5_3.3V_6

E9	S5_1.8V_1
E10	S5_1.8V_2
E20	S5_1.8V_3
E21	S5_1.8V_3
E16	S5_1.8V_4
E17	S5_1.8V_4

C30	CPU_PWR
AG6	V5_VREF
A24	AVDDCK
B24	AVSSCK

A1	VSS_1
A29	VSS_2
B29	VSS_4
C1	VSS_5
E5	VSS_6
E8	VSS_7
E11	VSS_8
E12	VSS_9
E15	VSS_10
E18	VSS_11



REQUIRED STRAPS

	AUTO_ON#	AC_SDOUT	RTC_CLK	SPDIF_OUT	CLK_LANPCI	CLK_SIOFPCI	CLK_KBCPCI	CLK_FWHPCI	CLK_DBPCI	PCI_CLK7	PCI_CLK8
PULL HIGH	MANUAL PWR ON	USE DEBUG STRAPS	INTERNAL RTC	SIO 24MHz		USB PHY PWRDOWN DISABLE	USE USB PLL		CPU I/F = K8	ROM TYPE H,H = PCI ROM	
PULL LOW	AUTO PWR ON	IGNORE DEBUG STRAPS	EXTERNAL RTC (NOT SUPPORTED W/ IT8712)	SIO 48MHz	SEE NOTE1	USB PHY PWRDOWN ENABLE	BYPASS USB PLL	SEE NOTE2	CPU I/F = P4	H,L = LPC ROM I DEFAULT LPC Address Mapped below 1M L,H = LPC ROM II LPC Address Mapped to top 4G L,L = FWH ROM	

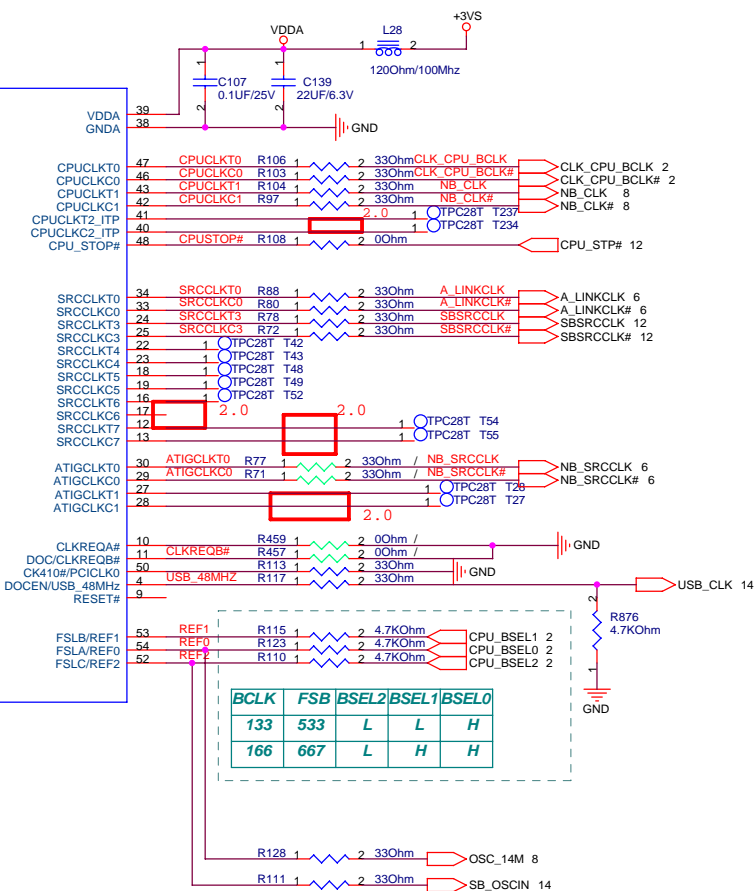
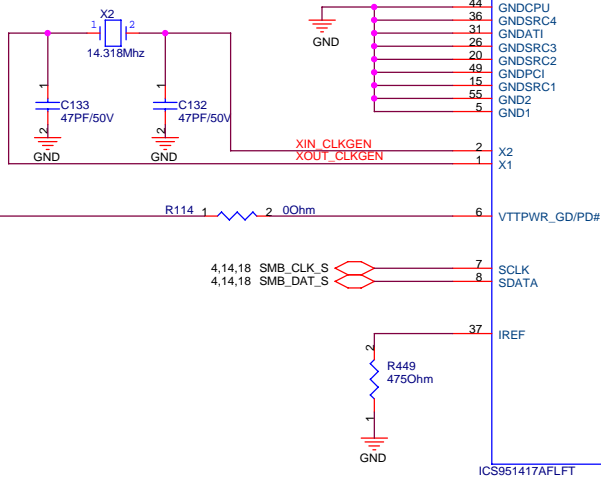
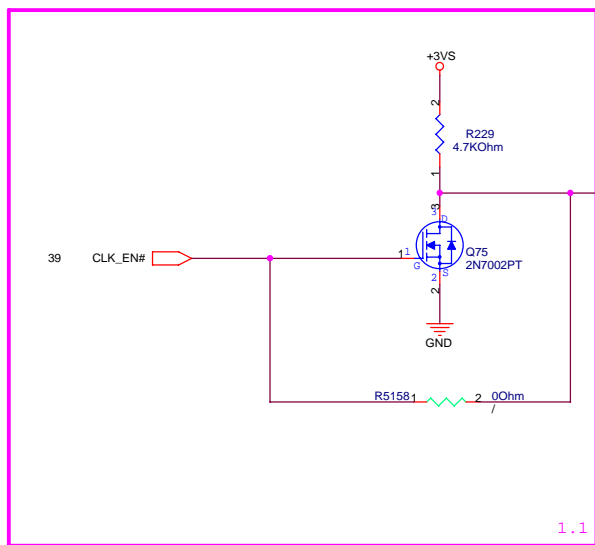
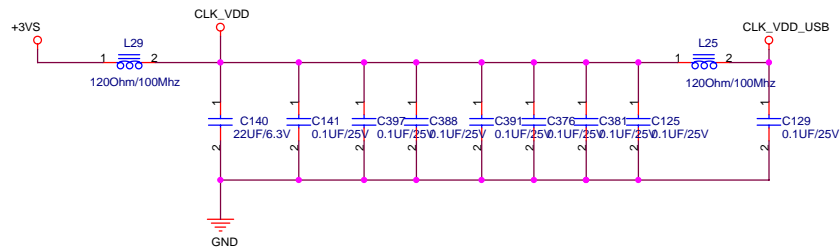
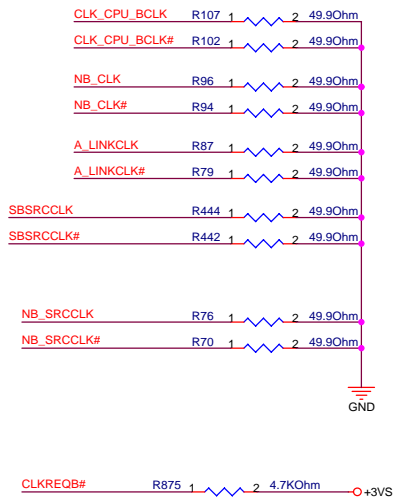
NOTE
1. USB CLK STRAPPING CHANGE

	A21,A22,A23	A31 AND NEWER
10K PULL UP	OSC/CLOCK BUFFER	CRYSTAL PAD
10K PULL DOWN	CRYSTAL PAD	OSC/CLOCK BUFFER

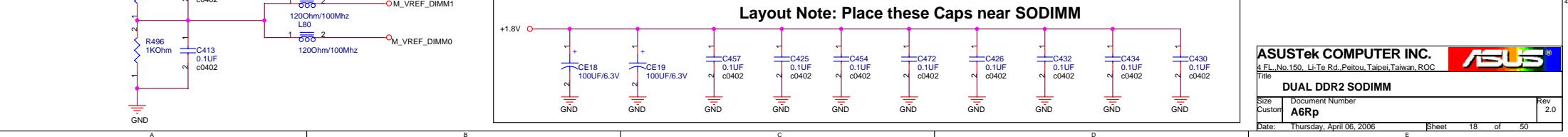
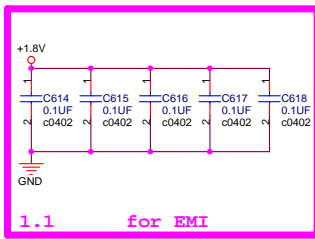
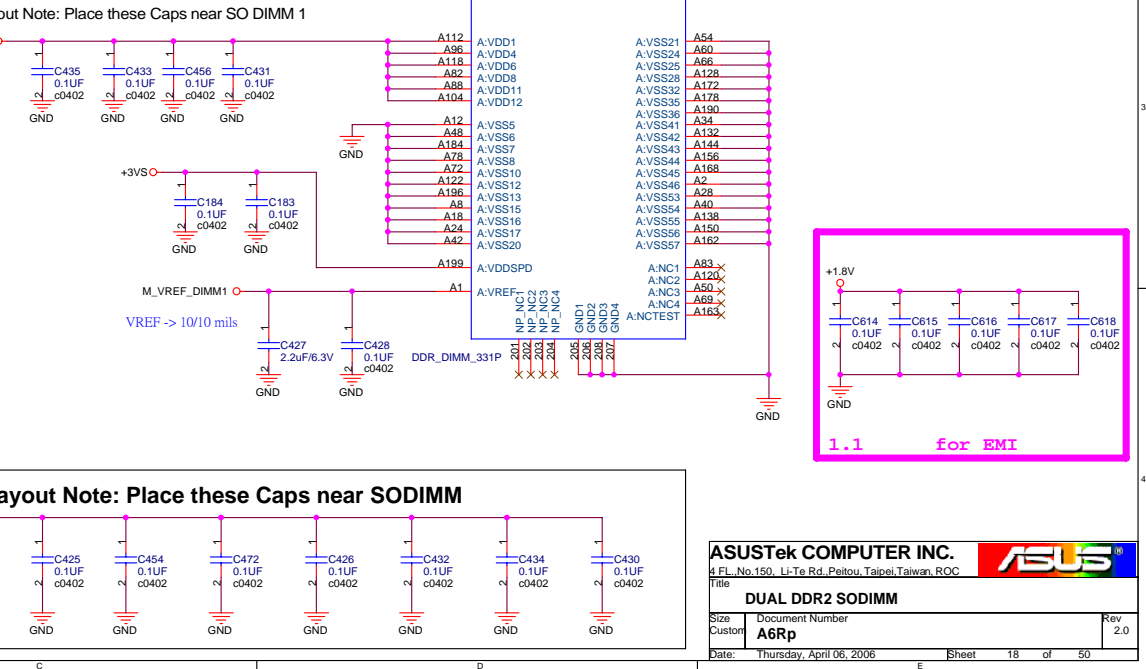
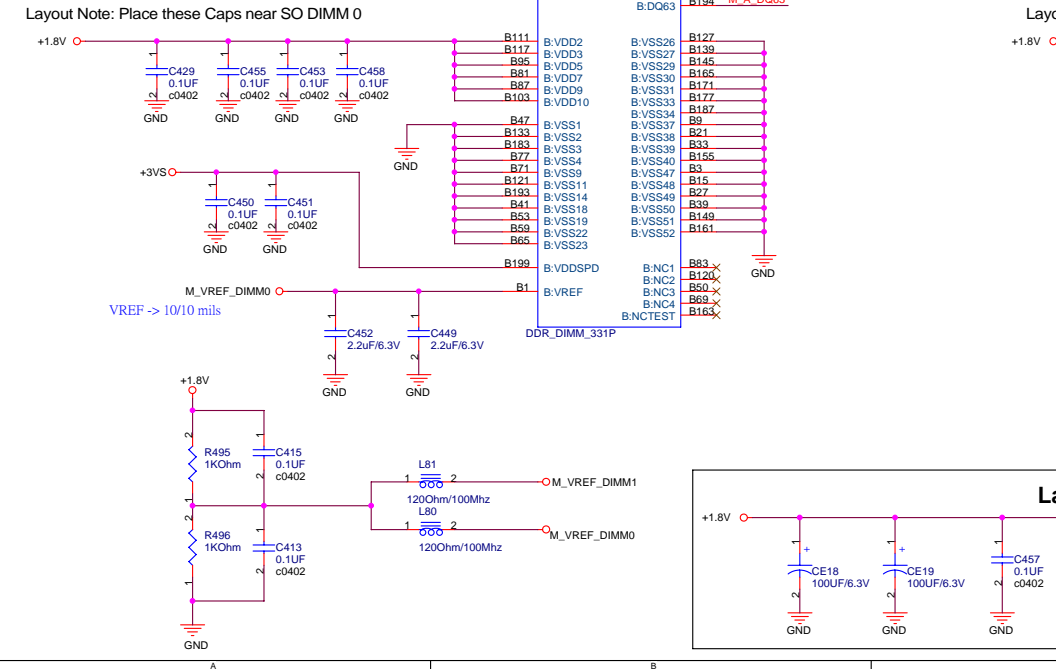
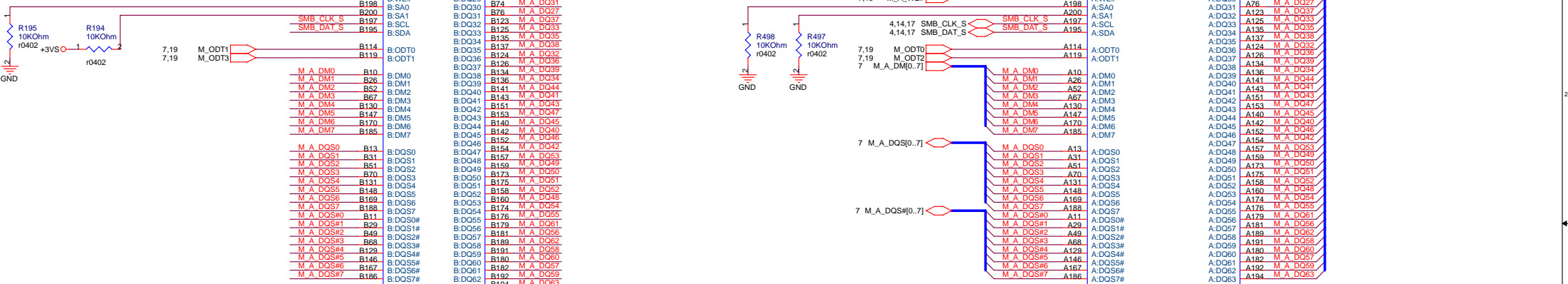
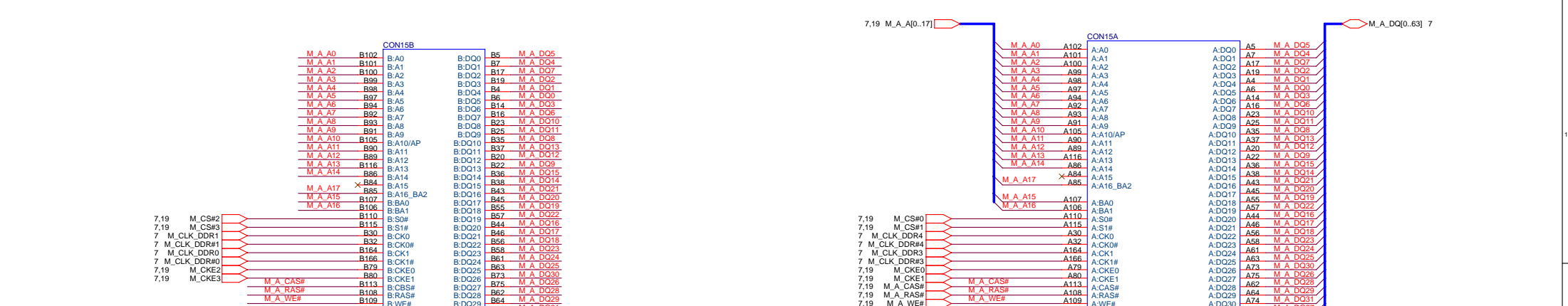
2. 14MHz CLOCK TYPE STRAPPING

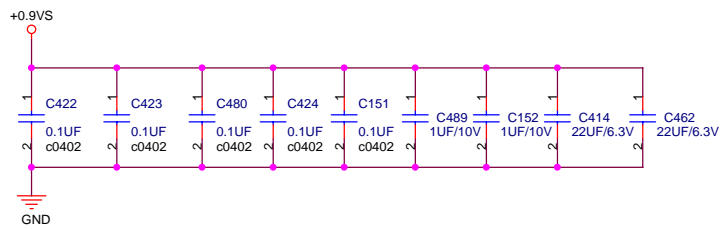
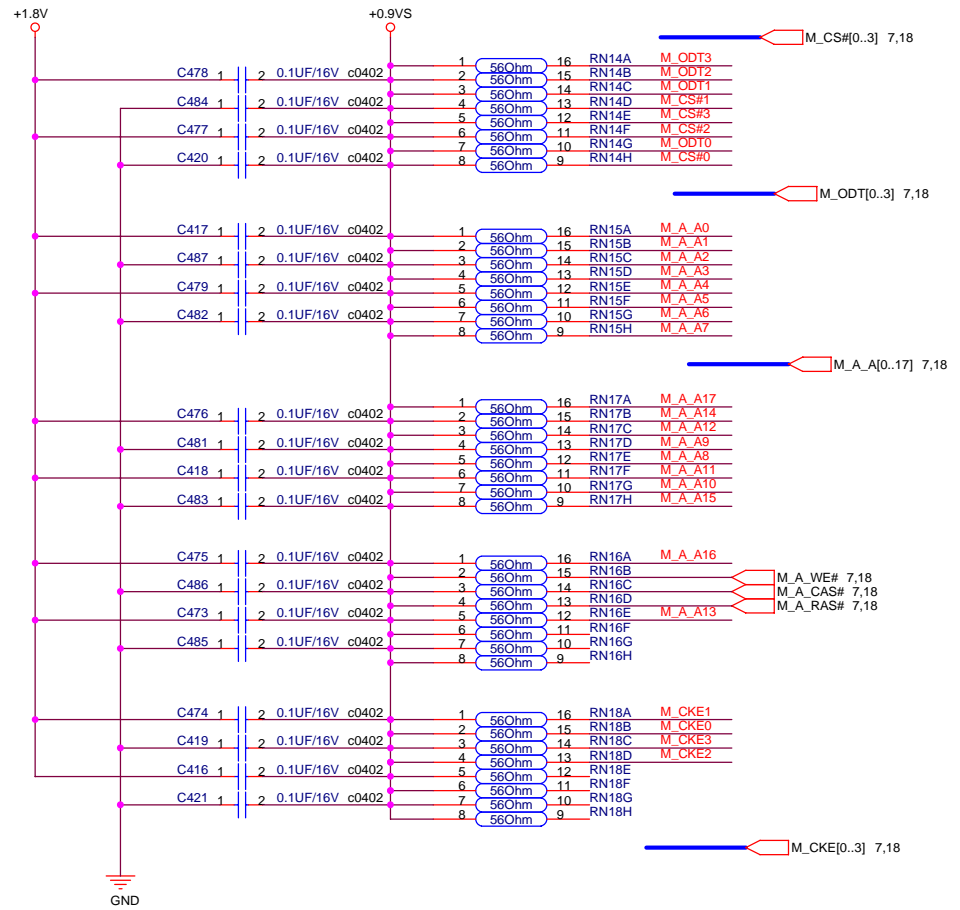
	A11-A31	A32 AND ABOVE
	14MHz CLOCK PAD IS CRYSTAL PAD	PCIE COMMON MODE SETTING
10K PULL UP	CLOCK INPUT BUFFER	PCIE CM_SET LOW
10K PULL DOWN	CRYSTAL PAD	PCIE CM_SET HIGH

PLACE termination close to source IC



1.1

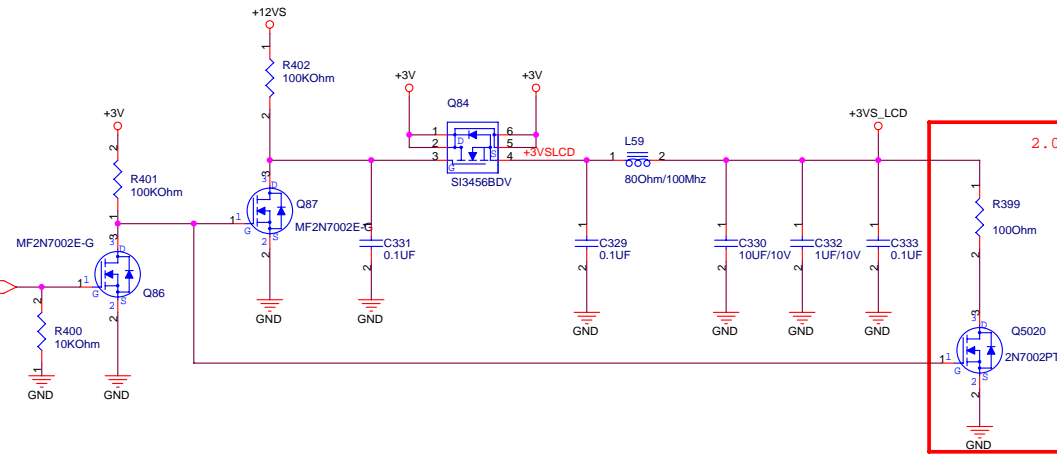




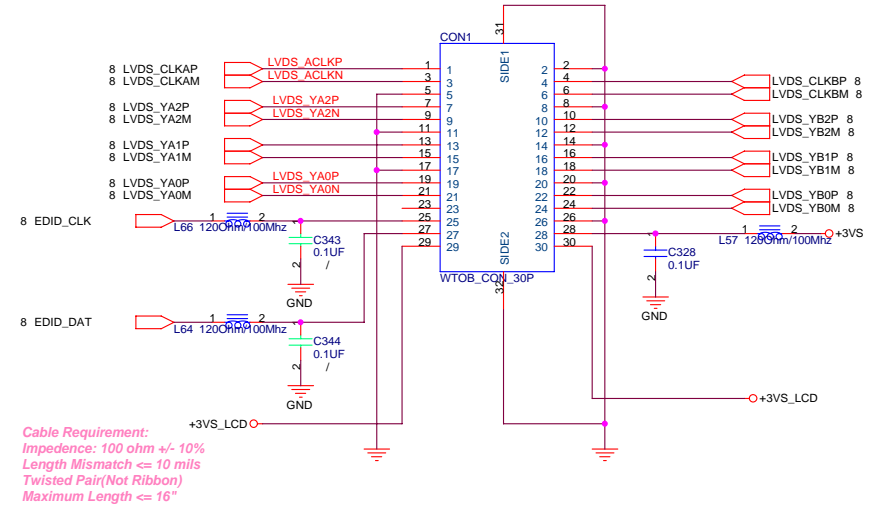
ASUS Title : **DDR2 TERMINATION**
 <OrgName> Engineer: <OrgAddr1>
 Size Project Name Rev
 Custom **A6Rp** 2.0
 Date: Thursday, April 06, 2006 Sheet 19 of 50

LCD Power

3V-3.6V
Full Active: 410 mA(Max. 500 mA)



LCD LVDS Interface

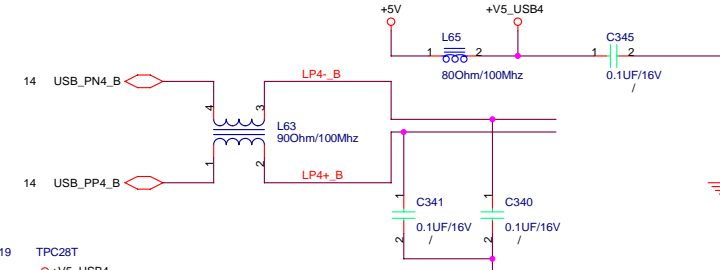
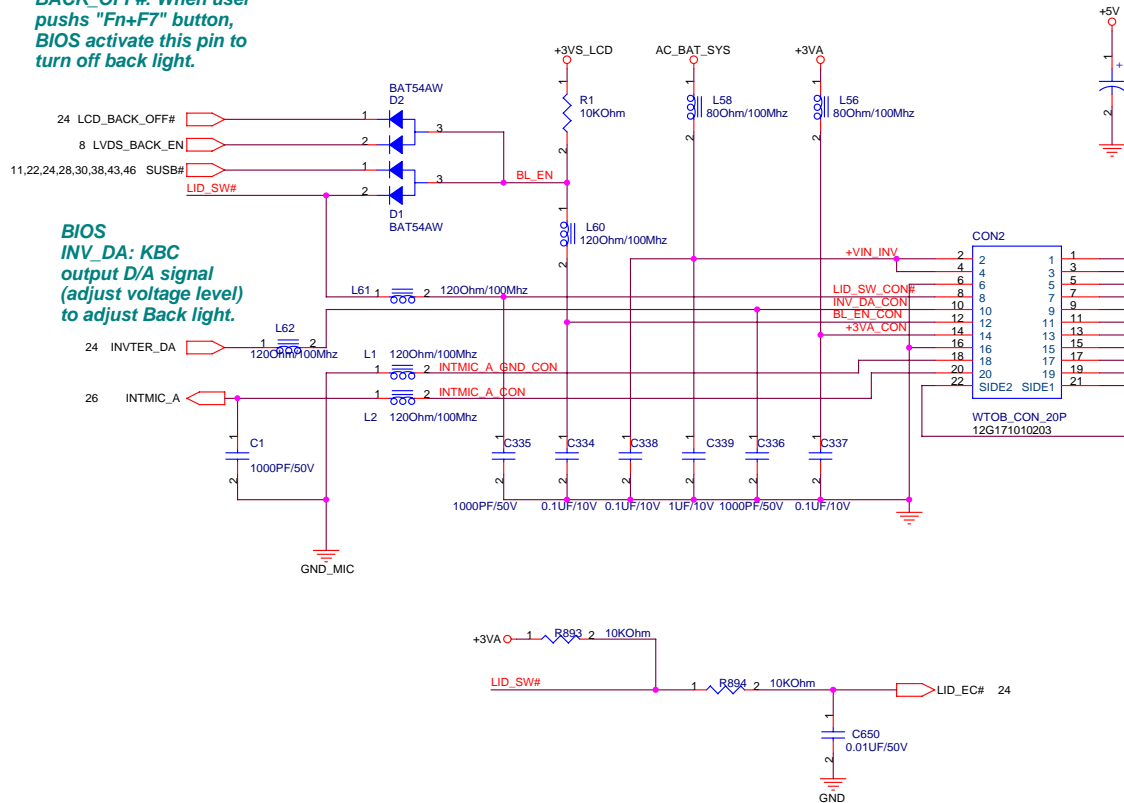


Cable Requirement:
Impedance: 100 ohm +/- 10%
Length Mismatch <= 10 mils
Twisted Pair(Not Ribbon)
Maximum Length <= 16"

INVERTER Interface

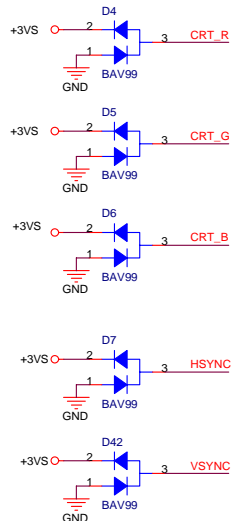
BIOS BACK_OFF#: When user pushes "Fn+F7" button, BIOS activate this pin to turn off back light.

BIOS INV_DA: KBC output D/A signal (adjust voltage level) to adjust Back light.

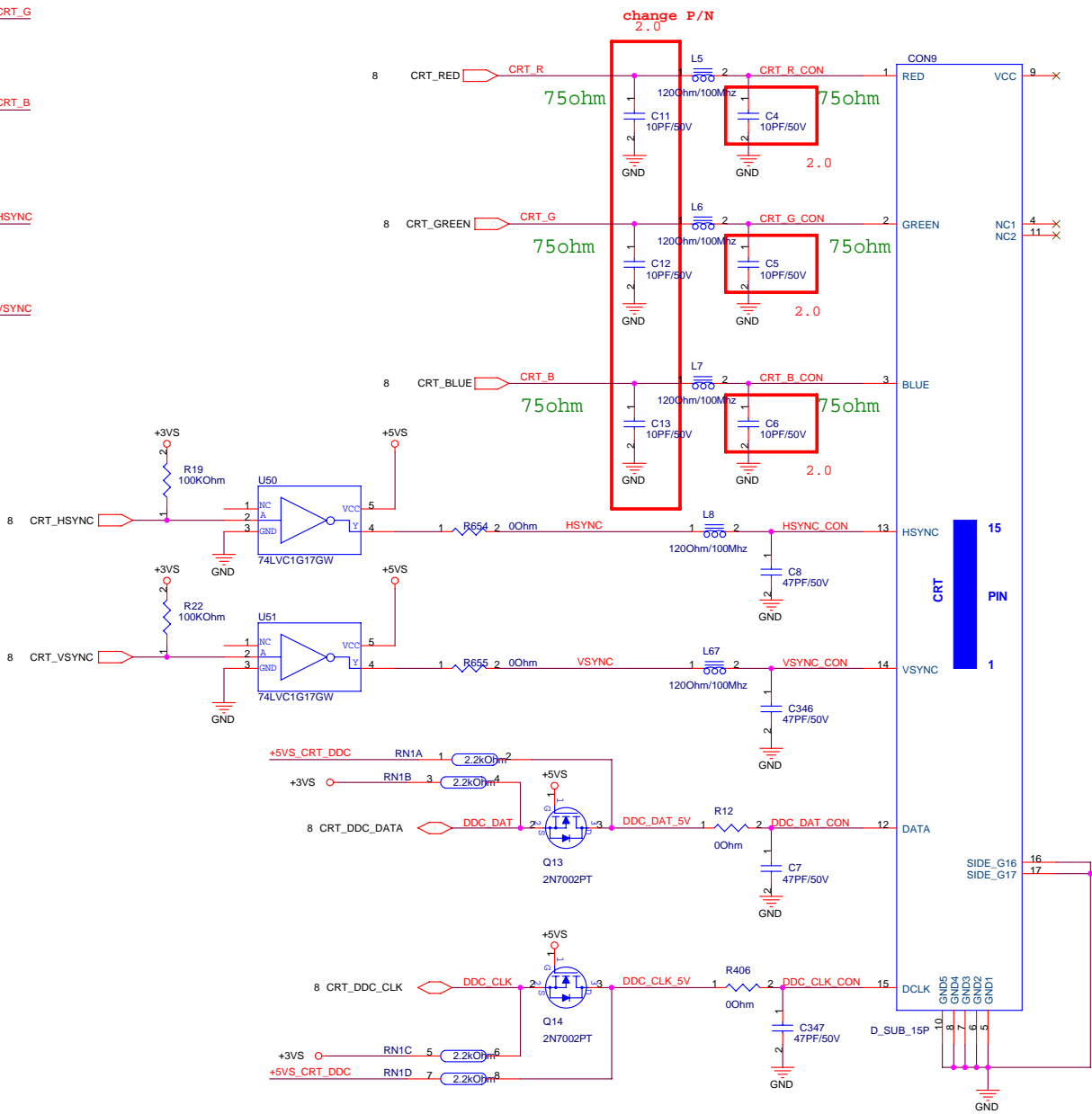
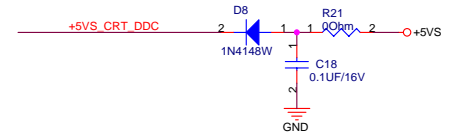


USB PORT 4 for USB CAMERA

Pin 19 : Add a USB 2.0 Shielding GND cable to USB module.

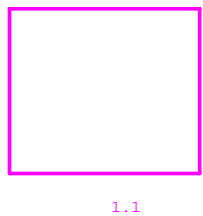
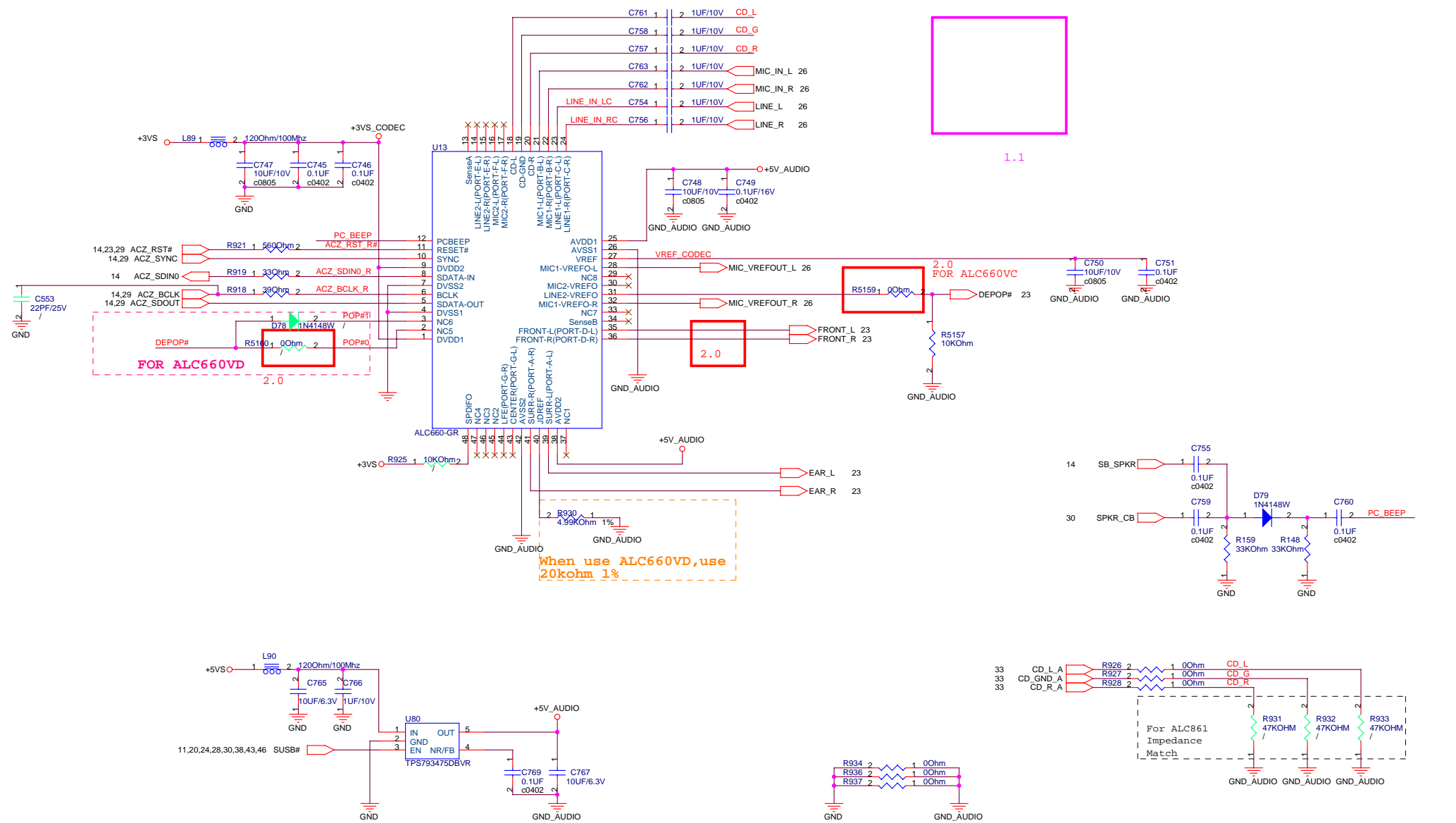


PLACE ESD Diodes near VGA port

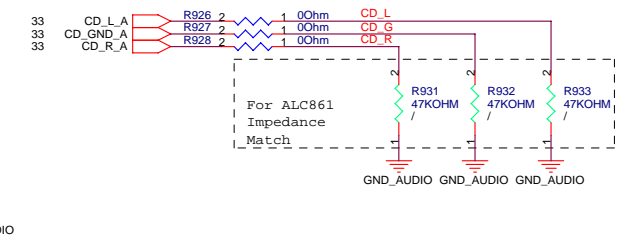
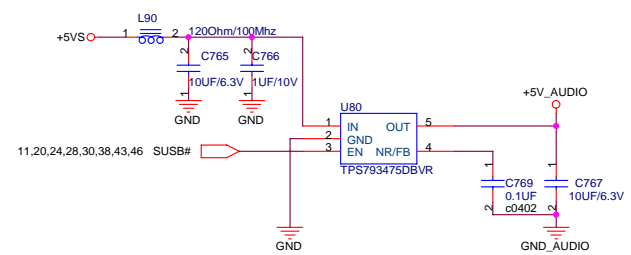
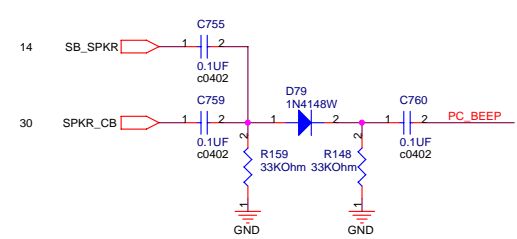


change P/N 2.0

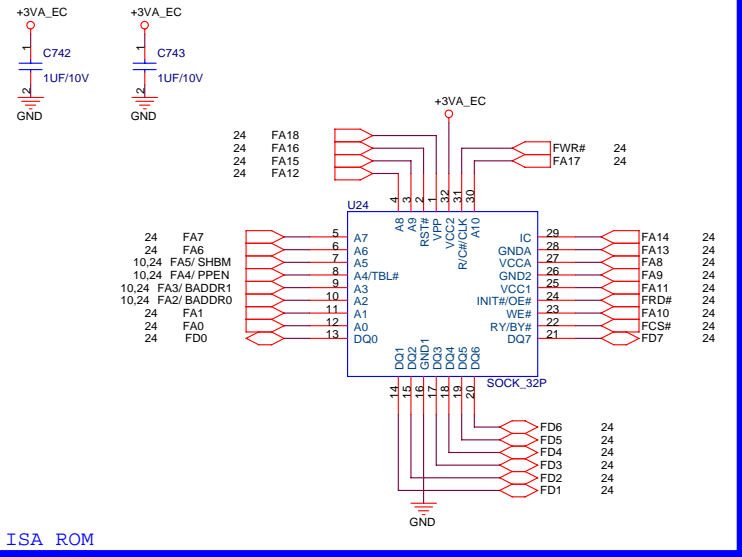




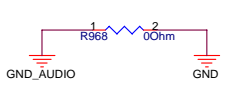
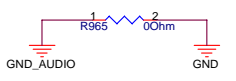
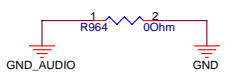
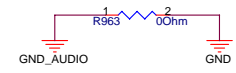
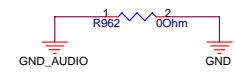
When use ALC660VD, use 20kohm 1%



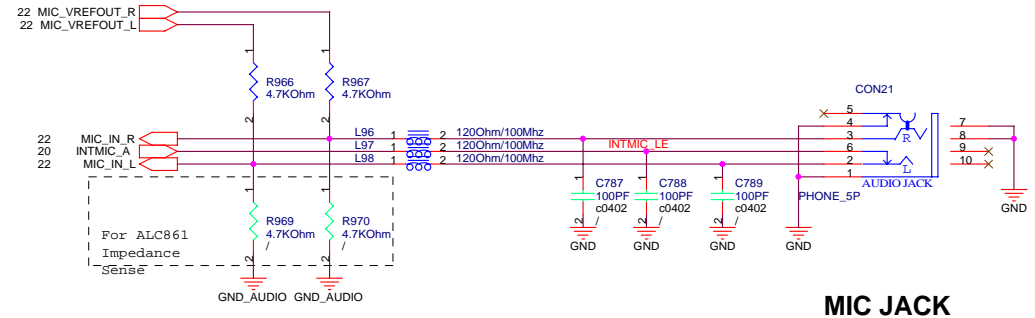
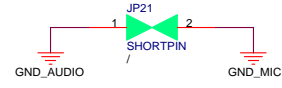
PLCC32 Socket PN:12G04300032F SST-PLCC32 4Mbits Flash ROM PN:05G001027221



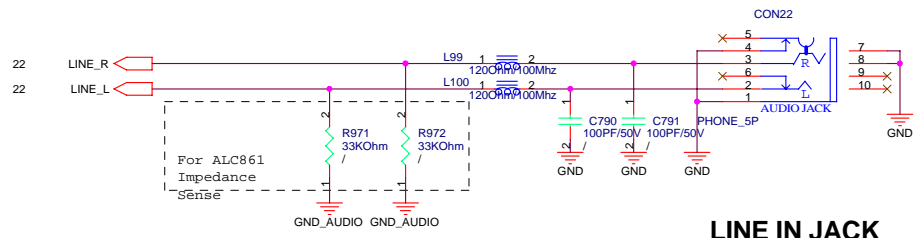
ISA ROM



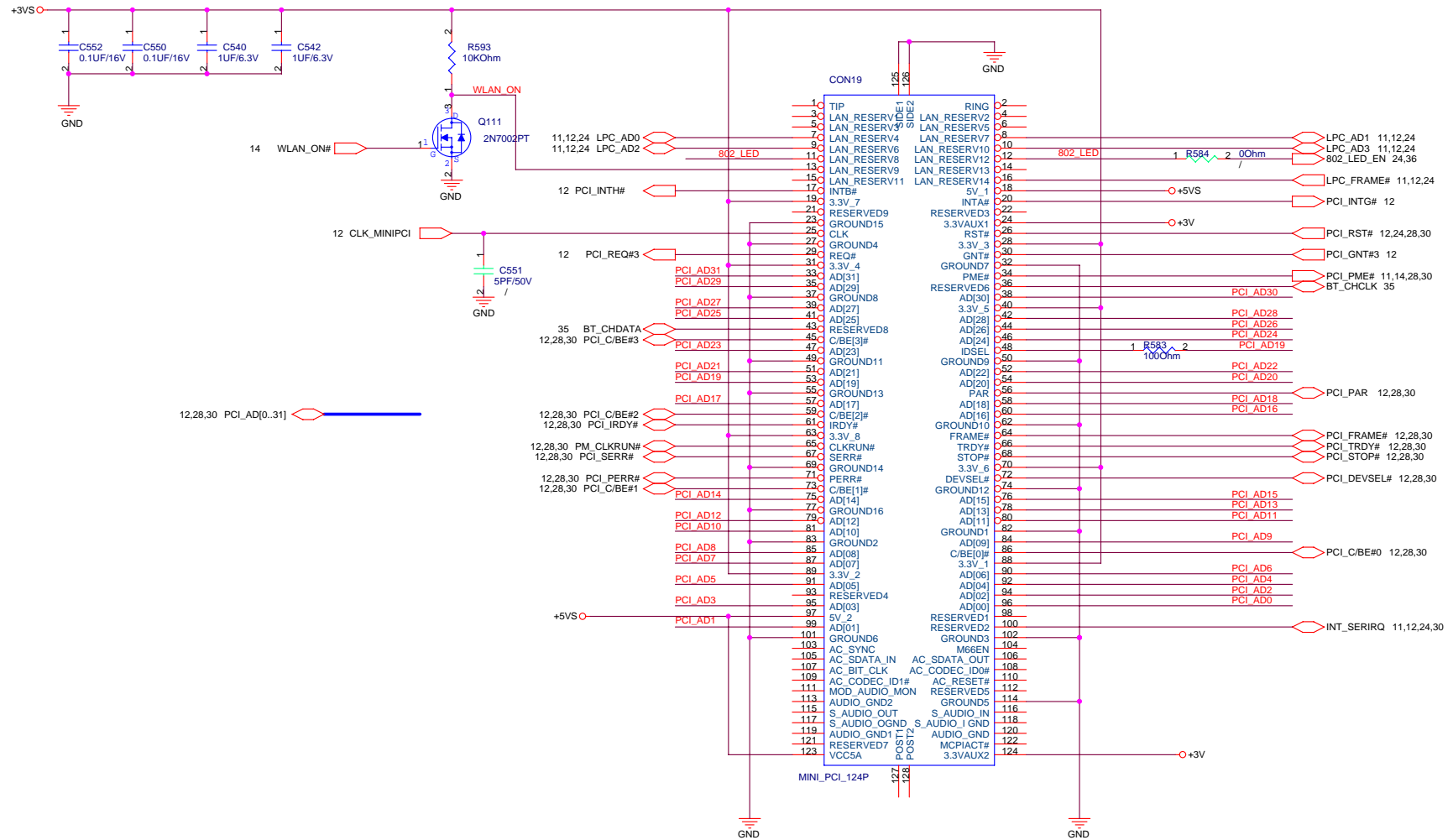
**INTMIC_A:GND_AUDIO
: W/P/X = 12/5/15mils**

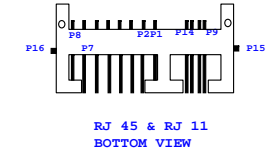
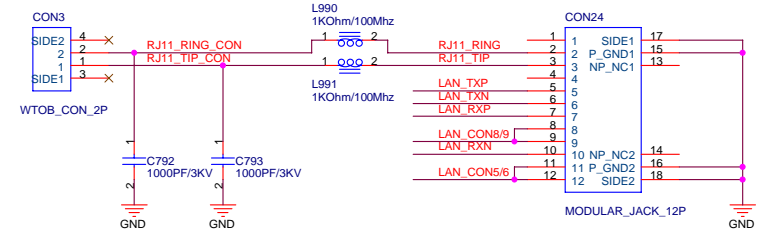
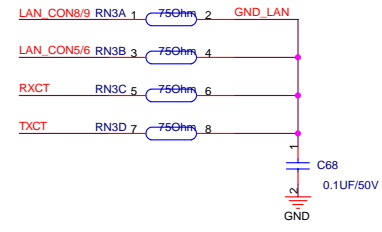
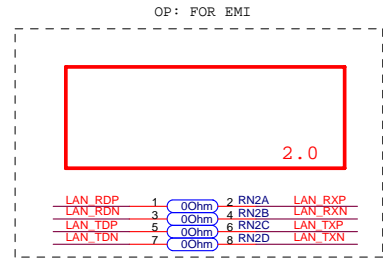
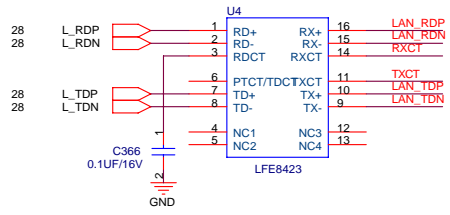


MIC JACK



LINE IN JACK

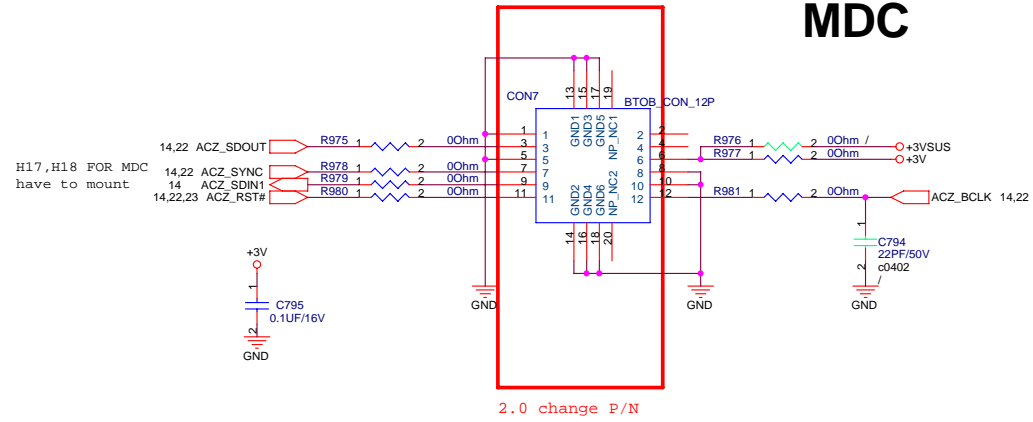


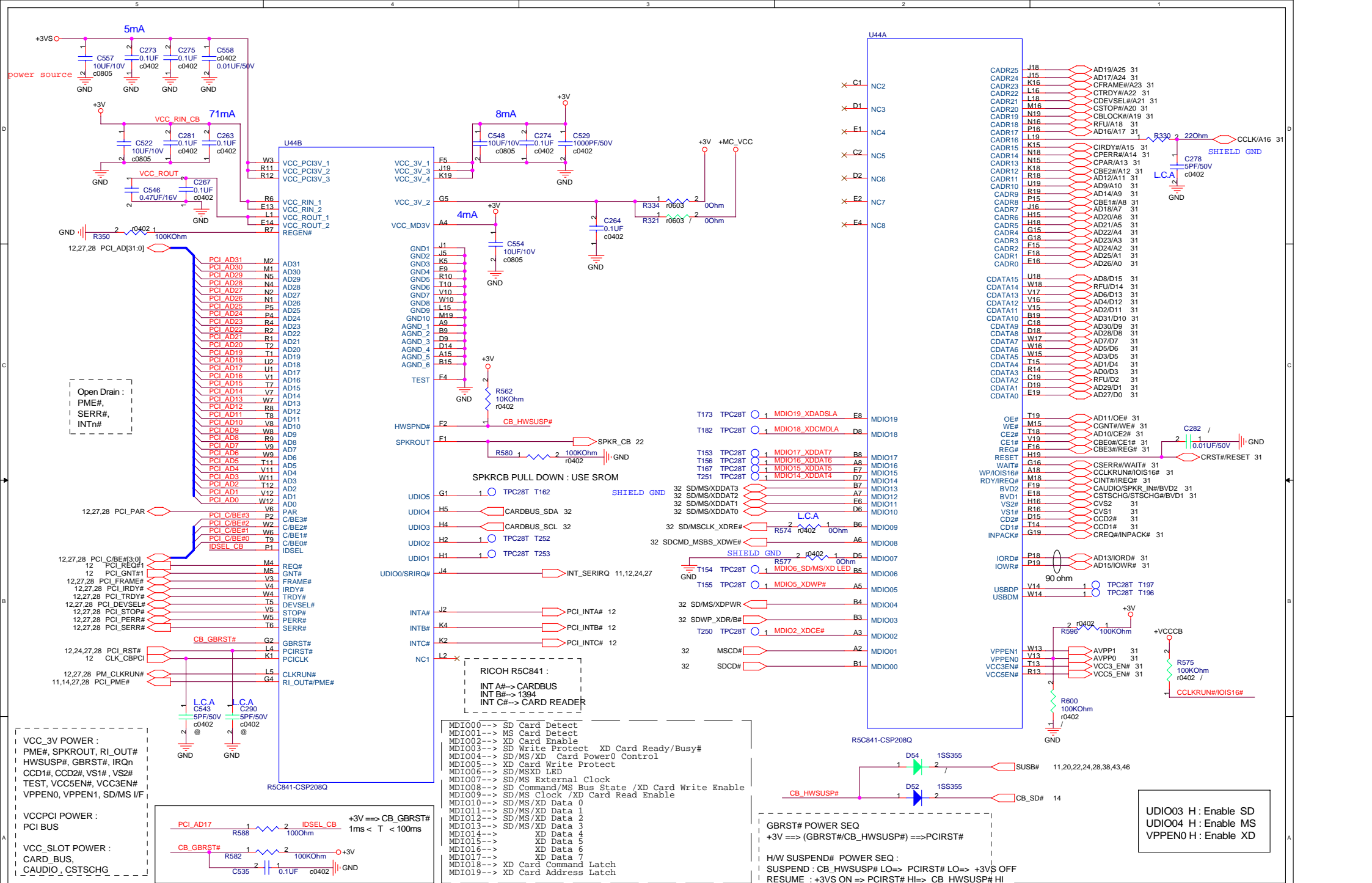


LAN PORT

MDC

MDC





RICOH R5C841 :
 INT A#-> CARDBUS
 INT B#-> 1394
 INT C#-> CARD READER

MDIO00--> SD Card Detect
 MDIO01--> MS Card Detect
 MDIO02--> XD Card Enable
 MDIO03--> SD Write Protect /XD Card Ready/Busy#
 MDIO04--> SD/MS /XD Card Power0 Control
 MDIO05--> XD Card Write Protect
 MDIO06--> SD/MSXD LED
 MDIO07--> SD/MS External Clock
 MDIO08--> SD Command/MS Bus State /XD Card Write Enable
 MDIO09--> SD/MS Clock /XD Card Read Enable
 MDIO10--> SD/MS/XD Data 0
 MDIO11--> SD/MS/XD Data 1
 MDIO12--> SD/MS/XD Data 2
 MDIO13--> SD/MS/XD Data 3
 MDIO14--> XD Data 4
 MDIO15--> XD Data 5
 MDIO16--> XD Data 6
 MDIO17--> XD Data 7
 MDIO18--> XD Card Command Latch
 MDIO19--> XD Card Address Latch

VCC_3V POWER :
 PME#, SPKR_OUT, RI_OUT#,
 HWSUSP#, GBRST#, IRQn
 CCD1#, CCD2#, VS1#, VS2#
 TEST, VCC5EN#, VCC3EN#,
 VPPEN0, VPPEN1, SD/MS I/F

VCCPCI POWER :
 PCI BUS

VCC_SLOT POWER :
 CARD_BUS,
 CAUDIO, CSTSCHG

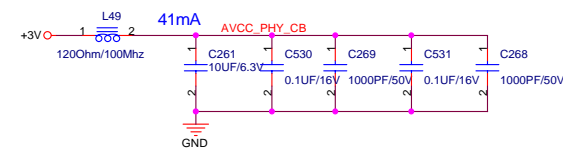
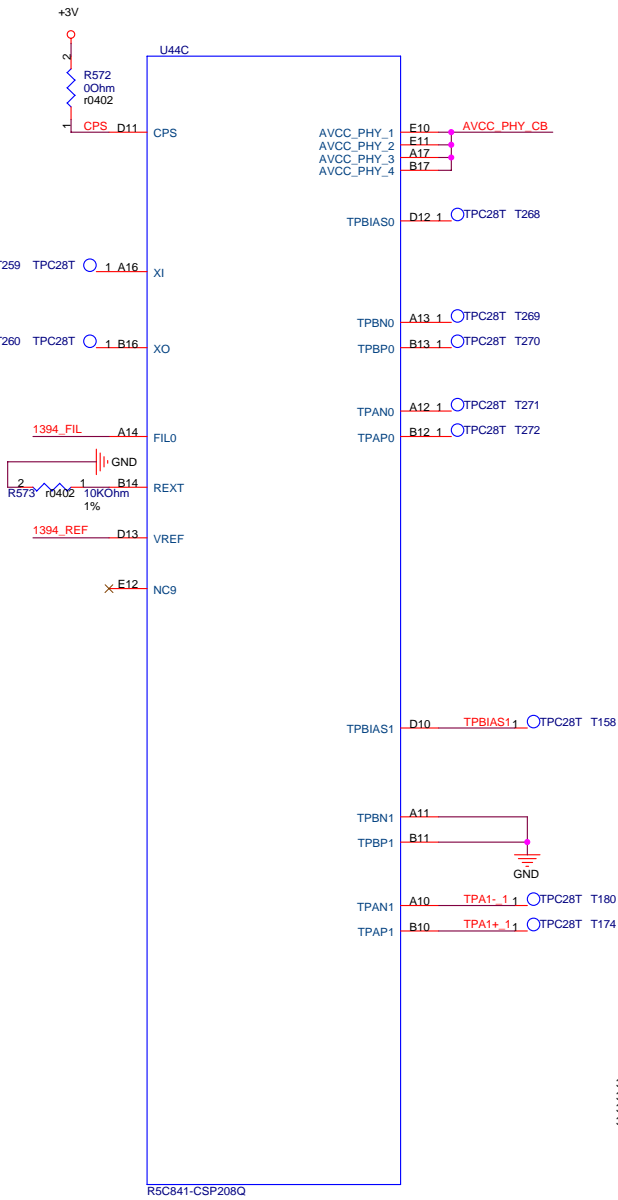
GBRST# POWER SEQ
 +3V ==> (GBRST#/CB_HWSUSP#) ==> PCIRST#

H/W SUSPEND# POWER SEQ :
 SUSPEND : CB_HWSUSP# LO=> PCIRST# LO=> +3VS OFF
 RESUME : +3VS ON => PCIRST# HI=> CB_HWSUSP# HI

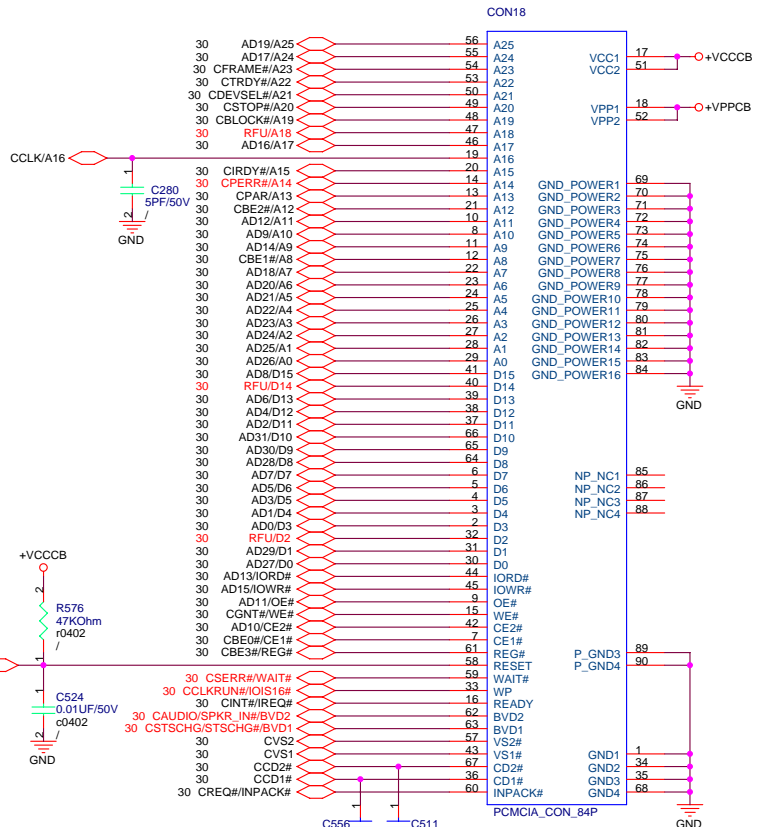
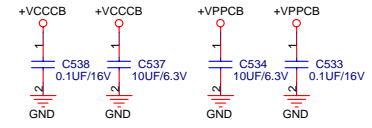
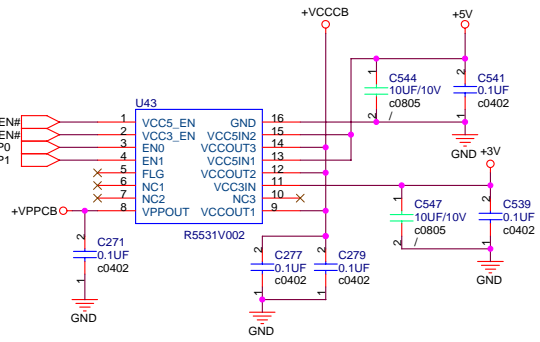
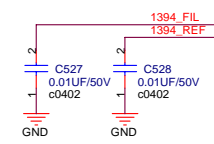
UDIO03 H : Enable SD
 UDIO04 H : Enable MS
 VPPEN0 H : Enable XD

ASUS Title : CARDBUS RICOH R5C841
 Engineer : <OrgAdd1>

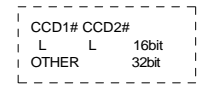
Size	Project Name	Rev
Custom	A6Rp	2.0
Date: Thursday, April 06, 2006	Sheet 30 of 50	

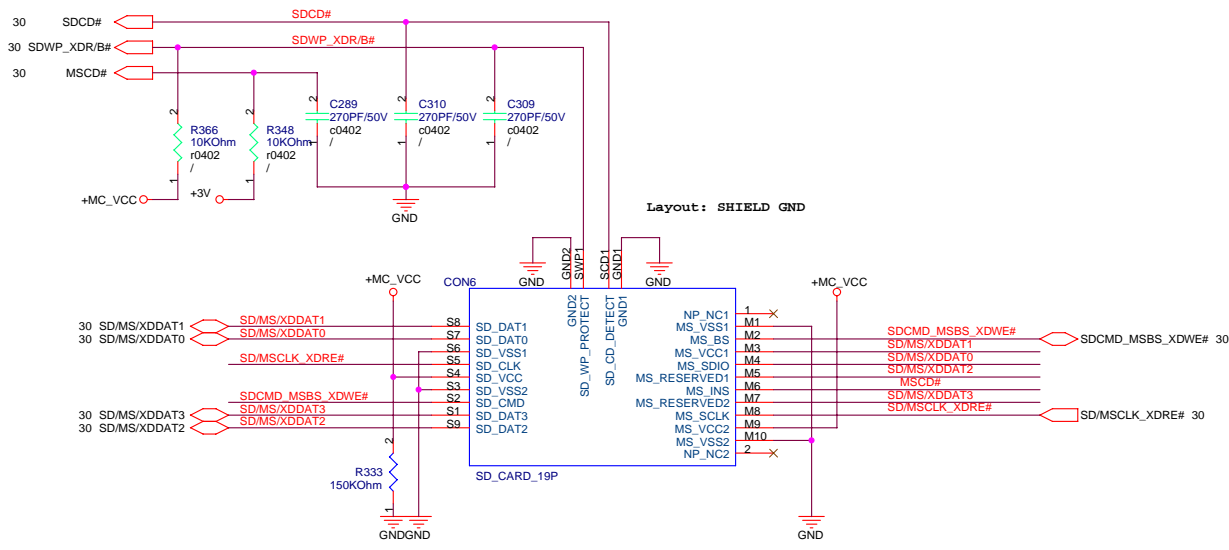
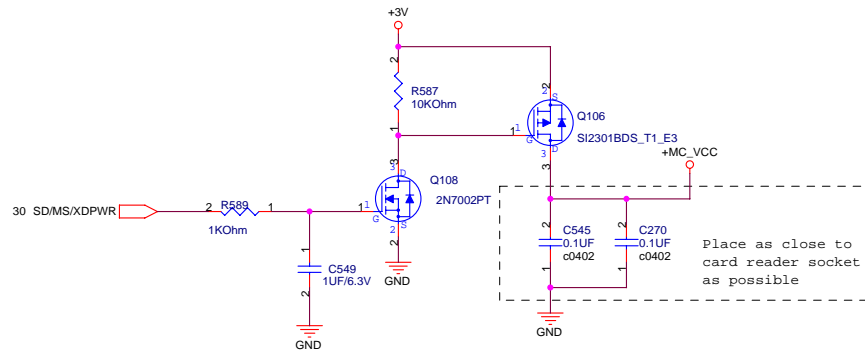
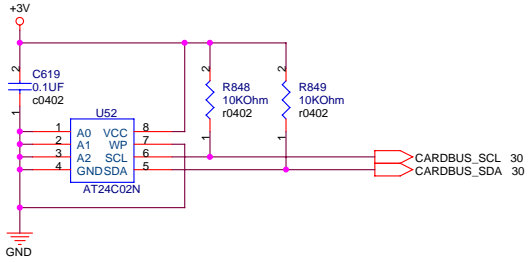


- CINT#/IREQ# 1 TPC28T T175
- CSERR#/WAIT# 1 TPC28T T166
- CREQ#/INPACK# 1 TPC28T T159
- AUDIO/SPKR_IN#/BVD2 1 TPC28T T160
- CSTOP#/A20 1 TPC28T T178
- CDEVSEL#/A21 1 TPC28T T176
- CTRDY#/A22 1 TPC28T T168
- CIRDY#/A15 1 TPC28T T169
- CSTSHG#/STSHG#/BVD1 1 TPC28T T157
- CBLOCK#/A13 1 TPC28T T171
- CPERR#/A14 1 TPC28T T179
- CCLKRUN#/IOIS16# 1 TPC28T T144

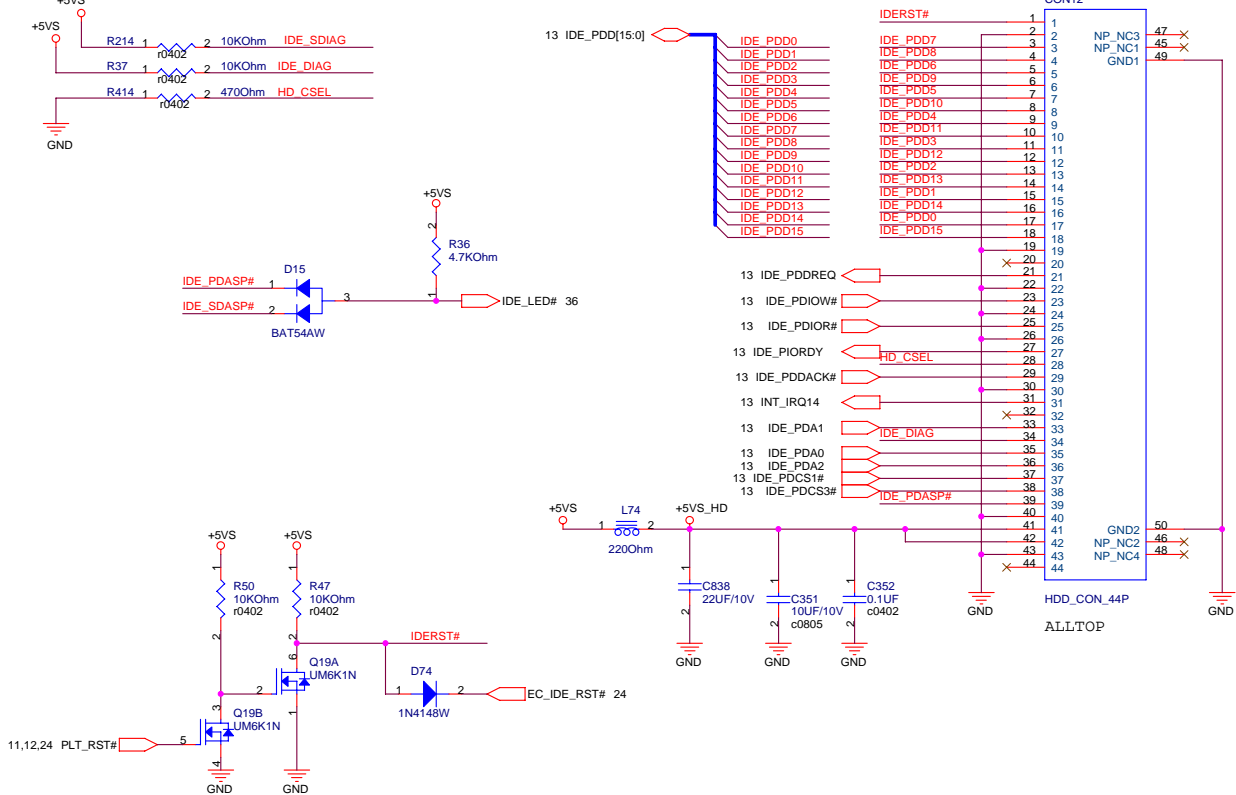


PCMCIA



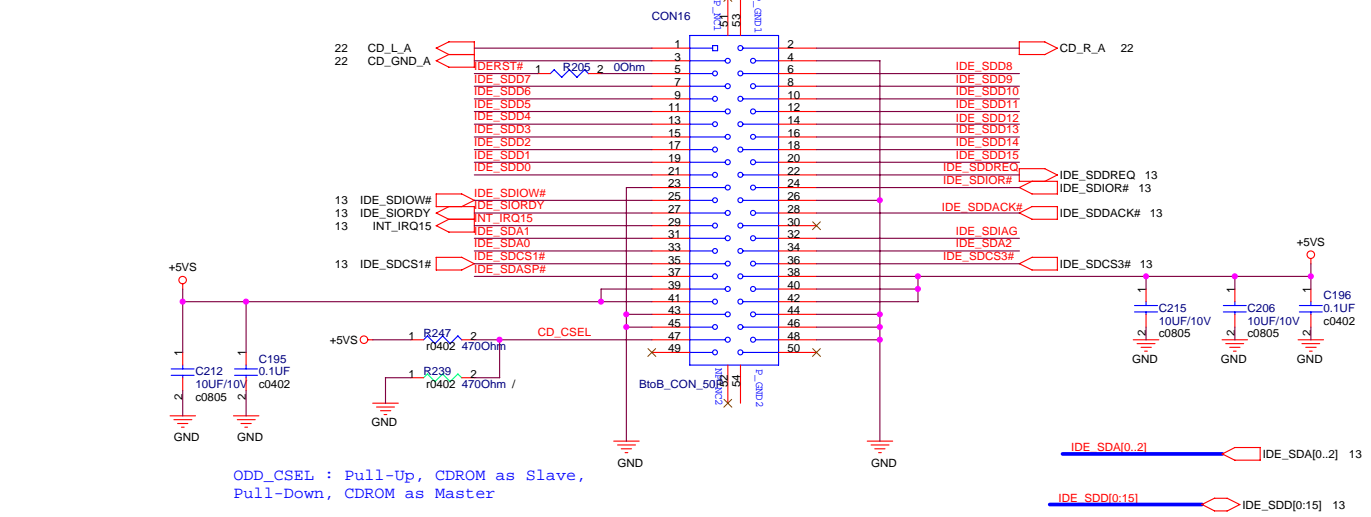


HD_CSEL : Pull-Down, HDD as Master

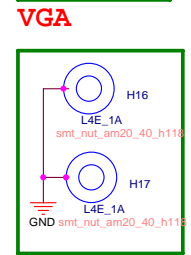
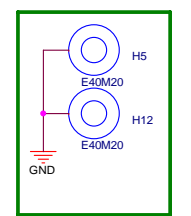
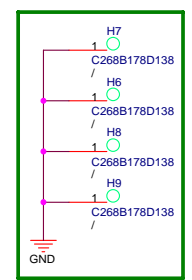


HDD

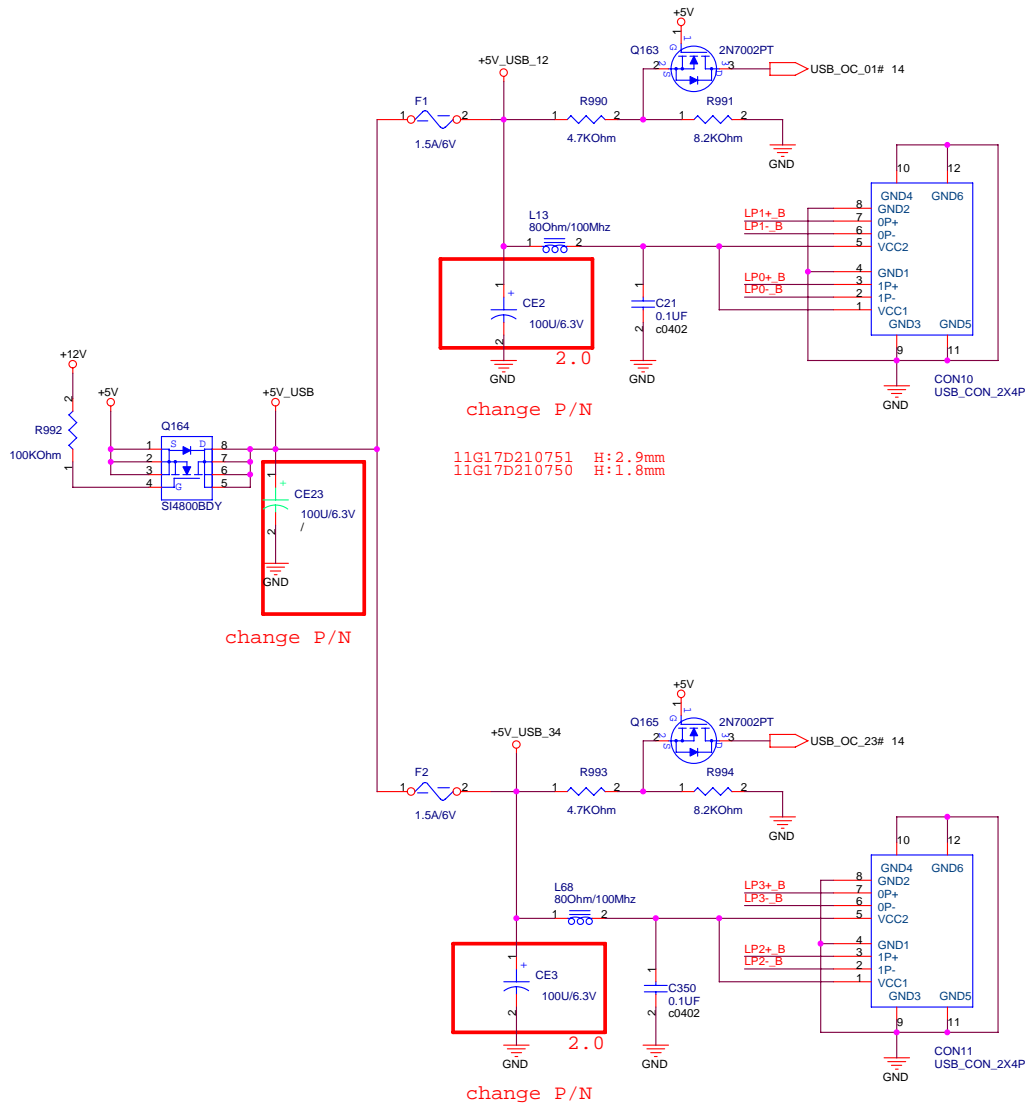
CD-ROM



ODD_CSEL : Pull-Up, CDROM as Slave,
 Pull-Down, CDROM as Master



USB

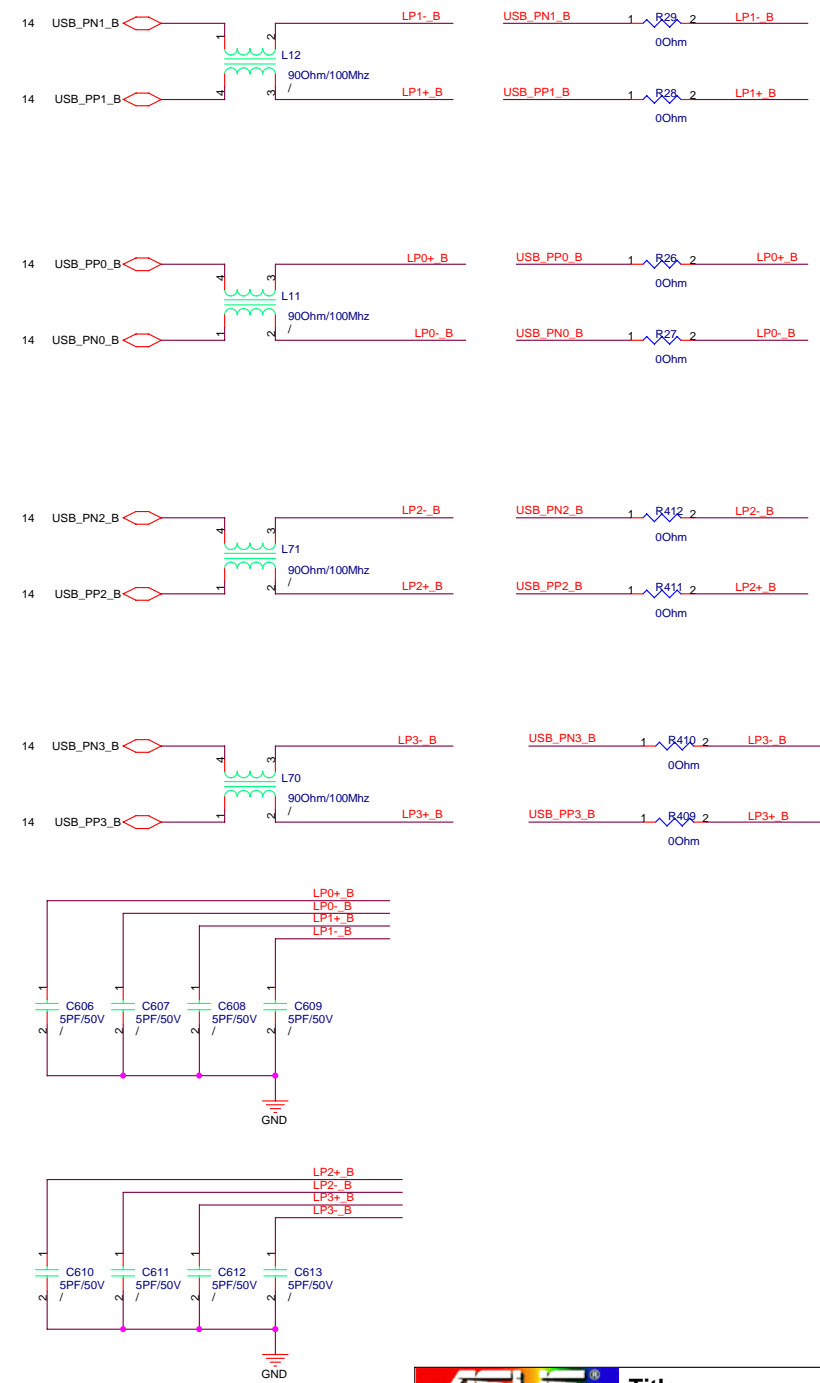


change P/N

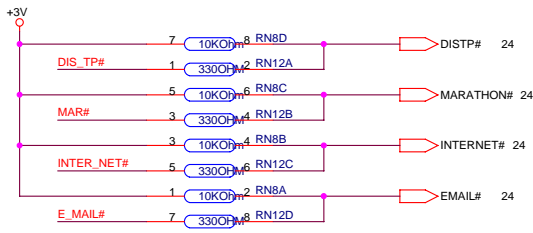
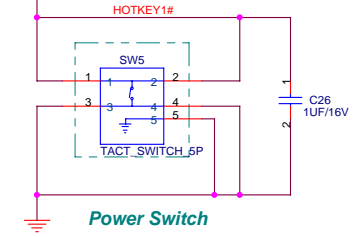
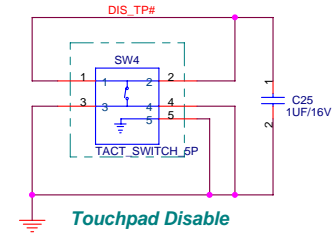
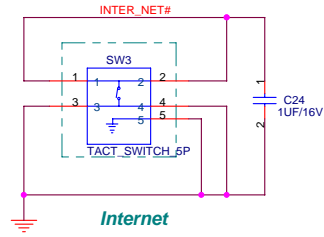
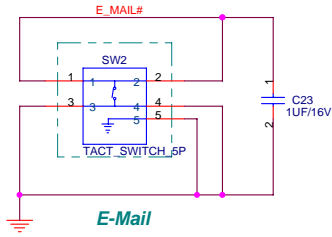
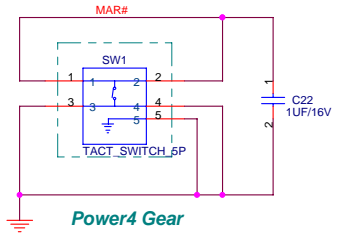
11G17D210751 H:2.9mm
11G17D210750 H:1.8mm

change P/N

change P/N

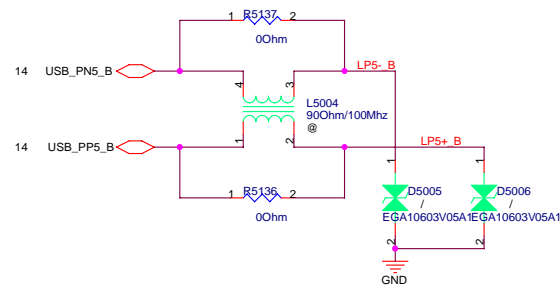
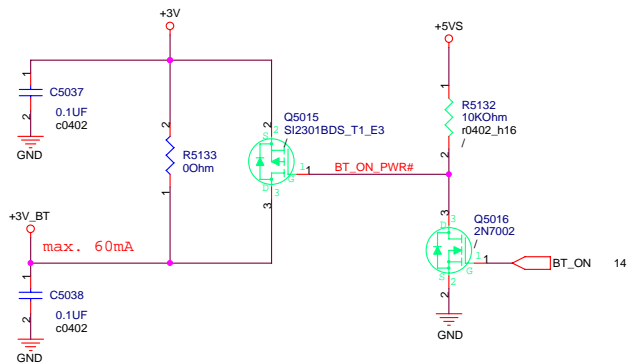


FUNCTION KEY



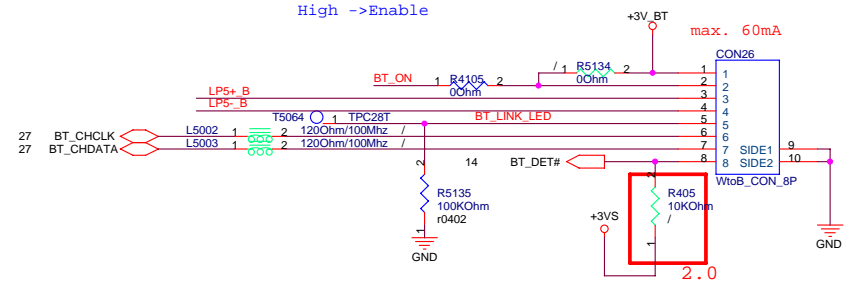
Uses 5-pin switch to improve ESD margin.

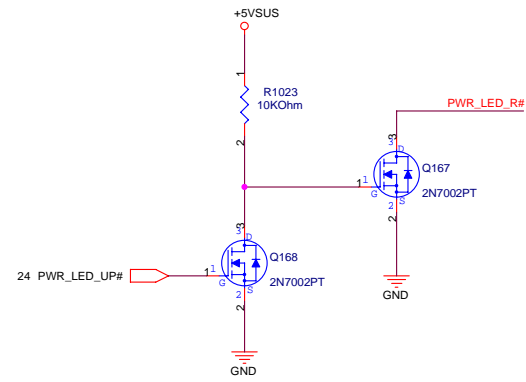
BT ON/OFF Control



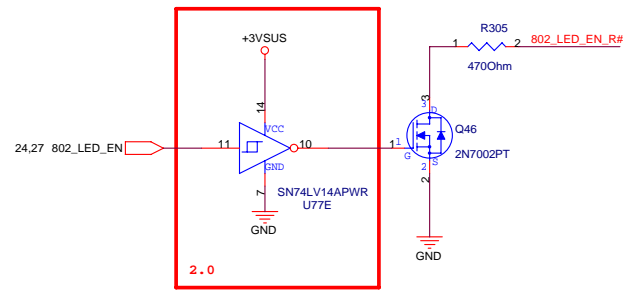
Bluetooth Module

Low -> Diable
High -> Enable

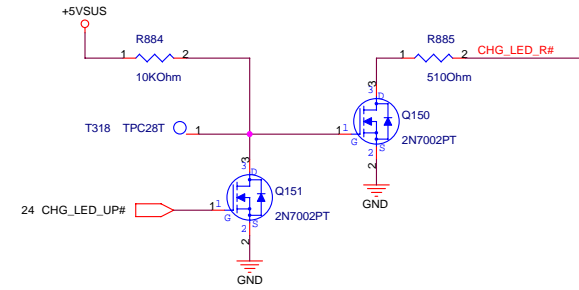




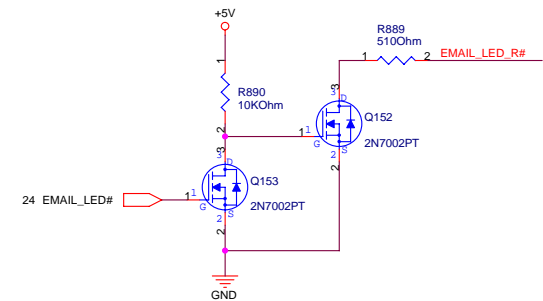
POWER_LED



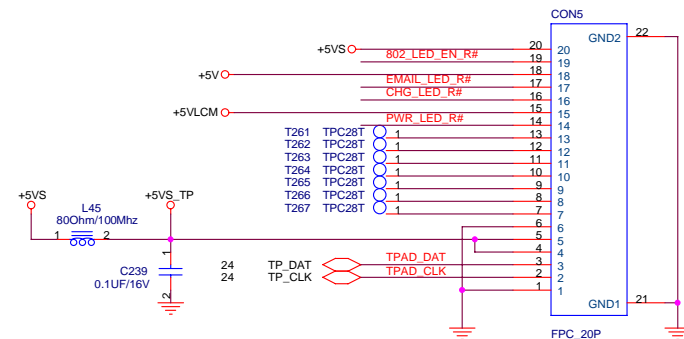
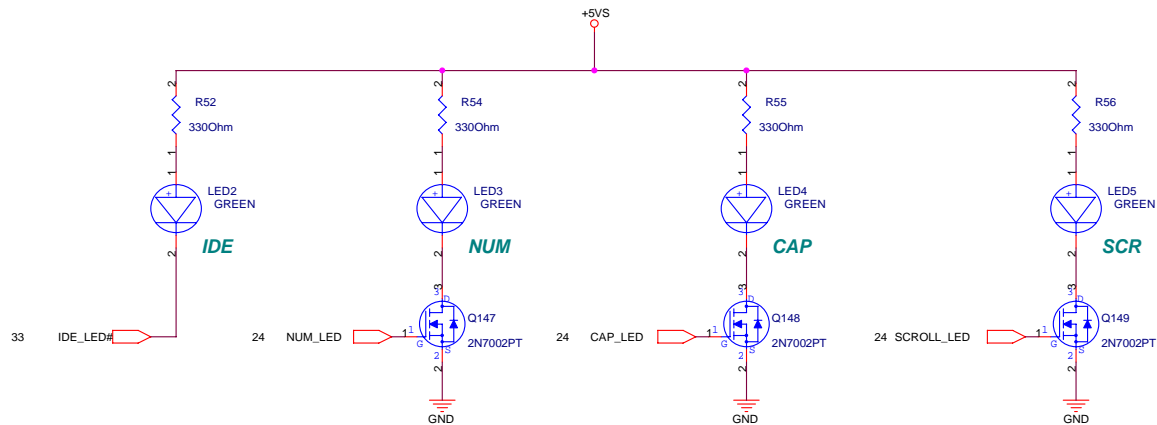
802_LED

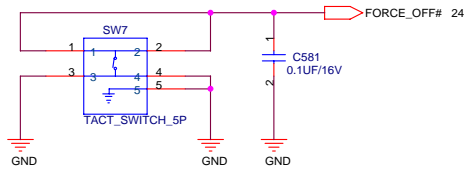


CHG_LED

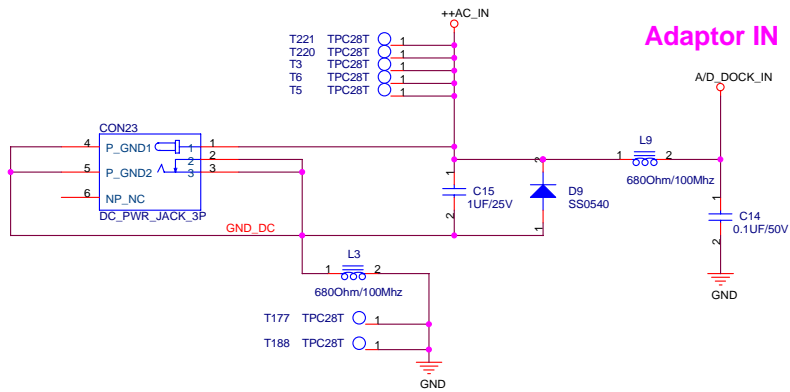


EMAIL_LED

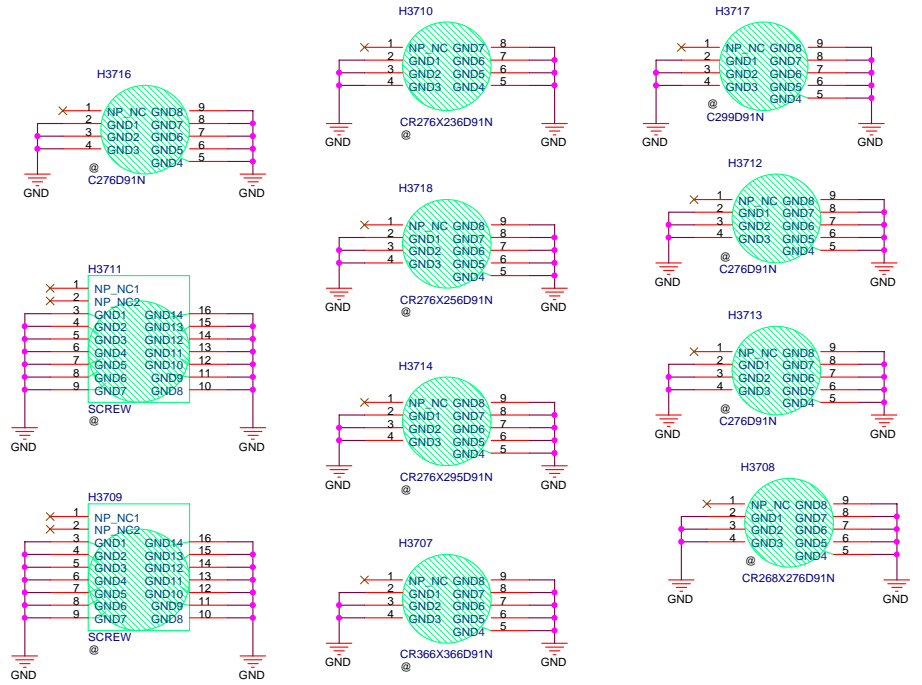


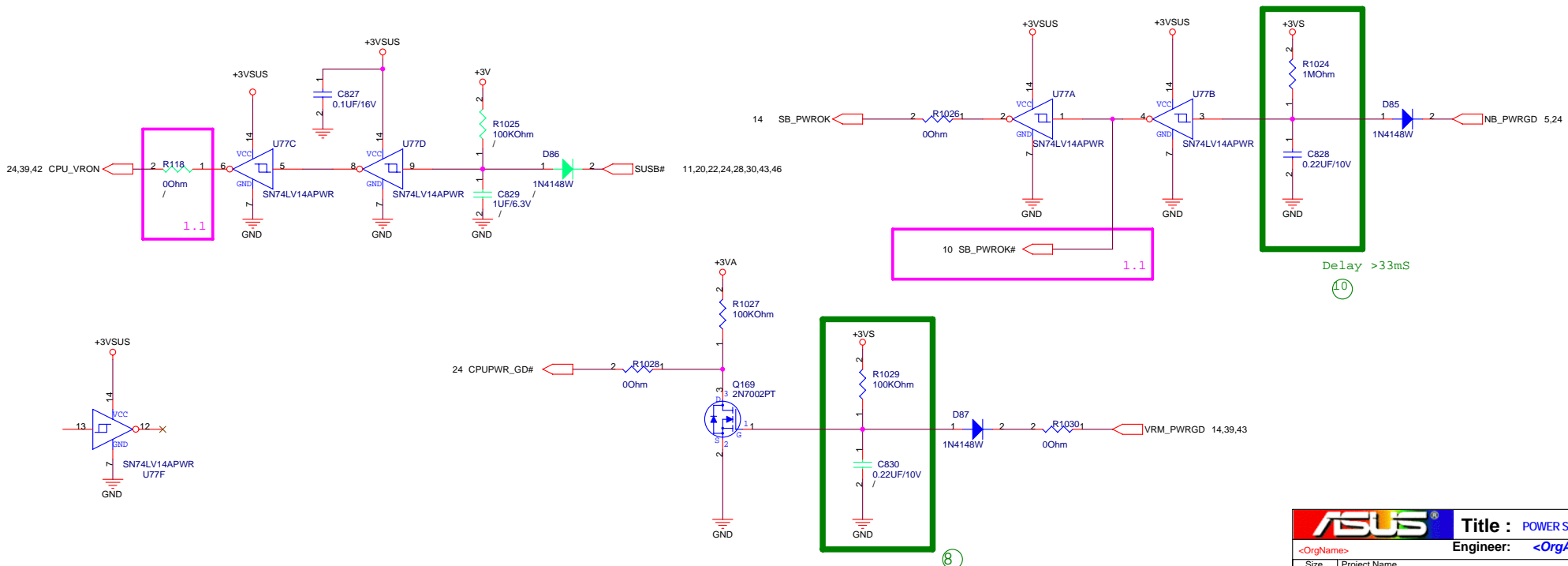
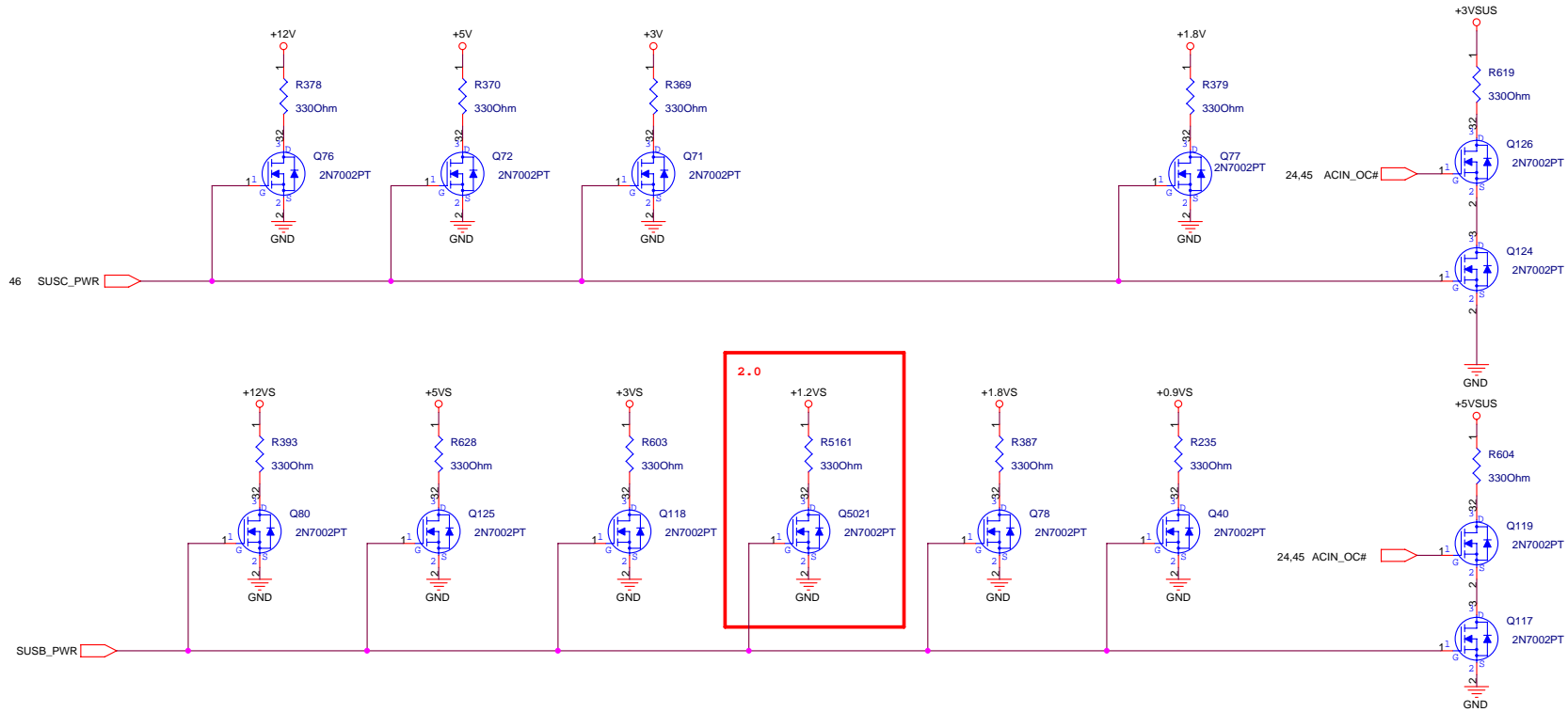


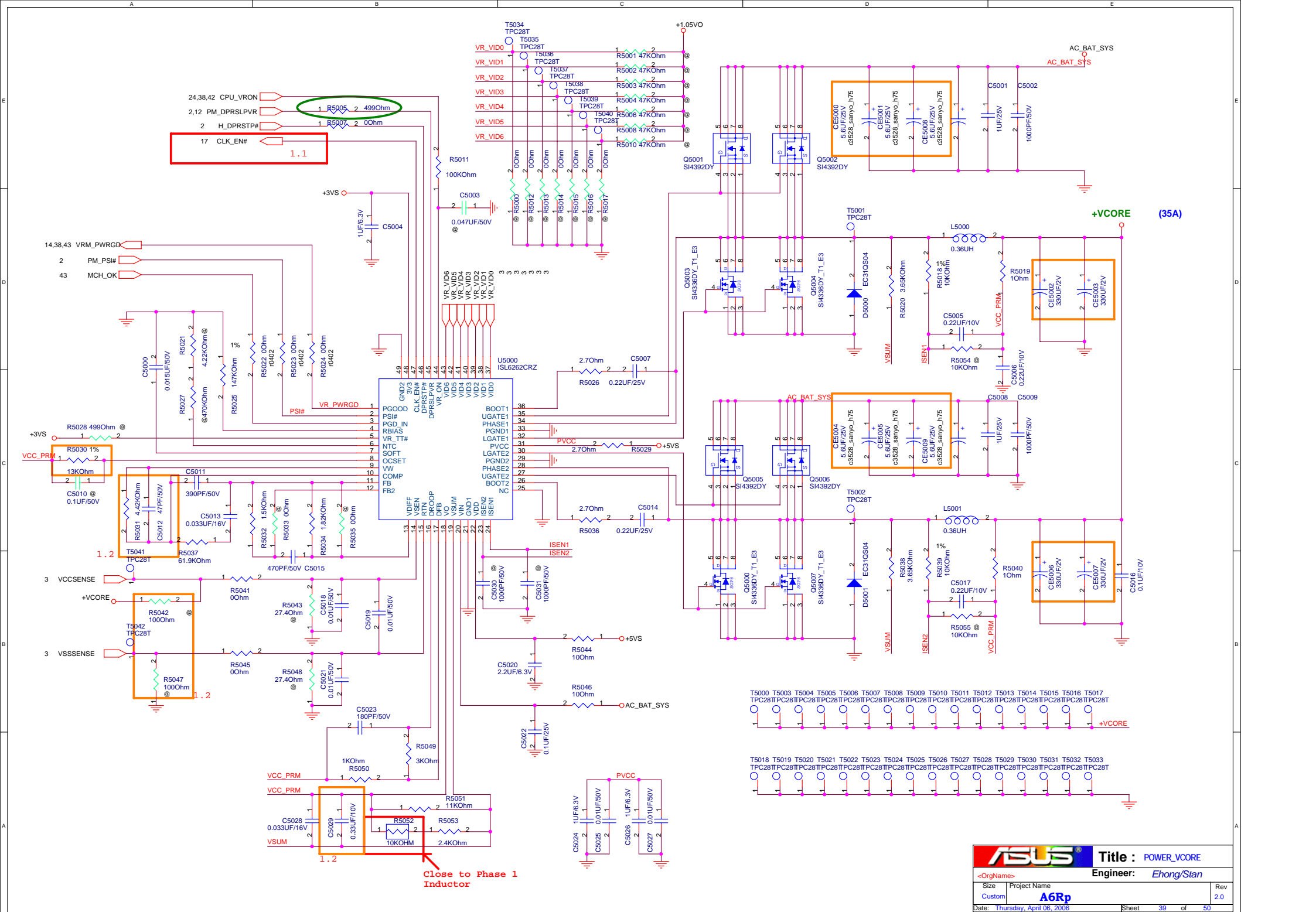
RESET SW.



Adaptor IN





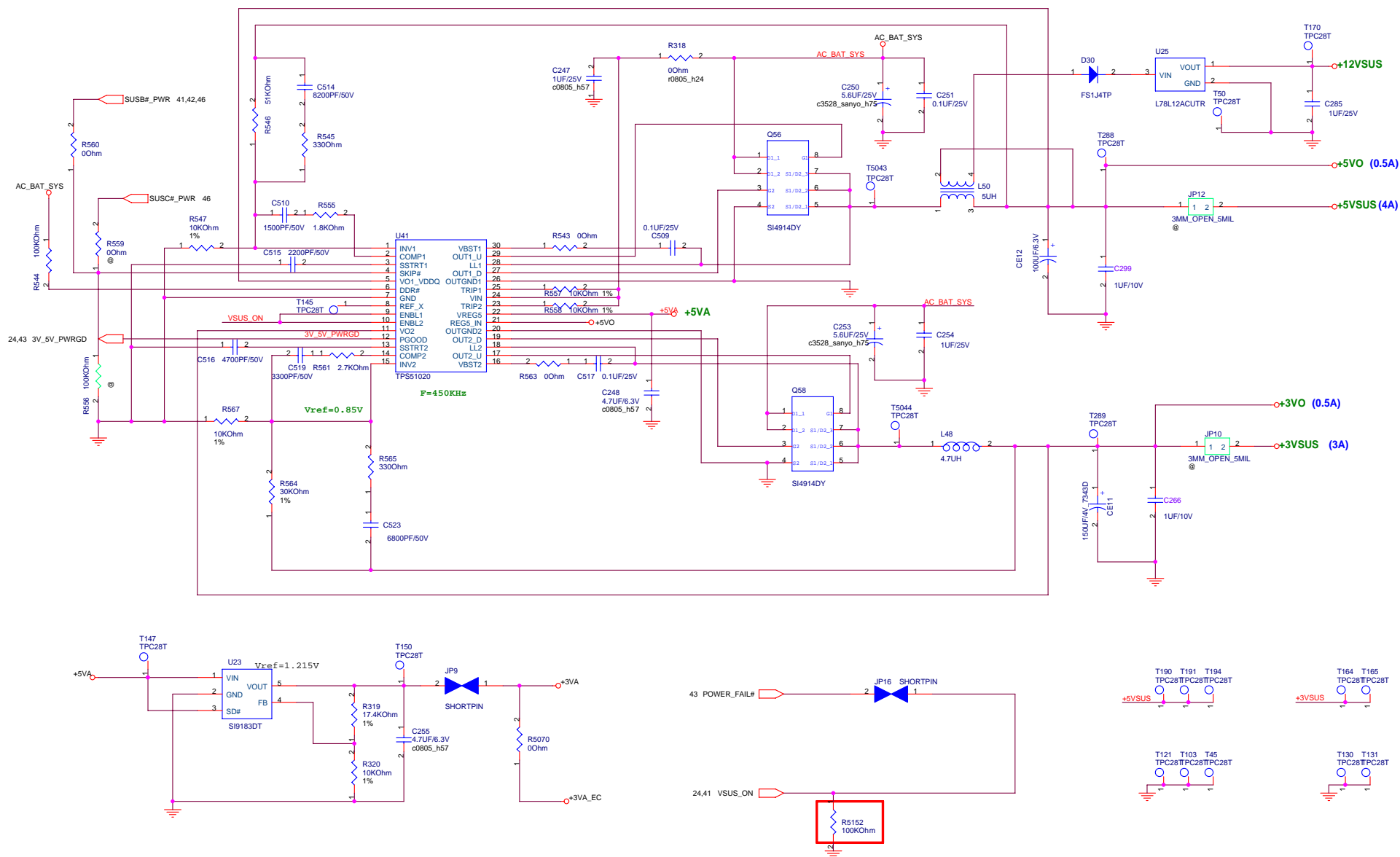


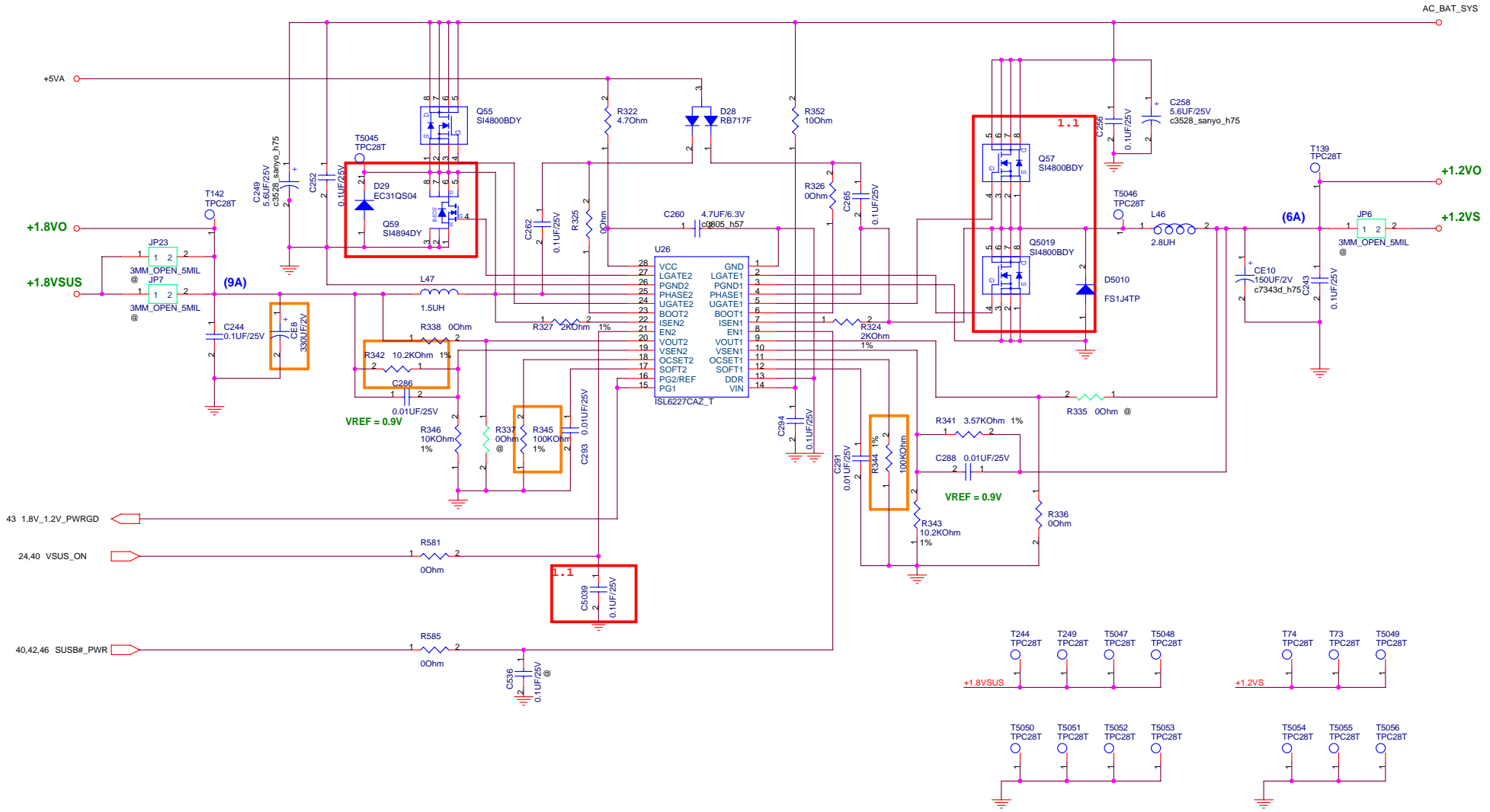
24.38,42 CPU_VRON
 2.12 PM_DPRSLPVR
 2 H_DPRSTP#
 17 CLK_EN#

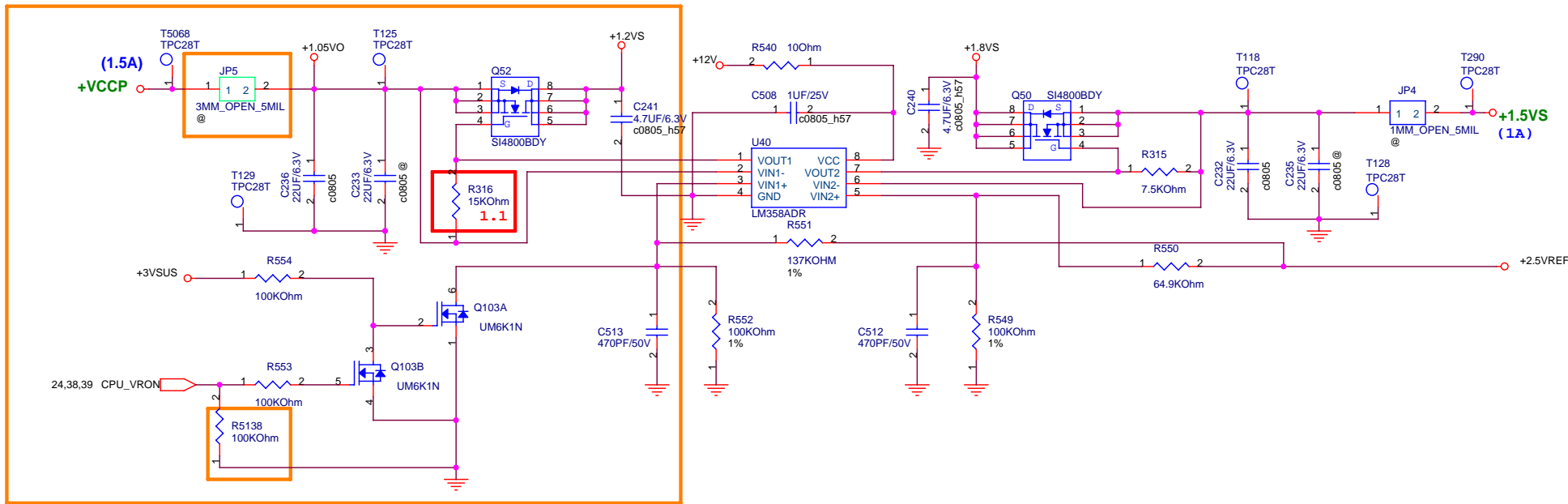
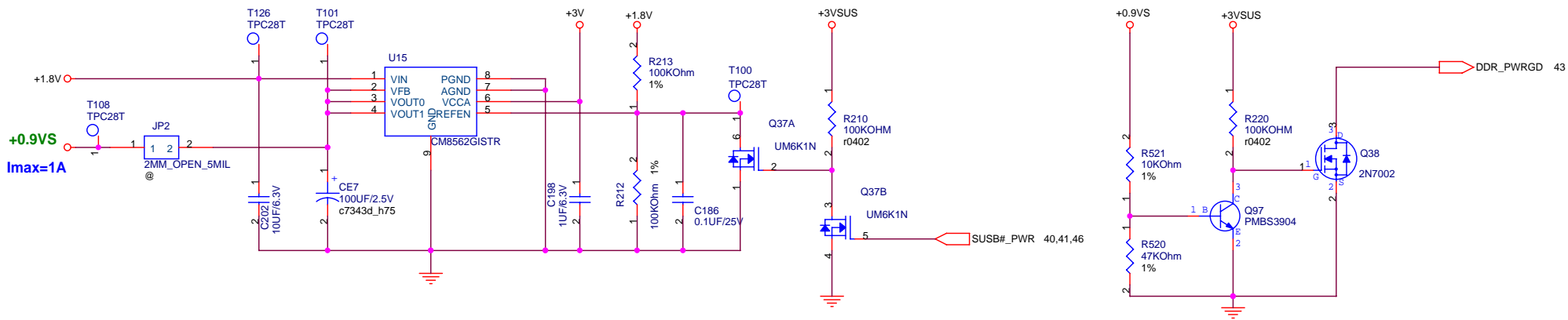
1 R5005 2 4990hm
 1 R5006 2 00hm

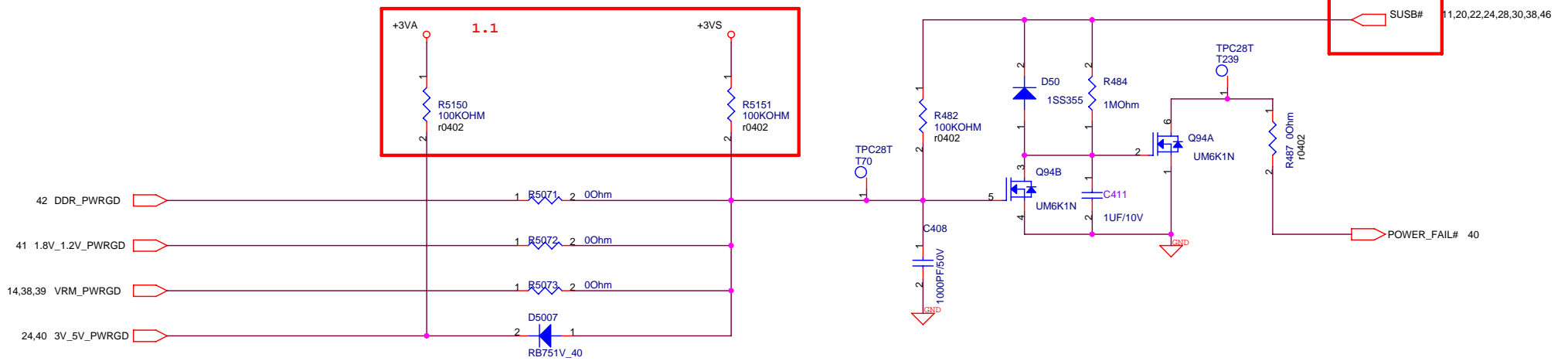
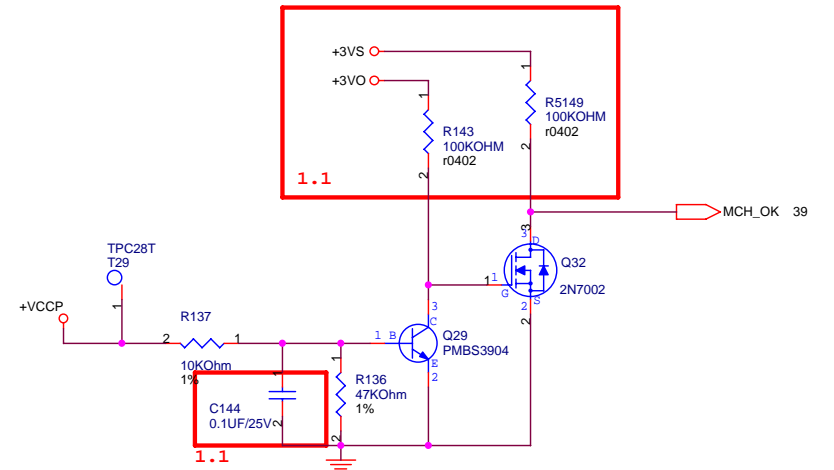
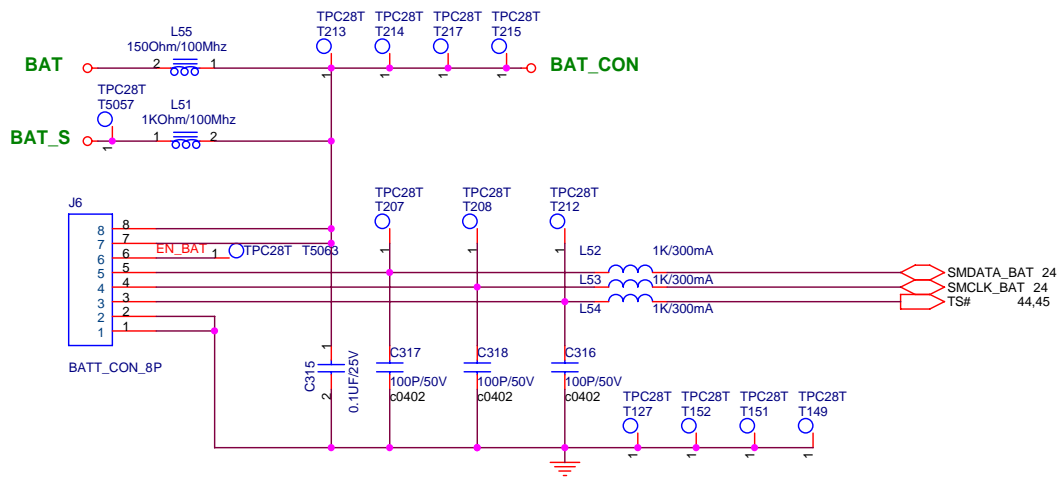
1.1

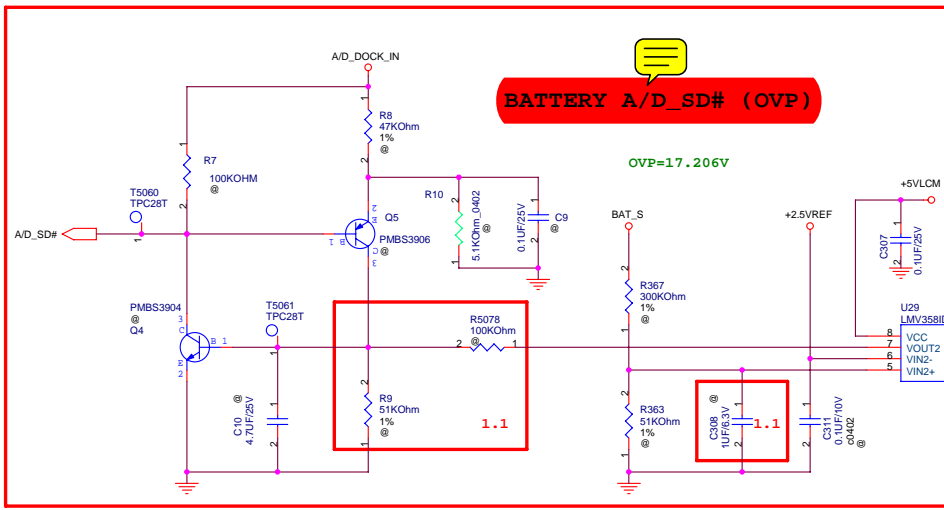
Close to Phase 1 Inductor



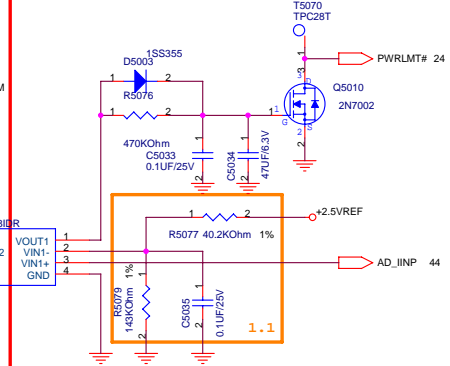




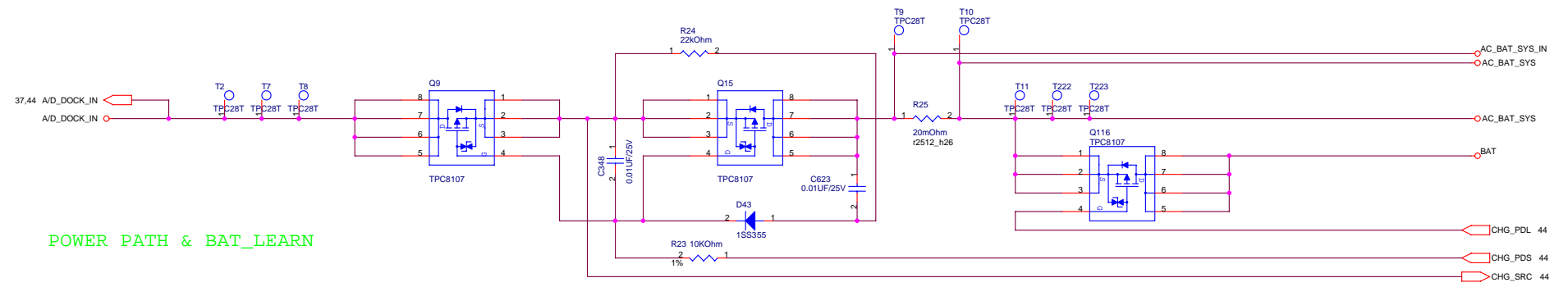
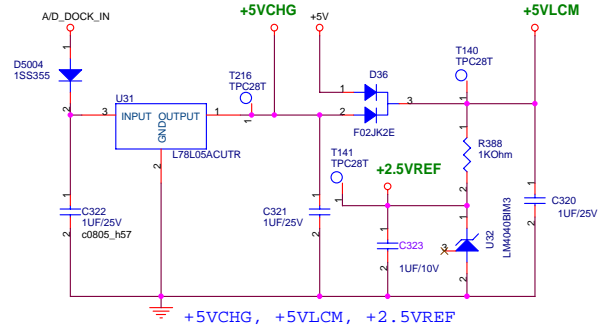
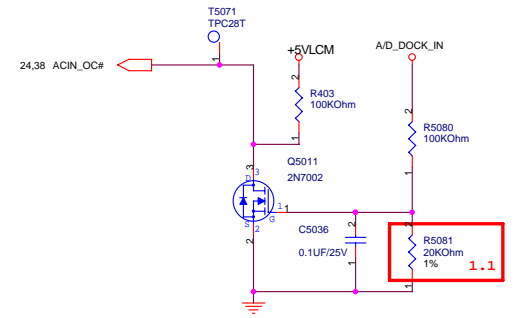
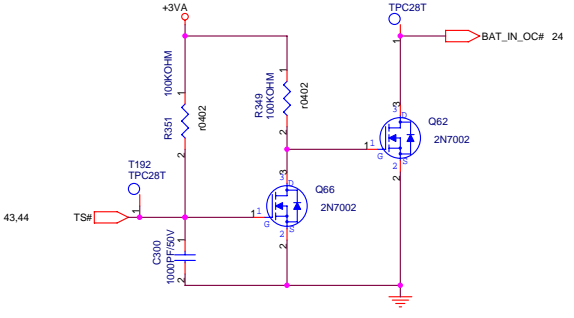


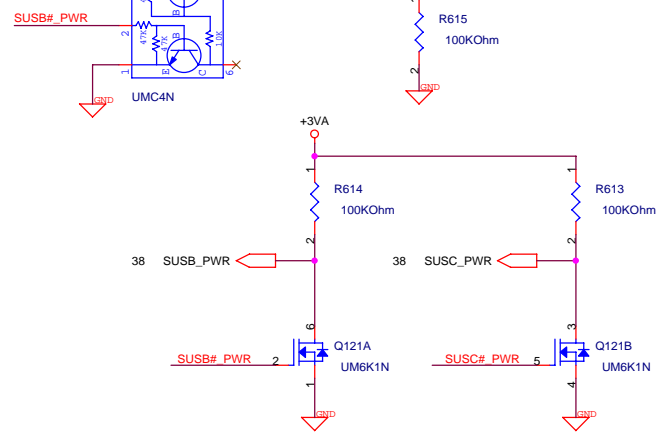
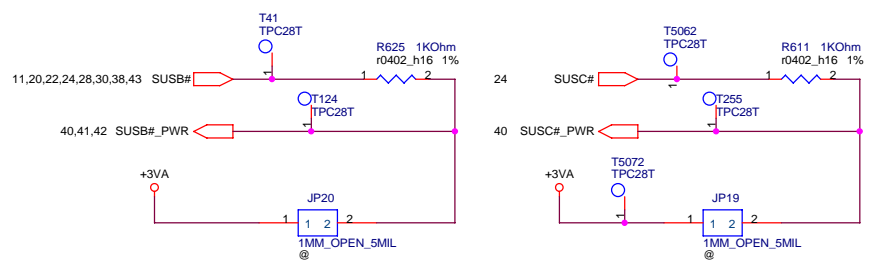
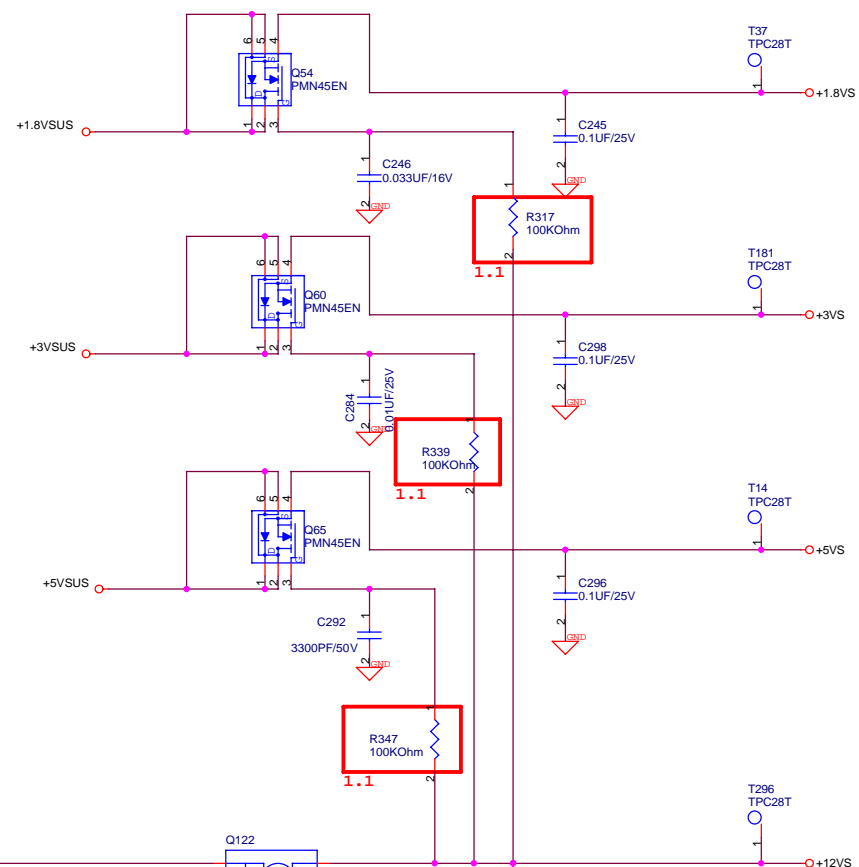
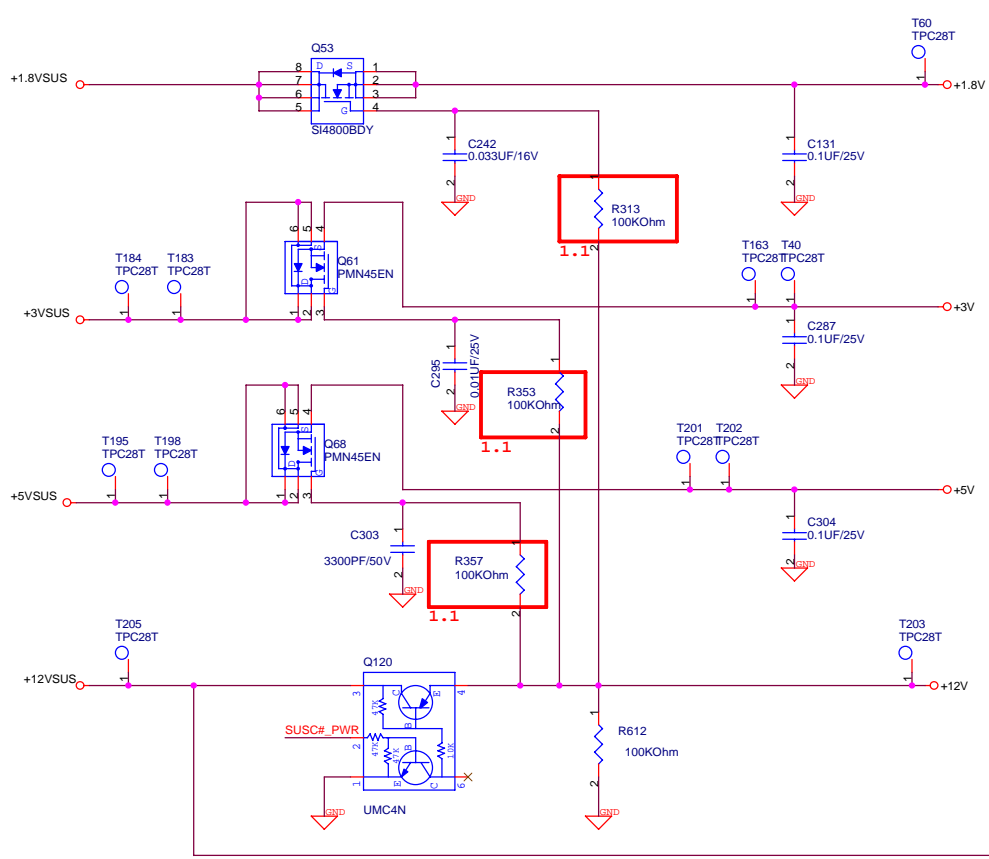


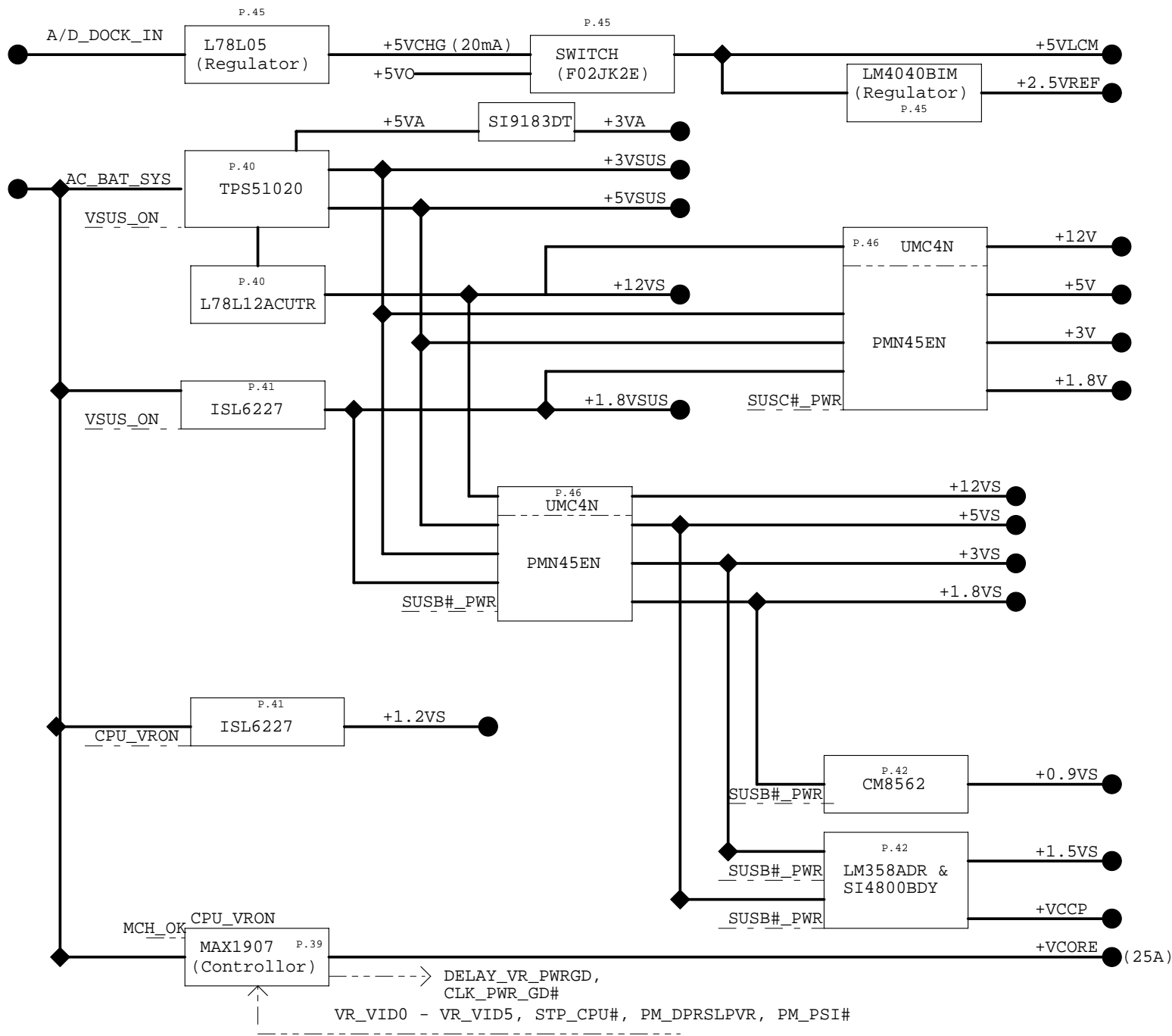
Power Limit Circuit



BATTERY IN DETECT







PCI Device	IDSEL#	REQ/GNT#	Interrupts
10/100 LAN	AD16	0	E
CARD READER	AD17	1	C
CARDBUS	AD17	1	A
1394	AD17	1	B
MINIPCI (802.11a/b/g)	AD19	3	G,H

SM-Bus Device	SM-Bus Address
Clock Generator	1101001x (D2)
SO-DIMM 0	1010000x (A0)
SO-DIMM 1	1010001x (A2)
Thermal Sensor	0101110x (5C)
PIC	1001001x (92)

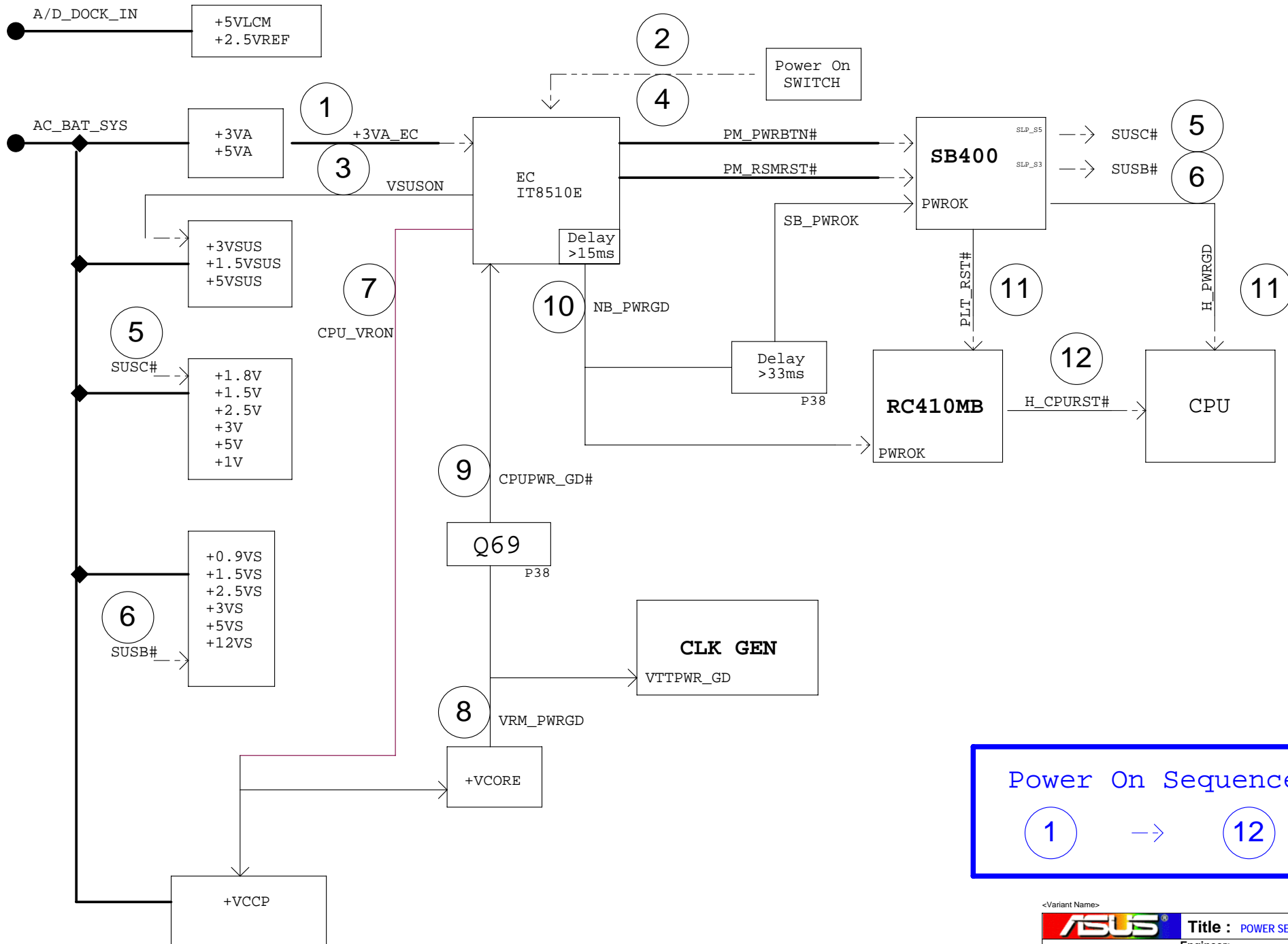
SB400 GPIO TABLE

GPIO	TYPE	POWER DOMAIN	FUNCTION
GPIO 0	I/OD	S0	
GPIO 1	I/O	S0	
GPIO 2	I/O	S0	SB_SPKR
GPIO 3	I/O	S0	FWH_WP#
GPIO 4	I/O	S0	PCB_ID0
GPIO 5	I/O	S0	PCB_ID1
GPIO 6	I/OD	S0	PCB_ID2
GPIO 7	I/O	S0	VRM_PWRGD
GPIO 8	I/O	S0	CB_SD#
GPIO 9	I/O	S0	BACK_OFF#
GPIO 10	I/O	S5	SB_PM_THERM#
GPIO 11	I/O	S0	802_LED_EN
GPIO 12	I/O	S0	WLAN_ON#
GPIO 13	I/O	S0	
GPIO 14	I/O	S0	PCI_GNT#5
GPIO 31	I/O	S0	
GPIO 32	I/O	S0	PCI_GNT#6
GPIO 33	I/O	S0	PCI_INTE#
GPIO 34	I/O	S0	PCI_INTF#
GPIO 35	I/O	S0	PCI_INTG#
GPIO 36	I/O	S0	PCI_INTH#
GPM 0	I	S5	
GPM 1	I	S5	
GPM 2	I/O	S5	
GPM 3	I	S5	
GPM 4	I	S5	
GPM 5	I	S5	
GPM 6	I/OD	S5	PWRLED_1HZ
GPM 7	I	S5	SYS_RESET#
GEVENT 0	I	S5	
GEVENT 1	I	S0	
GEVENT 2	I	S5	THRMTRIP#
GEVENT 3	I	S5	LPC_PME#
GEVENT 4	I	S5	PCI_PME#
GEVENT 5	I	S5	H_PROCHOT#
GEVENT 6	I	S5	
GEVENT 7	I	S5	
GEVENT 8			KB_SCI
EXTEVENT#0			EXT_SMI#
EXTEVENT#1			SIO_SMI#

KBC GPIO	W1V	Note
P23(Pin 35)	CHG_FULL_OC	
P22(Pin 36)	BAT_LEARN	
P21(Pin 37)	LID_EC#	
P20(Pin 38)	KBCRSM	
P42(Pin 23)		
P43(Pin 22)	OP_SD#	
P44(Pin 21)	KB_CPURST	
P45(Pin 20)	KB_GATEA20	
P46(Pin 19)	KBCSCI#	
P47(Pin 18)	PM_CLKRUN#	
P50(Pin 17)	BAT_LLOW#_OC	
P51(Pin 16)	KID0	
P52(Pin 15)	KID1	
P53(Pin 14)	CLR_DJ#	
P54(Pin 13)	BAT_SEL#	
P55(Pin 12)	BAT1_IN#_OC	
P56(Pin 11)		
P57(Pin 10)	INV_DA	
P67(Pin 74)	DJ_LED#	
P66(Pin 75)	SWDJ_EN#	
P65(Pin 76)	GAIN_AMP_K#	0->6 V/V 1->NORMAL
P64(Pin 77)	ACIN_OC	
P63(Pin 78)	DISTP#	
P62(Pin 79)	MARATHON#	
P61(Pin 80)	INTERNET#	
P60(Pin 1)	EMAIL#	
P75(Pin 4)	KB_CLK	
P74(Pin 5)	MS_CLK	
P73(Pin 6)	TPAD_CLK	
P72(Pin 7)	KB_DAT	
P71(Pin 8)	MS_DAT	
P70(Pin 9)	TPAD_DAT	
P77(Pin 2)	SMC_BAT	
P76(Pin 3)	SMD_BAT	
P27(Pin 31)	SCROLL_LED#	
P26(Pin 32)	NUM_LED#	
P25(Pin 33)	CAP_LED#	
P24(Pin 34)	SET_PLTRSTNS#	
P40(Pin 27)	EXT_SMI	
P41(Pin 26)	EMAIL_LED#	

Rev	Date	Description
1.0	05/03/01	1. Initial release.

Rev	Date	Description



Power On Sequence

1 → 12