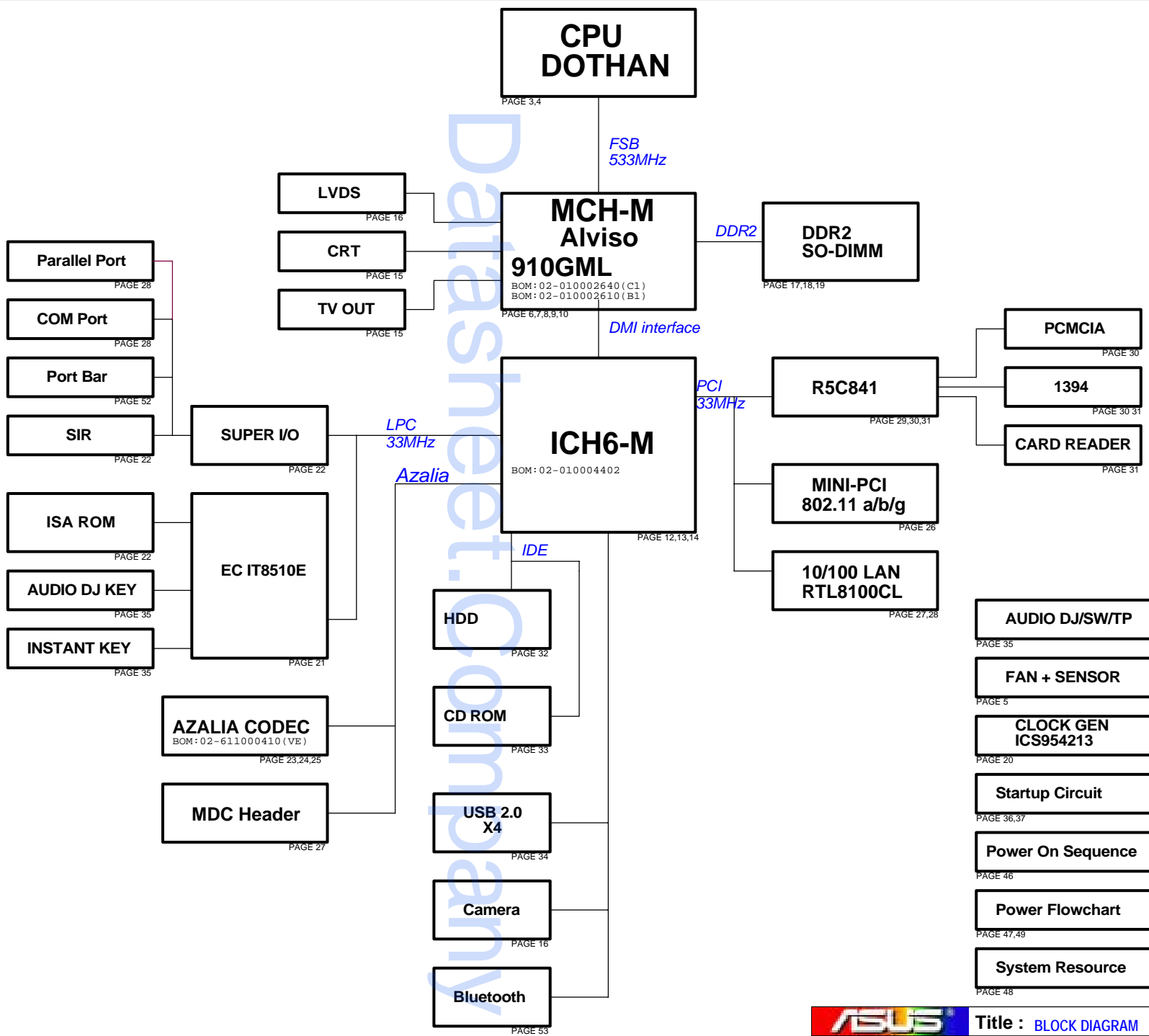


A3H CONTEXT

- 01_BLOCK DIAGRAM
- 02_REVISION LIST
- 03_DOYHAN CPU(1)
- 04_DOTHAN CPU(2)
- 05_THERMAL SENSOR,FAN
- 06_ALVISO GMCH(1)
- 07_ALVISO PCIE(2)
- 08_ALVISO DDR SLOT(3)
- 09_ALVISO POWER(4)
- 10_ALVISO GND(5)
- 11_GMCH STRAPPING/LVDS TRANS
- 12_ICH6M SATA,LPC,IDE(1)
- 13_ICH6M USB,PCI/E,PMIO(2)
- 14_ICH6M PWR,GND(3)
- 15_CRT&TV OUT CONN
- 16_LVDS&INVERTER(CAMERA,WLAN)
- 17_DDR2_SODIMM 0
- 18_DDR2_SODIMM 1
- 19_DDR2_ADDRESS TERMINATION
- 20_CLOCK GEN ICS954213
- 21_IT8510E
- 22_FWH,SIO,SIR
- 23_AZALIA ALC880
- 24_AMPLIFIER 2 CHANNEL
- 25_MIC,LINE-IN JACK
- 26_MINI-PCI
- 27_LAN RTL8100CL
- 28_RJ11/45,MDC,PRN
- 29_PCI CARDBUS R5C841
- 30_PCI PCMCIA SOCKET A
- 31_PCI IEEE1394A,3IN1 CON
- 32_HDD CONNECTOR
- 33_Q/SW,CD-ROM CONNECTOR
- 34_USB CONNECTOR
- 35_DJ BOARD/SW/TP
- 36_STARTUP CIRCUIT(1)
- 37_STARTUP CIRCUIT(2)
- 38_VCORE
- 39_SYSTEM(3V,5V)
- 40_2.5V,1.5V,1.8V,1.05V
- 41_VCCA,DDR2(0.9V)
- 42_PIC/BAT CONN/PWOK/THERM PT
- 43_CHARGE
- 44_BATLOW/SD#
- 45_LOAD SWITCH
- 46_POWER ON SEQUENCE
- 47_POWER FLOW CHART
- 48_SYSTEM RESOURCE
- 49_POWER FLOW DIAGRAM
- 50_HISTORY



REVISION LIST

POWER INTERFACE

SIGNALS TYPE POWER

PM_PSI#	O	+VCCP
VR_VID[5:0]	O	+VCCP
VRON	O	+3.3V
PM_DPRSLPVR	O	+3.3V
CPU_STP#	O	+3.3V
RST_BTN#	O	+3.3V
CLK_EN#	I	+3.3V
DELAY_VR_PWRGD	I	+3.3V
OTP_RESET#	I	+3.3V
SHUT_DOWN#	I	+3.3V
BAT_LEARN	I	+3.3V
BAT_LLOW#_OC	I	+3.3V
BAT_IN#_OC	I	+3.3V
CHG_EN#	I	+3.3V
CHG_FULL_OC	I	+3.3V
CHG_LED_UP	I	+3.3V
SMCLK_BAT1	IO	+3.3V
SMDATA_BAT1	IO	+3.3V
SUSB#	O	+3.3V
SUSC#	O	+3.3V
1.8V_PWRGD	I	+3.3V
1.5VS_PWRGD	I	+3.3V
VSUS_ON	O	+3.3V
ACIN_OC	I	+3.3V
ACIN#	I	AC_BAT_SYS
+3VA	PWR	+3.3V
+5VA	PWR	+5V
+5VLCM	PWR	+5VLCM
A/D_DOCK_IN	PWR	DC
AC_BAT_SYS	PWR	DC

POWER PLANE

POWER	VOLTAGE	CURRENT
+VCORE	0.7 - 1.77V	27A
+VCCP	1.05 - 1.2V	3.95A
+VCC_GMCH	1.05V	4.12A
+0.9VS	1.25V	0.85A
+1.5VS	1.5V	4.33A
+1.5V	1.5V	300 mA
+1.5VSUS	1.5V	270 mA
+1.8V	1.8V	6.68A
+2.5VS	2.5V	0.3 A
+3VS	3.3V	1.732A
+3V	3.3V	1.515A
+3VSUS	3.3V	540 mA
+5VS	5V	4.1A
+5V	5V	0.5A
+5VSUS	5V	0.5A
+12V	12V	0.25A
+12VS	12V	0.25A

IMPEDENCE

Single-Ended

<u>27.4 OHM WIDTH</u>
TOP/BOT 18 mils
<u>37.5 OHM WIDTH</u>
TOP/BOT 11 mils
IN1/IN2 9.5 mils
<u>42 OHM WIDTH</u>
TOP/BOT 9 mils
IN1/IN2 7.5 mils
<u>50 OHM WIDTH</u>
TOP/BOT 6 mils
IN1/IN2 5 mils
<u>55 OHM WIDTH</u>
TOP/BOT 5.5 mils
IN1/IN2 4.5 mils
<u>75 OHM WIDTH</u>
TOP/BOT 4 mils
IN1/IN3 3.5 mils
<u>70 OHM WIDTH/SPACE</u>
TOP/BOT 9 mils/ 4 mils
IN1/IN2 7.5 mils/ 4 mils
<u>85 OHM WIDTH/SPACE</u>
TOP/BOT 5.5 mils/ 4 mils
IN1/IN2 4.5 mils/ 4 mils
<u>90 OHM WIDTH/SPACE</u>
TOP/BOT 5.5 mils/ 5 mils
IN1/IN2 4.5 mils/ 5 mils
<u>100 OHM WIDTH/SPACE</u>
TOP/BOT 6 mils/ 11 mils
IN1/IN2 5 mils/ 12 mils
<u>110 OHM WIDTH/SPACE</u>
TOP/BOT 5 mils/ 13 mils
IN1/IN2 4 mils/ 12 mils

Differential

<u>70 OHM WIDTH/SPACE</u>
TOP/BOT 9 mils/ 4 mils
IN1/IN2 7.5 mils/ 4 mils
<u>85 OHM WIDTH/SPACE</u>
TOP/BOT 5.5 mils/ 4 mils
IN1/IN2 4.5 mils/ 4 mils
<u>90 OHM WIDTH/SPACE</u>
TOP/BOT 5.5 mils/ 5 mils
IN1/IN2 4.5 mils/ 5 mils
<u>100 OHM WIDTH/SPACE</u>
TOP/BOT 6 mils/ 11 mils
IN1/IN2 5 mils/ 12 mils
<u>110 OHM WIDTH/SPACE</u>
TOP/BOT 5 mils/ 13 mils
IN1/IN2 4 mils/ 12 mils

PCI INTERFACE

PCI_REQ#

MINIPCI	PCI_REQ#3
10/100	PCI_REQ#2
CB&1394	PCI_REQ#1

IDSEL

MINIPCI	PCI_AD19
10/100	PCI_AD16
CB&1394	PCI_AD17

PCB STACK-UP

PCB THICKNESS: 1.6 mm

- L1 TOP
- L2 GND
- L3 IN1
- L4 IN2
- L5 GND
- L6 BOT

PAGE 38

SIGNAL	IN:	VR_VID[0..5] PM_DPRSLPVR STP_CPU# PM_PSI# CPU_VRON MCH_OK
	OUT:	DELAY_VR_PWRGD CLK_PWR_GD#
POWER	IN:	AC_BAT_SYS +5VO +3VO
	OUT:	+VCORE

PAGE 39

SIGNAL	IN:	SUSC#_PWR VSUS_ON
POWER	IN:	AC_BAT_SYS
	OUT:	+12VO +3VO +5VO

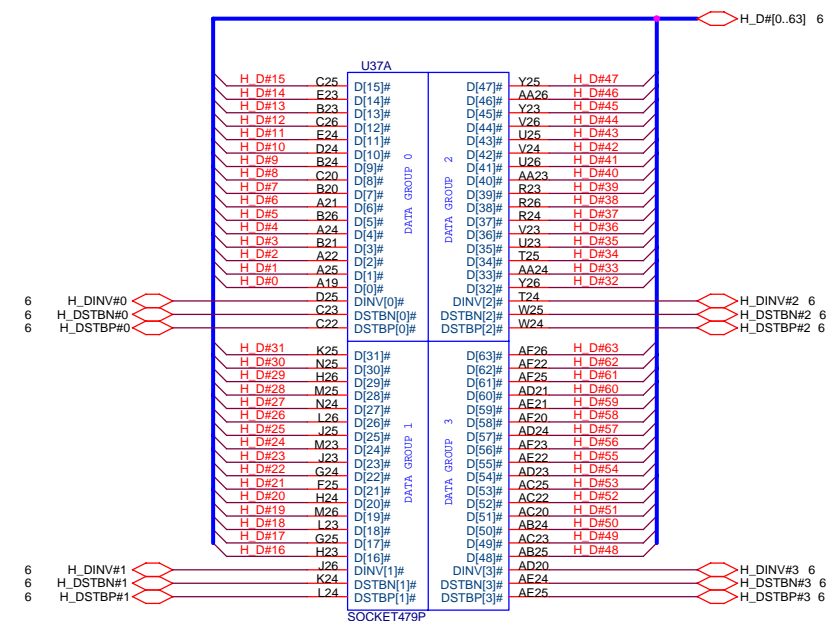
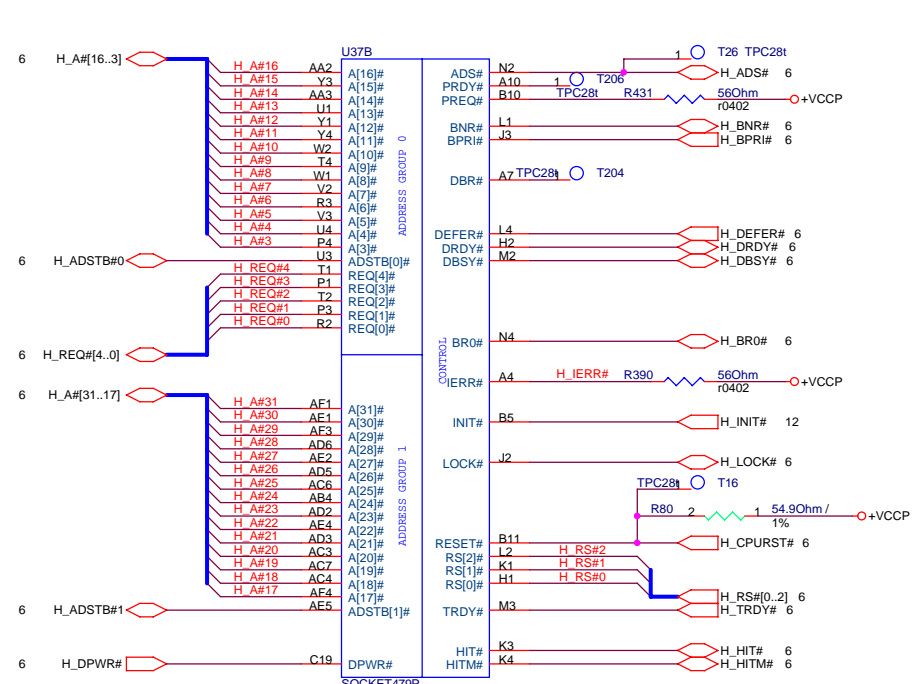
PAGE 40

SIGNAL	IN:	SUSB#_PWR SUSC#_PWR CPU_VRON
POWER	IN:	AC_BAT_SYS +5VO
	OUT:	+1.8V +1.5VS +2.5VS +VCC_GMCH_CORE +5VALWAYS +3VALWAYS +VCCP

PAGE 41

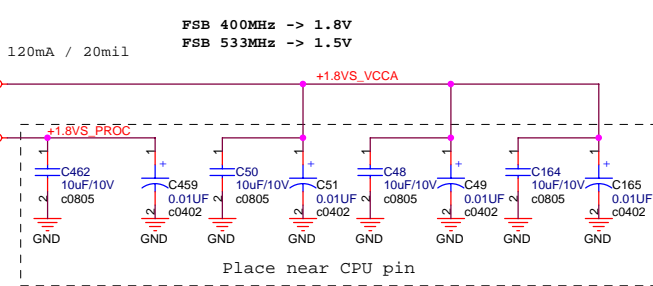
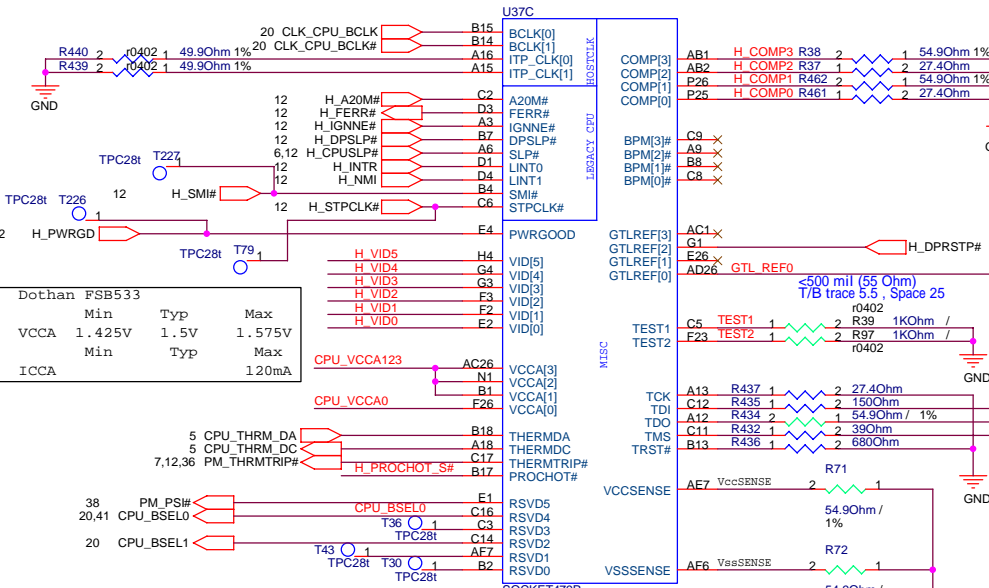
SIGNAL	IN:	SUSB#_PWR
POWER	IN:	+3V +1.8V
	OUT:	+0.9VS

		Title : REVISION LIST	
ASUSTeK COMPUTER INC		Engineer: Howard Tu	
Size	Project Name	Date	Rev
Custom	A3H	Thursday, June 30, 2005	1.0
Date: Thursday, June 30, 2005		Sheet	2 of 54

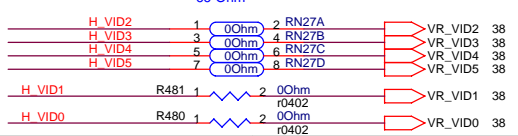


Layout note:
 COMP0 and COMP2 need to be Zo=27.4ohm traces.
 Best estimate is 18mil wide trace for outer layers and 14mil if on internal layer. See RDDP of Banias.
 Traces should be shorter than 0.5". Refer to latest CS layout

COMP1, COMP3 should be routed as Zo=55ohm traces shorter than 0.5"



B-STEP			
Bclk	FSB	BSEL1	BSEL0
100	400	0	1
133	533	0	0

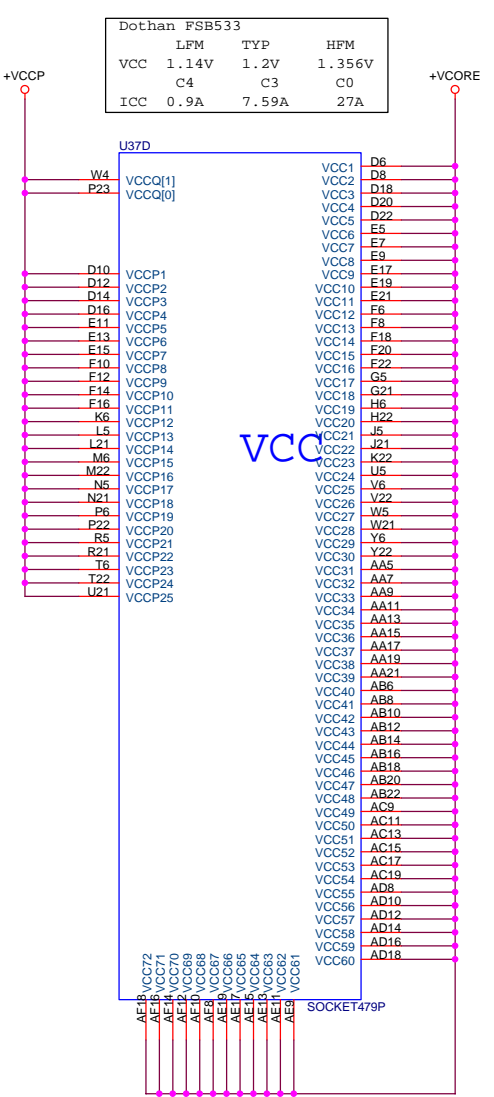


ASUS Title : **DOTHAN CPU (1)**

ASUSTek COMPUTER INC Engineer: **Howard Tu**

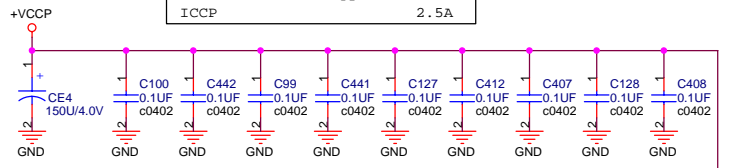
Size	Project Name	Rev
Custom	A3H	1.0

Date: Thursday, June 30, 2005 Sheet 3 of 54

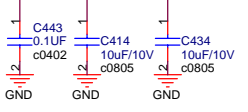


Dothan FSB533			
LFM	TYP	HFM	
VCC 1.14V	1.2V	1.356V	
C4	C3	C0	
ICC 0.9A	7.59A	27A	

Dothan FSB533			
Min	Typ	Max	
VCCP 0.997V	1.05V	1.102V	
ICC		2.5A	



+VCCP (CPU) Decoupling Capacitor (Place near CPU)



GND

MOBILE DOTHAN VID TABLE

VID[5..0]	Voltage	VID[5..0]	Voltage
000000	1.708V	100000	1.196V
000001	1.692V	100001	1.180V
000010	1.676V	100010	1.164V
000011	1.660V	100011	1.148V
000100	1.644V	100100	1.132V
000101	1.628V	100101	1.116V
000110	1.612V	100110	1.100V
000111	1.596V	100111	1.084V
001000	1.580V	101000	1.068V
001001	1.564V	101001	1.052V
001010	1.548V	101010	1.036V
001011	1.532V	101011	1.020V
001100	1.516V	101100	1.004V
001101	1.500V	101101	0.988V
001110	1.484V	101110	0.972V
001111	1.468V	101111	0.956V
010000	1.452V	110000	0.940V
010001	1.436V	110001	0.924V
010010	1.420V	110010	0.908V
010011	1.404V	110011	0.892V
010100	1.388V	110100	0.876V
010101	1.372V	110101	0.860V
010110	1.356V	110110	0.844V
010111	1.340V	110111	0.828V
011000	1.324V	111000	0.812V
011001	1.308V	111001	0.796V
011010	1.292V	111010	0.780V
011011	1.276V	111011	0.764V
011100	1.260V	111100	0.748V
011101	1.244V	111101	0.732V
011110	1.228V	111110	0.716V
011111	1.212V	111111	0.700V

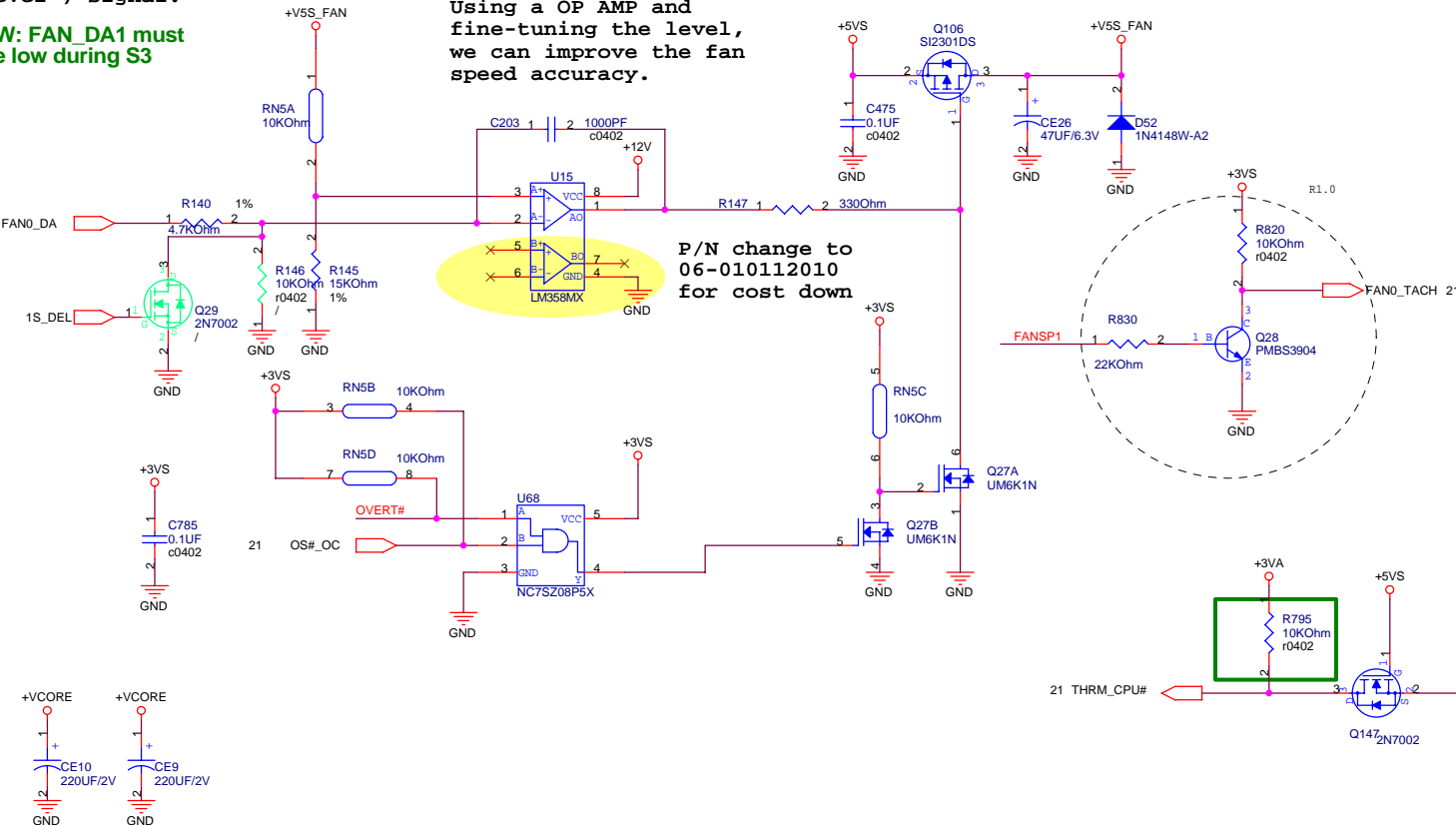
ASUS Title : **DOTHAN CPU (2)**
 ASUSTek COMPUTER INC Engineer: **Howard Tu**
 Size Project Name
 Custom **A3H** Rev 1.0
 Date: Thursday, June 30, 2005 Sheet 4 of 54

Fan Speed Control CPU FAN

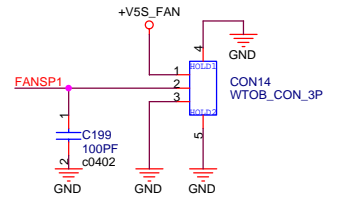
KBC will issue a analog (a voltage level) signal.

SW: FAN_DA1 must be low during S3

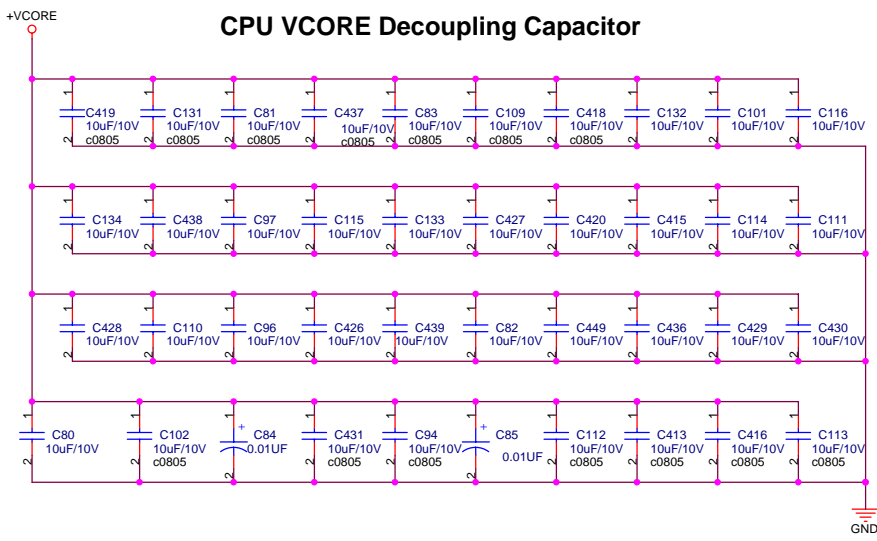
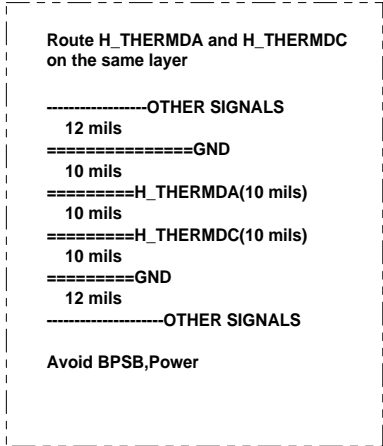
Using a OP AMP and fine-tuning the level, we can improve the fan speed accuracy.



P/N change to 06-010112010 for cost down



U6 output maximum will be 10.5V (VCC-1.5V) which will damage south bridge. Add a MOS to transfer it to +3V level.

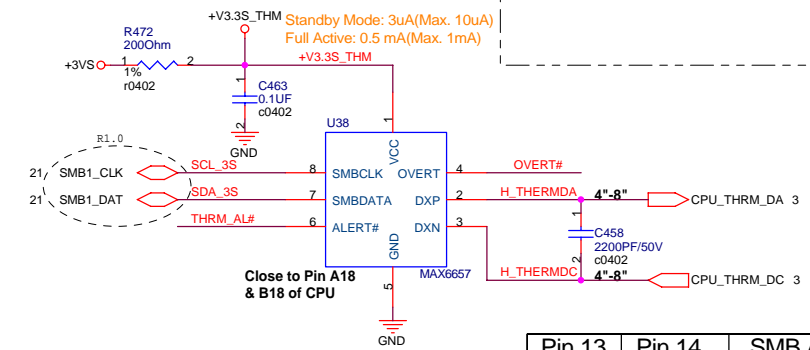


Mid Frequency Decoupling (Place around Processor)

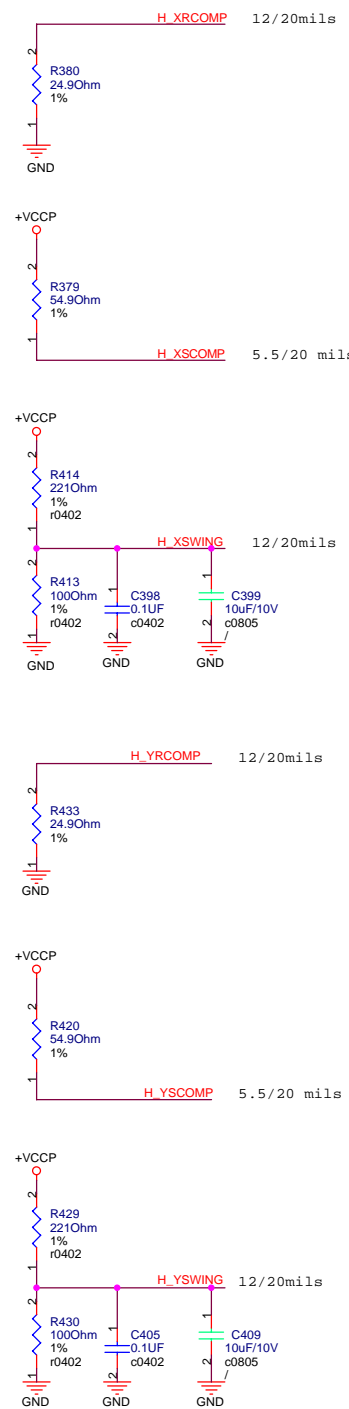
High Frequency Decoupling (Place underneath Processor) using 10uF/6.3V X5R

+VCORE Bulk Decoupling

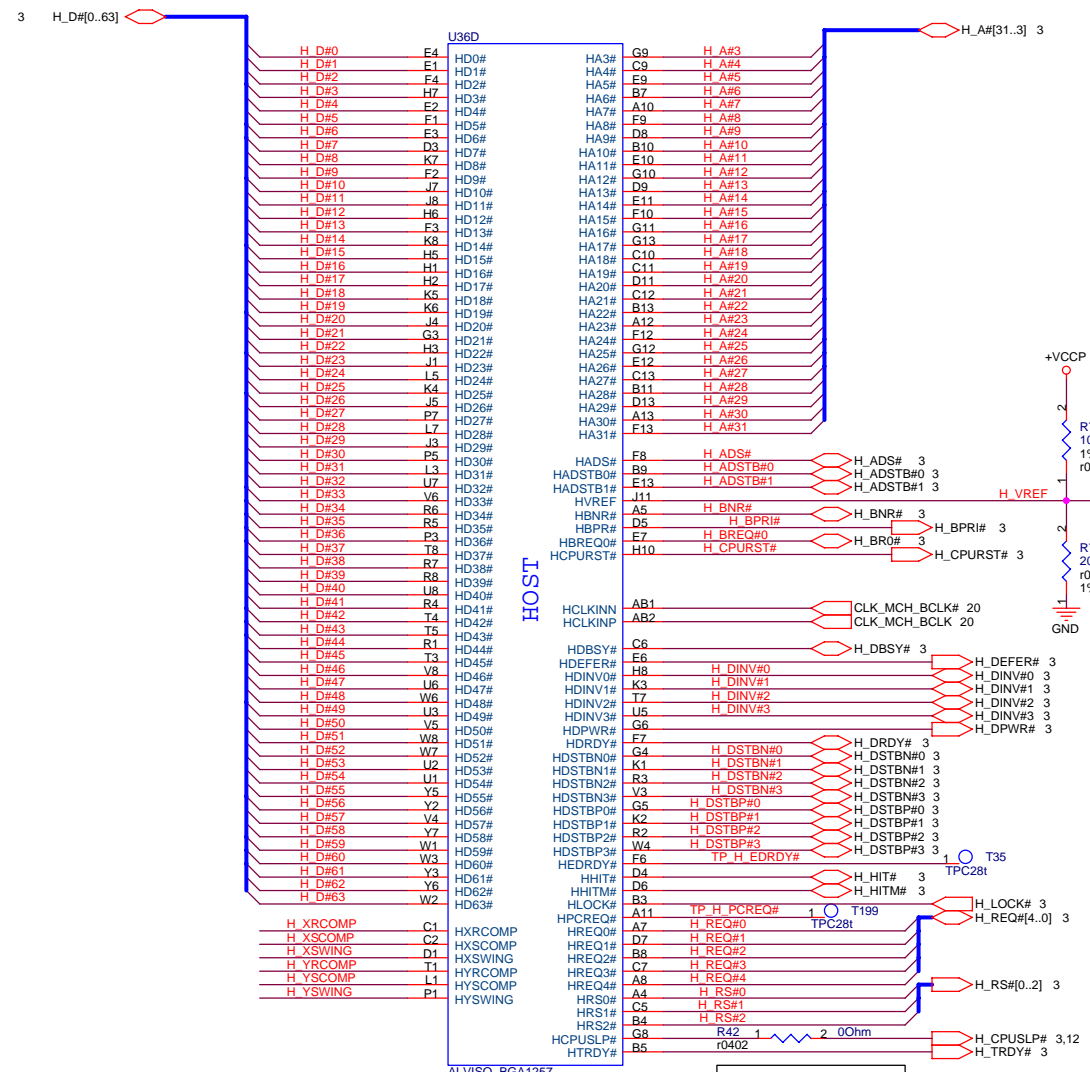
Four 200 uF are located in IMVP4



Pin 13	Pin 14	SMB Addr
1	X	5C **
0	1	5A
0	0	58

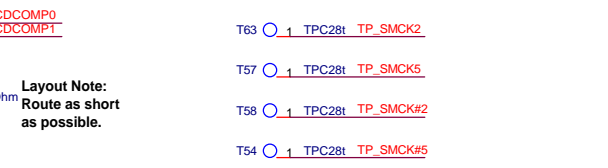
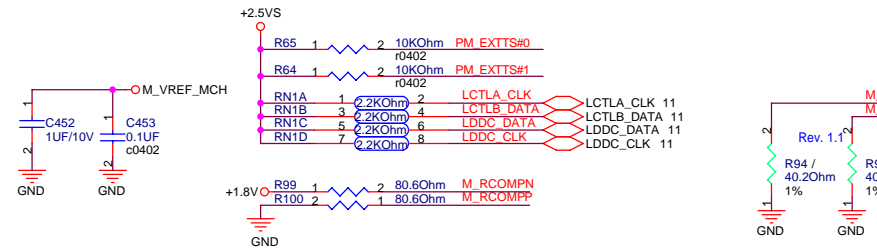
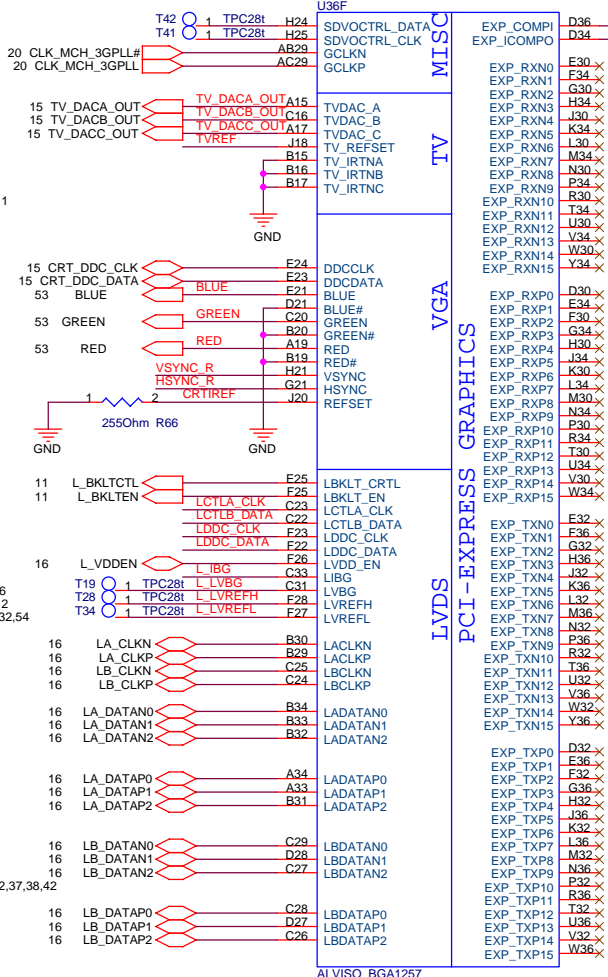
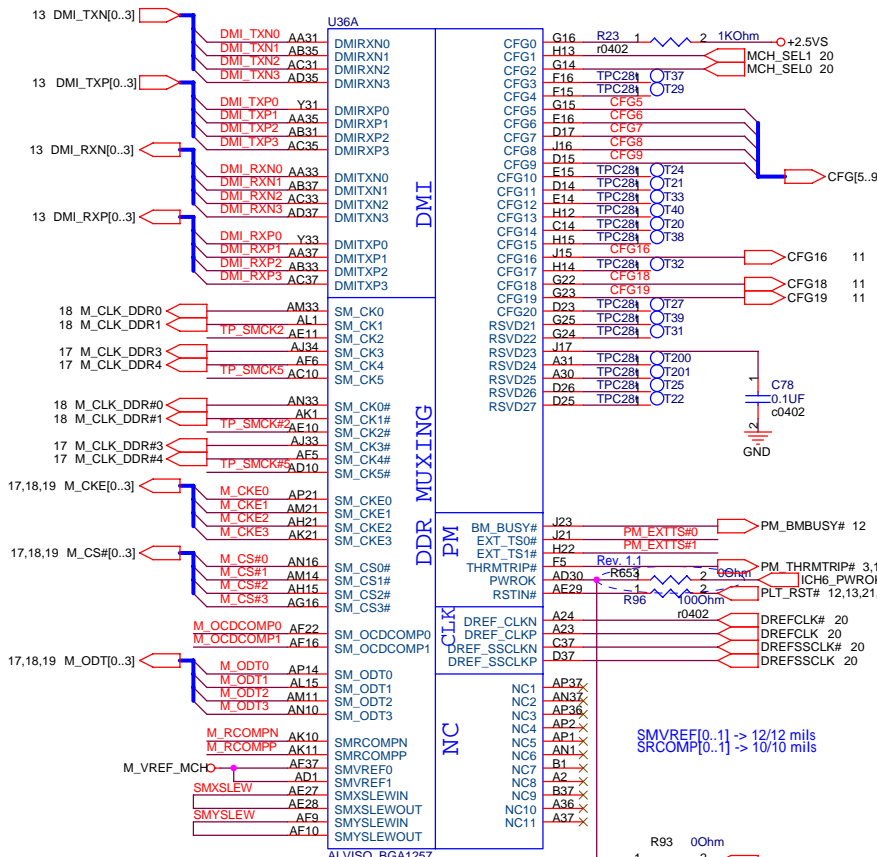
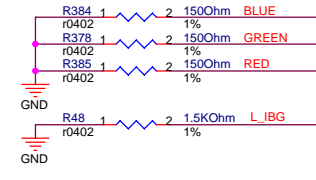
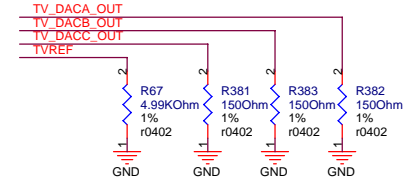
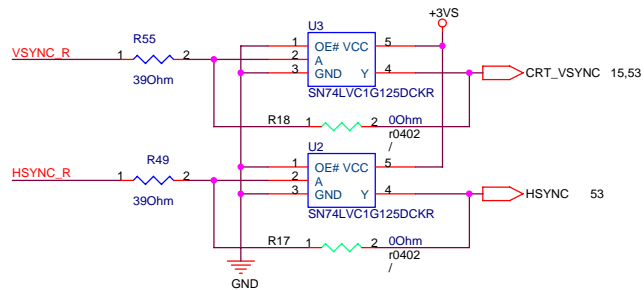


In OrCAD circuit,ALVISO PM P/N :02-010002600
 But we have to use ALVISO GM P/N : 02-010002610 in BOM list



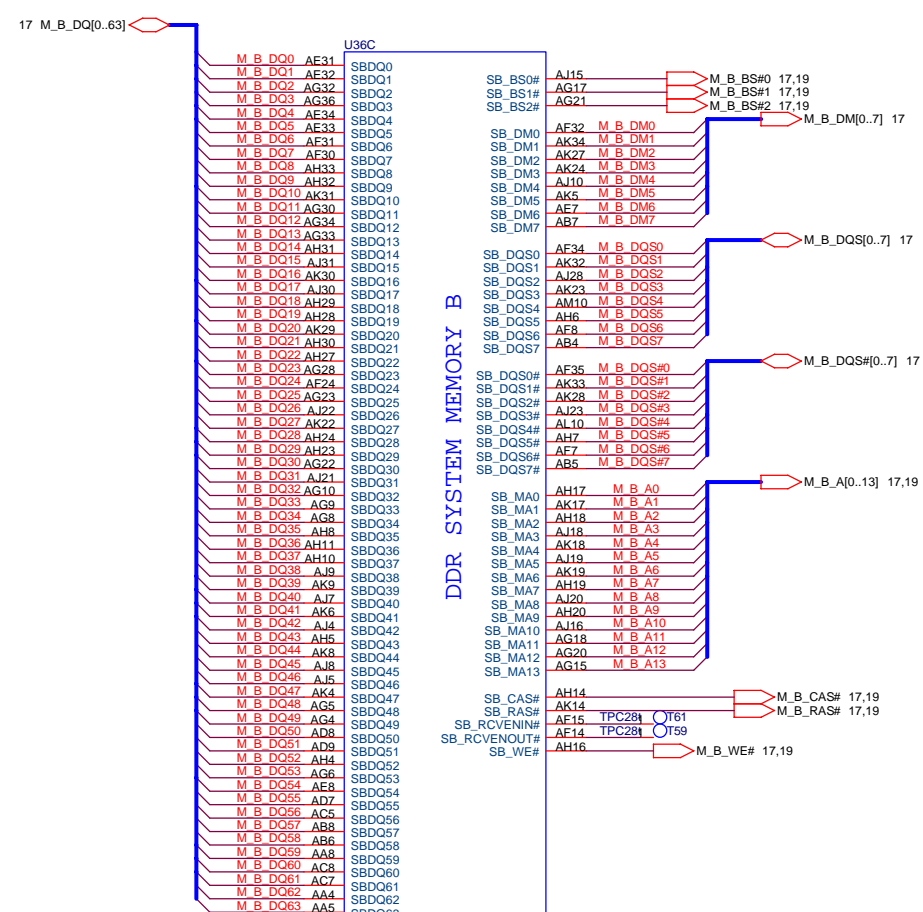
**Dothan A : R282
 NO STUFF**

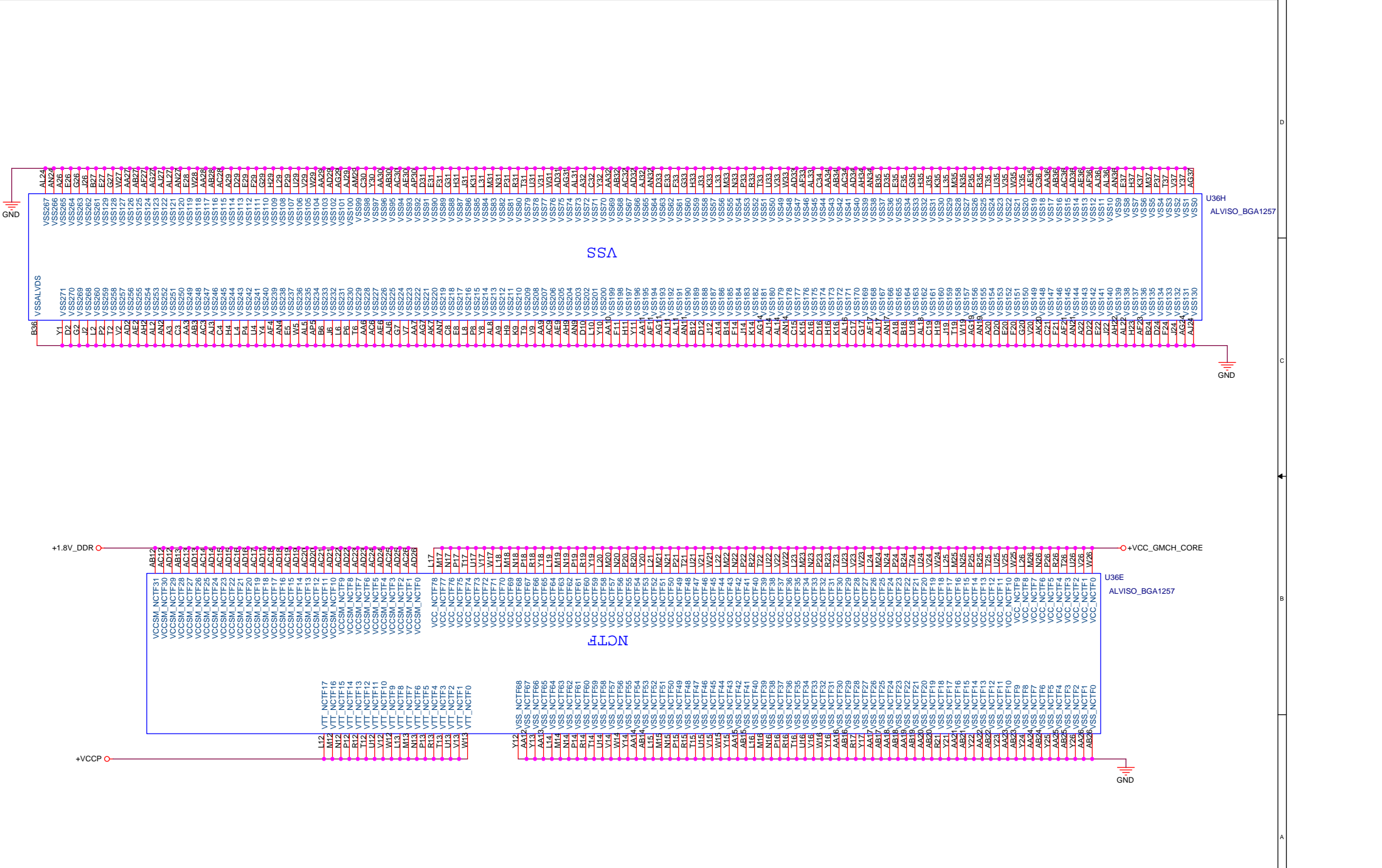
Near Alviso 0.5" ← → Near CRT Bead 0.5"



Layout Note: Route as short as possible.

ASUS Title : Alviso GMCH (2)
 ASUSTek COMPUTER INC Engineer: Howard Tu
 Size Project Name
 Custom A3H
 Date: Thursday, June 30, 2005 Sheet 7 of 54





VSSA

NCTF

U36H
ALVISO_BGA1257

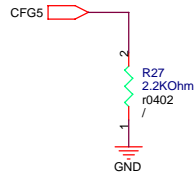
U36E
ALVISO_BGA1257

		Title : Alviso GMCH (5)	
ASUSTek COMPUTER INC		Engineer: Howard Tu	
Size Custom	Project Name A3H	Rev 1.0	
Date: Thursday, June 30, 2005		Sheet 10 of 54	

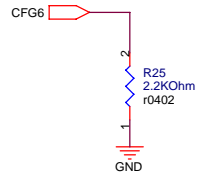
CFG[2:0] are HVMOS (+2.5VS)
 CFG[17..3] have internal pullup resistors. /AGTL+(VCCP)/
 CFG[19..18] have internal pulldown resistors. /HVMOS(+2.5VS)/
 SDVOCRTL_DATA has internal pulldown resistors.

SDVOCRTL_DATA :
 LOW = No SDVO device present (Default)

CFG5 : LOW = DMI X 2
 HIGH = DMI X 4 (Default)

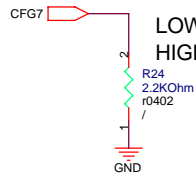


CFG6 : LOW = DDR2 SDRAM
 HIGH = DDR SDRAM (Default)



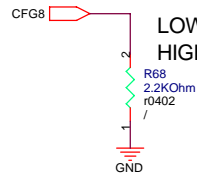
CFG7 : CPU STRAP

LOW = Mobile Prescott
 HIGH = Dothan CPU (Default)



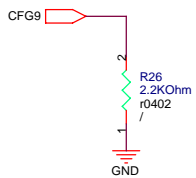
CFG8 : PCI-X POWER Saving

LOW = PCI-X POWER Saving
 HIGH (Default)



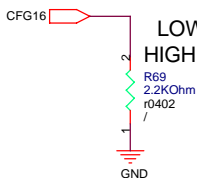
CFG9 : PCIE GRAPHIC LANE

LOW = REVERSE LANE
 HIGH = NORMAL OPERATION (Default)



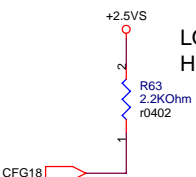
CFG16 : FSB DYNAMIC ODT

LOW = Dynamic ODT Disabled
 HIGH = Dynamic ODT Enabled (Default)



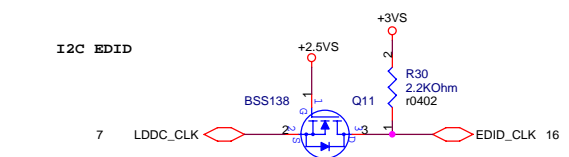
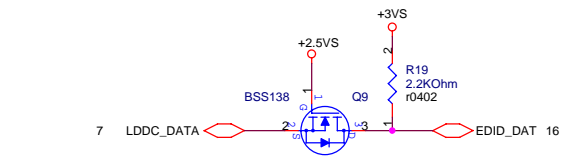
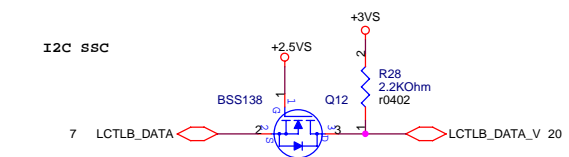
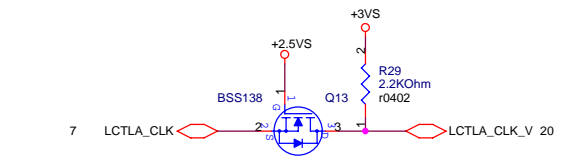
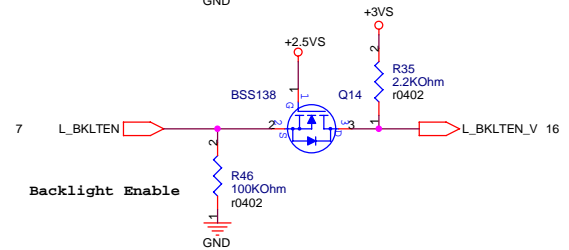
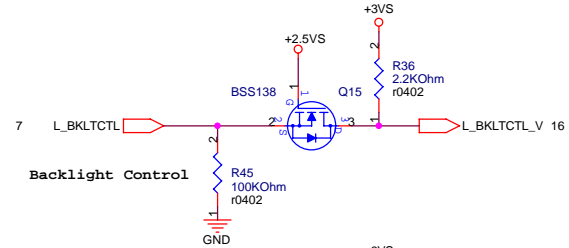
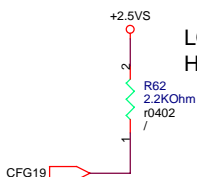
CFG18 : VCC SELECT

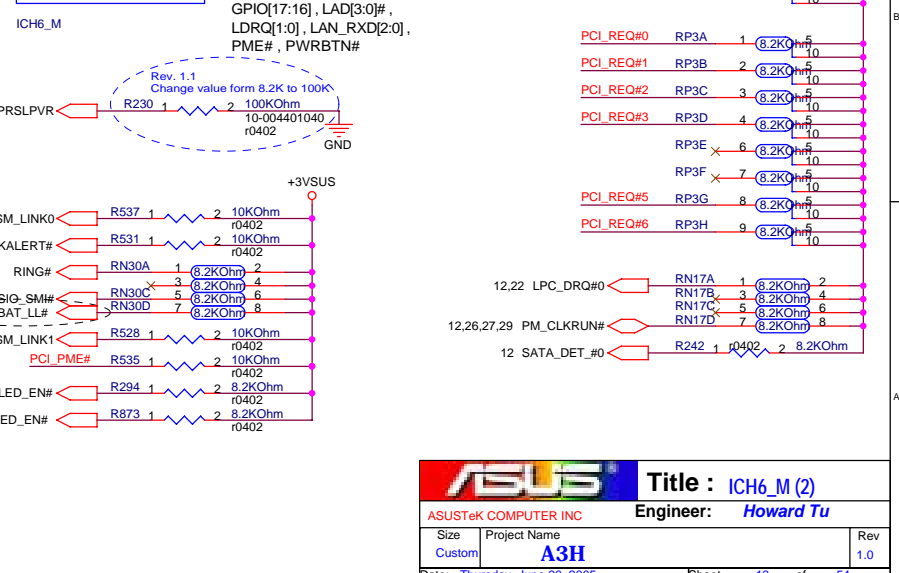
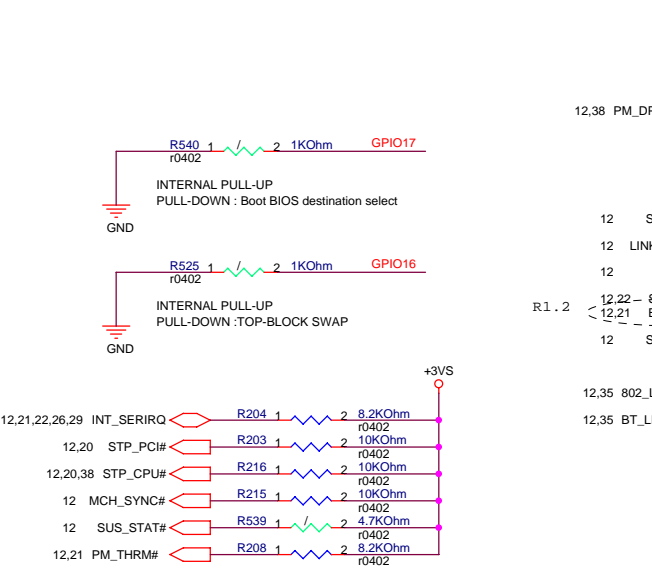
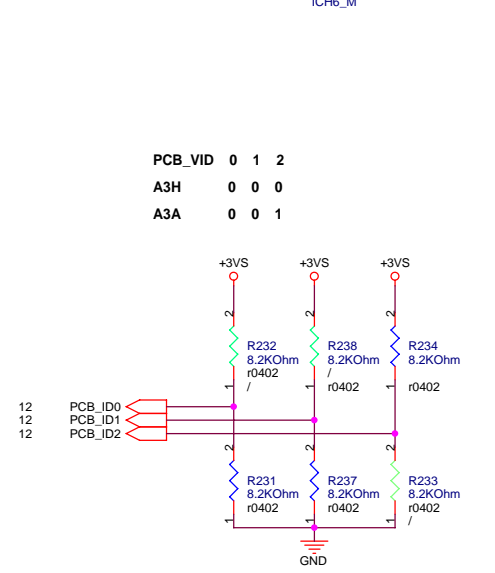
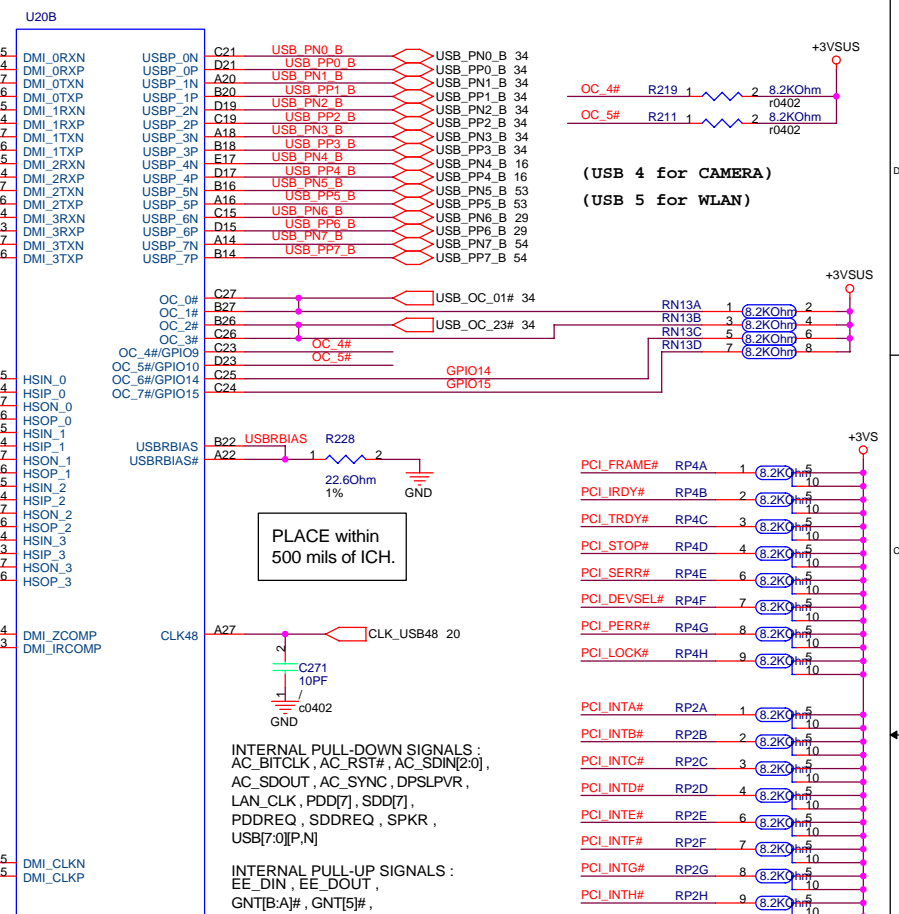
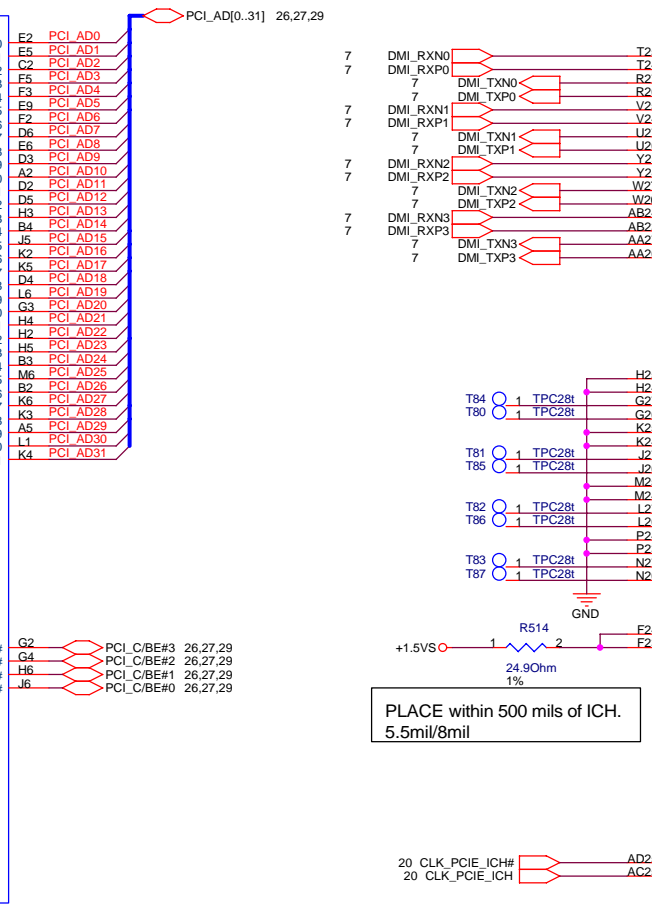
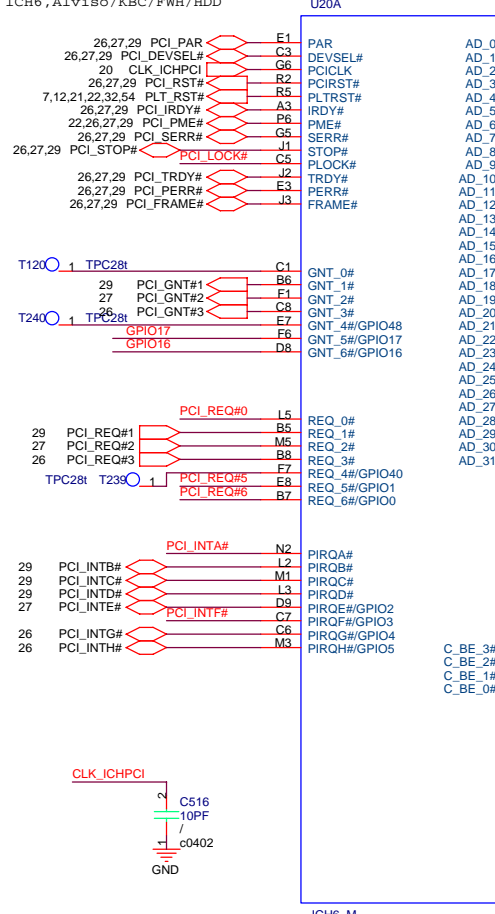
LOW = 1.05V (Default)
 HIGH = 1.5V



CFG19 : VTT SELECT

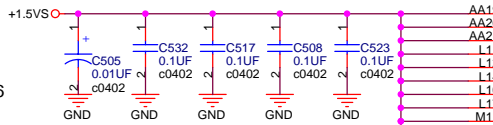
LOW = 1.05V (Default)
 HIGH = 1.2V



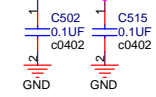


Place 0.01uF within 100mils of ICH near pin AA19

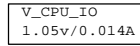
Place 4X0.1uF Distribute near pin ICH6 Package edge



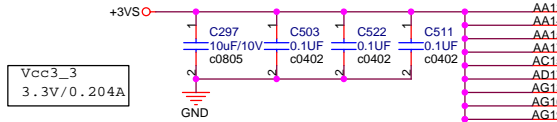
Place BOTH within 100mils of ICH near pin D27



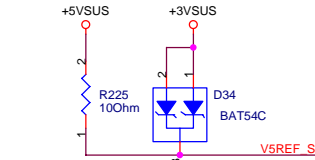
Place 0.1uF near AG10
Place 0.1uF near E26, E27
Place 0.1uF near AG13, AG16
Place 0.1uF near A2-A6, D1-H1



Place 0.1uF within 100mils of ICH near pin AG23



LAN3.3V/VCC3.3SUS



VCC3_3 3.3V/0.204A

Place 0.1uF near V7



Place BOTH within 100mils of ICH near pin A17



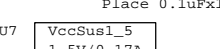
+VCC_RTC



+3.3VA_ICH



+1.5VA_USB



Place 0.1uF near G10



Place 0.1uF near U7

VCCSus1_5 1.5V/0.17A

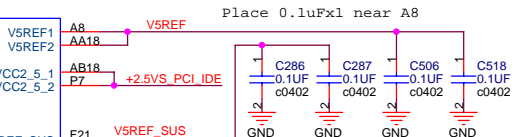
- AA19 VCC1_5_21
- AA20 VCC1_5_22
- AA21 VCC1_5_23
- L11 VCC1_5_24
- L12 VCC1_5_25
- L14 VCC1_5_26
- L16 VCC1_5_27
- M11 VCC1_5_28
- M17 VCC1_5_29
- P11 VCC1_5_30
- P11 VCC1_5_31
- P17 VCC1_5_32
- T11 VCC1_5_33
- T17 VCC1_5_34
- U12 VCC1_5_35
- U14 VCC1_5_36
- U16 VCC1_5_37
- U17 VCC1_5_38
- G8 VCC1_5_39
- D24 VCC1_5_40
- D25 VCC1_5_41
- D26 VCC1_5_42
- D27 VCC1_5_43
- E20 VCC1_5_44
- E21 VCC1_5_45
- E22 VCC1_5_46
- E23 VCC1_5_47
- E24 VCC1_5_48
- F20 VCC1_5_49
- G20 VCC1_5_50
- F9 VCC1_5_51
- F9 VCC1_5_52

- V_CPU_IO_1 VCCDMIPL
- V_CPU_IO_2 VCCSAPAPLL
- V_CPU_IO_3 VCCSUBPLL
- AA22 VCC3_3_1
- AA23 VCC3_3_2
- AA24 VCC3_3_3
- AA25 VCC3_3_4
- AA26 VCC3_3_5
- AA27 VCC3_3_6
- E25 VCC3_3_7
- E26 VCC3_3_8
- E27 VCC3_3_9
- G22 VCC3_3_10
- G23 VCC3_3_11
- G24 VCC3_3_12
- G25 VCC3_3_13
- H21 VCC3_3_14
- H22 VCC3_3_15
- J21 VCC3_3_16
- J22 VCC3_3_17
- K21 VCC3_3_18
- K22 VCC3_3_19
- L21 VCC3_3_20
- L22 VCC3_3_21
- M21 VCC3_3_22
- M22 VCC3_3_23
- N21 VCC3_3_24
- N22 VCC3_3_25
- N23 VCC3_3_26
- N24 VCC3_3_27
- N25 VCC3_3_28
- P21 VCC3_3_29
- P25 VCC3_3_30
- P26 VCC3_3_31
- P27 VCC3_3_32
- R21 VCC3_3_33
- R22 VCC3_3_34
- T21 VCC3_3_35
- T22 VCC3_3_36
- U21 VCC3_3_37
- U22 VCC3_3_38
- V21 VCC3_3_39
- V22 VCC3_3_40
- W21 VCC3_3_41
- W22 VCC3_3_42
- Y21 VCC3_3_43
- Y22 VCC3_3_44

- VCCSUS3_3_1 VCCSUS3_3_1
- VCCSUS3_3_2 VCCSUS3_3_2
- VCCSUS3_3_3 VCCSUS3_3_3
- VCCSUS3_3_4 VCCSUS3_3_4
- VCCSUS3_3_5 VCCSUS3_3_5
- VCCSUS3_3_6 VCCSUS3_3_6
- VCCSUS3_3_7 VCCSUS3_3_7
- VCCSUS3_3_8 VCCSUS3_3_8
- VCCSUS3_3_9 VCCSUS3_3_9
- VCCSUS3_3_10 VCCSUS3_3_10
- VCCSUS3_3_11 VCCSUS3_3_11
- VCCSUS3_3_12 VCCSUS3_3_12
- VCCSUS3_3_13 VCCSUS3_3_13
- VCCSUS3_3_14 VCCSUS3_3_14
- VCCSUS3_3_15 VCCSUS3_3_15
- VCCSUS3_3_16 VCCSUS3_3_16
- VCCSUS3_3_17 VCCSUS3_3_17
- VCCSUS3_3_18 VCCSUS3_3_18
- VCCSUS3_3_19 VCCSUS3_3_19
- VCCSUS3_3_20 VCCSUS3_3_20
- VCCSUS3_3_21 VCCSUS3_3_21
- VCCSUS3_3_22 VCCSUS3_3_22
- VCCSUS3_3_23 VCCSUS3_3_23
- VCCSUS3_3_24 VCCSUS3_3_24

- VCCRTC VCCSUS1_5_A
- U7 VCCSUS1_5_B
- G9 VCCSUS1_5_C
- G10 VCCSUS1_5_D
- G11 VCCSUS1_5_E
- AA6 VCC1_5_1
- AA4 VCC1_5_2
- AA5 VCC1_5_3
- AA6 VCC1_5_4
- AA4 VCC1_5_5
- AA7 VCC1_5_6
- AA8 VCC1_5_7
- AA9 VCC1_5_8
- AA7 VCC1_5_9
- AA8 VCC1_5_10
- AA9 VCC1_5_11
- AA7 VCC1_5_12
- AA8 VCC1_5_13
- AA9 VCC1_5_14
- AA7 VCC1_5_15
- AA8 VCC1_5_16
- AA9 VCC1_5_17
- AA7 VCC1_5_18
- AA8 VCC1_5_19
- AA9 VCC1_5_20

ICH6_M

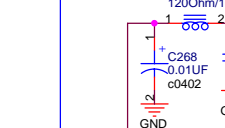


Place 0.1uF near AB18



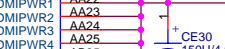
Vcc2_5 2.5V/0.015A

Place 150uF, 3 X 0.1uF within 100mils of ICH near pin F27, P27, AB27

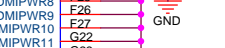


VCC1_5_B 1.425V/1.5V/1.575V / / 578mA

Place within 100mils of ICH near pin AG5

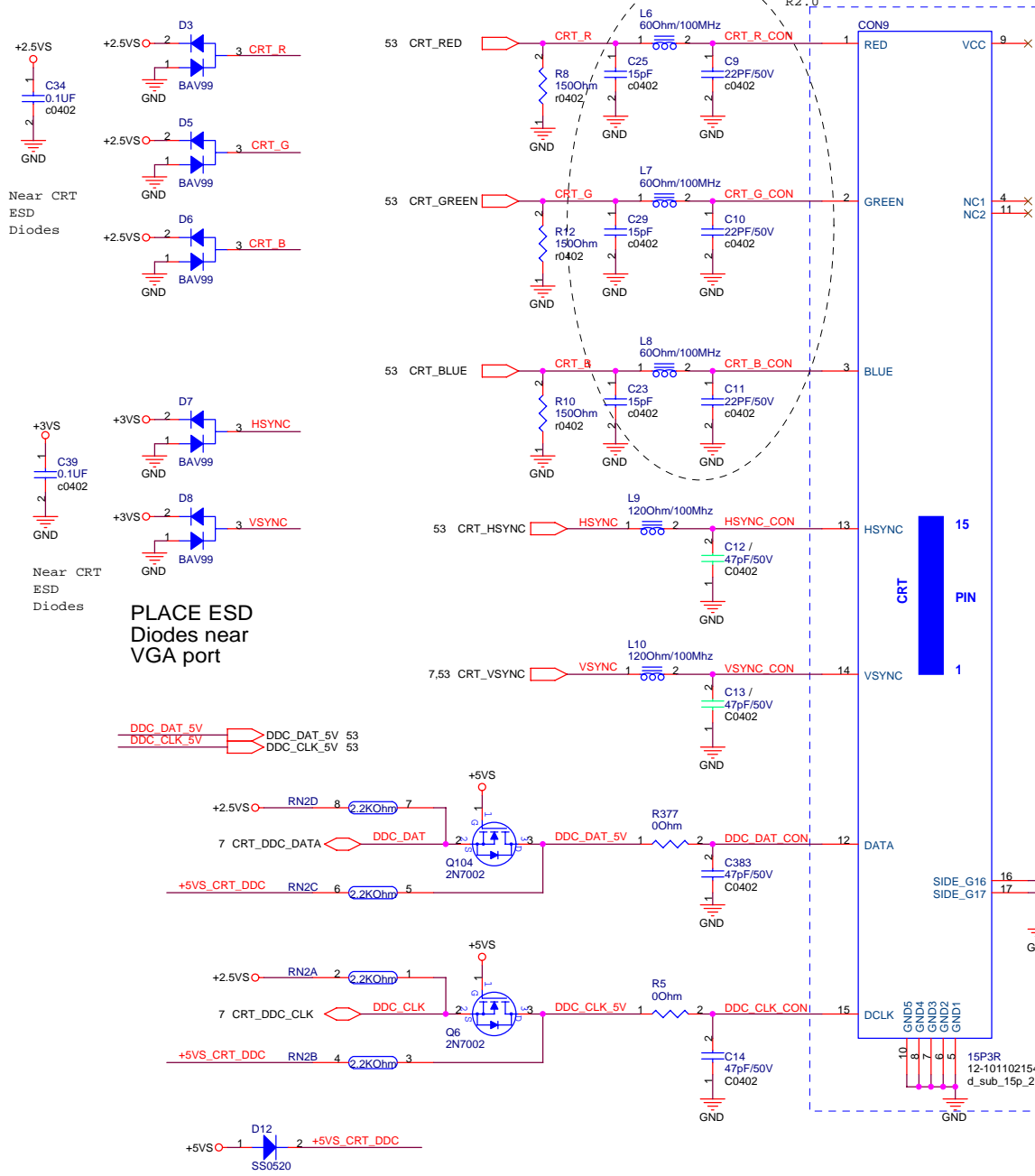


Place within 100mils of ICH near pin AG9

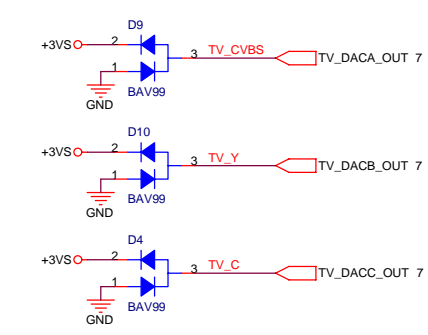
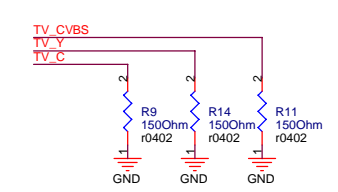
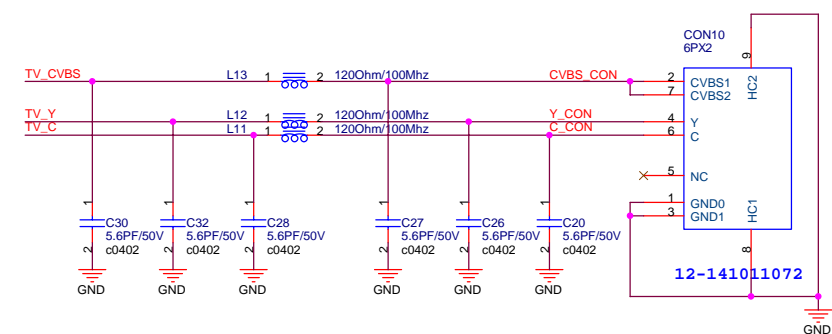


- A1 VSS1
- A12 VSS2
- A15 VSS3
- A19 VSS4
- A21 VSS5
- A23 VSS6
- A26 VSS7
- A4 VSS8
- A7 VSS9
- A9 VSS10
- AA11 VSS11
- AA13 VSS12
- AA16 VSS13
- AA4 VSS14
- AB1 VSS15
- AB10 VSS16
- AB2 VSS17
- AB7 VSS18
- AB9 VSS19
- AC10 VSS20
- AC12 VSS21
- AC22 VSS22
- AC23 VSS23
- AC24 VSS24
- AC26 VSS25
- AC3 VSS26
- AC6 VSS27
- AD1 VSS28
- AD10 VSS29
- AD15 VSS30
- AD18 VSS31
- AD2 VSS32
- AD2 VSS33
- AD24 VSS34
- AD6 VSS35
- AE10 VSS36
- AE11 VSS37
- AE12 VSS38
- AE2 VSS39
- AE25 VSS40
- AE6 VSS41
- AE7 VSS42
- AF1 VSS43
- AF12 VSS44
- AF26 VSS45
- AF3 VSS46
- AF7 VSS47
- AG1 VSS48
- AG12 VSS49
- AG14 VSS50
- AG17 VSS51
- AG20 VSS52
- AG22 VSS53
- AG3 VSS54
- AG7 VSS55
- B13 VSS56
- B15 VSS57
- B19 VSS58
- B21 VSS59
- B23 VSS60
- B25 VSS61
- B25 VSS62
- C18 VSS63
- C20 VSS64
- C22 VSS65
- C4 VSS66
- D1 VSS67
- D10 VSS68
- D13 VSS69
- D14 VSS70
- D18 VSS71
- D18 VSS72
- D20 VSS73
- D22 VSS74
- D7 VSS75
- E14 VSS76
- E15 VSS77
- E18 VSS78
- E19 VSS79
- E25 VSS80
- F17 VSS81
- F19 VSS82
- F22 VSS83
- F4 VSS84
- G1 VSS85
- G12 VSS86
- VSS87 G7
- VSS88 G9
- VSS89 H23
- VSS90 H26
- VSS91 H27
- VSS92 H22
- VSS93 J23
- VSS94 J25
- VSS95 J4
- VSS96 K1
- VSS97 K23
- VSS98 K26
- VSS99 K27
- VSS100 K7
- VSS101 L13
- VSS102 L5
- VSS103 L23
- VSS104 L24
- VSS105 L25
- VSS106 M12
- VSS107 M13
- VSS108 M14
- VSS109 M15
- VSS110 M16
- VSS111 M23
- VSS112 M26
- VSS113 M27
- VSS114 M4
- VSS115 N1
- VSS116 N11
- VSS117 N12
- VSS118 N13
- VSS119 N14
- VSS120 N15
- VSS121 N16
- VSS122 N17
- VSS123 N7
- VSS124 P12
- VSS125 P13
- VSS126 P14
- VSS127 P15
- VSS128 P16
- VSS129 P22
- VSS130 R11
- VSS131 R12
- VSS132 R13
- VSS133 R14
- VSS134 R15
- VSS135 R16
- VSS136 R17
- VSS137 R23
- VSS138 R24
- VSS139 R25
- VSS140 R4
- VSS141 T1
- VSS142 T12
- VSS143 T13
- VSS144 T14
- VSS145 T15
- VSS146 T16
- VSS147 T26
- VSS148 T27
- VSS149 T28
- VSS150 T7
- VSS151 T7
- VSS152 U13
- VSS153 U15
- VSS154 U23
- VSS155 U24
- VSS156 U25
- VSS157 U23
- VSS158 V26
- VSS159 V27
- VSS160 V4
- VSS161 W1
- VSS162 W23
- VSS163 W25
- VSS164 W7
- VSS165 Y23
- VSS166 Y26
- VSS167 Y27
- VSS168 Y6
- VSS169 W24
- VSS170 E27
- VSS171 B24
- VSS172 AF10

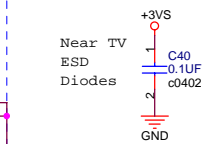
ASUS Title : ICH6_M (3)
 ASUSTek COMPUTER INC Engineer: Howard Tu
 Size Project Name
 Custom A3H
 Date: Thursday, June 30, 2005 Sheet 14 of 54



Note: CRT_Red, CRT Green, CRT Blue are ground reference.



PLACE ESD Diodes near TV port



Rev. 1.1
SMT Issue
Change type from P/N 12-10110015L to P/N 12-101102154

PLACE ESD Diodes near VGA port

Near CRT ESD Diodes

Near CRT ESD Diodes

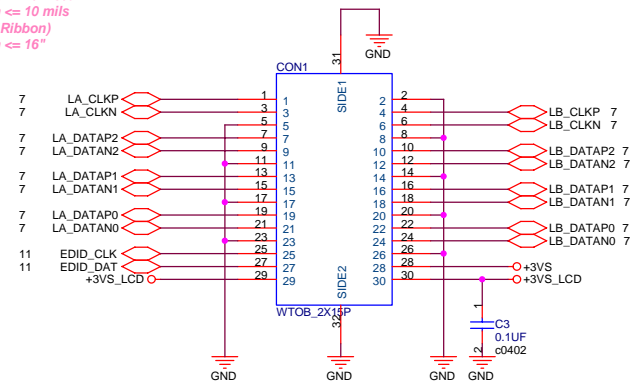
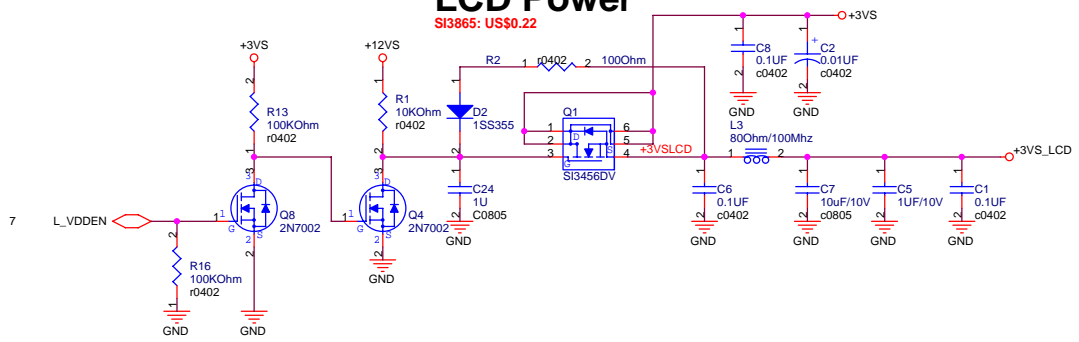
LCD Backlight Control

LCD LVDS Interface

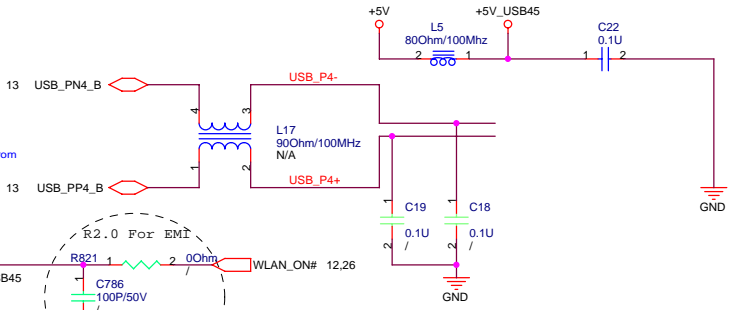
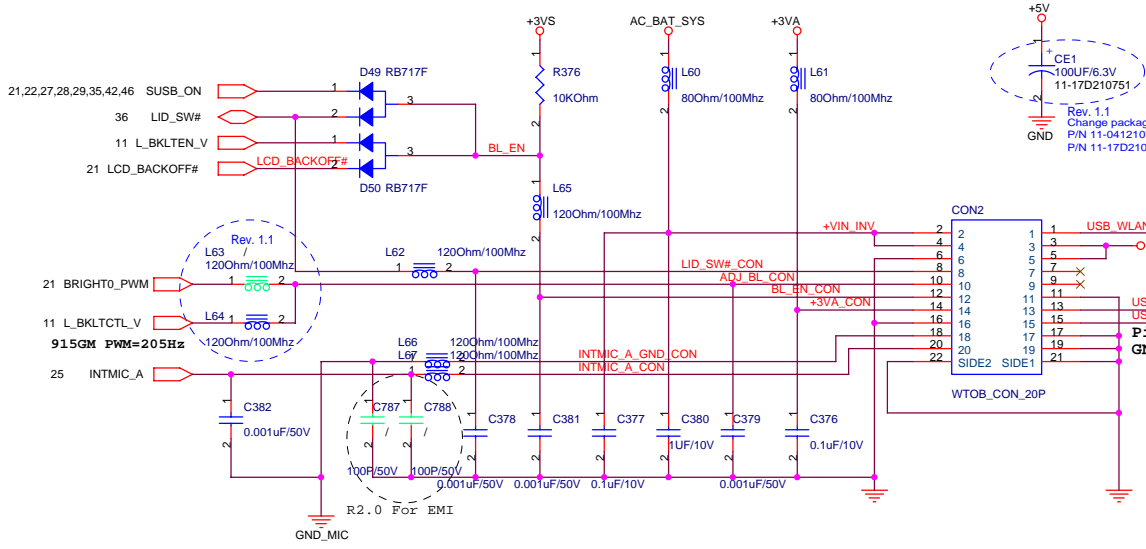
LCD Power

3V-3.6V
Full Active: 410 mA(Max. 500 mA)
3-3.6V
S0-S1M:410 mA(500 mA Max.)

Cable Requirement:
Impedence: 100 ohm +/- 10%
Length Mismatch <= 10 mils
Twisted Pair(Not Ribbon)
Maximum Length <= 16"



INVERTER Interface



USB PORT 4 for CAMERA

Pin 19 : Add a USB 2.0 Shielding GND cable to USB module.

BIOS
ADJ_BL: KBC
output D/A
signal (adjust
voltage level)
to adjust Back
light.

BIOS
BACK_OFF#:When user push "Fn+F7"
button, BIOS active this pin to
turn off back light.

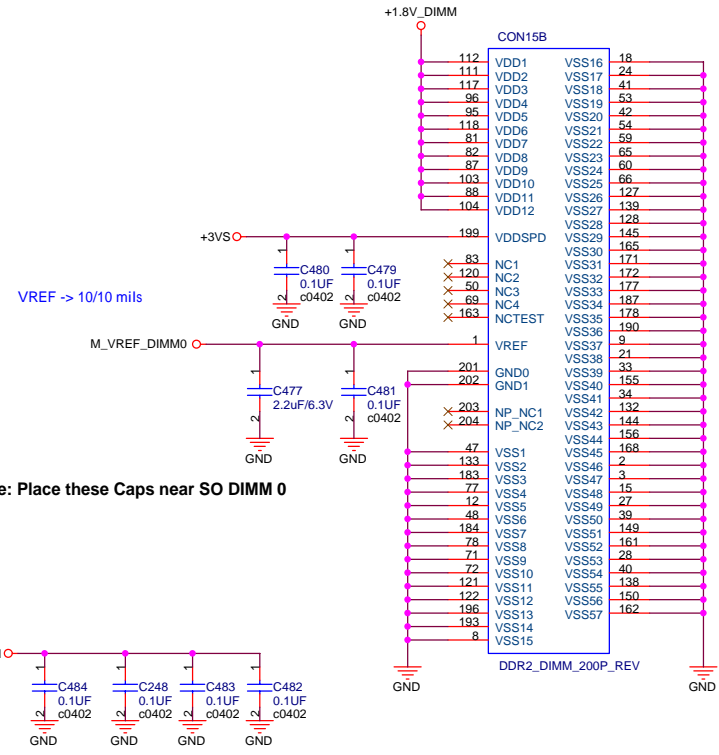
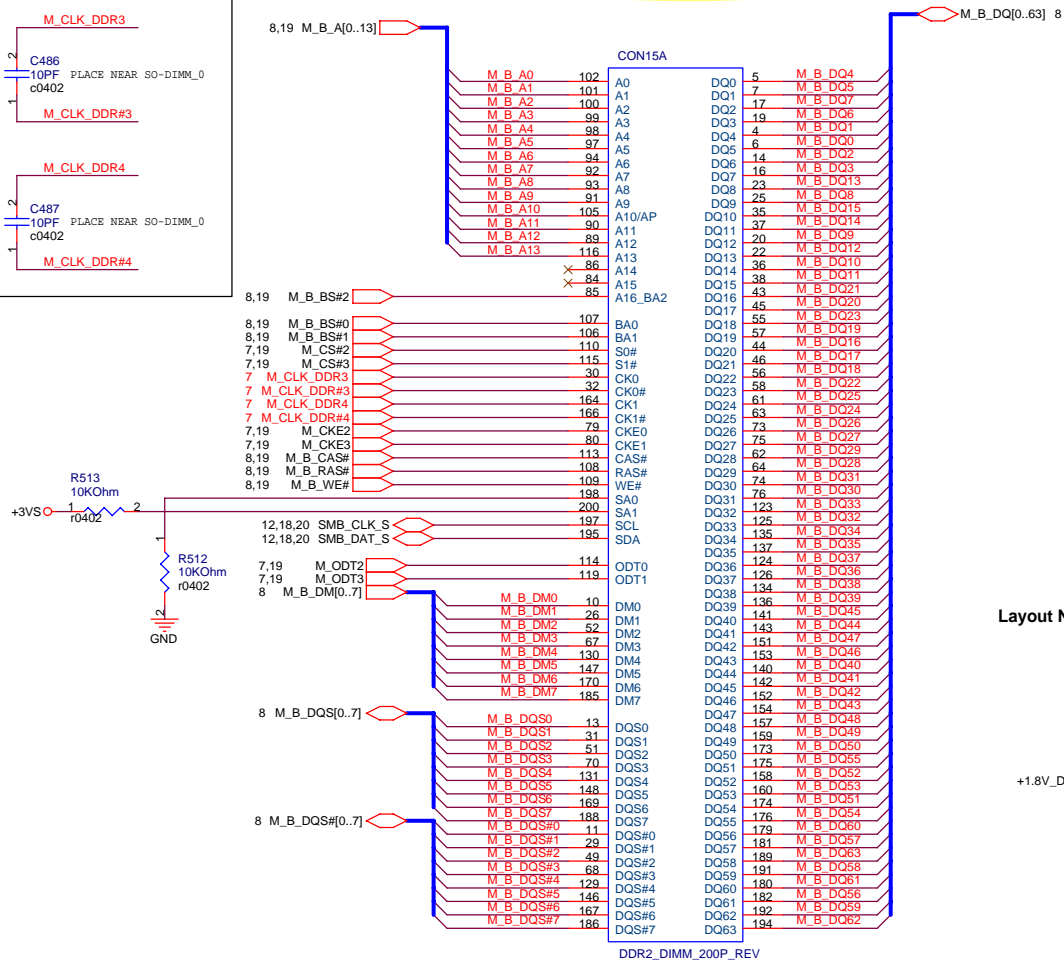
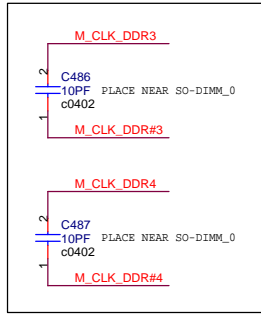
700Vrms@5 mArms
(Min. 3 mArms)6 mArms(Max. 6.5 mArms)

A3H/A3A don't use
USB PORT 5 for WLAN

ASUS		Title : LVDS & INVERTER	
ASUSTeK COMPUTER INC		Engineer: Howard Tu	
Size	Project Name	Rev	
Custom	A3H	1.0	
Date: Thursday, June 30, 2005	Sheet	16	of 54

For crosstalk

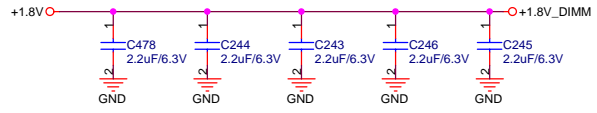
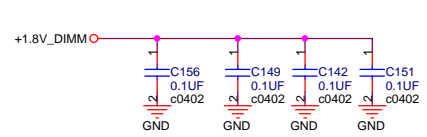
Change to PN: 12-02512200B



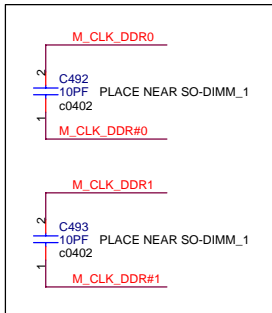
Layout Note: Place these Caps near SO DIMM 0

Layout Note: Place these Caps near SO DIMM 0

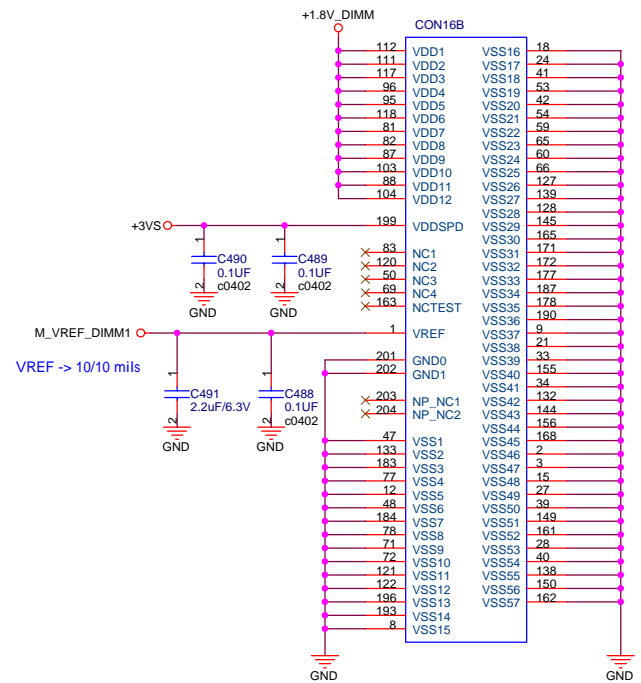
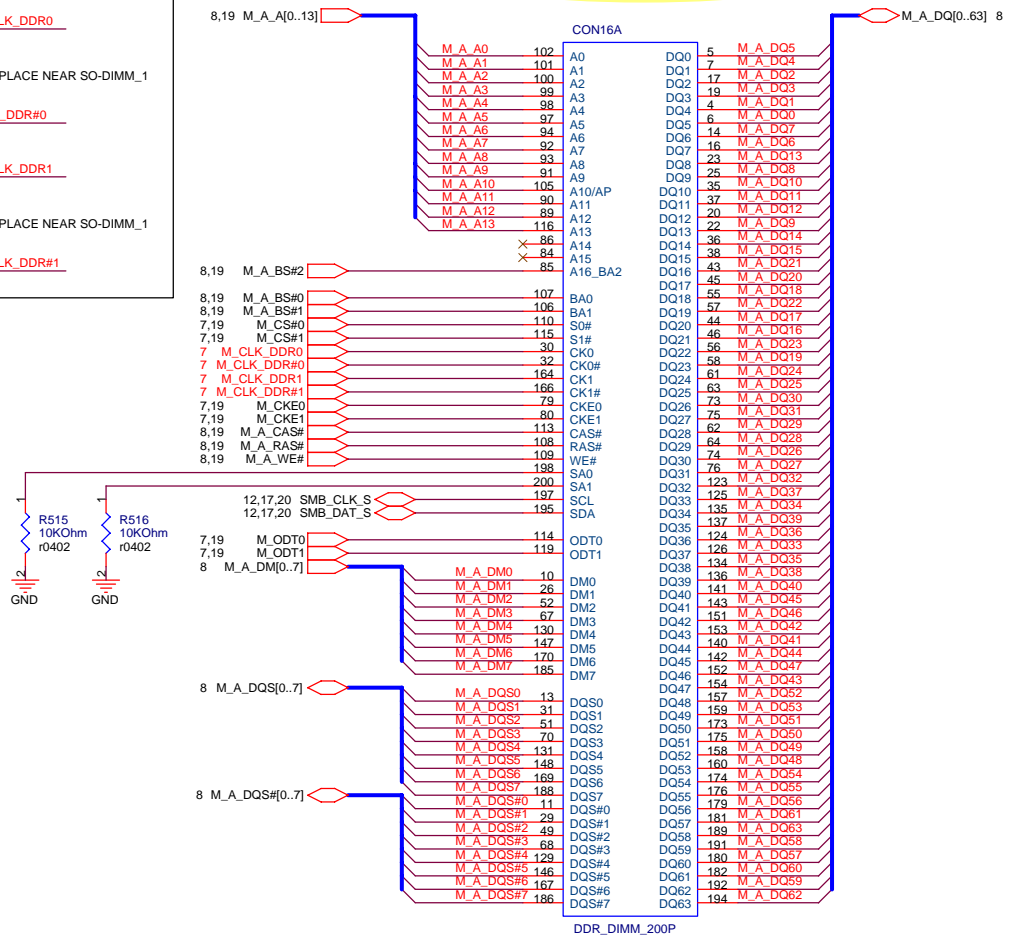
Layout Note: Place these High-Freq decoupling Caps near the GMCH



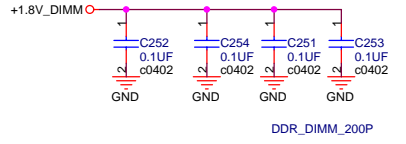
For crosstalk



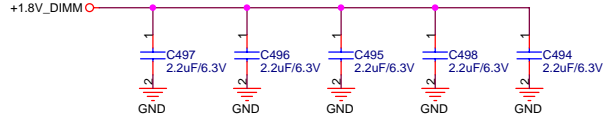
Change to PN:12-02512200A



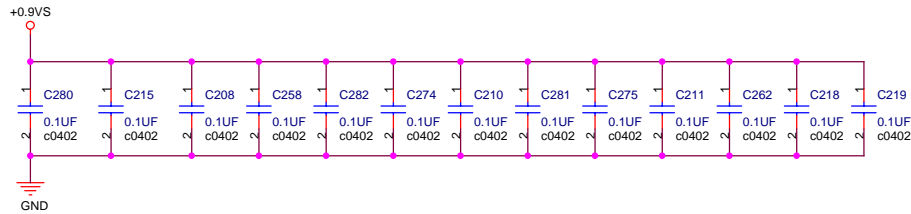
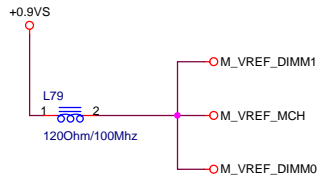
Layout Note: Place these Caps near SO DIMM 1



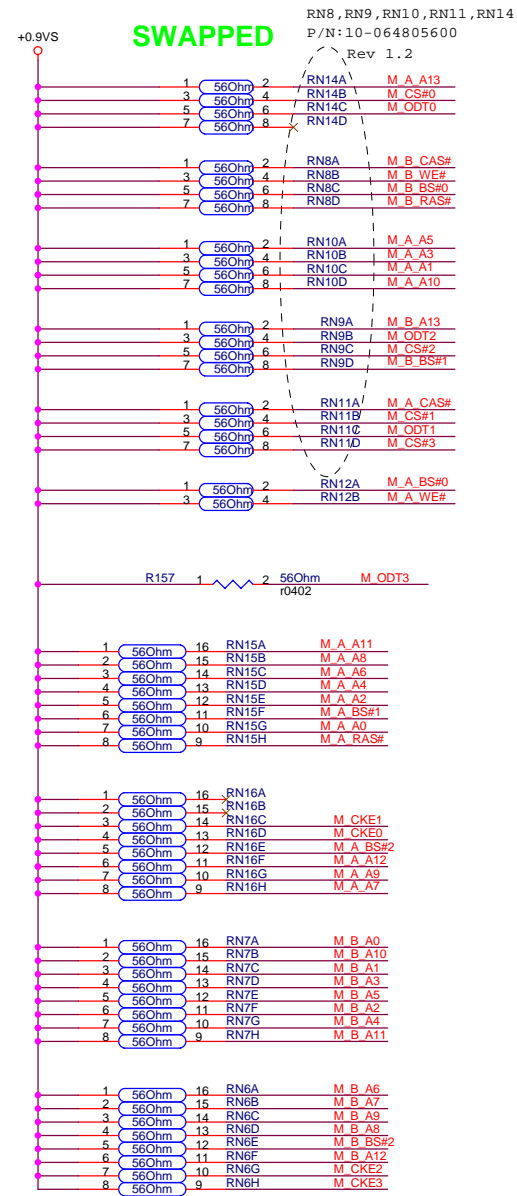
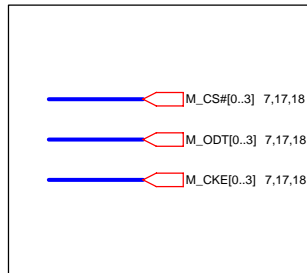
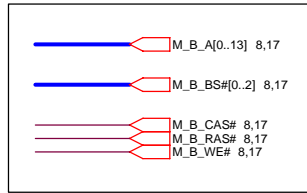
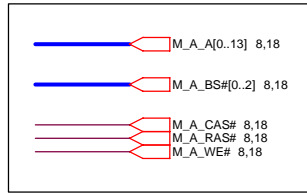
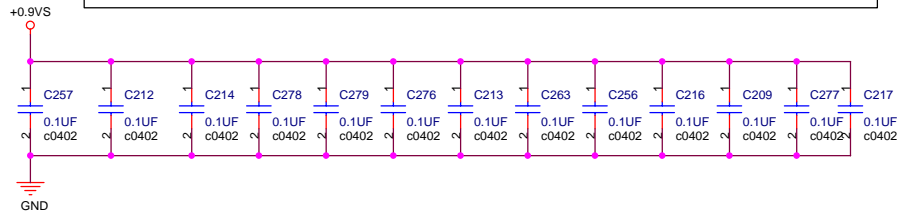
Layout Note: Place these Caps near SO DIMM 1



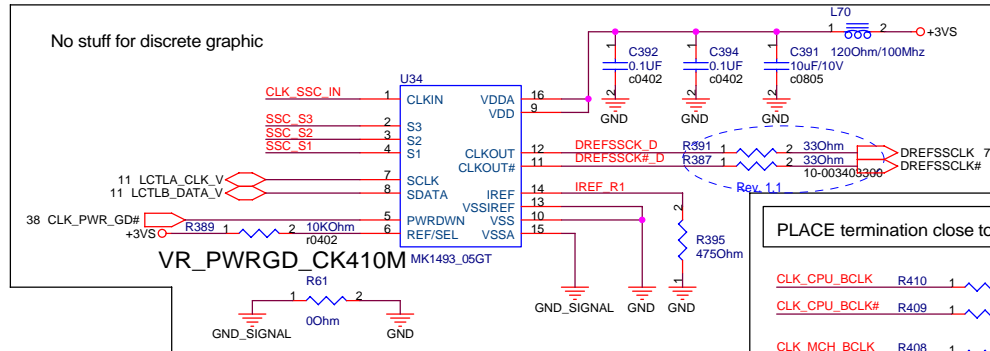
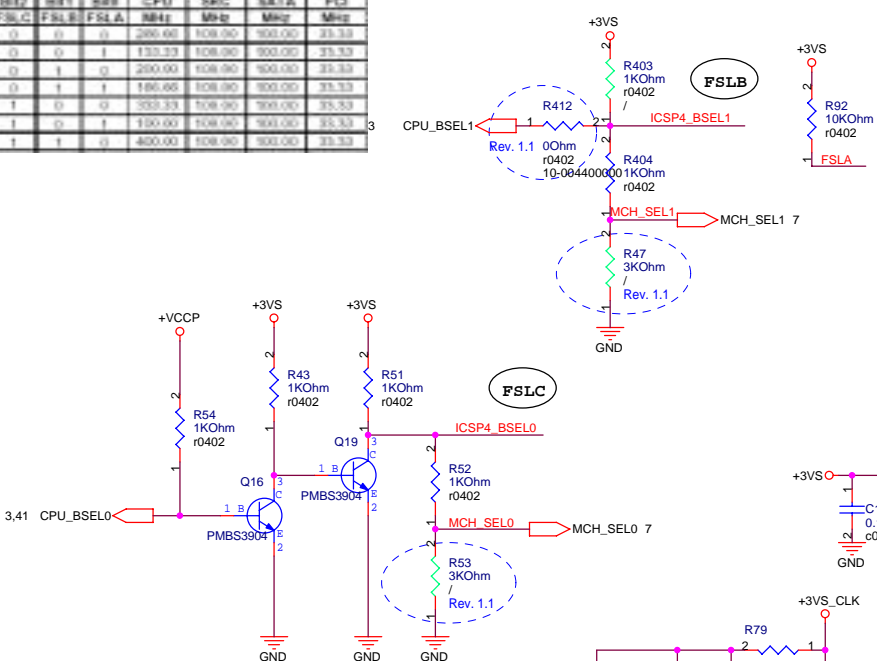
SO-DIMM 1 is placed father from the GMCH than SO-DIMM 0



Layout note: Place one cap close to every 2 pullup resistors terminated to +0.9VS

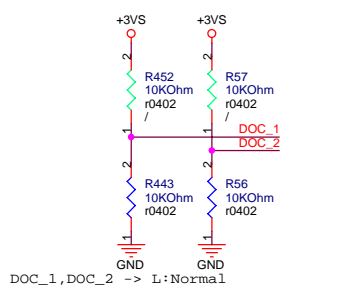
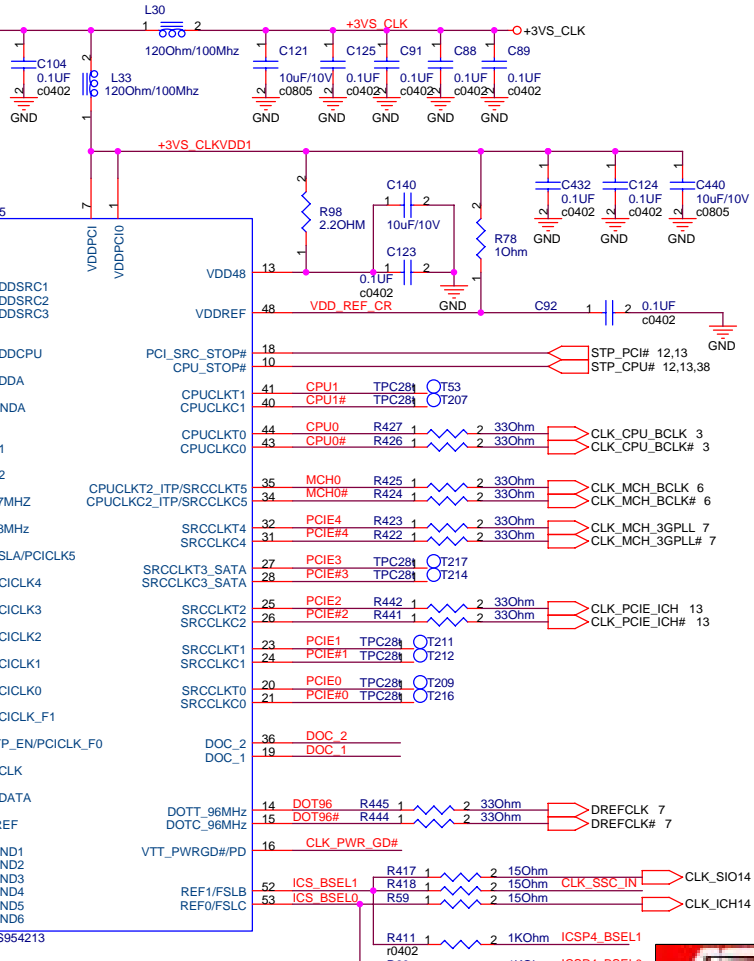
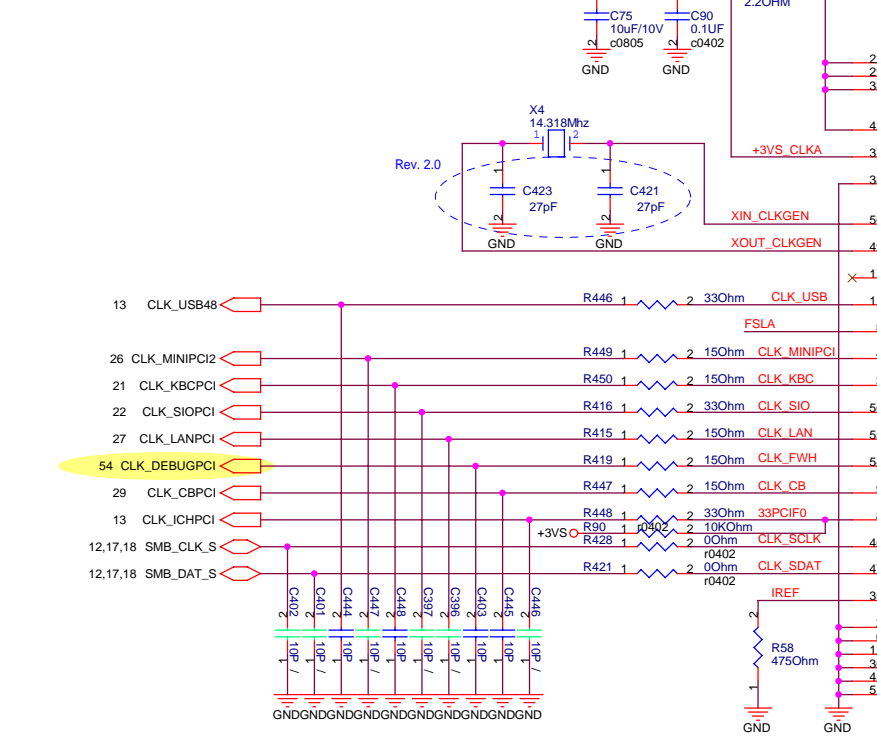


Bus	Rev	Rev	CPU	SRC	SATA	PCI
FSLC	FSLB	FSLA	MHz	MHz	MHz	MHz
0	0	0	200.00	100.00	100.00	33.33
0	1	0	133.33	100.00	100.00	33.33
0	1	0	200.00	100.00	100.00	33.33
1	0	0	133.33	100.00	100.00	33.33
1	0	0	200.00	100.00	100.00	33.33
1	1	0	400.00	100.00	100.00	33.33



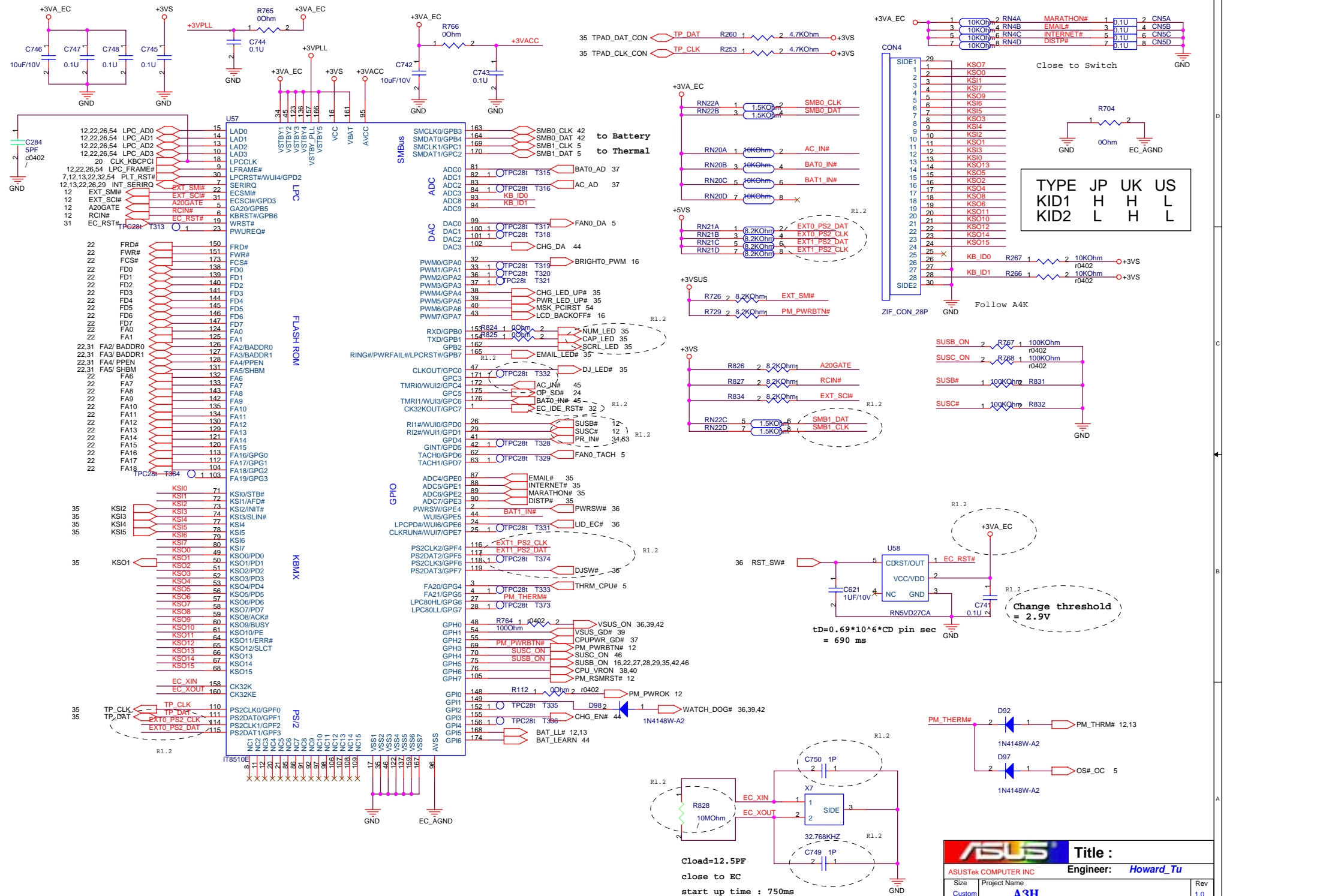
PLACE termination close to source IC

- CLK_CPU_BCLK R410 1 2 49.90hm r0402
- CLK_CPU_BCLK# R409 1 2 49.90hm r0402
- CLK_MCH_BCLK R408 1 2 49.90hm r0402
- CLK_MCH_BCLK# R407 1 2 49.90hm r0402
- DREFCLK R454 1 2 49.90hm r0402
- DREFCLK# R453 1 2 49.90hm r0402
- CLK_PCIE_ICH R455 1 2 49.90hm r0402
- CLK_PCIE_ICH# R456 1 2 49.90hm r0402
- CLK_MCH_3GPLL R406 1 2 49.90hm r0402
- CLK_MCH_3GPLL# R405 1 2 49.90hm r0402
- DREFSSCLK R396 1 2 49.90hm r0402
- DREFSSCLK# R388 1 2 49.90hm r0402



R441 10K pull up to +3VS for CPUCLK2_ITP
R442 10K pull down to GND for SRC5

ASUS Title : **CLOCK GEN**
 ASUSTek COMPUTER INC Engineer: **Howard Tu**
 Size Project Name
 Custom **A3H**
 Date: Thursday, June 30, 2005 Sheet 20 of 54



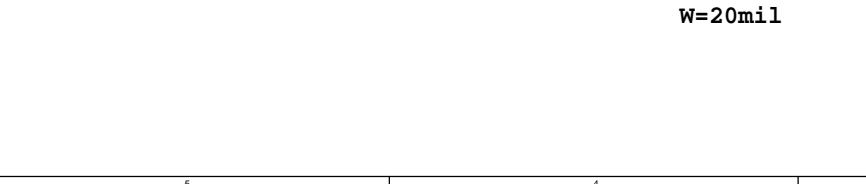
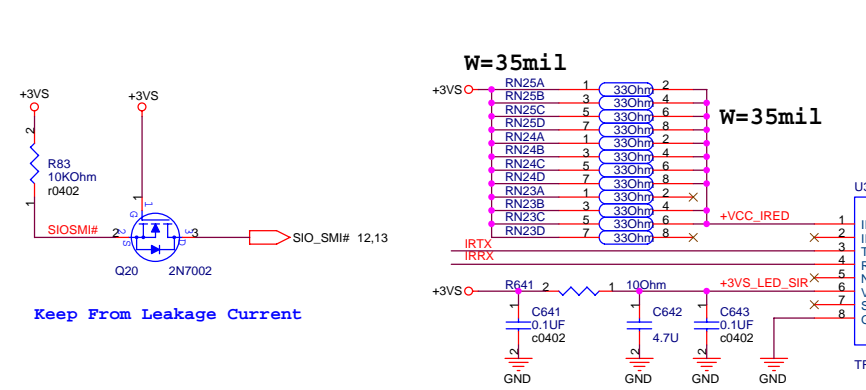
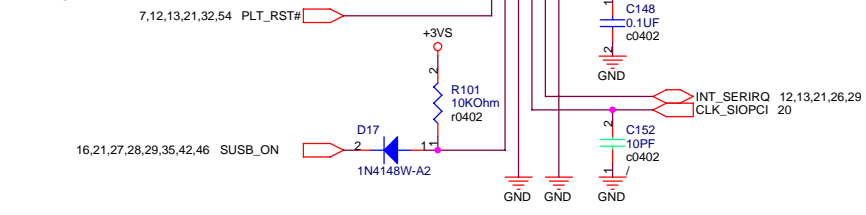
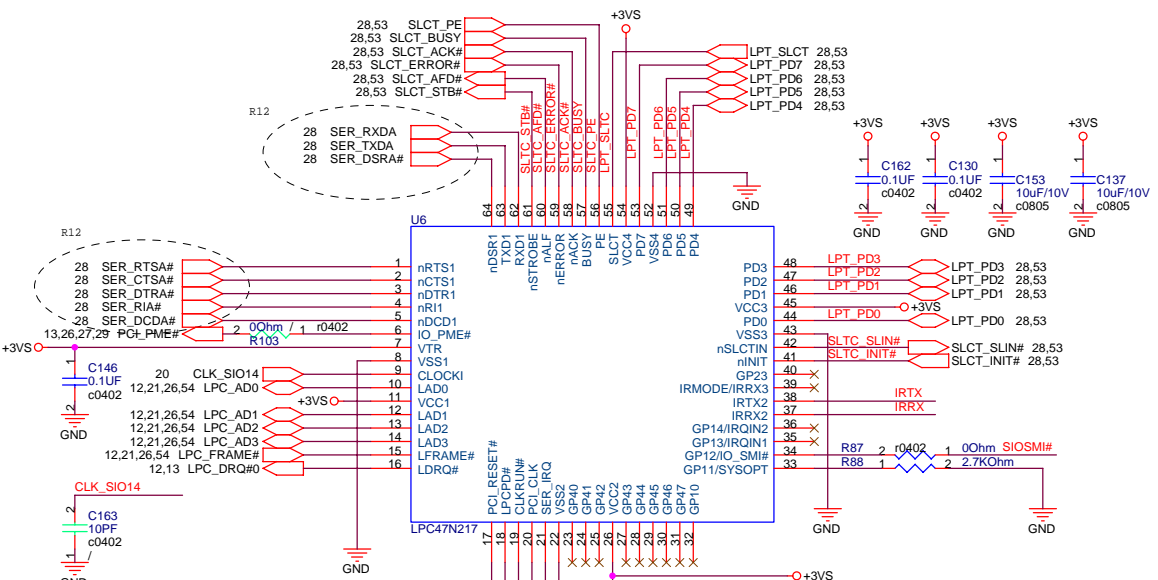
	JP	UK	US
KID1	H	H	L
KID2	L	H	L

$t_D = 0.69 \times 10^{-6} \times C_D \text{ pin sec}$
 $= 690 \text{ ms}$

Change threshold = 2.9V

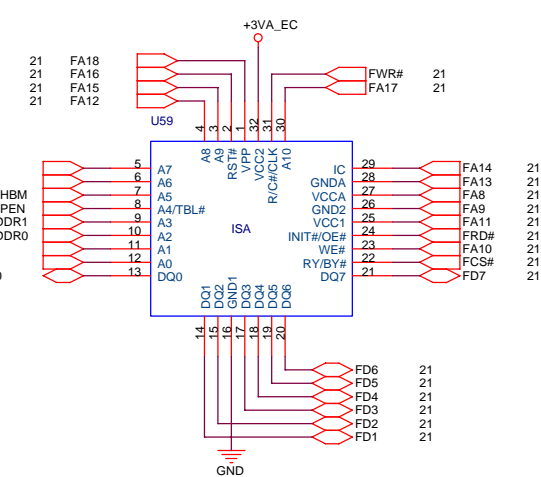
Cload=12.5PF
 close to EC
 start up time : 750ms

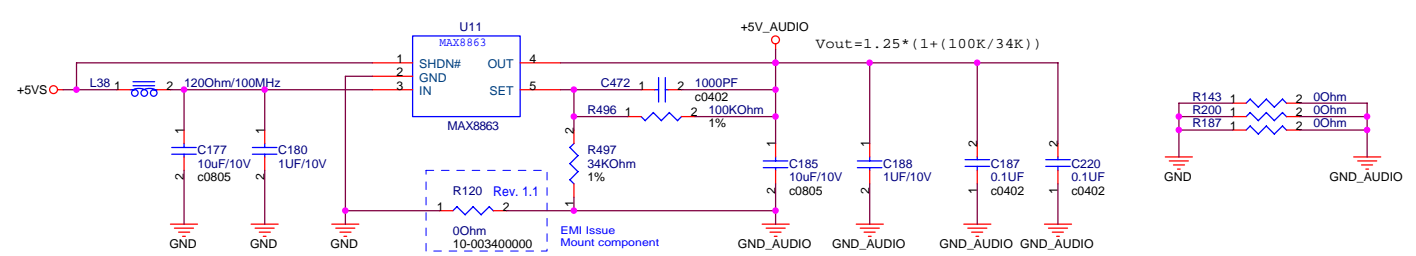
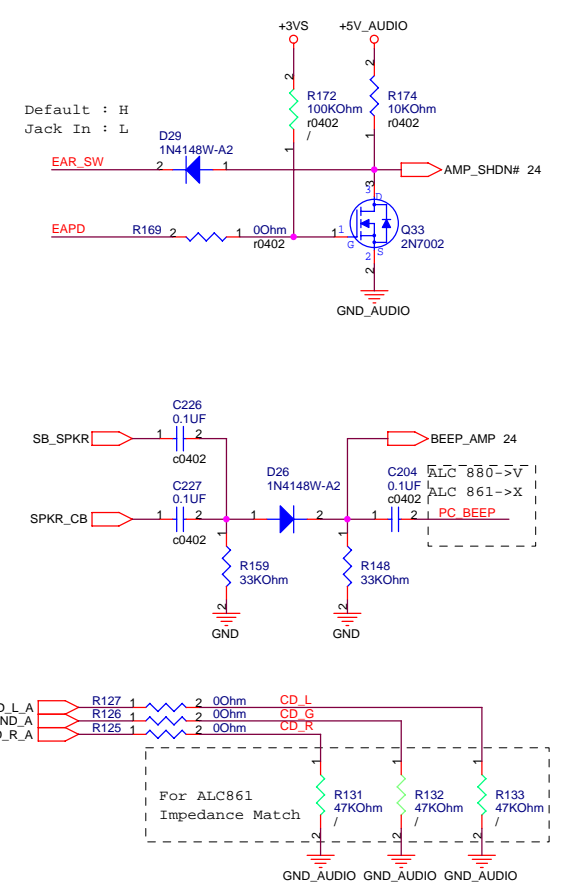
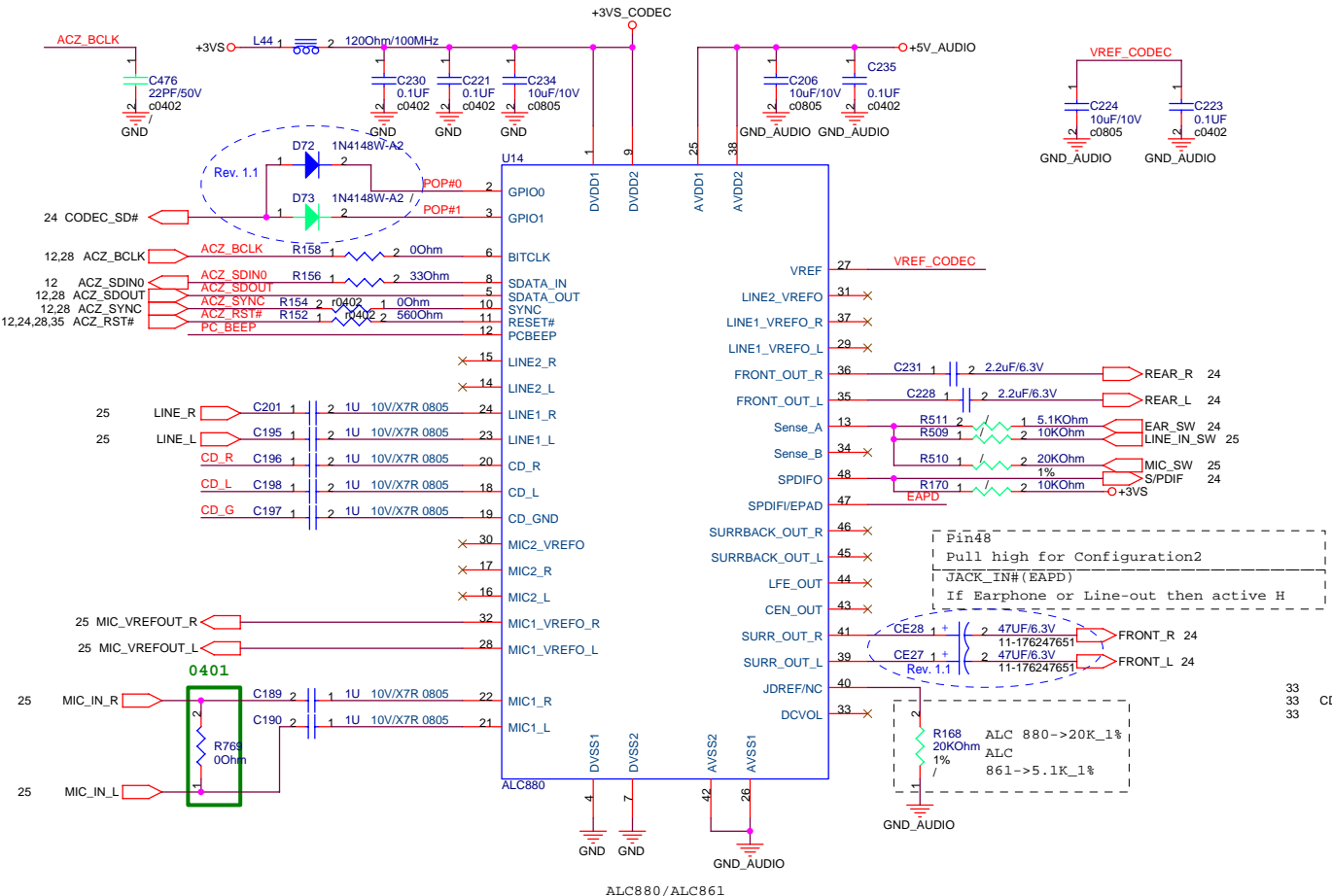
Super I/O

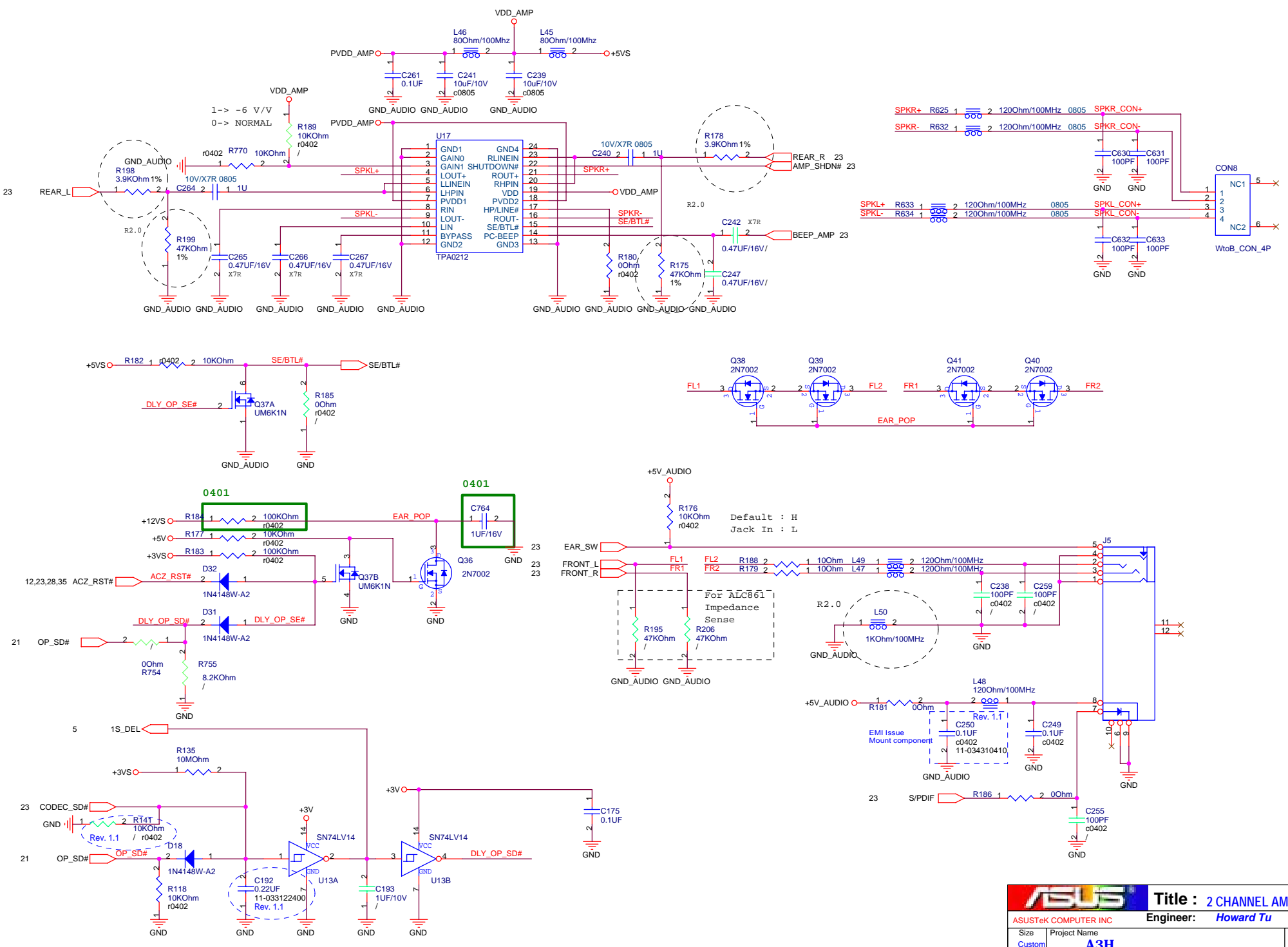


PLCC32 Socket
PN:12-043000321

SST-PLCC32 4Mbits Flash ROM
PN:05-001004100(+3.3V)

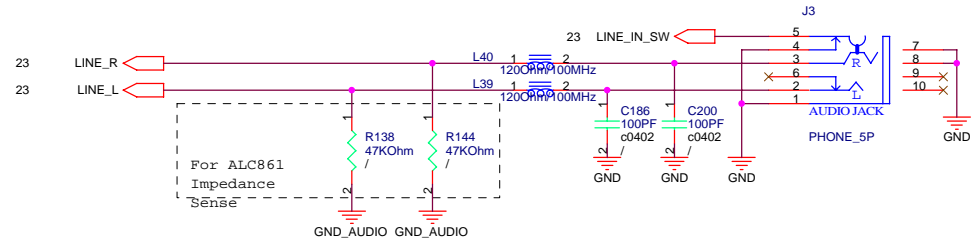
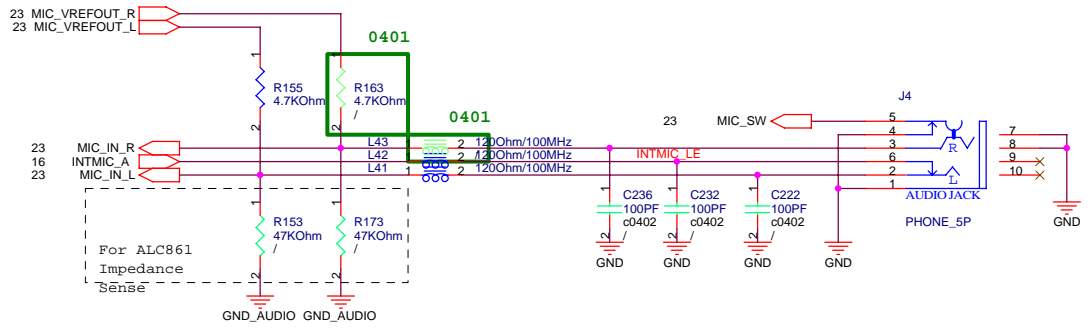
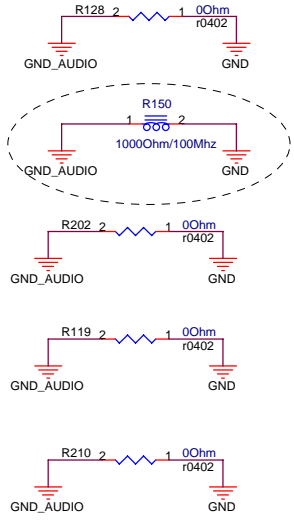
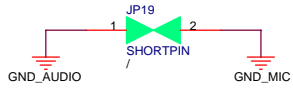


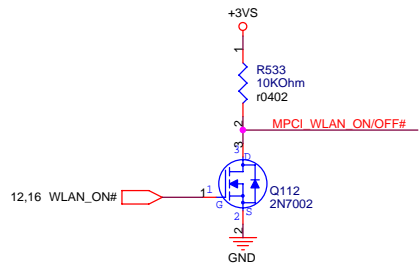




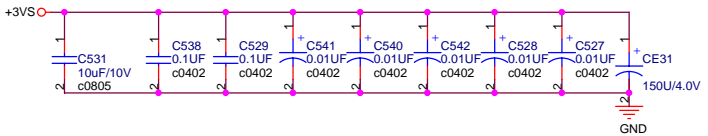
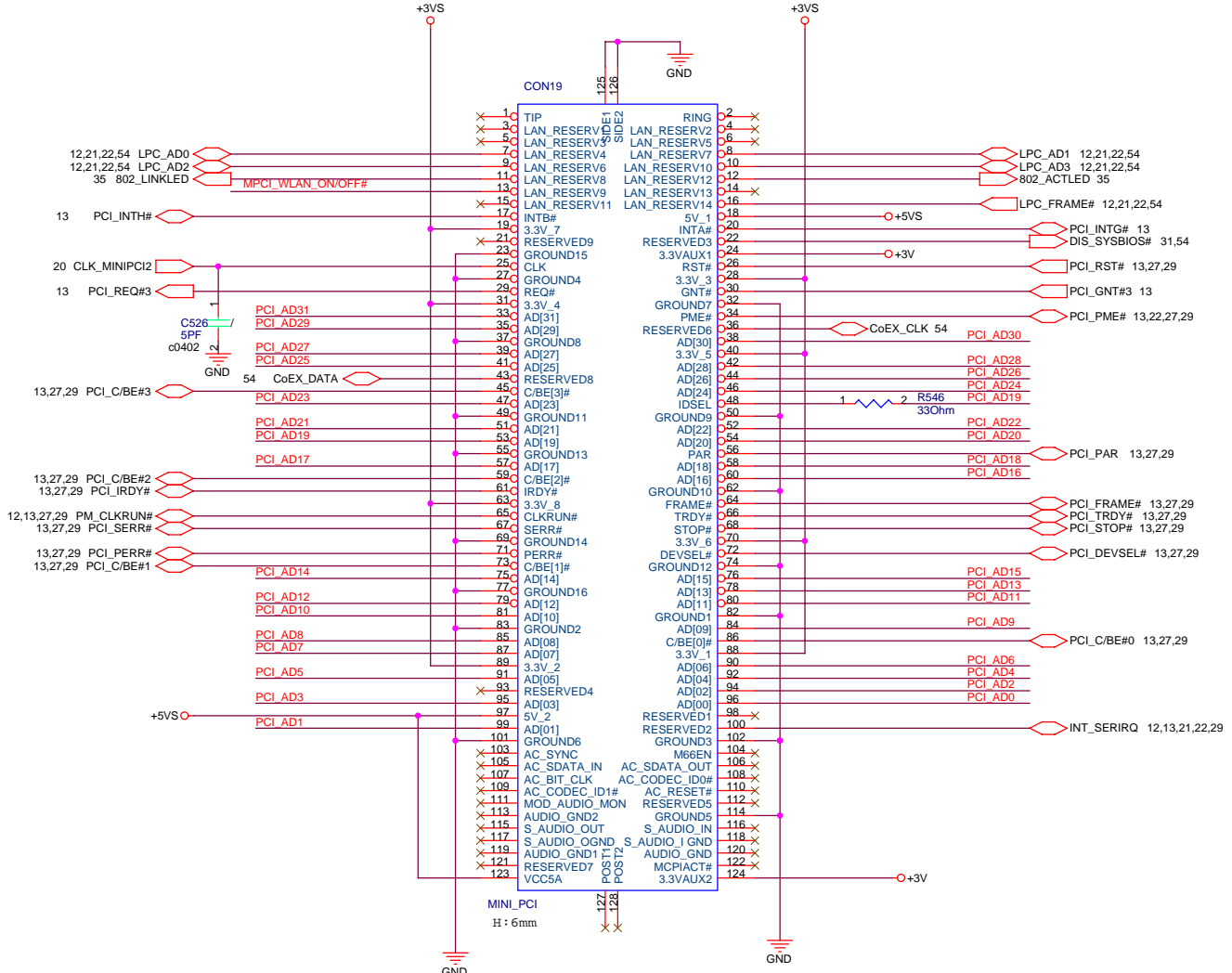
INTMIC_A:GND_AUDIO

: W/P/X = 12/5/15mils



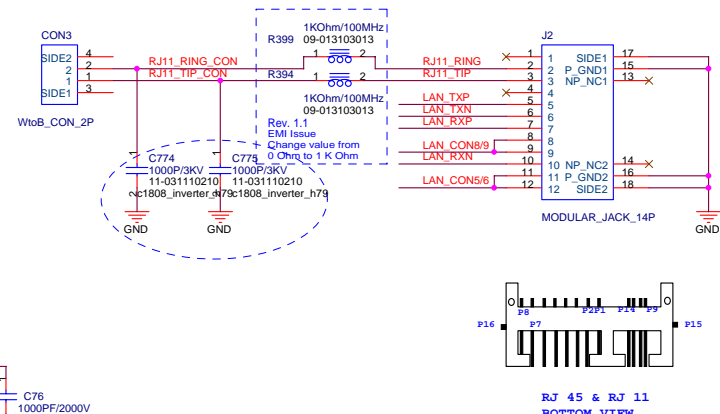
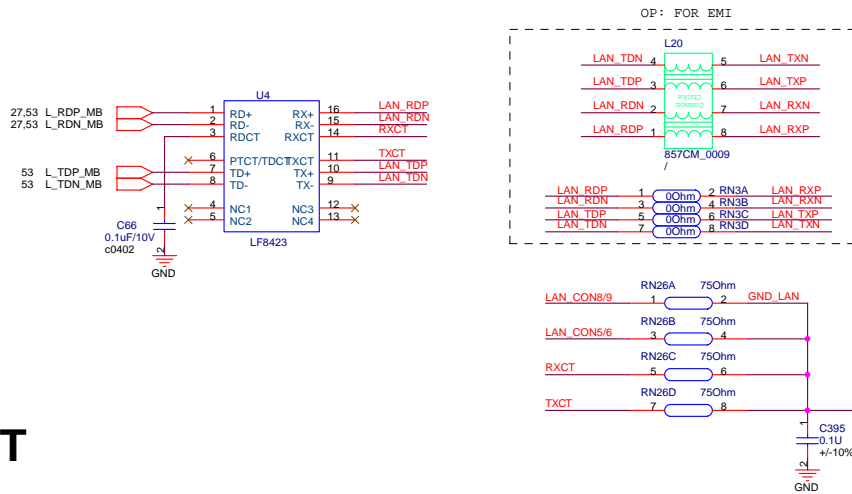


13,27,29 PCI_AD[0..31]

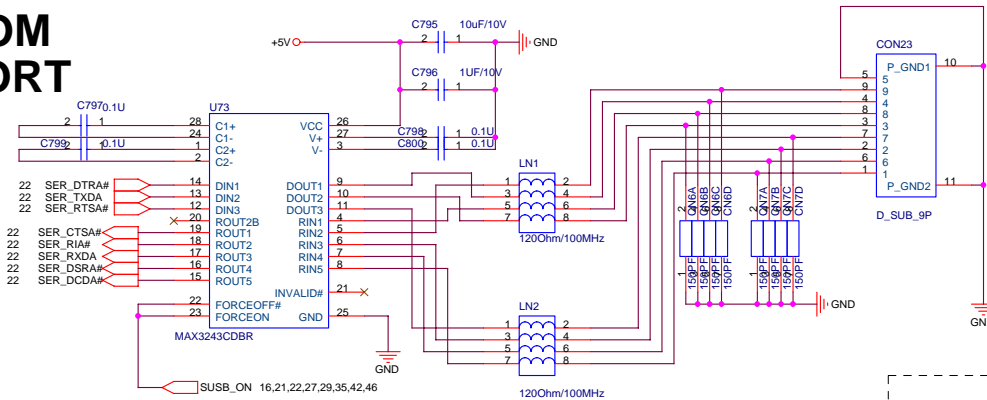


		Title : MINI PCI (802.11)	
ASUSTek COMPUTER INC		Engineer: Howard Tu	
Size	Project Name		Rev
Custom	A3H		1.0
Date: Thursday, June 30, 2005	Sheet	26	of 54

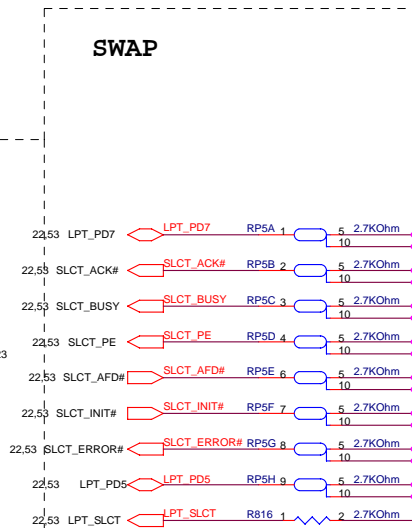
LAN PORT



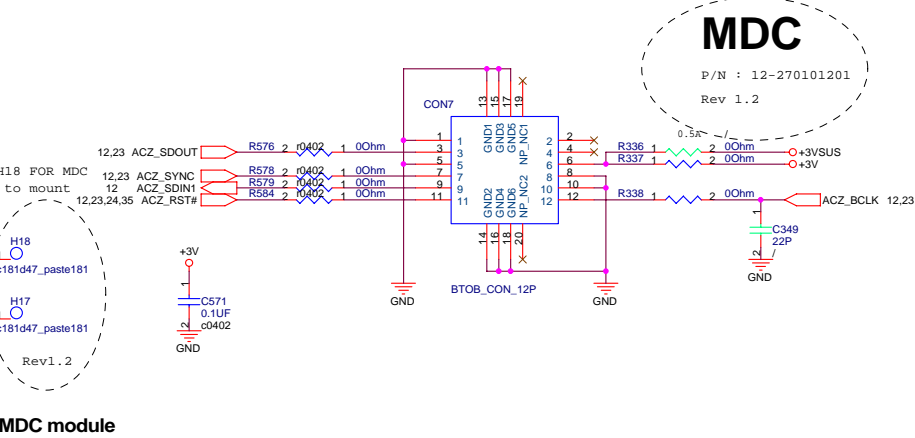
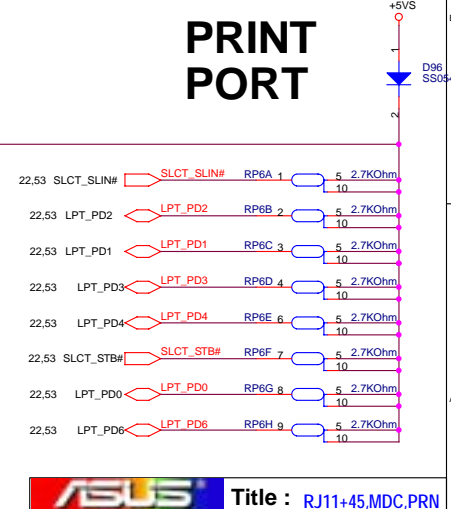
COM PORT



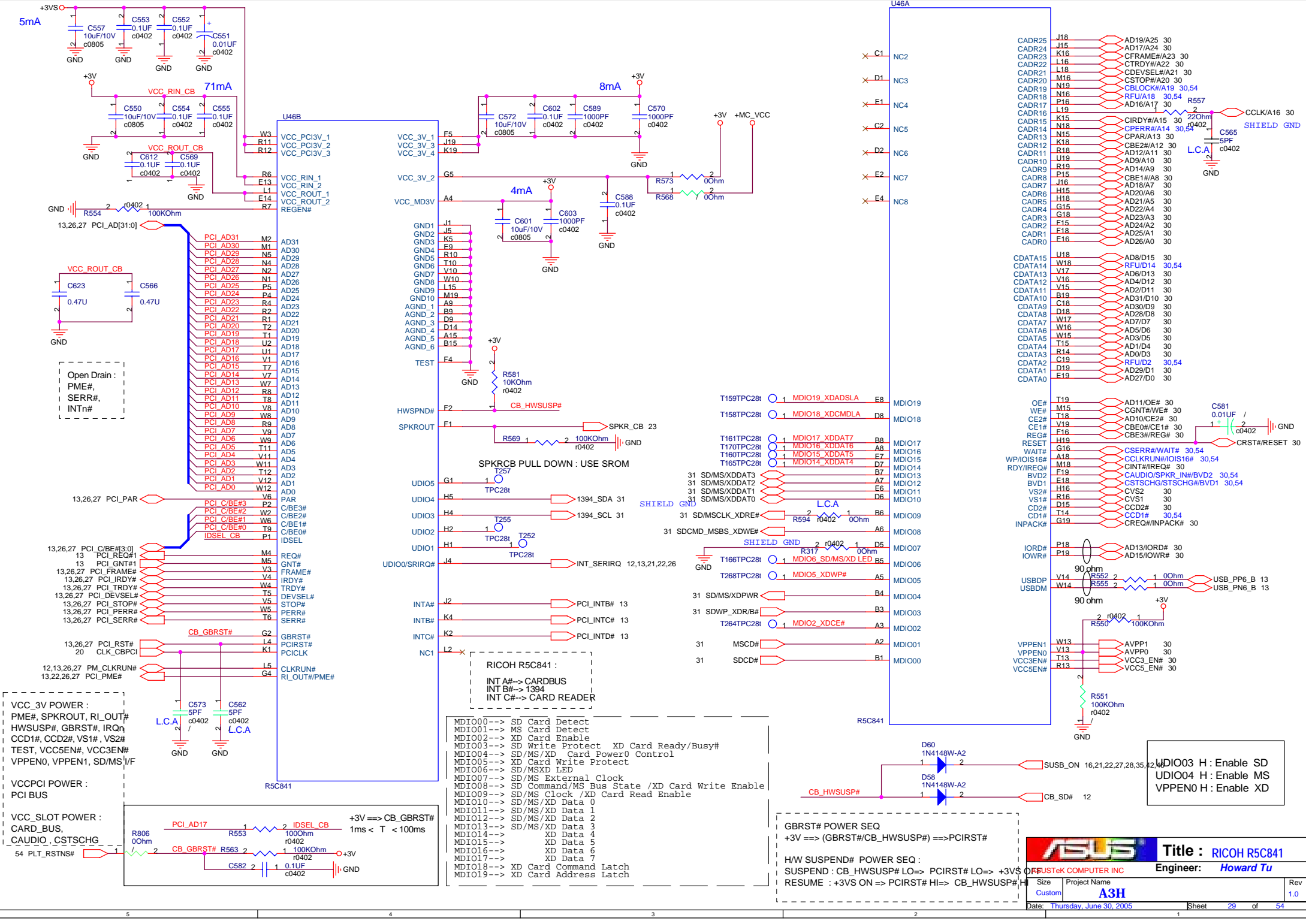
SWAP



PRINT PORT



ASUS Title : RJ11+45,MDC,PRN
 ASUSTek COMPUTER INC Engineer: Howard Tu
 Size Project Name Rev
 Custom A3H 1.0
 Date: Thursday, June 30, 2005 Sheet 28 of 54



RICOH R5C841 :
 INT A#-> CARDBUS
 INT B#-> 1394
 INT C#-> CARD READER

MDIO00-->	SD Card Detect
MDIO01-->	MS Card Detect
MDIO02-->	XD Card Enable
MDIO03-->	SD Write Protect / XD Card Ready/Busy#
MDIO04-->	SD/MS/XD Card Power0 Control
MDIO05-->	XD Card Write Protect
MDIO06-->	SD/MSXD LED
MDIO07-->	SD/MS External Clock
MDIO08-->	SD Command/MS Bus State /XD Card Write Enable
MDIO09-->	SD/MS Clock /XD Card Read Enable
MDIO10-->	SD/MS/XD Data 0
MDIO11-->	SD/MS/XD Data 1
MDIO12-->	SD/MS/XD Data 2
MDIO13-->	SD/MS/XD Data 3
MDIO14-->	SD/MS/XD Data 4
MDIO15-->	SD/MS/XD Data 5
MDIO16-->	SD/MS/XD Data 6
MDIO17-->	SD/MS/XD Data 7
MDIO18-->	XD Card Command Latch
MDIO19-->	XD Card Address Latch

GBRST# POWER SEQ
 +3V ==> (GBRST#/CB_HWSUSP#) ==> PCIRST#

H/W SUSPEND# POWER SEQ :
 SUSPEND : CB_HWSUSP# LO=> PCIRST# LO=> +3VS
 RESUME : +3VS ON => PCIRST# HI=> CB_HWSUSP# H

MDIO03 H: Enable SD
 UDIO04 H: Enable MS
 VPPEN0 H: Enable XD

ASUS Title : RICOH R5C841

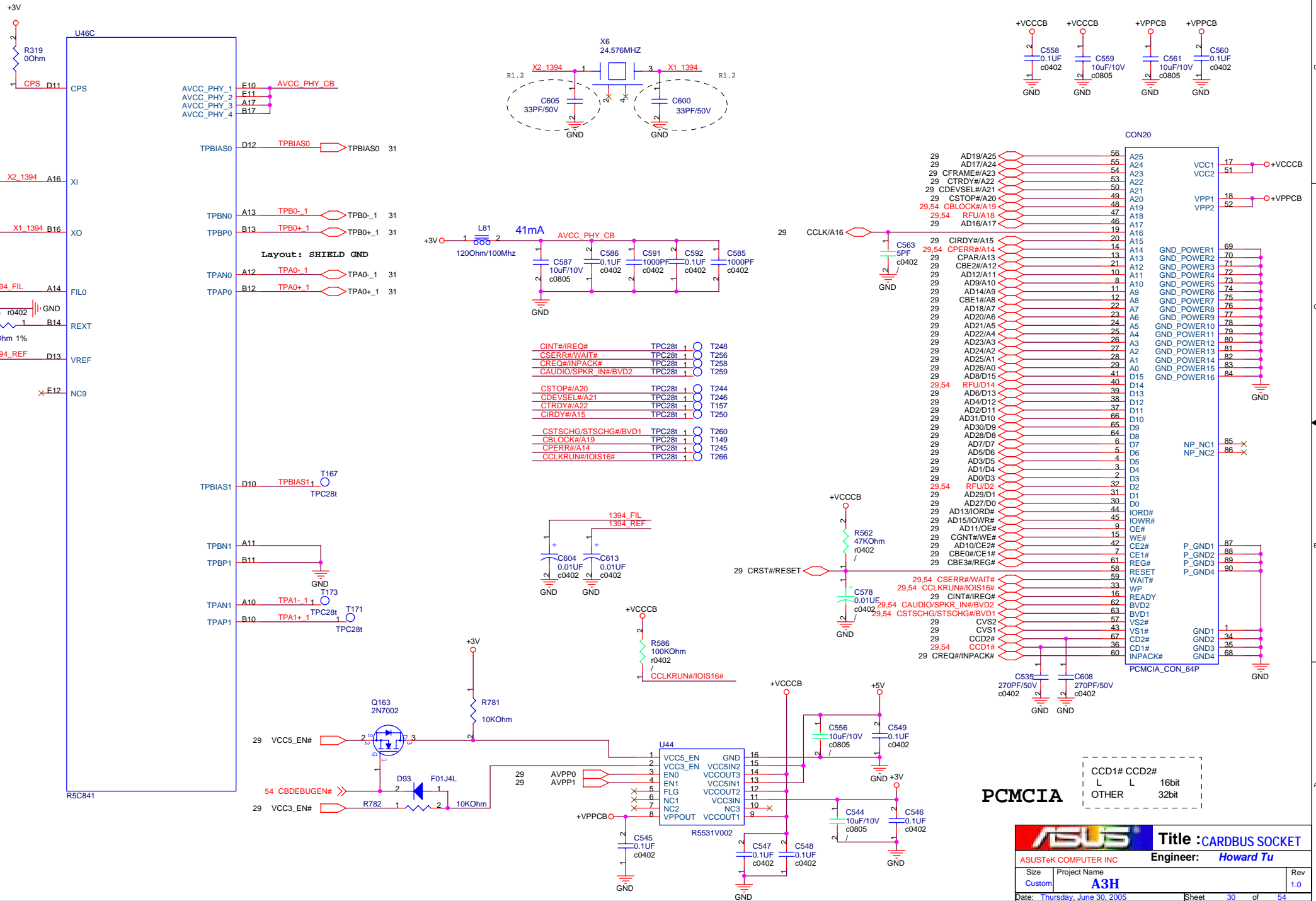
Engineer: Howard Tu

Project Name: A3H

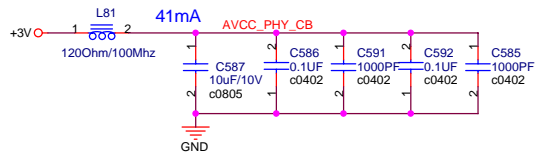
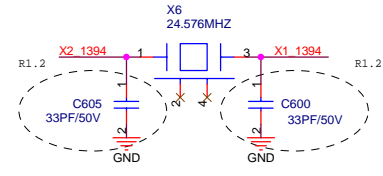
Size: Custom

Date: Thursday, June 30, 2005

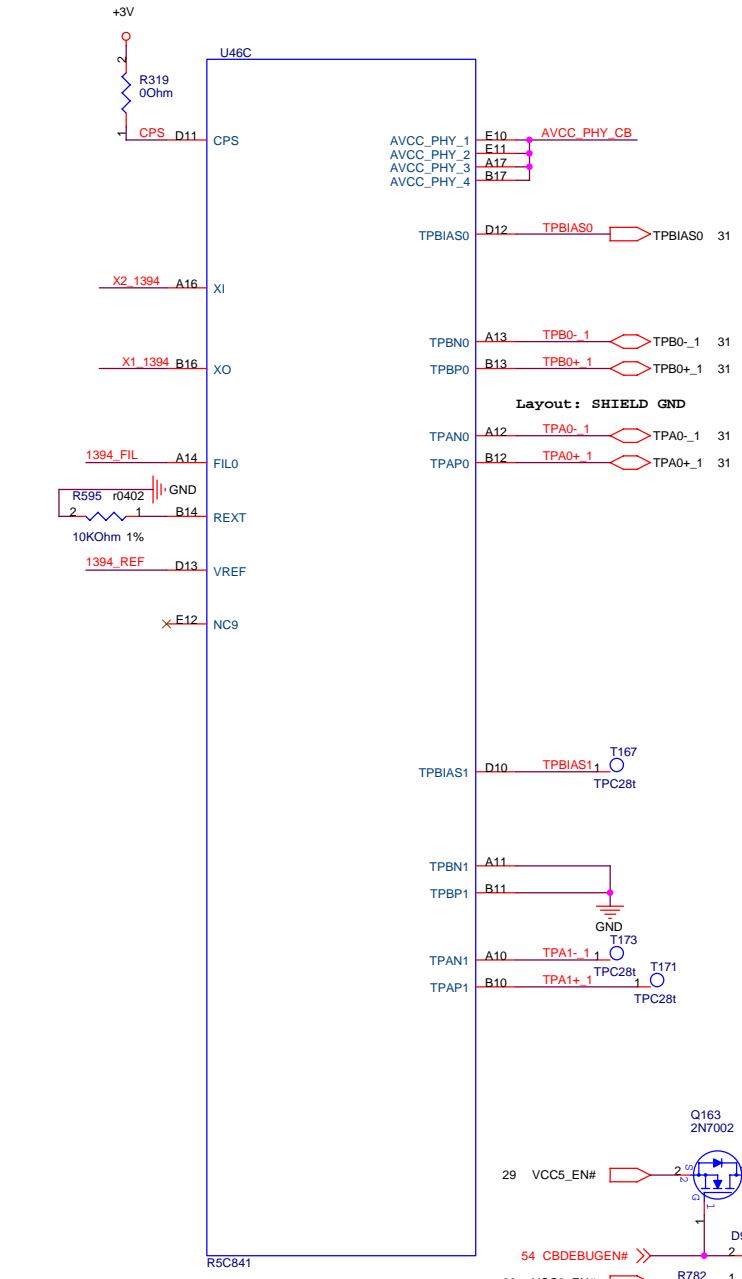
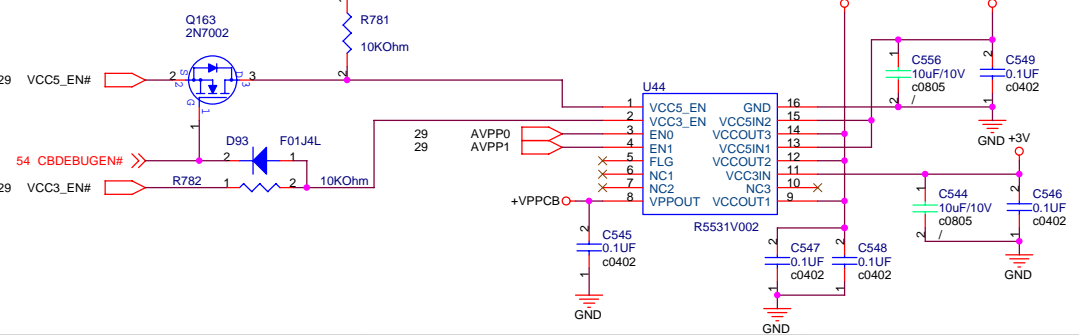
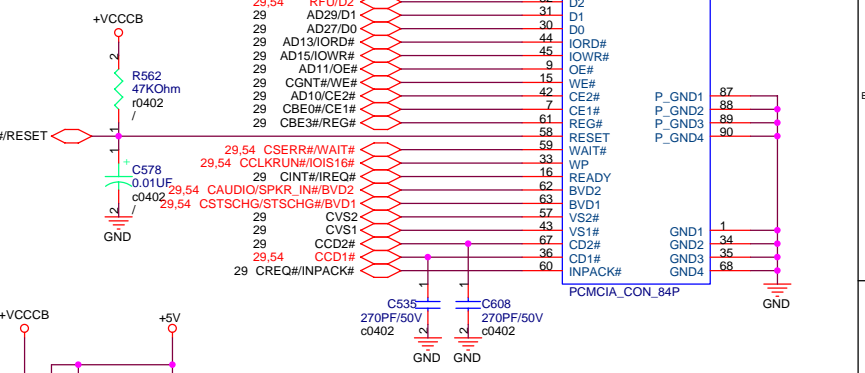
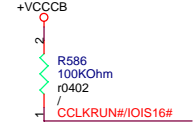
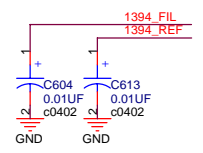
Sheet 29 of 54

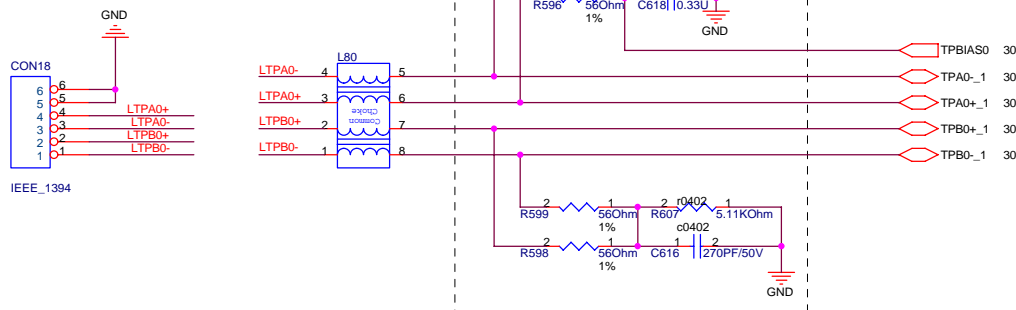


ASUS Title : CARBUS SOCKET
 ASUSTek COMPUTER INC Engineer: Howard Tu
 Size Project Name
 Custom A3H
 Date: Thursday, June 30, 2005 Sheet 30 of 54

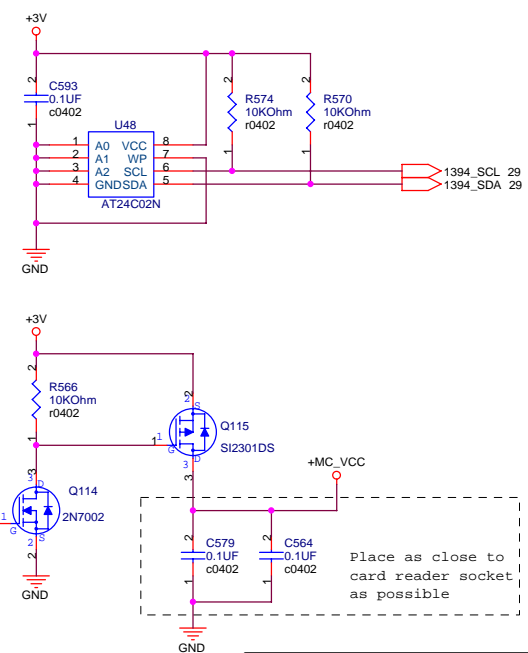


- CINT#/IREQ# TPC28t 1 T248
- CSERR#/WAIT# TPC28t 1 T256
- CREQ#/INPACK# TPC28t 1 T258
- CAUDIO/SPKR_IN#/BVD2 TPC28t 1 T259
- CSTOP#/A20 TPC28t 1 T244
- CDEVSEL#/A21 TPC28t 1 T246
- CTRDY#/A22 TPC28t 1 T157
- CIRDY#/A15 TPC28t 1 T250
- CSTSCHG/STSCHG#/BVD1 TPC28t 1 T260
- CBLOCK#/A19 TPC28t 1 T149
- CPERR#/A14 TPC28t 1 T245
- CCLKRUN#/IOIS16# TPC28t 1 T266





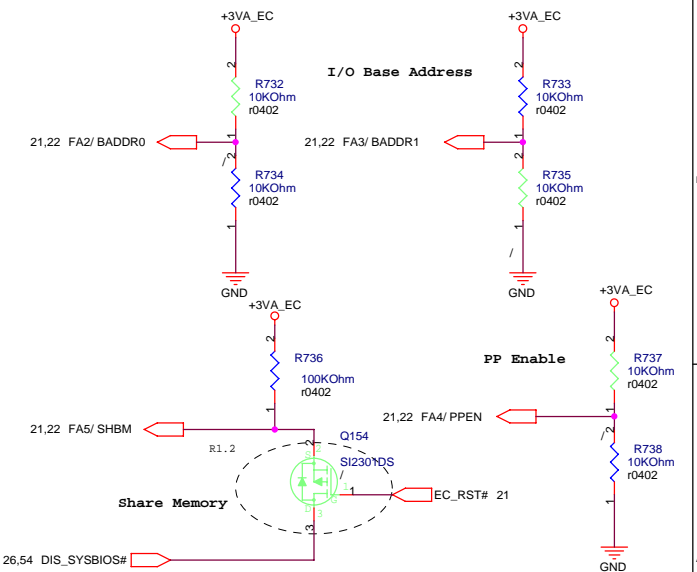
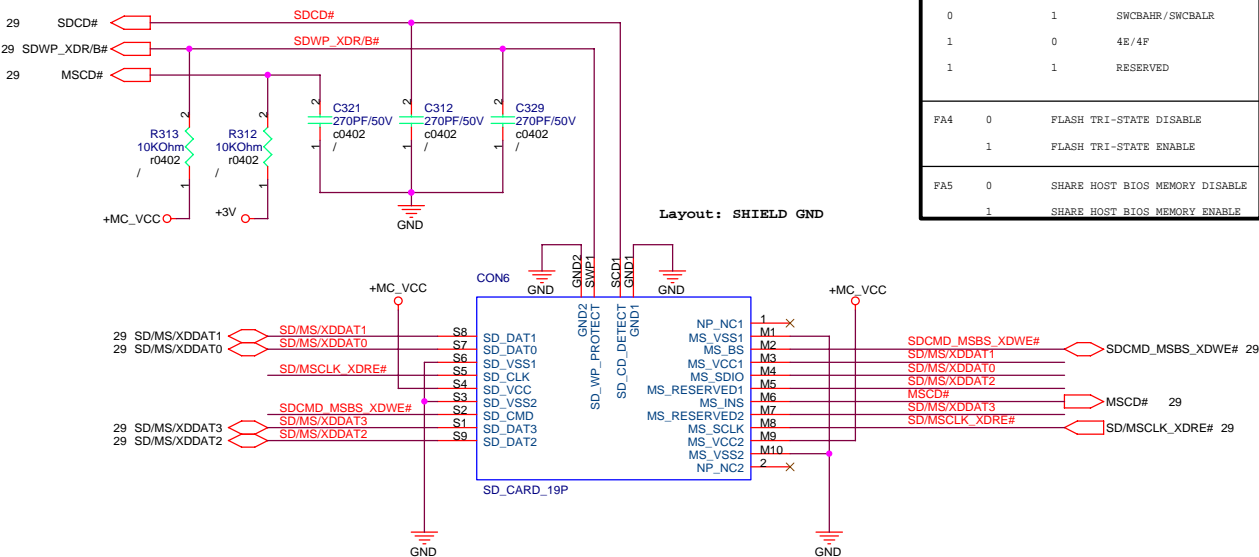
1. CLOSE TO R5C841
2. The area is as compact as possible, length < 10 mm
3. TPA Pair and TPB pair mismatch < 2.5mm
4. No via recommend, maximum is one.
5. Total length < 50 mm
6. Differential impedance is 110+/- 6 ohm
7. TPA Pair trace or TPB pair trace mismatch < 1.25mm

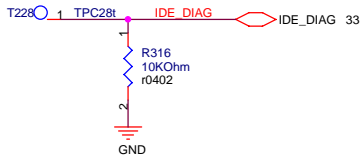


Place as close to card reader socket as possible

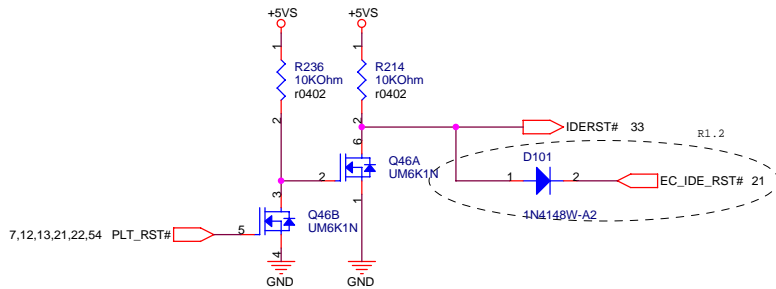
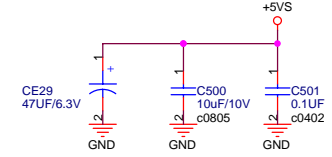
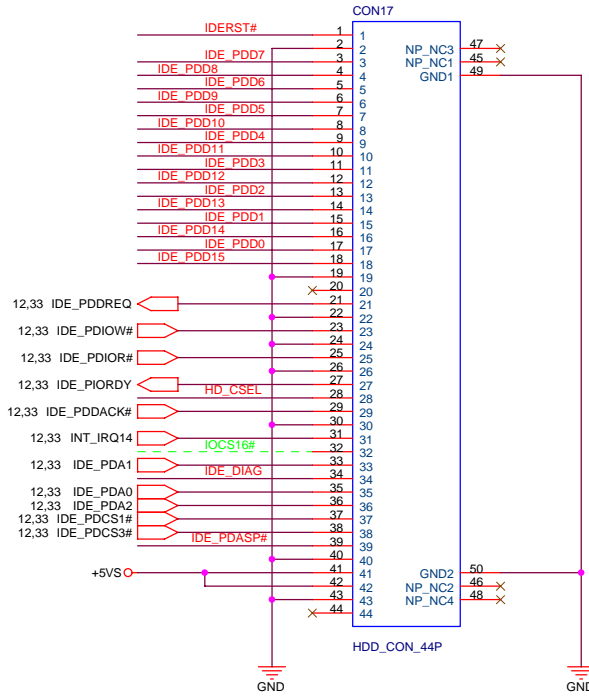
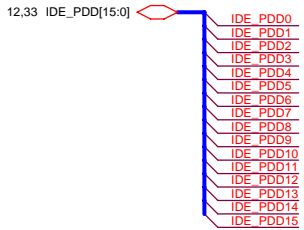
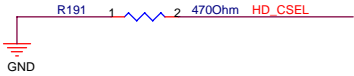
Hardware Strap Pin		
BADDR0/FA2	BADDR1/FA3	PORT
0	0	2E/2F
0	1	SWCBAHR/SWCBALR
1	0	4E/4F
1	1	RESERVED
FA4	0	FLASH TRI-STATE DISABLE
1	1	FLASH TRI-STATE ENABLE
FA5	0	SHARE HOST BIOS MEMORY DISABLE
1	1	SHARE HOST BIOS MEMORY ENABLE

EC Hardware Strap



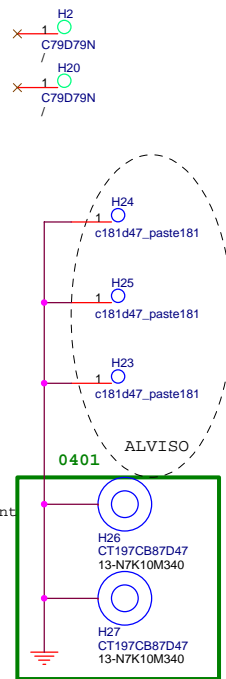
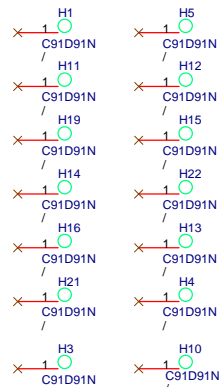
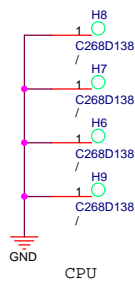
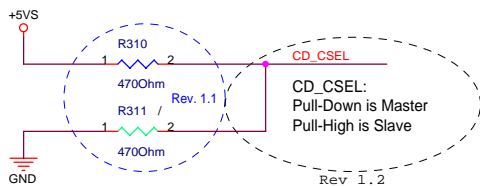
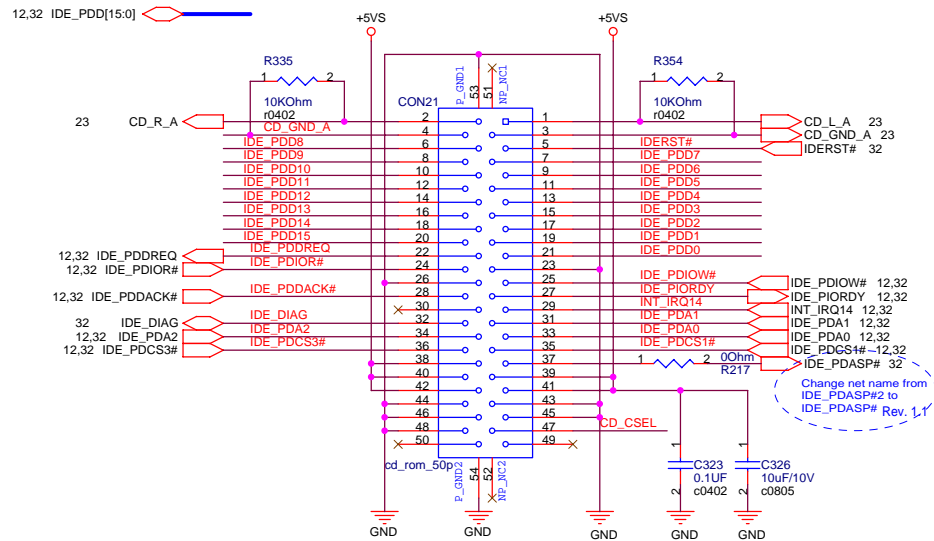
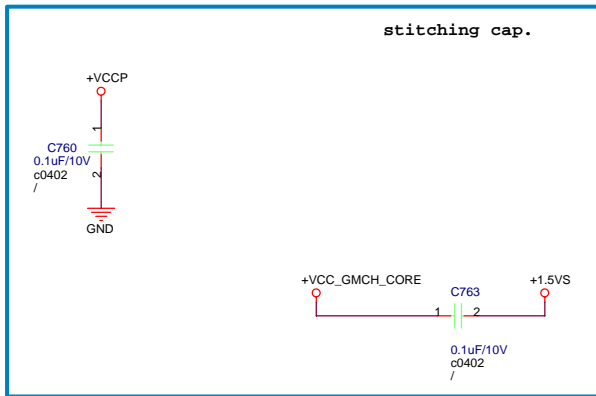


HD_CSEL : Pull-Down, HDD as Master

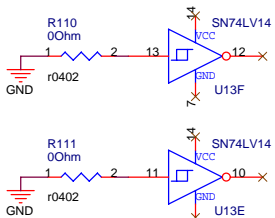


For EMI test (place on TOP layer)

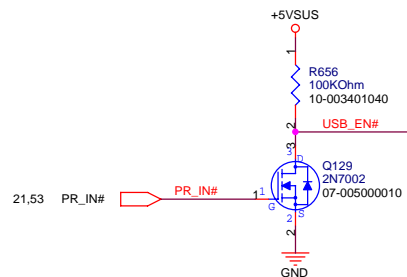
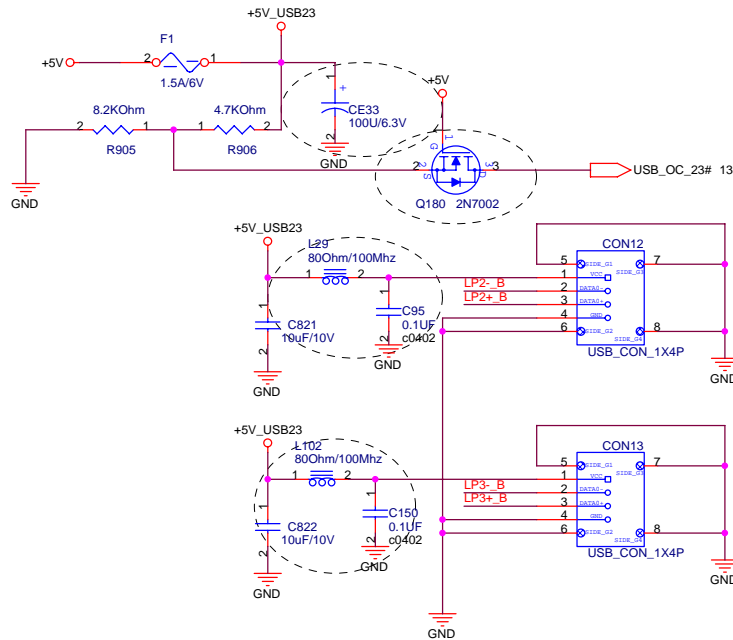
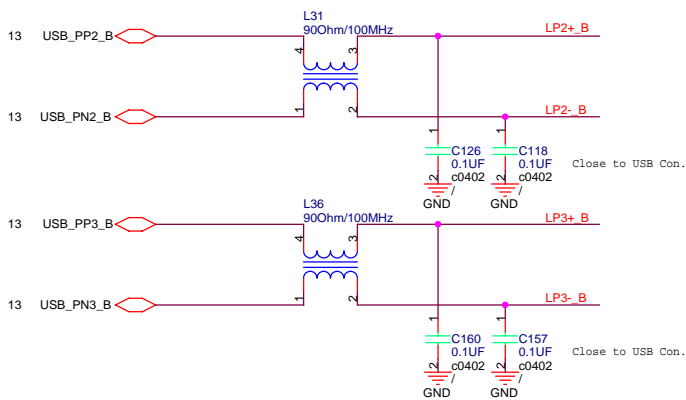
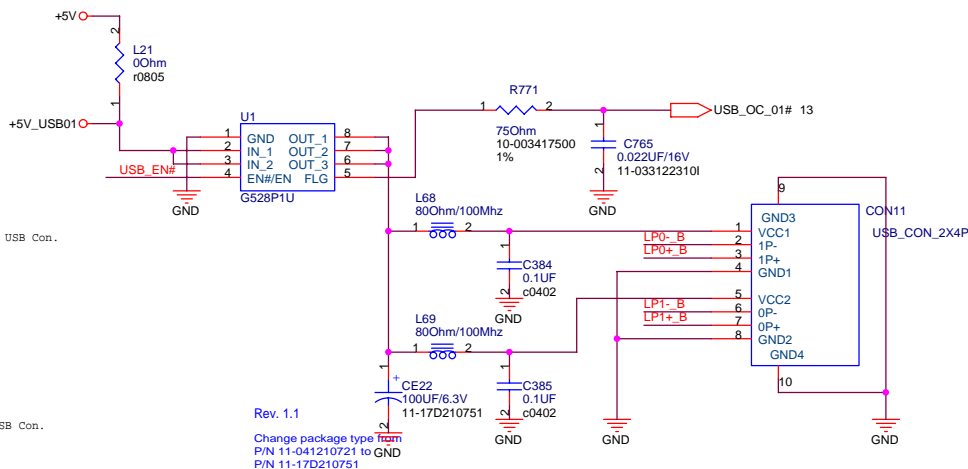
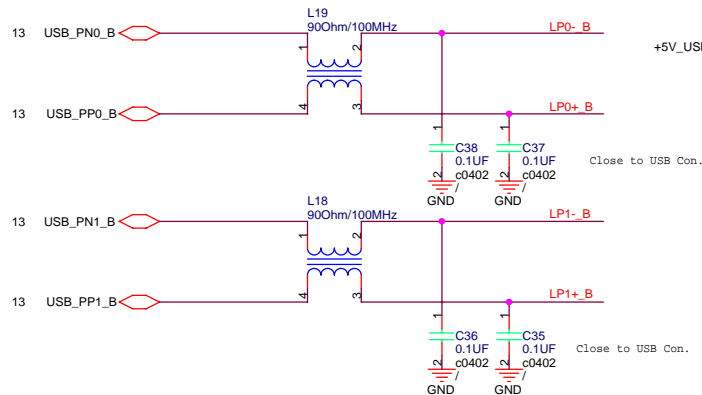
0119

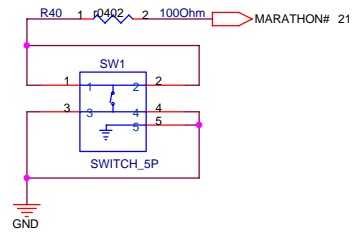


Holes for ALVISO have to mount

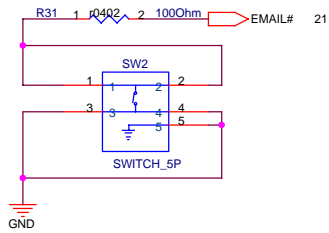


USB

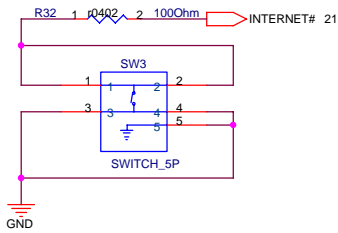




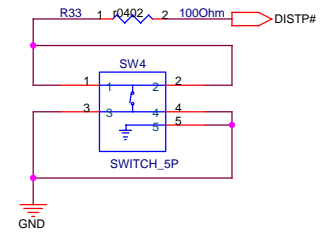
Power4 Gear



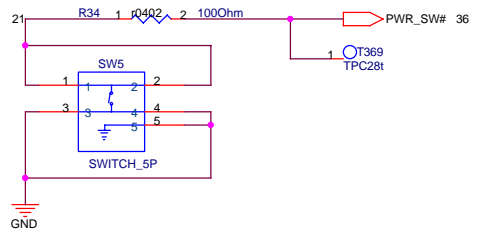
E-Mail



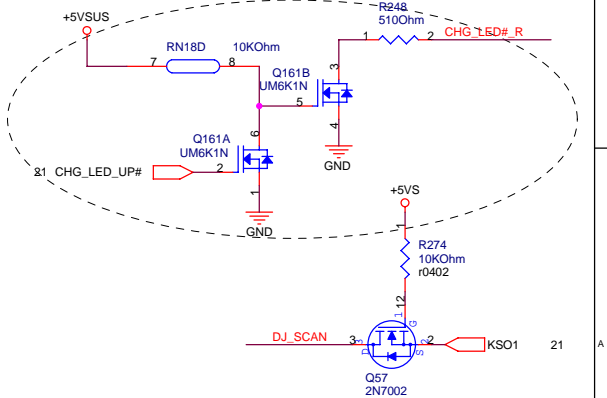
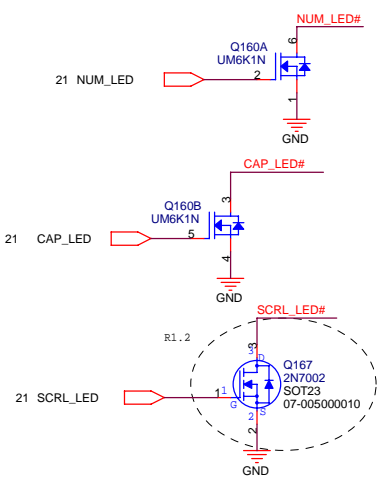
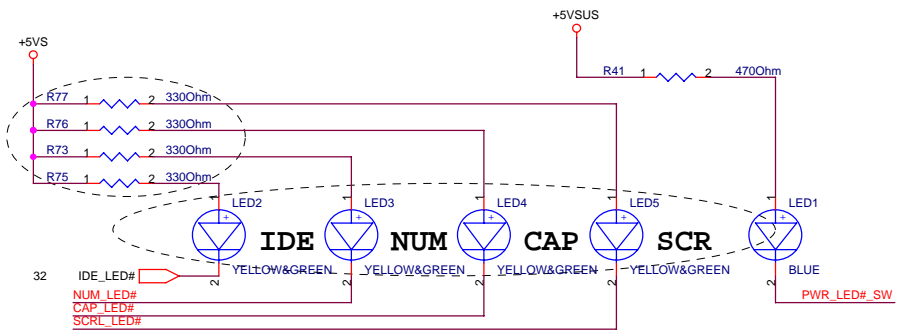
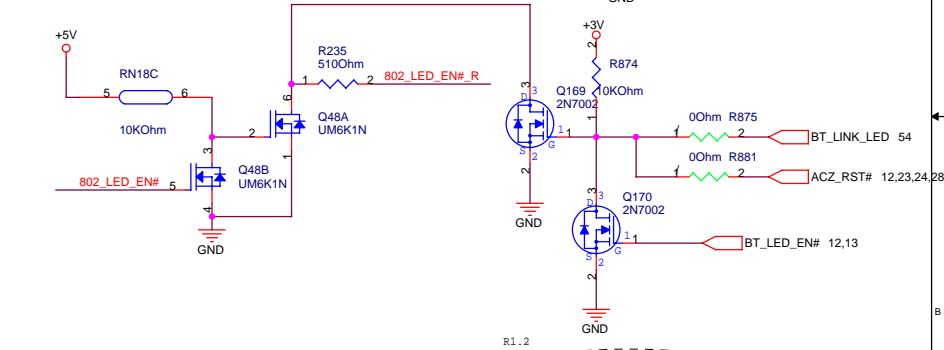
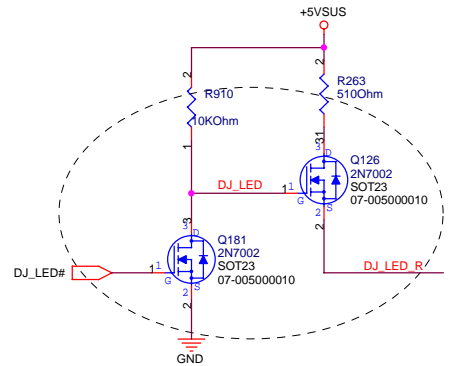
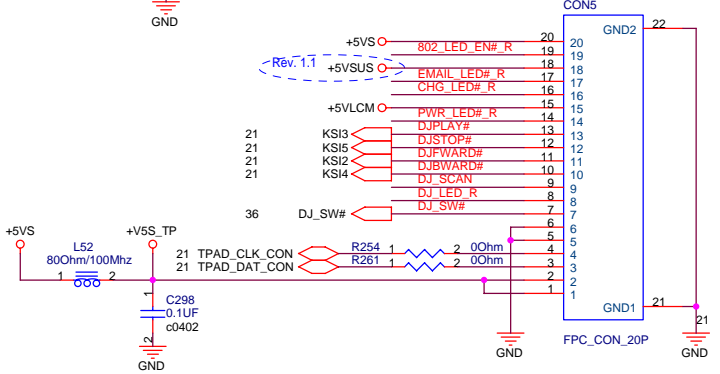
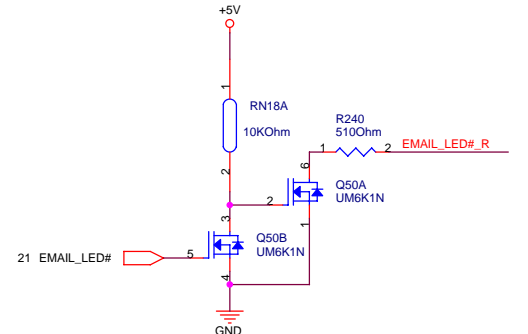
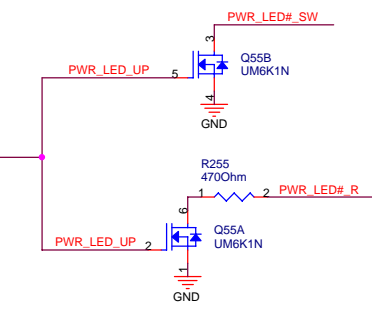
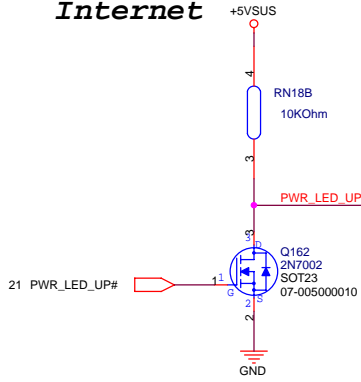
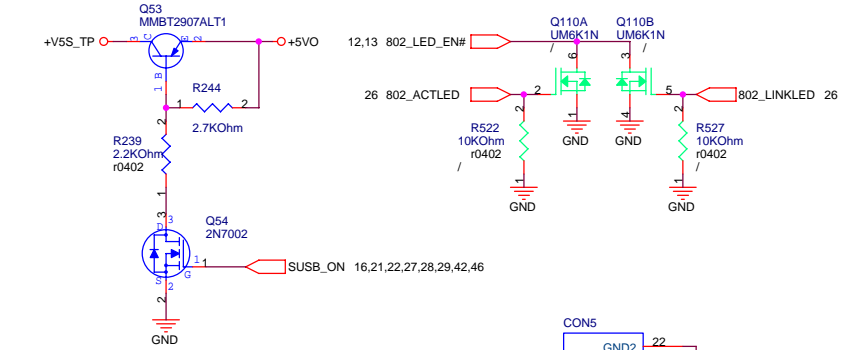
Internet

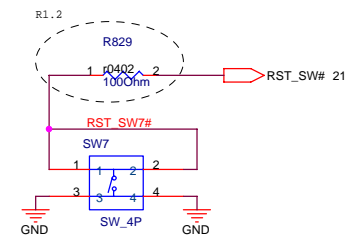
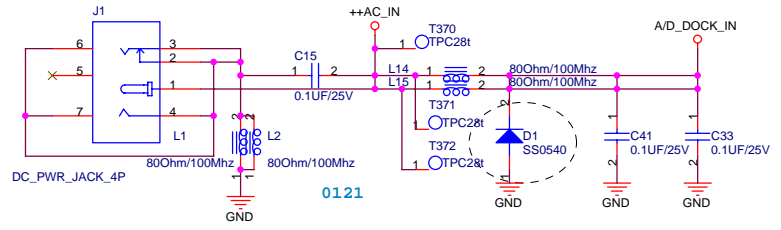
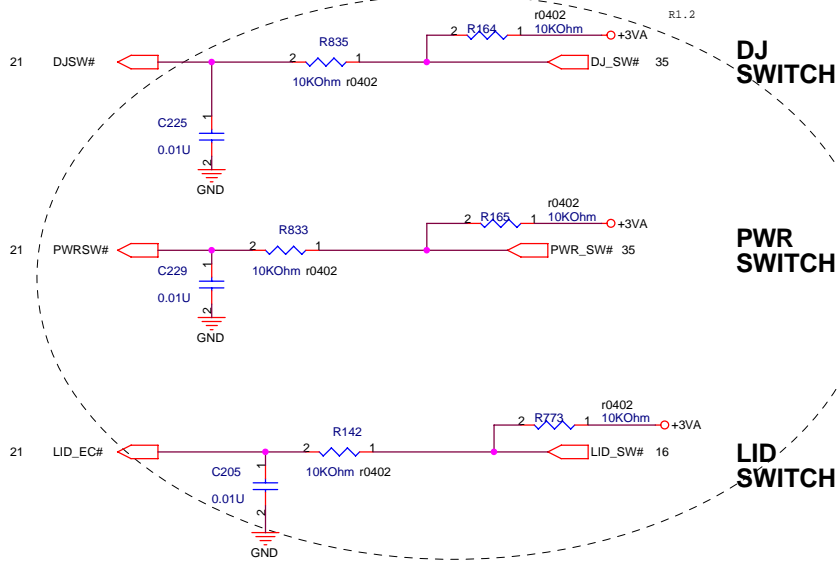


Touchpad Disable



Power Switch





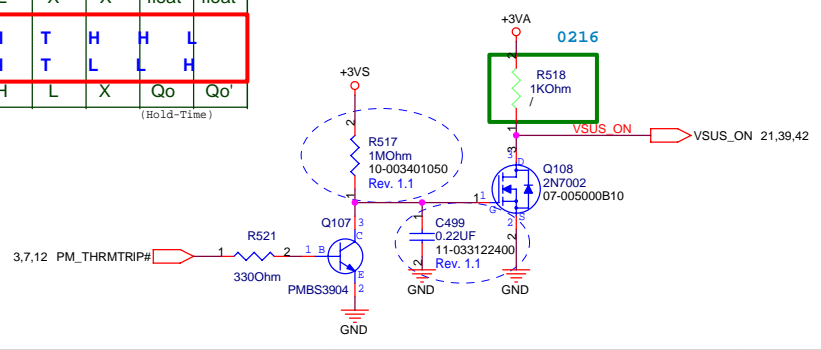
System Power Sequence
 +VCCRTC -> RTCRST# -> V5REFSUS -> 3.3/1.5VSUS ->
 RSMRST# -> SUSC# -> SUSB# -> VCCLAN -> LANPWROK
 -> V5REF -> PWROK -> GMCH -> VCCP -> VCORE
 SUSSTAT# -> PCIRST#
 CPU : +VCORE, +VCCP, +1.05VS
 NB : +1.05VS, +1.5VS, +2.5V, +VCCP
 SB : +1.5VSUS, +3.3VSUS, +VCCP, +1.5VS, +3.3VS
 DDR : +1.8V, +0.9VS
 M24 : +3.3VS, +2.5VS, +1.5VS, +1.8VS, AC_BAT_SYS

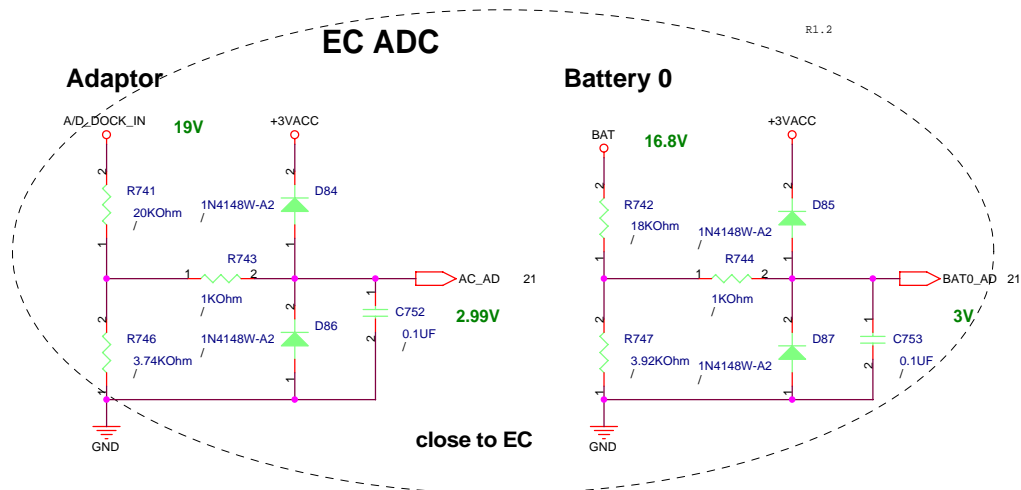
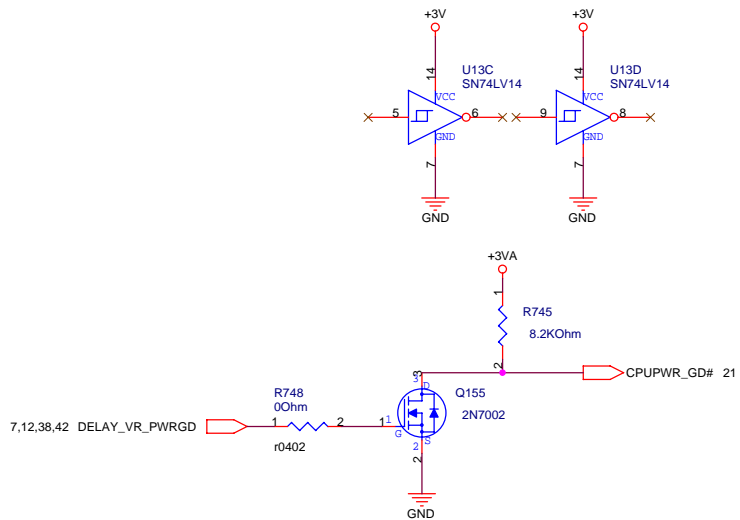
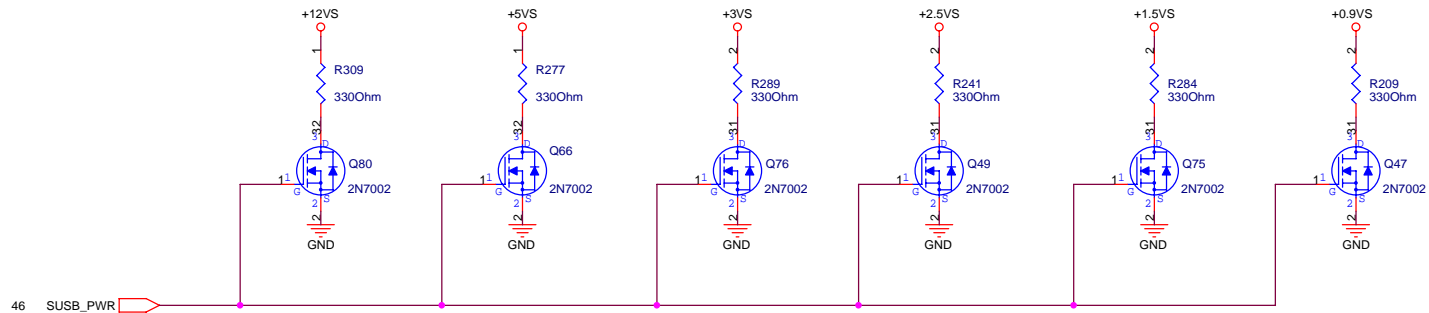
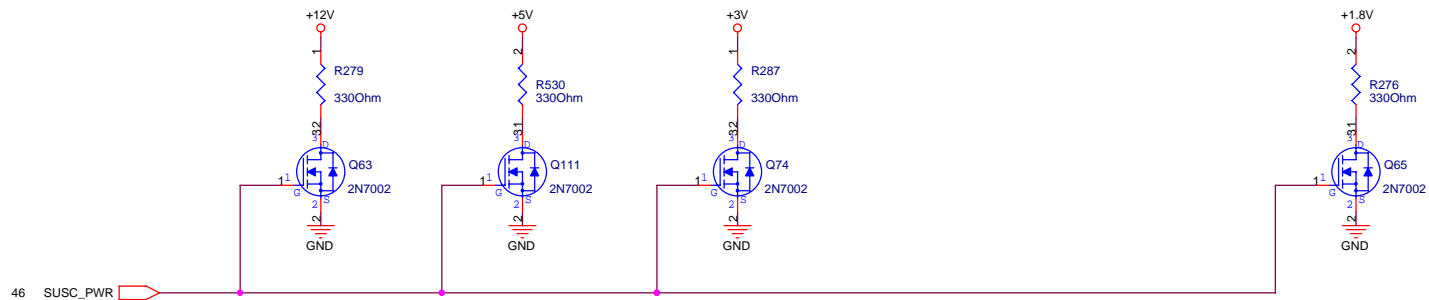
ASUS Title : Startup Circuit (1)
 ASUSTek COMPUTER INC Engineer: Howard Tu
 Size Project Name
 Custom A3H Rev 1.0
 Date: Thursday, June 30, 2005 Sheet 36 of 54

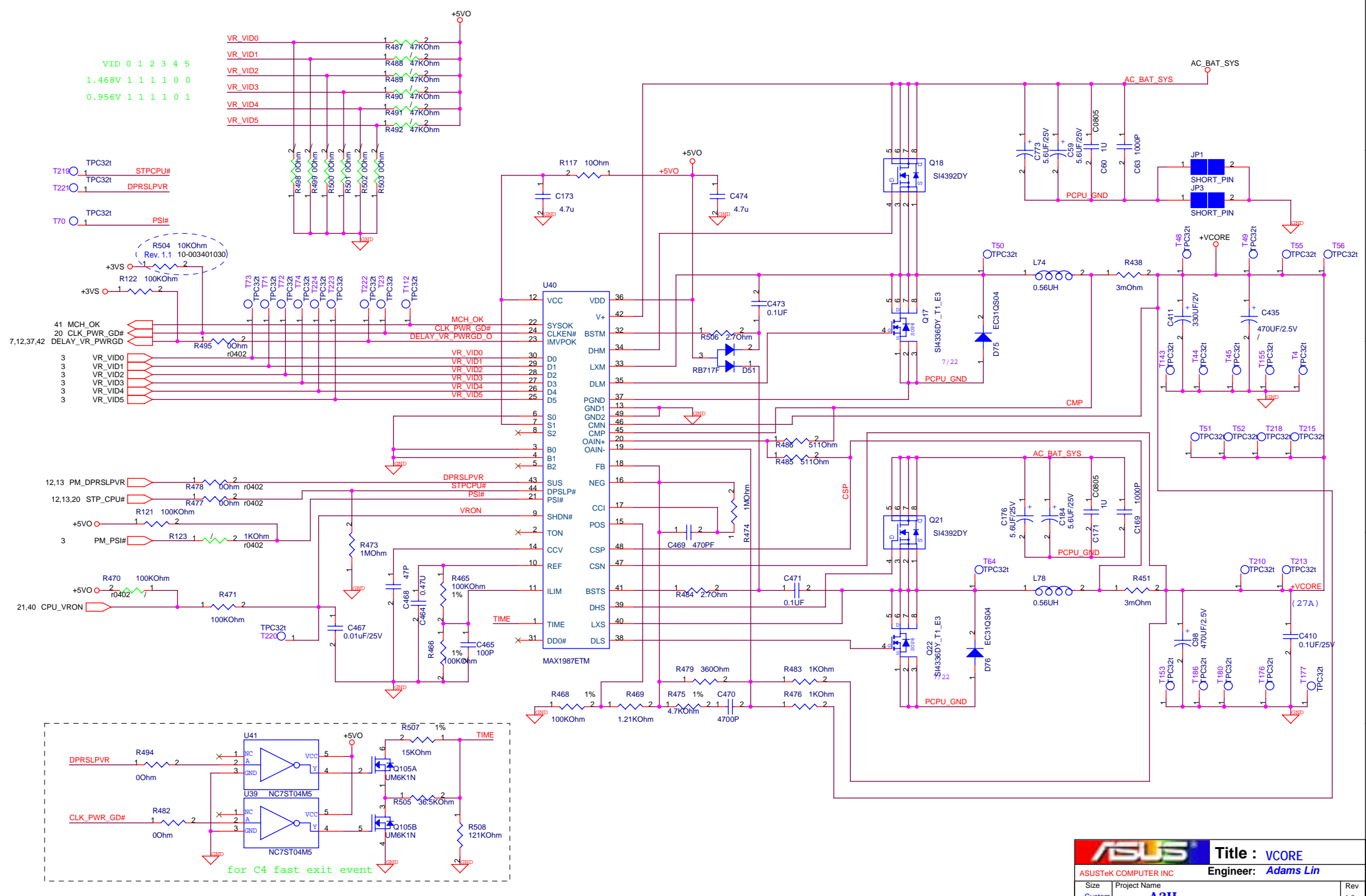
74HC74 TRUTH TABLE Rev 1.2

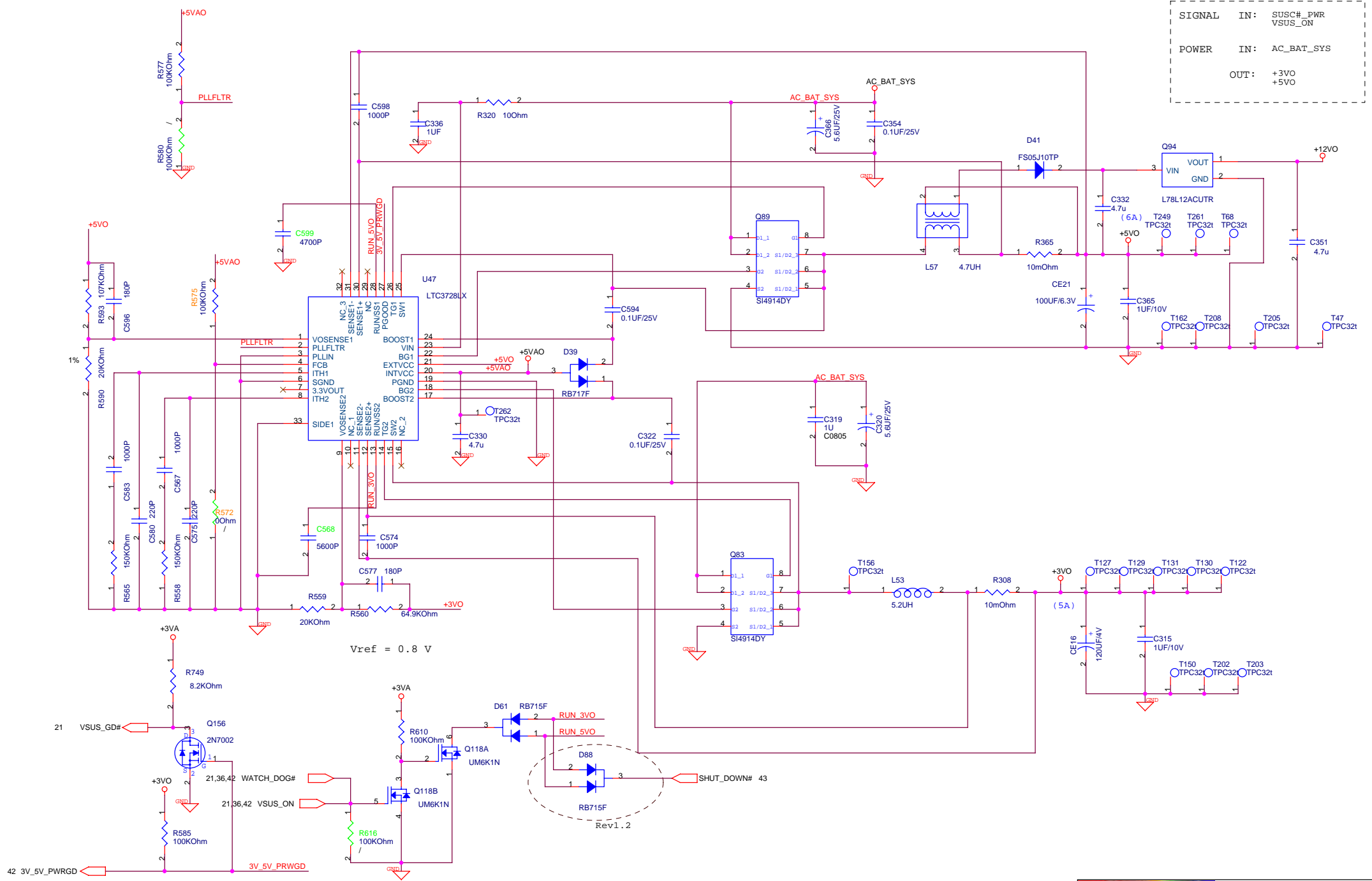
PRE#	CLR#	CLK	D	Q	Q'
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	float	float
H	H	T	H	H	L
H	H	T	L	L	H
H	H	L	X	Qo	Qo'

(Hold-Time)

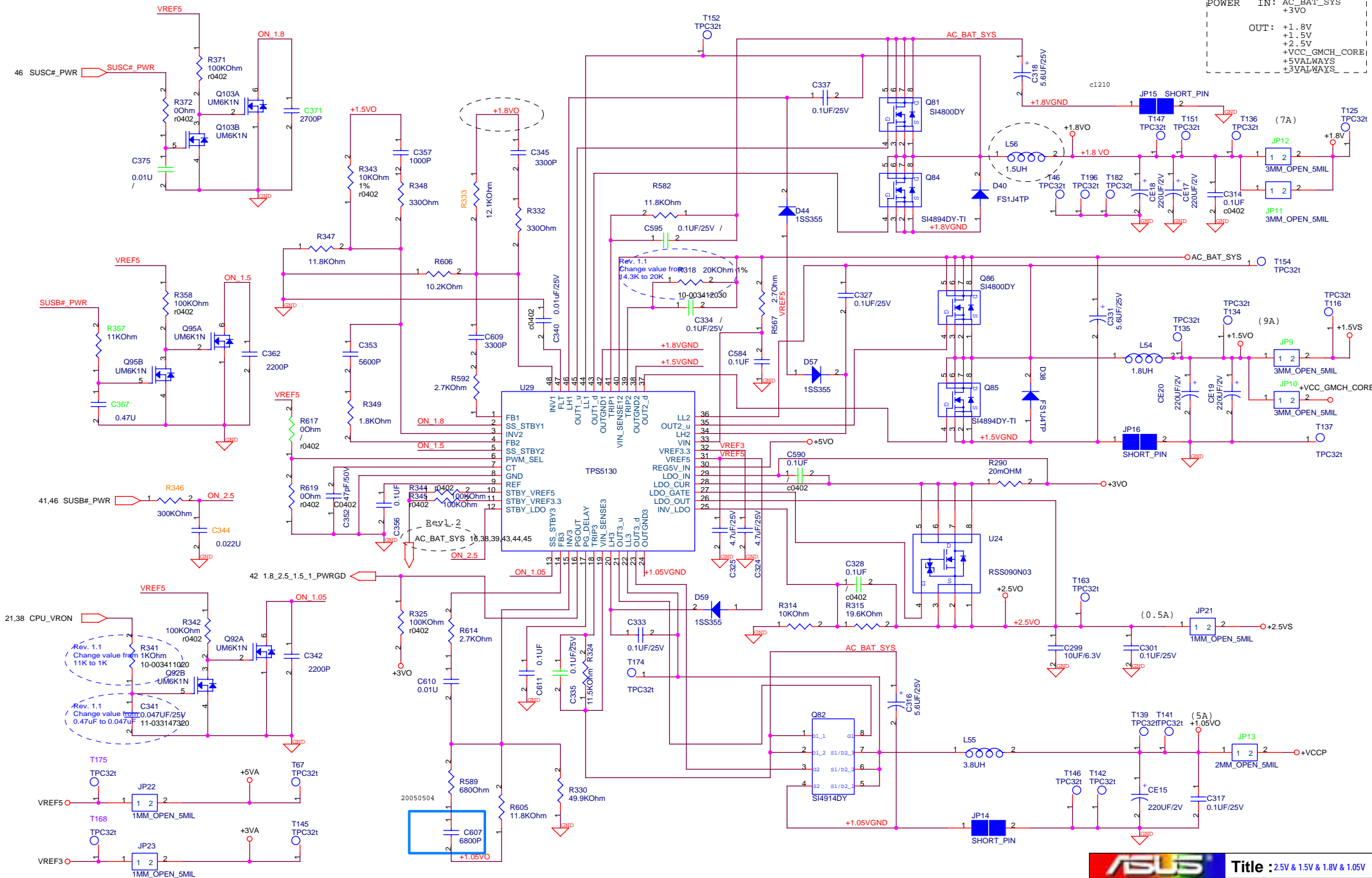








SIGNAL	IN:	SUSC#_PWR VSUS_ON
POWER	IN:	AC_BAT_SYS
	OUT:	+3VO +5VO



SIGNAL IN: SUSB#_PWR
 SUSC#_PWR
 POWER IN: AC_BAT_SYS
 +3VO
 OUT: +1.8V
 +1.5V
 +2.5V
 +VCC_GMCH_CORE
 +5VALWAYS
 +3VALWAYS

Rev. 1.1
 Change value for R318 20KOhm 1%
 14.3K to 20K

Rev. 1.1
 Change value from 1KOhm
 11K to 1K

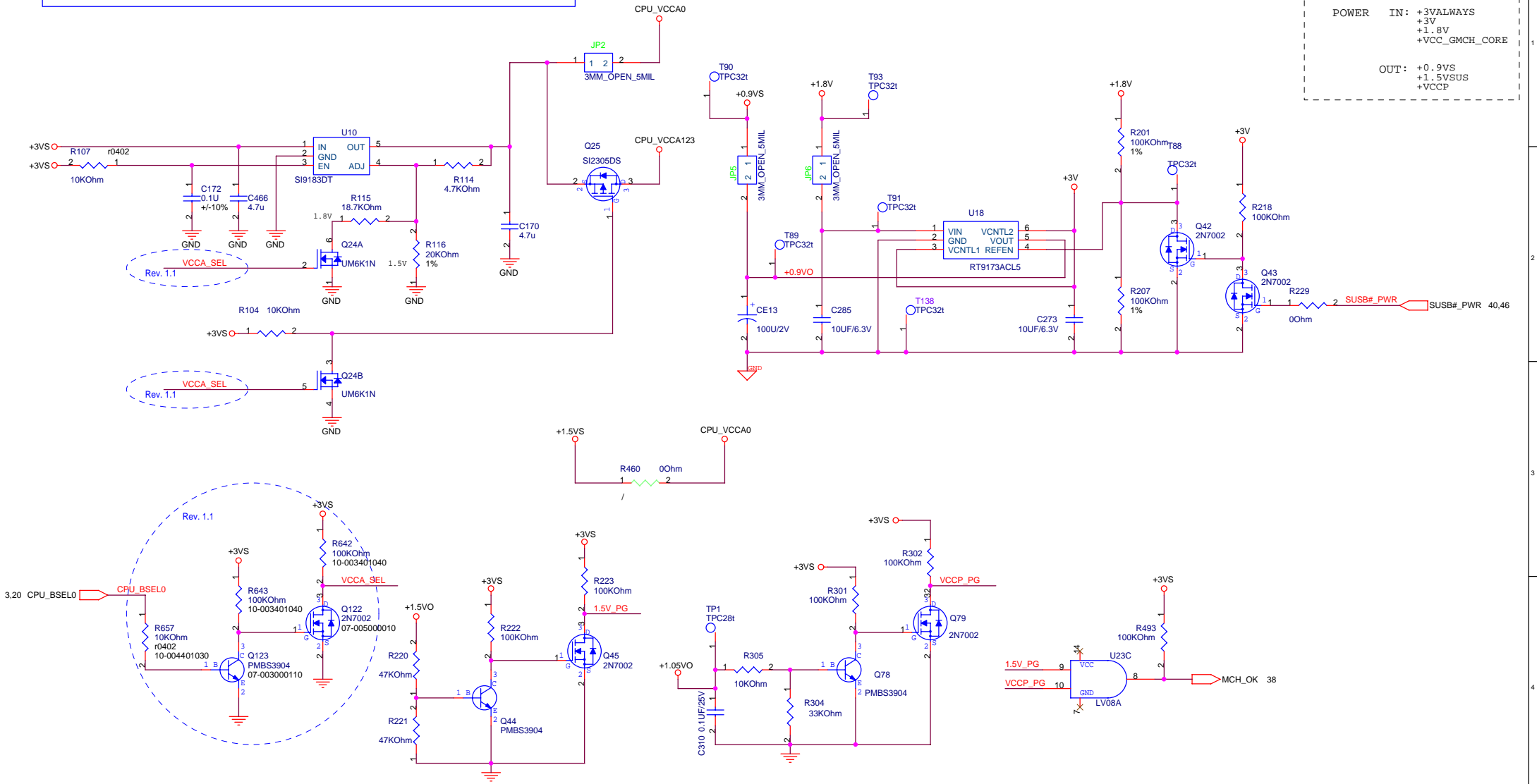
Rev. 1.1
 Change value from 0.047uF/25V
 0.47uF to 0.047uF

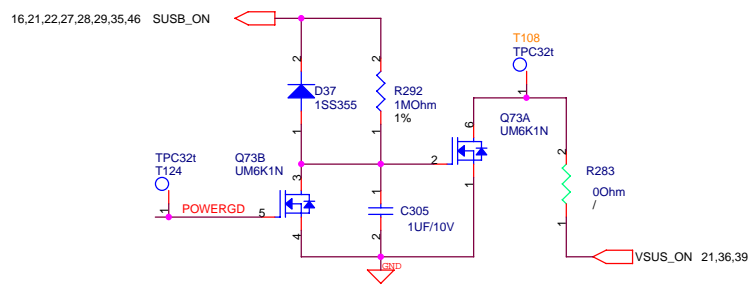
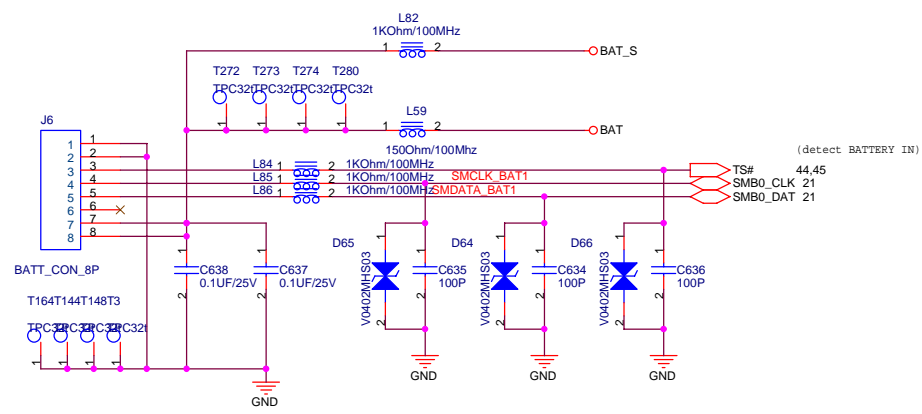
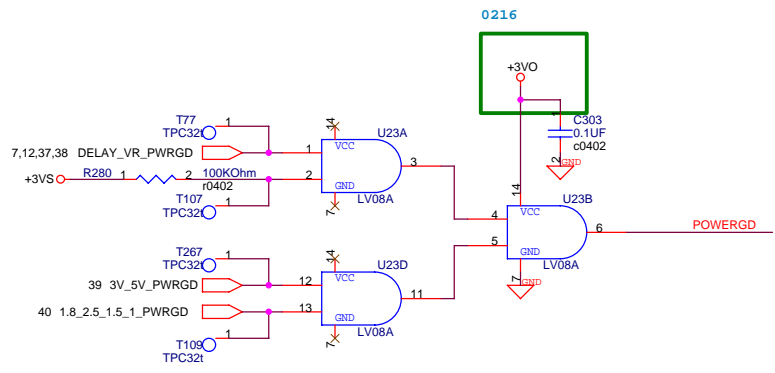
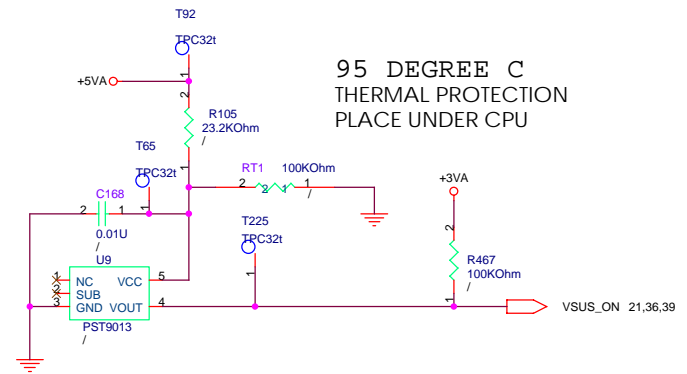
ASUS Title : 2.5V & 1.5V & 1.8V & 1.05V
 ASUSTek COMPUTER INC Engineer: Adams Lin

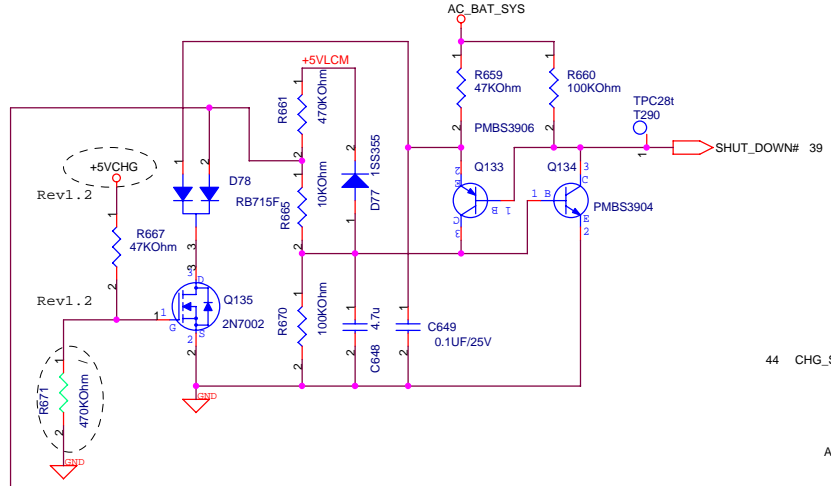
Size	Project Name	Rev
Custom	A3H	1.0
Date: Thursday, June 30, 2005		Sheet 40 of 54

For Duthon ,CPU_BSEL0 = LOW ,FSB=533MHZ ,VCCA0=1.5V ,VCCA123=0V
 For celeron ,CPU_BSEL0 = HIGH ,FSB=400MHZ ,VCCA0=1.8V ,VCCA123=1.8V

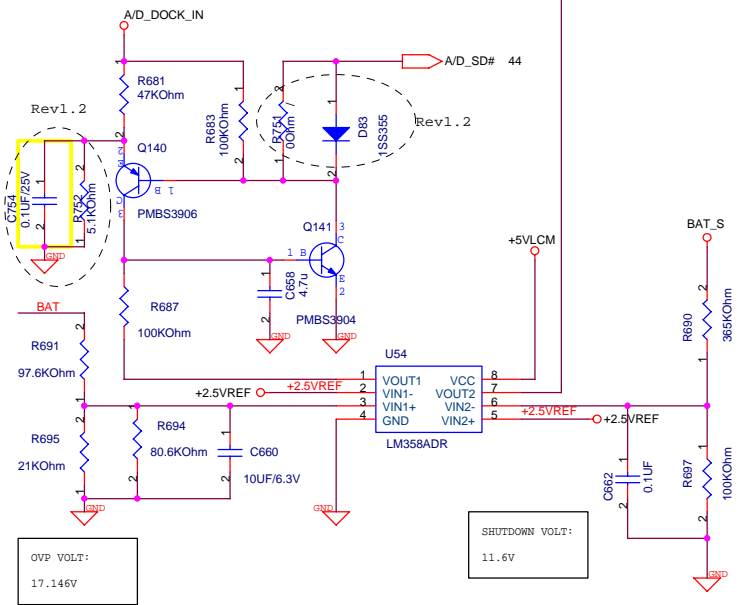
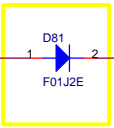
SIGNAL IN: USB#_PWR
 CPU_VRON
 POWER IN: +3VALWAYS
 +3V
 +1.8V
 +VCC_GMCH_CORE
 OUT: +0.9VS
 +1.5VSUS
 +VCCP





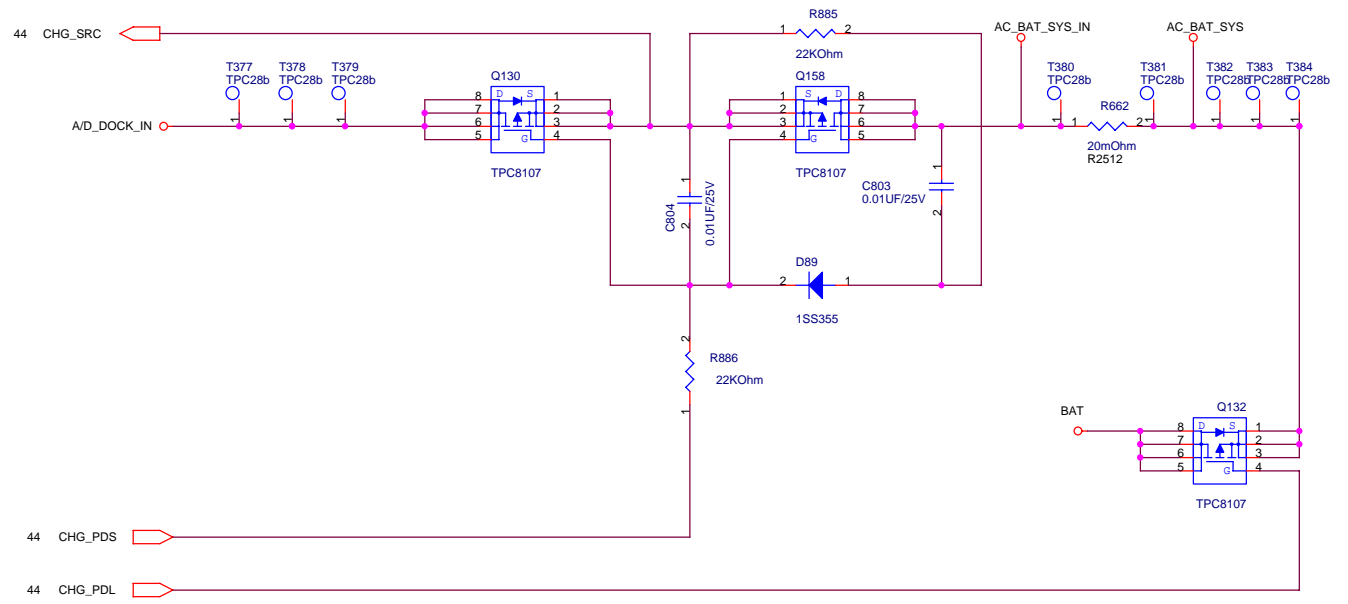


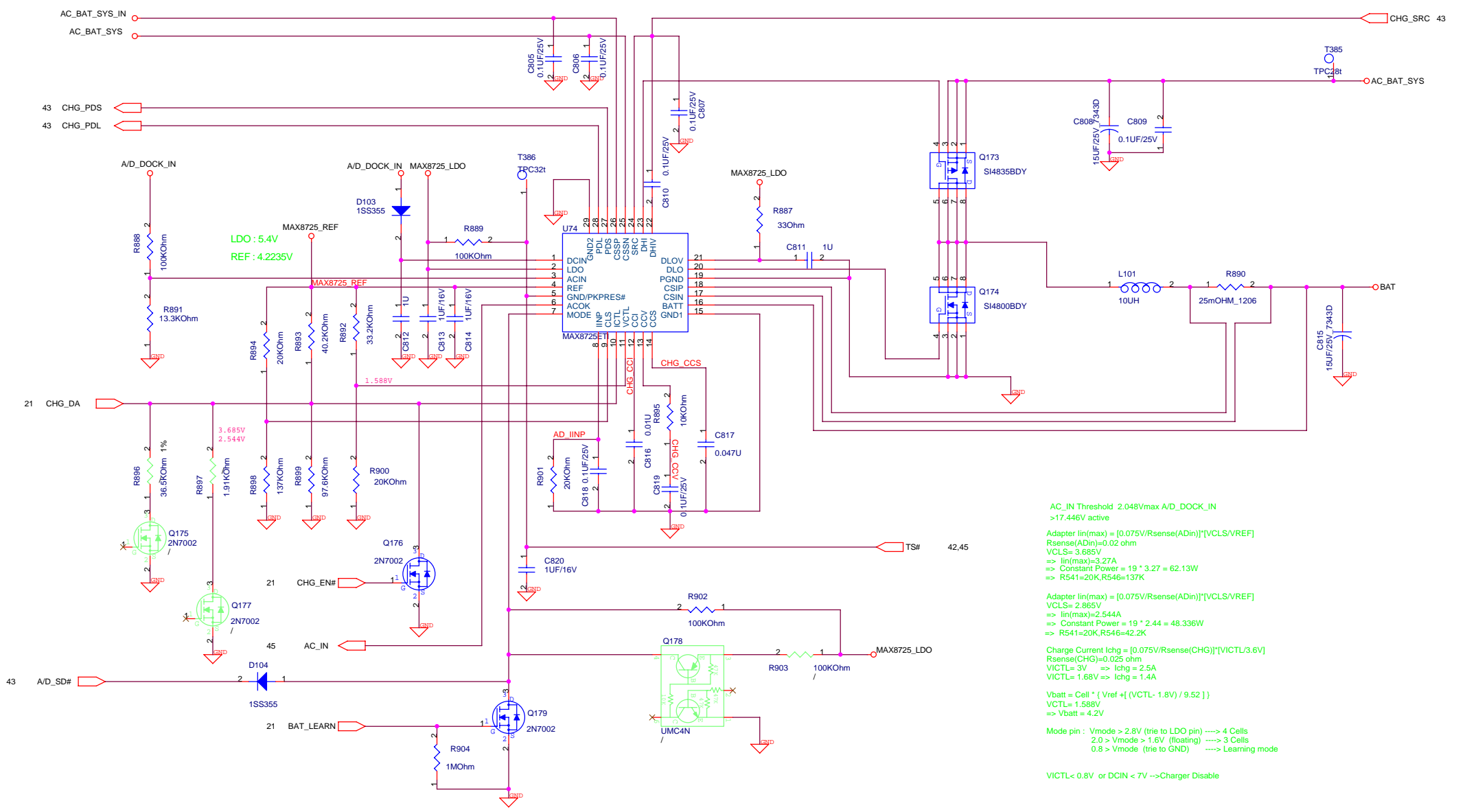
BATTERY SHUT_DOWN



OVP VOLT:
17.146V

SHUTDOWN VOLT:
11.6V





LDO : 5.4V
REF : 4.2235V

1.588V

3.685V
2.544V

AC_IN Threshold $2.048V_{max} A/D_DOCK_IN > 17.446V$ active
 Adapter $lin(max) = [0.075V/Rsense(Adin)] * [VCLS/VREF]$
 $Rsense(Adin) = 0.02\ ohm$
 $VCLS = 3.685V$
 $\Rightarrow lin(max) = 3.27A$
 $\Rightarrow Constant Power = 19 * 3.27 = 62.13W$
 $\Rightarrow R541 = 20K, R546 = 137K$

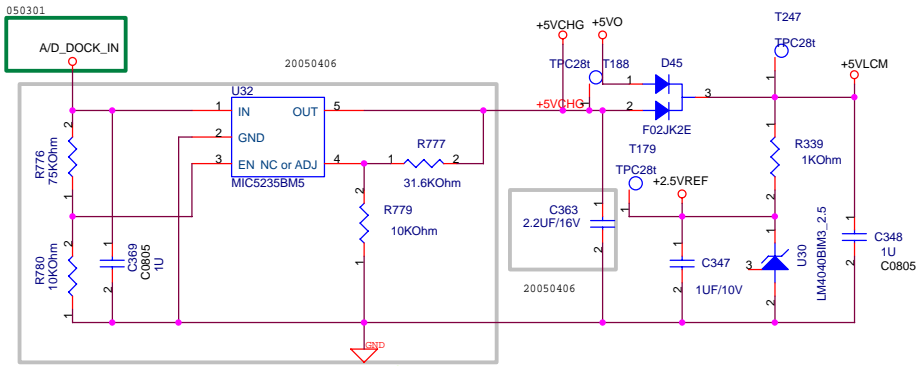
Adapter $lin(max) = [0.075V/Rsense(Adin)] * [VCLS/VREF]$
 $VCLS = 2.865V$
 $\Rightarrow lin(max) = 2.544A$
 $\Rightarrow Constant Power = 19 * 2.44 = 48.36W$
 $\Rightarrow R541 = 20K, R546 = 42.2K$

Charge Current $I_{chg} = [0.075V/Rsense(CHG)] * [VICTL/3.6V]$
 $Rsense(CHG) = 0.025\ ohm$
 $VICTL = 3V \Rightarrow I_{chg} = 2.5A$
 $VICTL = 1.68V \Rightarrow I_{chg} = 1.4A$

$V_{batt} = Cell * (Vref + [(VCTL - 1.8V) / 9.52])$
 $VCTL = 1.588V$
 $\Rightarrow V_{batt} = 4.2V$

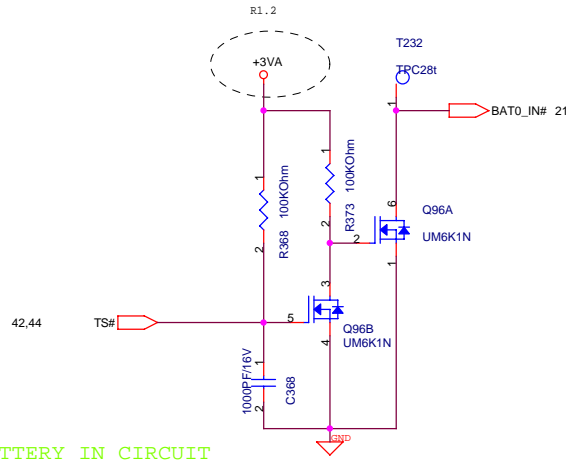
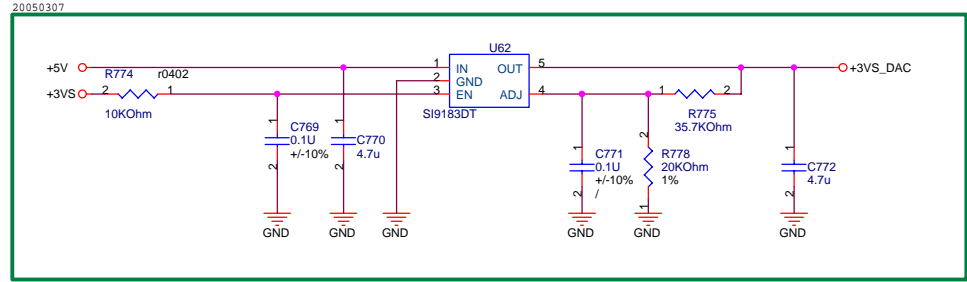
Mode pin : $V_{mode} > 2.8V$ (try to LDO pin) \rightarrow 4 Cells
 $2.0 > V_{mode} > 1.6V$ (floating) \rightarrow 3 Cells
 $0.8 > V_{mode}$ (try to GND) \rightarrow Learning mode

$VICTL < 0.8V$ or $DCIN < 7V \rightarrow$ Charger Disable

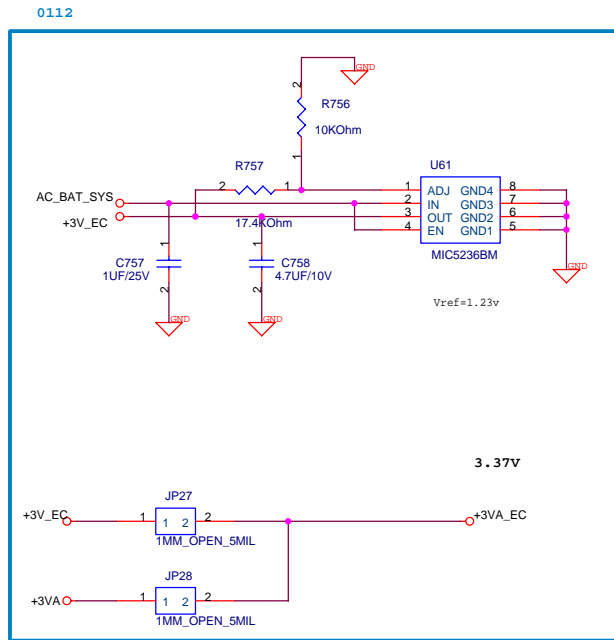


+5VCHG, +5VLCM, +2.5VREF

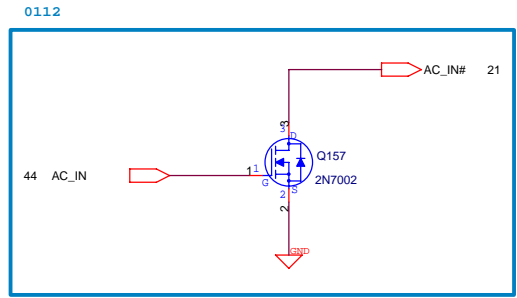
Ref: 1.24V
 ON: EN=2V (A/D_DOCK_IN=1.7V)
 OFF: EN=0.6V (A/D_DOCK_IN=5.1V)

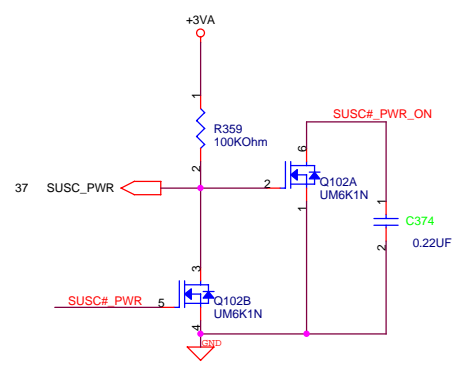
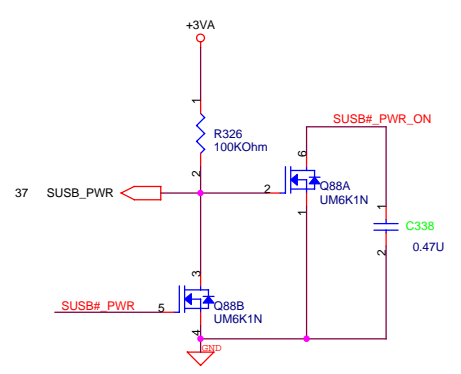
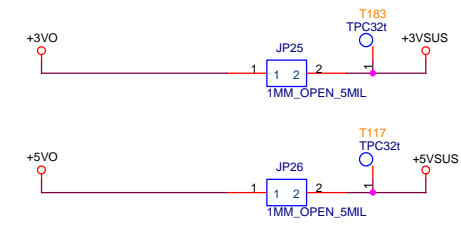
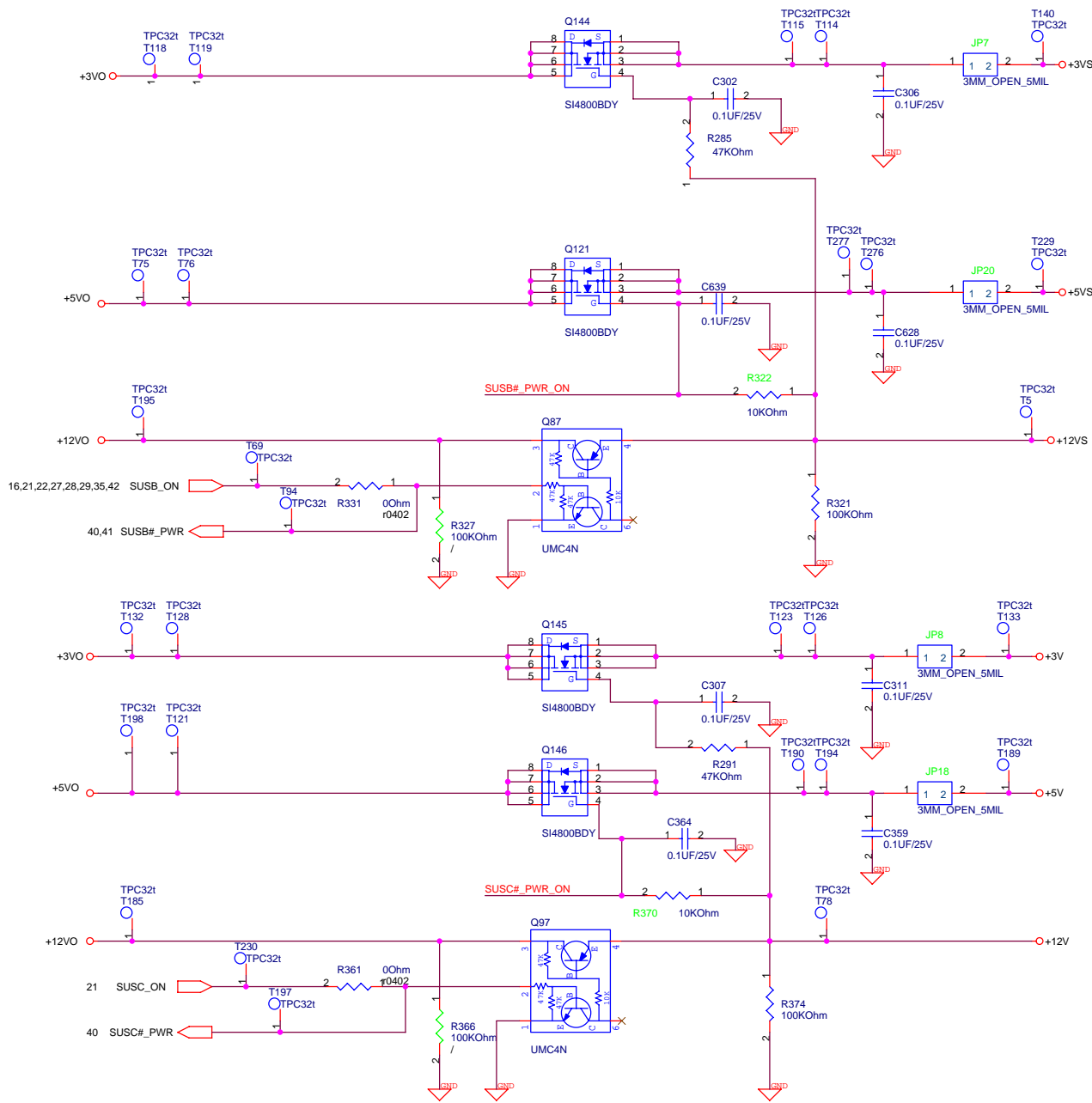


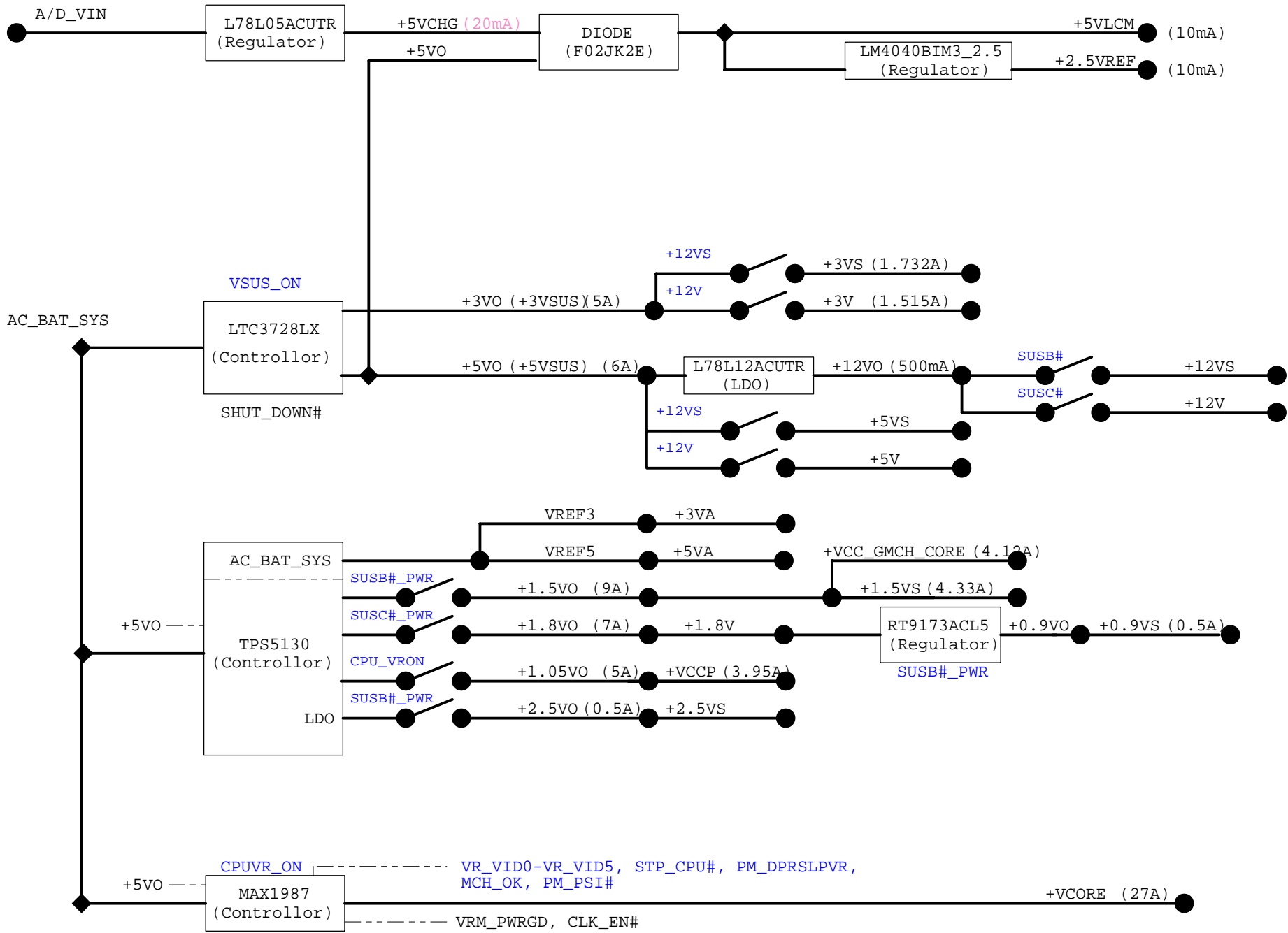
BATTERY IN CIRCUIT



3.37V







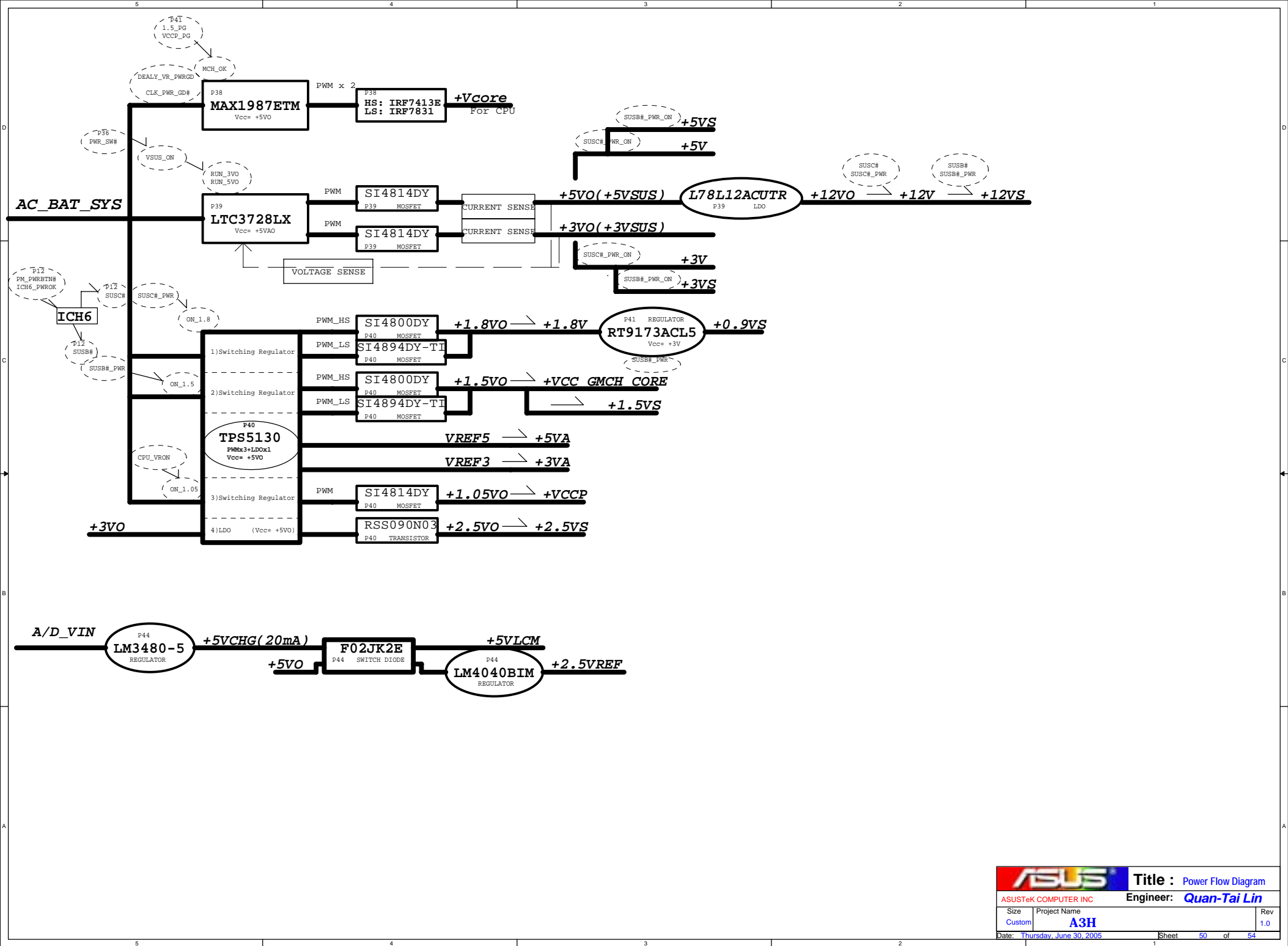
PCI Device	IDSEL#	REQ/GNT#	Interrupts
10/100 RTL8100CL	AD16	2	E
CARD READER	AD17	1	B
CARDBUS	AD17	1	C
1394	AD17	1	D
MINIPCI (802.11a/b/g)	AD19	3	G,H

SM-Bus Device	SM-Bus Address
Clock Generator	1101001x (D2)
SO-DIMM 0	1010000x (A0)
SO-DIMM 1	1010001x (A2)
Thermal Sensor	1001100x (98)

0221

ICH6-M GPIO	A5V	Note	Volt
GPI 0			+3VS
GPI 1			+3VS
GPI 2			+3VS
GPI 3			+3VS
GPI 4			+3VS
GPI 5			
GPI 7			+3VS
GPI 8	EXTSMI#		+3VSUS
GPI 11	LID_ICH#		+3VSUS
GPI 12	KB_SCI#		+3VSUS
GPI 13	SIO_SMI#		+3VSUS
GPI 14			+3VSUS
GPI 15			+3VSUS
GPO 16			
GPO 17			
GPO 19	PWRLED_1HZ		+3VS
GPO 21	BACK_OFF#		+3VS
GPO 23	FWH_WP#		+3VS
GPO 24	802_LED_EN#		+3VSUS
GPI 26	SATA_DET#0	Unused pull-up to Vcc3_3	+3VS
GPI 27			+3VSUS
GPI 28			+3VSUS
GPI 29	PCB_ID2	Default : 0	+3VS
GPI 30	PCB_ID0	Default : 0	+3VS
GPI 31	PCB_ID1	Default : 0	+3VS
GPI 33	CPUFAN_SPD_A		+3VS
GPO 34	WLAN_ON#		+3VS
GPI 40	PANEL_ID0		+3VS
GPI 41	PANEL_ID1		+3VS
GPO 48			
GPO 49			
GPI 25	CB_SD#	Diode	+3V

KBC GPIO	A5V	Note
P23(Pin 35)	CHG_FULL_OC	
P22(Pin 36)	BAT_LEARN	
P21(Pin 37)	KBC_P21	
P20(Pin 38)	KBCRSM	
P42(Pin 23)	WATCHDOG	
P43(Pin 22)	OP_SD#	POSTCode前拉Low,ACPI前拉High,ACPI後放掉
P44(Pin 21)	KB_CPURST	
P45(Pin 20)	KB_GATEA20	
P46(Pin 19)	KBCSCI	
P47(Pin 18)	PM_CLKRUN#	
P50(Pin 17)	BAT_LLOW#_OC	
P51(Pin 16)	KID1	
P52(Pin 15)	KID2	
P53(Pin 14)	CLR_DJ#	
P54(Pin 13)	BAT_SEL#	
P55(Pin 12)	BAT1_IN#_OC	
P56(Pin 11)	FAN_DA1	
P57(Pin 10)	ADJ_BL	
P67(Pin 74)	DJ_LED#	
P66(Pin 75)	SWDJ_EN#	
P65(Pin 76)	GAIN_AMP_K#	0->-6 V/V 1->NORMAL
P64(Pin 77)	ACIN_OC	
P63(Pin 78)	DISTP#	
P62(Pin 79)	MARATHON#	
P61(Pin 80)	INTERNET#	
P60(Pin 1)	EMAIL#	
P75(Pin 4)	KB_CLK	
P74(Pin 5)	MS_CLK	
P73(Pin 6)	TPAD_CLK	
P72(Pin 7)	KB_DAT	
P71(Pin 8)	MS_DAT	
P70(Pin 9)	TPAD_DAT	
P77(Pin 2)	SMC_BAT	
P76(Pin 3)	SMD_BAT	
P27(Pin 31)	SCROLL_LED#	
P26(Pin 32)	NUM_LED#	
P25(Pin 33)	CAP_LED#	
P24(Pin 34)	SET_PLTRSTNS#	
P40(Pin 27)	EXT_SMI	
P41(Pin 26)	EMAIL_LED#	

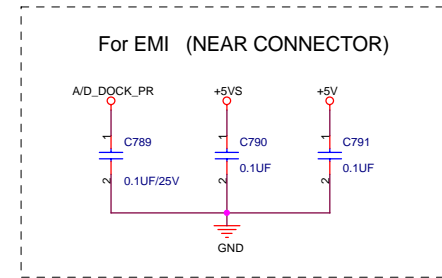
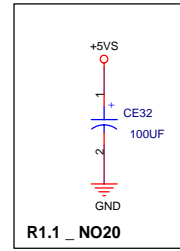
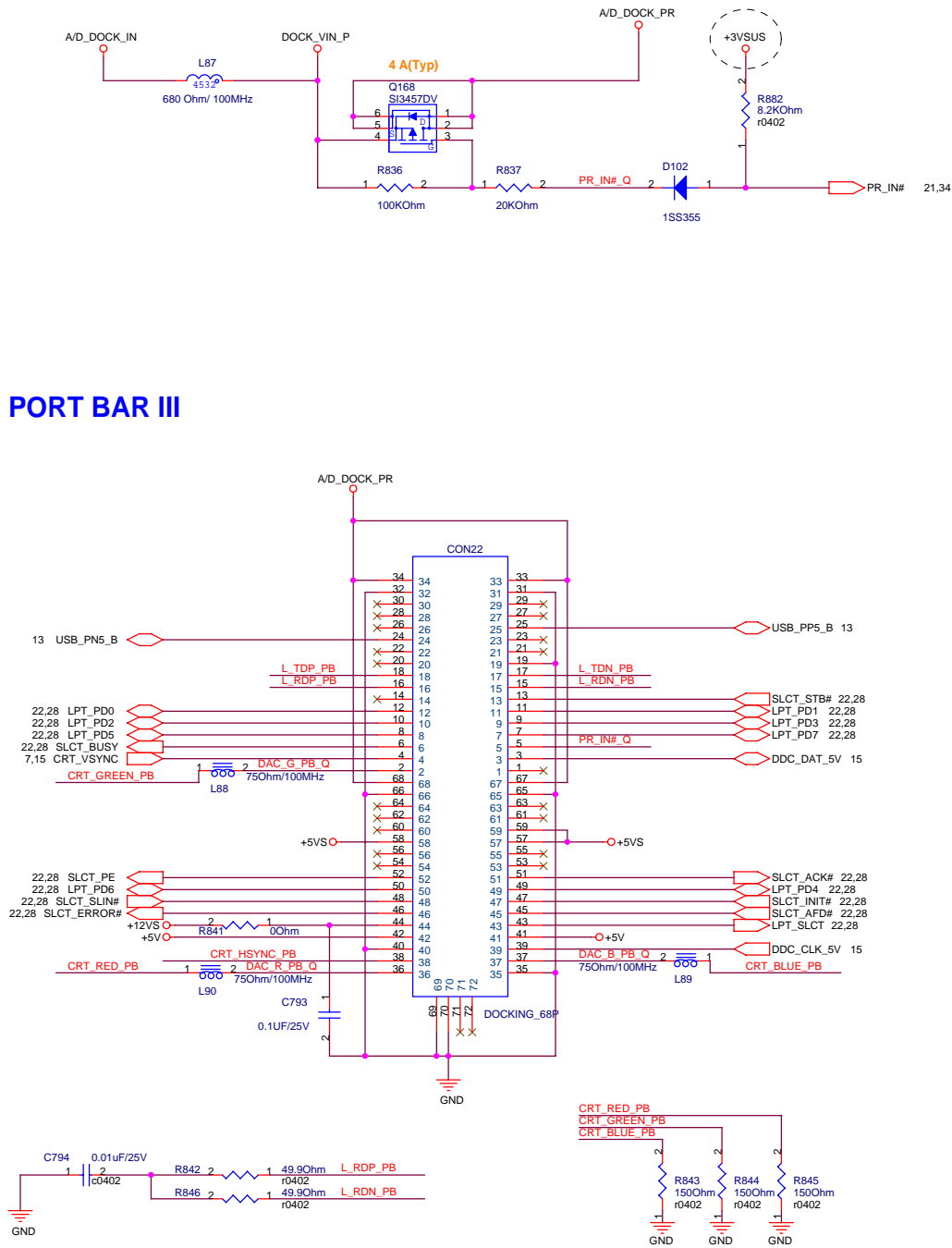


Rev.	Data	Description
1.0	04' 10/22	Initial release
1.1	04' 11/08	R193 not insert L63 not insert and mount L64 Q67 & Q69 not insert Modify CON4 pin assignment Mount R230 100K Ohm P/N 10-004401040 R94 & R95 not insert Modify Q71, Q77 & Q101 pin 5 & 6 signals C421 & C423 change value from 47pF to 27 pF P/N 11-034027042 C117 & C120 change value from 18pF to 24 pF P/N 11-033024000 R318 change value from 14.3 K to 20 K P/N 10-003412030
	04' 12/02	R141 not insert Delete R160 and add D72 and D73 (all not insert) R252 not insert and mount R247 Delete D33 and add D71 Net name "IDE_PDASP#2" change to "IDE_PDASP#" R504 change value from 100 K to 10 K P/N 10-003401030 Mount R412 Delete R166, Q32 and D20
	04' 12/06	Add R653 0 Ohm between U36-AD30 and "ICH6_PWROK" R47 & R53 not insert Mount R387 & R391 R41-1 change signal from "+3VS" to "+5VSUS" C192 change value from 0.1 uF to 0.22 uF P/N 11-033122400 R311 not insert and mount R310 CON5-18 change signal from "+5V" to "+5VSUS" Modify POWER & Audio DJ LED Circuit: Delete Q56 Add U52, Q125, Q126, Q128, D69, D70, D74, C645 & C646 Add R647, R648, R649, R650, R651, R652, R654 & R655 Delete Q32 & R166 and Q31-5 chang signal to "SUSC_PWR" Delete D20 D53-1 change signal from "PM_PWRBTN" to "PWR_SW_EN" Q408 not insert Modify Start-Up Circuit: Add D67, Q124, Q127, R644, R645 & C644 Add D68 & R646 but not insert R341 change value from 11 K to 1 K P/N 10-003411020 C341 change value from 0.47 uF to 0.047 uF P/N 11-033147320 Modify CPU_VCCA0 & CPU_VCCA123 Select Circuit: Add Q122, Q123, R642, R643 & R657 Q24-2 & Q24-5 change signal from "CPU_BSEL0" to "VCCA_SEL" R394 & R399 change value from 0 Ohm to 1K Ohm P/N 09-013103013
	04' 12/07	Add R656 & Q129 and U1 & U7 pin4 connect with "USB_EN#"
	04' 12/09	Delete D22 & signal "CODEC_SD#" connect with R135-2 Delete R136 & move C183 to conect with U13-5
	04' 12/13	Move R124 to conect with U13-5 & "DELAY_VR_PWRGD" Change value to 390K Ohm P/N 10-003403940 C183 change value to 0.22 uF P/N 11-033122400 CE27 & CE28 change package type to P/N 11-176247651 CE1 & CE22 change package type to P/N 11-17D210751 CN6 change package type to P/N 12-101100251

Rev.	Data	Description
1.1	04' 12/13	CON9 change package type to P/N 12-101102154 Mount R120 0 Ohm P/N 10-003400000 Mount L50 0 Ohm P/N 10-003400000 Mount C250 0.1uF P/N 11-034310410
	04' 12/15	R517 change value from 1K Ohm to 1M Ohm P/N 10-003401050 C499 change value from 0.1uF to 0.22uF P/N 11-033122400
	04'12/24	BAT holder P/N: 12-201110121, not temp_5182_rw50
1.2	04'12/27	RN8 ,RN9 ,RN10 ,RN11 ,RN14 P/N Change to 10-064805600 from 10-805600NV
	04'12/27	MDC P/N changes to 12-270101201,not temp_5182_rw49
	05'01/02	Add a diode D? to fix leakage current for power switch's LED (LED1)
	05'01/02	1) Modify the pin3 schematic of U52A (flipflop) 2) Add a resistance R? and a 2N7002 Q?
	05'01/02	1) Modify the pin11 schematic of U16B (flipflop) 2) Add a resistance R? and a UM6K1N Q127B
	05'01/03	ICH6 GPI(GPIO)41 pull high to +3VS with 8.2K ohm R? (P/N:10-004408220)
	05'01/03	LID_KBC# signal pull high to +3V,not +3VSUS
	05'01/03	LED[2..5] pull high to +5VS and change P/N to 07-015700246 as same as M7V
	05'01/03	Delete repeating limit resistance R269 100ohm
	05'01/05	R139 no mount and R109 value change to 1Mohm and P/N is 10-003401050
	05'01/05	R73,R75,R76,R77 change to 330ohm and P/N is 10-003413310
	05'01/05	H17,H18,H23,H24,H25 have to mount

Rev.	Date	Description
1.0	04' 10/22	Initial release
Rev1.2	05' 01/05	Add D? to connect RUN_3VO,RUN_5VO to SHUT_DOWN#
	05' 01/05	TPS5130 pin10.11 are with R344.R345 to connect to AC_BAT_SYS signal
	05' 01/05	R667.1 connect to +5VCHG R671 no mount C? 0.1UF no mount and add a R?47Kohm D83 no mount and add R? 0ohm R666 no mount R677 value change to 110Kohm R678 value change to 23.2Kohm R698 value change to 49.9Kohm R700 value change to 150Kohm Q137change to IRLML2402, add a R? 9.76Kohm, and R672.1 connect to AC_BAT_SYS U53.29 pull ground Add C? and C? 10UF Delete Q131 to change to D? U32.3 connect to A/D_VIN Change adapter in circuit
05' 06/22		

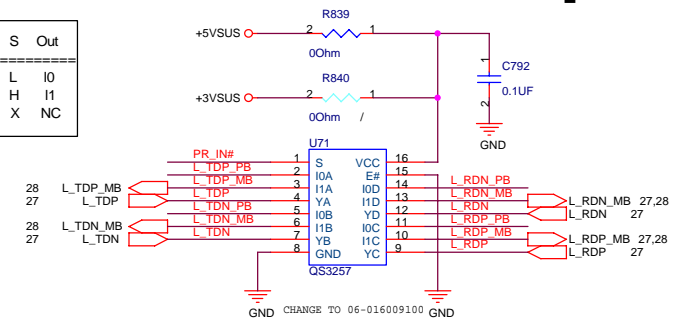
PORT BAR III



LAN Switch

Place near LAN chip!

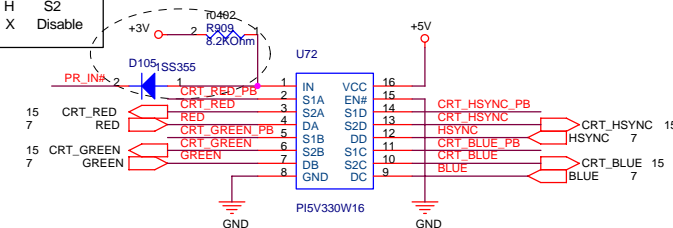
OE#	S	Out
L	L	I0
L	H	I1
H	X	NC



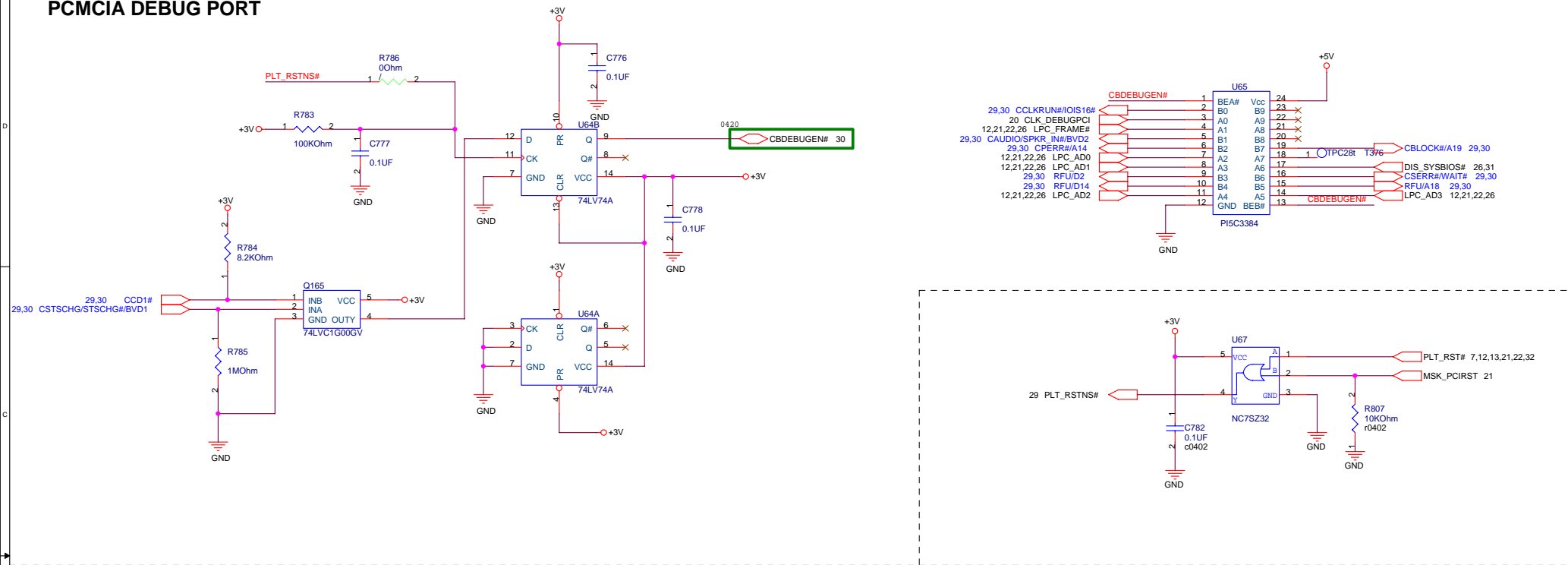
CRT Switch

Place near Alviso !

OE#	IN	Out
L	L	S1
L	H	S2
H	X	Disable



PCMCIA DEBUG PORT



Bluetooth

