

Power MOS Field-Effect Transistors

N-Channel Enhancement-Mode Power Field-Effect Transistors

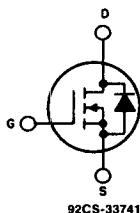
12A and 14A, 60V-100V

$r_{DS(on)}$ = 0.18 Ω and 0.25 Ω

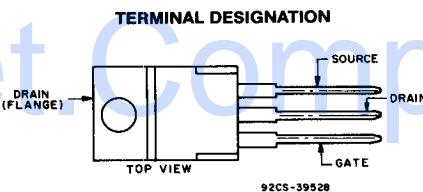
Features:

- SOA is power-dissipation limited
- Nanosecond switching speeds
- Linear transfer characteristics
- High input impedance
- Majority carrier device

N-CHANNEL ENHANCEMENT MODE



TERMINAL DIAGRAM



JEDEC TO-220AB

The IRF530, IRF531, IRF532 and IRF533 are n-channel enhancement-mode silicon-gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

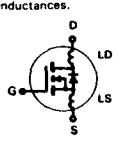
The IRF-types are supplied in the JEDEC TO-220AB plastic package.

Absolute Maximum Ratings

Parameter	IRF530	IRF531	IRF532	IRF533	Units
V_{DS} Drain - Source Voltage ①	100	60	100	60	V
V_{DGR} Drain - Gate Voltage ($R_{GS} = 20\text{ k}\Omega$) ①	100	60	100	60	V
$I_D @ T_C = 25^\circ\text{C}$ Continuous Drain Current	14	14	12	12	A
$I_D @ T_C = 100^\circ\text{C}$ Continuous Drain Current	9.0	9.0	8.0	8.0	A
I_{DM} Pulsed Drain Current ③	56	56	48	48	A
V_{GS} Gate - Source Voltage			± 20		V
$P_D @ T_C = 25^\circ\text{C}$ Max. Power Dissipation		75	(See Fig. 14)		W
Linear Operating Factor		0.6	(See Fig. 14)		W/ $^\circ\text{C}$
I_{LM} Inductive Current, Clamped	56	56	(See Fig. 15 and 16) L = 100 μH	48	A
T_J Operating Junction and Storage Temperature Range		-55 to 150			$^\circ\text{C}$
Lead Temperature	300 (0.063 in. (1.6mm) from case for 10s)				$^\circ\text{C}$

IRF530, IRF531, IRF532, IRF533

Electrical Characteristics @ $T_C = 25^\circ\text{C}$ (Unless Otherwise Specified)

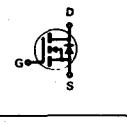
Parameter	Type	Min.	Typ.	Max.	Units	Test Conditions	
V_{DSS} Drain - Source Breakdown Voltage	IRF530 IRF532	100	—	—	V	$V_{GS} = 0\text{V}$	
	IRF531 IRF533	60	—	—	V	$I_D = 250\mu\text{A}$	
$V_{GS(\text{th})}$ Gate Threshold Voltage	ALL	2.0	—	4.0	V	$V_{DS} = V_{GS}, I_D = 250\mu\text{A}$	
I_{GSS} Gate-Source Leakage Forward	ALL	—	—	500	nA	$V_{GS} = 20\text{V}$	
I_{GSS} Gate-Source Leakage Reverse	ALL	—	—	500	nA	$V_{GS} = -20\text{V}$	
I_{DSS} Zero Gate Voltage Drain Current	ALL	—	—	250	μA	$V_{DS} = \text{Max. Rating}, V_{GS} = 0\text{V}$	
		—	—	1000	μA	$V_{DS} = \text{Max. Rating} \times 0.8, V_{GS} = 0\text{V}, T_C = 125^\circ\text{C}$	
$I_{D(on)}$ On-State Drain Current ②	IRF530 IRF531	14	—	—	A	$V_{DS} > I_{D(on)} \times R_{DS(on) \text{ max.}}, V_{GS} = 10\text{V}$	
	IRF532 IRF533	12	—	—	A		
$R_{DS(on)}$ Static Drain-Source On-State Resistance ②	IRF530 IRF531	—	0.14	0.18	Ω	$V_{GS} = 10\text{V}, I_D = 8.0\text{A}$	
	IRF532 IRF533	—	0.20	0.25	Ω		
g_{fs} Forward Transconductance ②	ALL	4.0	5.5	—	S (f)	$V_{DS} > I_{D(on)} \times R_{DS(on) \text{ max.}}, I_D = 8.0\text{A}$	
C_{iss} Input Capacitance	ALL	—	600	—	pF	$V_{GS} = 0\text{V}, V_{DS} = 25\text{V}, f = 1.0 \text{ MHz}$ See Fig. 10	
C_{oss} Output Capacitance	ALL	—	300	—	pF		
C_{rss} Reverse Transfer Capacitance	ALL	—	100	—	pF		
$t_{d(on)}$ Turn-On Delay Time	ALL	—	—	30	ns	$V_{DD} = 36\text{V}, I_D = 8.0\text{A}, Z_o = 15\Omega$	
t_r Rise Time	ALL	—	—	75	ns	See Fig. 17	
$t_{d(off)}$ Turn-Off Delay Time	ALL	—	—	40	ns	(MOSFET switching times are essentially independent of operating temperature.)	
t_f Fall Time	ALL	—	—	45	ns		
Q_g Total Gate Charge (Gate-Source Plus Gate-Drain)	ALL	—	18	30	nC	$V_{GS} = 10\text{V}, I_D = 18\text{A}, V_{DS} = 0.8 \text{ Max. Rating.}$ See Fig. 18 for test circuit. (Gate charge is essentially independent of operating temperature.)	
Q_{gs} Gate-Source Charge	ALL	—	9.0	14	nC		
Q_{gd} Gate-Drain ("Miller") Charge	ALL	—	9.0	14	nC		
L_D Internal Drain Inductance	ALL	—	3.5	—	nH	Measured from the contact screw on tab to center of die.	Modified MOSFET symbol showing the internal device inductances. 
		—	4.5	—	nH	Measured from the drain lead, 6mm (0.25 in.) from package to center of die.	
L_S Internal Source Inductance	ALL	—	7.5	—	nH	Measured from the source lead, 6mm (0.25 in.) from package to source bonding pad.	

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Thermal Resistance

R_{thJC} Junction-to-Case	ALL	—	—	1.67	$^\circ\text{C}/\text{W}$	
R_{thCS} Case-to-Sink	ALL	—	1.0	—	$^\circ\text{C}/\text{W}$	Mounting surface flat, smooth, and greased.
R_{thJA} Junction-to-Ambient	ALL	—	—	80	$^\circ\text{C}/\text{W}$	Free Air Operation

Source-Drain Diode Ratings and Characteristics

I_S Continuous Source Current (Body Diode)	IRF530 IRF531	—	—	14	A	Modified MOSFET symbol showing the integral reverse P-N junction rectifier. 
	IRF532 IRF533	—	—	12	A	
I_{SM} Pulse Source Current (Body Diode) ③	IRF530 IRF531	—	—	56	A	
	IRF532 IRF533	—	—	48	A	
V_{SD} Diode Forward Voltage ②	IRF530 IRF531	—	—	2.5	V	$T_C = 25^\circ\text{C}, I_S = 14\text{A}, V_{GS} = 0\text{V}$
	IRF532 IRF533	—	—	2.3	V	
t_{rr} Reverse Recovery Time	ALL	—	360	—	ns	$T_J = 150^\circ\text{C}, I_F = 14\text{A}, dI_F/dt = 100\text{A}/\mu\text{s}$
	ALL	—	2.1	—	μC	
Q_{RR} Reverse Recovered Charge	ALL	—	—	—	—	$T_J = 150^\circ\text{C}, I_F = 14\text{A}, dI_F/dt = 100\text{A}/\mu\text{s}$
t_{on} Forward Turn-on Time	ALL	—	—	—	—	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by $L_S + L_D$.

① $T_J = 25^\circ\text{C}$ to 150°C . ② Pulse Test: Pulse width $< 300\mu\text{s}$, Duty Cycle $< 2\%$.

③ Repetitive Rating: Pulse width limited

by max. junction temperature.

See Transient Thermal Impedance Curve (Fig. 5).

IRF530, IRF531, IRF532, IRF533

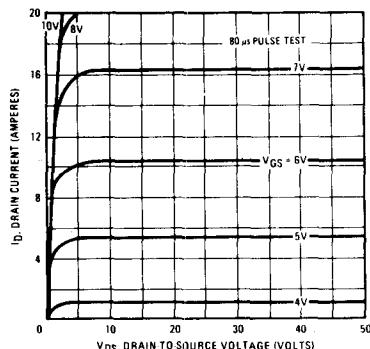


Fig. 1 – Typical Output Characteristics

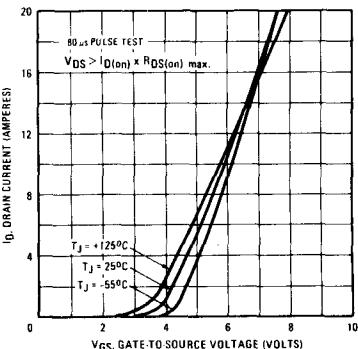


Fig. 2 – Typical Transfer Characteristics

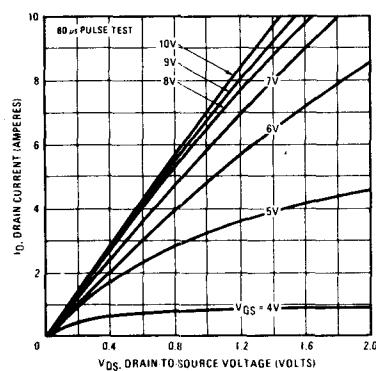


Fig. 3 – Typical Saturation Characteristics

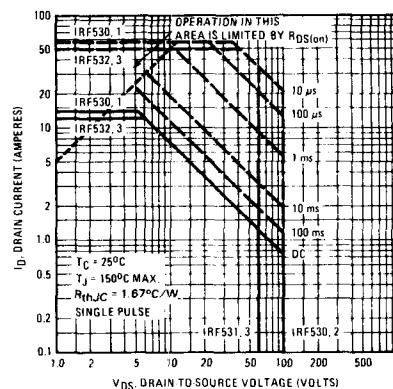


Fig. 4 – Maximum Safe Operating Area

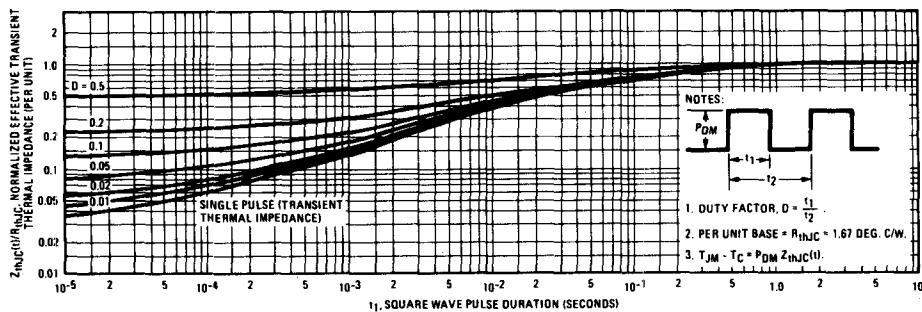


Fig. 5 – Maximum Effective Transient Thermal Impedance, Junction-to-Case Vs. Pulse Duration

IRF530, IRF531, IRF532, IRF533

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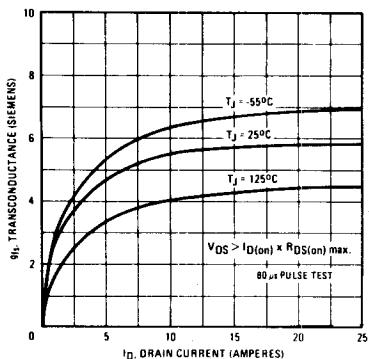


Fig. 6 – Typical Transconductance Vs. Drain Current

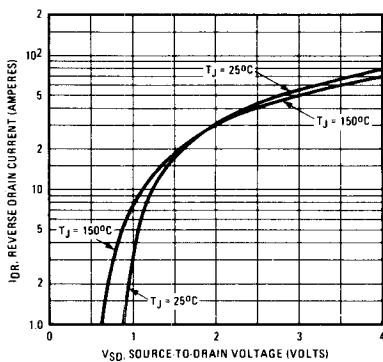


Fig. 7 – Typical Source-Drain Diode Forward Voltage

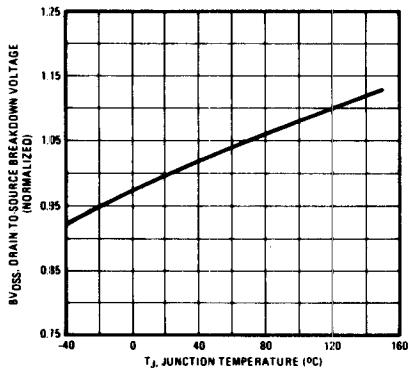


Fig. 8 – Breakdown Voltage Vs. Temperature

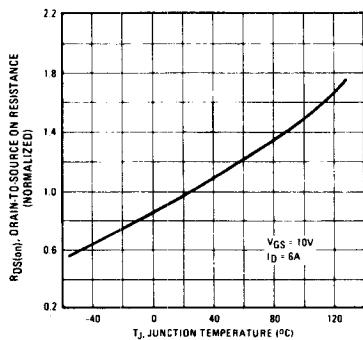


Fig. 9 – Normalized On-Resistance Vs. Temperature

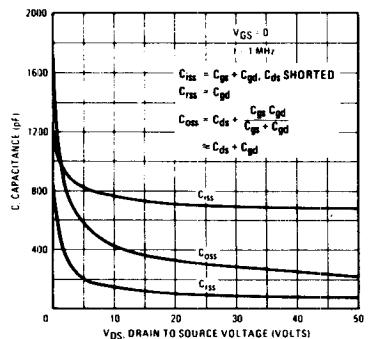


Fig. 10 – Typical Capacitance Vs. Drain-to-Source Voltage

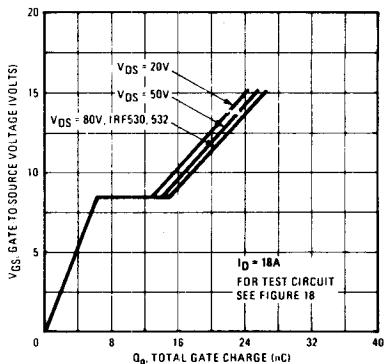


Fig. 11 – Typical Gate Charge Vs. Gate-to-Source Voltage

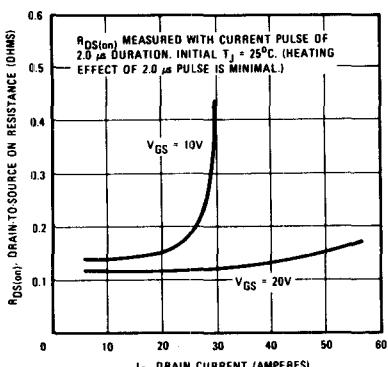
IRF530, IRF531, IRF532, IRF533

Fig. 12 – Typical On-Resistance Vs. Drain Current

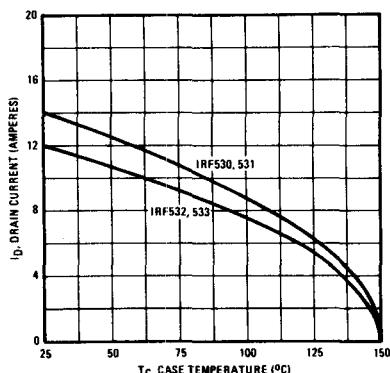


Fig. 13 – Maximum Drain Current Vs. Case Temperature

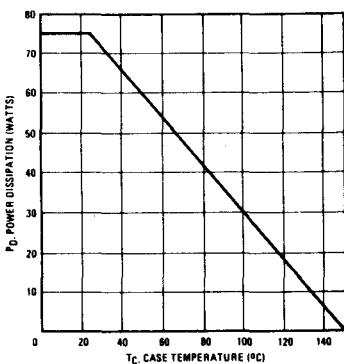


Fig. 14 – Power Vs. Temperature Derating Curve

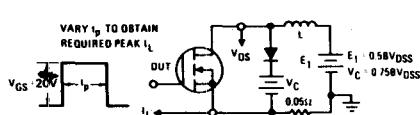


Fig. 15 – Clamped Inductive Test Circuit



Fig. 16 – Clamped Inductive Waveforms

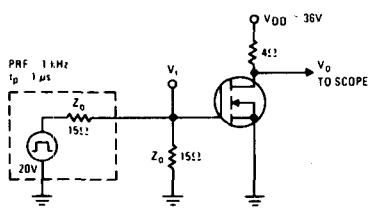


Fig. 17 – Switching Time Test Circuit

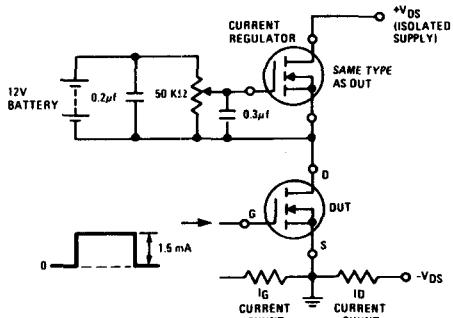


Fig. 18 – Gate Charge Test Circuit