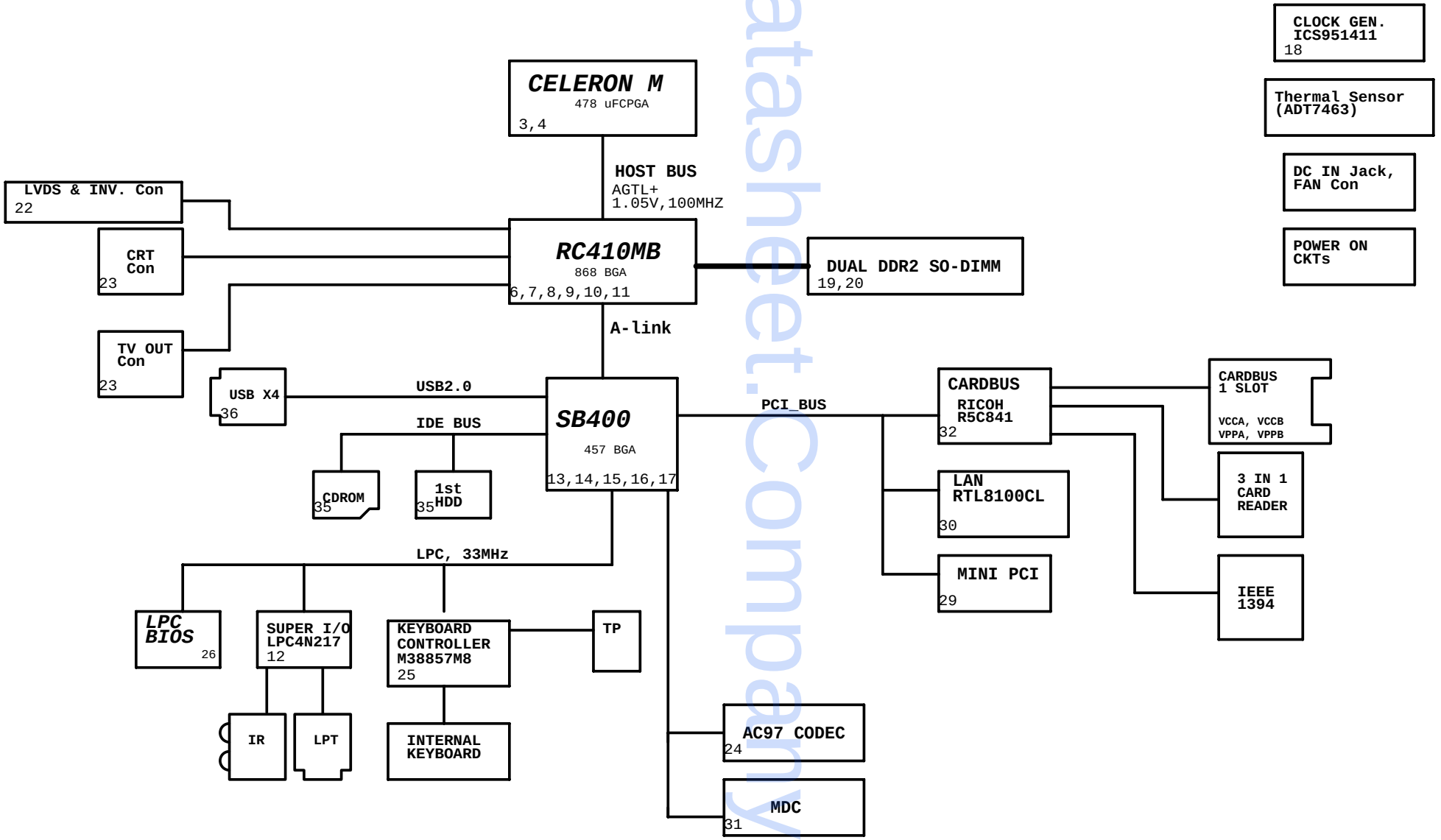
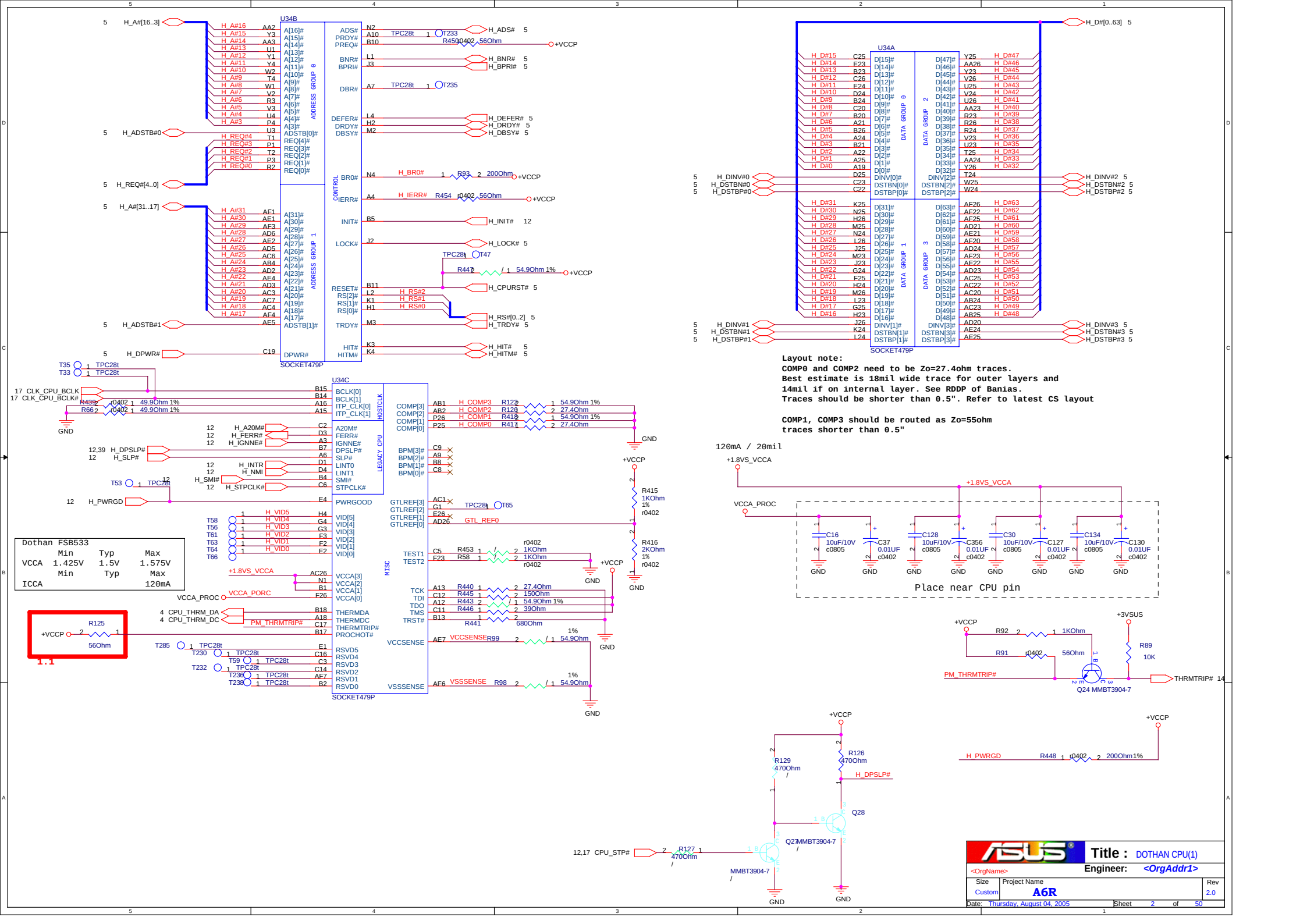
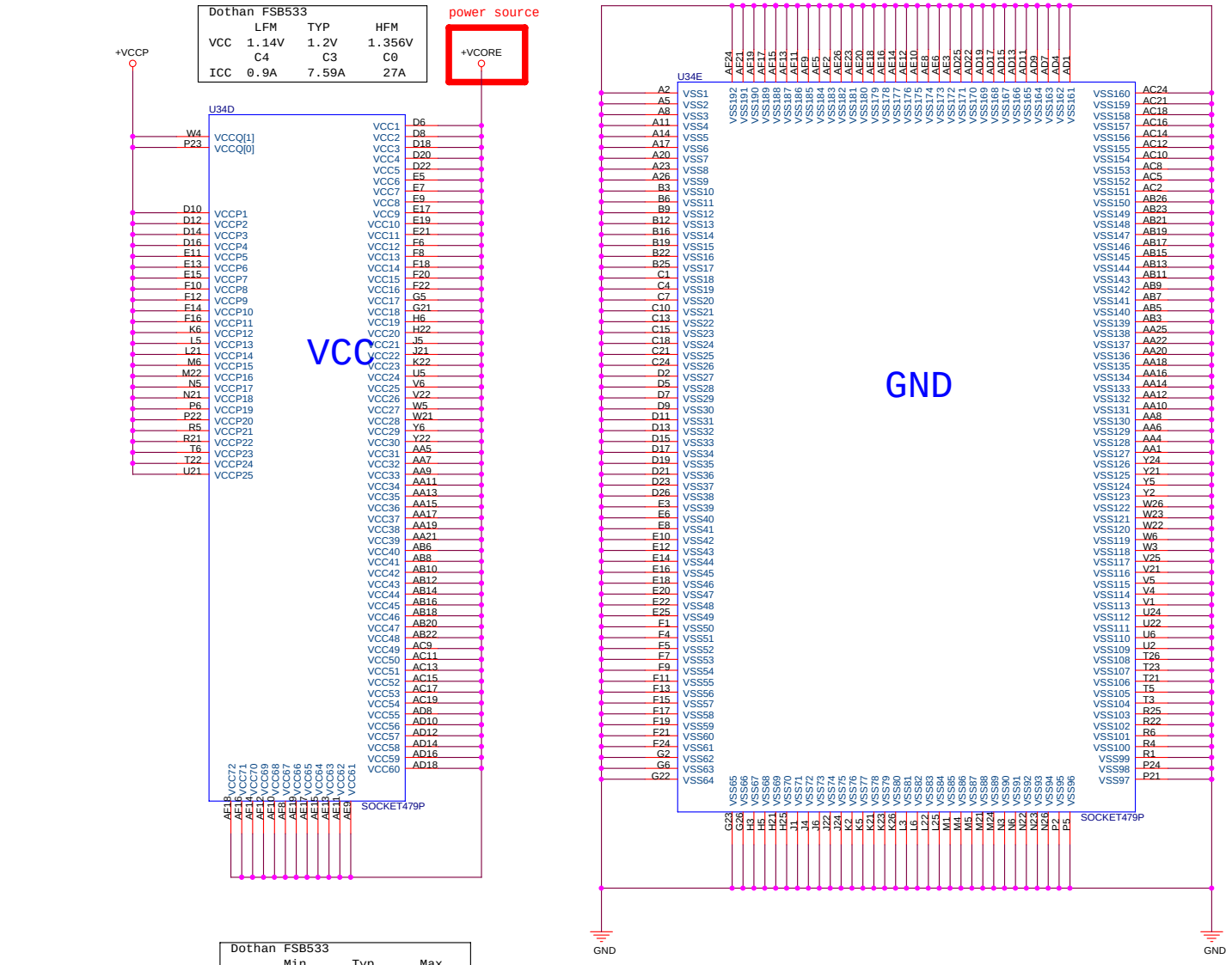
CELERON/RC410MB/IXP400 BLOCK DIAGRAM



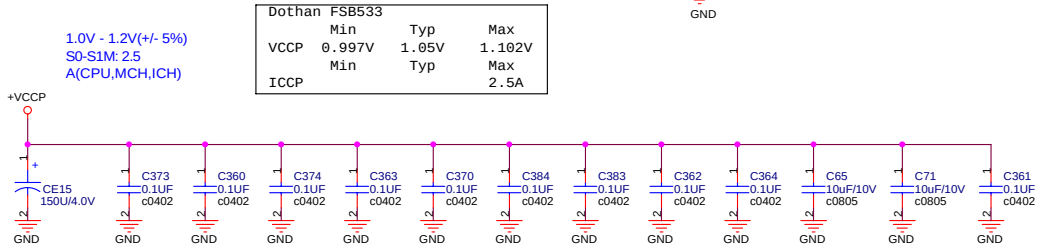
ASUS	Title : BLOCK DIAGRAM	
<OrgName>	Engineer: <OrgAddr1>	
Size: Custom	Project Name: A6R	Rev: 2.0
Date: Thursday, August 04, 2005	Sheet 1 of 50	


U34B
U34A
U34C
SOCKET479P
H_A#[16..3]
H_ADSTB#0
H_REQ#[4..0]
H_A#[31..17]
H_ADSTB#1
H_DPWR#
H_D#[0..63]
H_DINV#0
H_DSTBN#0
H_DSTBP#0
H_DINV#1
H_DSTBN#1
H_DSTBP#1
H_DINV#2
H_DSTBN#2
H_DSTBP#2
H_DINV#3
H_DSTBN#3
H_DSTBP#3
H_ADS#
H_BNR#
H_BPRI#
H_DEFER#
H_DRDY#
H_DBSY#
H_BR0#
H_IERR#
H_INIT#
H_LOCK#
H_CPURST#
H_RS#[0..2]
H_TRDY#
H_HIT#
H_HITM#
+VCCP
TPC28t
R450 56Ohm
R493 200Ohm
R454 56Ohm
R447 54.9Ohm 1%
ADDRESS GROUP 0
ADDRESS GROUP 1
DATA GROUP 0
DATA GROUP 1
DATA GROUP 2
DATA GROUP 3
CONTROL
Layout note:
COMP0 and COMP2 need to be Zo=27.4ohm traces.
Best estimate is 18mil wide trace for outer layers and
14mil if on internal layer. See RDDP of Banias.
Traces should be shorter than 0.5". Refer to latest CS layout
COMP1, COMP3 should be routed as Zo=55ohm
traces shorter than 0.5"
120mA / 20mil
+1.8VS_VCCA
VCCA_PROC
Place near CPU pin
C16 10uF/10V c0805
C37 0.01UF c0402
C128 10uF/10V c0805
C356 0.01UF c0402
C30 10uF/10V c0805
C127 0.01UF c0402
C134 10uF/10V c0805
C130 0.01UF c0402
Dothan FSB533
Min Typ Max
VCCA 1.425V 1.5V 1.575V
Min Typ Max
ICCA 120mA
R125 56Ohm
1.1
R415 1KOhm 1% r0402
R416 2KOhm 1% r0402
R453 1KOhm
R58 1KOhm
R440 27.4Ohm
R445 150Ohm
R443 54.9Ohm 1%
R446 39Ohm
R441 680Ohm
R99 54.9Ohm 1%
R98 54.9Ohm 1%
GTL_REF0
+3VSUS
R92 1KOhm
R91 56Ohm
R89 10K
Q24 MMBT3904-7
THRMTRIP# 14
R129 470Ohm
R126 470Ohm
Q28
Q27 MMBT3904-7
MMBT3904-7
12,17 CPU_STP#
R127 470Ohm
H_PWRGD
R448 200Ohm 1%
Title : DOTHAN CPU(1)
Engineer: <OrgAddr1>
<OrgName>
Size Custom
Project Name A6R
Rev 2.0
Date: Thursday, August 04, 2005
Sheet 2 of 50



MOBILE DOTHAN VID TABLE

VID[5..0]	Voltage	VID[5..0]	Voltage
000000	1.708V	100000	1.196V
000001	1.692V	100001	1.180V
000010	1.676V	100010	1.164V
000011	1.660V	100011	1.148V
000100	1.644V	100100	1.132V
000101	1.628V	100101	1.116V
000110	1.612V	100110	1.100V
000111	1.596V	100111	1.084V
001000	1.580V	101000	1.068V
001001	1.564V	101001	1.052V
001010	1.548V	101010	1.036V
001011	1.532V	101011	1.020V
001100	1.516V	101100	1.004V
001101	1.500V	101101	0.988V
001110	1.484V	101110	0.972V
001111	1.468V	101111	0.956V
010000	1.452V	110000	0.940V
010001	1.436V	110001	0.924V
010010	1.420V	110010	0.908V
010011	1.404V	110011	0.892V
010100	1.388V	110100	0.876V
010101	1.372V	110101	0.860V
010110	1.356V	110110	0.844V
010111	1.340V	110111	0.828V
011000	1.324V	111000	0.812V
011001	1.308V	111001	0.796V
011010	1.292V	111010	0.780V
011011	1.276V	111011	0.764V
011100	1.260V	111100	0.748V
011101	1.244V	111101	0.732V
011110	1.228V	111110	0.716V
011111	1.212V	111111	0.700V

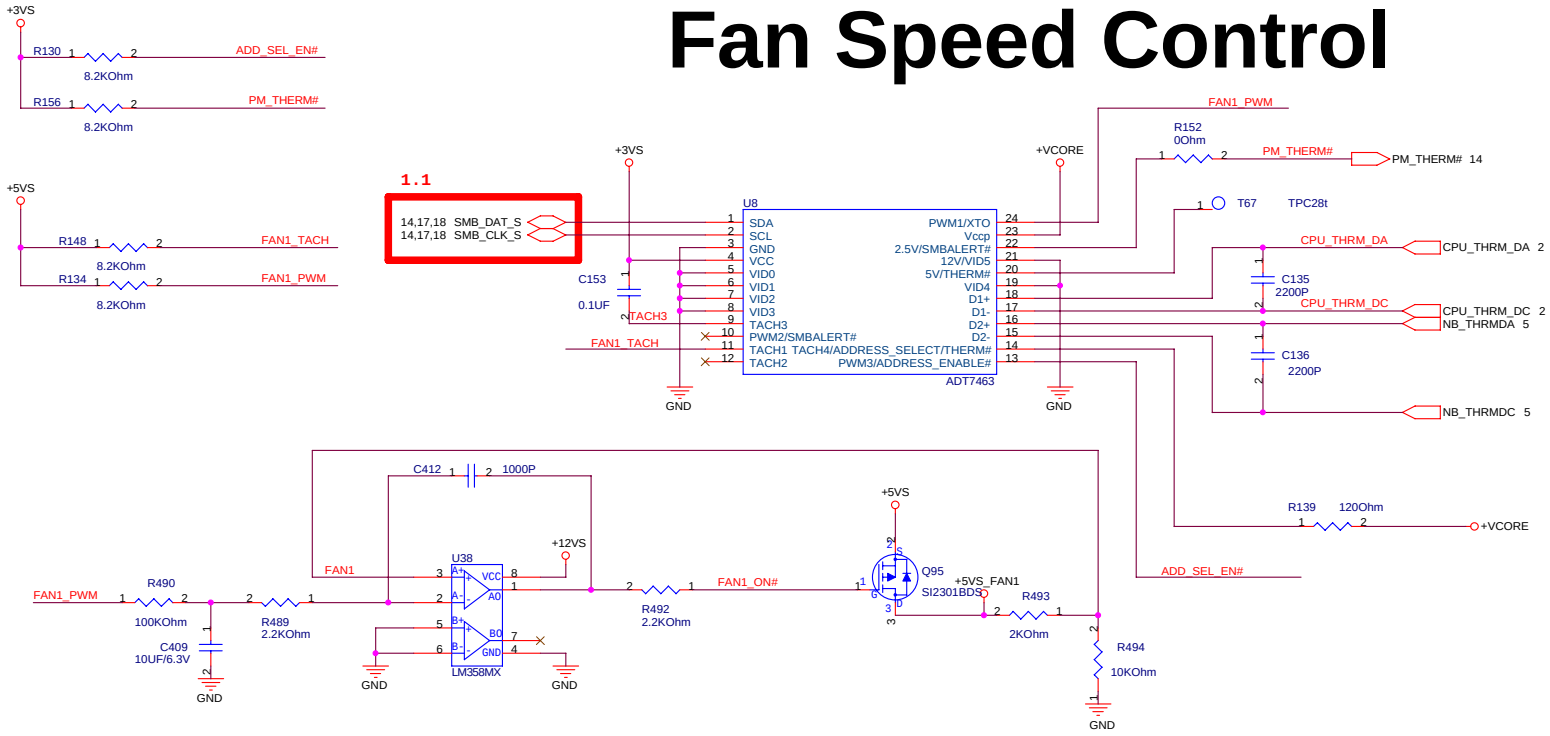


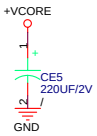
+VCCP (CPU) Decoupling Capacitor
(Place near CPU)

ASUS	Title : DOTHAN CPU(2)	
<OrgName>	Engineer: <OrgAddr1>	
Size: Custom	Project Name: A6R	Rev: 2.0
Date: Thursday, August 04, 2005	Sheet 3 of 50	

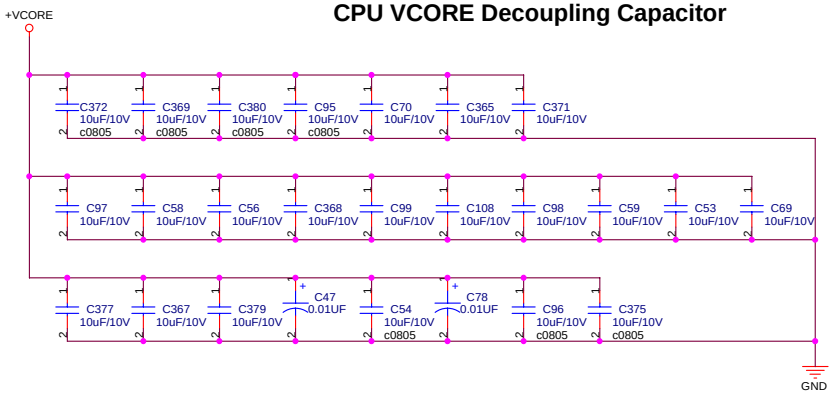
Fan Speed Control

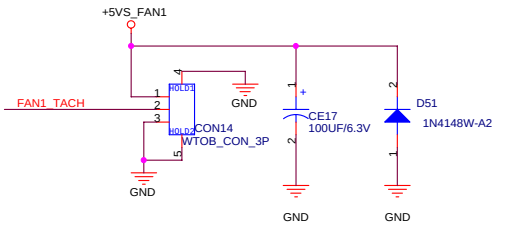
Pin 13	Pin 14	SMB Addr
1	X	5C **
0	1	5A
0	0	58



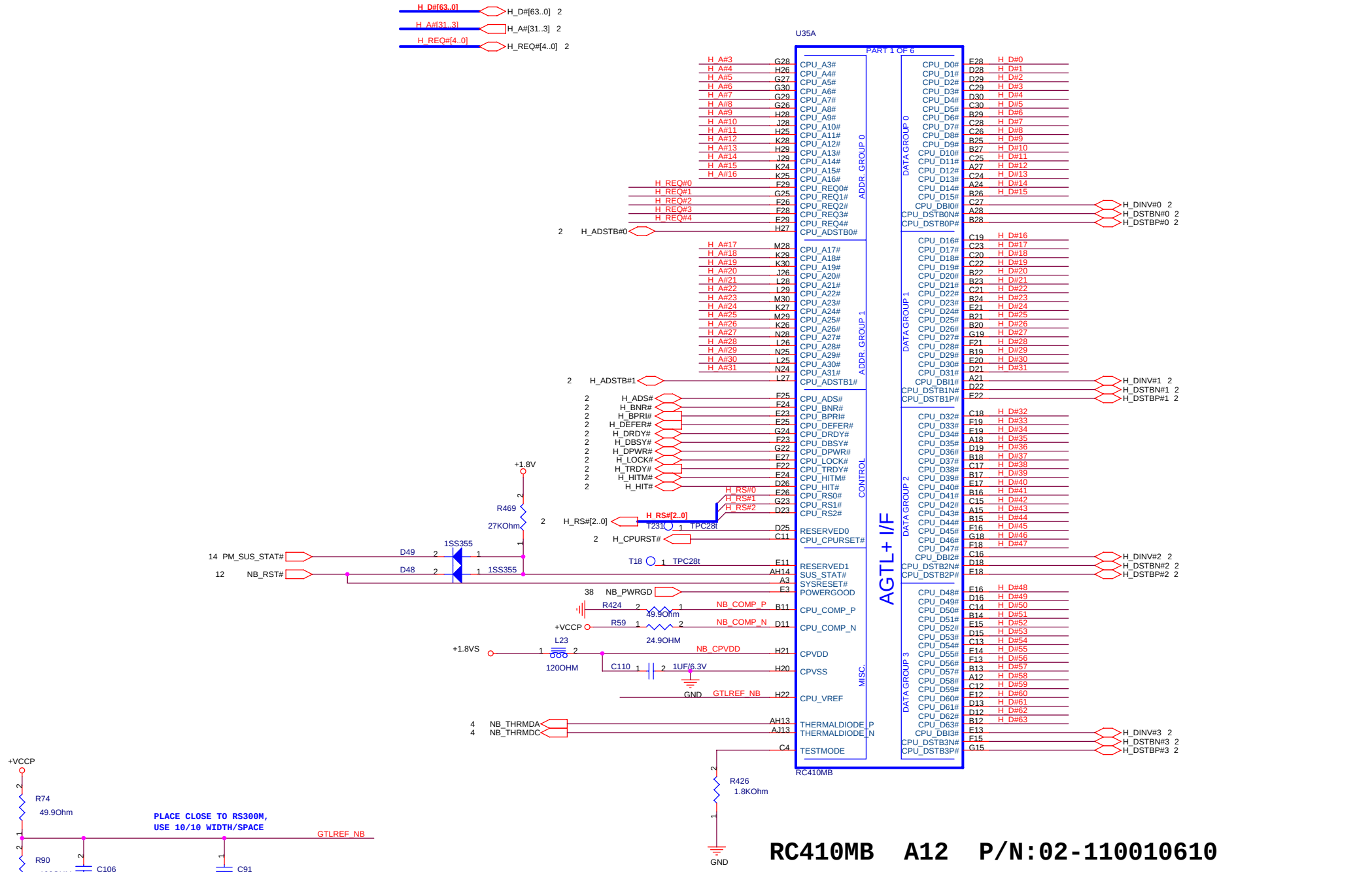


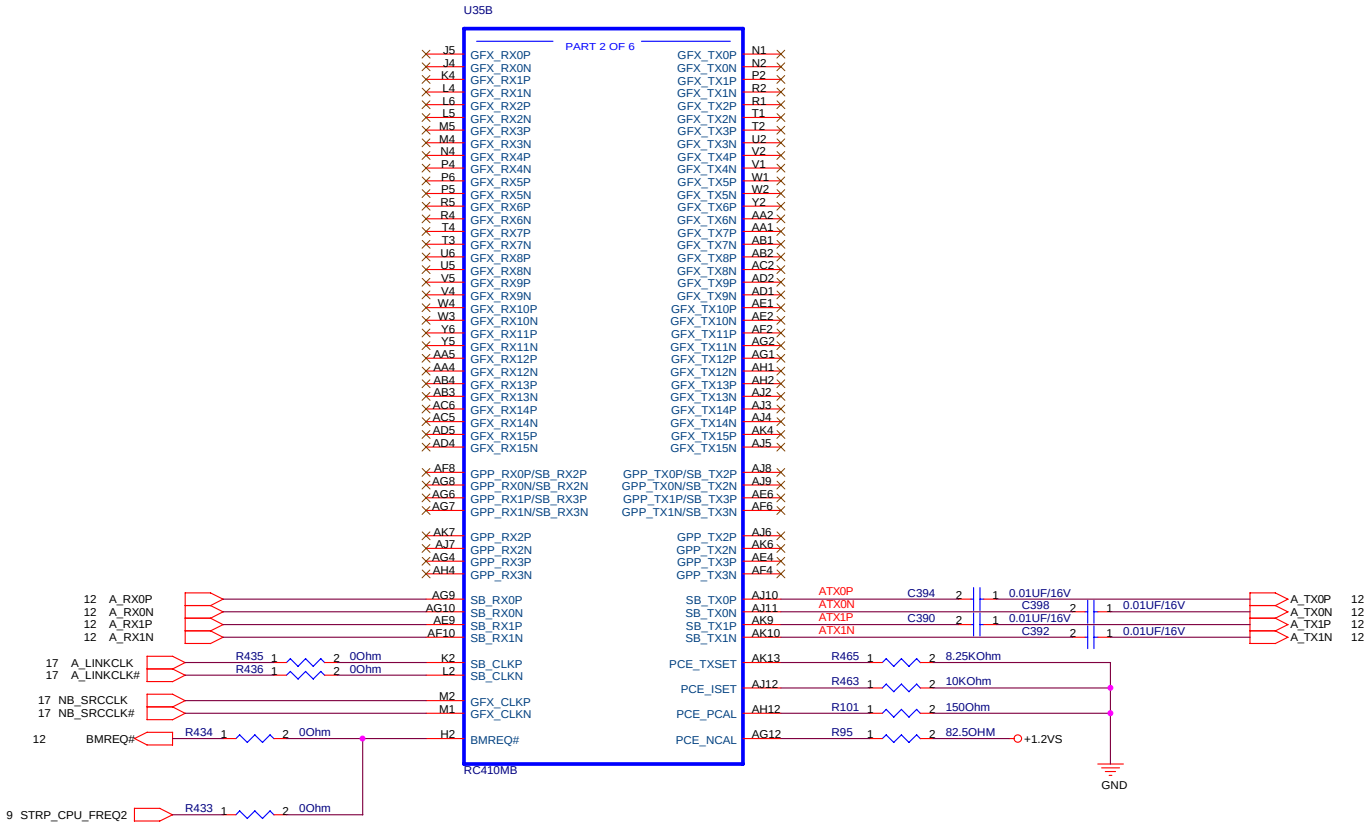
CPU VCORE Decoupling Capacitor



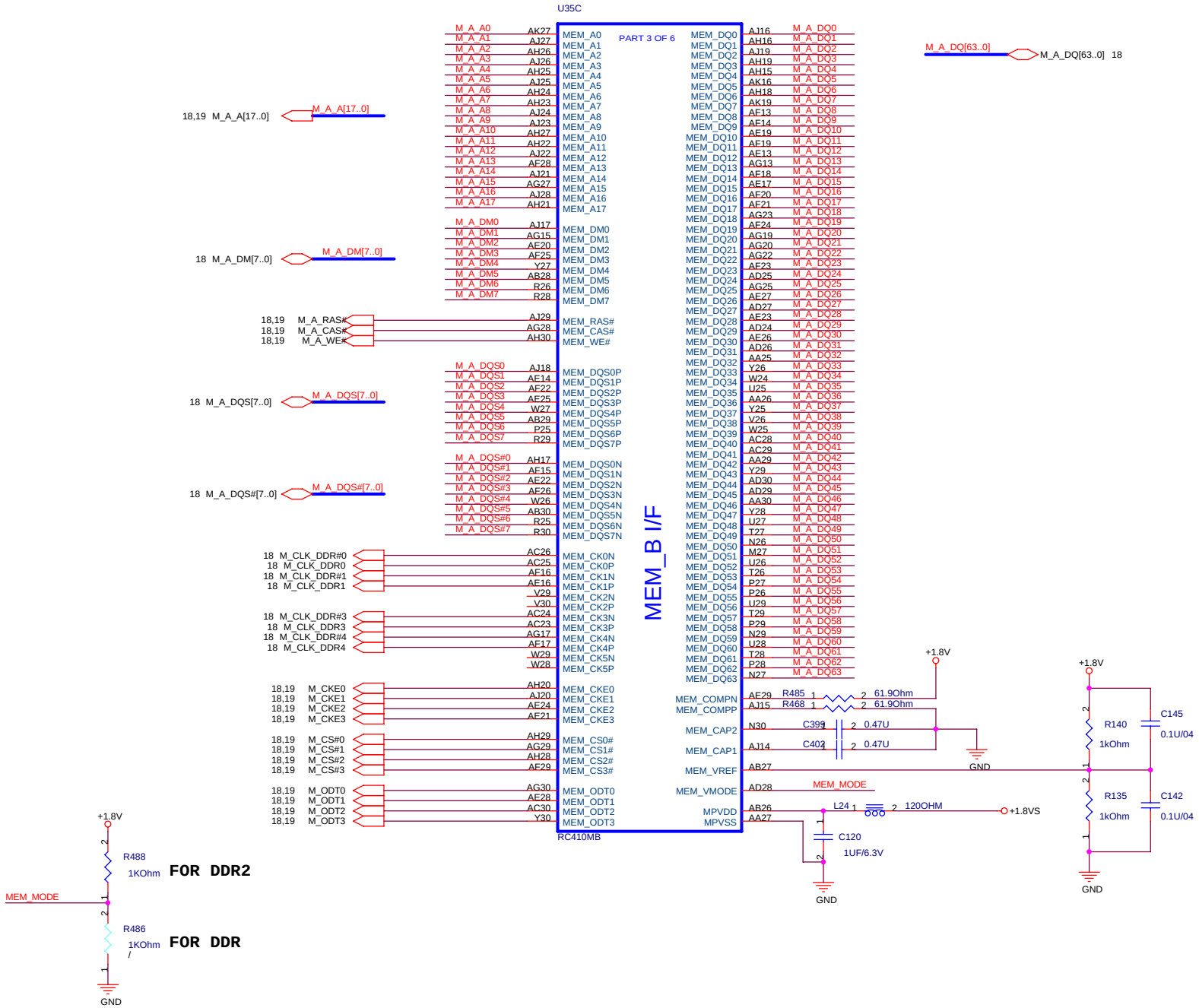


ASUS	Title : THERMAL SERSOR,FAN	
<OrgName>	Engineer: <OrgAddr1>	
Size: Custom	Project Name: A6R	Rev: 2.0
Date: Thursday, August 04, 2005	Sheet 4 of 50	

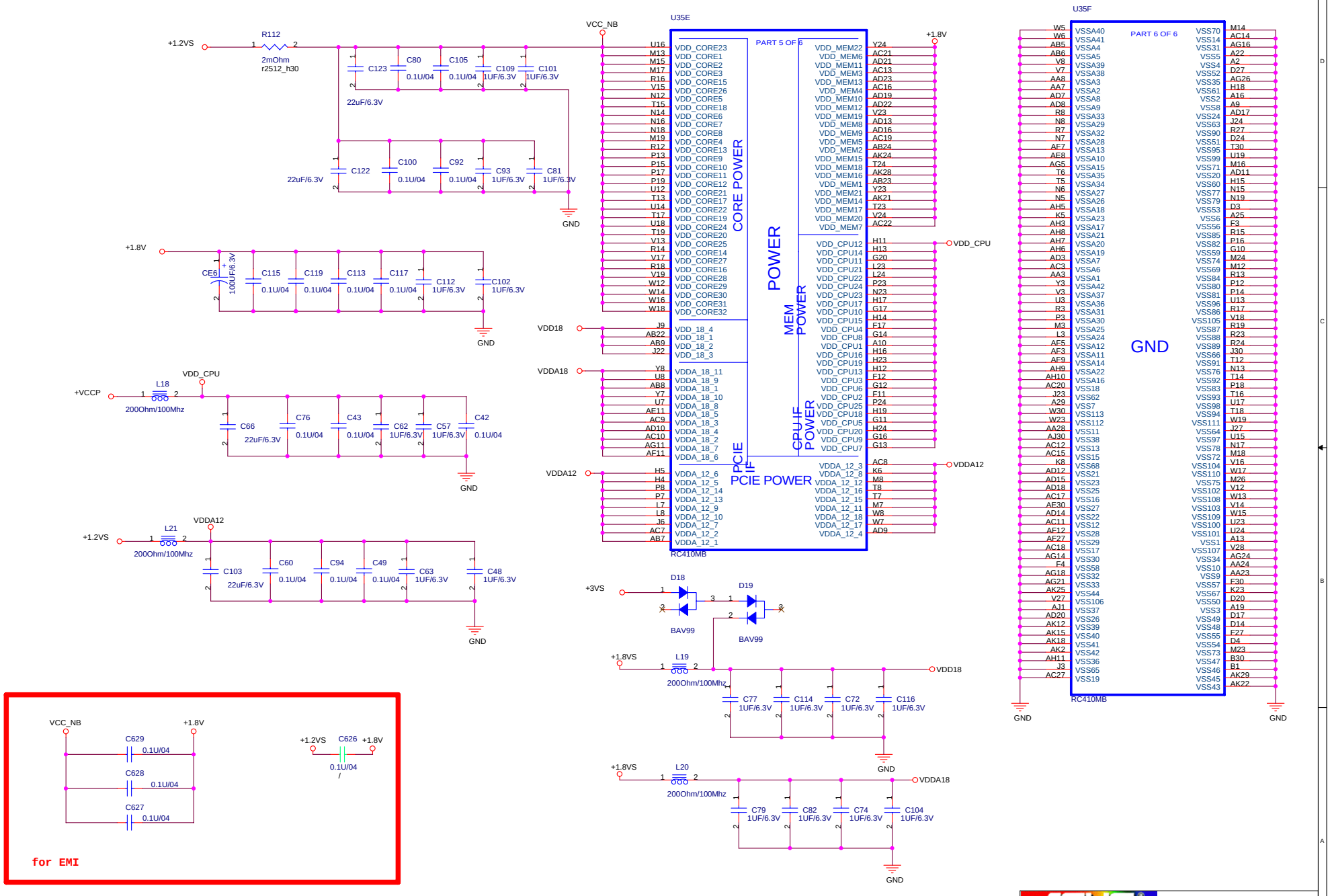

H_D#[63..0]
H_A#[31..3]
H_REQ#[4..0]
H_D#[63..0] 2
H_A#[31..3] 2
H_REQ#[4..0] 2
U35A
PART 1 OF 6
AGTL+ I/F
ADDR GROUP 0
ADDR GROUP 1
CONTROL
MISC.
DATA GROUP 0
DATA GROUP 1
DATA GROUP 2
DATA GROUP 3
RC410MB
H_ADSTB#0
H_ADSTB#1
H_ADS#
H_BNR#
H_BPRI#
H_DEFER#
H_DRDY#
H_DBSY#
H_DPWR#
H_LOCK#
H_TRDY#
H_HITM#
H_HIT#
H_RS#[2..0]
H_CPURST#
PM_SUS_STAT#
NB_RST#
NB_PWRGD
NB_COMP_P
NB_COMP_N
NB_CPVDD
GTLREF_NB
NB_THRMDA
NB_THRMDC
H_DINV#0 2
H_DSTBN#0 2
H_DSTBP#0 2
H_DINV#1 2
H_DSTBN#1 2
H_DSTBP#1 2
H_DINV#2 2
H_DSTBN#2 2
H_DSTBP#2 2
H_DINV#3 2
H_DSTBN#3 2
H_DSTBP#3 2
+1.8V
+VCCP
+1.8VS
R469
27KOhm
D49
D48
1SS355
T231
T18
TPC28t
R424
49.9Ohm
R59
24.9OHM
L23
120OHM
C110
1UF/6.3V
R426
1.8KOhm
GND
+VCCP
R74
49.9Ohm
PLACE CLOSE TO RS300M,
USE 10/10 WIDTH/SPACE
GTLREF_NB
R90
100OHM
C106
1UF/6.3V
C91
220P
GND
GND
GND
RC410MB A12 P/N:02-110010610
Title : RC410MB AGTL I/F(1)
<OrgName>
Engineer: <OrgAddr1>
Size Custom
Project Name A6R
Rev 2.0
Date: Thursday, August 04, 2005
Sheet 5 of 50



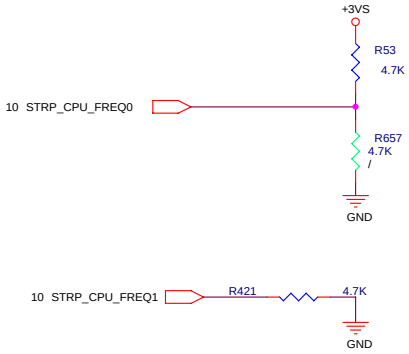
ASUS	Title :	RC410MB PCIE & A-Link(2)
<OrgName>	Engineer:	<OrgAddr1>
Size: Custom	Project Name: A6R	Rev: 2.0
Date: Thursday, August 04, 2005	Sheet 6 of 50	



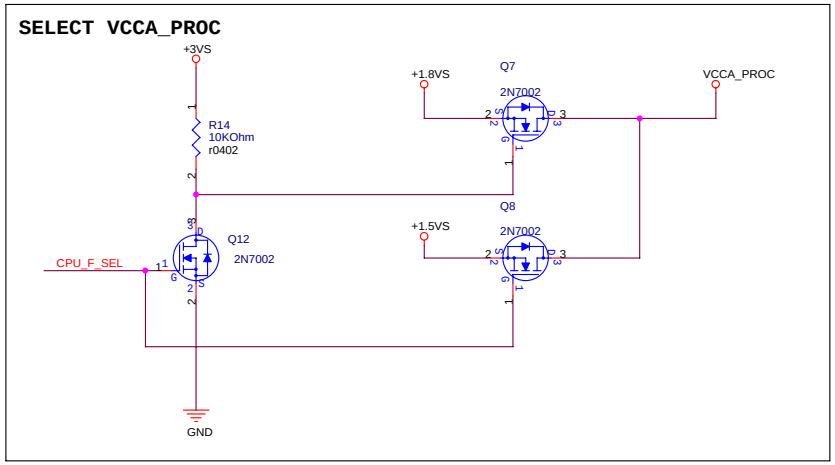
Title :	RC410MB DDR2 I/F (3)	
<OrgName>	Engineer: <OrgAddr1>	
Size: Custom	Project Name: A6R	Rev: 2.0
Date: Thursday, August 04, 2005	Sheet 7 of 50	

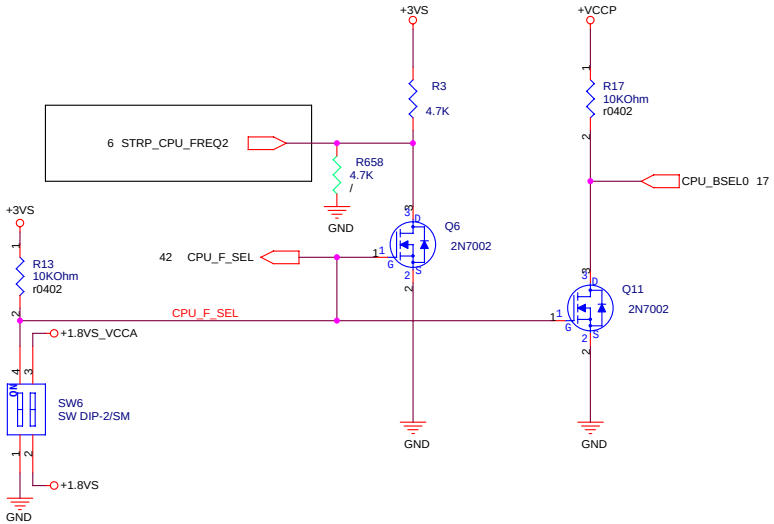


Title : RC410MB POWER (4)			
<OrgName>	Engineer: <OrgAddr1>		
Size: Custom	Project Name: A6R		Rev: 2.0
Date: Thursday, August 04, 2005	Sheet 8 of 50		

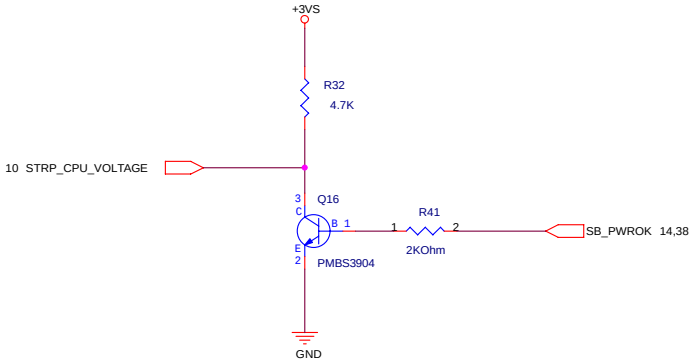


FSB	STRP_CPU_FREQ2	STRP_CPU_FREQ1	STRP_CPU_FREQ0
100MHZ	1	0	1
133MHZ	0	0	1





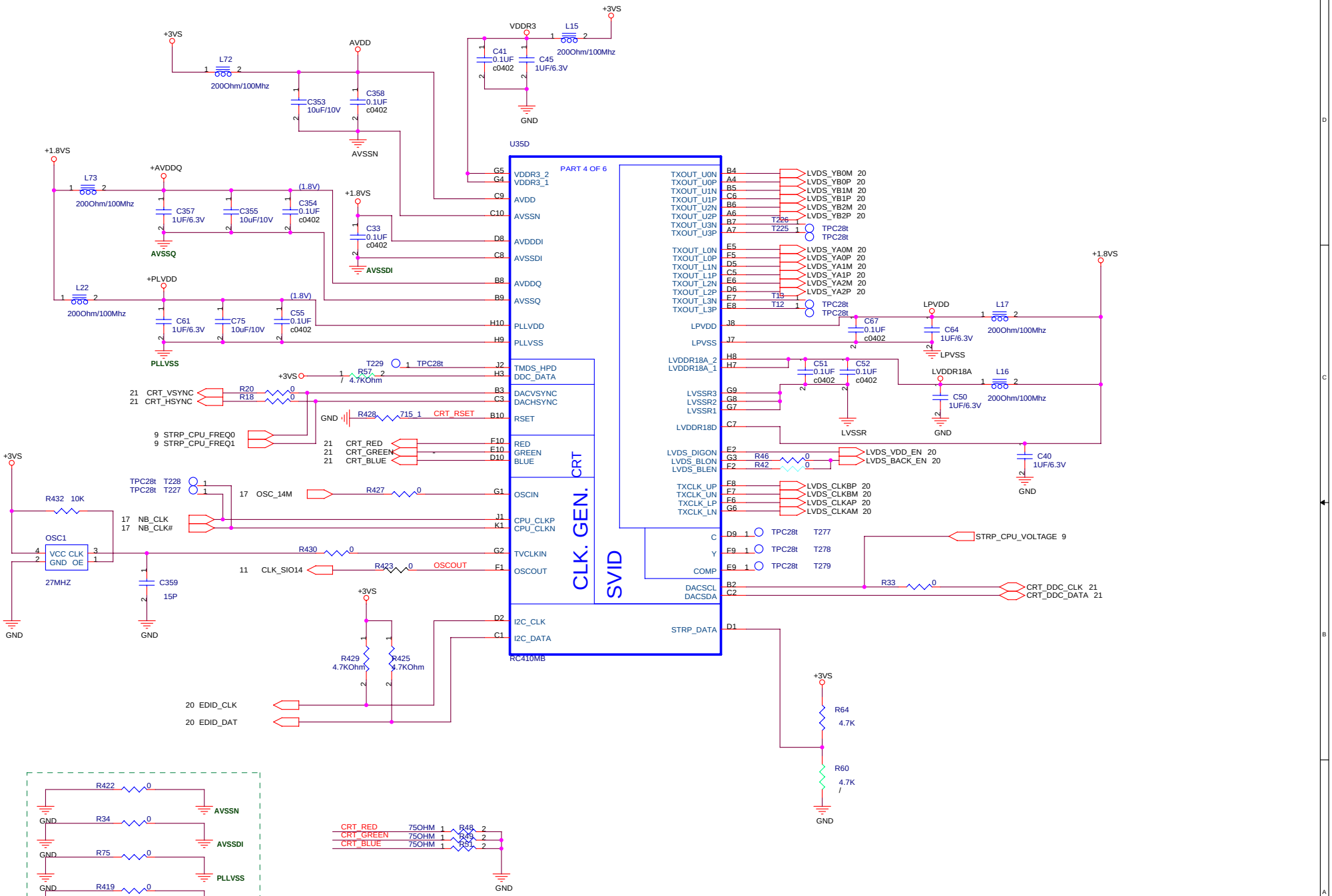
CELERON M
100



STRP_CPU_VOLTAGE: CPU VCC
0: MOBILE CPU
1: DESKTOP CPU
DEFAULT:0

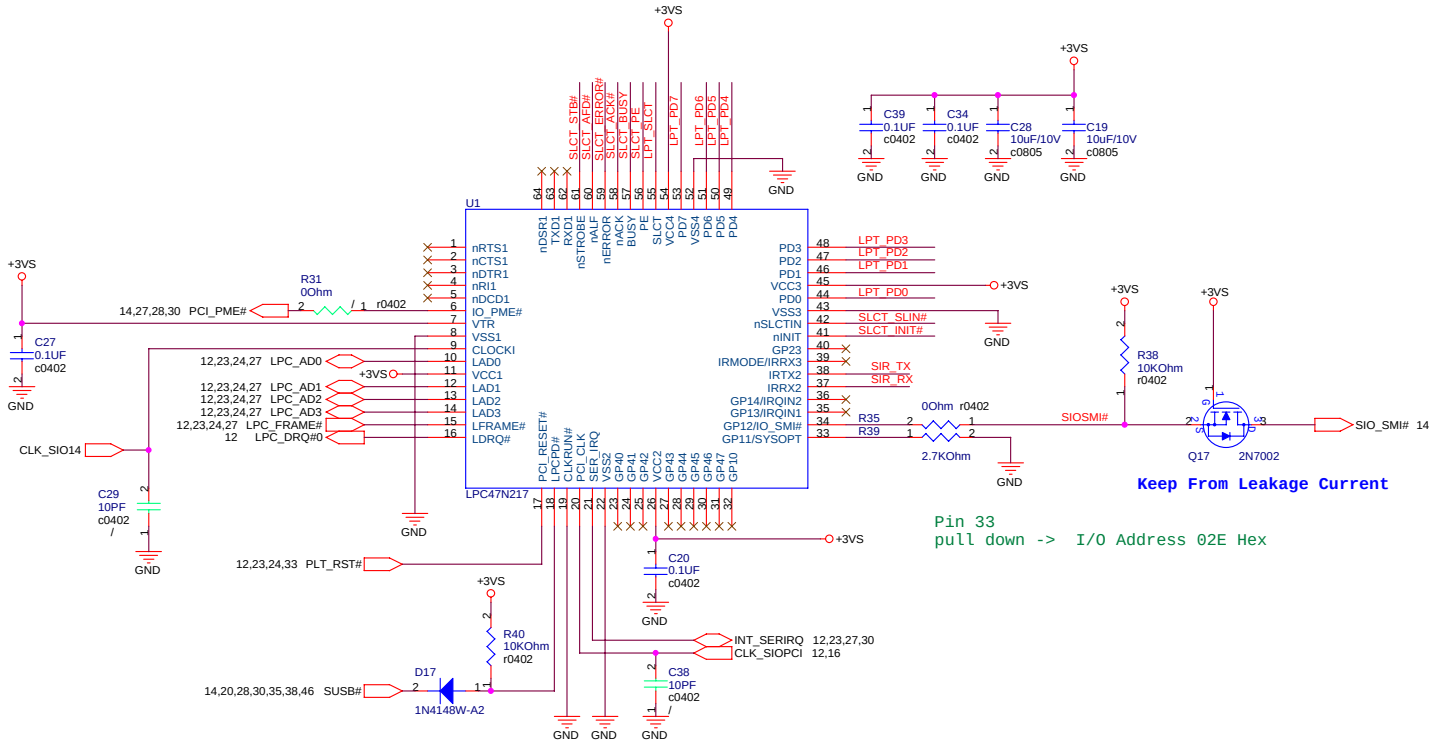
SW8
ON: CPU_F_SEL=0 FSB100MHz VCCA_PROC=1.8V
OFF: CPU_F_SEL=1 FSB133MHz VCCA_PROC=1.5V

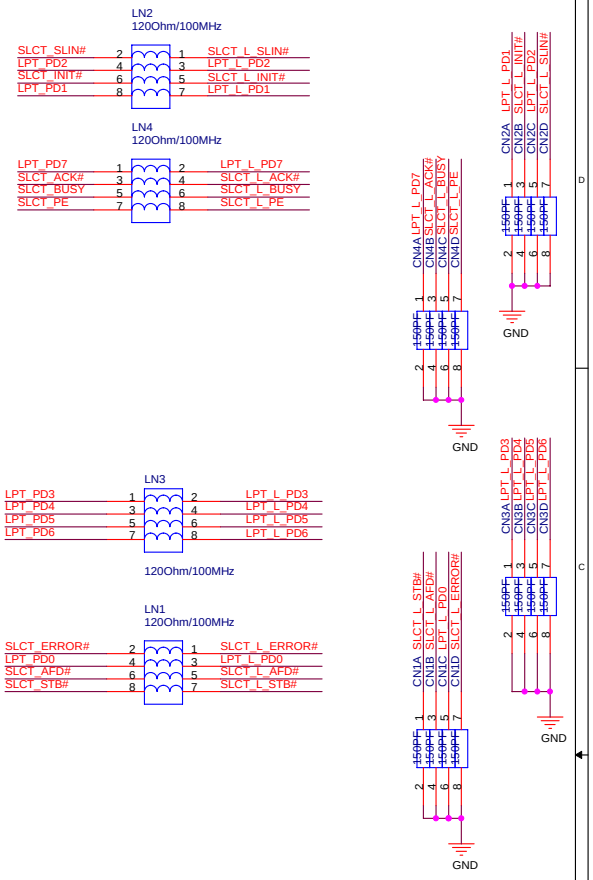
ASUS	Title : FSB SELECTION	
<OrgName>	Engineer: <OrgAddr1>	
Size: Custom	Project Name: A6R	Rev: 2.0
Date: Thursday, August 04, 2005	Sheet 9 of 50	



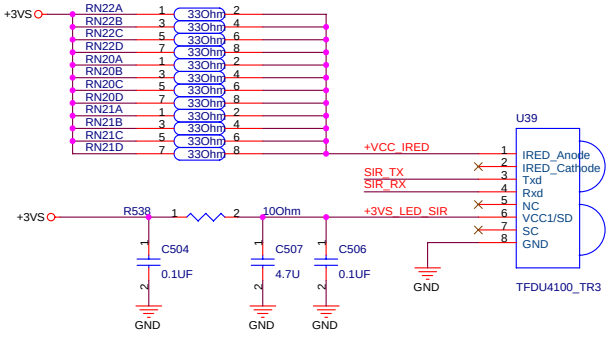
ASUS	Title : RC410MB VIDEO I/F (6)		
<OrgName>	Engineer: <OrgAddr1>		
Size: Custom	Project Name: A6R		Rev: 2.0
Date: Thursday, August 04, 2005	Sheet 10 of 50		

Super I/O

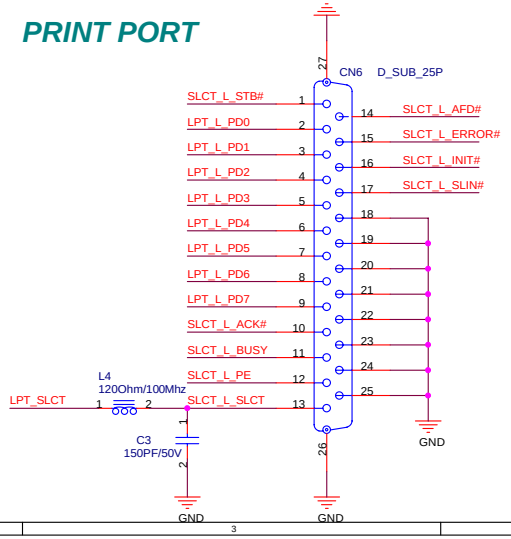


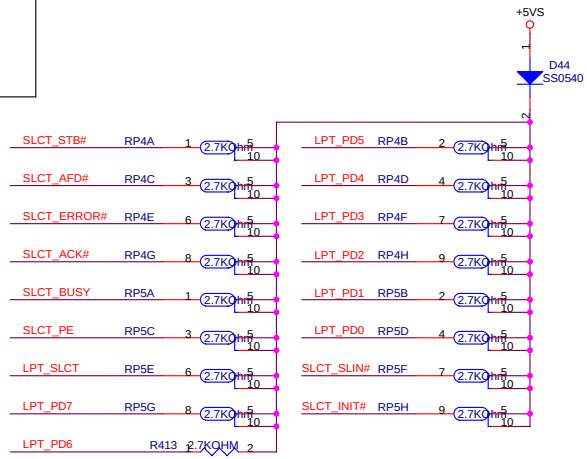


SIR



PRINT PORT





ASUS

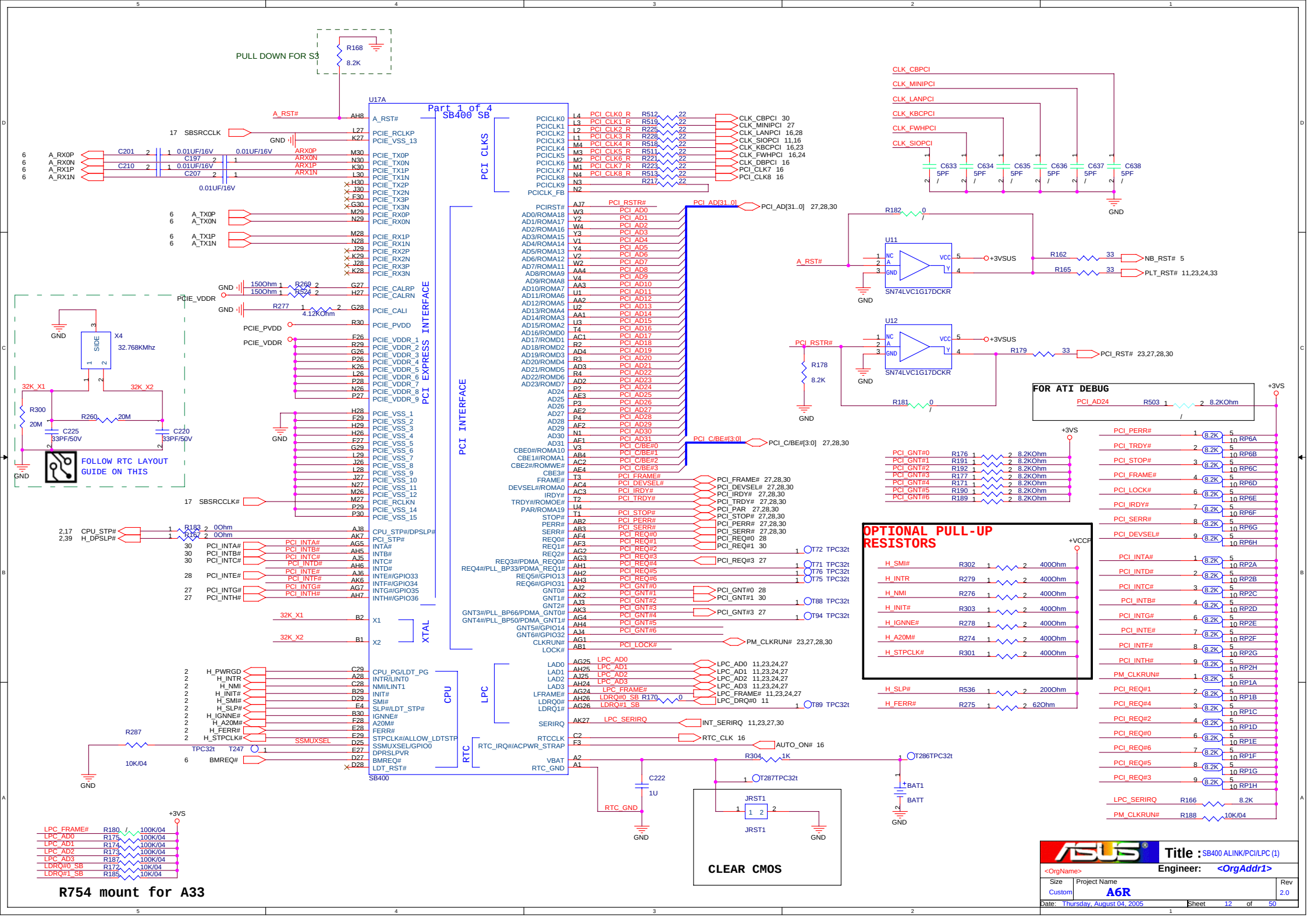
Title : SIO & SIR & PRINTER PORT

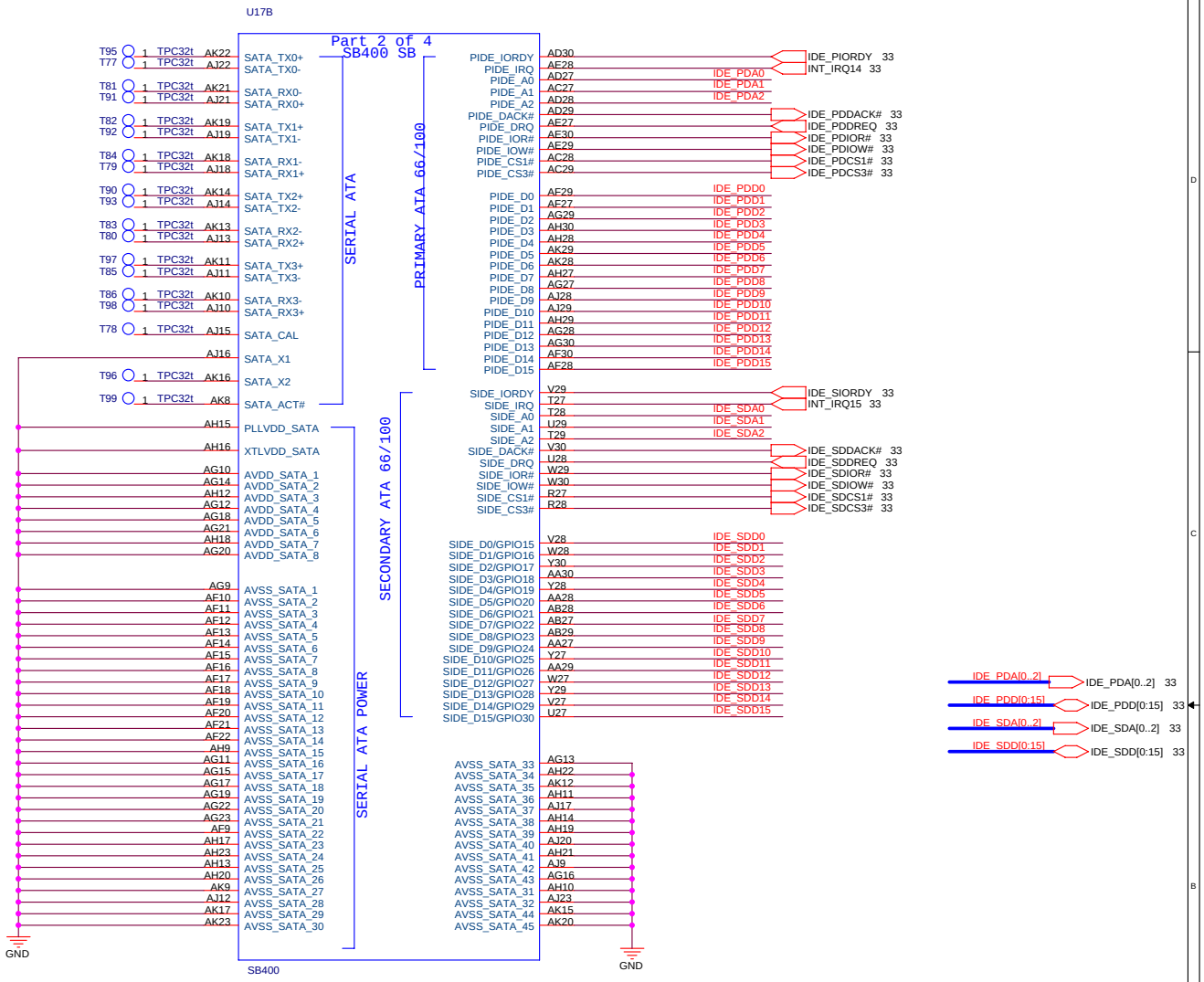
<OrgName>

Engineer: <OrgAddr1>

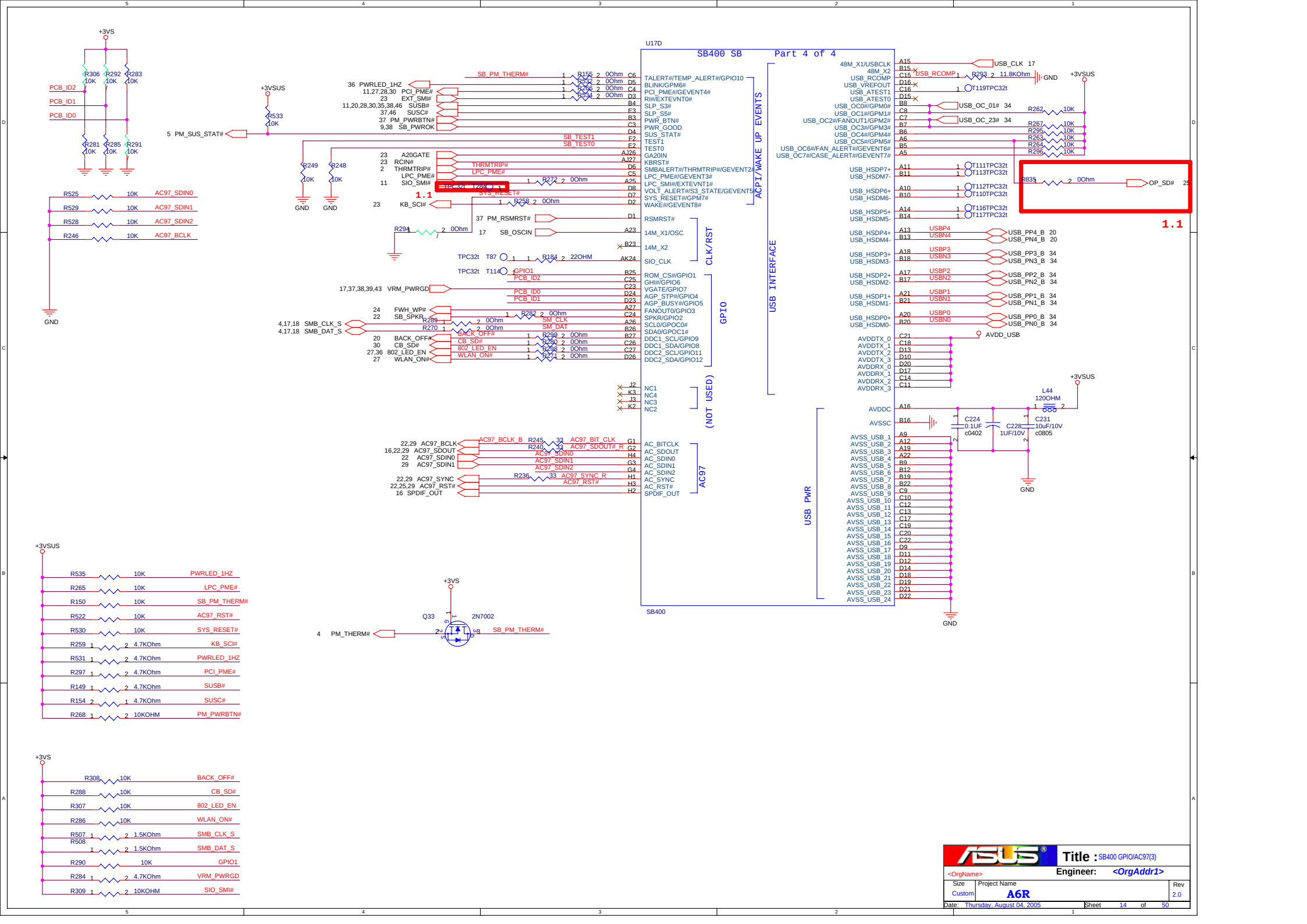
Size	Project Name	Rev
Custom	A6R	2.0

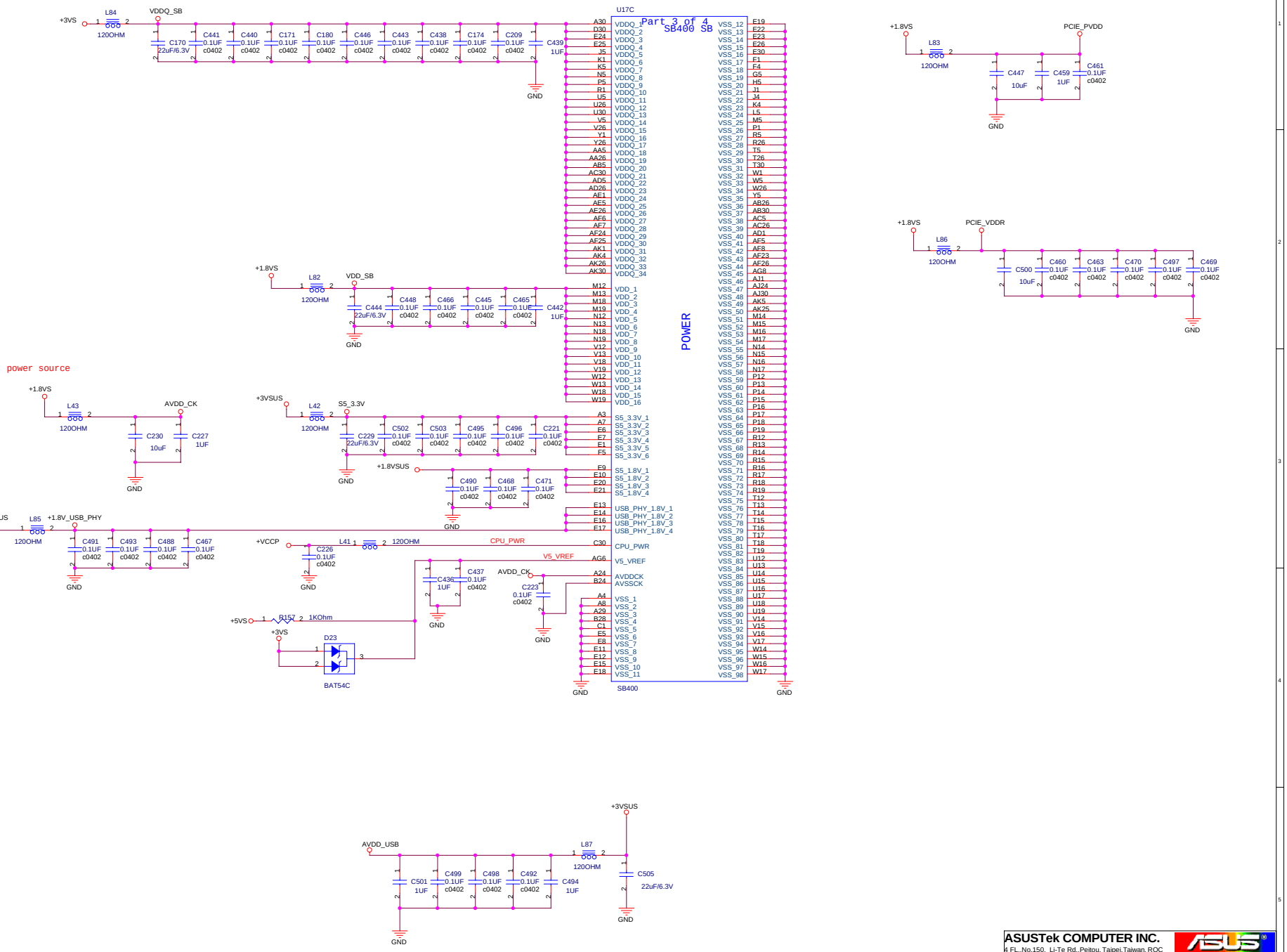
Date: Thursday, August 04, 2005 Sheet 11 of 50


PULL DOWN FOR S3
R168
8.2K
U17A
Part 1 of 4
SB400 SB
A_RST#
SBSRCCLK
A_RX0P
A_RX0N
A_RX1P
A_RX1N
C201
C197
C210
C207
0.01UF/16V
A_TX0P
A_TX0N
A_TX1P
A_TX1N
PCIE_RCLKP
PCIE_VSS_13
PCIE_TX0P
PCIE_TX0N
PCIE_TX1P
PCIE_TX1N
PCIE_TX2P
PCIE_TX2N
PCIE_TX3P
PCIE_TX3N
PCIE_RX0P
PCIE_RX0N
PCIE_RX1P
PCIE_RX1N
PCIE_RX2P
PCIE_RX2N
PCIE_RX3P
PCIE_RX3N
PCIE_CALRP
PCIE_CALRN
PCIE_CALI
PCIE_PVDD
PCIE_VDDR_1
PCIE_VDDR_2
PCIE_VDDR_3
PCIE_VDDR_4
PCIE_VDDR_5
PCIE_VDDR_6
PCIE_VDDR_7
PCIE_VDDR_8
PCIE_VDDR_9
PCIE_VSS_1
PCIE_VSS_2
PCIE_VSS_3
PCIE_VSS_4
PCIE_VSS_5
PCIE_VSS_6
PCIE_VSS_7
PCIE_VSS_8
PCIE_VSS_9
PCIE_VSS_10
PCIE_VSS_11
PCIE_VSS_12
PCIE_RCLKN
PCIE_VSS_14
PCIE_VSS_15
PCI EXPRESS INTERFACE
150Ohm
R269
R524
4.12KOhm
R277
X4
32.768KMhz
SIDE
32K_X1
32K_X2
R300
20M
R260
C225
C220
33PF/50V
FOLLOW RTC LAYOUT
GUIDE ON THIS
SBSRCCLK#
CPU_STP#
H_DPSLP#
R183
R167
0Ohm
CPU_STP#/DPSLP#
PCI_STP#
PCI_INTA#
PCI_INTB#
PCI_INTC#
PCI_INTD#
PCI_INTE#
PCI_INTF#
PCI_INTG#
PCI_INTH#
INTA#
INTB#
INTC#
INTD#
INTE#/GPIO33
INTF#/GPIO34
INTG#/GPIO35
INTH#/GPIO36
XTAL
CPU
H_PWRGD
H_INTR
H_NMI
H_INIT#
H_SMI#
H_SLP#
H_IGNNE#
H_A20M#
H_FERR#
H_STPCLK#
SSMUXSEL
R287
10K/04
TPC32t
T247
BMREQ#
CPU_PG/LDT_PG
INTR/LINT0
NMI/LINT1
INIT#
SMI#
SLP#/LDT_STP#
IGNNE#
A20M#
FERR#
STPCLK#/ALLOW_LDTSTP
SSMUXSEL/GPIO0
DPRSLPVR
BMREQ#
LDT_RST#
SB400
PCI CLKS
PCICLK0
PCICLK1
PCICLK2
PCICLK3
PCICLK4
PCICLK5
PCICLK6
PCICLK7
PCICLK8
PCICLK9
PCICLK_FB
PCI_CLK0_R
PCI_CLK1_R
PCI_CLK2_R
PCI_CLK3_R
PCI_CLK4_R
PCI_CLK5_R
PCI_CLK6_R
PCI_CLK7_R
PCI_CLK8_R
R512
R519
R225
R228
R518
R511
R221
R223
R513
R217
22
CLK_CBPCI 30
CLK_MINIPCI 27
CLK_LANPCI 16,28
CLK_SIOPCI 11,16
CLK_KBCPCI 16,23
CLK_FWHPCI 16,24
CLK_DBPCI 16
PCI_CLK7 16
PCI_CLK8 16
PCI INTERFACE
PCIRST#
PCI_RSTR#
PCI_AD0
PCI_AD1
PCI_AD2
PCI_AD3
PCI_AD4
PCI_AD5
PCI_AD6
PCI_AD7
PCI_AD8
PCI_AD9
PCI_AD10
PCI_AD11
PCI_AD12
PCI_AD13
PCI_AD14
PCI_AD15
PCI_AD16
PCI_AD17
PCI_AD18
PCI_AD19
PCI_AD20
PCI_AD21
PCI_AD22
PCI_AD23
PCI_AD24
PCI_AD25
PCI_AD26
PCI_AD27
PCI_AD28
PCI_AD29
PCI_AD30
PCI_AD31
PCI_AD[31..0]
PCI_C/BE#0
PCI_C/BE#1
PCI_C/BE#2
PCI_C/BE#3
PCI_C/BE#[3:0]
PCI_FRAME#
PCI_DEVSEL#
PCI_IRDY#
PCI_TRDY#
PCI_STOP#
PCI_PERR#
PCI_SERR#
PCI_REQ#0
PCI_REQ#1
PCI_REQ#2
PCI_REQ#3
PCI_REQ#4
PCI_REQ#5
PCI_REQ#6
PCI_GNT#0
PCI_GNT#1
PCI_GNT#2
PCI_GNT#3
PCI_GNT#4
PCI_GNT#5
PCI_LOCK#
PM_CLKRUN# 23,27,28,30
LPC
LAD0
LAD1
LAD2
LAD3
LFRAME#
LDRQ0#
LDRQ1#
SERIRQ
LPC_AD0
LPC_AD1
LPC_AD2
LPC_AD3
LPC_FRAME#
LDRQ#0_SB
LDRQ#1_SB
R170
INT_SERIRQ 11,23,27,30
RTC
RTCCLK
RTC_IRQ#/ACPWR_STRAP
VBAT
RTC_GND
RTC_CLK 16
AUTO_ON# 16
C222
1U
R304
1K
T286TPC32t
T287TPC32t
BAT1
BATT
JRST1
CLEAR CMOS
R754 mount for A33
LPC_FRAME#
LPC_AD0
LPC_AD1
LPC_AD2
LPC_AD3
LDRQ#0_SB
LDRQ#1_SB
R180
R175
R174
R173
R187
R172
R185
100K/04
10K/04
+3VS
CLK_CBPCI
CLK_MINIPCI
CLK_LANPCI
CLK_KBCPCI
CLK_FWHPCI
CLK_SIOPCI
C633
C634
C635
C636
C637
C638
5PF
GND
R182
U11
U12
SN74LVC1G17DCKR
+3VSUS
R162
R165
R179
NB_RST# 5
PLT_RST# 11,23,24,33
PCI_RST# 23,27,28,30
R178
8.2K
R181
FOR ATI DEBUG
PCI_AD24
R503
8.2KOhm
+3VS
PCI_GNT#0
PCI_GNT#1
PCI_GNT#2
PCI_GNT#3
PCI_GNT#4
PCI_GNT#5
PCI_GNT#6
R176
R191
R192
R177
R171
R190
R189
8.2KOhm
OPTIONAL PULL-UP
RESISTORS
+VCCP
H_SMI#
H_INTR
H_NMI
H_INIT#
H_IGNNE#
H_A20M#
H_STPCLK#
R302
R279
R276
R303
R278
R274
R301
400Ohm
H_SLP#
H_FERR#
R536
R275
200Ohm
62Ohm
PCI_PERR#
PCI_TRDY#
PCI_STOP#
PCI_FRAME#
PCI_LOCK#
PCI_IRDY#
PCI_SERR#
PCI_DEVSEL#
PCI_INTA#
PCI_INTD#
PCI_INTC#
PCI_INTB#
PCI_INTG#
PCI_INTE#
PCI_INTF#
PCI_INTH#
PM_CLKRUN#
PCI_REQ#1
PCI_REQ#4
PCI_REQ#2
PCI_REQ#0
PCI_REQ#6
PCI_REQ#5
PCI_REQ#3
LPC_SERIRQ
R166
R188
8.2K
10K/04
RP6A
RP6B
RP6C
RP6D
RP6E
RP6F
RP6G
RP6H
RP2A
RP2B
RP2C
RP2D
RP2E
RP2F
RP2G
RP2H
RP1A
RP1B
RP1C
RP1D
RP1E
RP1F
RP1G
RP1H
Title : SB400 ALINK/PCI/LPC (1)
Engineer: <OrgAddr1>
<OrgName>
Size
Custom
Project Name
A6R
Rev
2.0
Date: Thursday, August 04, 2005
Sheet 12 of 50



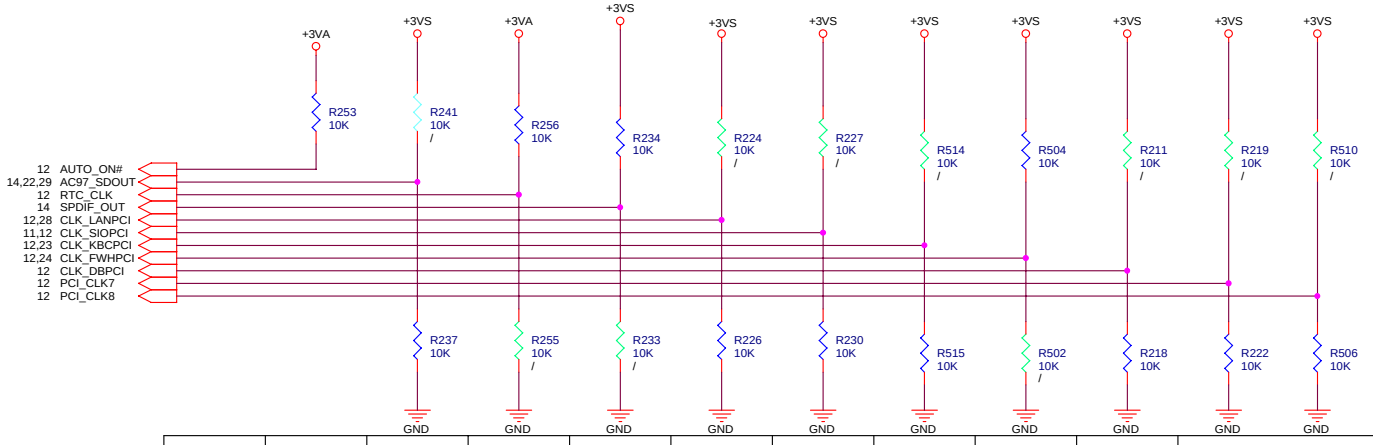
ASUS	Title : SB400 IDE/USB/MII (2)	
<OrgName>	Engineer: <OrgAddr1>	
Size: Custom	Project Name: A6R	Rev: 2.0
Date: Thursday, August 04, 2005	Sheet 13 of 50	


U17D
SB400 SB
Part 4 of 4
SB400
TALERT#/TEMP_ALERT#/GPIO10
BLINK/GPM6#
PCI_PME#/GEVENT4#
RI#/EXTEVNT0#
SLP_S3#
SLP_S5#
PWR_BTN#
PWR_GOOD
SUS_STAT#
TEST1
TEST0
GA20IN
KBRST#
SMBALERT#/THRMTRIP#/GEVENT2#
LPC_PME#/GEVENT3#
LPC_SMI#/EXTEVNT1#
VOLT_ALERT#/S3_STATE/GEVENT5#
SYS_RESET#/GPM7#
WAKE#/GEVENT8#
ACPI/WAKE UP EVENTS
RSMRST#
14M_X1/OSC
14M_X2
SIO_CLK
CLK/RST
ROM_CS#/GPIO1
GHI#/GPIO6
VGATE/GPIO7
AGP_STP#/GPIO4
AGP_BUSY#/GPIO5
FANOUT0/GPIO3
SPKR/GPIO2
SCL0/GPOC0#
SDA0/GPOC1#
DDC1_SCL/GPIO9
DDC1_SDA/GPIO8
DDC2_SCL/GPIO11
DDC2_SDA/GPIO12
GPIO
NC1
NC4
NC3
NC2
(NOT USED)
AC_BITCLK
AC_SDOUT
AC_SDIN0
AC_SDIN1
AC_SDIN2
AC_SYNC
AC_RST#
SPDIF_OUT
AC97
48M_X1/USBCLK
48M_X2
USB_RCOMP
USB_VREFOUT
USB_ATEST1
USB_ATEST0
USB_OC0#/GPM0#
USB_OC1#/GPM1#
USB_OC2#/FANOUT1/GPM2#
USB_OC3#/GPM3#
USB_OC4#/GPM4#
USB_OC5#/GPM5#
USB_OC6#/FAN_ALERT#/GEVENT6#
USB_OC7#/CASE_ALERT#/GEVENT7#
USB_HSDP7+
USB_HSDM7-
USB_HSDP6+
USB_HSDM6-
USB_HSDP5+
USB_HSDM5-
USB_HSDP4+
USB_HSDM4-
USB_HSDP3+
USB_HSDM3-
USB_HSDP2+
USB_HSDM2-
USB_HSDP1+
USB_HSDM1-
USB_HSDP0+
USB_HSDM0-
USB INTERFACE
AVDDTX_0
AVDDTX_1
AVDDTX_2
AVDDTX_3
AVDDRX_0
AVDDRX_1
AVDDRX_2
AVDDRX_3
AVDD_USB
AVDDC
AVSSC
AVSS_USB_1
AVSS_USB_2
AVSS_USB_3
AVSS_USB_4
AVSS_USB_5
AVSS_USB_6
AVSS_USB_7
AVSS_USB_8
AVSS_USB_9
AVSS_USB_10
AVSS_USB_11
AVSS_USB_12
AVSS_USB_13
AVSS_USB_14
AVSS_USB_15
AVSS_USB_16
AVSS_USB_17
AVSS_USB_18
AVSS_USB_19
AVSS_USB_20
AVSS_USB_21
AVSS_USB_22
AVSS_USB_23
AVSS_USB_24
USB PWR
+3VS
+3VSUS
GND
PCB_ID2
PCB_ID1
PCB_ID0
R306 10K
R292 10K
R283 10K
R281 10K
R285 10K
R291 10K
R533 10K
5 PM_SUS_STAT#
SB_TEST1
SB_TEST0
R249 10K
R248 10K
SB_PM_THERM#
R155 0Ohm
R252 0Ohm
R266 0Ohm
R534 0Ohm
36 PWRLED_1HZ
11,27,28,30 PCI_PME#
23 EXT_SMI#
11,20,28,30,35,38,46 SUSB#
37,46 SUSC#
37 PM_PWRBTN#
9,38 SB_PWROK
23 A20GATE
23 RCIN#
2 THRMTRIP#
LPC_PME#
11 SIO_SMI#
THRMTRIP#
LPC_PME#
R272 0Ohm
SYS_RESET#
1.1
23 KB_SCI#
R258 0Ohm
37 PM_RSMRST#
R294 0Ohm
17 SB_OSCIN
TPC32t T87
R184 22OHM
TPC32t T114
GPIO1
PCB_ID2
17,37,38,39,43 VRM_PWRGD
PCB_ID0
PCB_ID1
24 FWH_WP#
22 SB_SPKR
R282 0Ohm
4,17,18 SMB_CLK_S
4,17,18 SMB_DAT_S
R289 0Ohm
R270 0Ohm
SM_CLK
SM_DAT
20 BACK_OFF#
30 CB_SD#
27,36 802_LED_EN
27 WLAN_ON#
R299 0Ohm
R260 0Ohm
R298 0Ohm
R271 0Ohm
22,29 AC97_BCLK
16,22,29 AC97_SDOUT
22 AC97_SDIN0
29 AC97_SDIN1
AC97_BCLK_B
R245 33
R240 33
AC97_BIT_CLK
AC97_SDOUT#_R
AC97_SDIN0
AC97_SDIN1
AC97_SDIN2
22,29 AC97_SYNC
22,25,29 AC97_RST#
16 SPDIF_OUT
R236 33
AC97_SYNC_R
AC97_RST#
Q33 2N7002
4 PM_THERM#
SB_PM_THERM#
USB_CLK 17
USB_RCOMP
R293 11.8KOhm
T119TPC32t
USB_OC_01# 34
USB_OC_23# 34
R262 10K
R267 10K
R295 10K
R263 10K
R264 10K
R296 10K
T111TPC32t
T113TPC32t
R835 0Ohm
OP_SD# 25
T112TPC32t
T110TPC32t
T116TPC32t
T117TPC32t
1.1
USBP4
USBN4
USB_PP4_B 20
USB_PN4_B 20
USBP3
USBN3
USB_PP3_B 34
USB_PN3_B 34
USBP2
USBN2
USB_PP2_B 34
USB_PN2_B 34
USBP1
USBN1
USB_PP1_B 34
USB_PN1_B 34
USBP0
USBN0
USB_PP0_B 34
USB_PN0_B 34
L44 120OHM
C224 0.1UF c0402
C228 1UF/10V
C231 10uF/10V c0805
R525 10K AC97_SDIN0
R529 10K AC97_SDIN1
R528 10K AC97_SDIN2
R246 10K AC97_BCLK
R535 10K PWRLED_1HZ
R265 10K LPC_PME#
R150 10K SB_PM_THERM#
R522 10K AC97_RST#
R530 10K SYS_RESET#
R259 4.7KOhm KB_SCI#
R531 4.7KOhm PWRLED_1HZ
R297 4.7KOhm PCI_PME#
R149 4.7KOhm SUSB#
R154 4.7KOhm SUSC#
R268 10KOHM PM_PWRBTN#
R308 10K BACK_OFF#
R288 10K CB_SD#
R307 10K 802_LED_EN
R286 10K WLAN_ON#
R507 1.5KOhm SMB_CLK_S
R508 1.5KOhm SMB_DAT_S
R290 10K GPIO1
R284 4.7KOhm VRM_PWRGD
R309 10KOHM SIO_SMI#
Title : SB400 GPIO/AC97(3)
<OrgName>
Engineer: <OrgAddr1>
Size Custom
Project Name A6R
Rev 2.0
Date: Thursday, August 04, 2005
Sheet 14 of 50



ASUSTek COMPUTER INC.	
4 FL.,No.150, Li-Te Rd.,Peitou, Taipei,Taiwan, ROC	
Title	**SB400 PWR/DECOUPLING(4)**
Size: Custom	Document Number: **A6R**
Rev	2.0
Date: Thursday, August 04, 2005	Sheet 15 of 50

REQUIRED STRAPS



	AUTO_ON#	AC_SDOUT	RTC_CLK	SPDIF_OUT	CLK_LANPCI	CLK_SIOPCI	CLK_KBCPCI	CLK_FWHPCI	CLK_DBPCI	PCI_CLK7 PCI_CLK8
PULL HIGH	MANUAL PWR ON	USE DEBUG STRAPS	INTERNAL RTC	SIO 24MHz	SEE NOTE1	USB PHY PWRDOWN DISABLE	USE USB PLL	SEE NOTE2	CPU I/F = K8	ROM TYPE H,H = PCI ROM H,L = LPC ROM I DEFAULT LPC Address Mapped below 1M L,H = LPC ROM II LPC Address Mapped to top 4G L,L = FWH ROM
PULL LOW	AUTO PWR ON	IGNORE DEBUG STRAPS	EXTERNAL RTC (NOT SUPPORTED W/ IT8712)	SIO 48MHz		USB PHY PWRDOWN ENABLE	BYPASS USB PLL		CPU I/F = P4	

NOTE

1. USB CLK STRAPPING CHANGE

	A21,A22,A23	A31 AND NEWER
10K PULL UP	OSC/CLOCK BUFFER	CRYSTAL PAD
10K PULL DOWN	CRYSTAL PAD	OSC/CLOCK BUFFER

2. 14MHz CLOCK TYPE STRAPPING

	A11~A31	A32 AND ABOVE
	14MHz CLOCK PAD IS CRYSTAL PAD	PCIE COMMON MODE SETTING
10K PULL UP	CLOCK INPUT BUFFER	PCIE CM_SET LOW
10K PULL DOWN	CRYSTAL PAD	PCIE CM_SET HIGH

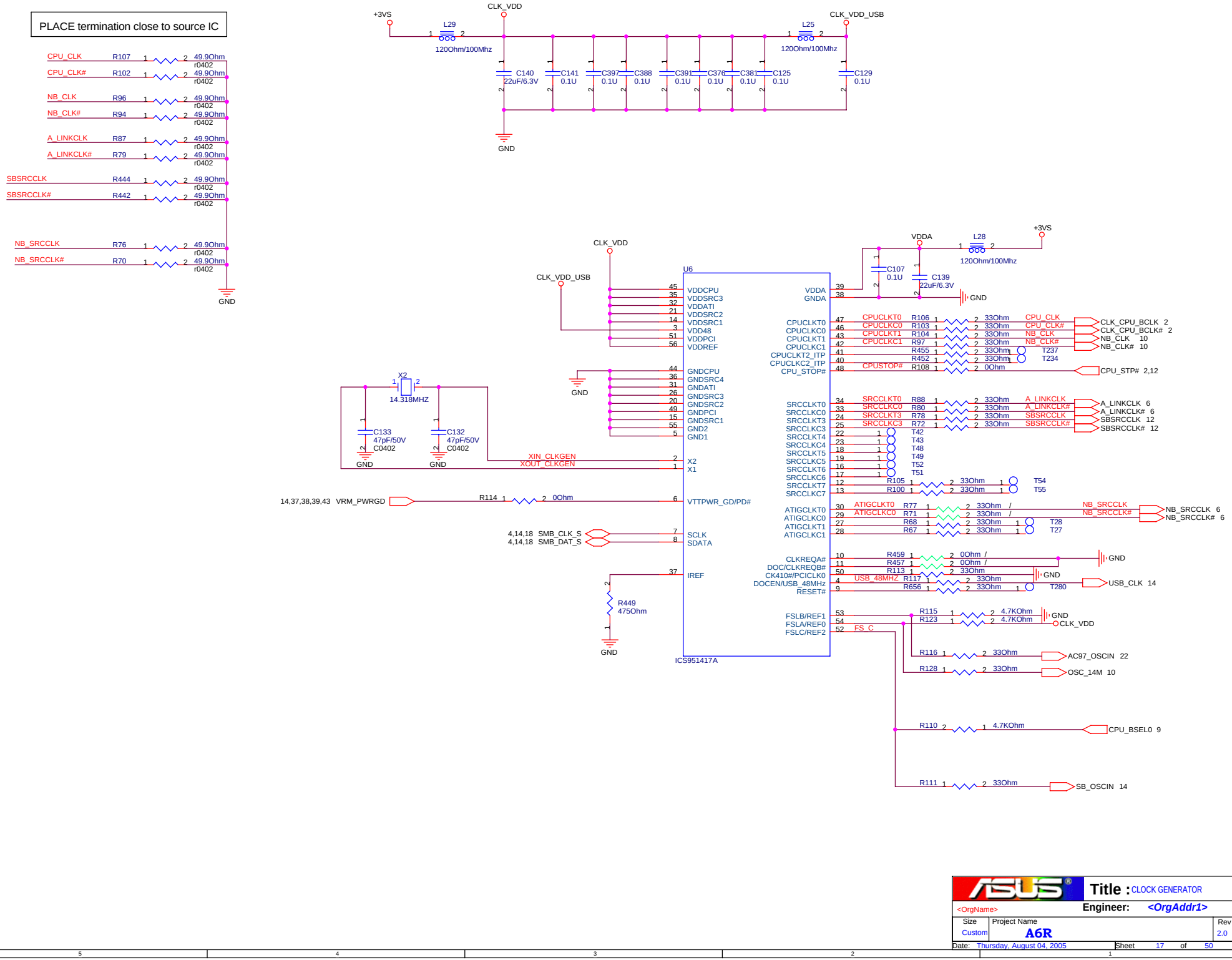
ASUS

Title : SB400 STRAPS(5)

<OrgName> Engineer: <OrgAddr1>

Size	Project Name	Rev
Custom	A6R	2.0

Date: Thursday, August 04, 2005 Sheet 16 of 50


PLACE termination close to source IC
CPU_CLK R107 49.9Ohm r0402
CPU_CLK# R102 49.9Ohm r0402
NB_CLK R96 49.9Ohm r0402
NB_CLK# R94 49.9Ohm r0402
A_LINKCLK R87 49.9Ohm r0402
A_LINKCLK# R79 49.9Ohm r0402
SBSRCCLK R444 49.9Ohm r0402
SBSRCCLK# R442 49.9Ohm r0402
NB_SRCCLK R76 49.9Ohm r0402
NB_SRCCLK# R70 49.9Ohm r0402
GND
+3VS
L29 120Ohm/100Mhz
CLK_VDD
C140 22uF/6.3V
C141 0.1U
C397 0.1U
C388 0.1U
C391 0.1U
C376 0.1U
C381 0.1U
C125 0.1U
L25 120Ohm/100Mhz
CLK_VDD_USB
C129 0.1U
U6
ICS951417A
VDDCPU
VDDSRC3
VDDATI
VDDSRC2
VDDSRC1
VDD48
VDDPCI
VDDREF
GNDCPU
GNDSRC4
GNDATI
GNDSRC3
GNDSRC2
GNDPCI
GNDSRC1
GND2
GND1
X2
X1
VTTPWR_GD/PD#
SCLK
SDATA
IREF
VDDA
GNDA
CPUCLKT0
CPUCLKC0
CPUCLKT1
CPUCLKC1
CPUCLKT2_ITP
CPUCLKC2_ITP
CPU_STOP#
SRCCLKT0
SRCCLKC0
SRCCLKT3
SRCCLKC3
SRCCLKT4
SRCCLKC4
SRCCLKT5
SRCCLKC5
SRCCLKT6
SRCCLKC6
SRCCLKT7
SRCCLKC7
ATIGCLKT0
ATIGCLKC0
ATIGCLKT1
ATIGCLKC1
CLKREQA#
DOC/CLKREQB#
CK410#/PCICLK0
DOCEN/USB_48MHz
RESET#
FSLB/REF1
FSLA/REF0
FSLC/REF2
FS_C
X2 14.318MHZ
C133 47pF/50V C0402
C132 47pF/50V C0402
XIN_CLKGEN
XOUT_CLKGEN
R449 475Ohm
14,37,38,39,43 VRM_PWRGD
R114 0Ohm
4,14,18 SMB_CLK_S
4,14,18 SMB_DAT_S
VDDA
L28 120Ohm/100Mhz
+3VS
C107 0.1U
C139 22uF/6.3V
CPUCLKT0 R106 33Ohm CPU_CLK
CPUCLKC0 R103 33Ohm CPU_CLK#
CPUCLKT1 R104 33Ohm NB_CLK
CPUCLKC1 R97 33Ohm NB_CLK#
R455 33Ohm T237
R452 33Ohm T234
CPUSTOP# R108 0Ohm
CPU_STP# 2,12
CLK_CPU_BCLK 2
CLK_CPU_BCLK# 2
NB_CLK 10
NB_CLK# 10
SRCCLKT0 R88 33Ohm A_LINKCLK
SRCCLKC0 R80 33Ohm A_LINKCLK#
SRCCLKT3 R78 33Ohm SBSRCCLK
SRCCLKC3 R72 33Ohm SBSRCCLK#
T42
T43
T48
T49
T52
T51
R105 33Ohm T54
R100 33Ohm T55
A_LINKCLK 6
A_LINKCLK# 6
SBSRCCLK 12
SBSRCCLK# 12
ATIGCLKT0 R77 33Ohm / NB_SRCCLK
ATIGCLKC0 R71 33Ohm / NB_SRCCLK#
R68 33Ohm T28
R67 33Ohm T27
NB_SRCCLK 6
NB_SRCCLK# 6
R459 0Ohm /
R457 0Ohm /
R113 33Ohm
USB_48MHZ R117 33Ohm
R656 33Ohm T280
USB_CLK 14
R115 4.7KOhm
R123 4.7KOhm
R116 33Ohm
AC97_OSCIN 22
R128 33Ohm
OSC_14M 10
R110 4.7KOhm
CPU_BSEL0 9
R111 33Ohm
SB_OSCIN 14
GND
CLK_VDD
Title : CLOCK GENERATOR
<OrgName>
Engineer: <OrgAddr1>
Size Custom
Project Name A6R
Rev 2.0
Date: Thursday, August 04, 2005
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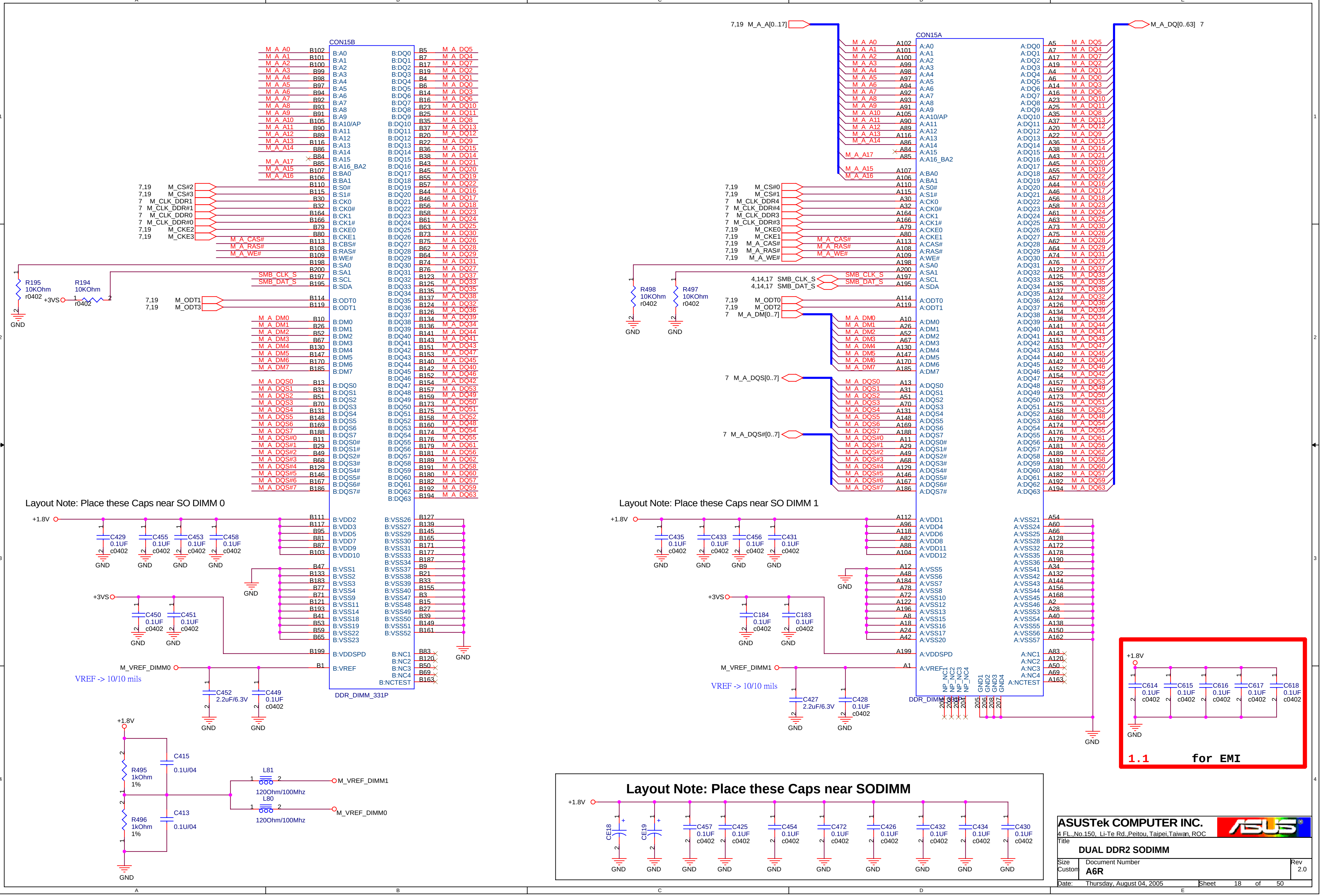
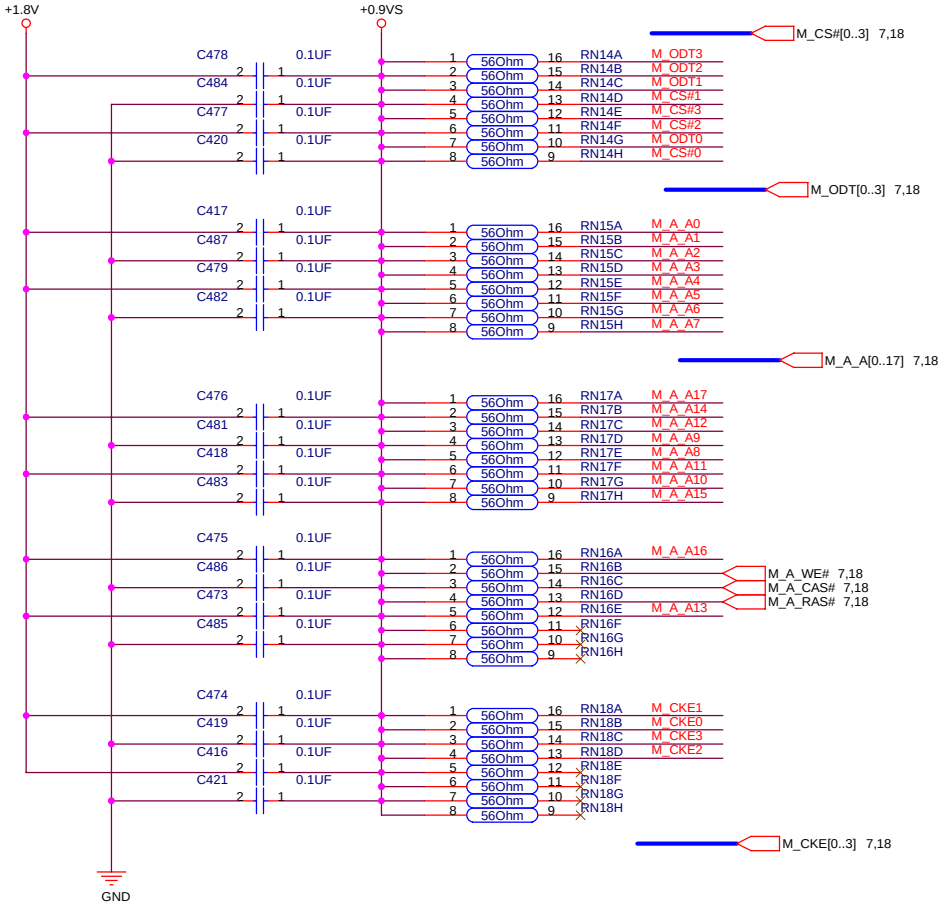


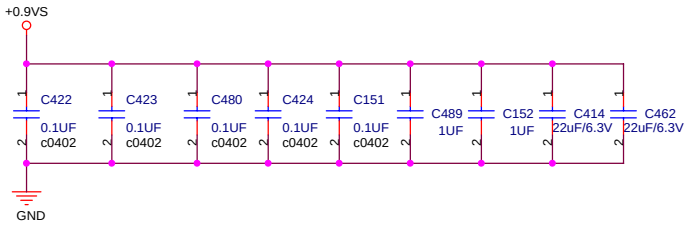
ASUSTek COMPUTER INC.
4 FL.,No.150, Li-Te Rd.,Peitou, Taipei,Taiwan, ROC

Title: DUAL DDR2 SODIMM

Size: Custom | Document Number: A6R | Rev: 2.0

Date: Thursday, August 04, 2005 | Sheet 18 of 50

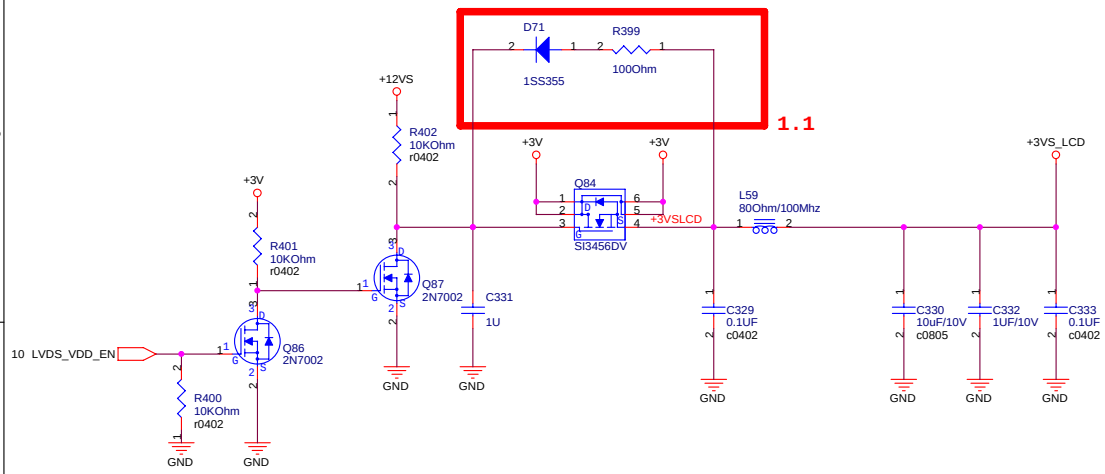




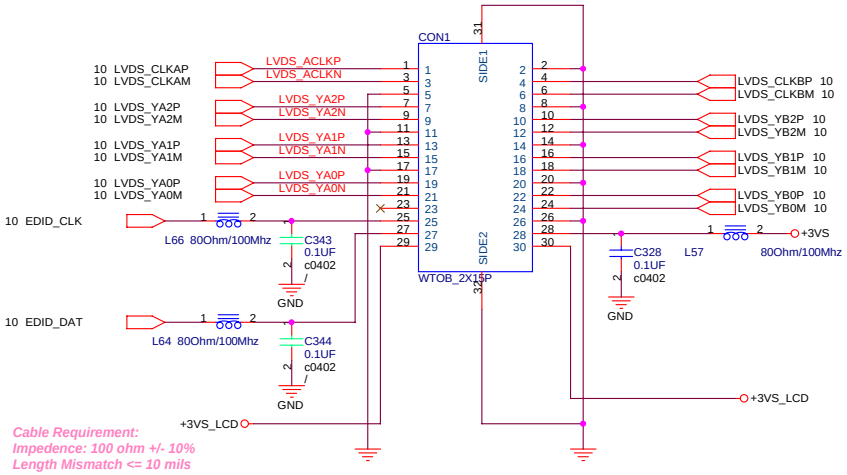
Title : DDR2 TERMINATION		
<OrgName>	Engineer: <OrgAddr1>	
Size: Custom	Project Name: A6R	Rev: 2.0
Date: Thursday, August 04, 2005	Sheet 19 of 50	

LCD Power

3V-3.6V
Full Active: 410 mA(Max. 500 mA)



LCD LVDS Interface

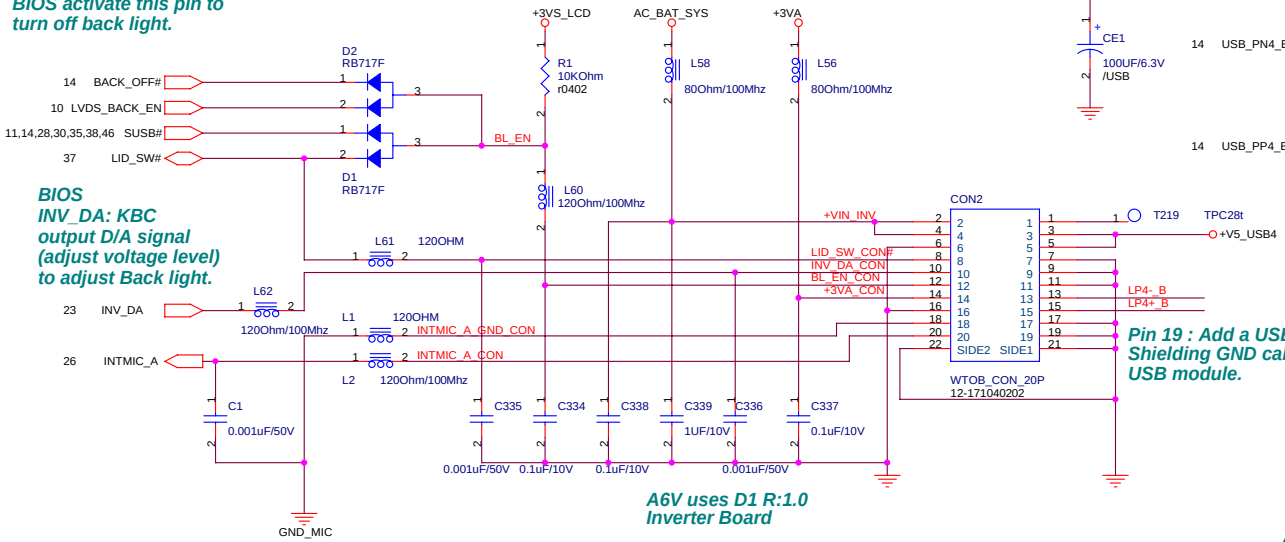


Cable Requirement:
Impedence: 100 ohm +/- 10%
Length Mismatch <= 10 mils
Twisted Pair(Not Ribbon)
Maximum Length <= 16"

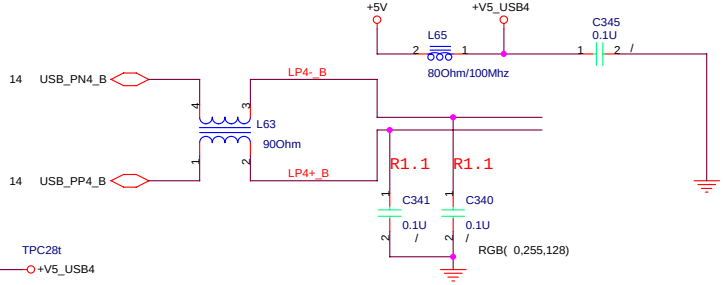
INVERTER Interface

BIOS
BACK_OFF#: When user pushs "Fn+F7" button, BIOS activate this pin to turn off back light.

BIOS
INV_DA: KBC output D/A signal (adjust voltage level) to adjust Back light.



A6V uses D1 R:1.0 Inverter Board

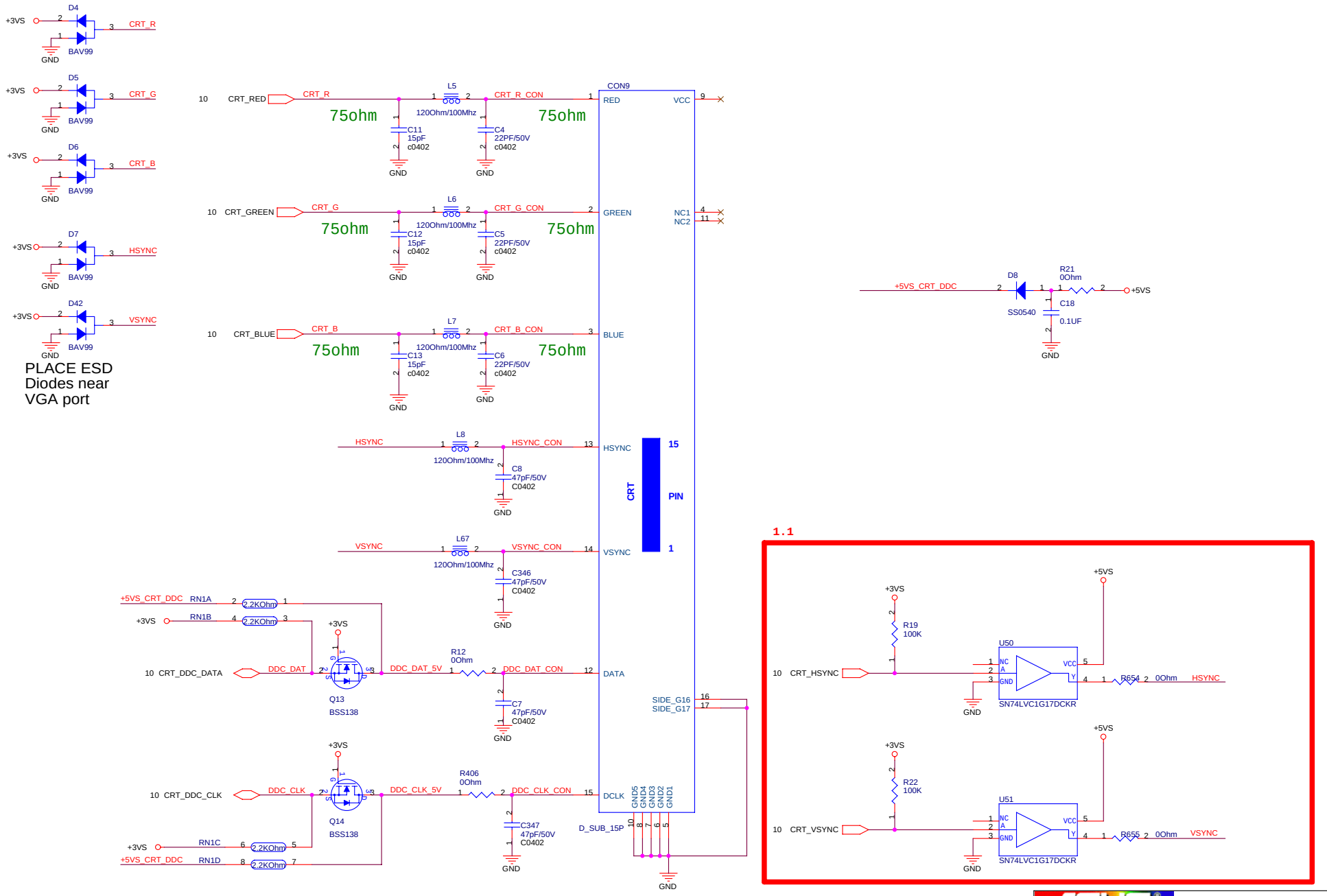


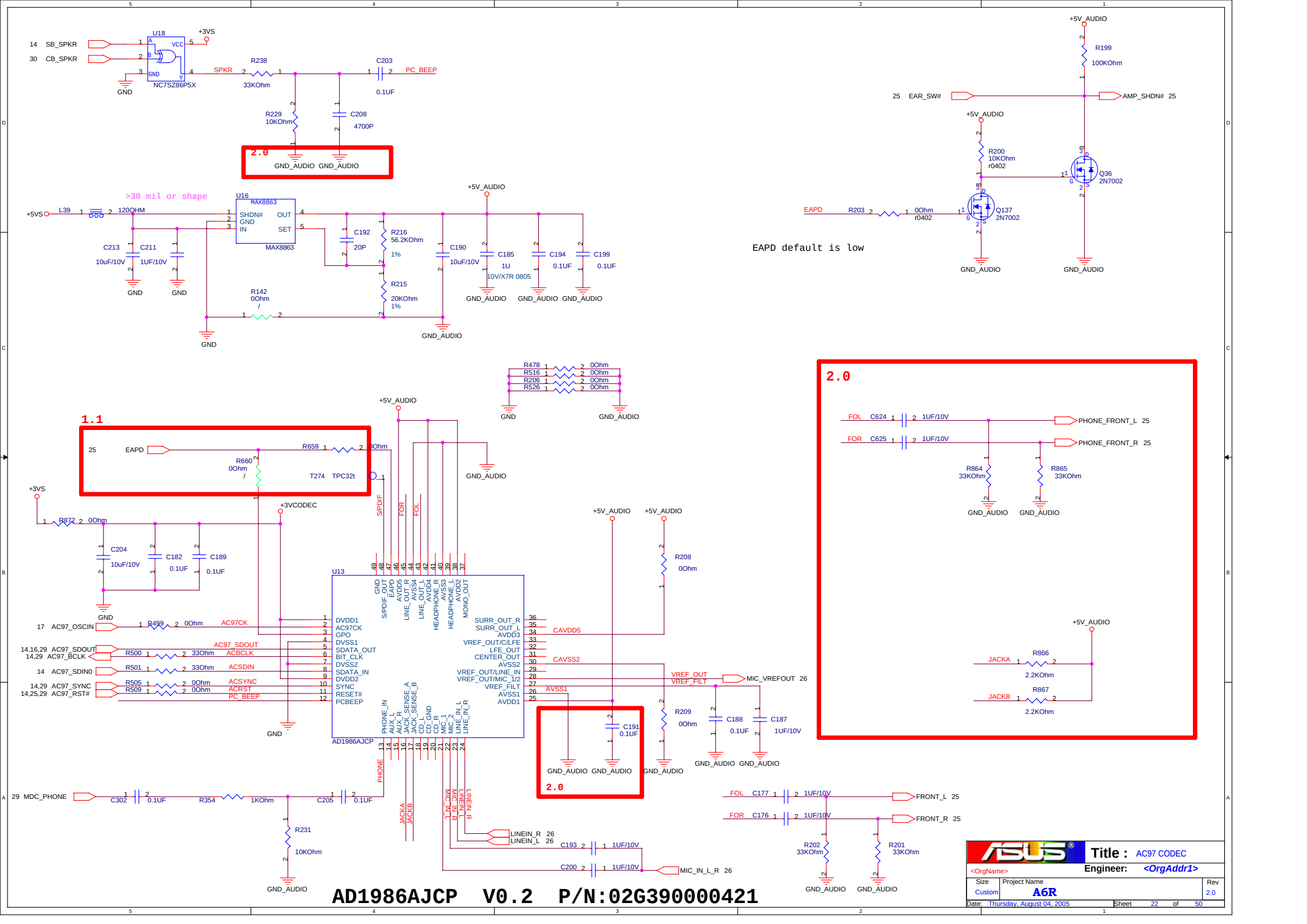
USB PORT 4 for USB CAMERA

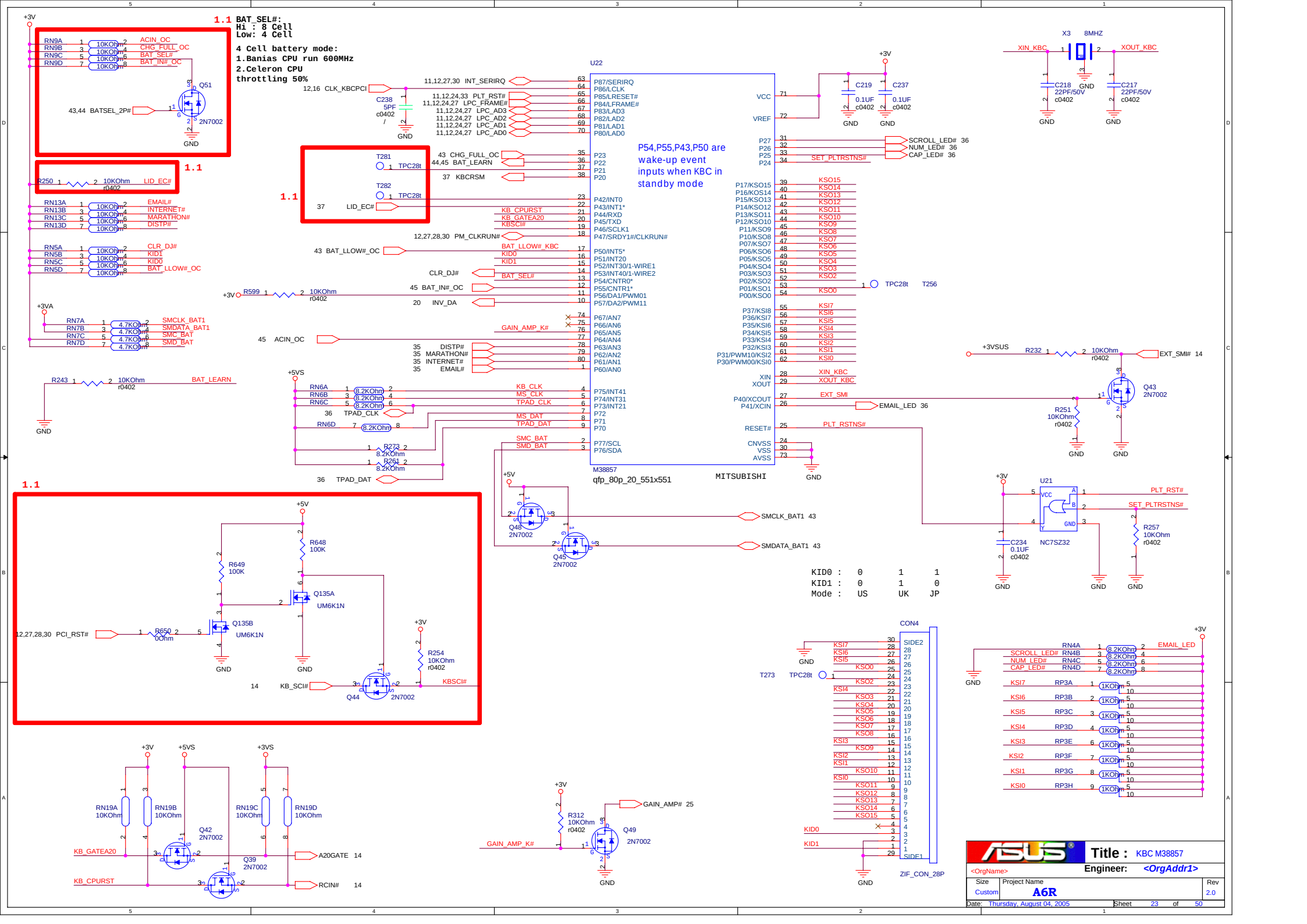
Pin 19 : Add a USB 2.0 Shielding GND cable to USB module.

A6V doesn't support USB WLAN function!

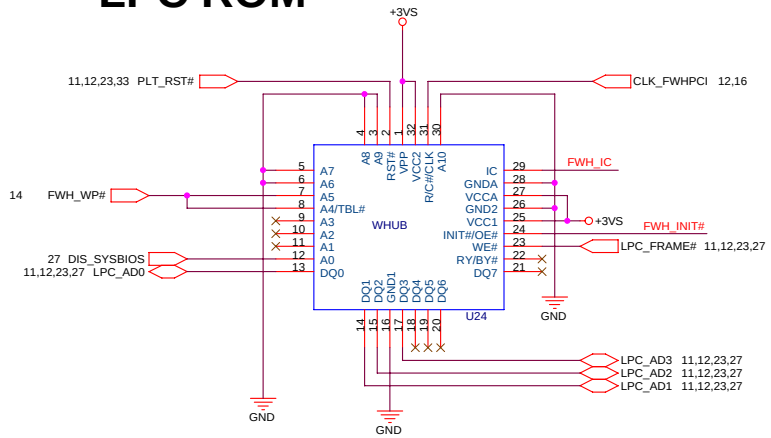
ASUS	Title :	LVDS & INVERTER (CAMERA)
<OrgName>	Engineer:	<OrgAddr1>
Size: Custom	Project Name: A6R	Rev: 2.0
Date: Thursday, August 04, 2005	Sheet 20 of 50	


D4
+3VS
CRT_R
BAV99
GND
D5
CRT_G
D6
CRT_B
D7
HSYNC
D42
VSYNC
PLACE ESD
Diodes near
VGA port
CON9
CRT_RED
CRT_R
CRT_R_CON
RED
VCC
L5
120Ohm/100Mhz
75ohm
C11
15pF
c0402
C4
22PF/50V
c0402
CRT_GREEN
CRT_G
CRT_G_CON
GREEN
NC1
NC2
L6
C12
C5
CRT_BLUE
CRT_B
CRT_B_CON
BLUE
L7
C13
C6
HSYNC
HSYNC_CON
L8
C8
47pF/50V
C0402
VSYNC
VSYNC_CON
L67
C346
CRT
15
PIN
1
+5VS_CRT_DDC
RN1A
RN1B
2.2KOhm
CRT_DDC_DATA
DDC_DAT
DDC_DAT_5V
R12
0Ohm
DDC_DAT_CON
DATA
Q13
BSS138
C7
SIDE_G16
SIDE_G17
CRT_DDC_CLK
DDC_CLK
DDC_CLK_5V
R406
0Ohm
DDC_CLK_CON
DCLK
Q14
RN1C
RN1D
C347
D_SUB_15P
GND5
GND4
GND3
GND2
GND1
D8
SS0540
R21
0Ohm
C18
0.1UF
+5VS
1.1
CRT_HSYNC
R19
100K
U50
SN74LVC1G17DCKR
R654
CRT_VSYNC
R22
U51
R655
Title : TV , CRT CONNECTOR
<OrgName>
Engineer: <OrgAddr1>
Size
Custom
Project Name
A6R
Rev
2.0
Date: Thursday, August 04, 2005
Sheet 21 of 50

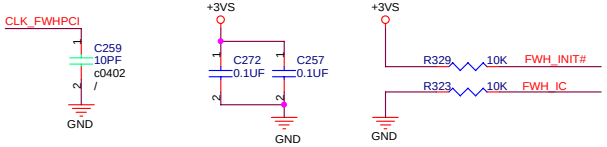

14 SB_SPKR
30 CB_SPKR
U18
NC7SZ86P5X
+3VS
GND
SPKR
R238
33KOhm
C203
0.1UF
PC_BEEP
R229
10KOhm
C208
4700P
2.0
GND_AUDIO
>30 mil or shape
+5VS
L39
120OHM
U16
MAX8863
SHDN#
GND
IN
OUT
SET
C213
10uF/10V
C211
1UF/10V
C192
20P
R216
56.2KOhm
1%
R215
20KOhm
1%
R142
0Ohm
C190
10uF/10V
C185
1U
10V/X7R 0805
C194
0.1UF
C199
0.1UF
+5V_AUDIO
+5V_AUDIO
R199
100KOhm
25 EAR_SW#
AMP_SHDN# 25
R200
10KOhm
r0402
Q36
2N7002
EAPD
R203
0Ohm
r0402
Q137
2N7002
EAPD default is low
GND_AUDIO
R478
R516
R206
R526
0Ohm
1.1
25 EAPD
R659
0Ohm
R660
0Ohm
T274 TPC32t
+3VS
+3VCODEC
R872
0Ohm
C204
10uF/10V
C182
0.1UF
C189
0.1UF
U13
AD1986AJCP
17 AC97_OSCIN
R499
0Ohm
AC97CK
14,16,29 AC97_SDOUT
14,29 AC97_BCLK
R500
33Ohm
ACBCLK
AC97_SDOUT
14 AC97_SDIN0
R501
33Ohm
ACSDIN
14,29 AC97_SYNC
14,25,29 AC97_RST#
R505
0Ohm
R509
0Ohm
ACSYNC
ACRST
PC_BEEP
S/PDIF
FOR
FOL
R208
0Ohm
CAVDD5
CAVSS2
AVSS1
VREF_OUT
VREF_FILT
MIC_VREFOUT 26
R209
0Ohm
C188
0.1UF
C187
1UF/10V
C191
0.1UF
2.0
2.0
FOL C624
1UF/10V
PHONE_FRONT_L 25
FOR C625
1UF/10V
PHONE_FRONT_R 25
R864
33KOhm
R865
33KOhm
JACKA
R866
2.2KOhm
JACKB
R867
2.2KOhm
29 MDC_PHONE
C302
0.1UF
R354
1KOhm
C205
0.1UF
R231
10KOhm
LINEIN_R 26
LINEIN_L 26
C193
1UF/10V
C200
1UF/10V
MIC_IN_L_R 26
FOL C177
1UF/10V
FRONT_L 25
FOR C176
1UF/10V
FRONT_R 25
R202
33KOhm
R201
33KOhm
AD1986AJCP V0.2 P/N:02G390000421
Title : AC97 CODEC
<OrgName>
Engineer: <OrgAddr1>
Size Custom
Project Name A6R
Rev 2.0
Date: Thursday, August 04, 2005
Sheet 22 of 50


1.1 BAT_SEL#:
Hi : 8 Cell
Low: 4 Cell
4 Cell battery mode:
1.Banias CPU run 600MHz
2.Celeron CPU
throttling 50%
P54,P55,P43,P50 are wake-up event inputs when KBC in standby mode
U22
M38857
qfp_80p_20_551x551
MITSUBISHI
X3 8MHZ
U21
NC7SZ32
CON4
ZIF_CON_28P
KID0 : 0 1 1
KID1 : 0 1 0
Mode : US UK JP
Title : KBC M38857
Engineer: <OrgAddr1>
A6R
Thursday, August 04, 2005

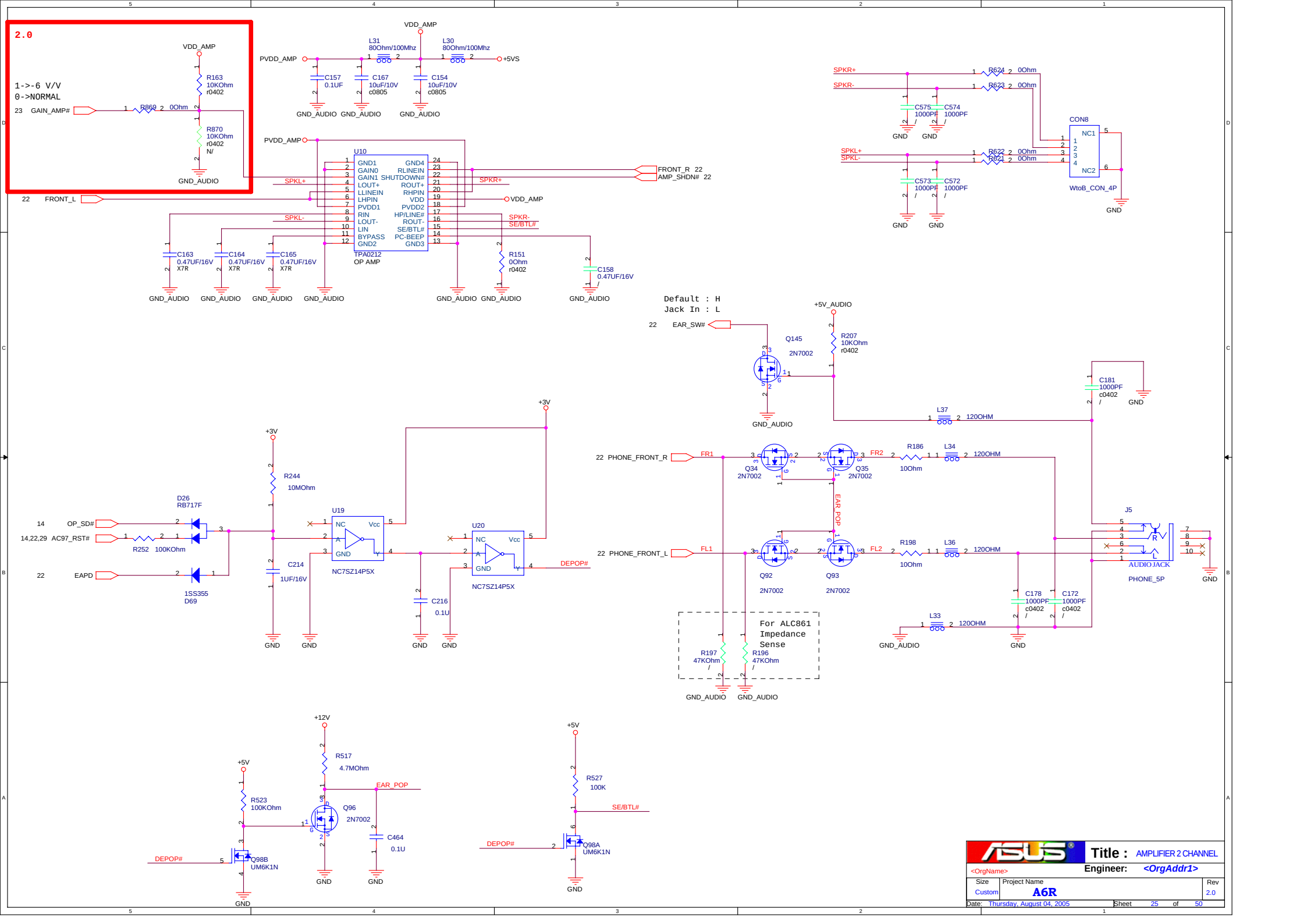
LPC ROM



PLCC32 Socket Part Number :
12-043000321
SST FWH/LPC Part Number :
05-001017122(燒)



Title : FWH			
<OrgName>	Engineer: <OrgAddr1>		
Size: Custom	Project Name: A6R		Rev: 2.0
Date: Thursday, August 04, 2005	Sheet 24 of 50		


2.0
1->-6 V/V
0->NORMAL
23 GAIN_AMP#
R869 0Ohm
R163 10KOhm r0402
R870 10KOhm r0402 N/
VDD_AMP
GND_AUDIO
PVDD_AMP
L31 80Ohm/100Mhz
L30 80Ohm/100Mhz
+5VS
C157 0.1UF
C167 10uF/10V c0805
C154 10uF/10V c0805
U10
TPA0212
OP AMP
GND1 GAIN0 GAIN1 LOUT+ LLINEIN LHPIN PVDD1 RIN LOUT- LIN BYPASS GND2
GND4 RLINEIN SHUTDOWN# ROUT+ RHPIN VDD PVDD2 HP/LINE# ROUT- SE/BTL# PC-BEEP GND3
22 FRONT_L
SPKL+
SPKL-
SPKR+
SPKR-
SE/BTL#
FRONT_R 22
AMP_SHDN# 22
C163 0.47UF/16V X7R
C164 0.47UF/16V X7R
C165 0.47UF/16V X7R
R151 0Ohm r0402
C158 0.47UF/16V
SPKR+
SPKR-
SPKL+
SPKL-
R624 0Ohm
R623 0Ohm
R622 0Ohm
R621 0Ohm
C575 1000PF
C574 1000PF
C573 1000PF
C572 1000PF
CON8
NC1 NC2
WtoB_CON_4P
Default : H
Jack In : L
22 EAR_SW#
Q145 2N7002
R207 10KOhm r0402
+5V_AUDIO
L37 120OHM
C181 1000PF c0402
22 PHONE_FRONT_R
22 PHONE_FRONT_L
FR1
FR2
FL1
FL2
Q34 2N7002
Q35 2N7002
Q92 2N7002
Q93 2N7002
R186 10Ohm
R198 10Ohm
L34 120OHM
L36 120OHM
L33 120OHM
EAR_POP
J5
AUDIO JACK
PHONE_5P
C178 1000PF c0402
C172 1000PF c0402
For ALC861
Impedance
Sense
R197 47KOhm
R196 47KOhm
+3V
R244 10MOhm
D26 RB717F
14 OP_SD#
14,22,29 AC97_RST#
R252 100KOhm
22 EAPD
1SS355 D69
U19
U20
NC7SZ14P5X
C214 1UF/16V
C216 0.1U
DEPOP#
+12V
R517 4.7MOhm
R523 100KOhm
Q96 2N7002
Q98B UM6K1N
C464 0.1U
+5V
R527 100K
Q98A UM6K1N
GND
Title : AMPLIFIER 2 CHANNEL
Engineer: <OrgAddr1>
<OrgName>
Size Custom
Project Name A6R
Rev 2.0
Date: Thursday, August 04, 2005
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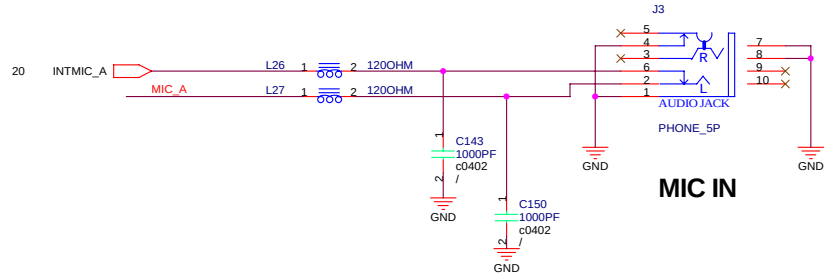
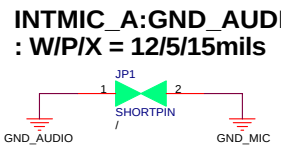
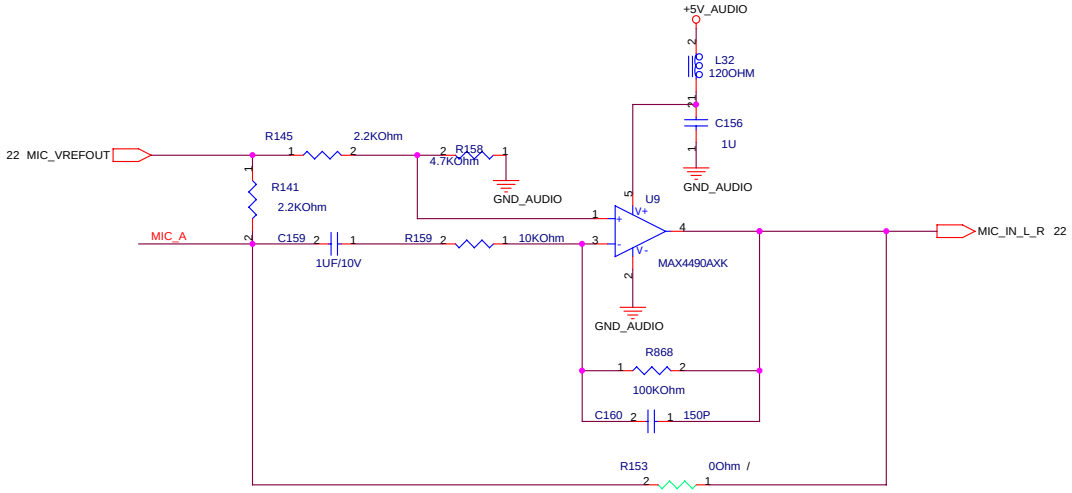
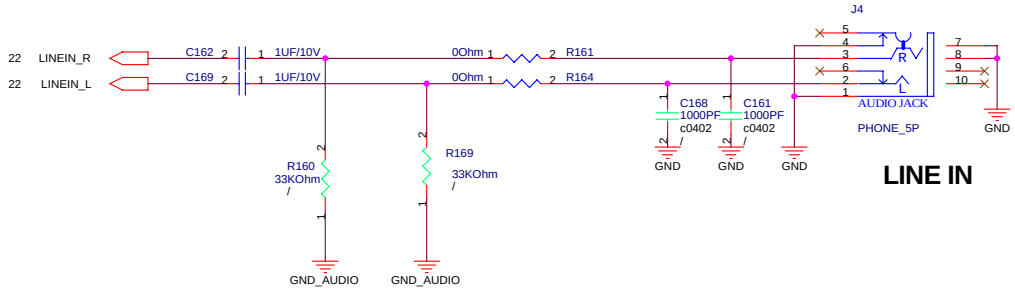
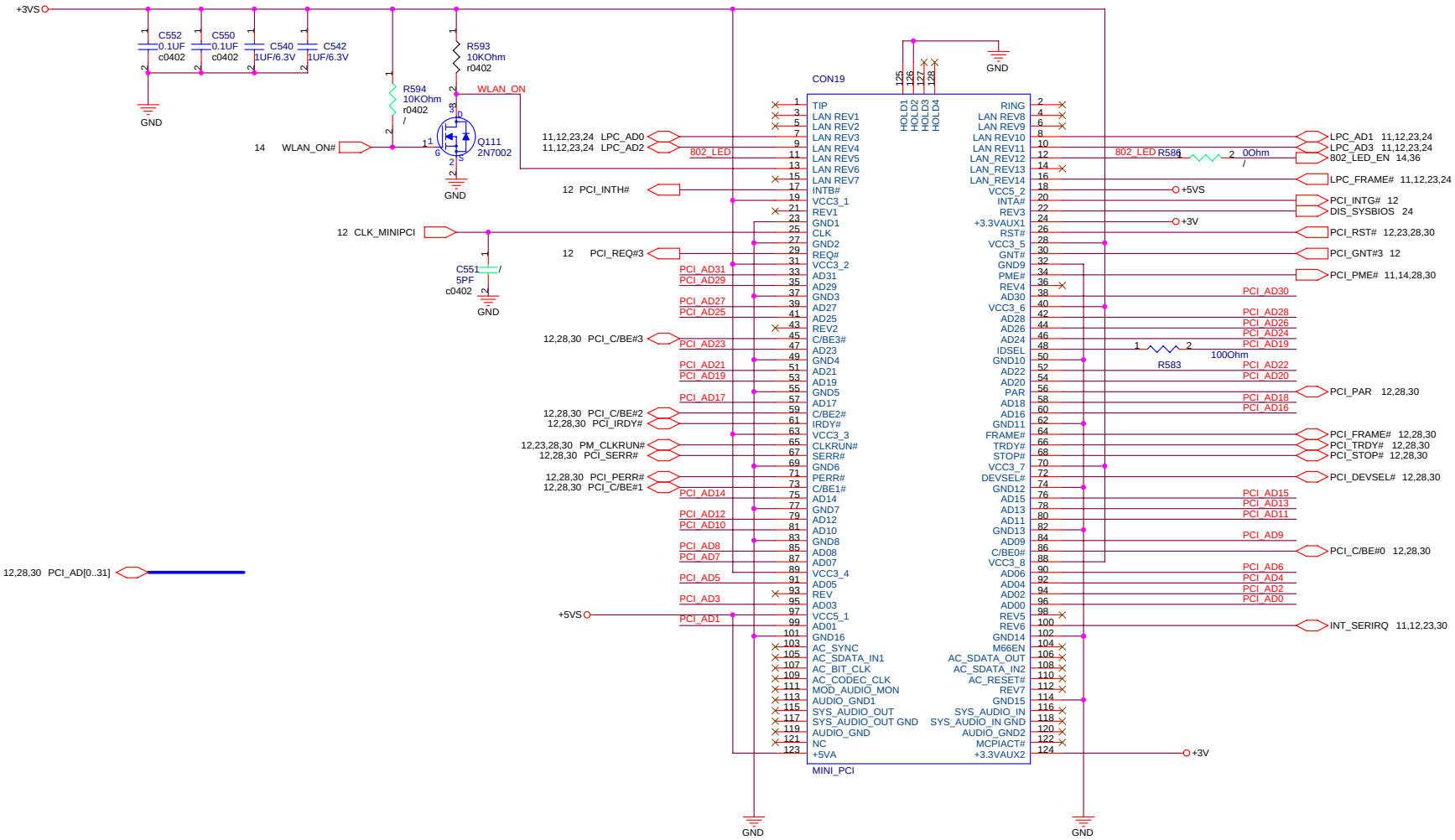




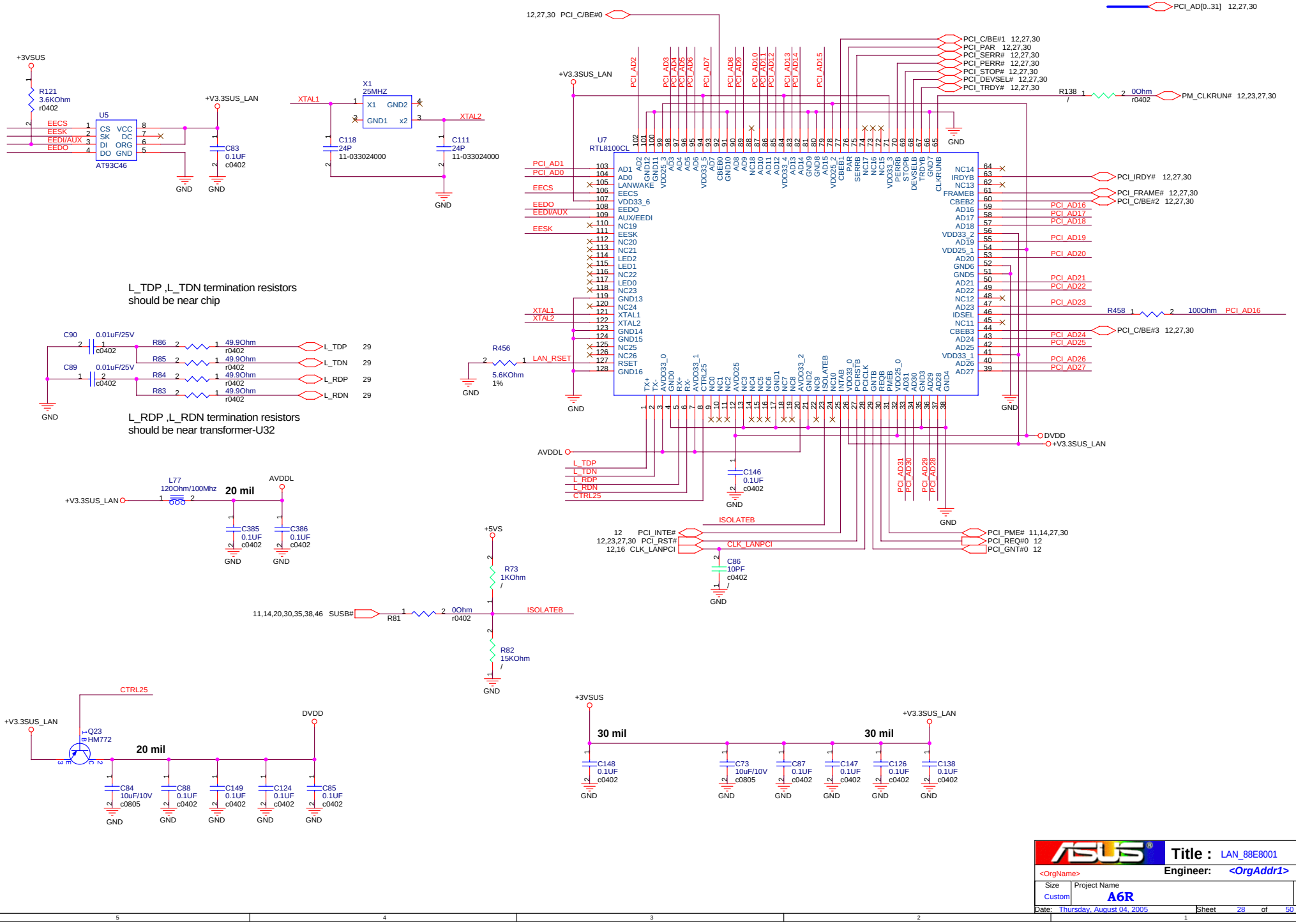


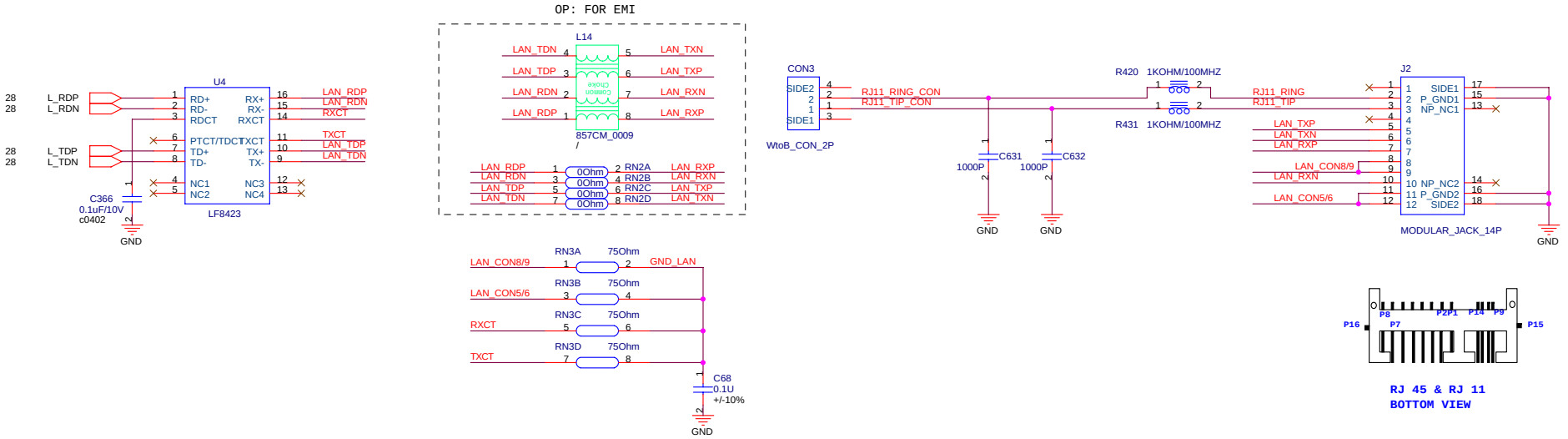


ASUS	Title : MIC,LINE-IN JACK	
<OrgName>	Engineer: <OrgAddr1>	
Size: Custom	Project Name: A6R	Rev: 2.0
Date: Thursday, August 04, 2005	Sheet 26 of 50	



Title : MINIPCI_WIRELESS		
<OrgName>	Engineer: <OrgAddr1>	
Size: Custom	Project Name: A6R	Rev: 2.0
Date: Thursday, August 04, 2005	Sheet 27 of 50	

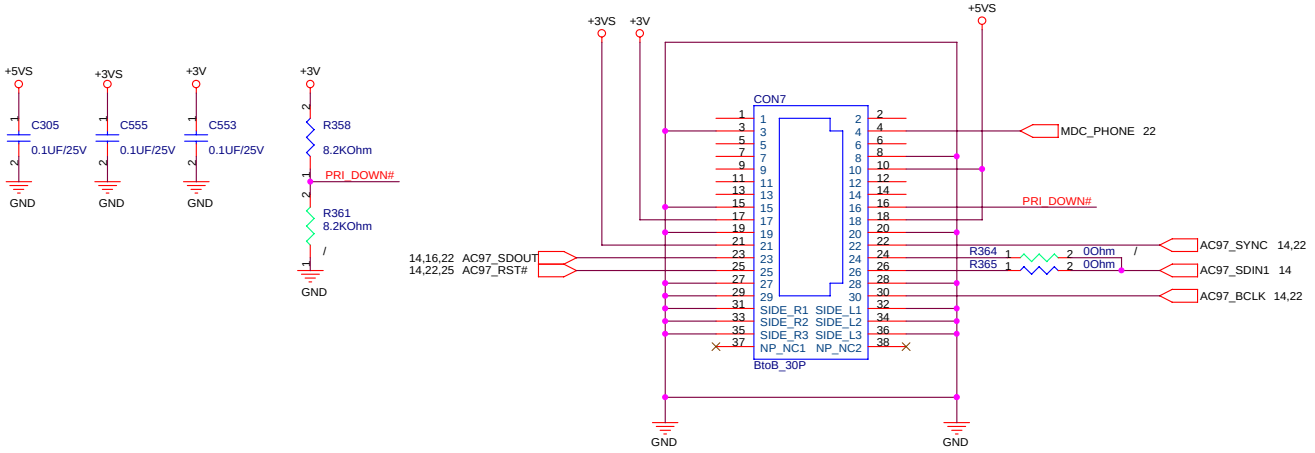

+3VSUS
R121
3.6KOhm
r0402
EECS
EESK
EEDI/AUX
EEDO
U5
CS VCC
SK DC
DI ORG
DO GND
AT93C46
GND
+V3.3SUS_LAN
C83
0.1UF
c0402
XTAL1
X1
25MHZ
X1 GND2
GND1 x2
XTAL2
C118
24P
11-033024000
C111
24P
11-033024000
L_TDP ,L_TDN termination resistors
should be near chip
C90
0.01uF/25V
C89
0.01uF/25V
c0402
R86
R85
R84
R83
49.9Ohm
r0402
L_TDP 29
L_TDN 29
L_RDP 29
L_RDN 29
L_RDP ,L_RDN termination resistors
should be near transformer-U32
L77
120Ohm/100Mhz
20 mil
AVDDL
C385
C386
0.1UF
c0402
12,27,30 PCI_C/BE#0
PCI_AD[0..31] 12,27,30
PCI_C/BE#1 12,27,30
PCI_PAR 12,27,30
PCI_SERR# 12,27,30
PCI_PERR# 12,27,30
PCI_STOP# 12,27,30
PCI_DEVSEL# 12,27,30
PCI_TRDY# 12,27,30
R138
0Ohm
r0402
PM_CLKRUN# 12,23,27,30
U7
RTL8100CL
PCI_IRDY# 12,27,30
PCI_FRAME# 12,27,30
PCI_C/BE#2 12,27,30
PCI_AD16
PCI_AD17
PCI_AD18
PCI_AD19
PCI_AD20
PCI_AD21
PCI_AD22
PCI_AD23
PCI_AD24
PCI_AD25
PCI_AD26
PCI_AD27
R458
100Ohm
PCI_C/BE#3 12,27,30
R456
5.6KOhm
1%
LAN_RSET
DVDD
+V3.3SUS_LAN
C146
0.1UF
c0402
ISOLATEB
12 PCI_INTE#
12,23,27,30 PCI_RST#
12,16 CLK_LANPCI
CLK_LANPCI
C86
10PF
c0402
PCI_PME# 11,14,27,30
PCI_REQ#0 12
PCI_GNT#0 12
+5VS
R73
1KOhm
11,14,20,30,35,38,46 SUSB#
R81
0Ohm
r0402
R82
15KOhm
CTRL25
Q23
HM772
20 mil
C84
10uF/10V
c0805
C88
C149
C124
C85
0.1UF
c0402
30 mil
C148
C73
10uF/10V
c0805
C87
C147
C126
C138
0.1UF
c0402
GND
Title : LAN_88E8001
<OrgName>
Engineer: <OrgAddr1>
Size Custom
Project Name A6R
Rev 2.0
Date: Thursday, August 04, 2005
Sheet 28 of 50



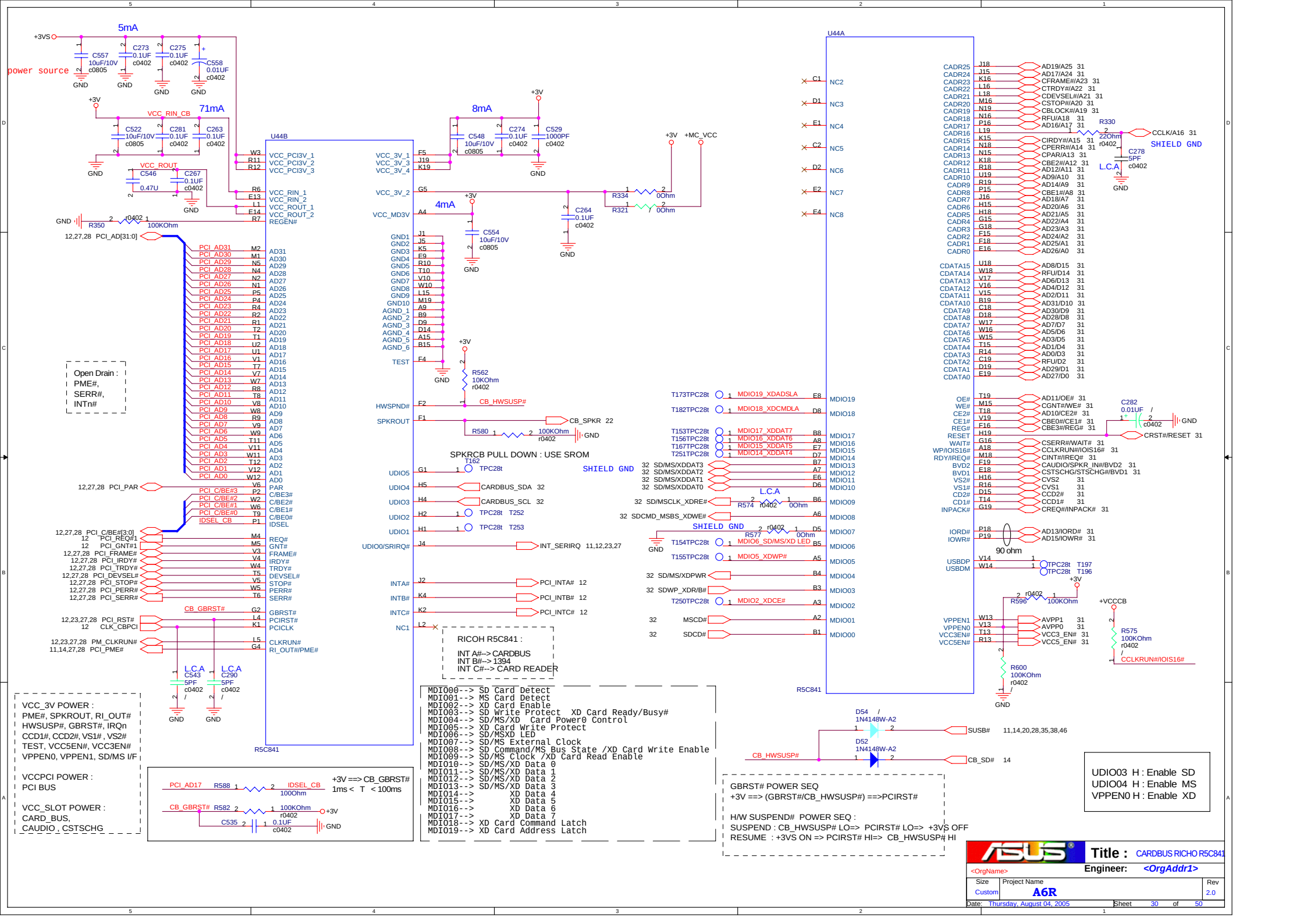
RJ 45 & RJ 11
BOTTOM VIEW

LAN PORT

MDC



ASUS	Title : RJ11+45 & MDC	
<OrgName>	Engineer: <OrgAddr1>	
Size: Custom	Project Name: A6R	Rev: 2.0
Date: Thursday, August 04, 2005	Sheet 29 of 50	


5mA
power source
+3VS
C557 10uF/10V c0805
C273 0.1UF c0402
C275 0.1UF c0402
C558 0.01UF c0402
GND
71mA
VCC_RIN_CB
C522 10uF/10V c0805
C281 0.1UF c0402
C263 0.1UF c0402
VCC_ROUT
C546 0.47U
C267 0.1UF c0402
R350 100KOhm
12,27,28 PCI_AD[31:0]
PCI_AD31 PCI_AD30 PCI_AD29 PCI_AD28 PCI_AD27 PCI_AD26 PCI_AD25 PCI_AD24 PCI_AD23 PCI_AD22 PCI_AD21 PCI_AD20 PCI_AD19 PCI_AD18 PCI_AD17 PCI_AD16 PCI_AD15 PCI_AD14 PCI_AD13 PCI_AD12 PCI_AD11 PCI_AD10 PCI_AD9 PCI_AD8 PCI_AD7 PCI_AD6 PCI_AD5 PCI_AD4 PCI_AD3 PCI_AD2 PCI_AD1 PCI_AD0
12,27,28 PCI_PAR
PCI_C/BE#3 PCI_C/BE#2 PCI_C/BE#1 PCI_C/BE#0 IDSEL_CB
12,27,28 PCI_C/BE#[3:0]
12 PCI_REQ#1
12 PCI_GNT#1
12,27,28 PCI_FRAME#
12,27,28 PCI_IRDY#
12,27,28 PCI_TRDY#
12,27,28 PCI_DEVSEL#
12,27,28 PCI_STOP#
12,27,28 PCI_PERR#
12,27,28 PCI_SERR#
CB_GBRST#
12,23,27,28 PCI_RST#
12 CLK_CBPCI
12,23,27,28 PM_CLKRUN#
11,14,27,28 PCI_PME#
L.C.A C543 5PF c0402
L.C.A C290 5PF c0402
U44B
VCC_PCI3V_1 VCC_PCI3V_2 VCC_PCI3V_3
VCC_RIN_1 VCC_RIN_2 VCC_ROUT_1 VCC_ROUT_2 REGEN#
AD31 AD30 AD29 AD28 AD27 AD26 AD25 AD24 AD23 AD22 AD21 AD20 AD19 AD18 AD17 AD16 AD15 AD14 AD13 AD12 AD11 AD10 AD9 AD8 AD7 AD6 AD5 AD4 AD3 AD2 AD1 AD0
PAR C/BE3# C/BE2# C/BE1# C/BE0# IDSEL
REQ# GNT# FRAME# IRDY# TRDY# DEVSEL# STOP# PERR# SERR#
GBRST# PCIRST# PCICLK
CLKRUN# RI_OUT#/PME#
R5C841
VCC_3V_1 VCC_3V_3 VCC_3V_4
VCC_3V_2
VCC_MD3V
GND1 GND2 GND3 GND4 GND5 GND6 GND7 GND8 GND9 GND10
AGND_1 AGND_2 AGND_3 AGND_4 AGND_5 AGND_6
TEST
HWSPND#
SPKROUT
UDIO5 UDIO4 UDIO3 UDIO2 UDIO1
UDIO0/SRIRQ#
INTA# INTB# INTC#
NC1
8mA
C548 10uF/10V c0805
C274 0.1UF c0402
C529 1000PF c0402
4mA
C554 10uF/10V c0805
C264 0.1UF c0402
+MC_VCC
R334 0Ohm
R321 0Ohm
R562 10KOhm r0402
CB_HWSUSP#
R580 100KOhm r0402
CB_SPKR 22
SPKRCB PULL DOWN : USE SROM
T162 TPC28t
UDIO5 CARDBUS_SDA 32
UDIO4 CARDBUS_SCL 32
UDIO3 TPC28t T252
UDIO2 TPC28t T253
UDIO0/SRIRQ# INT_SERIRQ 11,12,23,27
INTA# PCI_INTA# 12
INTB# PCI_INTB# 12
INTC# PCI_INTC# 12
RICOH R5C841 :
INT A#--> CARDBUS
INT B#--> 1394
INT C#--> CARD READER
Open Drain : PME#, SERR#, INTn#
VCC_3V POWER : PME#, SPKROUT, RI_OUT# HWSUSP#, GBRST#, IRQn CCD1#, CCD2#, VS1# , VS2# TEST, VCC5EN#, VCC3EN# VPPEN0, VPPEN1, SD/MS I/F
VCCPCI POWER : PCI BUS
VCC_SLOT POWER : CARD_BUS, CAUDIO , CSTSCHG
PCI_AD17 R588 100Ohm IDSEL_CB
CB_GBRST# R582 100KOhm r0402 +3V
C535 0.1UF c0402 GND
+3V ==> CB_GBRST# 1ms < T < 100ms
MDIO000--> SD Card Detect
MDIO001--> MS Card Detect
MDIO002--> XD Card Enable
MDIO003--> SD Write Protect XD Card Ready/Busy#
MDIO004--> SD/MS/XD Card Power0 Control
MDIO005--> XD Card Write Protect
MDIO006--> SD/MSXD LED
MDIO007--> SD/MS External Clock
MDIO008--> SD Command/MS Bus State /XD Card Write Enable
MDIO009--> SD/MS Clock /XD Card Read Enable
MDIO010--> SD/MS/XD Data 0
MDIO011--> SD/MS/XD Data 1
MDIO012--> SD/MS/XD Data 2
MDIO013--> SD/MS/XD Data 3
MDIO014--> XD Data 4
MDIO015--> XD Data 5
MDIO016--> XD Data 6
MDIO017--> XD Data 7
MDIO018--> XD Card Command Latch
MDIO019--> XD Card Address Latch
U44A
NC1 NC2 NC3 NC4 NC5 NC6 NC7 NC8
MDIO19 MDIO18 MDIO17 MDIO16 MDIO15 MDIO14 MDIO13 MDIO12 MDIO11 MDIO10 MDIO09 MDIO08 MDIO07 MDIO06 MDIO05 MDIO04 MDIO03 MDIO02 MDIO01 MDIO00
T173TPC28t MDIO19_XDADSLA
T182TPC28t MDIO18_XDCMDLA
T153TPC28t MDIO17_XDDAT7
T156TPC28t MDIO16_XDDAT6
T167TPC28t MDIO15_XDDAT5
T251TPC28t MDIO14_XDDAT4
32 SD/MS/XDDAT3
32 SD/MS/XDDAT2
32 SD/MS/XDDAT1
32 SD/MS/XDDAT0
SHIELD GND
L.C.A
32 SD/MSCLK_XDRE# R574 0Ohm
32 SDCMD_MSBS_XDWE#
SHIELD GND R577 0Ohm MDIO6_SD/MS/XD LED
T154TPC28t MDIO6_SD/MS/XD LED
T155TPC28t MDIO5_XDWP#
32 SD/MS/XDPWR
32 SDWP_XDR/B#
T250TPC28t MDIO2_XDCE#
32 MSCD#
32 SDCD#
CADR25 CADR24 CADR23 CADR22 CADR21 CADR20 CADR19 CADR18 CADR17 CADR16 CADR15 CADR14 CADR13 CADR12 CADR11 CADR10 CADR9 CADR8 CADR7 CADR6 CADR5 CADR4 CADR3 CADR2 CADR1 CADR0
AD19/A25 AD17/A24 CFRAME#/A23 CTRDY#/A22 CDEVSEL#/A21 CSTOP#/A20 CBLOCK#/A19 RFU/A18 AD16/A17 CIRDY#/A15 CPERR#/A14 CPAR/A13 CBE2#/A12 AD12/A11 AD9/A10 AD14/A9 CBE1#/A8 AD18/A7 AD20/A6 AD21/A5 AD22/A4 AD23/A3 AD24/A2 AD25/A1 AD26/A0
R330 22Ohm r0402
CCLK/A16 31
SHIELD GND
C278 5PF c0402
L.C.A
GND
CDATA15 CDATA14 CDATA13 CDATA12 CDATA11 CDATA10 CDATA9 CDATA8 CDATA7 CDATA6 CDATA5 CDATA4 CDATA3 CDATA2 CDATA1 CDATA0
AD8/D15 RFU/D14 AD6/D13 AD4/D12 AD2/D11 AD31/D10 AD30/D9 AD28/D8 AD7/D7 AD5/D6 AD3/D5 AD1/D4 AD0/D3 RFU/D2 AD29/D1 AD27/D0
OE# WE# CE2# CE1# REG# RESET WAIT# WP/IOIS16# RDY/IREQ# BVD2 BVD1 VS2# VS1# CD2# CD1# INPACK#
AD11/OE# CGNT#/WE# AD10/CE2# CBE0#/CE1# CBE3#/REG# CRST#/RESET CSERR#/WAIT# CCLKRUN#/IOIS16# CINT#/IREQ# CAUDIO/SPKR_IN#/BVD2 CSTSCHG/STSCHG#/BVD1 CVS2 CVS1 CCD2# CCD1# CREQ#/INPACK#
C282 0.01UF c0402 GND
IORD# IOWR#
AD13/IORD# AD15/IOWR#
90 ohm
USBDP USBDM
TPC28t T197
TPC28t T196
+3V
R596 100KOhm r0402
+VCCCB
VPPEN1 VPPEN0 VCC3EN# VCC5EN#
AVPP1 AVPP0 VCC3_EN# VCC5_EN#
R575 100KOhm r0402 CCLKRUN#/IOIS16#
R600 100KOhm r0402
R5C841
D54 1N4148W-A2
D52 1N4148W-A2
CB_HWSUSP#
SUSB# 11,14,20,28,35,38,46
CB_SD# 14
GBRST# POWER SEQ
+3V ==> (GBRST#/CB_HWSUSP#) ==>PCIRST#
H/W SUSPEND# POWER SEQ :
SUSPEND : CB_HWSUSP# LO=> PCIRST# LO=> +3VS OFF
RESUME : +3VS ON => PCIRST# HI=> CB_HWSUSP# HI
UDIO03 H : Enable SD
UDIO04 H : Enable MS
VPPEN0 H : Enable XD
Title : CARDBUS RICHO R5C841
<OrgName>
Engineer: <OrgAddr1>
Size Custom
Project Name A6R
Rev 2.0
Date: Thursday, August 04, 2005
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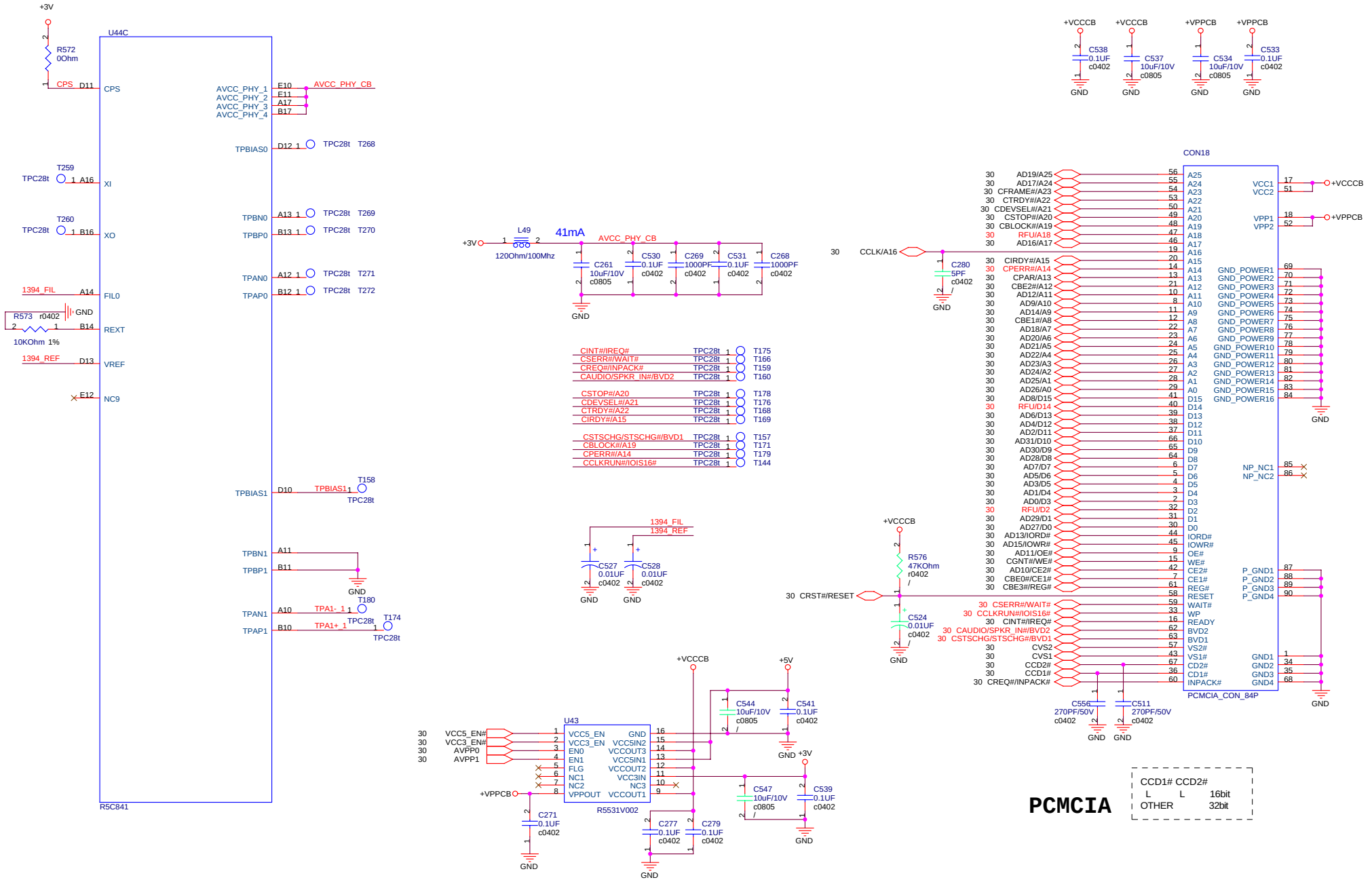
+3V
R572
0Ohm
U44C
CPS D11
CPS
XI
XO
FIL0
REXT
VREF
NC9
1394_FIL
R573 r0402
10KOhm 1%
1394_REF
T259
T260
TPC28t
AVCC_PHY_1
AVCC_PHY_2
AVCC_PHY_3
AVCC_PHY_4
AVCC_PHY_CB
TPBIAS0
TPBN0
TPBP0
TPAN0
TPAP0
TPBIAS1
TPBIAS1
TPBN1
TPBP1
TPAN1
TPAP1
TPA1-
TPA1+
R5C841
L49
41mA
120Ohm/100Mhz
C261 10uF/10V c0805
C530 0.1UF c0402
C269 1000PF c0402
C531 0.1UF c0402
C268 1000PF c0402
GND
CINT#/IREQ#
CSERR#/WAIT#
CREQ#/INPACK#
CAUDIO/SPKR_IN#/BVD2
CSTOP#/A20
CDEVSEL#/A21
CTRDY#/A22
CIRDY#/A15
CSTSCHG/STSCHG#/BVD1
CBLOCK#/A19
CPERR#/A14
CCLKRUN#/IOIS16#
T175
T166
T159
T160
T178
T176
T168
T169
T157
T171
T179
T144
C527 0.01UF c0402
C528 0.01UF c0402
T180
T174
U43
VCC5_EN#
VCC3_EN#
AVPP0
AVPP1
+VPPCB
VCC5_EN
VCC3_EN
EN0
EN1
FLG
NC1
NC2
VPPOUT
GND
VCC5IN2
VCCOUT3
VCC5IN1
VCCOUT2
VCC3IN
NC3
VCCOUT1
R5531V002
C271 0.1UF c0402
C277 0.1UF c0402
C279 0.1UF c0402
C544 10uF/10V c0805
C541 0.1UF c0402
C547 10uF/10V c0805
C539 0.1UF c0402
+5V
+VCCCB
+VCCCB
+VPPCB
+VPPCB
C538 0.1UF c0402
C537 10uF/10V c0805
C534 10uF/10V c0805
C533 0.1UF c0402
CON18
CCLK/A16
C280 5PF c0402
CRST#/RESET
R576 47KOhm r0402
C524 0.01UF c0402
AD19/A25
AD17/A24
CFRAME#/A23
CTRDY#/A22
CDEVSEL#/A21
CSTOP#/A20
CBLOCK#/A19
RFU/A18
AD16/A17
CIRDY#/A15
CPERR#/A14
CPAR/A13
CBE2#/A12
AD12/A11
AD9/A10
AD14/A9
CBE1#/A8
AD18/A7
AD20/A6
AD21/A5
AD22/A4
AD23/A3
AD24/A2
AD25/A1
AD26/A0
AD8/D15
RFU/D14
AD6/D13
AD4/D12
AD2/D11
AD31/D10
AD30/D9
AD28/D8
AD7/D7
AD5/D6
AD3/D5
AD1/D4
AD0/D3
RFU/D2
AD29/D1
AD27/D0
AD13/IORD#
AD15/IOWR#
AD11/OE#
CGNT#/WE#
AD10/CE2#
CBE0#/CE1#
CBE3#/REG#
CSERR#/WAIT#
CCLKRUN#/IOIS16#
CINT#/IREQ#
CAUDIO/SPKR_IN#/BVD2
CSTSCHG/STSCHG#/BVD1
CVS2
CVS1
CCD2#
CCD1#
CREQ#/INPACK#
A25
A24
A23
A22
A21
A20
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A17
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A15
A14
A13
A12
A11
A10
A9
A8
A7
A6
A5
A4
A3
A2
A1
A0
D15
D14
D13
D12
D11
D10
D9
D8
D7
D6
D5
D4
D3
D2
D1
D0
IORD#
IOWR#
OE#
WE#
CE2#
CE1#
REG#
RESET
WAIT#
WP
READY
BVD2
BVD1
VS2#
VS1#
CD2#
CD1#
INPACK#
VCC1
VCC2
VPP1
VPP2
GND_POWER1
GND_POWER2
GND_POWER3
GND_POWER4
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GND_POWER7
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GND_POWER9
GND_POWER10
GND_POWER11
GND_POWER12
GND_POWER13
GND_POWER14
GND_POWER15
GND_POWER16
NP_NC1
NP_NC2
P_GND1
P_GND2
P_GND3
P_GND4
GND1
GND2
GND3
GND4
PCMCIA_CON_84P
C556 270PF/50V c0402
C511 270PF/50V c0402
PCMCIA
CCD1# CCD2#
L L 16bit
OTHER 32bit
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<OrgName>
Engineer: <OrgAddr1>
Size Custom
Project Name A6R
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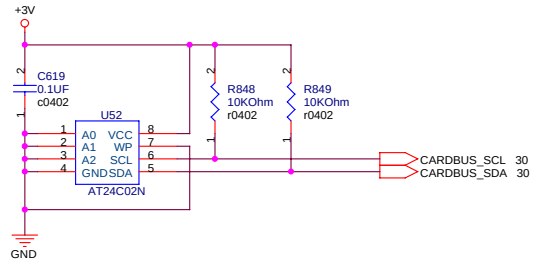
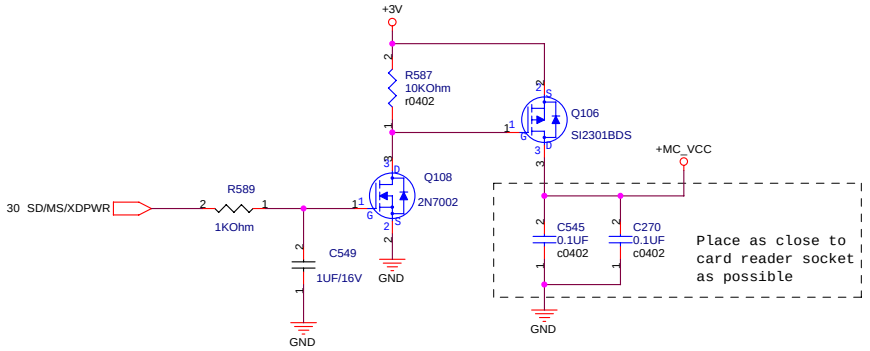
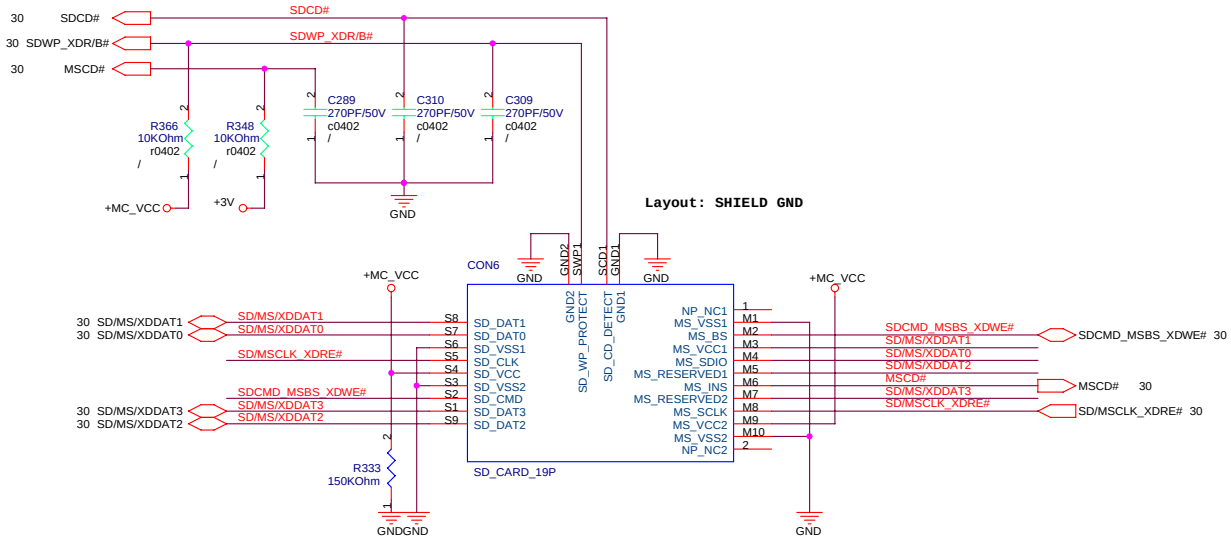


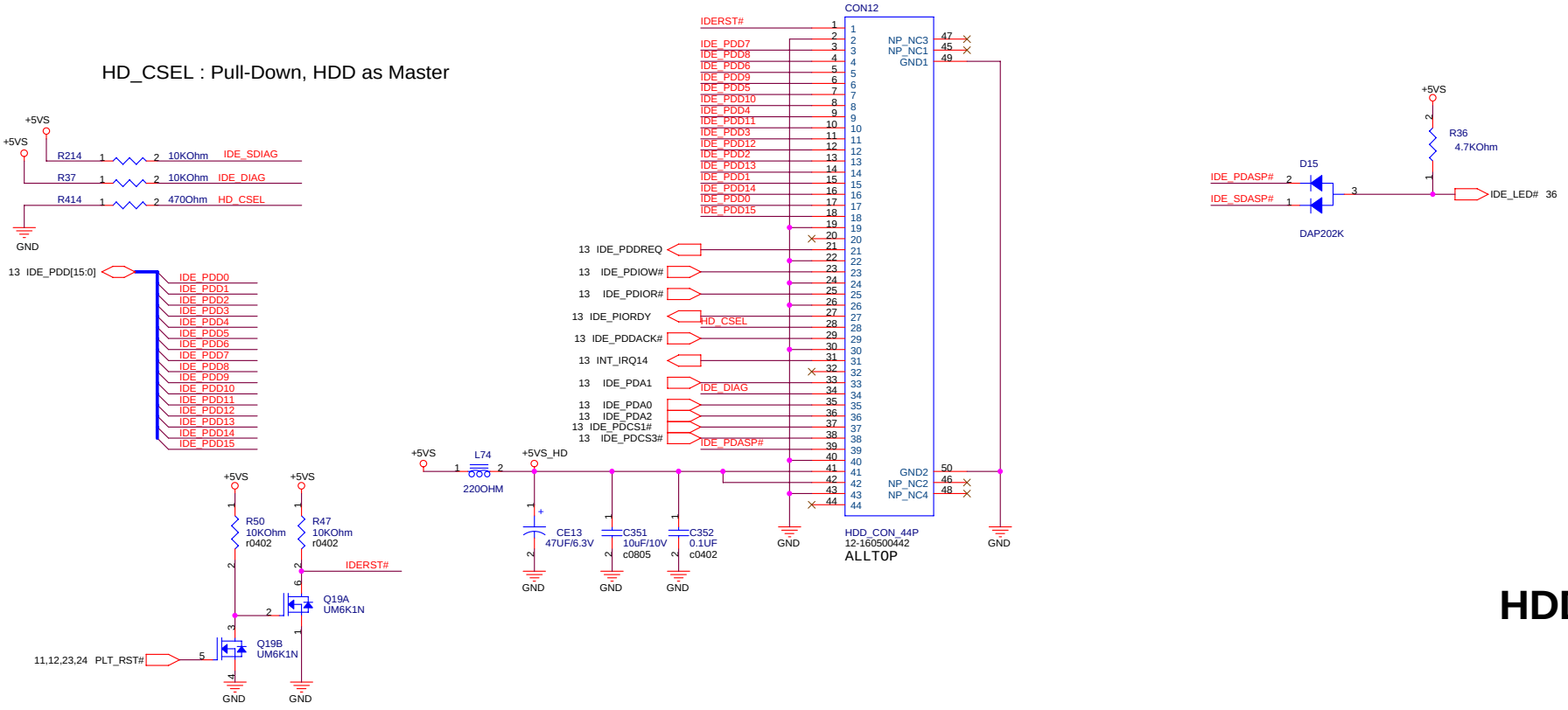




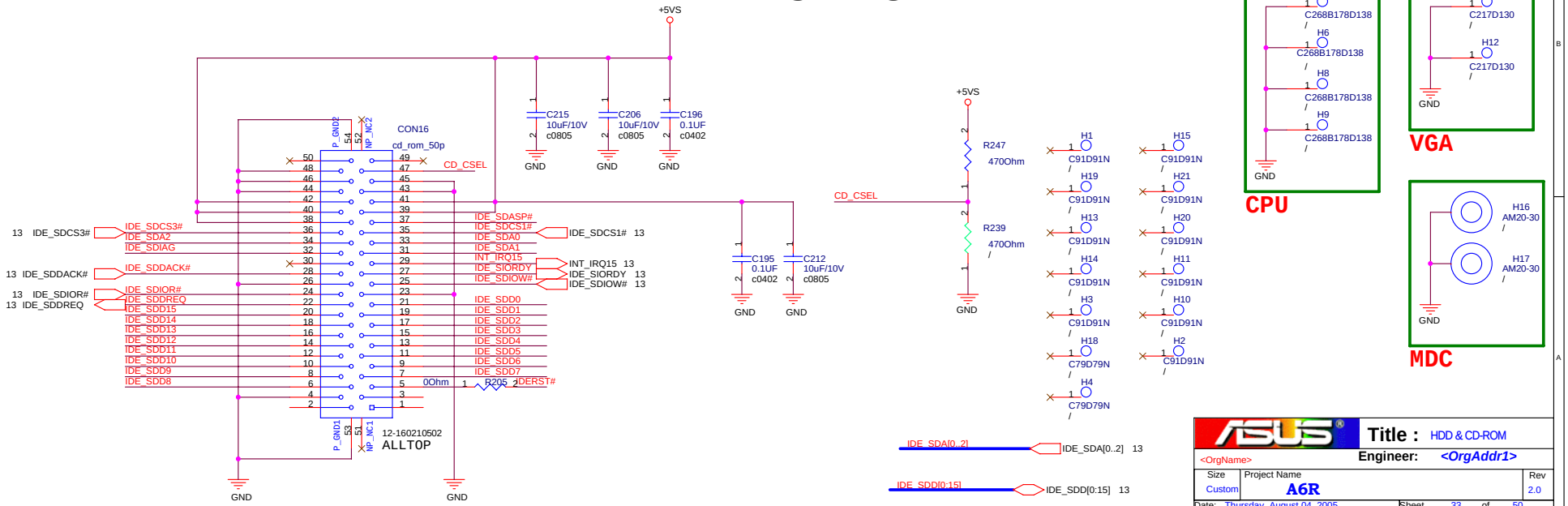
ASUS	Title : IEEE 1394 & 4 IN 1 CON		
<OrgName>	Engineer: <OrgAddr1>		
Size: Custom	Project Name: A6R		Rev: 2.0
Date: Thursday, August 04, 2005	Sheet 32 of 50		

HDD

HD_CSEL : Pull-Down, HDD as Master



CD-ROM



Title :	HDD & CD-ROM	
<OrgName>	Engineer:	<OrgAddr1>
Size: Custom	Project Name: A6R	Rev: 2.0
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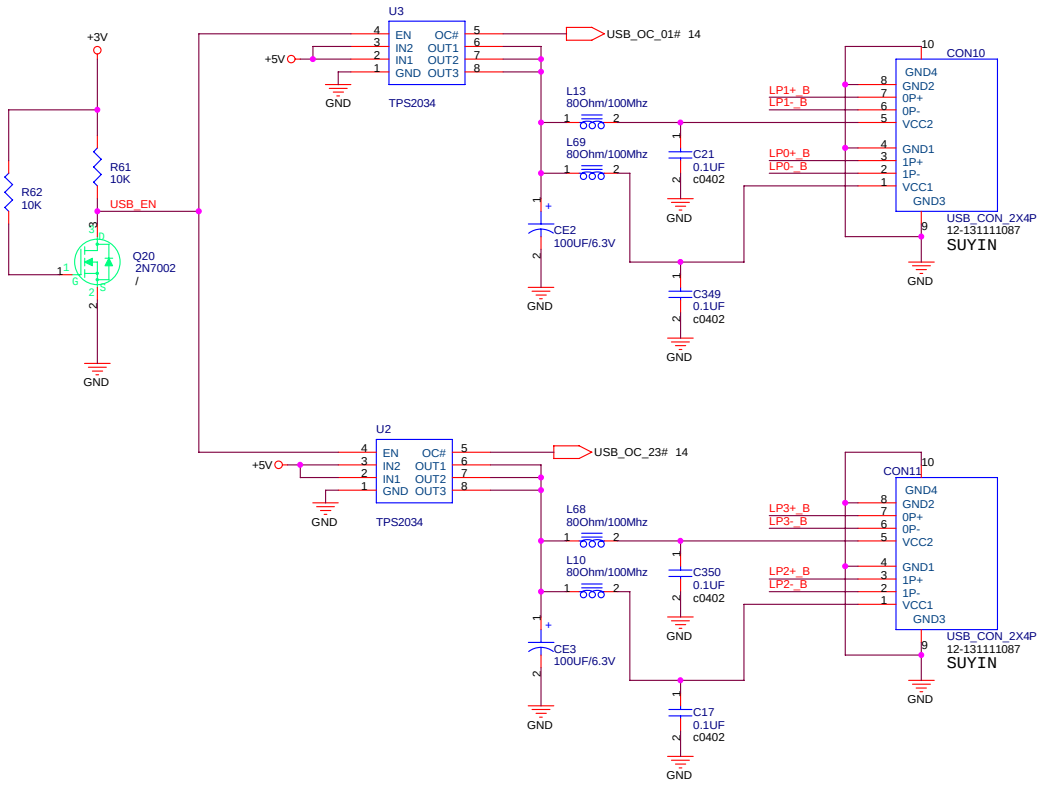
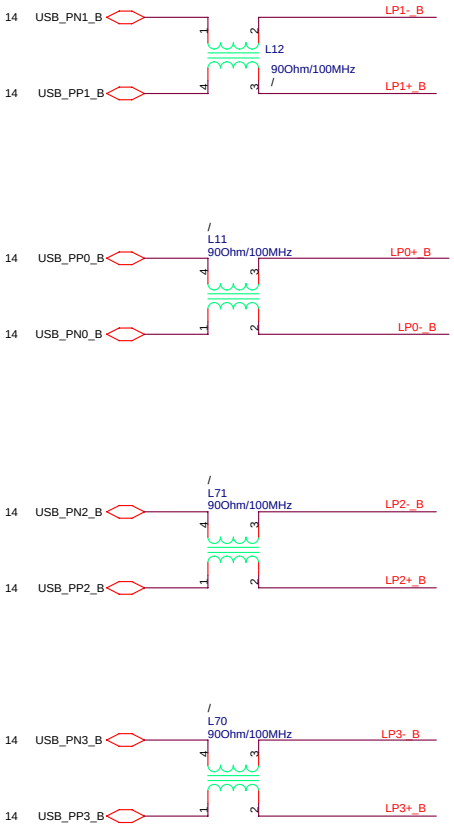
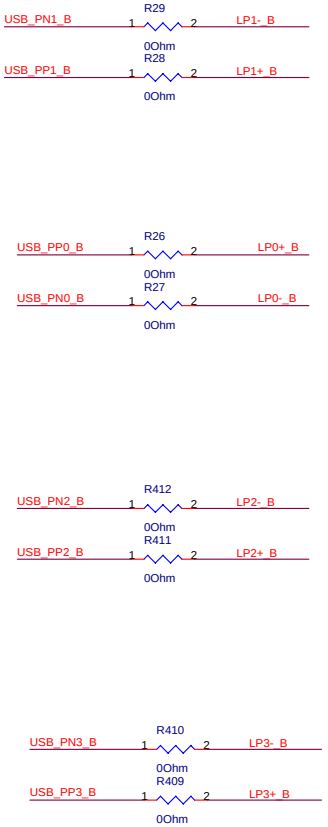
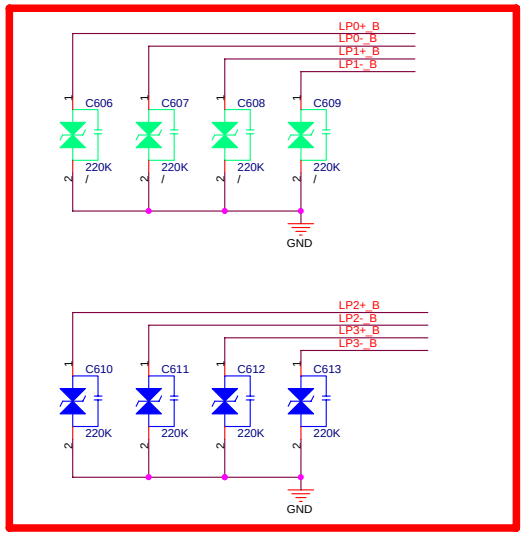
USB









1.1

ASUS	Title : USB	
<OrgName>	Engineer: <OrgAddr1>	
Size: Custom	Project Name: A6R	Rev: 2.0
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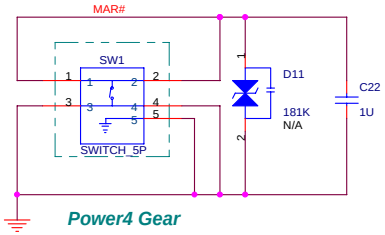
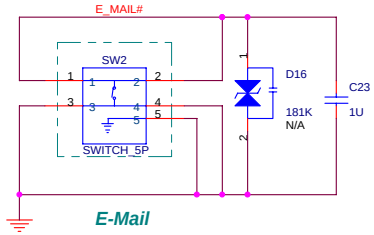
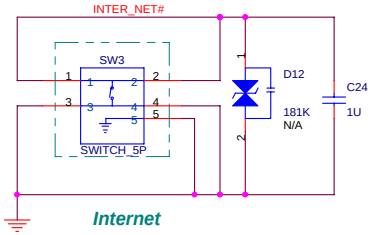
FUNCTION KEY



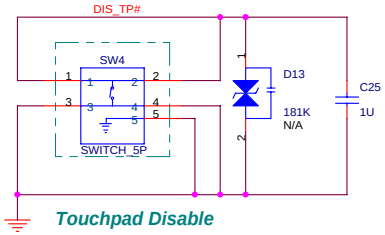
Power4 Gear



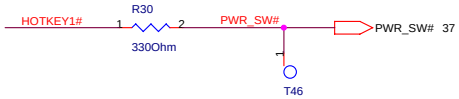
E-Mail

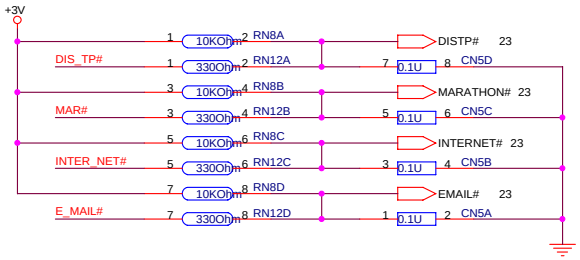


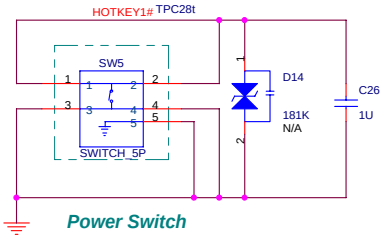
Internet



Touchpad Disable

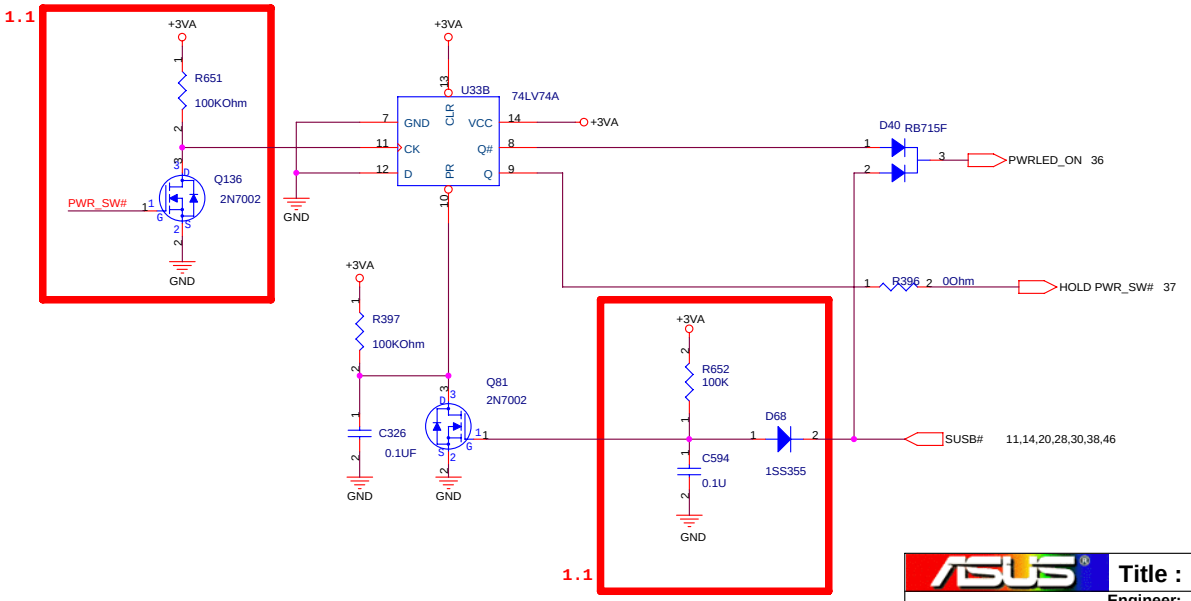


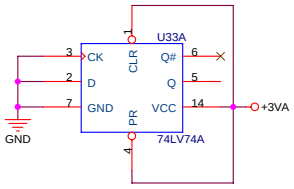




Power Switch

Uses 5-pin switch to improve ESD margin.





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Size: Custom	Project Name: A6R	Rev: 2.0
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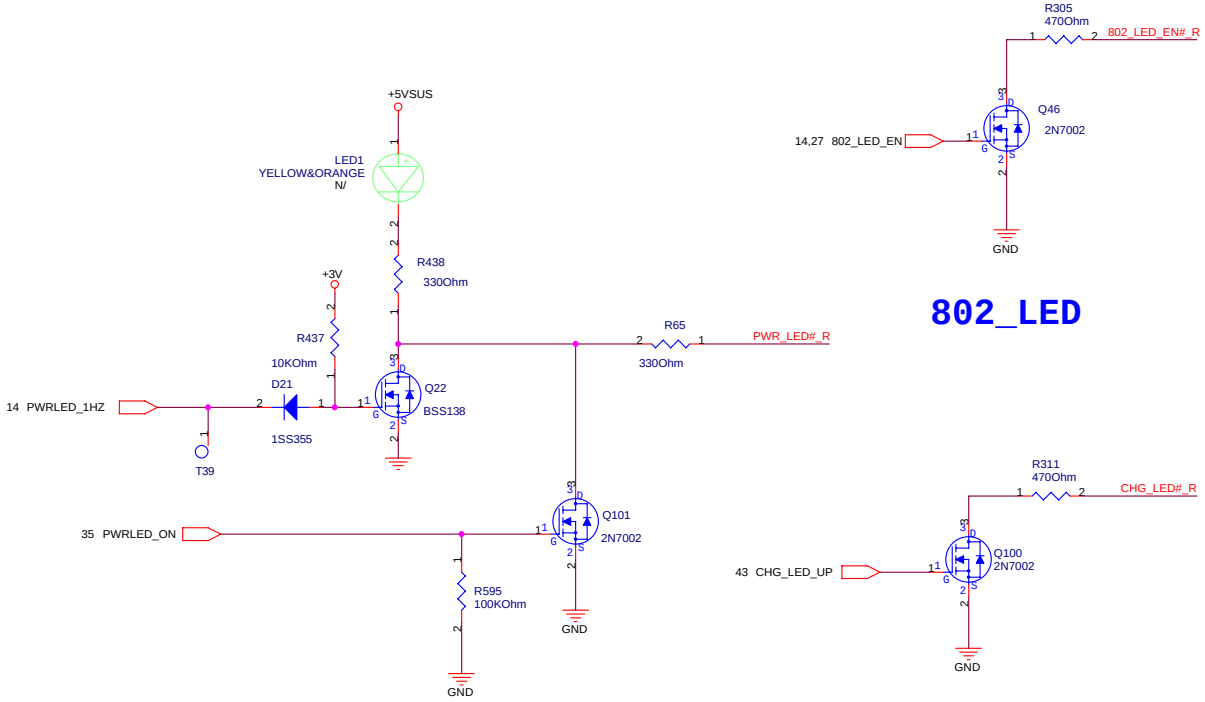
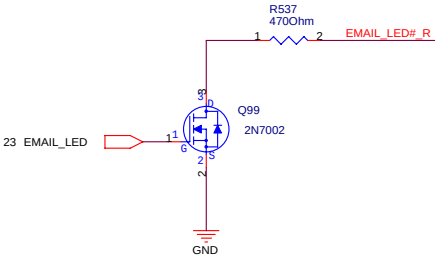
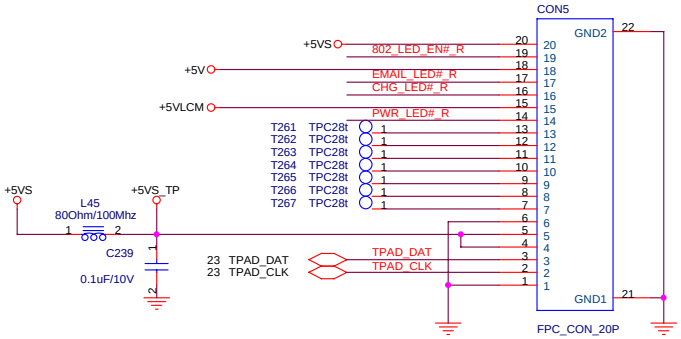


802_LED

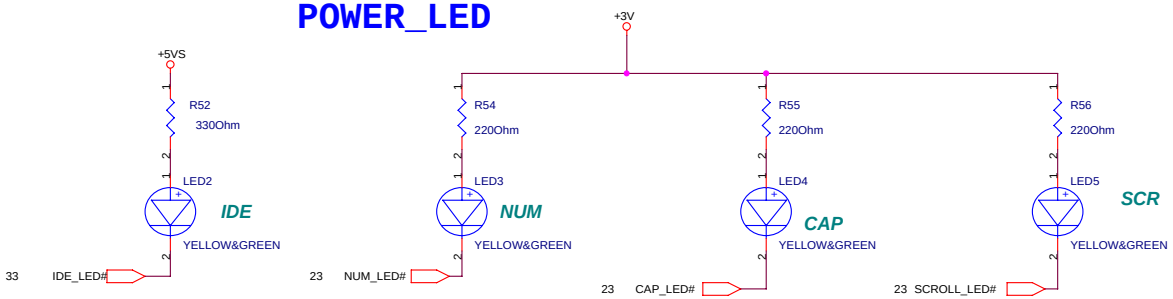
CHG_LED



EMAIL_LED



POWER_LED



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Size: Custom	Project Name: A6R	Rev: 2.0
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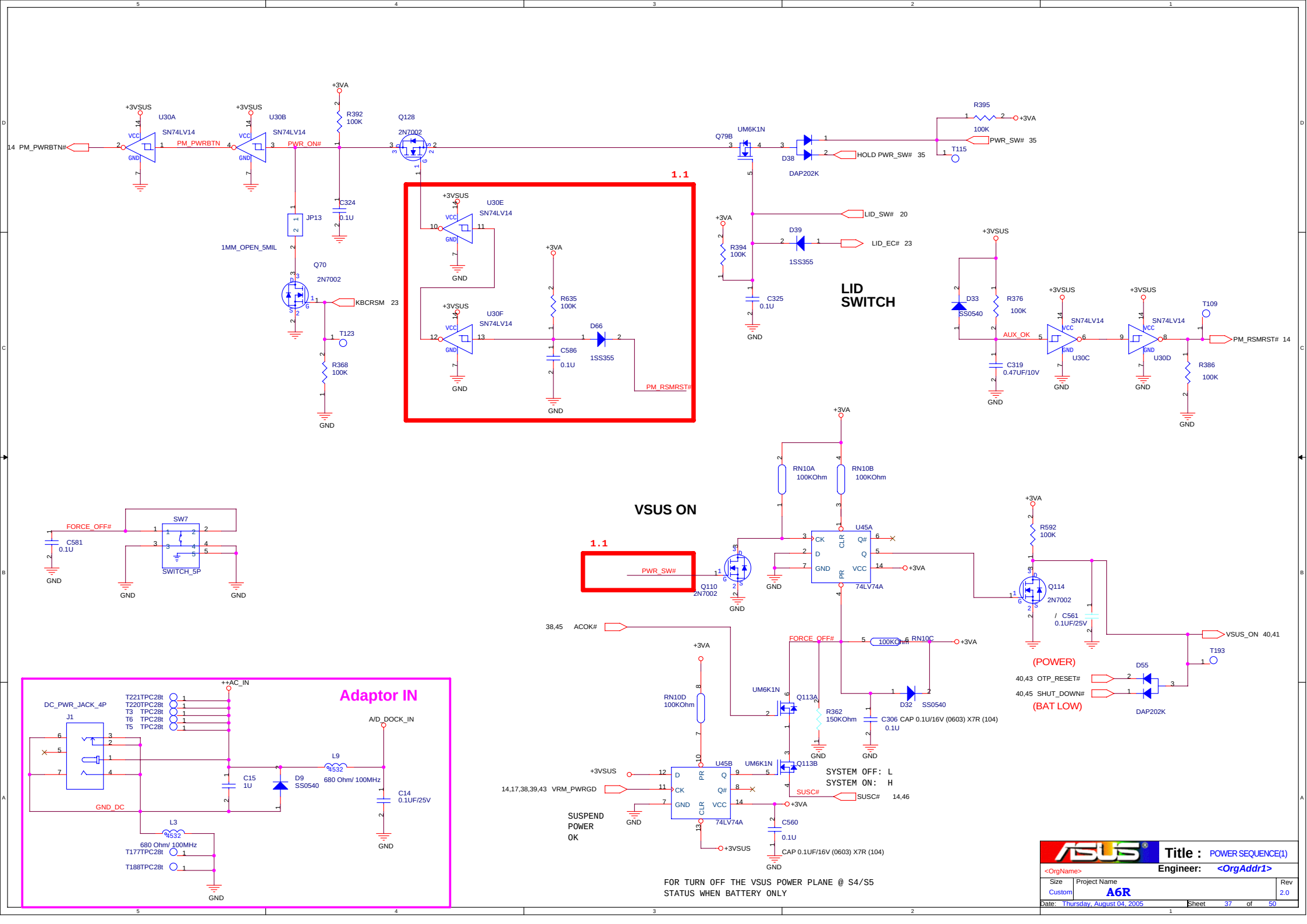
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U30A
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PM_PWRBTN
U30B
PWR_ON#
R392 100K
Q128
2N7002
C324 0.1U
JP13
1MM_OPEN_5MIL
Q70
2N7002
KBCRSM 23
T123
R368 100K
GND
1.1
U30E
U30F
R635 100K
D66
1SS355
C586 0.1U
PM_RSMRST#
Q79B
UM6K1N
D38
DAP202K
HOLD PWR_SW# 35
R395 100K
PWR_SW# 35
T115
LID_SW# 20
LID_EC# 23
D39
1SS355
R394 100K
C325 0.1U
LID SWITCH
D33
SS0540
R376 100K
AUX_OK
U30C
U30D
C319 0.47UF/10V
T109
R386 100K
PM_RSMRST# 14
FORCE_OFF#
SW7
SWITCH_5P
C581 0.1U
VSUS ON
PWR_SW#
Q110
2N7002
RN10A 100KOhm
RN10B 100KOhm
U45A
74LV74A
R592 100K
Q114
2N7002
C561 0.1UF/25V
VSUS_ON 40,41
T193
(POWER)
40,43 OTP_RESET#
40,45 SHUT_DOWN#
(BAT LOW)
D55
DAP202K
38,45 ACOK#
RN10C 100KOhm
D32 SS0540
RN10D 100KOhm
Q113A
Q113B
UM6K1N
R362 150KOhm
C306 CAP 0.1U/16V (0603) X7R (104) 0.1U
U45B
74LV74A
+3VSUS
14,17,38,39,43 VRM_PWRGD
SUSC#
SUSC# 14,46
SYSTEM OFF: L
SYSTEM ON: H
SUSPEND POWER OK
C560 0.1U
CAP 0.1UF/16V (0603) X7R (104)
FOR TURN OFF THE VSUS POWER PLANE @ S4/S5
STATUS WHEN BATTERY ONLY
Adaptor IN
++AC_IN
DC_PWR_JACK_4P
J1
T221TPC28t
T220TPC28t
T3 TPC28t
T6 TPC28t
T5 TPC28t
C15 1U
D9 SS0540
L9 680 Ohm/ 100MHz
A/D_DOCK_IN
C14 0.1UF/25V
GND_DC
L3 680 Ohm/ 100MHz
T177TPC28t
T188TPC28t
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Engineer: <OrgAddr1>
<OrgName>
Size Custom
Project Name A6R
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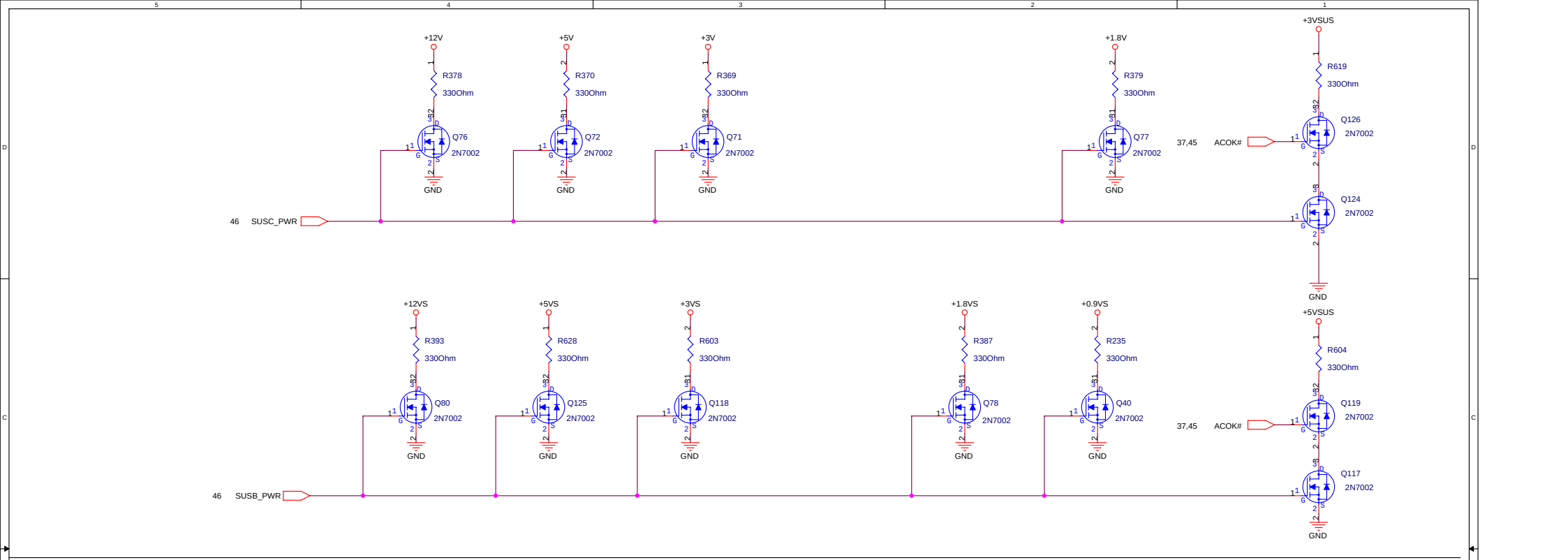

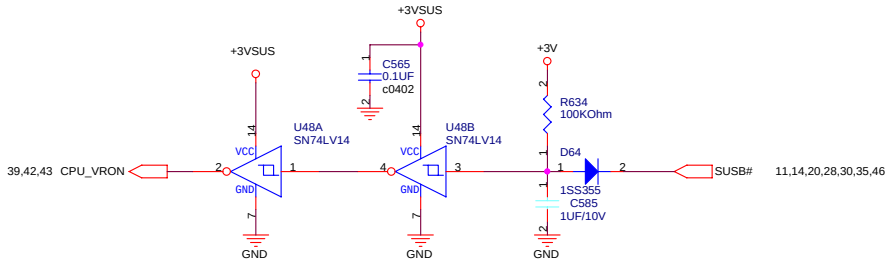

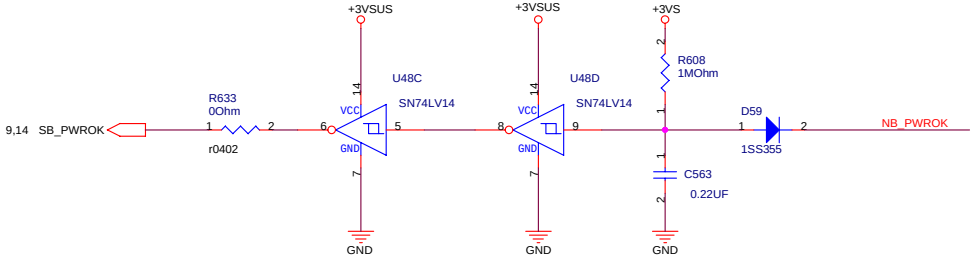

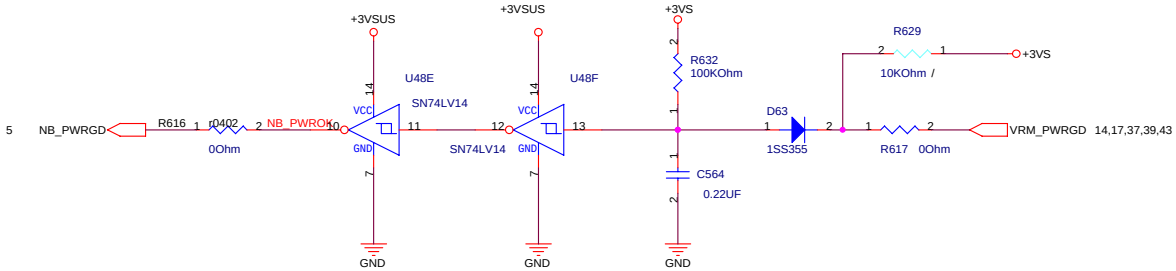

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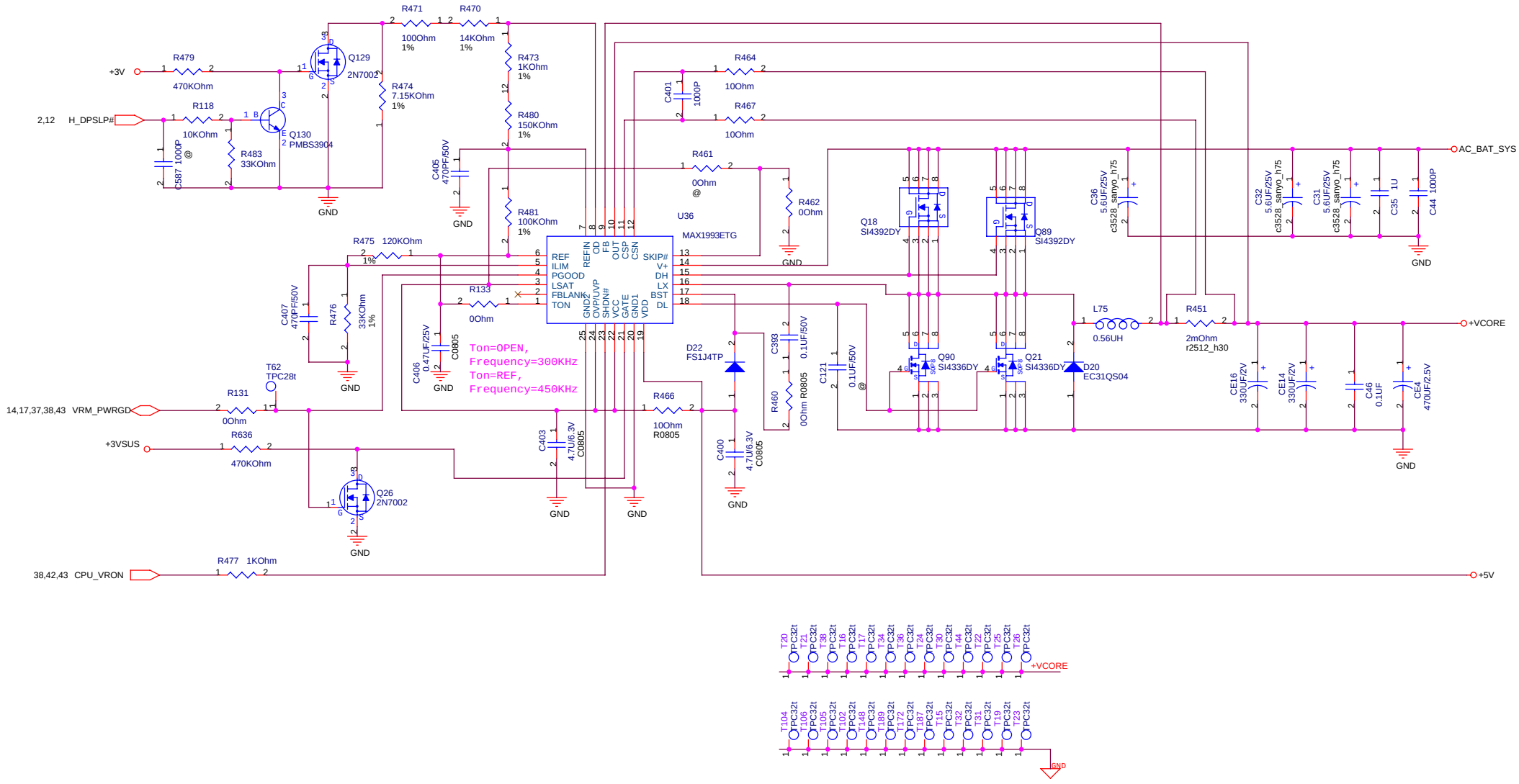
Size: Custom	Project Name: A6R	Rev: 2.0
Date: Thursday, August 04, 2005	Sheet 38 of 50	



Title : VCORE		
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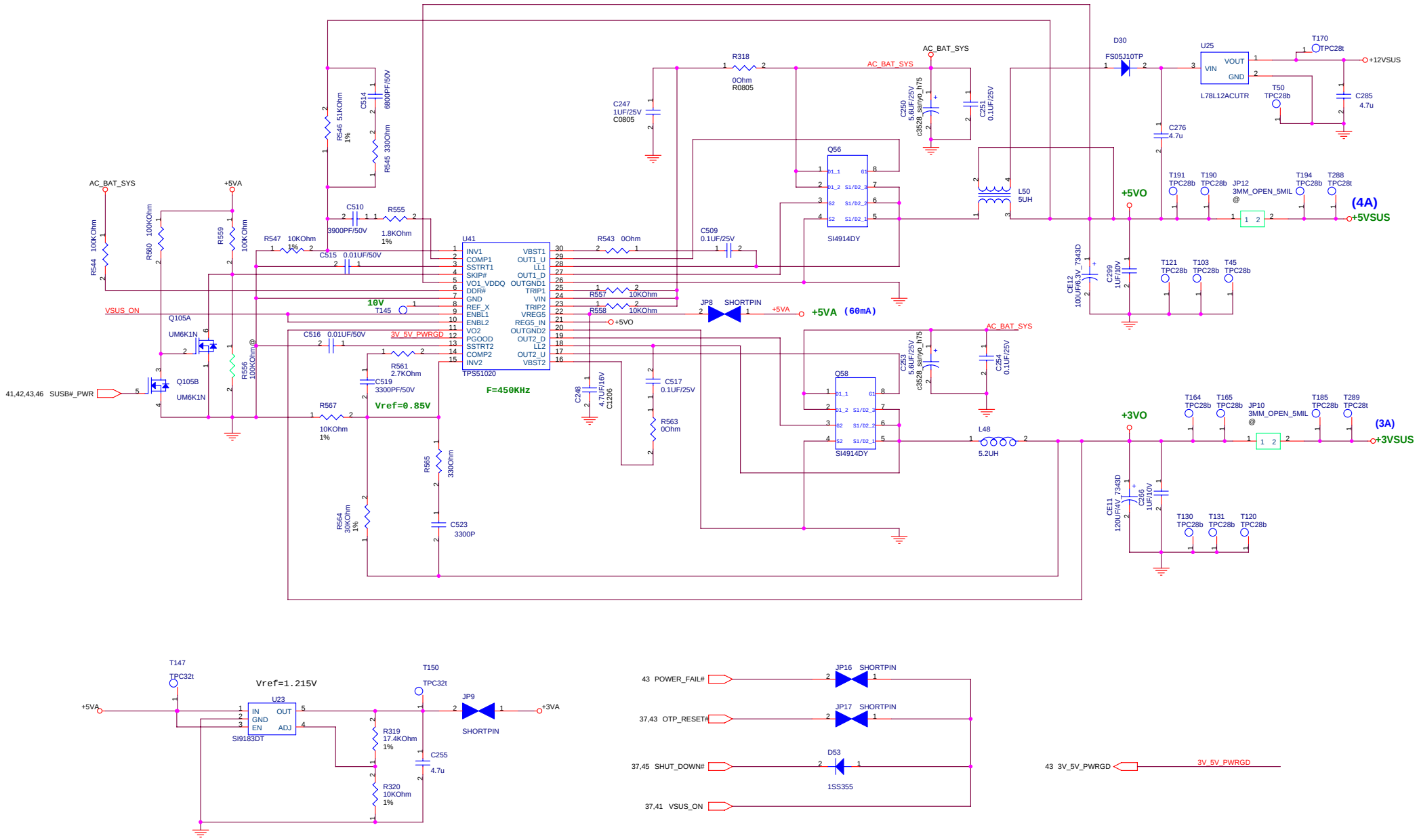
Date: Thursday, August 04, 2005	Sheet 39 of 50	



ASUS	Title :	SYSTEM_+5VA & +3VA
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Size: Custom	Project Name: A6R	Rev: 2.0
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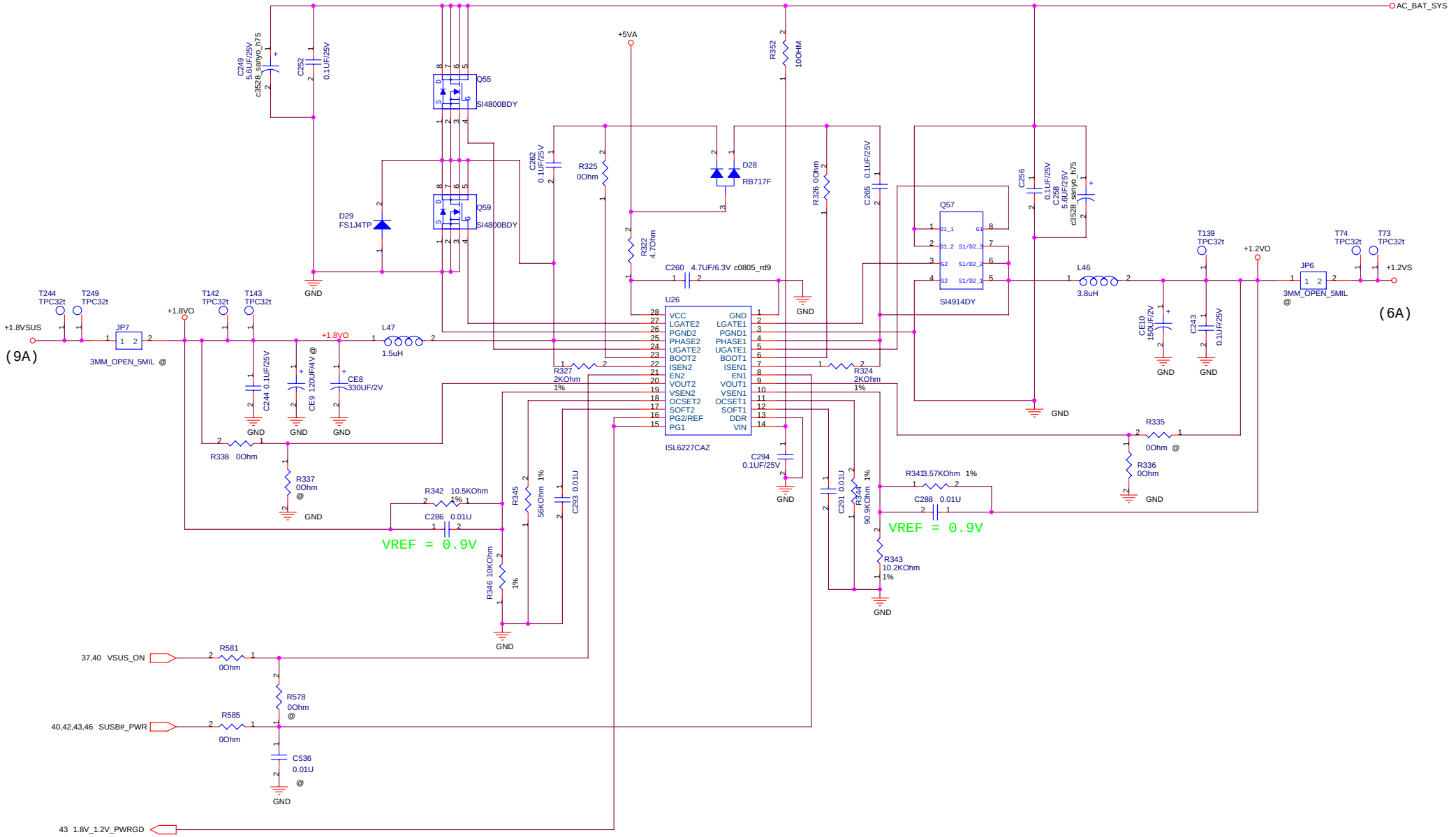

ASUS	Title : 1.8V&1.2VS		
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Size: Custom	Project Name: A6R		Rev: 2.0
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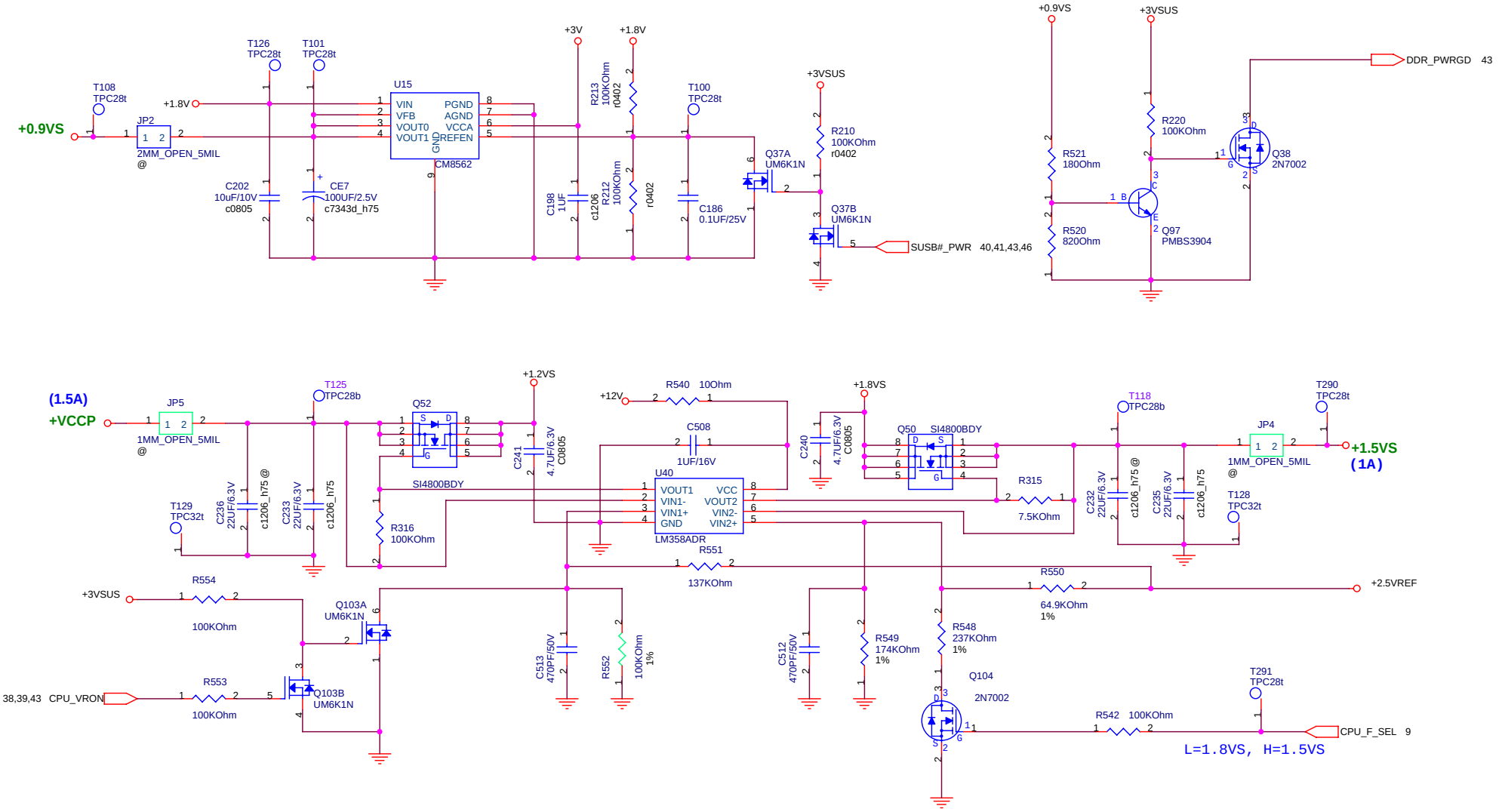

Title : 1.05VA & +0.9VS		
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Size: B	Project Name: A6R	Rev: 2.0
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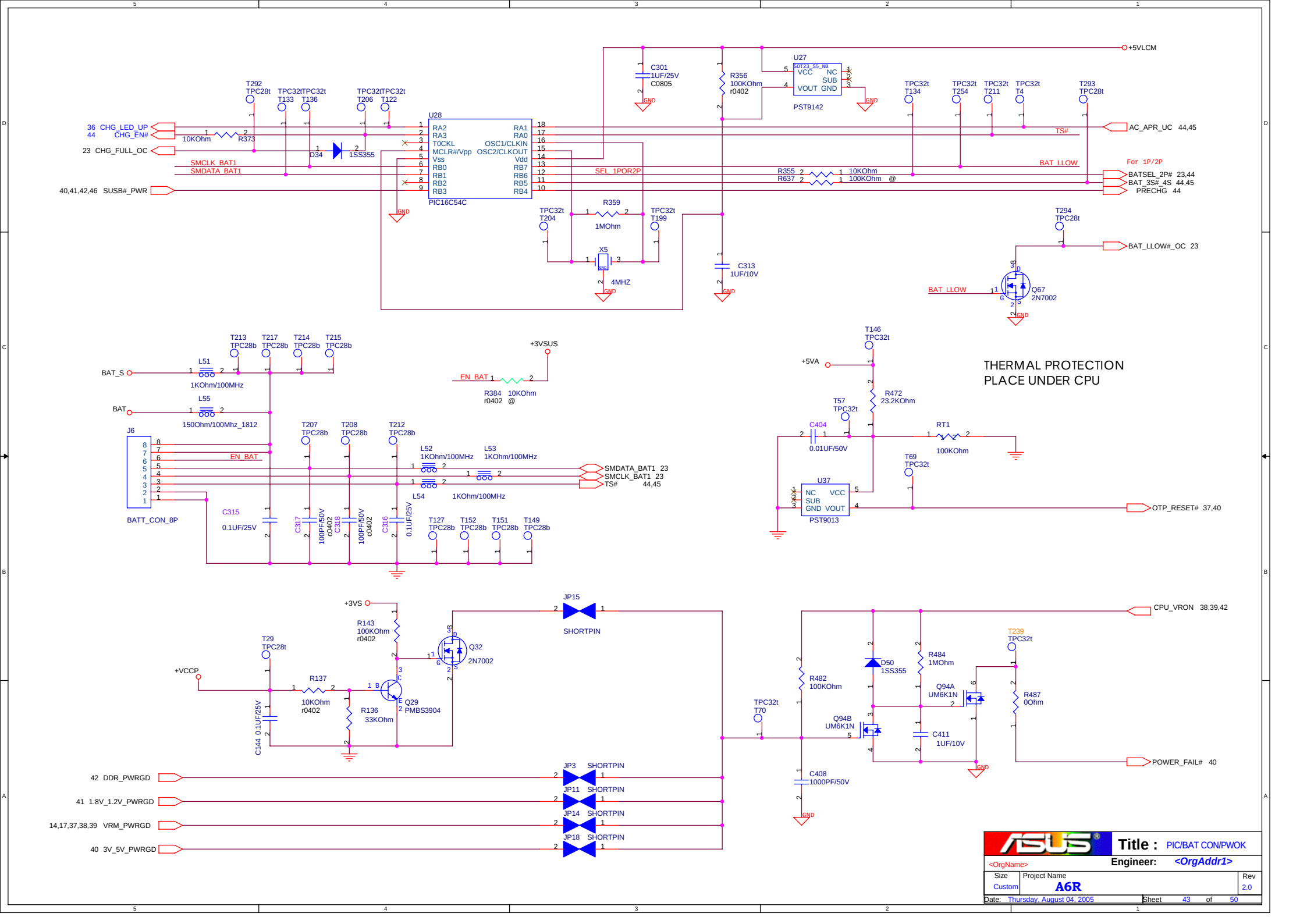
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VCC NC
SUB
VOUT GND
PST9142
C301
1UF/25V
C0805
R356
100KOhm
r0402
T292 TPC28t
T133 TPC32t
T136 TPC32t
T206 TPC32t
T122 TPC32t
T134 TPC32t
T254 TPC32t
T211 TPC32t
T4 TPC32t
T293 TPC28t
36 CHG_LED_UP
44 CHG_EN#
10KOhm
R373
23 CHG_FULL_OC
D34
1SS355
SMCLK_BAT1
SMDATA_BAT1
40,41,42,46 SUSB#_PWR
U28
RA2 RA1
RA3 RA0
T0CKL OSC1/CLKIN
MCLR#/Vpp OSC2/CLKOUT
Vss Vdd
RB0 RB7
RB1 RB6
RB2 RB5
RB3 RB4
PIC16C54C
SEL_1POR2P
TS#
AC_APR_UC 44,45
BAT_LLOW
For 1P/2P
R355 10KOhm
R637 100KOhm @
BATSEL_2P# 23,44
BAT_3S#_4S 44,45
PRECHG 44
R359
1MOhm
TPC32t T204
TPC32t T199
X5
4MHZ
C313
1UF/10V
T294 TPC28t
BAT_LLOW#_OC 23
BAT_LLOW
Q67
2N7002
THERMAL PROTECTION
PLACE UNDER CPU
T213 TPC28b
T217 TPC28b
T214 TPC28b
T215 TPC28b
BAT_S
L51
1KOhm/100MHz
BAT
L55
150Ohm/100Mhz_1812
J6
BATT_CON_8P
EN_BAT
+3VSUS
R384 10KOhm
r0402 @
T207 TPC28b
T208 TPC28b
T212 TPC28b
L52 1KOhm/100MHz
L53 1KOhm/100MHz
L54 1KOhm/100MHz
SMDATA_BAT1 23
SMCLK_BAT1 23
TS# 44,45
C315
0.1UF/25V
C317
100PF/50V
c0402
C318
100PF/50V
c0402
C316
0.1UF/25V
T127 TPC28b
T152 TPC28b
T151 TPC28b
T149 TPC28b
T146 TPC32t
+5VA
R472
23.2KOhm
T57 TPC32t
C404
0.01UF/50V
RT1
100KOhm
T69 TPC32t
U37
NC VCC
SUB
GND VOUT
PST9013
OTP_RESET# 37,40
+3VS
R143
100KOhm
r0402
Q32
2N7002
JP15
SHORTPIN
T29 TPC28t
+VCCP
R137
10KOhm
r0402
R136
33KOhm
Q29
PMBS3904
C144 0.1UF/25V
JP3 SHORTPIN
JP11 SHORTPIN
JP14 SHORTPIN
JP18 SHORTPIN
42 DDR_PWRGD
41 1.8V_1.2V_PWRGD
14,17,37,38,39 VRM_PWRGD
40 3V_5V_PWRGD
CPU_VRON 38,39,42
T239 TPC32t
R482
100KOhm
D50
1SS355
R484
1MOhm
Q94A
UM6K1N
Q94B
UM6K1N
R487
0Ohm
C411
1UF/10V
TPC32t T70
C408
1000PF/50V
POWER_FAIL# 40
GND
Title : PIC/BAT CON/PWOK
<OrgName>
Engineer: <OrgAddr1>
Size Custom
Project Name A6R
Rev 2.0
Date: Thursday, August 04, 2005
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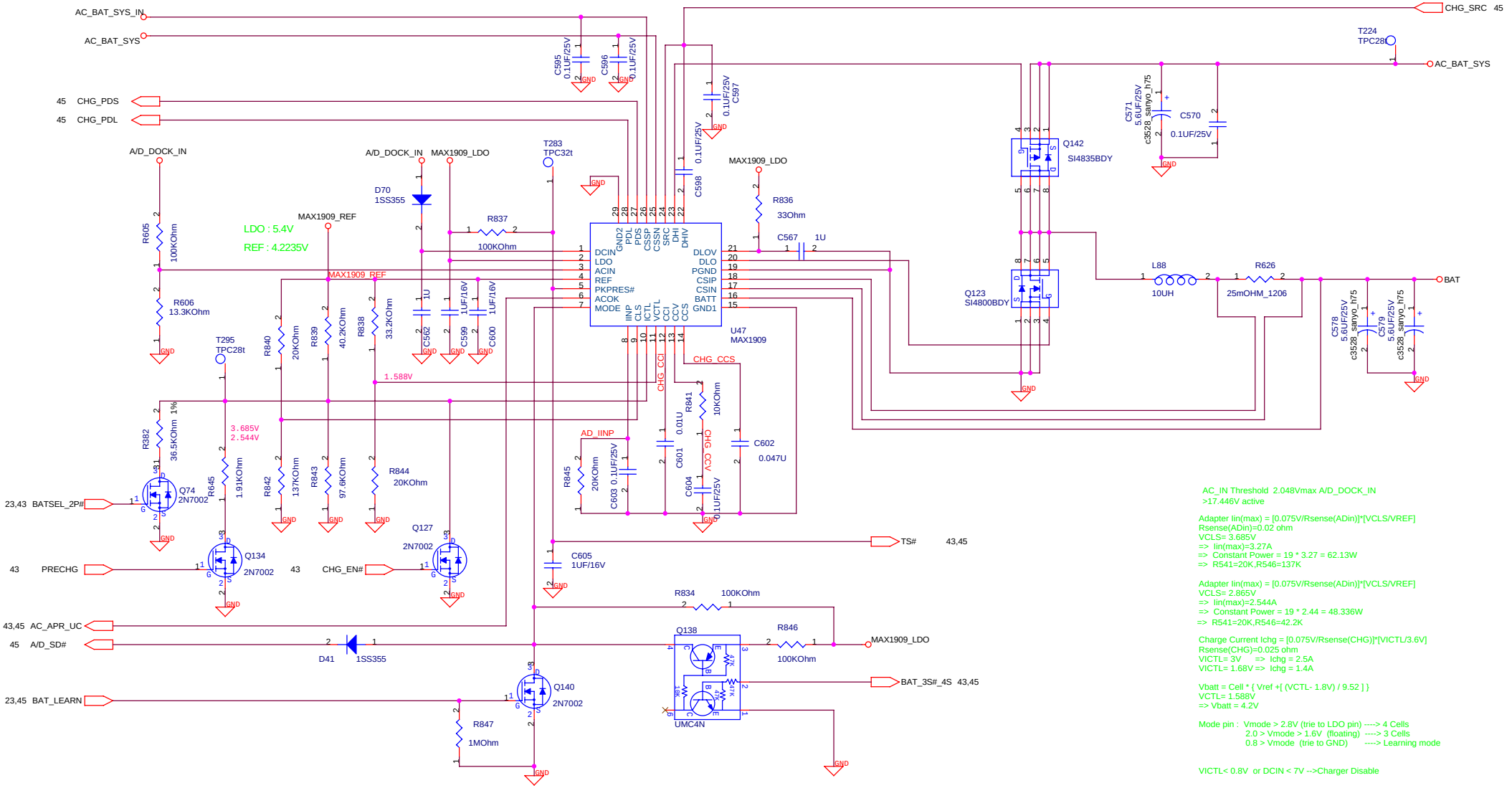


AC_IN Threshold 2.048Vmax A/D_DOCK_IN
>17.446V active

Adapter Iin(max) = [0.075V/Rsense(ADin)]*[VCLS/VREF]
Rsense(ADin)=0.02 ohm
VCLS= 3.685V
=> Iin(max)=3.27A
=> Constant Power = 19 * 3.27 = 62.13W
=> R541=20K,R546=137K

Adapter Iin(max) = [0.075V/Rsense(ADin)]*[VCLS/VREF]
VCLS= 2.865V
=> Iin(max)=2.544A
=> Constant Power = 19 * 2.44 = 48.336W
=> R541=20K,R546=42.2K

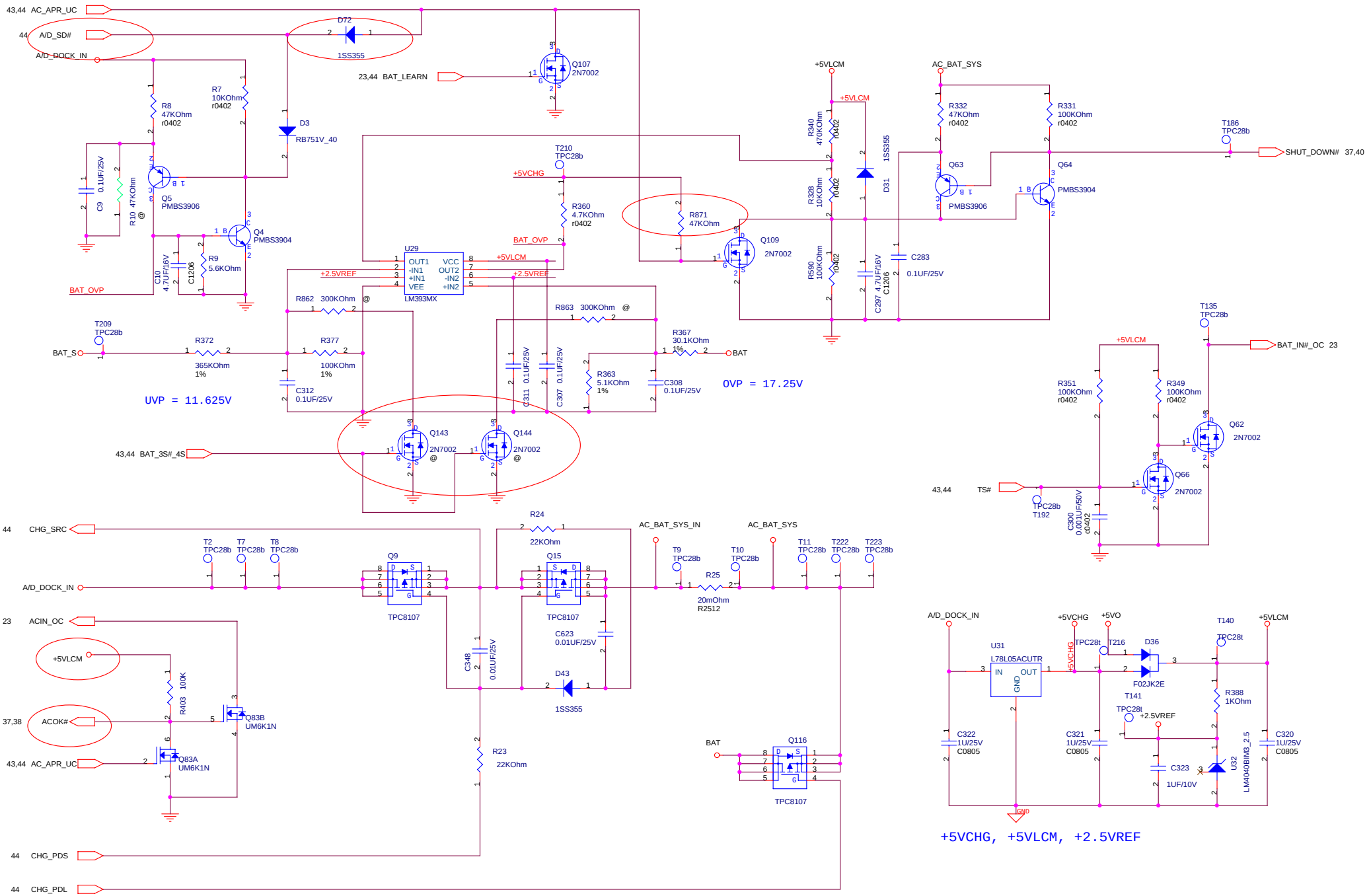
Charge Current Ichg = [0.075V/Rsense(CHG)]*[VICTL/3.6V]
Rsense(CHG)=0.025 ohm
VICTL= 3V => Ichg = 2.5A
VICTL= 1.68V => Ichg = 1.4A

Vbatt = Cell * { Vref +[(VCTL- 1.8V) / 9.52] }
VCTL= 1.588V
=> Vbatt = 4.2V

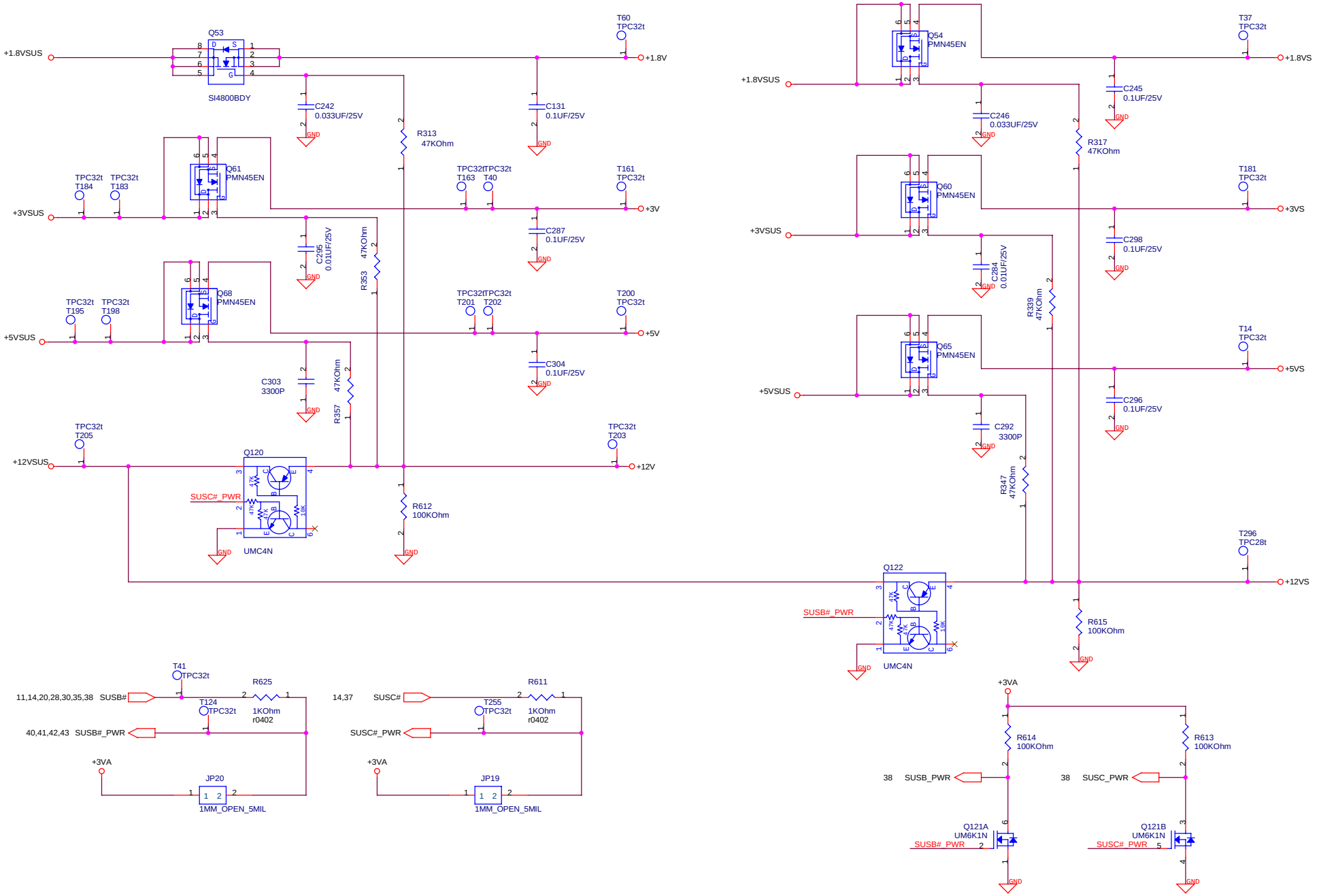
Mode pin : Vmode > 2.8V (trie to LDO pin) ----> 4 Cells
2.0 > Vmode > 1.6V (floating) ----> 3 Cells
0.8 > Vmode (trie to GND) ----> Learning mode

VICTL< 0.8V or DCIN < 7V -->Charger Disable

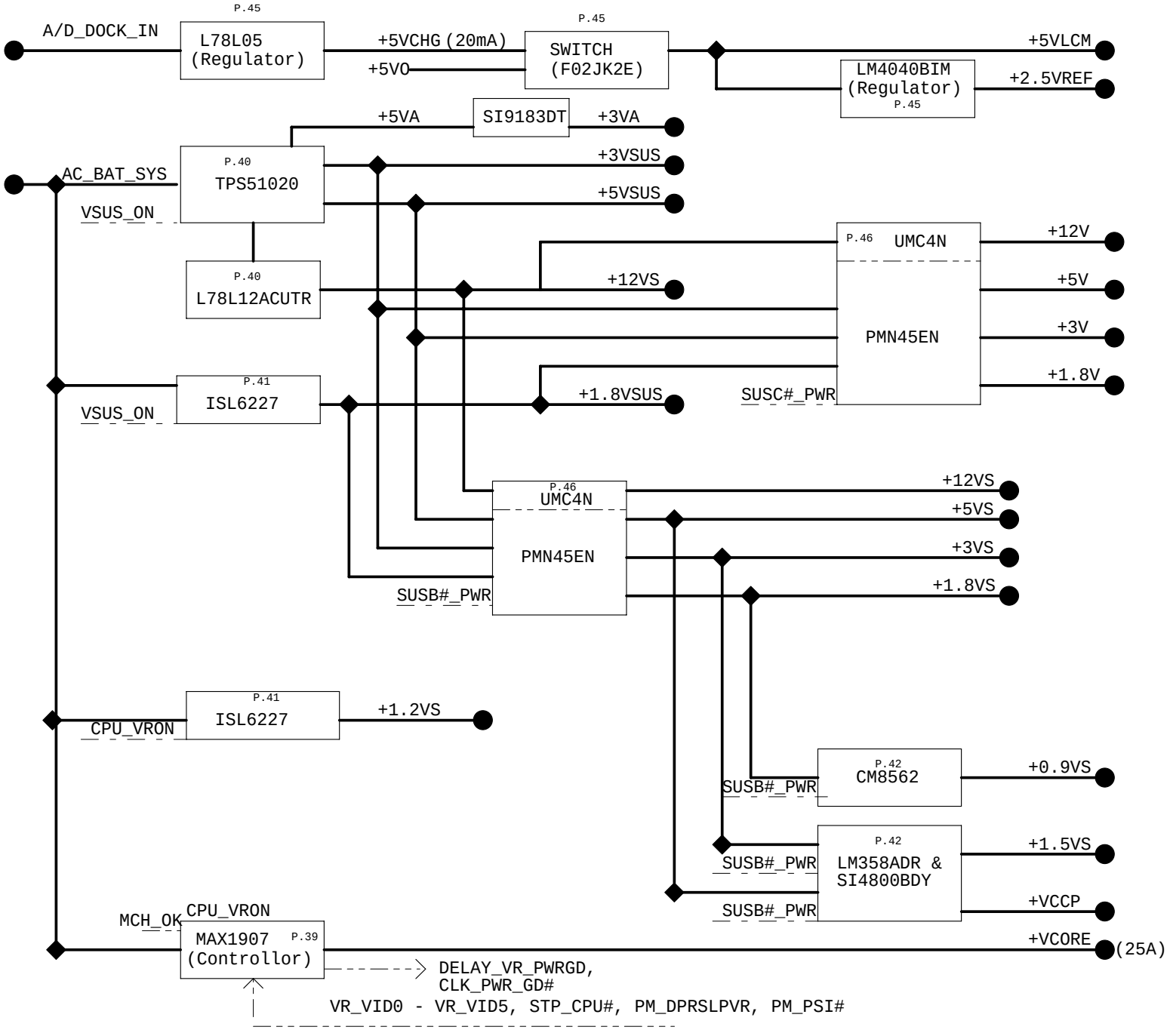
ASUS	Title : CHARGE	
<OrgName>	Engineer: <OrgAddr1>	
Size: Custom	Project Name: A6R	Rev: 2.0
Date: Thursday, August 04, 2005	Sheet 44 of 50	



ASUS	Title : BATLOW/SD#	
<OrgName>	Engineer: <OrgAddr1>	
Size: Custom	Project Name: A6R	Rev: 2.0
Date: Thursday, August 04, 2005	Sheet 45 of 50	



Title : LOAD SWITCH		
<OrgName>	Engineer: <OrgAddr1>	
Size: Custom	Project Name: A6R	Rev: 2.0
Date: Thursday, August 04, 2005	Sheet 46 of 50	



ASUS	Title :	POWER BLOCK DIAGRAM
<OrgName>	Engineer:	<OrgAddr1>
Size: Custom	Project Name: A6R	Rev: 2.0
Date: Thursday, August 04, 2005	Sheet 47 of 50	

PCI Device	IDSEL#	REQ/GNT#	Interrupts
10/100 LAN	AD16	0	E
CARD READER	AD17	1	C
CARDBUS	AD17	1	A
1394	AD17	1	B
MINIPCI (802.11a/b/g)	AD19	3	G,H

SM-Bus Device	SM-Bus Address
Clock Generator	1101001x (D2)
SO-DIMM 0	1010000x (A0)
SO-DIMM 1	1010001x (A2)
Thermal Sensor	0101110x (5C)
PIC	1001001x (92)

SB400 GPIO TABLE

GPIO	TYPE	POWER DOMAIN	FUNCTION
GPIO 0	I/OD	S0	
GPIO 1	I/O	S0	
GPIO 2	I/O	S0	SB_SPKR
GPIO 3	I/O	S0	FWH_WP#
GPIO 4	I/O	S0	PCB_ID0
GPIO 5	I/O	S0	PCB_ID1
GPIO 6	I/OD	S0	PCB_ID2
GPIO 7	I/O	S0	VRM_PWRGD
GPIO 8	I/O	S0	CB_SD#
GPIO 9	I/O	S0	BACK_OFF#
GPIO 10	I/O	S5	SB_PM_THERM#
GPIO 11	I/O	S0	802_LED_EN
GPIO 12	I/O	S0	WLAN_ON#
GPIO 13	I/O	S0	
GPIO 14	I/O	S0	PCI_GNT#5
GPIO 31	I/O	S0	
GPIO 32	I/O	S0	PCI_GNT#6
GPIO 33	I/O	S0	PCI_INTE#
GPIO 34	I/O	S0	PCI_INTF#
GPIO 35	I/O	S0	PCI_INTG#
GPIO 36	I/O	S0	PCI_INTH#
GPM 0	I	S5	
GPM 1	I	S5	
GPM 2	I/O	S5	
GPM 3	I	S5	
GPM 4	I	S5	
GPM 5	I	S5	
GPM 6	I/OD	S5	PWRLED_1HZ
GPM 7	I	S5	SYS_RESET#
GEVENT 0	I	S5	
GEVENT 1	I	S0	
GEVENT 2	I	S5	THRMTRIP#
GEVENT 3	I	S5	LPC_PME#
GEVENT 4	I	S5	PCI_PME#
GEVENT 5	I	S5	H_PROCHOT#
GEVENT 6	I	S5	
GEVENT 7	I	S5	
GEVENT 8			KB_SCI
EXTEVENT#0			EXT_SMI#
EXTEVENT#1			SIO_SMI#

KBC GPIO	W1V	Note
P23(Pin 35)	CHG_FULL_OC	
P22(Pin 36)	BAT_LEARN	
P21(Pin 37)	LID_EC#	
P20(Pin 38)	KBCRSM	
P42(Pin 23)		
P43(Pin 22)	OP_SD#	
P44(Pin 21)	KB_CPURST	
P45(Pin 20)	KB_GATEA20	
P46(Pin 19)	KBCSCI#	
P47(Pin 18)	PM_CLKRUN#	
P50(Pin 17)	BAT_LLOW#_OC	
P51(Pin 16)	KID0	
P52(Pin 15)	KID1	
P53(Pin 14)	CLR_DJ#	
P54(Pin 13)	BAT_SEL#	
P55(Pin 12)	BAT1_IN#_OC	
P56(Pin 11)		
P57(Pin 10)	INV_DA	
P67(Pin 74)	DJ_LED#	
P66(Pin 75)	SWDJ_EN#	
P65(Pin 76)	GAIN_AMP_K#	0->-6 V/V 1->NORMAL
P64(Pin 77)	ACIN_OC	
P63(Pin 78)	DISTP#	
P62(Pin 79)	MARATHON#	
P61(Pin 80)	INTERNET#	
P60(Pin 1)	EMAIL#	
P75(Pin 4)	KB_CLK	
P74(Pin 5)	MS_CLK	
P73(Pin 6)	TPAD_CLK	
P72(Pin 7)	KB_DAT	
P71(Pin 8)	MS_DAT	
P70(Pin 9)	TPAD_DAT	
P77(Pin 2)	SMC_BAT	
P76(Pin 3)	SMD_BAT	
P27(Pin 31)	SCROLL_LED#	
P26(Pin 32)	NUM_LED#	
P25(Pin 33)	CAP_LED#	
P24(Pin 34)	SET_PLTRSTNS#	
P40(Pin 27)	EXT_SMI	
P41(Pin 26)	EMAIL_LED#	

ASUS

Title : SYSTEM RESOURCE

<OrgName>

Engineer: <OrgAddr1>

Size	Project Name	Rev
Custom	A6R	2.0

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Rev	Date	Description
1.0	05/03/01	1. Initial release.

Rev	Date	Description

ASUS	Title : HISTORY	
<OrgName>	Engineer: <OrgAddr1>	
Size: Custom	Project Name: A6R	Rev: 2.0
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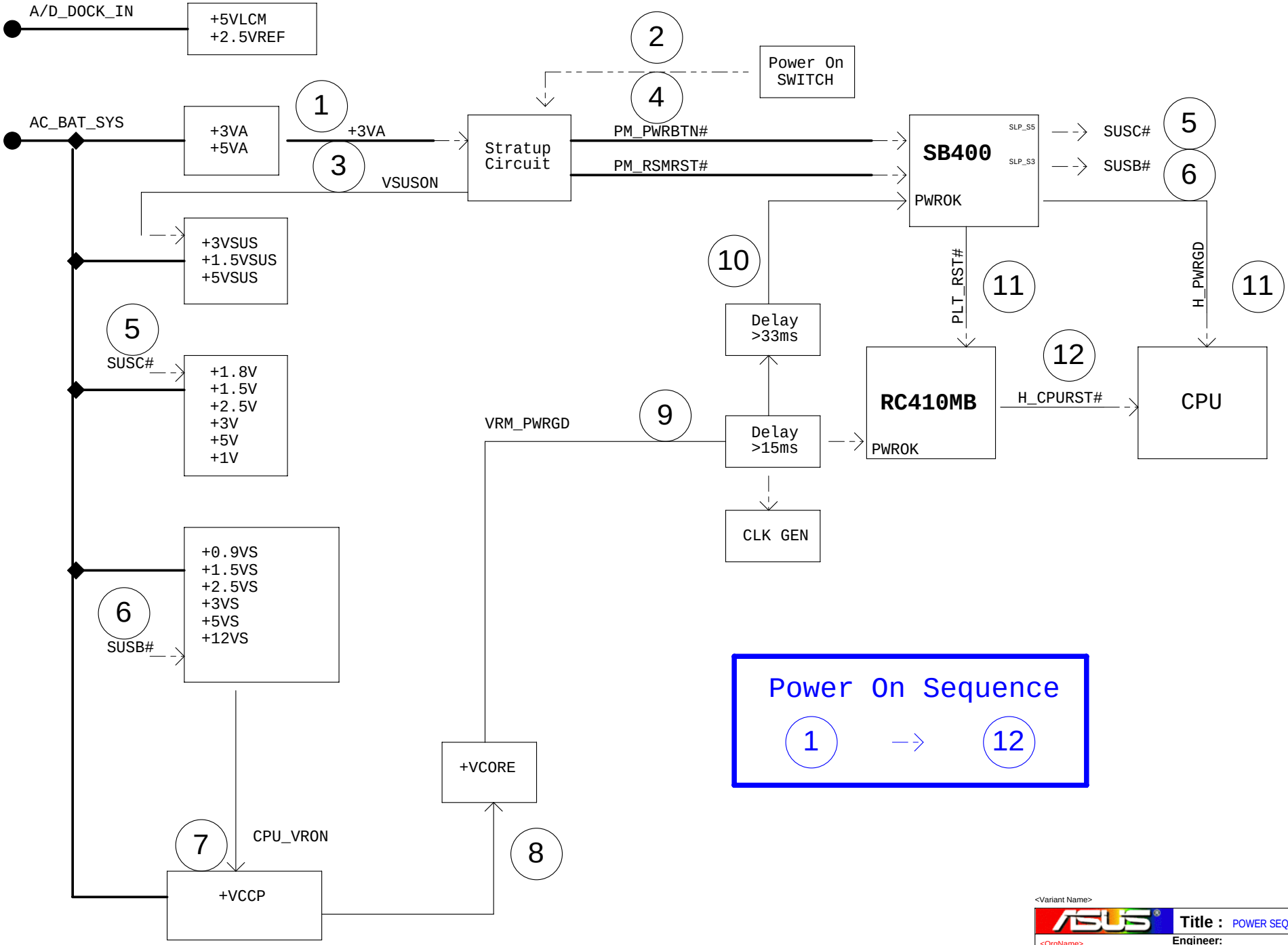

<Variant Name>

Title : POWER SEQUENCY

<OrgName>

Engineer:

Size	Project Name	Rev
Custom	A6R	2.0

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