CPD

Communications Products Division

Target, Advanced and Preliminary Information

In this data book the following conventions are used in designating a data sheet "Target," "Advanced" or "Preliminary":

Target Specification —

The target specification is intended as an initial disclosure of specification goals for the product. Product is in first stages of design cycle.

Advance Information —

Indicates a product still in the design cycle, undergoing testing processes, and any specifications are based on design goals only. Do not use for final design.

Preliminary Data —

Indicates a product not completely released to production. The specifications are based on preliminary evaluations and are not guaranteed. Small quantities are available, and Silicon Systems should be consulted for current information.

COMMUNICATIONS PRODUCTS SELECTOR GUIDE

Device Number	B212 B103	B202	CCITT V.21	CCITT V.23	CCITT V.22	CCITT V.22bis	Description	Power Supply	Available Packages
K-Series Single Chip Modem Family									
73K212L	✗						low power, integrated single-chip modem	+5V	28 DIP, 28 PLCC
73K212SL	✗						73K212L with serial interface only	+5V	22 DIP
73K221L			✗		✗		low power, integrated single-chip modem	+5V	22, 28 DIP, 28 PLCC
73K221SL			✗		✗		73K221L with serial interface only	+5V	22 DIP
73K222L	✗		✗		✗		low power, integrated single-chip modem	+5V	22, 28 DIP, 28 PLCC
73K222SL	✗		✗		✗		73K222L with serial interface only	+5V	22 DIP
73K222U	✗		✗		✗		73K222L with 16C450 UART	+5V	40 DIP, 44 PLCC
73K224L	✗		✗		✗	✗	Bell 212A/103, CCITT V.22bis/V.22/V.21	+5V	28 DIP, 28, 32 PLCC
73K224SL	✗		✗		✗	✗	73K224L with serial interface	+5V	22 DIP
73K302L	✗	✗					Bell 212A/202/103	+5V	28 DIP, 28 PLCC
73K302SL	✗	✗					Bell 212A/202/103; serial interface only	+5V	22 DIP
73K321L			✗	✗			CCITT V.23/V.21	+5V	28 DIP, 28 PLCC
73K321SL			✗	✗			73K321L with serial interface only	+5V	22 DIP
73K322L			✗	✗	✗		CCITT V.23/V.22/V.21	+5V	28 DIP, 28 PLCC
73K322SL			✗	✗	✗		73K322L with serial interface only	+5V	22 DIP
73K324L	B212		✗	✗	✗	✗	CCITT V.22bis/V.22/V.23/V.21 controllers, UARTs, and special modem products	+5V	28 DIP, 28, 32 PLCC
Controllers, UARTs and Special Modem Products									
73D2248/2348				✗	✗	✗	modem device set w/ AT, MNP	+5V	Various QFP & TQFP
73M223				✗			1200 bit/s modem IC, compact HDX V.23 modem	+5V	16 DIP, 16 SOL
73M550							16C550 pin compatible UART receive and transmit FIFOs	+5V	40 DIP, 44 PLCC, 48 GT
73M1550							28-pin version of 73M550, full UART in 28-pin package	+5V	28 DIP, PLCC
73M2550							28-pin version of 73M550, adds µPRST function	+5V	28 DIP, PLCC
73M2910/2910A							modem controller device	+3V/+5V	100 QFP, TQFP
73M2918/2918A							Plug & Play Microcontroller & UART	+3.3V/+5V	100 QFP, TQFP

Device Number	Circuit Function	Features	Power	Available Packages
Analog Signalling and Switching Products				
75T202	Integrated DTMF Receiver	low power, binary output	+5V	18 DIP
75T203	Integrated DTMF Receiver	early detect, binary output	+5V	18 DIP
75T204	Integrated DTMF Receiver	low power, binary output	+5V	14 DIP, 16 SO
75T2089	Integrated DTMF Transceiver	generator & receiver, µP interface	+5V	22 DIP
75T2090	Integrated DTMF Transceiver	like 75T2089 w/ call progress detect	+5V	22 DIP
75T2091	Integrated DTMF Transceiver	like 75T2090 w/ early detect	+5V	28 DIP, PLCC
75T980	Imprecise Call Progress Detector	energy detect in 305-640 Hz band, Teltone	+5V	8 DIP
78A207	Integrated MF Receiver	detects central office toll signals	+5V	20 DIP
PCM/ATM Products				
78P300	T1/E1 Short Haul Transceiver	receive jitter attenuation	+5V	28 DIP, PLCC
78P304A	Low-Power 38P300	receive jitter attenuation	+5V	28 DIP, PLCC
78P7200	DS-3/E3/STS-1 Line Interface Trans.	DS-3/E3/STS-1 transceiver w/receive equalization & higher transmitter drive	+5V	28 DIP, PLCC
78Q2250	155 Mbit/s ATM Transceiver for NRZ	on-chip clock/data recovery	3V or 5V	48 TQFP
LAN Products				
78Q8373	Single-chip Ethernet IC for PCMCIA	on-chip PCMCIA bus logic, 10BaseT transceiver	3V or 5V	100 TQFP
78Q8377	Single-chip Ethernet for ISA/PnP	on-chip Plug & Play logic, 10BaseT transceiver	+5V	128 QFP
78Q8378	Single-chip Ethernet for PCMCIA	on-chip PCMCIA multi-function logic	3V or 5V	100 TQFP
78Q8392L	Low-power Coax Transceiver	pin-compatible w/NSC 8392	-9V	16 DIP, 28 PLCC
Set-Top Box and Wireless Products				
79W2522	Dual 4-Bit ADCs	20 to 60 Mbit/s, 6-bit linearity, internal VCO	+5V	28 SO

Section 1

CUSTOM SOLUTIONS

silicon systems®
A TDK Group Company

CUSTOM SOLUTIONS

SILICON SYSTEMS LEADS THE WAY DEVELOPING MIXED-SIGNAL CUSTOM PRODUCTS.

This is a story about leadership. Silicon Systems is dedicated to taking the point in the creation of high-performance, application-specific custom, mixed-signal integrated circuits (MSICs®).

Such dedication means we bring a lot to the party. Including truly innovative analog, digital, and mixed analog/digital ICs. A full complement of mixed-signal CMOS, BiCMOS and Bipolar wafer fabrication processes, state-of-the-art automated design tools, production, assembly, test, and QA capability.

No one's more experienced

More than 20 years of successful IC design work makes us the most experienced engineering team in the MSICs field. Add it all up and you get a company that saves you time and money while delivering you the most sophisticated mixed-signal custom ICs you can get.

Faster to market for mixed-signal applications

Whatever your mixed-signal design application, Silicon Systems gives you a competitive advantage. In communications, disk drives, other storage products, automotive control systems, or other analog/digital signal processing applications, you can depend on our technical know-how to do the job right and turn your design around faster.

CMOS. Bipolar. BiCMOS. Analog. Digital. We've done it

Our designers are an experienced bunch. They're uniquely able to take a look at your specific application problem and move quickly to the right IC solution.

Our team is particularly adept at identifying key issues such as power, cost and performance trade-offs. So we can gear our efforts toward delivering you an optimized solution, manufactured with the appropriate fab process.

Technique	Application	Silicon Systems Designed Examples
CMOS Analog Processing	For analog continuous time, sampled data (switched-capacitor implementation), and high-current power transistor applications. Low power, high density capability also supports inclusion of ROMs, RAMs, and other analog/digital subsystems.	• Complete single-chip 2400 bit/s modem • 14.4 kbps modem chip set • Direct-broadcast satellite descrambler • Servo and spindle motor controllers with 1.5 Amp motor interfaces • High-resolution analog data acquisition • Cellular baseband processor
BiCMOS Signal Processing	For high-performance, low noise, wideband signal acquisition and processing applications. Offers TTL, CMOS and/or ECL logic interfaces with high current drive.	• Sub 1 nV/√Hz HDD R/W amplifiers • AGC, pulse detection amplifiers • High-speed data separators • Wideband transceivers • PLLs (phase locked loops) • Optical signal processing • Digital cellular, PCS IF circuits
Digital CMOS	For ASIC controllers, digital signal processors, sequencers and data path applications with on-board ROM, RAM, and PLA sub-systems. Offers standard TTL and/or CMOS logic interfaces.	• Digital communications LAN devices • Hard disk drive controllers • SCSI interface controllers • UARTs • Digital signal processors for hard disk servo and telecommunications

The right mix of analog and digital

Providing total analog/digital systems on a chip allows you to meet your cost and performance objectives whether you're designing the next generation of communication, computer peripheral, or industrial control systems.

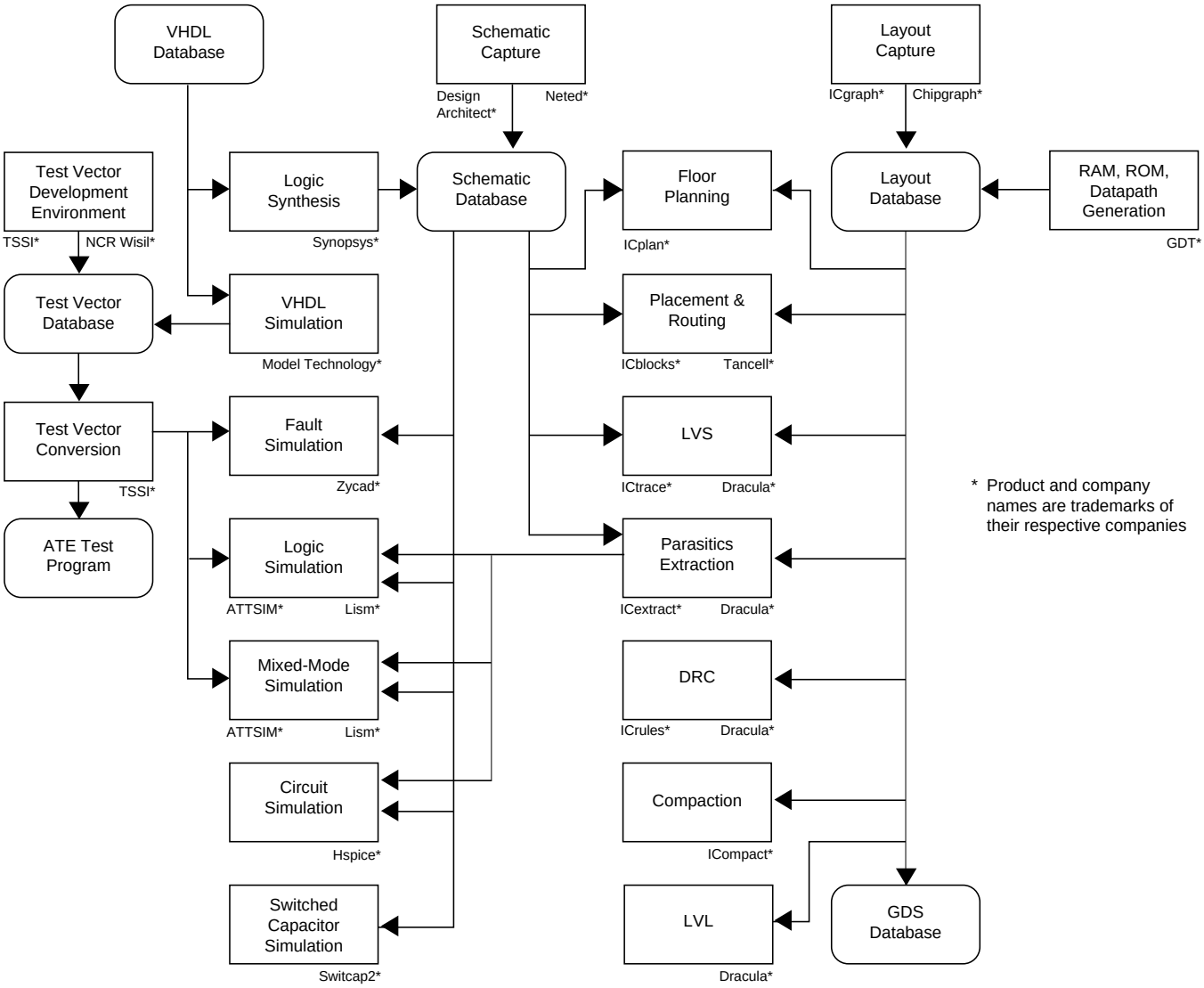
We've turned to CMOS to effectively implement low-power, highly integrated systems solutions for everything from modems and cellular phones to hard disk drive controllers and digital signal processors.

We've gone the BiCMOS route to meet the high-performance needs of products like wideband transceivers, wireless IF modems, R/W amplifiers, low-noise amplifiers, pulse detectors, high-speed data separators and high-performance, low-power combo devices.

SOPHISTICATED TOOLS FOR STRUCTURED CUSTOM DESIGN

At each of six design centers capable of worldwide service – Tustin, San Jose and Nevada City, California; Longmont, Colorado; Tokyo and Singapore – Silicon Systems employs PEGASYS, any internal design automation system developed from carefully selected vendor tools and our own proprietary software. Using Mentor Graphics workstations of both electrical and physical design, PEGASYS helps create complex designs while significantly reducing schedules, costs and errors.

By integrating third-party tools and custom software, we're better able to design and analyze mixed-signal integrated circuits in all CMOS, Bipolar and BiCMOS technologies. It's an approach that has given us the edge in mixed-signal design and helped put Silicon Systems' customers in a favorable position in the marketplace.



PEGASYS Design System

Specifically, PEGASYS brings the following to each design:

- Fully integrated design environment
- Methodology for precision circuit design
- Integrated electrical and physical design
- Unique blend of full-custom and automated layout techniques
- Complete layout verification
- Full mixed-signal parasitic extraction

Our design automation staff integrates the third-party tools and optimizes their use on the Mentor platform. This framework can easily accommodate new tools when needed, and it enables us to support a combination of analog and digital design techniques in all CMOS, Bipolar and BiCMOS chip designs. By mixing design methodologies, we can achieve optimum systems performance, even when schedules are tight.

Electrical design

A single CAE (computer aided engineering) environment provides for schematic capture, synthesis, simulation, and fault grading. We support this software with extensive libraries of pre-designed cells and components. Highly specialized cells or components can be designed and enhanced where required. We simulate each circuit to meet precise performance specifications using:

- Analog circuit simulation
- Digital logic simulation
- VHDL simulation
- Mixed-mode simulation
- Switched-capacitor filter simulation
- Analog and mixed-mode behavioral simulation

Admittedly, simulation alone is not the key to perfecting performance. That's why we work aggressively to refine our understanding of models to make them work with simulation. Inside our progressive device modeling and characterization (DMC) laboratory, we develop accurate circuit simulation models and parameters. The DMC lab provides complete device model data for our processes using capabilities such as AC measurement, statistical analysis and worst-case modeling. Accurate models are a cornerstone of our design-for-quality approach.

To ensure high quality test vectors, production test vectors are derived from simulation vectors using the TSSI tools early in the design process. The industry-standard Zycad fault simulator is then used to determine fault coverage.

Physical design

Our PEGASYS layout system aids the mask designer through all physical design phases, ensuring consistency throughout the design cycle. This flexible, fully integrated environment supports a broad range of layout techniques, from full-custom to full-automation.

Capabilities include:

- Chip floor planning
- Analog device generators
- Schematic driven layout
- On-line point-to-point routing
- Compaction
- Automatic place and route
- Support of custom cells, standard cells, and compiled blocks in any combination
- Design rule checking (drc)
- Layout-versus-schematic verification (lvs)
- Parasitic extraction/back annotation
- Output in industry standard GDS format

In the first generation Pegasys system, Silicon Systems pioneered a device-generator based approach to precision analog layout. In partnership with Mentor Graphics, we have enhanced this technique for our current system, based on Mentor Graphics V8 ICstation® tools. ICstation® provides tremendous flexibility, combined with ease of customization, to fully support analog and mixed-signal designs. A variety of layout styles and techniques are combined to meet each chip's specific requirements. Rigorous verification checks ensure the quality and accuracy of the layout, for both physical and electrical properties. Post-layout simulation uses true parasitic modeling to handle remaining problems before first silicon fabrication.

STATE OF THE ART CMOS DIGITAL AND ANALOG PROCESSES

Silicon Systems offers four proven CMOS process technologies for creating cost effective, highly integrated systems solutions. These processes combine small geometry digital circuit capability with high performance analog capability. Table 1 summarizes Silicon Systems' CMOS process capabilities.

Our newest CK process is designed to support high breakdown, high current power FETs, 15V NPNs for specialized analog needs, poly capacitors and resistors, low noise differential amplifiers and high performance A/D and D/A converters. It also includes highly optimized and silicon area efficient digital cells including DSPs, microcontrollers, sequencers, memory managers and data paths.

The CJ process provides high performance analog and digital cells and includes the same analog and digital complex devices in our CK process.

Our CG process supports high-performance analog circuitry with precision poly-poly capacitors. Complex analog circuitry includes 1.25 Amp power FETs, 12-bit switched capacitor analog to digital converters and low distortion operational amplifiers and filters. Complex digital circuitry includes DSPs, microcontrollers, sequencers, memory mangers and data paths.

BIPOLAR & BICMOS PROCESS TECHNOLOGIES

Our bipolar MSICs take advantage of a high-performance Bipolar process, BN (for 5V applications).

BN - Low-power/ 8 GHz Bipolar at 5 volts

Because we employ full oxide isolation in our BN process, we can fabricate very fast, very small transistors and reduce sidewall capacitances. This supports not only high speed, but low power.

The BN process features high-performance NPN transistors to support mixing high-performance emitter coupled logic (ECL) with analog circuitry. To provide for strict TTL I/O compatibility, we use superior PtSi Schottky diodes.

The resulting speed and packing density allows you to effectively implement dense high-performance, low-power Bipolar analog/digital capability into your system designs.

For a feature-by-feature comparison of Silicon Systems' BN Bipolar process, see Table 3.

BiCMOS process technologies

Our BiCMOS process portfolio is expanding to support the evolving demands of the mixed-signal IC market. Now in production is our BCA process which combines 13 GHz NPNs with 1.0µ CMOS features to support the design of efficient, high performance, mixed-signal circuits. High bandwidth analog circuits can be combined with dense digital logic to support the development of 5V data channels with transfer rates into the 120+ Mbit/s range, while maintaining low power consumption. The BCA technology has also allowed our designers to develop 3V only circuits to address very low power applications.

Our second generation BiCMOS process, BCB, will provide the next step in performance with a parallel improvement in circuit density. BCB advances our BiCMOS with 0.8µ CMOS feature sizes and improved interconnect capability resulting in a significant performance step for CMOS logic. This will allow implementation of mixed-signal circuits that support data transfer rates well beyond 200 Mbit/s, while maintaining very low power dissipation. The dense digital advantages of BCB will also expand the possibilities for cost effective customization and programmability in both 5V and 3V environments.

For a summary of our BiCMOS processes see Table 2.

Process	Type	Application Voltage	BVDSS	Drawn Gate Length	Interconnect Pitches Poly 1	Metal 1	Metal 2	Features
CG	Si-Gate, dual metal, dual poly, PWell	5V	7V	1.5µ	3.0µ	4.5µ	6.0µ	• DDD S/D structure • Poly-poly capacitors • Shrinkable to 1.2µ
CJ	Si-Gate, dual metal, dual poly, NWell	5V	7V	1.0µ	2.0µ	3.0µ	3.3µ	• Ldd S/D structure • Poly-poly capacitors • Shrinkable to 0.8µ
CK	Si-Gate, dual metal, dual poly, NWell	5V	7V	0.8µ	1.6µ	2.0µ	2.4µ	• Ldd S/D structure • Poly-poly capacitors • Shrinkable to 0.5µ • High voltage FETs • 15V NPNs

TABLE 1: CMOS Process Chart

Process	Appl. Voltage	BVDSS	Drawn Gate Length	Interconnect Pitches Poly	M0	M1	M2	BV_{CEO}	NPN Ft	Emitter	Features
BCA:	5V	10V	1.0µ	2.6µ	3.2µ	3.8µ	5.0µ	8V	13 GHz	1.0µ	**Bipolar:** • High Performance NPNs • Polysilicon emitters • PtSi Schottky Diodes • Poly resisters • Gate Oxide Capacitors • Poly Capacitors • Sidewall Oxide Isolation • Fuses **CMOS:** • Lightly Doped Drains
BCB:	5V	8V	0.8µ	1.6µ	2.4µ	2.0µ	2.4µ	8V	15 GHz	0.8µ	

TABLE 2: BiCMOS Process Chart

Process	Type	BV_{CEO}	NPN Ft	Emitter Size	M1 Pitch	M2 Pitch	Features
BN	Oxide-isolated	6V	8 GHz	2.0µ	4.5µ	8.0µ	• High performance NPNs • PtSi Schottky diodes • Nitride capacitors • Ion implanted resistors • Sidewall oxide isolation • Collector/base plugs

TABLE 3: Bipolar Process Chart

A SUPERIOR FINISH FOR CMOS, BIPOLAR AND BICMOS

You might say this is the payoff window. The benefits of our process technologies, design tools and our unique custom approach all come together during wafer fabrication, test and assembly.

Our two manufacturing centers, located in Tustin and Santa Cruz, California, can offer specialized capabilities to match your particular fabrication requirements. Both facilities provide you with high resolution stepper photolithography technology, positive resist, dry plasma etch systems, high current ion implantation and automatic sputtering.

Fabrication sites in both Tustin and Santa Cruz accommodate 4- and 6-inch wafer fabrication and Bipolar, CMOS and BiCMOS processes.

The right package

Silicon Systems offers a wide range of packages to meet the small footprint requirements of advanced storage and communication products. We continue to be innovative in surface mount technology by providing PLCC, SO, VSOP, VTSOP, QFP, TQFP, VTQFP and UTQFP packages. At our ISO 9002-certified Singapore assembly & test facility we have the full capability to support high quality automated packaging while also maintaining rapid cycle times.

Promis. Quality through CAM

Process and Management Information System (PROMIS) underscores our commitment to computer-aided manufacturing (CAM). And to delivering you a superior quality product on time.

We use PROMIS to facilitate the data required in our manufacturing, monitoring and statistical process control (SPC) systems.

With PROMIS we more effectively manage our inventory, accurately track wafers in process, and closely monitor the clean room environment.

PROMIS also assists our SPC efforts, as does our commitment to fully train all of our manufacturing personnel in SPC basics.

We design for quality

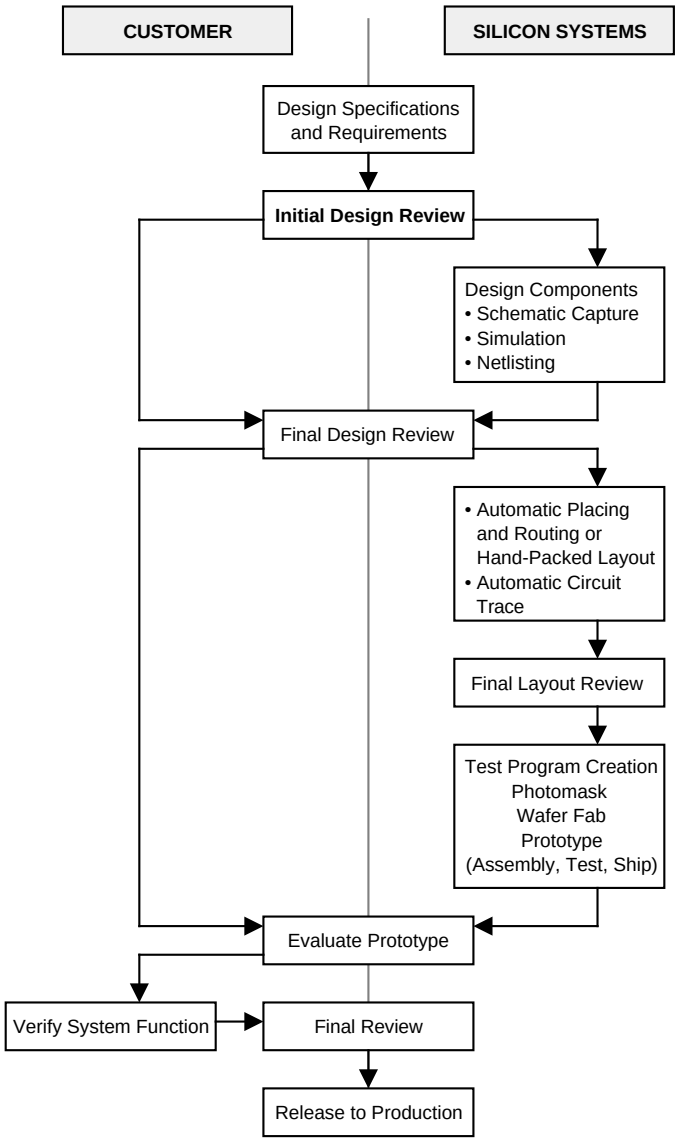
It's our view that quality is nothing less than absolute customer satisfaction. To achieve it, we begin far "upstream" in the product development process. Our design-for-quality approach scrutinizes the design itself with statistically based models, comprehensive simulation tools and vigorous design reviews.

The results of such an effort are IC products that boast lower defect rates, higher parametric performance and far fewer redesigns. Moreover, our persistence in improving quality keeps us focused on finding better and faster ways to satisfy future customer demands.

Quality that delivers

With effective systems such as PROMIS and our design-for-quality approach in place, Silicon Systems is prepared to deliver you finished products you can really depend on. On time. And within budget.

For details on how you can take best advantage of Silicon Systems' custom mixed-signal IC solutions, see your nearest Silicon Systems representative, or contact us. Silicon Systems, Inc. 14351 Myford Road, Tustin, CA 92680-7022. 714-573-6000. FAX: (714) 573-6914.



Customer Interface for Full-Custom and Cell-Based Designs

Section 2

QUALITY AND TECHNOLOGY

SECTION 1

1.1 INTRODUCTION

Silicon Systems is committed to the goal of customer satisfaction through the on-time delivery of defect free products that exceed the customer's expectations and requirements. This section outlines Silicon Systems' ongoing activities for the control and continual improvement of quality in every aspect of our organization.

Silicon Systems is diligently working to maintain and improve its position as a world-class provider of mixed-signal integrated circuits (MSICs®).

We realize and practice the concept that quality and reliability must be designed and built into our products. In addition, Silicon Systems utilizes rigid inspections and data analysis to evaluate the acceptability and variation existing in incoming materials and performs stringent outgoing quality verification. The manufacturing process flow is encompassed by an effective system of test/inspection checks and in-line monitors which focus on the control and reduction of process variation. These gates and monitors ensure precise adherence to prescribed standards and procedures.

Silicon Systems also incorporates the use of statistical process control techniques into company operations. The control and reduction of the process variation by the use of statistical problem solving techniques, analytical controls and other quantitative methods ensures that Silicon Systems' products maintain the highest levels of quality and reliability. Our Quality and Technology organizations are committed to working closely with our customers to provide assistance and a continually improving level of product quality.

1.2 SILICON SYSTEMS' QUALITY MANDATE: CONTINUOUS IMPROVEMENT

Continuous improvement is Silicon System's strategic thrust for the 1990's. In order to ensure that all aspects of our business are encompassed by this mandate, Corporate Quality and Technology has been chartered with the responsibility for developing, educating and overseeing the worldwide continuous improvement process. The continuous improvement initiative will lead to developing a new organizational culture, changing attitudes and stronger ownership and accountability for total customer satisfaction.

1.3 CHARACTERISTICS OF SILICON SYSTEMS' CONTINUOUS IMPROVEMENT PROCESS

- Executive Steering Committee leadership and direction - defines the right things to do and provides guidance - the right way to do them.
- Continuous improvement is measured everywhere and by everyone. Metrics that reflect pride in accomplishment are celebrated.
- Benchmarking is employed as a method to shorten learning curves and ensure successful ventures.
- Quality management and employee empowerment are encouraged at all levels.

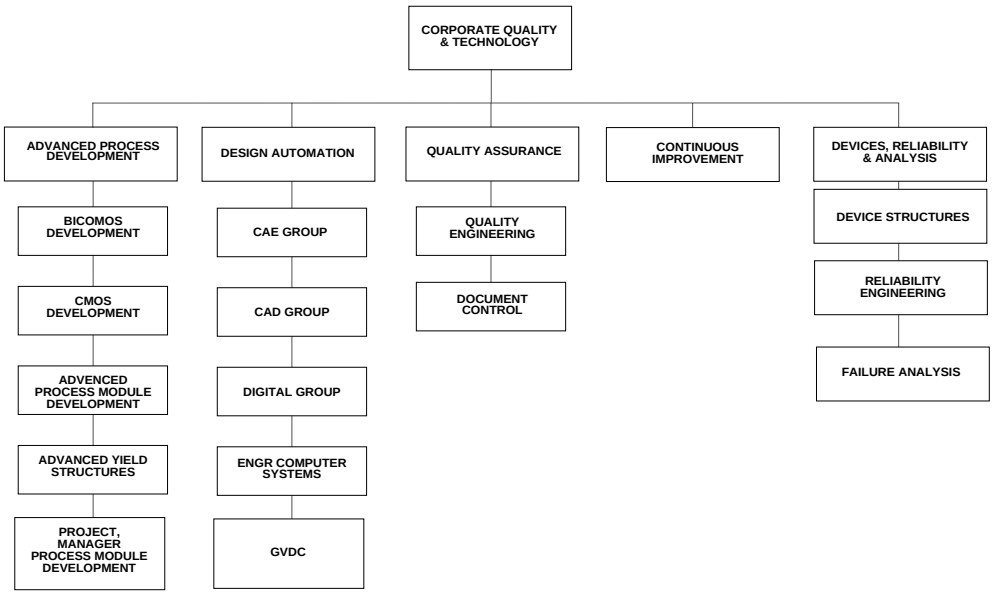


FIGURE 1: Organizational Chart

- Supplier partnership is a critical element of our quality strategy.

This is the essence of Silicon Systems - a total quality involved company - forward looking and immersed in the goal of customer satisfaction and best-in-class business pursuits.

1.4 CORPORATE QUALITY AND TECHNOLOGY

It is the objective of the Corporate Quality and Technology organization to ensure that proactive quality systems are in place to ensure that Silicon Systems' products will meet or exceed customer requirements and expectations. In addition, the Quality and Technology organization works to facilitate the timely implementation of solutions and monitors the effectiveness of corrective actions. These organizational strategies support the continuing enhancement of quality consciousness throughout Silicon Systems.

1.5 ISO 9000 CERTIFICATION

Silicon Systems has determined that ISO 9000 certification is an important strategy for achieving total customer satisfaction. Our Singapore assembly and test operations facility has been ISO 9002 certified through SISIR and our domestic facilities' quality systems have been ISO 9001 certified through Intertek. We believe strongly that ISO 9000 certification proves that Silicon Systems is doing the right things to do things right.

SECTION 2: QUALITY ASSURANCE

2.1 QUALITY OBJECTIVES

While all Silicon Systems employees have direct responsibility for quality in their functions, the Quality Assurance Organizations have the ultimate responsibility for the quality and reliability of our products. This is accomplished through the development, administration and assessment of formal quality systems which assure Silicon Systems' management, as well as our customers, that products will fulfill the requirements of customer purchase orders and all other specifications.

Corporate Quality Assurance supports, coordinates and actively participates in the formal qualification of suppliers, material, processes, and products, and the administration of quality systems to assure that our products meet Silicon Systems quality standards. Product Quality Assurance provides the liaison between Silicon Systems and the customer for all product quality related concerns. Manufacturing Quality Assurance administers the manufacturing quality systems and reports quality monitor data to the factory.

It is the practice of Silicon Systems to have corporate quality and reliability objectives encompass all of its activities. This starts with a strong commitment of support from the corporate level and continues with exceptional customer support long after the product has been shipped.

Silicon Systems emphasizes the belief that quality and reliability must be built into all of its products by ensuring that all employees are educated in the quality philosophy of the company. Some of the features built into Silicon Systems quality culture include:

1. Structured training programs directed at wafer fabrication, test, process control personnel and supporting organizations.
   - Team-based problem solving methodologies.
   - Corporate-wide training of quality philosophy and statistical methods.
2. Stringent in-process inspections, gates, and monitors.
3. Rigorous evaluation of designs, materials, and processing procedures.
4. Stringent electrical testing (100% and QC AQL/ Sample testing).
5. Ongoing reliability monitors and process verifications.
6. Real-time use of statistical process control methodology.
7. Corporate level audits of manufacturing, subcontractors, and suppliers.
8. Timely corrective action system.
9. Control of non-conforming material.

These focused quality methods result in products which deliver superior performance and reliability in the field.

2.2.1 INCOMING INSPECTIONS

Incoming inspection plays a key role in Silicon Systems' quality efforts. Small variations in incoming material can traverse the entire production cycle before being detected much later in the process. By paying strict attention to the monitoring of materials at the earliest possible stage, variation can be reduced, resulting in a stable uniform process.

2.2.2 IN-PROCESS INSPECTIONS

Silicon Systems has established key inspection monitors in the following strategic areas: wafer fabrication, wafer probe, assembly, and final test.

Quality control monitors have been integrated throughout the manufacturing flow, so that data may be collected and analyzed to verify the results of intermediary manufacturing steps. This data is used to document quality trends or long term improvements in the quality of specific operations.

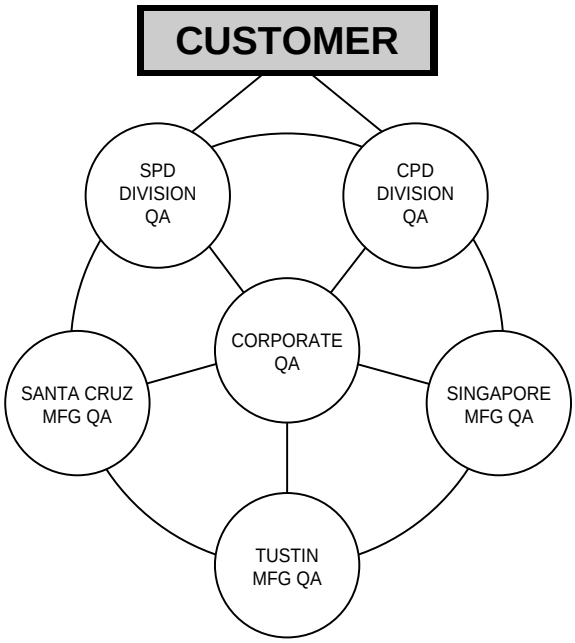


FIGURE 2
Quality Assurance Relationships
Quality Steering Committee

Abnormality control is being used to enhance the effectiveness of this process. In process monitors such as oxide integrity, electromigration immunity and other parameters monitor long term reliability as well as circuit performance.

2.3 QUALITY STEERING COMMITTEE

The Corporate, Product and Manufacturing Quality Assurance organizations work closely together to provide leadership in the development, integration and assessment of Silicon Systems' worldwide quality systems and procedures.

This team approach ensures that policies and procedures are standardized and facilitates rapid improvement in products, processes and services.

2.4 DESIGN FOR QUALITY

Since the foundation of a reliable product is rooted in the design process, the Quality and Technology organizations actively participate in comprehensive cross-functional reviews of design stages prior to the product's transition to production status. These review stages assure a predictable and effective development cycle. Other important design-related functions include ensuring that process specification revisions are translated into updated design parameters and the translation of manufacturing process capability into design guidelines. This is accomplished through the identification and monitoring of critical process and device parameters. Wafer level test at the early stages of process development also plays a critical role. These elements, included in Silicon Systems design for quality effort, support the development of robust design rules which are as insensitive as possible to inherent manufacturing variation. The result is a product that delivers predictable and reliable long term performance.

2.5 PPM REDUCTION PROGRAM

The primary purpose of a PPM reduction program is to provide a formalized feedback system in which data from nonconforming products can be used to improve future product consistency and reliability. The action portion of this program is accomplished in three stages:

1. Identification of defects by failure mode.
2. Identification of defect causes and initiation of corrective action.
3. Measurement of results and setting of improved goals.

The data summarized from the established PPM program is compiled as a ratio of units rejected/tested. This ratio is then expressed in terms of defective parts per million (PPM). Founded on a statistically valid database of PPM data and an established five-year strategic plan identifying PPM improvement goals, Silicon Systems has consistently achieved excellent quality standards and will continue to progressively improve PPM standards.

2.6 COMPUTER AIDED MANUFACTURING CONTROL

Computer Aided Manufacturing (CAM) is used throughout Silicon Systems for the identification, control, collection and dissemination of timely information for logistics control. Silicon Systems also uses this type of computerized system for statistical process control and manufacturing monitoring. PROMIS, (PROcess Management and Information System), displays approved/controlled recipes, processes, and procedures; tracks work-in-process; reports accurate inventory information; allows continuous recording of facilities data; contains statistical analysis capabilities; and much more. PROMIS allows for a paperless facility, a major element in minimizing contamination of clean room areas.

TEST	CONDITIONS	PURPOSE OF EVALUATION
Biased temperature/humidity	85°C/85° %RH	Resistance to high humidity with bias
Highly accelerated stress test (HAST)	JDEC A110	Evaluates package integrity
High temperature operating life (HTOL)	Mil 883D, Method 1005	Resistance to electrical and thermal stress
Early Failure Rate	Mil 883D, Method 1005	Detect infant mortality
Steam pressure	121°C/15PSI	Resistance to high humidity
Temperature cycling	Mil 883D, Method 1010	Resistance to thermal excursion (air)
Thermal shock	Mil 883D, Method 1011	Resistance to thermal excursion (liquid)
Salt atmosphere	Mil 883D, Method 1009	Resistance to corrosive environment
Constant acceleration	Mil 883D, Method 2001	Resistance to constant acceleration
Mechanical shock	Mil 883D, Method 2002	Resistance to mechanical shocks
Solderability	Mil 883D, Method 2003	Evaluates solderability of leads
Lead integrity	Mil 883D, Method 2004	Evaluates lead integrity before board assembly
Vibration, variable frequency	Mil 883D, Method 2007	Resistance to vibration
Thermal resistance	Silicon Systems Method	Evaluates thermal dissipation
Electrostatic damage	Mil 883D, Method 3015	Evaluates ESD susceptability
Latch-up	Silicon Systems Method	Evaluates latch-up susceptibility
Seal fine and gross leak	Mil Std 883D, Method 1014	Evaluates hermeticity of sealed packages

TABLE 1: Reliability Stress Tests

SECTION 3: RELIABILITY

3.1 RELIABILITY PROGRAM

A primary objective at Silicon Systems is to improve the reliability of our products through characterization of our manufacturing operations. The identification of specific failure mechanisms occuring in the wafer fabrication and assembly processes is a prerequisite to effective corrective action aimed at reducing defects and improving quality and reliability.

Silicon Systems has defined various programs that will characterize product reliability levels on a continuous basis. These programs can be categorically described by:

1. Qualifications
2. Production monitors
3. Evaluations
4. Failure analysis
5. Wafer level reliability
6. Data collection and presentation for improvement projects

3.2 QUALIFICATIONS

Extensive qualification testing and data collection ensures that all new product designs, processes, and packaging configurations meet the absolute maximum ratings of design and the worst case performance criteria for end users. A large database generated by means of accelerated stress testing results in a high degree of confidence in predicting final use performance. The qualification criteria used are periodically reviewed to be consistent with Silicon Systems' increasing quality and reliability goals in support of our customers.

3.3 PRODUCTION MONITORS

This program has been established to randomly select a statistically significant sample of production products for subjection to maximum stress test levels in order to evaluate the useful life of the product in a field use environment.

Table 1 lists reliability test methods that are in use at Silicon Systems. This analysis of production monitor at Silicon Systems provides valuable information on possible design/process changes which assure continued improved reliability. The monitors are periodically reviewed for effectiveness and improvements.

3.4 EVALUATIONS

The evaluation program at Silicon Systems is an ongoing effort that defines standards which address the reliability assessment of the circuit design, process parameters, and package of a new product. This program continuously analyzes updated performance characteristics of product as they undergo improvement efforts at Silicon Systems.

3.5 FAILURE ANALYSIS

The failure analysis function is an integral part of the Quality and Technology department at Silicon Systems. Silicon Systems has assembled a highly technical and sophisticated failure analysis laboratory and staff. This laboratory provides visual analysis, electrical reject mode analysis, and both destructive and non-destructive data to aid the engineers in developing corrective action for improvement. These test analyses may include metallurgical, optical, chemical, electrical, SEM with X-ray dispersive analysis, and E-Beam non-contact analysis as needed.

These conclusive in-house testing and analysis techniques, are complemented by outside support, such as scanning acoustic microscopy, focused ion beam, and complete surface and material analysis. This allows Silicon Systems to monitor all aspects of product manufacturing to ensure that the product of highest quality is shipped to our customers.

3.6 WAFER LEVEL RELIABILITY PROGRAM

The primary advantage of wafer level reliability testing is the speed at which results can be derived, thereby providing additional response time and an early warning of process changes. This tool provides Silicon Systems with a very rapid analysis tool which allows for the early identification of possible problems and a determination of their origin.

The continuous improvement approach taken at Silicon Systems uses wafer level reliability tests as tools to improve the process, identify potential problems, determine the sources of any process weakness and eliminate problems upstream in the process. This results in a focus on reliability improvement that goes well beyond merely determining the projected lifetime of a product to a detailed characterization, measurement and control of the specific parameters which actuallly determine product lifetime.

3.7 DATA COLLECTION AND PRESENTATION FOR IMPROVEMENT PROJECTS

Data collected from each element of the Reliability program is summarized for scope and impact and distributed among all engineering disciplines in the company. This data facilitates improvement and provides our customers an opportunity to review the performance of our product.

3.8 RELIABILITY METHODS

The Reliability Program utilizes a number of stress tests that are presently being used to define performance levels of our products. Many of these stress tests are per MIL-STD-883D as shown in Table 1.

3.9 RELIABILITY PREDICTION METHODOLOGY

At Silicon Systems, the Arrhenius model is used to relate a failure rate at an accelerated temperature test condition to a normal use temperature condition.

The model basically states $FR = A \exp(-Ea/KT)$

Where:

- FR = Failure rate
- A = Constant
- Ea = Activation Energy (eV)
- K = Boltzmann's constant 8.62×10^{-5} eV/ degree K
- T = Absolute temperature (degree K)

3.10 ESD PREVENTION

Silicon Systems recognizes that the protection of Electrostatic Discharge (ESD) sensitive devices from damage by electrical transients and static electricity is vital. ESD safe procedures are incorporated throughout all operations which come in contact with these devices. Continuous improvement in the ESD protection levels is being accomplished through the incorporation of increasingly robust protection devices during the circuit design process as well as work area improvements.

Silicon Systems' quality activity incorporates several protection measures for the control of ESD. Some of the preventive measures include handling of parts at static safe-guarded workstations, the wearing of wrist straps during all handling operations, the use of conductive lab coats in all test areas and all areas which handle parts and the packaging of components in conductive or anti-static containers.

Section 3

K-SERIES SINGLE-CHIP MODEM FAMILY

Introduction

Silicon Systems' K-Series Family of One-Chip Modems

Silicon Systems is a leader in the design and manufacturing of CMOS VLSI modems. Currently, Silicon Systems offers the most extensive line of one-chip modem ICs available, with high-performance, cost-effective designs suitable for a wide range of applications. Silicon Systems' fully compatible modem IC family has redefined the modem IC as a universal component which can be easily integrated into any system. Designs can be upgraded to meet different standards and speeds by simply substituting one K-Series IC for another. Using a K-Series family modem IC in your application eliminates product obsolesence, and minimizes development costs.

The Silicon Systems K-series modem IC family consists of four basic products:

1. The SSI 73K222AL, a multi-mode device which combines both Bell 212A/103 and V.22/V.21 capability in one chip, with operating modes at 0 - 30, 600 and 1200 bit/s.

2. The SSI 73K222U which combines the functionality of the 73K222AL with the industry standard 16C450 UART.

3. The SSI 73K224L, a major technological breakthrough which provides 2400 bit/s V.22bis operation in addition to V.22/V.21 and Bell 212A/ 103 modes in a single IC.

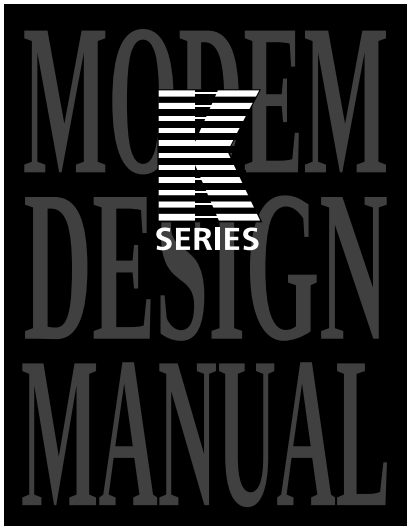
4. The SSI 73K322L provides CCITT V.22/V.21 plus V.23 modes.

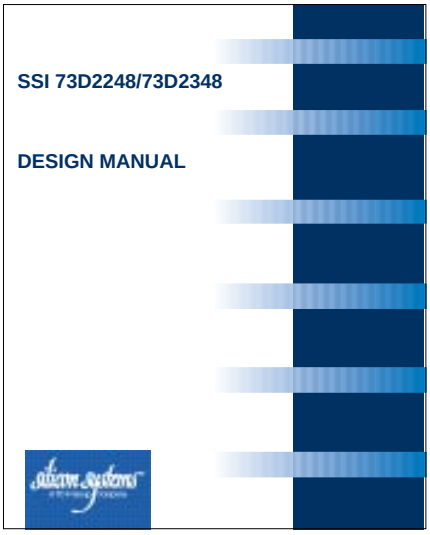
New additions to Silicon Systems' modem IC family extend the available operating modes and provide features which greatly simplify modem design. The SSI 73K324L offers V.22bis, V.22/V.21 and V.23 operating modes on one chip. These products dramatically reduce external circuitry required for dedicated integral modem designs.

Silicon Systems' one-chip modem IC products represent technical achievements unmatched in the industry. An advanced Digital Signal Processor resides on the same chip with sophisticated analog circuitry in the SSI 73K224L and SSI 73K324L products. "U" versions of the K-Series devices integrate an industry standard UART with full modem capability on a single chip. In addition, an innovative bus structure makes a separate controller unnecessary in dedicated integral designs.

K-Series Modem Design Manual

The Silicon Systems K-Series Modem Design Manual contains a large body of application literature for the K-Series family of single chip modem products. This manual is intended as a tutorial for those users who may be designing with modems for the first time, and also as a helpful guide for more experienced modem designers.





The K-Series Modem Design Manual is available through our worldwide network of representatives and distributors.

SSI 73K212AL
Bell 212A/103
Single-Chip Modem

January 1996

DESCRIPTION

The SSI 73K212AL is a highly integrated single-chip modem IC which provides the functions needed to construct a typical Bell 212A full-duplex modem. Using an advanced CMOS process that integrates analog, digital and switched–capacitor filter functions on a single substrate, the SSI 73K212AL offers excellent performance and a high level of functional integration in a single 28-Lead PLCC, 28- or 22-pin DIP configuration. The SSI 73K212AL operates from a single +5V supply. The SSI 73K212AL is a new version replacing the SSI 73K212L. The SSI 73K212AL should be specified for all new designs.

The SSI 73K212AL includes the DPSK and FSK modulator/demodulator functions, call progress and handshake tone monitor test modes and a DTMF dialer. This device supports all Bell 212A modes of operation allowing both synchronous and asychronous communications.

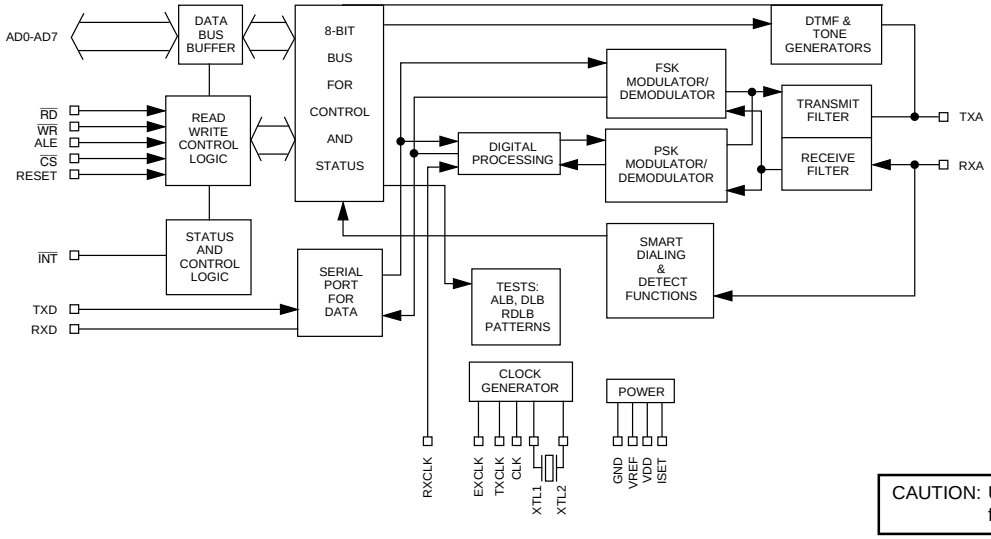
Test features such as analog loop, digital loop, and remote digital loopback are provided. Internal pattern generators are also included for self-testing. The SSI 73K212AL is designed to appear to the systems designer as a microprocessor peripheral, and will easily interface with popular one-chip microprocessors

(continued)

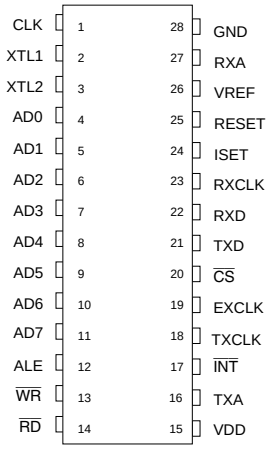
FEATURES

- **One-chip Bell 212A and 103 standard compatible modem data pump**
- **Full-duplex operation at 0-300 bit/s (FSK) or 1200 bit/s (DPSK)**
- **Pin and software compatible with other SSI K-Series 1-chip modems**
- **Interfaces directly with standard microprocessors (8048, 80C51 typical)**
- **Serial or parallel microprocessor bus for control**
- **Serial port for data transfer**
- **Both synchronous and asynchronous modes of operation**
- **Call progress, carrier, precise answer tone and long loop detectors**
- **DTMF generators**
- **Test modes available: ALB, DL, RDL, Mark, Space, Alternating bit patterns**
- **Precise automatic gain control allows 45 dB dynamic range**
- **CMOS technology for low power consumption using 30 mW @ 5V**
- **Single +5V supply**

BLOCK DIAGRAM



PIN DIAGRAM



CAUTION: Use handling procedures necessary for a static sensitive component.

DESCRIPTION (continued)

(80C51 typical) for control of modem functions through its 8-bit multiplexed address/data bus or serial control bus. An ALE control line simplifies address demultiplexing. Data communications occurs through a separate serial port only.

The SSI 73K212AL is ideal for use in either free standing or integral system modem products where full-duplex 1200 bit/s data communications over the 2-wire switched telephone network is desired. Its high functionality, low power consumption and efficient packaging simplify design requirements and increase system reliability. A complete modem requires only the addition of the phone line interface, a control microprocessor, and RS-232 level convertor for a typical system. The SSI 73K212AL is part of SSi's K-Series family of pin and function compatible single-chip modem products. These devices allow systems to be configured for higher speeds and Bell or CCITT operation with only a single component change.

OPERATION

ASYNCHRONOUS MODE

Data transmission for the DPSK mode requires that data ultimately be transmitted in a synchronous fashion. The SSI 73K212AL includes ASYNC/SYNC and SYNC/ASYNC converters which delete or insert stop bits in order to transmit data within a 0.01% rate. In asynchronous mode the serial data comes from the TXD pin into the ASYNC/SYNC converter. The ASYNC/SYNC converter accepts the data provided on the TXD pin which normally must be 1200 bit/s +1.0%, -2.5%. The rate converter will then insert or delete stop bits in order to output a signal which is 1200 bit/s ± .01% (±0.01% is the required synchronous data rate accuracy).

The serial data stream from the ASYNC/SYNC converter is passed through the data scrambler and onto the analog modulator. The data scrambler can be bypassed under processor control when unscrambled data must be transmitted. The ASYNC/SYNC rate converter and the data scrambler are bypassed in all FSK modes. If serial input data contains a break signal through one character (including start and stop bits) the break will be extended to at least 2 • N + 3 bits long (where N is the number of transmitted bits/character). Serial data from the demodulator is passed first through the data descrambler and then through the SYNC/ASYNC rate converter. The SYNC/ASYNC convertor will reinsert any deleted stop bits and transmit output data at an intra-character rate (bit-to-bit timing) of no greater than 1219 bit/s. An incoming break signal (low through two characters) will be passed through without incorrectly inserting a stop bit.

SYNCHRONOUS MODE

The Bell 212A standard defines synchronous operation only at 1200 bit/s. Operation is similar to that of the asynchronous mode except that data must be synchronized to a provided clock and no variation in data transfer rate is allowable. Serial input data appearing at TXD must be valid on the rising edge of TXCLK.

TXCLK is an internally derived 1200 Hz signal in internal mode and is connected internally to the RXCLK pin in slave mode. Receive data at the RXD pin is clocked out on the falling edge of RXCLK. The ASYNCH/SYNCH converter is bypassed when synchronous mode is selected and data is transmitted out at the same rate as it is input.

DPSK MODULATOR/DEMODULATOR

The SSSI 73K212AL modulates a serial bit stream into dibit pairs that are represented by four possible phase shifts as prescribed by the Bell 212A standard. The baseband signal is then filtered to reduce intersymbol interference on the bandlimited 2-wire telephone line. Transmission occurs using either a 1200 Hz (originate mode) or 2400 Hz carrier (answer mode). Demodulation is the reverse of the modulation process, with the incoming analog signal eventually decoded into di-bits and converted back to a serial bit stream. The demodulator also recovers the clock which was encoded into the analog signal during modulation. Demodulation occurs using either a 1200 Hz carrier (answer mode or ALB originate mode) or a 2400 Hz carrier (originate mode or ALB answer mode). The SSI 73K212AL uses a phase locked loop coherent demodulation technique for optimum receiver performance.

FSK MODULATOR/DEMODULATOR

The FSK modulator produces a frequency modulated analog output signal using two discrete frequencies to

represent the binary data. In the Bell 103, the standard frequencies of 1270 and 1070 Hz (originate, mark and space) or 2225 and 2025 Hz (answer, mark and space) are used. V.21 mode uses 980 and 1180 Hz (originate, mark and space) or 1650 and 1850 Hz (answer, mark and space). Demodulation involves detecting the received frequencies and decoding them into the appropriate binary value. The rate converter and scrambler/descrambler are bypassed in the 103 mode.

PASSBAND FILTERS AND EQUALIZERS

High and low band filters are included to shape the amplitude and phase response of the transmit and receive signals and provide compromise delay equalization and rejection of out-of-band signals in the receive channel. Amplitude and phase equalization are necessary to compensate for distortion of the transmission line and to reduce intersymbol interference in the bandlimited receive signal. The transmit signal filtering approximates a 75% square root of raised Cosine frequency response characteristic.

AGC

The automatic gain control maintains a signal level at the input to the demodulators which is constant to within 1 dB. It corrects quickly for increases in signal which would cause clipping and provides a total receiver dynamic range of >45 dB.

PARALLEL BUS INTERFACE

Four 8-bit registers are provided for control, option select and status monitoring. These registers are addressed with the AD0, AD1, and AD2 multiplexed address lines (latched by ALE) and appear to a control microprocessor as four consecutive memory locations. Two control registers and the tone register are read/write memory. The status detect register is read only and cannot be modified except by modem response to monitored parameters.

SERIAL COMMAND INTERFACE

The serial command mode allows access to the SSI 73K212AL control and status registers via a serial command port (22-pin version only). In this mode the A0 , A1 and A2 lines provide register addresses for data passed through the data pin under control of the $\overline{RD}$ and $\overline{WR}$ lines. A read operation is initiated when the $\overline{RD}$ line is taken low. The next eight cycles of EXCLK will then transfer out eight bits of the selected address location LSB first. A write takes place by shifting in eight bits of data LSB first for eight consecutive cycles of EXCLK. $\overline{WR}$ is then pulsed low and data transferred into the selected register occurs on the rising edge of $\overline{WR}$.

SPECIAL DETECT CIRCUITRY

The special detect circuitry monitors the received analog signal to determine status or presence of carrier, call-progress tones, answer tone and weak received signal, (long loop condition). An unscrambled mark request signal is also detected when the received data out of the DPSK demodulator before the descrambler has been high for 165.5 ms $\pm$ 6.5 ms minimum. The appropriate detect register bit is set when one of these conditions changes and an interrupt is generated for all purposes except long loop. The interrupts are disabled (masked) when the enable interrupt bit is set to 0.

DTMF GENERATOR

The DTMF generator will output one of 16 standard tone pairs determined by a 4-bit binary value and TX DTMF mode bit previously loaded into the tone register. Tone generation is initiated when the DTMF mode is selected using the tone register and the transmit enable (CR0 bit D1) is changed from 0 to 1.

PIN DESCRIPTION

POWER

NAME	28-PIN	22-PIN	TYPE	DESCRIPTION
GND	28	1	I	System Ground.
VDD	15	11	I	Power supply input, 5V ± 10%. Bypass with 0.1 and 22 μF capacitors to ground.
VREF	26	21	O	An internally generated reference voltage. Bypass with 0.1 μF capacitor to GND.
ISET	24	19	I	Chip current reference. Sets bias current for op-amps. The chip current is set by connecting this pin to VDD through a 2 MΩ resistor. ISET should be bypassed to GND with a 0.1 μF capacitor.

PARALLEL MICROPROCESSOR INTERFACE

ALE	12	-	I	Address latch enable. The falling edge of ALE latches the address on AD0-AD2 and the chip select on $\overline{CS}$.
AD0-AD7	4-11	-	I/O	Address/data bus. These bidirectional tri-state multiplexed lines carry information to and from the internal registers.
$\overline{CS}$	20	-	I	Chip select. A low during the falling edge of ALE on this pin allows a read cycle or a write cycle to occur. AD0-AD7 will not be driven and no registers will be written if $\overline{CS}$ (latched) is not active. The state of $\overline{CS}$ is latched on the falling edge of ALE.
CLK	1	2	O	Output clock. This pin is selectable under processor control to be either the crystal frequency (for use as a processor clock) or 16x the data rate for use as a baud rate clock in DPSK modes only. The pin defaults to the crystal frequency on reset.
$\overline{INT}$	17	13	O	Interrupt. This open drain output signal is used to inform the processor that a detect flag has occurred. The processor must then read the detect register to determine which detect triggered the interrupt. $\overline{INT}$ will stay low until the processor reads the detect register or does a full reset.
$\overline{RD}$	14	-	I	Read. A low requests a read of the SSI 73K212AL internal registers. Data cannot be output unless both $\overline{RD}$ and the latched $\overline{CS}$ are active or low.

PARALLEL MICROPROCESSOR INTERFACE (continued)

NAME	28-PIN	22-PIN	TYPE	DESCRIPTION
RESET	25	20	I	Reset. An active high signal on this pin will put the chip into an inactive state. All control register bits (CR0, CR1, Tone) will be reset. The output of the CLK pin will be set to the crystal frequency. An internal pull down resistor permits power on reset using a capacitor to VDD.
$\overline{WR}$	13	-	I	Write. A low on this informs the SSI 73K212AL that data is available on AD0-AD7 for writing into an internal register. Data is latched on the rising edge of $\overline{WR}$. No data is written unless both $\overline{WR}$ and the latched $\overline{CS}$ are low.

SERIAL MICROPROCESSOR INTERFACE

A0-A2	-	5-7	I	Register Address Selection. These lines carry register addresses and should be valid during any read or write operation.
DATA	-	8	I/O	Serial Control Data. Data for a read/write operation is clocked in or out on the falling edge of the EXCLK pin. The direction of data flow is controlled by the $\overline{RD}$ pin. $\overline{RD}$ low outputs data. $\overline{RD}$ high inputs data.
$\overline{RD}$	-	10	I	Read. A low on this input informs the SSI 73K212AL that data or status information is being read by the processor. The falling edge of the $\overline{RD}$ signal will initiate a read from the addressed register. The $\overline{RD}$ signal must continue for eight falling edges of EXCLK in order to read all eight bits of the referenced register. Read data is provided LSB first. Data will not be output unless the $\overline{RD}$ signal is active.
$\overline{WR}$	-	9	I	Write. A low on this input informs the SSI 73K212AL that data or status information has been shifted in through the DATA pin and is available for writing to an internal register. The normal procedure for a write is to shift in data LSB first on the DATA pin for eight consecutive falling edges of EXCLK and then to pulse $\overline{WR}$ low. Data is written on the rising edge of $\overline{WR}$.
Note:	In the serial, 22-pin version, the pins AD0-AD7, ALE and $\overline{CS}$ are removed and replaced with the pins; A0, A1, A2, DATA, and an unconnected pin. Also, the $\overline{RD}$ and $\overline{WR}$ controls are used differently. The Serial Control mode is provided in the parallel control versions by tying ALE high and $\overline{CS}$ low. In this configuration AD7 becomes DATA and AD0, AD1 and AD2 become A0, A1 and A2, respectively.			

DTE USER INTERFACE

NAME	28-PIN	22-PIN	TYPE	DESCRIPTION
EXCLK	19	15	I	External Clock. This signal is used in synchronous transmission when the external timing option has been selected. In the external timing mode the rising edge of EXCLK is used to strobe synchronous DPSK transmit data applied to the TXD pin. Also used for serial control interface.
RXCLK	23	18	O	Receive Clock. The falling edge of this clock output is coincident with the transitions in the serial received data output. The rising edge of RXCLK can be used to latch the valid output data. RXCLK will be valid as long as a carrier is present.
RXD	22	17	O/Weak pull-up	Received Data Output. Serial receive data is available on this pin. The data is always valid on the rising edge of RXCLK when in synchronous mode. RXD will output constant marks if no carrier is detected.
TXCLK	18	14	O	Transmit Clock. This signal is used in synchronous transmission to latch serial input data on the TXD pin. Data must be provided so that valid data is available on the rising edge of the TXCLK. The transmit clock is derived from different sources depending upon the synchronization mode selection. In Internal Mode the clock is generated internally. In External Mode TXCLK is phase locked to the EXCLK pin. In Slave Mode TXCLK is phase locked to the RXCLK pin. TXCLK is always active.
TXD	21	16	I	Transmit Data Input. Serial data for transmission is applied on this pin. In synchronous modes, the data must be valid on the rising edge of the TXCLK clock. In asynchronous modes (1200 bit/s or 300 baud) no clocking is necessary. DPSK data must be 1200 bit/s +1%, -2.5%.

ANALOG INTERFACE AND OSCILLATOR

RXA	27	22	I	Received modulated analog signal input from the telephone line interface.
TXA	16	12	O	Transmit analog output to the telephone line interface.
XTL1 XTL2	2 3	3 4	I I	These pins are for the internal crystal oscillator requiring a 11.0592 MHz parallel mode crystal and two load capacitors to Ground. Consult crystal manufacturer for proper valves. XTL2 can also be driven from an external clock.

REGISTER DESCRIPTIONS

Four 8-bit internal registers are accessible for control and status monitoring. The registers are accessed in read or write operations by addressing the A0, A1 and A2 address lines in serial mode, or the AD0, AD1 and AD2 lines in parallel mode. In parallel mode the address lines are latched by ALE. Register CR0 controls the method by which data is transferred over the phone line. CR1 controls the interface between the microprocessor and the SSI 73K212AL internal state. DR is a detect register which provides an indication of monitored modem status conditions. TR, the tone control register, controls the DTMF generator, answer and guard tones and RXD output gate used in the modem initial connect sequence. All registers are read/write except for DR which is read only. Register control and status bits are identified below:

REGISTER BIT SUMMARY

	ADDRESS	DATA BIT NUMBER							
REGISTER	AD2 - AD0	D7	D6	D5	D4	D3	D2	D1	D0
CONTROL REGISTER 0 CR0	000	0	0	TRANSMIT MODE 3	TRANSMIT MODE 2	TRANSMIT MODE 1	TRANSMIT MODE 0	TRANSMIT ENABLE	ANSWER/ ORIGINATE
CONTROL REGISTER 1 CR1	001	TRANSMIT PATTERN 1	TRANSMIT PATTERN 0	ENABLE DETECT INTERRUPT	BYPASS SCRAMBLER	CLK CONTROL	RESET	TEST MODE 1	TEST MODE 0
DETECT REGISTER DR	010	X	X	RECEIVE DATA	UNSCR. MARKS	CARRIER DETECT	ANSWER TONE	CALL PROGRESS	LONG LOOP
TONE CONTROL REGISTER TR	011	RXD OUTPUT CONTROL	0	TRANSMIT ANSWER TONE	TRANSMIT DTMF	DTMF3	DTMF2	DTMF1	DTMF0
CONTROL REGISTER 2 CR2	100	X	X	X	THESE REGISTER LOCATIONS ARE RESERVED FOR				X
CONTROL REGISTER 3 CR3	101	X	X	X	USE WITH OTHER K-SERIES FAMILY MEMBERS				X
ID REGISTER ID	110	ID	ID	ID	ID	X	X	X	X

NOTE: When a register containing reserved control bits is written into, the reserved bits must be programmed as 0's.

X = Undefined. State not guaranteed. Mask in software.

REGISTER ADDRESS TABLE

	ADDRESS	DATA BIT NUMBER							
REGISTER	**AD2 - AD0**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
CONTROL REGISTER 0 CR0	**000**	**0**	**0**	**TRANSMIT MODE 3**	**TRANSMIT MODE 2**	**TRANSMIT MODE 1**	**TRANSMIT MODE 0**	**TRANSMIT ENABLE**	**ORIGINATE/ ANSWER**
				0000=PWR DOWN 0001=INT SYNCH 0010=EXT SYNCH 0011=SLAVE SYNCH 0100=ASYNCH 8 BITS/CHAR 0101=ASYNCH 9 BITS/CHAR 0110=ASYNCH 10 BITS/CHAR 0111=ASYNCH 11 BITS/CHAR 1100=FSK				0=DISABLE TXA OUTPUT 1=ENABLE TXA OUTPUT	0=ANSWER 1=ORIGINATE
CONTROL REGISTER 1 CR1	**001**	**TRANSMIT PATTERN 1**	**TRANSMIT PATTERN 0**	**ENABLE DETECT INTERRUPT**	**BYPASS SCRAMBLER**	**CLK CONTROL**	**RESET**	**TEST MODE 1**	**TEST MODE 0**
		00=TX DATA 01=TX ALTERNATE 10=TX MARK 11=TX SPACE		0=DISABLE 1=ENABLE	0=NORMAL 1=BYPASS SCRAMBLER	0=XTAL 1=16 X DATA RATE OUTPUT AT CLK PIN IN DPSK MODE ONLY	0=NORMAL 1=RESET	00=NORMAL 01=ANALOG LOOPBACK 10=REMOTE DIGITAL LOOPBACK 11=LOCAL DIGITAL LOOPBACK	
DETECT REGISTER DR	**010**	**X**	**X**	**RECEIVE DATA**	**UNSCR. MARKS**	**CARRIER DETECT**	**ANSWER TONE**	**CALL PROGRESS**	**LONG LOOP**
				OUTPUTS RECEIVED DATA STREAM	0=CONDITION NOT DETECTED 1=CONDITION DETECTED				
TONE CONTROL REGISTER TR	**011**	**RXD OUTPUT CONTROL**	**0**	**TRANSMIT ANSWER TONE**	**TRANSMIT DTMF**	**DTMF3**	**DTMF2**	**DTMF1**	**DTMF0**
		RXD PIN 0=NORMAL 1=TRI STATE		0=OFF 1=ON	0=DATA 1=TX DTMF	4 BIT CODE FOR 1 OF 16 DUAL TONE COMBINATIONS.			
ID REGISTER 10	**110**	**ID**	**ID**	**ID**	**ID**	**X**	**X**	**X**	**X**

00XX=73K212AL, 322L, 321L
01XX=73K221AL, 302L
10XX=73K222AL
1100=73K224L
1110=73K324L
1101=73K312L

X = Undefined mask in software

CONTROL REGISTER 0

	D7	D6	D5	D4	D3	D2	D1	D0
CR0 000	0	0	TRANSMIT MODE 3	TRANSMIT MODE 2	TRANSMIT MODE 1	TRANSMIT MODE 0	TRANSMIT ENABLE	ANSWER/ ORIGINATE

BIT NO.	NAME	CONDITION	DESCRIPTION
D0	Answer/ Originate	0	Selects answer mode (transmit in high band, receive in low band).
		1	Selects originate mode (transmit in low band, receive in high band).
D1	Transmit Enable	0	Disables transmit output at TXA.
		1	Enables transmit output at TXA.
			Note: Answer tone and DTMF TX control require TX enable.
D5, D4,D3, D2	Transmit Mode	D5 D4 D3 D2	
		0 0 0 0	Selects power down mode. All functions disabled except digital interface.
		0 0 0 1	Internal synchronous mode. In this mode TXCLK is an internally derived 1200 Hz signal. Serial input data appearing at TXD must be valid on the rising edge of TXCLK. Receive data is clocked out of RXD on the falling edge of RXCLK.
		0 0 1 0	External synchronous mode. Operation is identical to internal synchronous, but TXCLK is connected internally to EXCLK pin, and a 1200 Hz clock must be supplied externally.
		0 0 1 1	Slave synchronous mode. Same operation as other synchronous modes. TXCLK is connected internally to the RXCLK pin in this mode.
		0 1 0 0	Selects DPSK asynchronous mode - 8 bits/character (1 start bit, 6 data bits, 1 stop bit).
		0 1 0 1	Selects DPSK asynchronous mode - 9 bits/character (1 start bit, 7 data bits, 1 stop bit).
		0 1 1 0	Selects DPSK asynchronous mode - 10 bits/character (1 start bit, 8 data bits, 1 stop bit).
		0 1 1 1	Selects DPSK asynchronous mode - 11 bits/character (1 start bit, 8 data bits, Parity and 1 stop or 2 stop bits).
		1 1 0 0	Selects FSK operation.
D6, D7		0	Not used, must be written as "0."

CONTROL REGISTER 1

	D7	D6	D5	D4	D3	D2	D1	D0
CR1 001	TRANSMIT PATTERN 1	TRANSMIT PATTERN 0	ENABLE DETECT INTER.	BYPASS SCRAMB	CLK CONTROL	RESET	TEST MODE 1	TEST MODE 0

BIT NO.	NAME	CONDITION	DESCRIPTION
D1, D0	Test Mode	D1 D0	
		0 0	Selects normal operating mode.
		0 1	Analog loopback mode. Loops the transmitted analog signal back to the receiver, and causes the receiver to use the same center frequency as the transmitter. To squelch the TXA pin, transmit enable bit must be low.
		1 0	Selects remote digital loopback. Received data is looped back to transmit data internally, and RXD is forced to a mark. Data on TXD is ignored.
		1 1	Selects local digital loopback. Internally loops TXD back to RXD and continues to transmit data carrier at the TXA pin.
D2	Reset	0	Selects normal operation.
		1	Resets modem to power down state. All control register bits (CR0, CR1, Tone) are reset to zero. The output of the CLK pin will be set to the crystal frequency on reset.
D3	CLK Control (Clock Control)	0	Selects 11.0592 MHz crystal echo output at CLK pin.
		1	Selects 16x the data rate, output at CLK pin in DPSK modes only.
D4	Bypass	0 Scrambler	Selects normal operation. DPSK transmit data is passed through scrambler.
		1	Selects Scrambler Bypass. Bypass DPSK data is routed around scrambler in the transmit path.
D5	Enable Detect Interrupt	0	Disables interrupt at $\overline{INT}$ pin.
		1	Enables $\overline{INT}$ output. An interrupts will be generated with a change in status of DR bits D1-D4. The answer tone and call progress detect interrupts are masked when the TX enable bit is set. Carrier detect is masked when TX DTMF is activated. All interrupts will be disabled if the device is in power down mode.

CONTROL REGISTER 1 (continued)

	D7	D6	D5	D4	D3	D2	D1	D0
CR1 001	TRANSMIT PATTERN 1	TRANSMIT PATTERN 0	ENABLE DETECT INTER.	BYPASS SCRAMB	CLK CONTROL	RESET	TEST MODE 1	TEST MODE 0

BIT NO.	NAME	CONDITION	DESCRIPTION
D7, D6	Transmit Pattern	D7 D6	
		0 0	Selects normal data transmission as controlled by the state of the TXD pin.
		0 1	Selects an alternating mark/space transmit pattern for modem testing.
		1 0	Selects a constant mark transmit pattern.
		1 1	Selects a constant space transmit pattern.

DETECT REGISTER

	D7	D6	D5	D4	D3	D2	D1	D0
DR 010	X	X	RECEIVE DATA	UNSCR. MARK	CARR. DETECT	ANSWER TONE	CALL PROG.	LONG LOOP

BIT NO.	NAME	CONDITION	DESCRIPTION
D0	LONG LOOP	0	Indicates normal received signal.
		1	Indicates low received signal.
D1	CALL PROGRESS DETECT	0	No call progress tone detected.
		1	Indicates presence of call progress tones. The call progress detection circuitry is activated by energy in the 350 to 620 Hz call progress band.
D2	ANSWER TONE DETECT	0	No answer tone detected.
		1	Indicates detection of 2225 Hz answer tone. The device must be in originate mode for detection of answer tone.
D3	CARRIER DETECT	0	No carrier detected in the receive channel.
		1	Indicated carrier has been detected in the received channel.
D4	UNSCRAM-BLED MARK	0	No unscrambled mark.
		1	Indicates detection of unscrambled marks in the received data. A valid indication requires that unscrambled marks be received for >165.5 ± 6.5 ms.

DETECT REGISTER (continued)

	D7	D6	D5	D4	D3	D2	D1	D0
DR 010	X	X	RECEIVE DATA	UNSCR. MARK	CARR. DETECT	ANSWER TONE	CALL PROG.	LONG LOOP

BIT NO.	NAME	CONDITION	DESCRIPTION
D5	RECEIVE DATA		Continuously outputs the received data stream. This data is the same as that output on the RXD pin, but it is not disabled when RXD is tri-stated.
D6, D7			Not used. Mask in software.

TONE REGISTER

	D7	D6	D5	D4	D3	D2	D1	D0
TR 011	RXD OUTPUT CONTR.		TRANSMIT ANSWER TONE	TRANSMIT DTMF	DTMF 3	DTMF 2	DTMF 1	DTMF 0

BIT NO.	NAME	CONDITION	DESCRIPTION
D3, D2, D1, D0	DTMF	D3 D2 D1 D0 0 0 0 0 1 1 1 1	Programs 1 of 16 DTMF tone pairs that will be transmitted when TX DTMF and TX enable bit (CR0, bit D1) are set. Tone encoding is shown below:

KEYBOARD EQUIVALENT	DTMF CODE D3 D2 D1 D0	TONES LOW HIGH
1	0 0 0 1	697 1209
2	0 0 1 0	697 1336
3	0 0 1 1	697 1477
4	0 1 0 0	770 1209
5	0 1 0 1	770 1336
6	0 1 1 0	770 1477
7	0 1 1 1	852 1209
8	1 0 0 0	852 1336
9	1 0 0 1	852 1477
0	1 0 1 0	941 1336
*	1 0 1 1	941 1209
#	1 1 0 0	941 1477
A	1 1 0 1	697 1633
B	1 1 1 0	770 1633
C	1 1 1 1	852 1633
D	0 0 0 0	941 1633

TONE REGISTER (continued)

	D7	D6	D5	D4	D3	D2	D1	D0
TR 011	RXD OUTPUT CONTR.	0	TRANSMIT ANSWER TONE	TRANSMIT DTMF	DTMF 3	DTMF 2	DTMF 1	DTMF 0

BIT NO.	NAME	CONDITION	DESCRIPTION
D4	TRANSMIT DTMF	0	Disable DTMF.
		1	Activates DTMF. The selected DTMF tones are transmitted continuously when this bit is high (with Transmit Enable, CR0-D1). TX DTMF overrides all other transmit functions.
D5	TRANSMIT ANSWER TONE	0	Disables answer tone generator.
		1	Enables answer tone generator. A 2225 Hz answer tone will be transmitted continuously when the Transmit Enable bit is set in CR0. The device must be in answer mode.
D7	RXD OUTPUT CONTROL	0	Enables RXD pin. Receive data will be output on RXD.
		1	Disables RXD pin. The RXD pin reverts to a high impedance with internal, weak pull-up resistor.

ID REGISTER

	D7	D6	D5	D4	D3	D2	D1	D0
ID 110	ID	ID	ID	ID	X	X	X	X

BIT NO.	NAME	CONDITION	DESCRIPTION
D7, D6, D5 D4	Device Identification Signature	D7 D6 D5 D4	Indicates Device:
		0 0 X X	SSI 73K212AL, 73K321L or 73K322L or 73K321L
		0 1 X X	SSI 73K221L or 73K302L
		1 0 X X	SSI 73K222AL
		1 1 0 0	SSI 73K224L
		1 1 1 0	SSI 73K324L
		1 1 0 1	SSI 73K312L
D3-D0	Undefined	Undefined	Mask in software

ELECTRICAL SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING
VDD Supply Voltage	7V
Storage Temperature	-65 to 150°C
Soldering Temperature (10 sec.)	260°C
Applied Voltage	-0.3 to VDD + 0.3V
Note: All inputs and outputs are protected from static charge using built-in, industry standard protection devices and all outputs are short-circuit protected.	

RECOMMENDED OPERATING CONDITIONS

PARAMETER	CONDITION	MIN	NOM	MAX	UNIT
VDD Supply Voltage		4.5	5	5.5	V
TA, Operating Free-Air Temperature		-40		+85	°C
Clock Variation	(11.0592 MHz) Crystal or external clock	-0.01		+0.01	%
External Components (Refer to Application section for placement.)					
VREF Bypass capacitor	(External to GND)	0.1			µF
Bias setting resistor	(Placed between VDD and ISET pins)	1.8	2	2.2	MΩ
ISET Bypass capacitor	(ISET pin to GND)	0.1			µF
VDD Bypass capacitor 1	(External to GND)	0.1			µF
VDD Bypass capacitor 2	(External to GND)	22			µF
XTL1 Load capacitor	Depends on crystal characteristics;			40	pF
XTL2 Load capacitor	from pin to GND			20	

DC ELECTRICAL CHARACTERISTICS

(TA = -40°C to 85°C, VDD = recommended range unless otherwise noted.)

PARAMETER	CONDITION	MIN	NOM	MAX	UNIT
IDD, Supply Current	ISET Resistor = 2 MΩ				
IDDA, Active	CLK = 11.0592 MHz		8	12	mA
IDD1, Power-down	CLK = 11.0592 MHz			4	mA
IDD2, Power-down	CLK = 19.200 kHz			3	mA
Digital Inputs					
VIH, Input High Voltage					
Reset, XTL1, XTL2		3.0		VDD	V
All other inputs		2.0		VDD	V
VIL, Input Low Voltage		0		0.8	V
IIH, Input High Current	VI = VIH Max			100	µA
IIL, Input Low Current	VI = VIL Min	-200			µA
Reset Pull-down Current	Reset = VDD	1		50	µA
Input Capacitance	All Digital Input Pins			10	pF
Digital Outputs					
VOH, Output High Voltage	IOH MIN = -0.4 mA	2.4		VDD	V
VOL, Output Low Voltage	IO MAX = 1.6 mA			0.4	V
VOL, CLK Output	IO = 3.6 mA			0.6	V
RXD Tri-State Pull-up Curr.	RXD = GND	-1		-50	µA
CMAX, CLK Output	Maximum Capacitive Load			15	pF

ELECTRICAL SPECIFICATIONS (continued)

DYNAMIC CHARACTERISTICS AND TIMING

(TA = -40°C to + 85°C, VDD = recommended range unless otherwise noted.)

PARAMETER	CONDITION	MIN	NOM	MAX	UNIT
PSK Modulator					
Carrier Suppression	Measured at TXA	55			dB
Output Amplitude	TX scrambled marks	-11	-10.0	-9	dBm0
FSK Mod/Demod					
Output Freq. Error	CLK = 11.0592 MHz	-0.35		+0.35	%
Transmit Level	Transmit Dotting Pattern	-11	-10.0	-9	dBm0
Harmonic Distortion in 700-2900 Hz band	THD in the alternate band DPSK or FSK		-60	-50	dB
Output Bias Distortion	Transmit Dotting Pattern In ALB @ RXD		±8		%
Total Output Jitter	Random Input in ALB @ RXD	-15		+15	%
DTMF Generator					
Freq. Accuracy		-0.25		+0.25	%
Output Amplitude	Low-Band, DPSK Mode	-10	-9	-8	dBm0
Output Amplitude	High-Band, DPSK Mode	-8	-7	-6	dBm0
Twist	High-Band to Low-Band, DPSK mode	1.0	2.0	3.0	dB
Long Loop Detect	DPSK or FSK	-38		-28	dBm0
Dynamic Range	Refer to Performance Curves		45		dB
Call Progress Detector					
Detect Level	2-Tones in 350-600 Hz band	-34		0	dBm0
Reject Level	2-Tones in 350-600 Hz band			-41	dBm0
Delay Time	-70 dBm0 to -30 dBm0 STEP	27		80	ms
Hold Time	-30 dBm0 to -70 dBm0 STEP	27		80	ms
Hysteresis		2			dB

Note: Parameters expressed in dBm0 refer to the following definition:

0 dB loss in the Transmit path to the line.
2 dB gain in the Receive path from the line.

Refer to the Basic Box Modem diagram in the Applications section for the DAA design.

DYNAMIC CHARACTERISTICS AND TIMING (continued)

PARAMETER	CONDITION	MIN	NOM	MAX	UNIT
Carrier Detect					
Threshold	DPSK or FSK receive data	-49		-42	dBm0
Delay Time	-70 dBm0 to -30 dBm0 STEP	15		45	ms
Hysteresis	Single tone detected	2	3		dB
Hold Time	-30 dBm0 to -70 dBm0 STEP	10		24	ms
Answer Tone Detector					
Detect Level	In FSK mode	-49		-42	dBm0
Delay Time	-70 dBm0 to -30 dBm0 STEP	20		45	ms
Hold Time	-30 dBm0 to -70 dBm0 STEP	10		30	ms
Detect Freq. Range		-2.5		+2.5	%
Output Smoothing Filter					
TXA pin Output Impedance			200	300	Ω
Output load	TXA pin; FSK Single Tone out for THD = -50 db in 0.3 to 3.4 kHz	10		 50	kΩ pF
Spurious Freq. Comp.	Frequency = 76.8 kHz			-39	dBm0
	Frequency = 153.6 kHz			-45	dBm0
Clock Noise	TXA pin; 76.8 kHz			1.0	mVms
Carrier VCO					
Capture Range	Originate or Answer	-10		+10	Hz
Capture Time	-10 Hz to +10 Hz Carrier Freq. Change Assum.		40	100	ms
Recovered Clock					
Capture Range	% of frequency center frequency (center at 1200 Hz)	-625		+625	ppm
Data Delay Time	Analog data in at RXA pin to receive data valid at RXD pin		30	50	ms

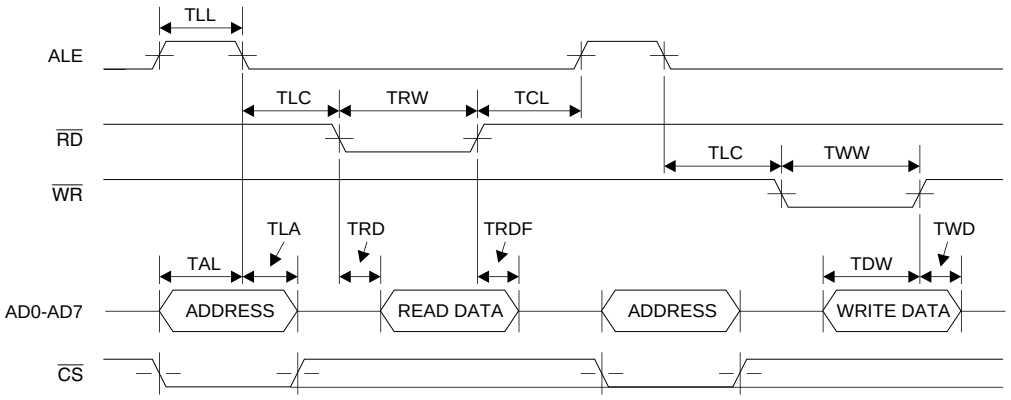
DYNAMIC CHARACTERISTICS AND TIMING (Continued)

PARAMETER	CONDITION	MIN	NOM	MAX	UNIT
Timing (Refer to Timing Diagrams)					
TAL	$\overline{CS}$/Addr. setup before ALE low	30			ns
TLA	$\overline{CS}$/Addr. hold after ALE low	20			ns
TLC	ALE low to $\overline{RD}$/$\overline{WR}$ low	40			ns
TCL	$\overline{RD}$/$\overline{WR}$ Control to ALE high	10			ns
TRD	Data out from $\overline{RD}$ low	0		160	ns
TLL	ALE width	60			ns
TRDF	Data float after $\overline{RD}$ high	0		80	ns
TRW	$\overline{RD}$ width	200		25000	ns
TWW	$\overline{WR}$ width	140		25000*	ns
TDW	Data setup before $\overline{WR}$ high	150			ns
TWD	Data hold after $\overline{WR}$ high	20			ns
TCKD	Data out after EXCLK low			200	ns
TCKW	$\overline{WR}$ after EXCLK low	150			ns
TDCK	Data setup before EXCLK low	150			ns
TAC	Address setup before control**	50			ns
TCA	Address hold after control**	50			ns
TWH	Data Hold after EXCLK	20			ns
* Maximum time applies to parallel version only.					
** Control for setup is the falling edge of $\overline{RD}$ or $\overline{WR}$. Control for hold is the falling edge of $\overline{RD}$ or the rising edge of $\overline{WR}$.					

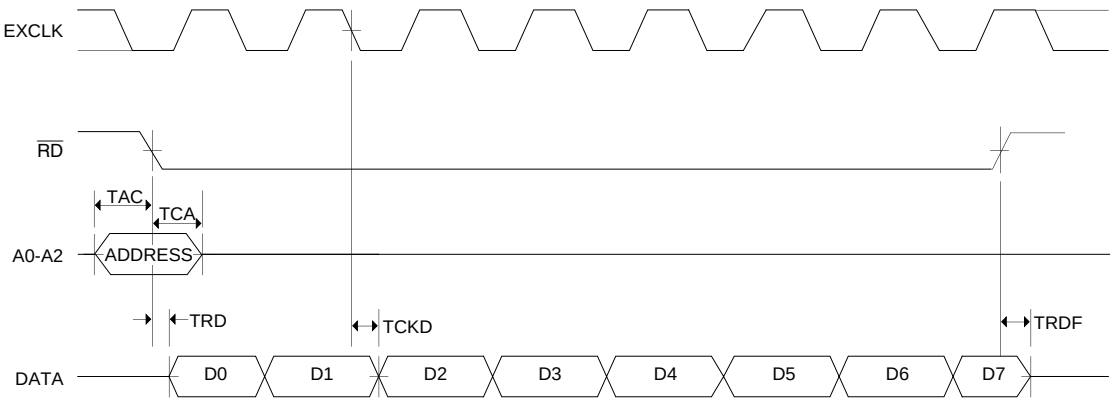
NOTE: Asserting ALE, $\overline{CS}$, and $\overline{RD}$ or $\overline{WR}$ concurrently can cause unintentional register accesses. When using non-8031 compatible processors, care must be taken to prevent this from occurring when designing the interface logic.

TIMING DIAGRAMS

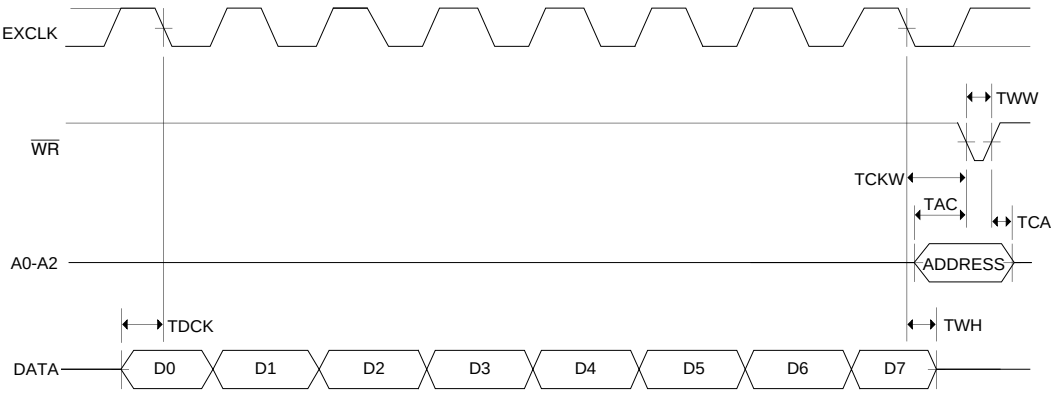
BUS TIMING DIAGRAM (PARALLEL VERSION)



READ TIMING DIAGRAM (SERIAL VERSION)



WRITE TIMING DIAGRAM (SERIAL VERSION)



APPLICATIONS INFORMATION

GENERAL CONSIDERATIONS

Figures 1 and 2 show basic circuit diagrams for K-Series modem integrated circuits. K-Series products are designed to be used in conjunction with a control processor, a UART or RS-232 serial data interface, and a DAA phone line interface to function as a typical intelligent modem. The K-Series ICs interface directly with Intel 8048 and 80C51 microprocessors for control and status monitoring purposes.Two typical DAA arrangements are shown: one for a split ±5 or ±12 volt design and one for a single 5 volt design. These diagrams are for reference only and do not represent production-ready modem designs.

K-Series devices are available with two control interface versions: one for a parallel multiplexed address/data interface, and one for a serial interface. The parallel version is intended for use with 8039/48 or 8031/51 microcontrollers from Intel or many other manufacturers. The serial interface 22-pin version can be used with other microcontrollers or in applications where only a limited number of port lines are available or the application does not lend itself to a multiplexed address/data interface. The parallel versions may also be used in the serial mode, as explained in the data sheet pin description.

In most applications the controller will monitor the serial data for commands from the DTE and the received data for break signals from the far end modem. In this way, commands to the modem are sent over the same line as the transmitted data. In other applications the RS-232 interface handshake lines are used for modem control.

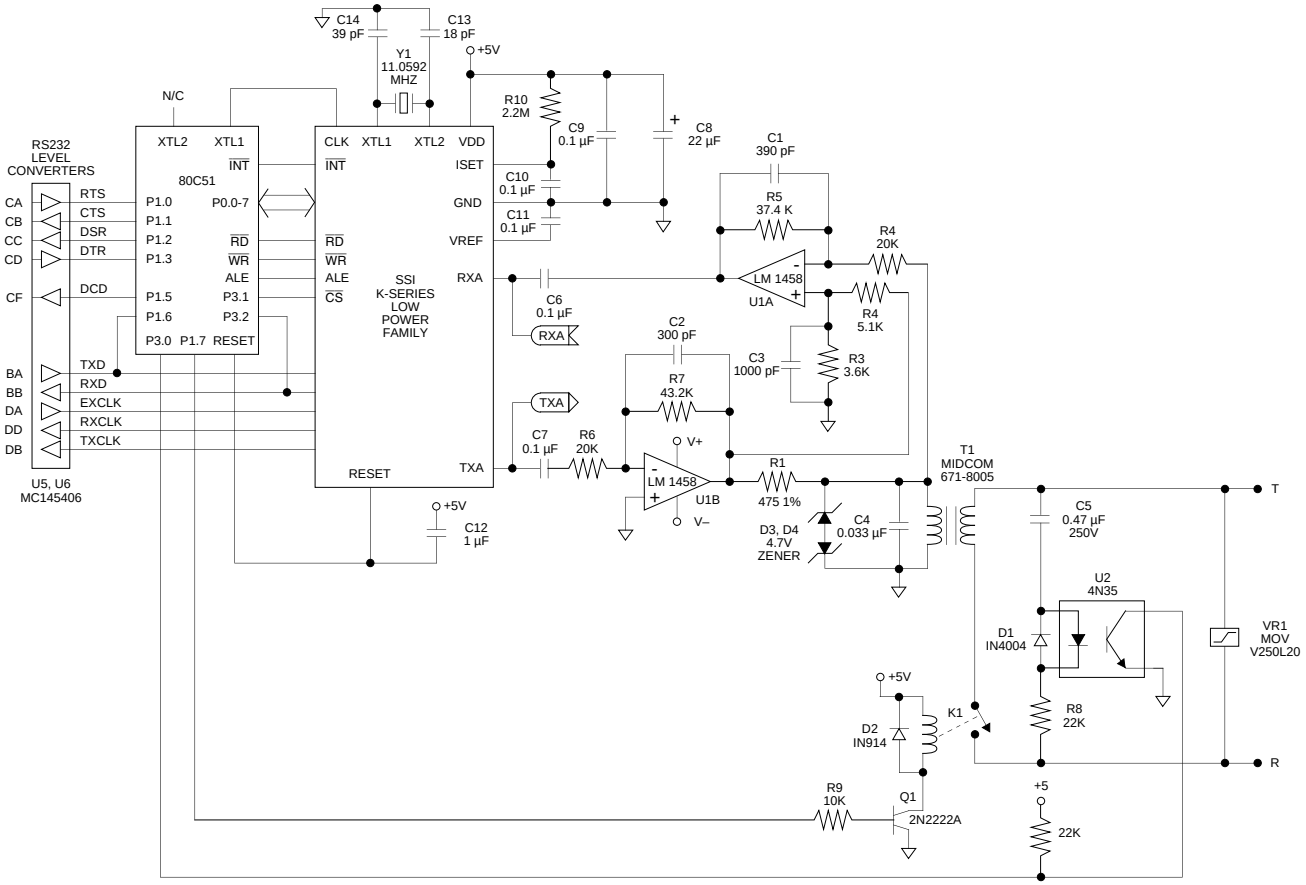


FIGURE 1: Basic Box Modem with Dual-Supply Hybrid

DIRECT ACCESS ARRANGEMENT (DAA)

The telephone line interfaces show two examples of how the "hybrid" may be implemented. The split supply design (Figure 1) is a typical two op-amp hybrid. The receive op-amp serves two purposes. It supplies gain to amplify the receive signal to the proper level for the modem's detectors and demodulator, and it removes the transmitted signal from the receive signal present at the transformer. This is done by supplying a portion of the transmitted signal to the non-inverting input of the receive op-amp at the same amplitude as the signal appearing at the transformer, making the transmit signal common mode.

The single-supply hybrid is more complex than the dual-supply version described above, but its use eliminates the need for a second power supply. This circuit (Figure 2) uses a bridged drive to allow undistorted signals to be sent with a single 5V supply. Because DTMF tones utilize a higher amplitude than data, these signals will clip if a single-ended drive approach is used. The bridged driver uses an extra op-amp (U1A) to invert the signal coming from the gain setting op-amp (U1B) before sending it to the other leg of the transformer. Each op-amp then supplies half the drive signal to the transformer. The receive amplifier (U1C) picks off its signal at the junction of the impedance matching resistor and the transformer. Because the bottom leg of the transformer is being driven in one direction by U1A and the resistor is driven in the opposite direction at the same time by U1B, the junction of the transformer and resistor remains relatively constant and the receive signal is unaffected.

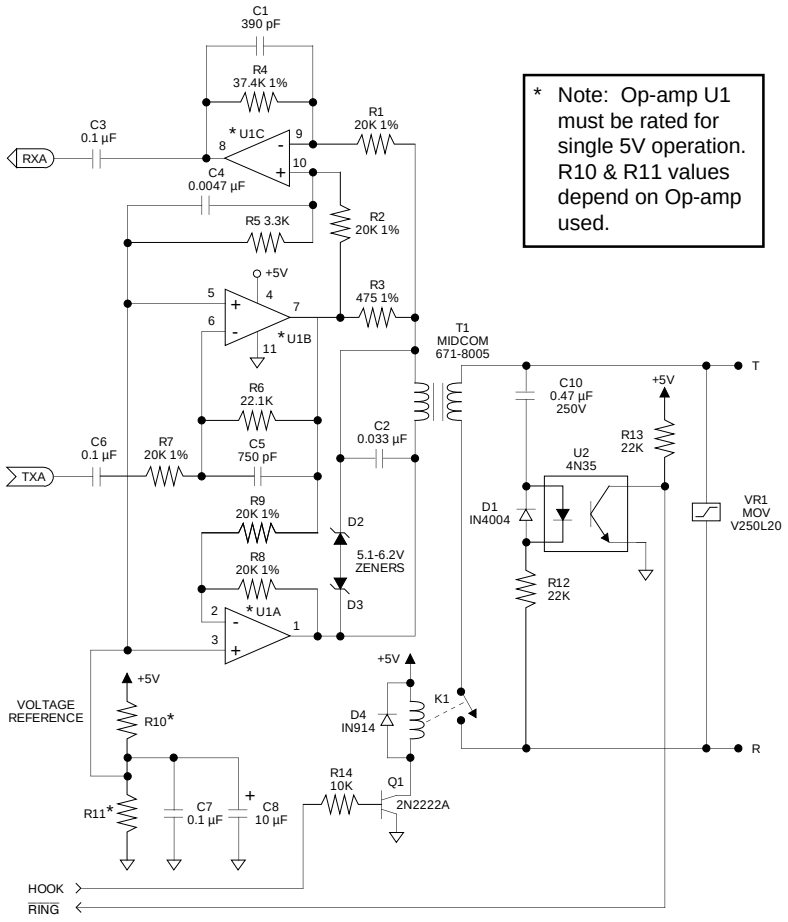


FIGURE 2: Single 5V Hybrid Version

DESIGN CONSIDERATIONS

Silicon Systems 1-chip modem products include all basic modem functions. This makes these devices adaptable for use in a variety of applications, and as easy to control as conventional digital bus peripherals.

Unlike digital logic circuitry, however, modem designs must properly contend with precise frequency tolerances and very low level analog signals, to ensure acceptable performance. Using good analog circuit design practices will generally result in a sound design. Following are additional recommendations which should be taken into consideration when starting new designs.

CRYSTAL OSCILLATOR

The K-Series crystal oscillator requires a parallel mode (antiresonant) crystal which operates at 11.0592 MHz. It is important that this frequency be maintained to within ±0.01% accuracy.

In order for a parallel mode crystal to operate correctly and to specification, it must have a load capacitor connected to the junction of each of the crystal and internal inverter connections, terminated to ground. The values of these capacitors depend primarily on the crystal's characteristics, and to a lesser degree on the internal inverter circuit. The values used affect the accuracy and start up characteristics of the oscillator.

LAYOUT CONSIDERATIONS

Good analog/digital design rules must be used to control system noise in order to obtain highest performance in modem designs. The more digital circuitry present on the PC board, the more this attention to noise control is needed. The modem should be treated as a high impedance analog device. A 22 µF electrolytic capacitor in parallel with a 0.1 µF ceramic capacitor between VDD and GND is recommended. Liberal use of ground planes and larger traces on power and ground are also highly favored. High speed digital circuits tend to generate a significant amount of EMI (Electro-Magnetic Interference) which must be minimized in order to meet regulatory agency limitations. To accomplish this, high speed digital devices should be locally bypassed, and the telephone line interface and K-Series device should be located close to each other near the area of the board where the phone line connection is accessed. To avoid problems, power supply and ground traces should be routed separately to the analog and digital functions on the board, and digital signals should not be routed near low level or high impedance analog traces. The analog and digital grounds should only connect at one point near the K-Series device ground pin to avoid ground loops. The K-Series modem IC's should have both high frequency and low frequency bypassing as close to the package as possible.

MODEM PERFORMANCE CHARACTERISTICS

The curves presented here define modem IC performance under a variety of line conditions while inducing disturbances that are typical of those encountered during data transmission on public service telephone lines. Test data was taken using an AEA Electronics' "Autotest I" modem test set and line simulator, operating under computer control. All tests were run full-duplex, using a Concord Data Systems 224 as the reference modem. A 511 pseudo-random-bit pattern was used for each data point. Noise was C-message weighted and all signal-to-noise (S/N) ratios reflect total power measurements similar to the CCITT V.56 measurement specification. The individual tests are defined as follows.

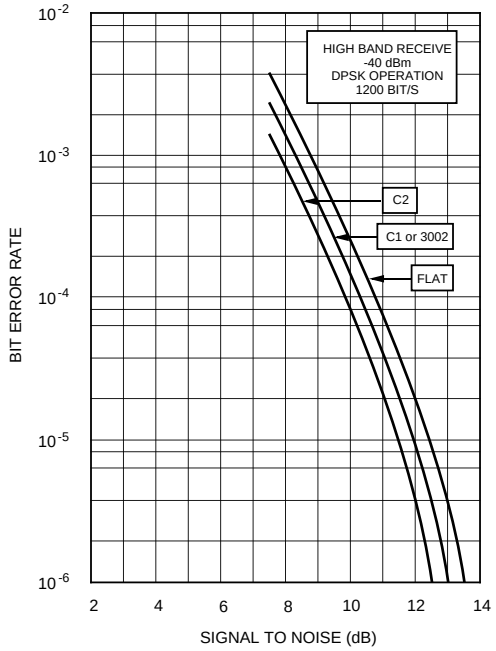
BER vs. S/N

This test measures the ability of the modem to operate over noisy lines with a minimum of data-transfer errors. Since some noise is generated in the best of dial-up lines, the modem must operate with the lowest S/N ratio possible. Better modem performance is indicated by test curves that are closest to the BER axis. A narrow spread between curves representing the four line parameters indicates minimal variation in performance while operating over a range of aberrant operating conditions. Typically, a DPSK modem will exhibit better BER-performance test curves receiving in the low band than in the high band.

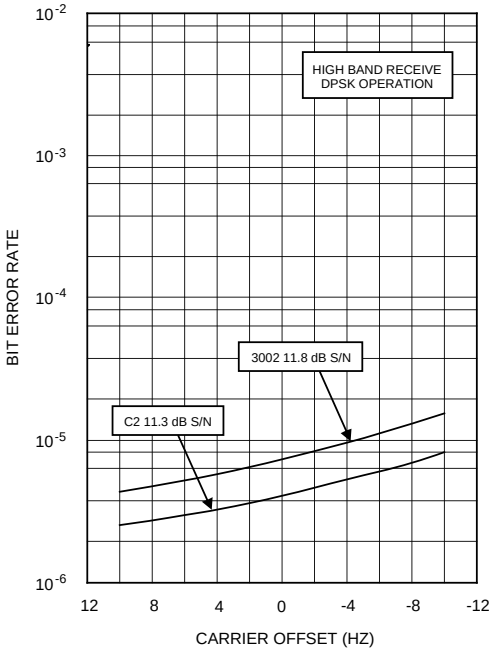
BER vs. Receive Level

This test measures the dynamic range of the modem. Because signal levels vary widely over dial-up lines, the widest possible dynamic range is desirable. The minimum Bell specification calls for 36 dB of dynamic range. S/N ratios are held constant at the indicated values while the receive level is lowered from a very high to very low signal levels. The width of the "bowl" of these curves, taken at the BER point, is the measure of dynamic range.

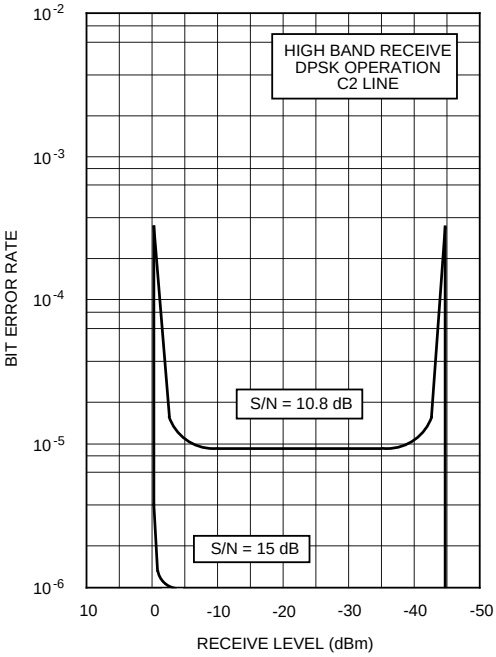
SSI 73K212AL
BER vs SIGNAL TO NOISE



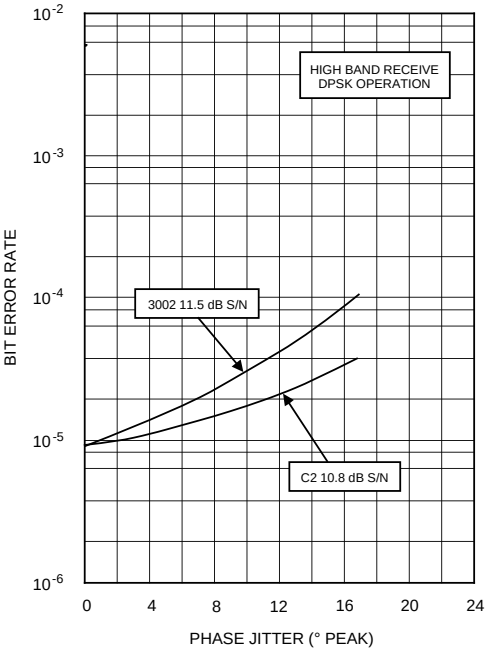
SSI 73K212AL
BER vs CARRIER OFFSET



***SSI 73K212AL**
BER vs RECEIVE LEVEL



***SSI 73K212AL**
BER vs PHASE JITTER



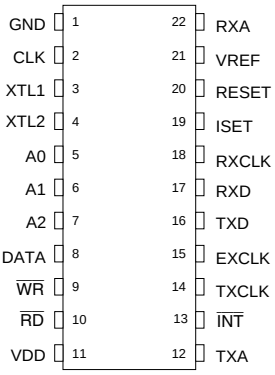
***** = "EQ On" indicates bit CR1 D4 is set for additional phase equalization.

SSI 73K212AL
Bell 212A/103
Single-Chip Modem

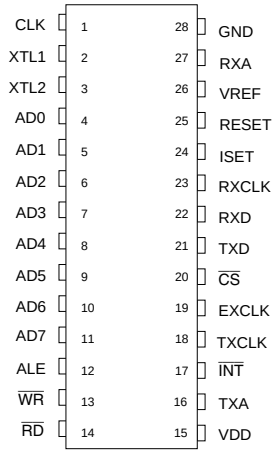
PACKAGE PIN DESIGNATIONS

(Top View)

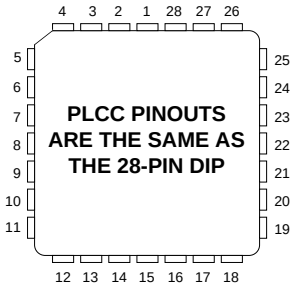
CAUTION: Use handling procedures necessary for a static sensitive component.



400-Mil 22-Pin DIP



600-Mil 28-Pin DIP



28-Pin PLCC

ORDERING INFORMATION

PART DESCRIPTION	ORDER NO.	PKG. MARK
SSI 73K212AL 28-pin	73K212AL – IP	73K212AL – IP
Plastic Dual In-Line	or 73K212AL – IP	or 73K212AL – IP
	73K212AL – IH	73K212AL – IH
Plastic Leaded Chip Carrier	or 73K212L – IH	73K212AL – IH
SSI 73K212AL 22-pin	73K212ASL – IP	73K212ASL – IP
Plastic Dual In-Line	or 73K212SL – IP	73K212SL – IP

Silicon Systems, Inc., 14351 Myford Road, Tustin, CA 92680-7022, (714) 573-6000, FAX: (714) 573-6914

SSI 73K221AL
CCITT V.22, V.21
Single-Chip Modem

February 1996

DESCRIPTION

The SSI 73K221AL is a highly integrated single-chip modem IC which provides the functions needed to construct a CCITT V.22 and V.21 compatible modem, capable of 1200 or 0-300 bit/s full-duplex operation over dial-up lines. The SSI 73K221AL is an enhancement of the SSI 73K212L single-chip modem with performance characteristics suitable for European and Asian telephone systems. The SSI 73K221AL produces either 550 or 1800 Hz guard tone, recognizes and generates a 2100 Hz answer tone, and allows V.21 for 300 Hz FSK operation. The SSI 73K221AL integrates analog, digital, and switched-capacitor array functions on a single substrate, offering excellent performance and a high level of functional integration in a single 28-pin DIP or PLCC or 22-pin DIP configuration. The SSI 73K221AL, operates from a single +5 volt supply. The 73221AL replaces the 73K221L in all applications and should be specified for all new designs.

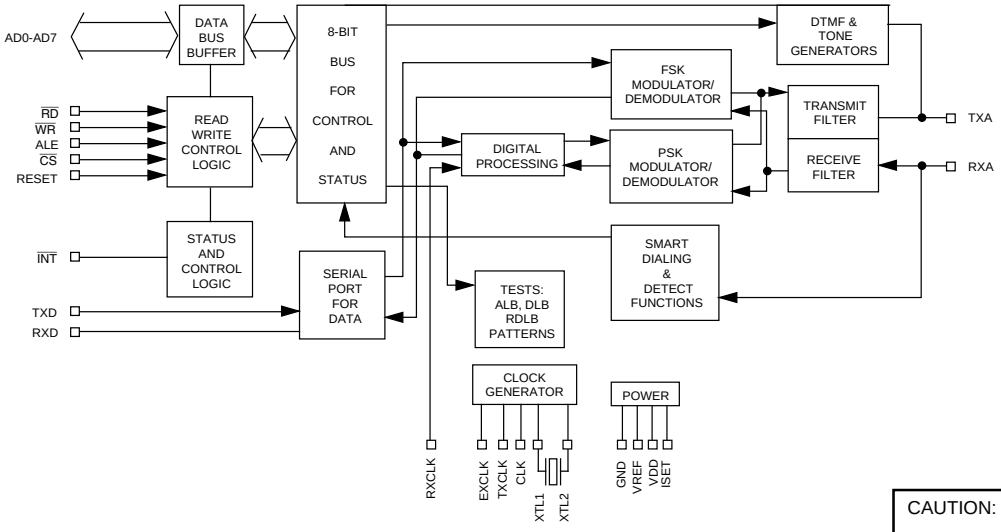
The SSI 73K221AL includes the DPSK and FSK modulator/demodulator functions, call progress and handshake tone monitor test modes, and a tone generator capable of producing DTMF, answer and 550 or 1800 Hz guard tone. This device supports V.22 (Except mode v) and V. 21 modes of operation,

(continued)

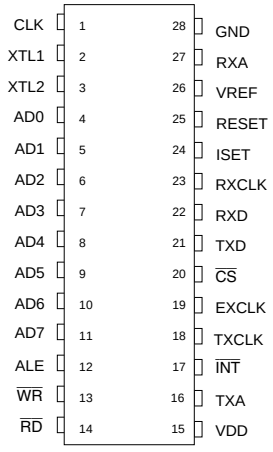
FEATURES

- **One-chip CCITT V.22 and V.21 standard compatible modem data pump**
- **Full-duplex Operation at 0-300 bit/s (FSK) or 600 and 1200 bit/s (DPSK)**
- **Pin and software compatible with other SSI K-Series 1-chip modems**
- **Interfaces directly with standard microprocessors (8048, 80C51 typical)**
- **Serial (22-pin DIP) or parallel (28-pin DIP or PLCC) microprocessor bus for control**
- **Serial port for data transfer**
- **Both Synchronous and Asynchronous modes of operation**
- **Call progress, carrier, precise answer tone (2100 Hz), and long loop detectors**
- **DTMF, and 550 or 1800 Hz guard tone generators**
- **Test modes available: ALB, DL, RDL, Mark, Space, Alternating bit patterns**
- **Precise automatic gain control allows 45 dB dynamic range**
- **Space efficient 22- or 28-pin DIP or 28-Pin PLCC packages**
- **CMOS technology for low power consumption using 30 mW @ 5V**
- **Single +5 volt supply**

BLOCK DIAGRAM



PIN DIAGRAM



CAUTION: Use handling procedures necessary for a static sensitive component.

DESCRIPTION (continued)

allowing both synchronous and asynchronous communications. The SSI 73K221AL is designed to appear to the systems designer as a microprocessor peripheral, and will easily interface with popular one-chip microprocessors (80C51 typical) for control of modem functions through its 8-bit multiplexed address/data bus or alternatively via the serial control bus. An ALE control line simplifies address demultiplexing. Data communications occurs through a separate serial port only.

The SSI 73K221AL is ideal for use in either free standing or integral system modem products where full-duplex 1200 bit/s data communications over the 2-wire switched telephone network is desired. Its high functionality, low power consumption and efficient packaging simplify design requirements and increase system reliability. A complete modem requires only the addition of the phone line interface, a control microprocessor, and RS-232 level converter for a typical system. The SSI 73K221AL is part of Silicon Systems' K-Series family of pin and function compatible single-chip modem products. These devices allow systems to be configured for higher speeds and Bell or CCITT operation with only a single component change.

OPERATION

ASYNCHRONOUS MODE

Data transmission for the DPSK mode requires that data ultimately be transmitted in a synchronous fashion, The SSI 73K221AL includes ASYNC/SYNC and SYNC/ASYNC converters which delete or insert stop bits in order to transmit data at a regular rate. In Asynchronous mode the serial data comes from the TXD pin into the ASYNC/SYNC rate converter. The ASYNC/SYNC rate converter accepts the data provided on the TXD pin which normally must be 1200 or 600 bit/s +1.0%, -2.5%. The rate converter will then insert or delete stop bits in order to output a signal which is 1200 or 600 bit/s $\pm$ 0.01%.

The serial data stream from the ASYNC/SYNC converter is passed through the data scrambler and onto the analog modulator. The data scrambler can be bypassed under processor control when unscrambled data must be transmitted. The ASYNC/SYNC rate converter and the data scrambler are bypassed in all FSK modes. If serial input data contains a break signal through one character (including start and stop bits) the break will be extended to at least $2 \bullet N + 3$ bits long (where N is the number of transmitted bits/character).

Serial data from the demodulator is passed first through the data descrambler and then through the SYNC/ASYNC rate converter. The SYNC/ASYNC convertor will reinsert any deleted stop bits and transmit output data at an intra-character rate (bit-to-bit timing) of no greater than 1219 bit/s. An incoming break signal (low through two characters) will be passed through without incorrectly inserting a stop bit.

The SYNC/ASYNC converter also has an extended Overspeed mode which allows selection of an output range of either +1% or +2.3%. In the extended Overspeed mode, stop bits are output at 7/8 the normal width.

SYNCHRONOUS MODE

The CCITT V.22 standard defines synchronous operation at 600 and 1200 bit/s. The Bell 212A standard defines synchronous operation only at 1200 bit/s. Operation is similar to that of the Asynchronous mode except that data must be synchronized to a provided clock and no variation in data transfer rate is allowable. Serial input data appearing at TXD must be valid on the rising edge of TXCLK.

TXCLK is an internally derived signal in Internal mode and is connected internally to the RXCLK pin in Slave mode. Receive data at the RXD pin is clocked out on the falling edge of RXCLK. The ASYNC/SYNC converter is bypassed when Synchronous mode is selected and data is transmitted at the same rate as it is input.

DPSK MODULATOR/DEMODULATOR

The SSI 73K221AL modulates a serial bit stream into dibit pairs that are represented by four possible phase shifts as prescribed by the V.22 standard. The baseband signal is then filtered to reduce intersymbol interference on the bandlimited 2-wire telephone line. Transmission occurs on either a 1200 Hz (Originate mode) or 2400 Hz carrier (Answer mode). Demodulation is the reverse of the modulation process, with the incoming analog signal eventually decoded into di-bits and converted back to a serial bit stream. The demodulator also recovers the clock which was encoded into the analog signal during modulation. Demodulation

occurs using either a 1200 Hz carrier (Answer mode or ALB Originate mode) or a 2400 Hz carrier (Originate mode or ALB Answer mode). The SSI 73K221AL uses a phase locked loop coherent demodulation technique for optimum performance.

FSK MODULATOR/DEMODULATOR

The FSK modulator produces a frequency modulated analog output signal using two discrete frequencies to represent the binary data. V.21 mode uses 980 and 1180 Hz (originate, mark and space) or 1650 and 1850 Hz (answer, mark and space). Demodulation involves detecting the received frequencies and decoding them into the appropriate binary value. The rate converter and scrambler/descrambler are bypassed in the V.21 mode.

PASSBAND FILTERS AND EQUALIZERS

High and low band filters are included to shape the amplitude and phase response of the transmit and receive signals and provide compromise delay equalization and rejection of out-of-band signals in the receive channel. Amplitude and phase equalization are necessary to compensate for distortion of the transmission line and to reduce intersymbol interference in the bandlimited receive signal. The transmit signal filtering approximates a 75% square root of raised Cosine frequency response characteristic.

AGC

The automatic gain control maintains a signal level at the input to the demodulators which is constant to within 1 dB. It corrects quickly for increases in signal which would cause clipping and provides a total dynamic range of >45 dB.

PARALLEL BUS INTERFACE

Four 8-bit registers are provided for control, optionselect and status monitoring. These registers are addressed with the AD0, AD1, and AD2 multiplexed address lines (latched by ALE) and appear to a control microprocessor as four consecutive memory locations. Two control registers and the tone register are read/write memory. The detect register is read only and cannot be modified except by modem response to monitored parameters.

SERIAL COMMAND INTERFACE

The serial Command mode allows access to the SSI 73K221AL control and status registers via a serial command port (22-pin version only). In this mode the A0, A1 and A2 lines provide register addresses for data passed through the data pin under control of the $\overline{RD}$ and $\overline{WR}$ lines. A read operation is initiated when the $\overline{RD}$ line is taken low. The first bit is available after $\overline{RD}$ is brought low and the next seven cycles of EXCLK will then transfer out the remaining seven bits of the selected address LSB first. A write takes place by shifting in eight bits of data LSB first for eight consecutive cycles of EXCLK. $\overline{WR}$ is then pulsed low and data transferred into the addressed register on the rising edge of $\overline{WR}$.

SPECIAL DETECT CIRCUITRY

The special detect circuitry monitors the received analog signal to determine status or presence of carrier, call-progress tones, answer tone and weak received signal (long loop condition). An unscrambled mark signal is also detected when the received data out of the DPSK demodulator before the descrambler has been mark for 165.5 ms $\pm$ 6.5 ms minimum. The appropriate detect register bit is set when one of these conditions changes and an interrupt is generated for all conditions except long loop. The interrupts are disabled (masked) when the enable interrupt bit is set to 0.

DTMF GENERATOR

The DTMF generator will output one of 16 standard tone pairs determined by a 4-bit binary value and TX DTMF mode bit previously loaded into the tone register. Tone generation is initiated when the DTMF mode is selected using the tone register and the transmit enable (CR0 bit D1) is changed from 0 to 1.

PIN DESCRIPTION

POWER

NAME	28-PIN	22-PIN	TYPE	DESCRIPTION
GND	28	1	I	System Ground.
VDD	15	11	I	Power supply input, 5V ±10%. Bypass with 0.1 and 22 µF capacitors to ground.
VREF	26	21	O	An internally generated reference voltage. Bypass with 0.1 µF capacitor to GND.
ISET	24	19	I	Chip current reference. Sets bias current for op-amps. The chip current is set by connecting this pin to VDD through a 2 MΩ resistor. ISET should be bypassed to GND with a 0.1 µF capacitor.

PARALLEL MICROPROCESSOR INTERFACE

ALE	12	-	I	Address latch enable. The falling edge of ALE latches the address on AD0-AD2 and the chip select on $\overline{CS}$.
AD0-AD7	4-11	-	I/O	Address/data bus. These bidirectional tri-state multiplexed lines carry information to and from the internal control registers.
$\overline{CS}$	20	-	I	Chip select. A low on this pin during the falling edge of ALE allows a read cycle or a write cycle to occur. AD0-AD7 will not be driven and no registers will be written if $\overline{CS}$ (latched) is not active. The state $\overline{CS}$ is a latched on the falling edge of ALE.
CLK	1	2	O	Output clock. This pin is selectable under processor control to be either the crystal frequency (for use as a processor clock) or 16 x the data rate for use as a baud rate clock in DPSK modes only. The pin defaults to the crystal frequency on reset.
$\overline{INT}$	17	13	O	Interrupt. This open drain output signal is used to inform the processor that a detect flag has occurred. The processor must then read the detect register to determine which detect triggered the interrupt. $\overline{INT}$ will stay low until the processor reads the detect register or does a full reset.
$\overline{RD}$	14	-	I	Read. A low requests a read of the SSI 73K221AL internal registers. Data cannot be output unless both $\overline{RD}$ and the latched $\overline{CS}$ are active or low.
RESET	25	20	I	Reset. An active high signal on this pin will put the chip into an inactive state. All control register bits (CR0, CR1, Tone) will be reset. The output of the CLK pin will be set to the crystal frequency. An internal pull down permits power on reset using a capacitor to VDD.

PARALLEL MICROPROCESSOR INTERFACE (continued)

NAME	28-PIN	22-PIN	TYPE	DESCRIPTION
$\overline{WR}$	13	-	I	Write. A low on this pin informs the SSI 73K221AL that data is available on AD0-AD7 for writing into an internal register. Data is latched on the rising edge of $\overline{WR}$. No data is written unless both $\overline{WR}$ and the latched $\overline{CS}$ are low.

SERIAL MICROPROCESSOR INTERFACE

A0-A2	-	5-7	I	Register Address Selection. These lines carry register addresses and should be valid during any read or write operation.
DATA	-	8	I/O	Serial Control Data. Data for a read/write operation is clocked in or out on the falling edge of the EXCLK pin. The direction of data flow is controlled by the $\overline{RD}$ pin. $\overline{RD}$ low outputs data. $\overline{RD}$ high inputs data.
$\overline{RD}$	-	10	I	Read. A low on this input informs the SSI 73K221AL that data or status information is being read by the processor. The falling edge of the $\overline{RD}$ signal will initiate a read from the addressed register. The $\overline{RD}$ signal must continue for eight falling edges of EXCLK in order to read all eight bits of the referenced register. Read data is provided LSB first. Data will not be output unless the $\overline{RD}$ signal is active.
$\overline{WR}$	-	9	I	Write. A low on this input informs the SSI 73K221AL that data or status information has been shifted in through the DATA pin and is available for writing to an internal register. The normal procedure for a write is to shift in data LSB first on the DATA pin for eight consecutive falling edges of EXCLK and then to pulse $\overline{WR}$ low. Data is written on the rising edge of $\overline{WR}$.

Note: In the serial, 22-pin version, the pins AD0-AD7, ALE and $\overline{CS}$ are removed and replaced with the pins; A0, A1, A2, DATA, and an unconnected pin. Also, the $\overline{RD}$ and $\overline{WR}$ controls are used differently.

The Serial Control mode is provided in the parallel control versions by tying ALE high and $\overline{CS}$ low. In this configuration AD7 becomes DATA and AD0, AD1 and AD2 become A0, A1 and A2, respectively.

PIN DESCRIPTION (continued)

DTE USER INTERFACE

NAME	28-PIN	22-PIN	TYPE	DESCRIPTION
EXCLK	19	15	I	External Clock. This signal is used in synchronous transmission when the external timing option has been selected. In the External Timing mode the rising edge of EXCLK is used to strobe synchronous DPSK transmit data applied to the TXD pin. Alternately used for serial control interface.
RXCLK	23	18	O	Receive Clock. The falling edge of this clock output is coincident with the transitions in the serial received data output. The rising edge of RXCLK can be used to latch the valid output data at RXD. RXCLK will be valid as long as a carrier is present in DPSK synchronous modes.
RXD	22	17	O	Received Digital Data Output. Serial receive data is available on this pin. The data is always valid on the rising edge of RXCLK when in Synchronous mode. RXD will output constant marks if no carrier is detected.
TXCLK	18	14	O	Transmit Clock. This signal is used in DPSK synchronous transmission to latch serial input data on the TXD pin. Data must be provided so that valid data is available on the rising edge of the TXCLK. The transmit clock is derived from different sources depending upon the Synchronization mode selection. In Internal Mode the clock is generated internally. In External Mode TXCLK is phase locked to the EXCLK pin. In Slave Mode TXCLK is phase locked to the RXCLK pin. TXCLK is always active.
TXD	21	16	I	Transmit Data Input. Serial data for transmission is applied to this pin. In Synchronous modes, the data must be valid on the rising edge of the TXCLK. In Asynchronous modes (1200/600 bit/s or 300 baud) no clocking is necessary. DPSK data must be 1200/600 bit/s +1%, -2.5% or +2.3%, -2.5 % in extended Overspeed mode.

ANALOG INTERFACE AND OSCILLATOR

RXA	27	22	I	Received modulated analog signal input from the telephone line interface.
TXA	16	12	O	Transmit analog output to the telephone line interface.
XTL1 XTL2	2 3	3 4	I I	These pins are for the internal crystal oscillator requiring an 11.0592 MHz Parallel mode crystal. Load capacitors should be connected from XTL1 and XTL2 to Ground. XTL2 can also be driven from an external clock.

REGISTER DESCRIPTIONS

Four 8-bit internal registers are accessible for control and status monitoring. The registers are accessed in read or write operations by addressing the A0 and A1 address lines in Serial mode, or the AD0 and AD1 lines in Parallel mode. In Parallel mode AD0 and AD1 lines are latched by ALE. Register CR0 controls the method by which data is transferred over the phone line. CR1 controls the interface between the microprocessor and the SSI 73K221AL internal state. DR is a detect register which provides an indication of monitored modem status conditions. TR, the tone control register, controls the DTMF generator, answer and guard tones and RXD output driver used in the modem initial connect sequence. All registers are read/write except for DR which is read only. Register control and status bits are identified below:

REGISTER BIT SUMMARY

		ADDRESS	DATA BIT NUMBER							
REGISTER		AD2 - AD0	D7	D6	D5	D4	D3	D2	D1	D0
CONTROL REGISTER 0	CR0	000	MODULATION OPTION	0	TRANSMIT MODE 3	TRANSMIT MODE 2	TRANSMIT MODE 1	TRANSMIT MODE 0	TRANSMIT ENABLE	ANSWER/ ORIGINATE
CONTROL REGISTER 1	CR1	001	TRANSMIT PATTERN 1	TRANSMIT PATTERN 0	ENABLE DETECT INTERRUPT	BYPASS SCRAMBLER	CLK CONTROL	RESET	TEST MODE 1	TEST MODE 0
DETECT REGISTER	DR	010	X	X	RECEIVE DATA	UNSCR. MARKS	CARRIER DETECT	ANSWER TONE	CALL PROGRESS	LONG LOOP
TONE CONTROL REGISTER	TR	011	RXD OUTPUT CONTROL	TRANSMIT GUARD TONE	TRANSMIT ANSWER TONE	TRANSMIT DTMF	DTMF3	DTMF2	DTMF1/ OVERSPEED	DTMF0/ GUARD/
CONTROL REGISTER 2	CR2	100	X	X	X	THESE REGISTER LOCATIONS ARE RESERVED FOR				X
CONTROL REGISTER 3	CR3	101	X	X	X	USE WITH OTHER K-SERIES FAMILY MEMBERS				X
ID REGISTER	ID	110	ID	ID	ID	ID	X	X	X	X

NOTE: When a register containing reserved control bits is written into, the reserved bits must be programmed as 0's.

X = Undefined, mask in software

REGISTER ADDRESS TABLE

REGISTER	ADDRESS AD2 - AD0	DATA BIT NUMBER D7	D6	D5	D4	D3	D2	D1	D0
CONTROL REGISTER 0 CR0	000	MODULATION OPTION	0	TRANSMIT MODE 3	TRANSMIT MODE 2	TRANSMIT MODE 1	TRANSMIT MODE 0	TRANSMIT ENABLE	ORIGINATE/ ANSWER
		0=1200 BIT/S DPSK 1=600 BIT/S DPSK		0000=PWR DOWN 0001=INT SYNCH 0010=EXT SYNCH 0011=SLAVE SYNCH 0100=ASYNCH 8 BITS/CHAR 0101=ASYNCH 9 BITS/CHAR 0110=ASYNCH 10 BITS/CHAR 0111=ASYNCH 11 BITS/CHAR 1100=FSK				0=DISABLE TXA OUTPUT 1=ENABLE TXA OUTPUT	0=ANSWER 1=ORIGINATE
CONTROL REGISTER 1 CR1	001	TRANSMIT PATTERN 1	TRANSMIT PATTERN 0	ENABLE DETECT INTERRUPT	BYPASS SCRAMBLER	CLK CONTROL	RESET	TEST MODE 1	TEST MODE 0
		00=TX DATA 01=TX ALTERNATE 10=TX MARK 11=TX SPACE		0=DISABLE 1=ENABLE	0=NORMAL 1=BYPASS SCRAMBLER	0=XTAL 1=16 X DATA RATE OUTPUT AT CLK PIN IN DPSK MODE ONLY	0=NORMAL 1=RESET	00=NORMAL 01=ANALOG LOOPBACK 10=REMOTE DIGITAL LOOPBACK 11=LOCAL DIGITAL LOOPBACK	
DETECT REGISTER DR	010	X	X	RECEIVE DATA	UNSCR. MARKS	CARRIER DETECT	ANSWER TONE	CALL PROGRESS	LONG LOOP
				OUTPUTS RECEIVED DATA STREAM	0=CONDITION NOT DETECTED 1=CONDITION DETECTED				
TONE CONTROL REGISTER TR	011	RXD OUTPUT CONTROL	TRANSMIT GUARD/ TONE	TRANSMIT ANSWER TONE	TRANSMIT DTMF	DTMF3	DTMF2	DTMF1/ OVERSPEED	DTMF0/ GUARD/ TONE
		RXD PIN 0=NORMAL 1=TRI STATE	0=OFF 1=ON	0=OFF 1=ON	0=DATA 1=TX DTMF	4 BIT CODE FOR 1 OF 16 DUAL TONE COMBINATIONS.			1800 Hz G.T. 550 Hz G.T.
ID REGISTER 10	110	ID	ID	ID	ID	X	X	X	X

00XX=73K212L/AL, 322L, 321L
01XX=73K221L/AL, 302L
10XX=73K222L/AL
1100=73K224L
1110=73K324L
1101=73K312L

X = Undefined, mask in software

CONTROL REGISTER 0

	D7	D6	D5	D4	D3	D2	D1	D0
CR0 000	MODUL. OPTION	0	TRANSMIT MODE 3	TRANSMIT MODE 2	TRANSMIT MODE 1	TRANSMIT MODE 0	TRANSMIT ENABLE	ANSWER/ ORIGINATE

BIT NO.	NAME	CONDITION	DESCRIPTION
D0	Answer/ Originate	0	Selects Answer mode (transmit in high band, receive in low band).
		1	Selects Originate mode (transmit in low band, receive in high band).
D1	Transmit Enable	0	Disables transmit output at TXA.
		1	Enables transmit output at TXA. Note: TX Enable must be set to 1 to allow Answer Tone and DTMF transmission.
D5, D4,D3, D2	Transmit Mode	D5 D4 D3 D2	
		0 0 0 0	Selects Power Down mode. All functions disabled except digital interface.
		0 0 0 1	Internal Synchronous mode. In this mode TXCLK is an internally derived 1200 Hz signal. Serial input data appearing at TXD must be valid on the rising edge of TXCLK. Receive data is clocked out of RXD on the falling edge of RXCLK.
		0 0 1 0	External Synchronous mode. Operation is identical to internal synchronous, but TXCLK is connected internally to EXCLK pin, and a 1200 Hz ±0.01% clock must be supplied externally.
		0 0 1 1	Slave Synchronous mode. Same operation as other Synchronous modes. TXCLK is connected internally to the RXCLK pin in this mode.
		0 1 0 0	Selects DPSK Asynchronous mode - 8 bits/character (1 start bit, 6 data bits, 1 stop bit).
		0 1 0 1	Selects DPSK Asynchronous mode - 9 bits/character (1 start bit, 7 data bits, 1 stop bit).
		0 1 1 0	Selects DPSK Asynchronous mode - 10 bits/character (1 start bit, 8 data bits, 1 stop bit).
		0 1 1 1	Selects DPSK Asynchronous mode - 11 bits/character (1 start bit, 8 data bits, Parity and 1 stop bit).
		1 1 0 0	Selects FSK operation.
D6		0	Not used; must be written as a “0.”

CONTROL REGISTER 0 (continued)

	D7	D6	D5	D4	D3	D2	D1	D0
CR0 000	MODUL. OPTION	0	TRANSMIT MODE 3	TRANSMIT MODE 2	TRANSMIT MODE 1	TRANSMIT MODE 0	TRANSMIT ENABLE	ANSWER/ ORIGINATE

BIT NO.	NAME	CONDITION	DESCRIPTION
D7	Modulation Option	D7 D5 D4	Selects:
		0 0 X	DPSK mode at 1200 bit/s.
		1 0 X	DPSK mode at 600 bit/s. X = Don't care

CONTROL REGISTER 1

	D7	D6	D5	D4	D3	D2	D1	D0
CR1 001	TRANSMIT PATTERN 1	TRANSMIT PATTERN 0	ENABLE DETECT INTER.	BYPASS SCRAMB	CLK CONTROL	RESET	TEST MODE 1	TEST MODE 0

BIT NO.	NAME	CONDITION	DESCRIPTION
D1, D0	Test Mode	D1 D0	
		0 0	Selects normal Operating mode.
		0 1	Analog Loopback mode. Loops the transmitted analog signal back to the receiver, and causes the receiver to use the same center frequency as the transmitter. To squelch the TXA pin, transmit enable must be forced low.
		1 0	Selects remote digital loopback. Received data is looped back to transmit data internally, and RXD is forced to a mark. Data on TXD is ignored.
		1 1	Selects local digital loopback. Internally loops TXD back to RXD and continues to transmit carrier from TXA pin.
D2	Reset	0	Selects normal operation.
		1	Resets modem to power down state. All control register bits (CR0, CR1, Tone) are reset to zero. The output of the CLK pin will be set to the crystal frequency.
D3	CLK Control (Clock Control)	0	Selects 11.0592 MHz crystal echo output at CLK pin.
		1	Selects 16 X the data rate, output at CLK pin in DPSK modes only.

CONTROL REGISTER 1 (continued)

	D7	D6	D5	D4	D3	D2	D1	D0
CR1 001	TRANSMIT PATTERN 1	TRANSMIT PATTERN 0	ENABLE DETECT INTER.	BYPASS SCRAMB	CLK CONTROL	RESET	TEST MODE 1	TEST MODE 0

BIT NO.	NAME	CONDITION	DESCRIPTION
D4	Bypass Scrambler	0	Selects normal operation. DPSK data is passed through scrambler.
D5	Enable Detect Interrupt	1	Selects Scrambler Bypass. Bypass DPSK data is routed around scrambler in the transmit path.
		0	Disables interrupt at $\overline{INT}$ pin.
		1	Enables $\overline{INT}$ output. An interrupts will be generated with a change in status of DR bits D1-D4. The answer tone and call progress detect interrupts are masked when the TX enable bit is set. Carrier detect is masked when TX DTMF is activated. All interrupts will be disabled if the device is in Power Down mode.
D7, D6	Transmit Pattern	D7 D6	
		0 0	Selects normal data transmission as determined by the state of the TXD pin.
		0 1	Selects an alternating mark/space transmit pattern for modem testing.
		1 0	Selects a constant mark transmit pattern.
		1 1	Selects a constant space transmit pattern.

DETECT REGISTER

	D7	D6	D5	D4	D3	D2	D1	D0
DR 010	X	X	RECEIVE DATA	UNSCR. MARK	CARR. DETECT	ANSWER TONE	CALL PROG.	LONG LOOP

BIT NO.	NAME	CONDITION	DESCRIPTION
D0	Long Loop	0	Indicates normal received signal.
		1	Indicates low received signal level.
D1	Call Progress Detect	0	No call progress tone detected.
		1	Indicates presence of call progress tones. The call progress detection circuitry is activated by energy in the 350 to 620 Hz call progress band.

DETECT REGISTER (continued)

	D7	D6	D5	D4	D3	D2	D1	D0
DR 010			RECEIVE DATA	UNSCR. MARK	CARR. DETECT	ANSWER TONE	CALL PROG.	LONG LOOP

BIT NO.	NAME	CONDITION	DESCRIPTION
D2	Answer Tone Detect	0	No answer tone detected.
		1	Indicates detection of 2100 Hz answer tone. The device must be in Originate mode for detection of answer tone.
D3	Carrier Detect	0	No carrier detected in the receive channel.
		1	Indicates carrier has been detected in the received channel.
D4	Unscrambled Mark	0	No unscrambled mark.
		1	Indicates detection of unscrambled marks in the received data. This may be used in the V.22 connect sequence or for requesting a remote modem to configure itself for remote digital loopback. A valid indication means that unscrambled marks have been received for > 165.5 ± 6.5 ms.
D5	Receive Data		Continuously outputs the received data stream. This data is the same as that output on the RXD pin, but it is not disabled when RXD is tri-stated.
D6, D7	Not Used	Undefined	Not used. Mask in software.

TONE REGISTER

	D7	D6	D5	D4	D3	D2	D1	D0
TR 011	RXD OUTPUT CONTR.	TRANSMIT GUARD TONE	TRANSMIT ANSWER TONE	TRANSMIT DTMF	DTMF 3	DTMF 2	DTMF 1/ OVER-SPEED	DTMF 0/ GUARD

BIT NO.	NAME	CONDITION	DESCRIPTION
D0	DTMF 0/ Guard Tone	D6 D4 D0	D0 interacts with bits D6, D5, and D4 as shown.
		X 1 X	Transmit DTMF tones.
		X 0 0	Transmits 1800 Hz guard tone.
		X 0 1	Transmits 550 Hz guard tone.
D1	DTMF 1/	D4 D1	D1 interacts with D4 as shown.
		0 0	Asynchronous DPSK 1200 or 600 bit/s +1.0% - 2.5%
		0 1	Asynchronous DPSK 1200 or 600 bit/s +2.3% -2.5%.

TONE REGISTER (continued)

	D7	D6	D5	D4	D3	D2	D1	D0
TR 011	RXD OUTPUT CONTR.	TRANSMIT GUARD TONE	TRANSMIT ANSWER TONE	TRANSMIT DTMF	DTMF 3	DTMF 2	DTMF 1/ OVER-SPEED	DTMF 0/ GUARD

BIT NO.	NAME	CONDITION	DESCRIPTION
D3, D2, D1, D0	DTMF 3, 2, 1, 0	D3 D2 D1 D0 0 0 0 0 - 1 1 1 1	Programs 1 of 16 DTMF tone pairs that will be transmitted when TX DTMF and TX enable bit (CR0, bit D1) is set. Tone encoding is shown below:
D4	Transmit DTMF	0	Disable DTMF.
		1	Activates DTMF. The selected DTMF tones are transmitted continuously when this bit is high. TX DTMF overrides all other transmit functions. Modem must be in DPSK mode during DTMF transmission.
D5	Transmit Answer Tone	0	Disables answer tone generator.
		1	Enables answer tone generator. A 2100 Hz answer tone will be transmitted continuously when the Transmit Enable bit is set in CR0. The device must be in Answer mode.

KEYBOARD EQUIVALENT	DTMF CODE D3	D2	D1	D0	TONES LOW	HIGH
1	0	0	0	1	697	1209
2	0	0	1	0	697	1336
3	0	0	1	1	697	1477
4	0	1	0	0	770	1209
5	0	1	0	1	770	1336
6	0	1	1	0	770	1477
7	0	1	1	1	852	1209
8	1	0	0	0	852	1336
9	1	0	0	1	852	1477
0	1	0	1	0	941	1336
*	1	0	1	1	941	1209
#	1	1	0	0	941	1477
A	1	1	0	1	697	1633
B	1	1	1	0	770	1633
C	1	1	1	1	852	1633
D	0	0	0	0	941	1633

TONE REGISTER (continued)

	D7	D6	D5	D4	D3	D2	D1	D0
TR 011	RXD OUTPUT CONTR.	TRANSMIT GUARD TONE	TRANSMIT ANSWER TONE	TRANSMIT DTMF	DTMF 3	DTMF 2	DTMF 1/ OVER-SPEED	DTMF 0/ GUARD

BIT NO.	NAME	CONDITION	DESCRIPTION
D6	TX Guard (Transmit Guard Tone)	0	Disables guard tone generator.
		1	Enables guard tone generator (See D0 for selection of guard tones).
D7	RXD Output Control	0	Enables RXD pin. Receive data will be output on RXD.
		1	Disables RXD pin. The RXD pin becomes a high impedance with internal weak pull-up resistor.

ID REGISTER

	D7	D6	D5	D4	D3	D2	D1	D0
ID 110	ID	ID	ID	ID	X	X	X	X

BIT NO.	NAME	CONDITION	DESCRIPTION
D7, D6, D5 D4	Device Identification Signature	D7 D6 D5 D4	Indicates Device:
		0 0 X X	SSI 73K212L/AL, 73K321L or 73K322L or 73K321L
		0 1 X X	SSI 73K221L/AL or 73K302L
		1 0 X X	SSI 73K222L/AL or 73K321L
		1 1 0 0	SSI 73K224L
		1 1 1 0	SSI 73K324L
		1 1 0 1	SSI 73K312L
D3-D0	Not Used	Undefined	Mask in software

ELECTRICAL SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT
VDD Supply Voltage	7	V
Storage Temperature	-65 to 150	°C
Soldering Temperature (10 sec.)	260	°C
Applied Voltage	-0.3 to VDD+0.3	V
Note: All inputs and outputs are protected from static charge using built-in, industry standard protection devices and all outputs are short-circuit protected.		

RECOMMENDED OPERATING CONDITIONS

PARAMETER	CONDITION	MIN	NOM	MAX	UNIT
VDD Supply voltage		4.5	5	5.5	V
TA, Operating Free-Air Temperature		-40		+85	°C
Clock Variation	(11.0592 MHz) Crystal or external clock	-0.01		+0.01	%
External Components (Refer to Application section for placement.)					
VREF Bypass Capacitor	(External to GND)	0.1			µF
Bias setting resistor	(Placed between VDD and ISET pins)	1.8	2	2.2	MΩ
ISET Bypass Capacitor	(ISET pin to GND)	0.1			µF
VDD Bypass Capacitor 1	(External to GND)	0.1			µF
VDD Bypass Capacitor 2	(External to GND)	22			µF
XTL1 Load Capacitor	Depends on crystal characteristics;			40	pF
XTL2 Load Capacitor	from pin to GND			20	

ELECTRICAL SPECIFICATIONS (continued)

DC ELECTRICAL CHARACTERISTICS

(TA = -40°C to 85°C, VDD = recommended range unless otherwise noted.)

PARAMETER	CONDITION	MIN	NOM	MAX	UNIT
IDD, Supply Current	ISET Resistor = 2 MΩ				
IDDA, Active	CLK = 11.0592 MHz		8	12	mA
IDD1, Power-down	CLK = 11.0592 MHz			4	mA
IDD2, Power-down	CLK = 19.200 KHz			3	mA
Digital Inputs					
VIH, Input High Voltage					
Reset, XTL1, XTL2		3.0		VDD	V
All other inputs		2.0		VDD	V
VIL, Input Low Voltage		0		0.8	V
IIH, Input High Current	VI = VIH Max			100	µA
IIL, Input Low Current	VI = VIL Min	-200			µA
Reset Pull-down Current	Reset = VDD	1		50	µA
Input Capacitance	All Digital Input Pins			10	pF
Digital Outputs					
VOH, Output High Voltage	IOH MIN = -0.4 mA	2.4		VDD	V
VOL, Output Low Voltage	IO MAX = 1.6 mA			0.4	V
VOL, CLK Output	IO = 3.6 mA			0.6	V
RXD Tri-State Pull-up Curr.	RXD = GND	-1		-50	µA
CMAX, CLK Output	Maximum Capacitive Load			15	pF

DYNAMIC CHARACTERISTICS AND TIMING
(TA = -40°C to +85°C, VDD = recommended range unless otherwise noted.)

PARAMETER	CONDITION	MIN	NOM	MAX	UNIT
PSK Modulator					
Carrier Suppression	Measured at TXA	55			dB
Output Amplitude	TX scrambled marks	-11	-10	-9	dBm0
FSK Mod/Demod					
Output Freq. Error	CLK = 11.0592 MHz	-0.35		+0.35	%
Transmit Level	Transmit Dotting Pattern	-11	-10	-9	dBm0
Harmonic Distortion in 700-2900 Hz band	THD in the alternate band DPSK or FSK		-60	-50	dB
Output Bias Distortion	Transmit Dotting Pattern In ALB @ RXD		±8		%
Total Output Jitter	Random Input in ALB @ RXD	-15		+15	%
DTMF Generator (Modem must be in DPSK mode to meet specifications)					
Freq. Accuracy		- 0.25		+0.25	%
Output Amplitude	Low Group, DPSK Mode	-10	-9	-8	dBm0
Output Amplitude	High Group, DPSK Mode	-8	-7	-6	dBm0
Twist	High-Group to Low-Group	1.0	2.0	3.0	dB
Long Loop Detect	DPSK or FSK	-38		-28	dBm0
Dynamic Range	Refer to Performance Curves		45		dB
Call Progress Detector					
Detect Level	2-Tones in 350-600 Hz band	-34		0	dBm0
Reject Level	2-Tones in 350-600 Hz band			-41	dBm0
Delay Time	-70 dBm0 to -30 dBm0 STEP	27		80	ms
Hold Time	-30 dBm0 to -70 dBm0 STEP	27		80	ms
Hysteresis		2			dB

Note: Parameters expressed in dBm0 refer to the following definition:

5V Version
0 dB loss in the Transmit path to the line.
2 dB gain in the Receive path from the line.

Refer to the Basic Box Modem diagram in the Applications section for the DAA design.

DYNAMIC CHARACTERISTICS AND TIMING (continued)

PARAMETER	CONDITION	MIN	NOM	MAX	UNIT
Carrier Detect					
Threshold	DPSK or FSK receive data	-49		-42	dBm0
Delay Time	-70 dBm0 to -30 dBm0 STEP	15		45	ms
Hysteresis	Single tone detected	2	3.0		dB
Hold Time	-30 dBm0 to -70 dBm0 STEP	10		24	ms
Answer Tone Detector					
Detect Level	Not in V.21 mode	-49.5		-42	dBm0
Delay Time	-70 dBm0 to -30 dBm0 STEP	20		45	ms
Hold Time	-30 dBm0 to -70 dBm0 STEP	10		30	ms
Detect Freq. Range		-2.5		+2.5	%
Output Smoothing Filter					
Output load	TXA pin; FSK Single	10			kΩ
	Tone out for THD = -50 db in 0.3 to 3.4 KHz			50	pF
Spurious Freq. Comp.	Frequency = 76.8 kHz			-39	dBm0
	Frequency = 153.6 kHz			-45	dBm0
Output Impedance	TXA pin		200	300	Ω
Clock Noise	TXA pin; 76.8 kHz			1.0	mVms
Carrier VCO					
Capture Range	Originate or Answer	-10		+10	Hz
Capture Time	-10 Hz to +10 Hz Carrier Frequency Change		40	100	ms
Recovered Clock					
Capture Range		-625		+625	ppm
Data Delay Time	Analog data in at RXA pin to receive data valid at RXD pin		30	50	ms

DYNAMIC CHARACTERISTICS AND TIMING (continued)

PARAMETER	CONDITION	MIN	NOM	MAX	UNIT
Guard Tone Generator					
Tone Accuracy	550 or 1800 Hz	-20		+20	Hz
Tone Level	550 Hz	-4.0	-3.0	-2.0	dB
(Below DPSK Output)	1800 Hz	-7.0	-6.0	-5.0	dB
Harmonic Distortion	550 Hz			-50	dB
700 to 2900 Hz	1800 Hz			-60	dB
Timing (Refer to Timing Diagrams)					
TAL	$\overline{CS}$/Addr. setup before ALE low	30			ns
TLA	$\overline{CS}$/Addr. hold after ALE low	20			ns
TLC	ALE low to $\overline{RD}$/$\overline{WR}$ low	40			ns
TCL	$\overline{RD}$/$\overline{WR}$ Control to ALE high	10			ns
TRD	Data out from $\overline{RD}$ low	0		160	ns
TLL	ALE width	60			ns
TRDF	Data float after $\overline{RD}$ high	0		80	ns
TRW	$\overline{RD}$ width	200		25000	ns
TWW	$\overline{WR}$ width	140		25000*	ns
TDW	Data setup before $\overline{WR}$ high	150			ns
TWD	Data hold after $\overline{WR}$ high	20			ns
TCKD	Data out after EXCLK low			200	ns
TCKW	$\overline{WR}$ after EXCLK low	150			ns
TDCK	Data setup before EXCLK low	150			ns
TAC	Address setup before control**	50			ns
TCA	Address hold after control**	50			ns
TWH	Data hold after EXCLK	150			ns

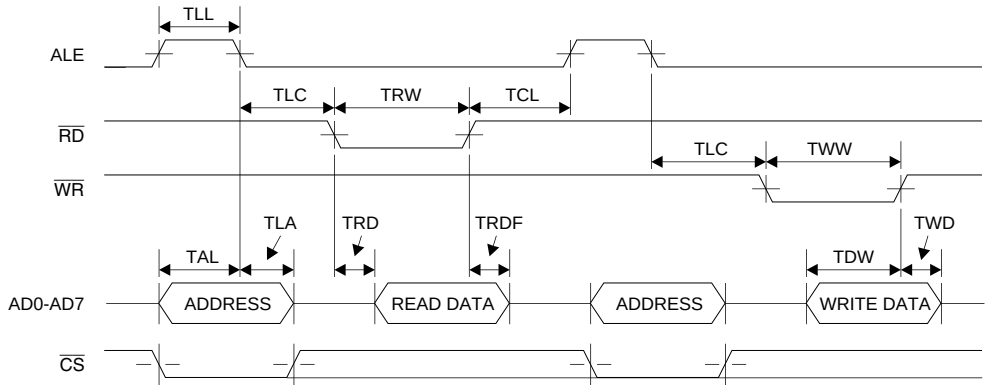
* Maximum time applies to parallel version only.

** Control for setup is the falling edge of $\overline{RD}$ or $\overline{WR}$.
Control for hold is the falling edge of $\overline{RD}$ or the rising edge of $\overline{WR}$.

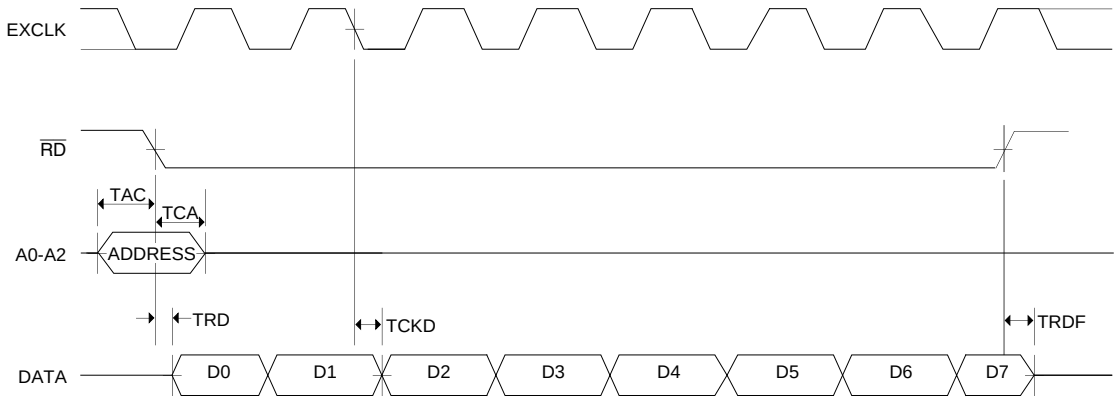
NOTE: Asserting ALE, $\overline{CS}$, and $\overline{RD}$ or $\overline{WR}$ concurrently can cause unintentional register accesses. When using non-831 compatible processors, care must be taken to prevent this from occurring when designing the interface logic.

TIMING DIAGRAMS

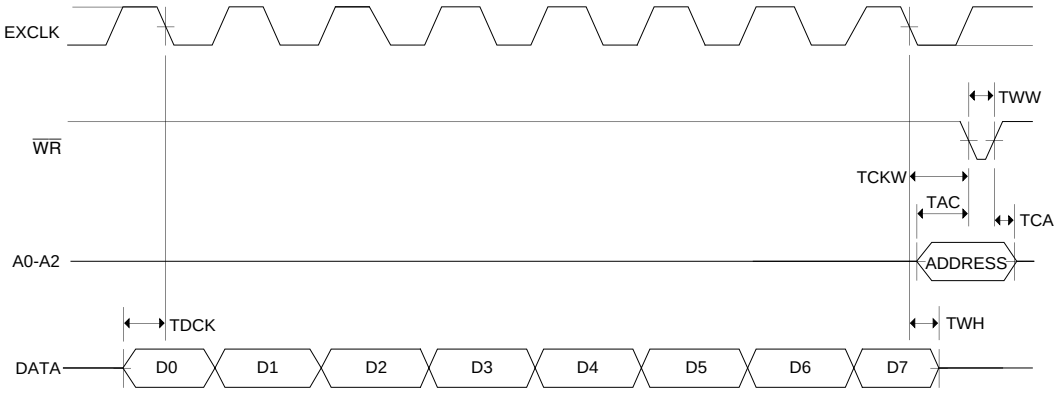
BUS TIMING DIAGRAM (PARALLEL VERSION)



READ TIMING DIAGRAM (SERIAL VERSION)



WRITE TIMING DIAGRAM (SERIAL VERSION)



APPLICATIONS INFORMATION

GENERAL CONSIDERATIONS

Figures 1 and 2 show basic circuit diagrams for K-Series modem integrated circuits. K-Series products are designed to be used in conjunction with a control processor, a UART or RS-232 serial data interface, and a DAA phone line interface to function as a typical intelligent modem. The K-Series ICs interface directly with Intel 8048 and 80C51 microprocessors for control and status monitoring purposes. Two typical DAA arrangements are shown: one for a split ±5 or ±12 volt design and one for a single 5 volt design. These diagrams are for reference only and do not represent production-ready modem designs.

K-Series devices are available with two control interface versions: one for a parallel multiplexed address/data interface, and one for a serial interface. The parallel version is intended for use with 8039/48 or 8031/51 microcontrollers from Intel or many other manufacturers. The serial interface 22-pin version can be used with other microcontrollers or in applications where only a limited number of port lines are available or the application does not lend itself to a multiplexed address/data interface. The parallel versions may also be used in the Serial mode, as explained in the data sheet pin description.

In most applications the controller will monitor the serial data for commands from the DTE and the received data for break signals from the far end modem. In this way, commands to the modem are sent over the same line as the transmitted data. In other applications the RS-232 interface handshake lines are used for modem control.

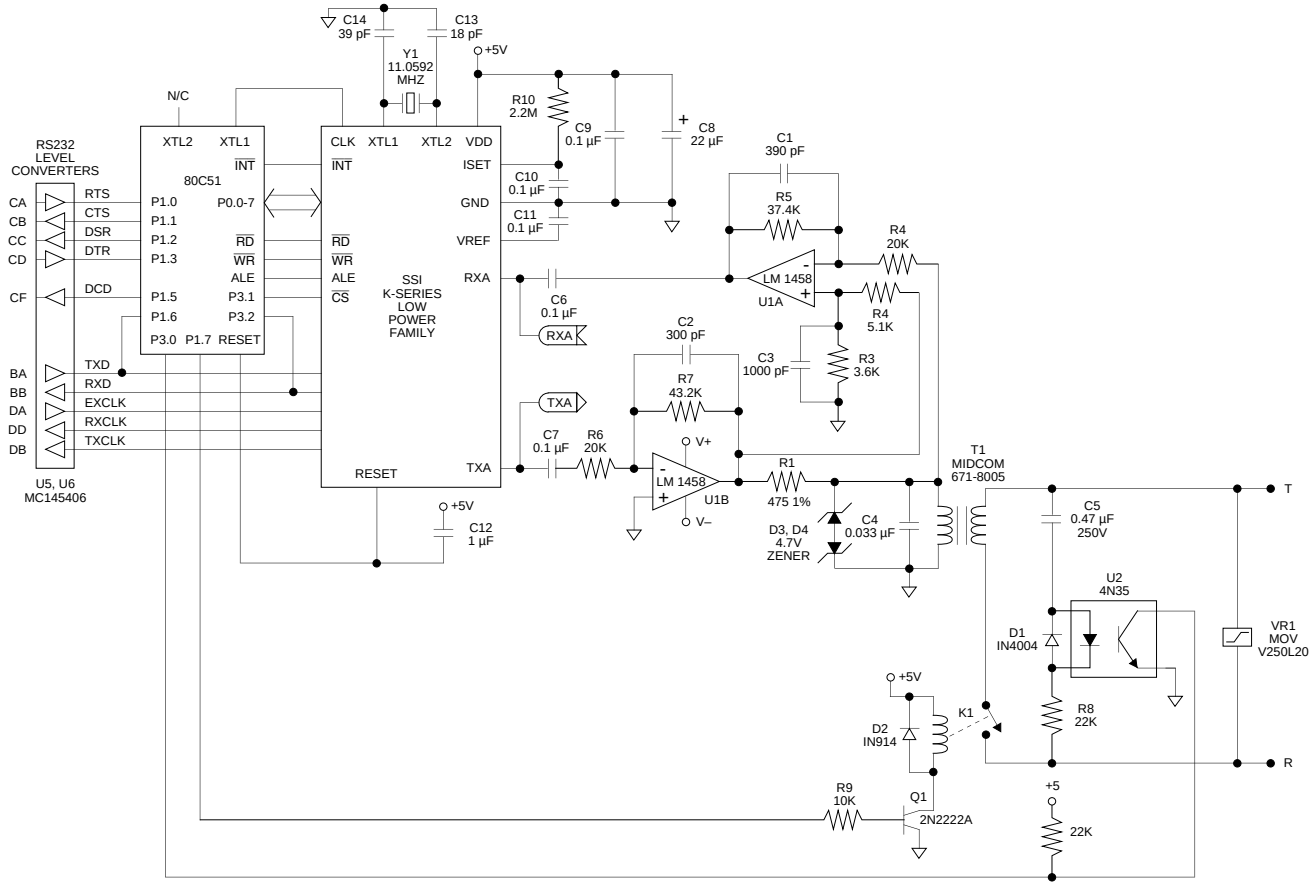


FIGURE 1: Basic Box Modem with Dual-Supply Hybrid

DIRECT ACCESS ARRANGEMENT (DAA)

The telephone line interfaces show two examples of how the "hybrid" may be implemented. The split supply design (Figure 1) is a typical two op-amp hybrid. The receive op-amp serves two purposes. It supplies gain to amplify the receive signal to the proper level for the modem's detectors and demodulator, and it removes the transmitted signal from the receive signal present at the transformer. This is done by supplying a portion of the transmitted signal to the non-inverting input of the receive op-amp at the same amplitude as the signal appearing at the transformer, making the transmit signal Common mode.

The single-supply hybrid is more complex than the dual-supply version described above, but its use eliminates the need for a second power supply. This circuit (Figure 2) uses a bridged drive to allow undistorted signals to be sent with a single 5 volt supply. Because DTMF tones utilize a higher amplitude than data, these signals will clip if a single-ended drive approach is used. The bridged driver uses an extra op-amp (U1A) to invert the signal coming from the gain setting op-amp (U1B) before sending it to the other leg of the transformer. Each op-amp then supplies half the drive signal to the transformer. The receive amplifier (U1C) picks off its signal at the junction of the impedance matching resistor and the transformer. Because the bottom leg of the transformer is being driven in one direction by U1A and the resistor is driven in the opposite direction at the same time by U1B, the junction of the transformer and resistor remains relatively constant and the receive signal is unaffected.

DESIGN CONSIDERATIONS

Silicon Systems 1-chip modem products include all basic modem functions. This makes these devices adaptable for use in a variety of applications, and as easy to control as conventional digital bus peripherals.

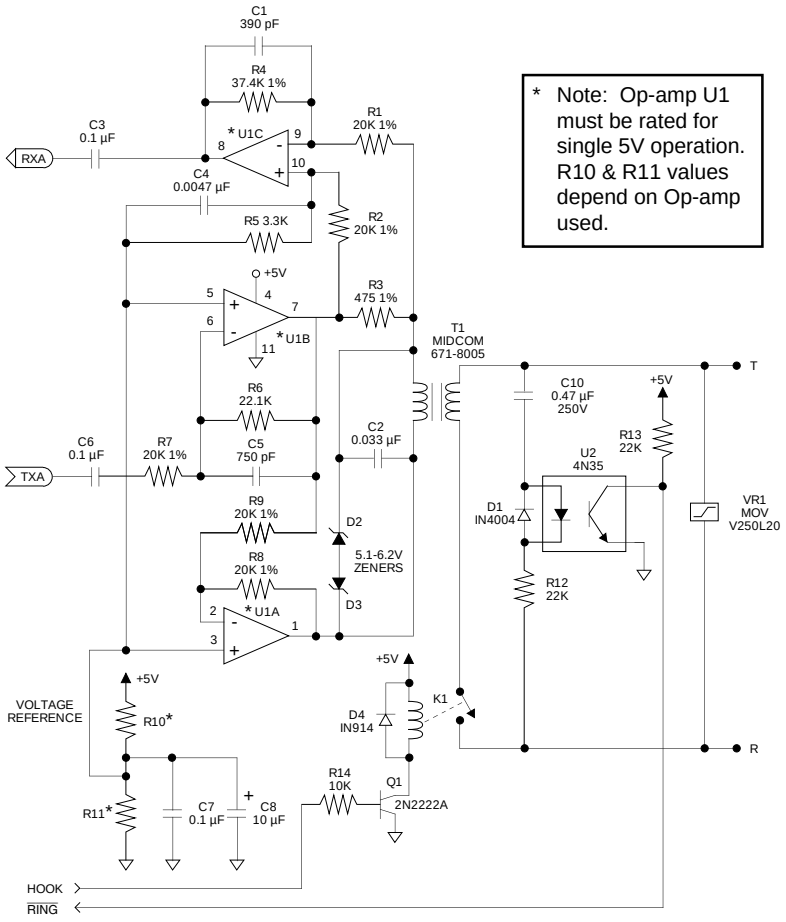


FIGURE 2: Single 5V Hybrid Version

Unlike digital logic circuitry, however, modem designs must properly contend with precise frequency tolerances and very low level analog signals, to ensure acceptable performance. Using good analog circuit design practices will generally result in a sound design. Following are additional recommendations which should be taken into consideration when starting new designs.

CRYSTAL OSCILLATOR

The K-Series crystal oscillator requires a Parallel mode (antiresonant) crystal which operates at 11.0592 MHz. It is important that this frequency be maintained to within ±0.01% accuracy.

In order for a Parallel mode crystal to operate correctly and to specification, it must have a load capacitor connected to the junction of each of the crystal and internal inverter connections, terminated to ground. The values of these capacitors depend primarily on the crystal's characteristics, and to a lesser degree on the internal inverter circuit. The values used affect the accuracy and start up characteristics of the oscillator.

LAYOUT CONSIDERATIONS

Good analog/digital design rules must be used to control system noise in order to obtain highest performance in modem designs. The more digital circuitry present on the PC board, the more this attention to noise control is needed. The modem should be treated as a high impedance analog device. A 22 µF electrolytic capacitor in parallel with a 0.1 µF ceramic capacitor between VDD and GND is recommended. Liberal use of ground planes and larger traces on power and ground are also highly favored. High speed digital circuits tend to generate a significant amount of EMI (Electro-Magnetic Interference) which must be minimized in order to meet regulatory agency limitations. To accomplish this, high speed digital devices should be locally bypassed, and the telephone line interface and K-Series device should be located close to each other near the area of the board where the phone line connection is accessed. To avoid problems, power supply and ground traces should be routed separately to the analog and digital functions on the board, and digital signals should not be routed near low level or high impedance analog traces. The analog and digital grounds should only connect at one point near the K-Series device ground pin to avoid ground loops. The K-Series modem IC's should have both high frequency and low frequency bypassing as close to the package as possible.

MODEM PERFORMANCE CHARACTERISTICS

The curves presented here define modem IC performance under a variety of line conditions while inducing disturbances that are typical of those encountered during data transmission on public service telephone lines. Test data was taken using an AEA Electronics' "Autotest I" modem test set and line simulator, operating under computer control. All tests were run full-duplex, using a Concord Data Systems 224 as the reference modem. A 511 pseudo-random-bit pattern was used for each data point. Noise was C-message weighted and all signal-to-noise (S/N) ratios reflect total power measurements similar to the CCITT V.56 measurement specification. The individual tests are defined as follows.

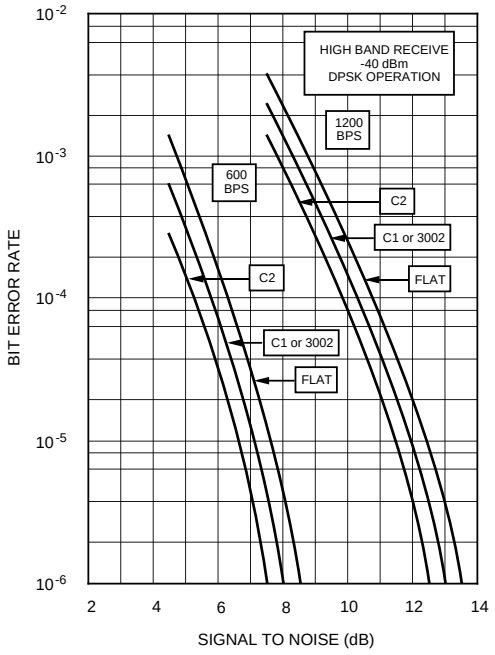
BER vs. S/N

This test measures the ability of the modem to operate over noisy lines with a minimum of data-transfer errors. Since some noise is generated in the best of dial-up lines, the modem must operate with the lowest S/N ratio possible. Better modem performance is indicated by test curves that are closest to the BER axis. A narrow spread between curves representing the four line parameters indicates minimal variation in performance while operating over a range of aberrant operating conditions. Typically, a DPSK modem will exhibit better BER-performance test curves receiving in the low band than in the high band.

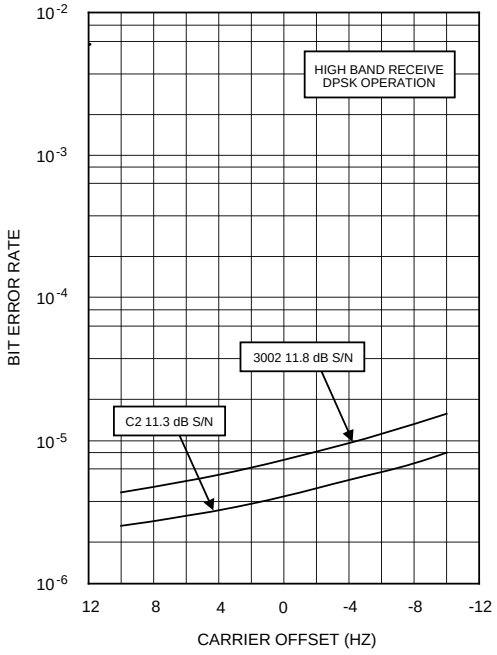
BER vs. Receive Level

This test measures the dynamic range of the modem. Because signal levels vary widely over dial-up lines, the widest possible dynamic range is desirable. The minimum Bell specification calls for 36 dB of dynamic range. S/N ratios are held constant at the indicated values while the receive level is lowered from a very high to very low signal levels. The width of the "bowl" of these curves, taken at the BER point, is the measure of dynamic range.

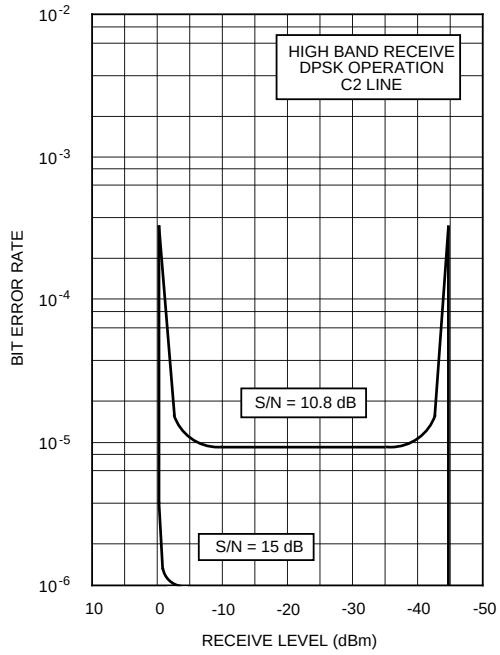
***SSI 73K221AL**
BER vs SIGNAL TO NOISE



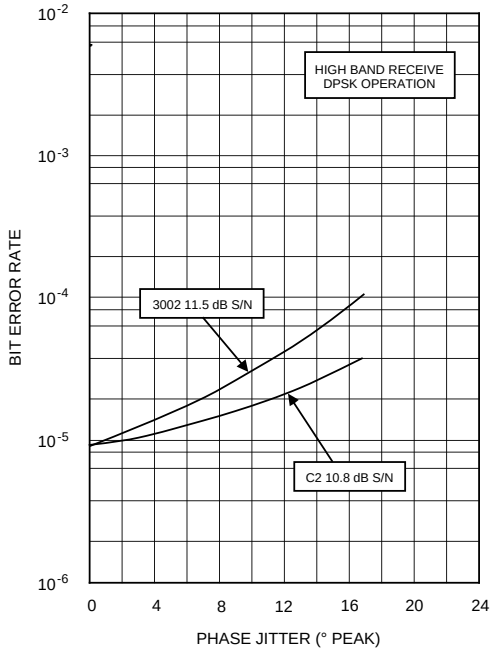
***SSI 73K221AL**
BER vs CARRIER OFFSET



***SSI 73K221AL**
BER vs RECEIVE LEVEL



***SSI 73K221AL**
BER vs PHASE JITTER

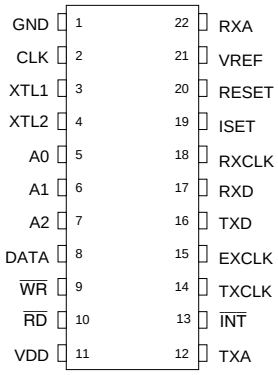


***** = "EQ On" indicates bit CR1 D4 is set for additional phase equalization.

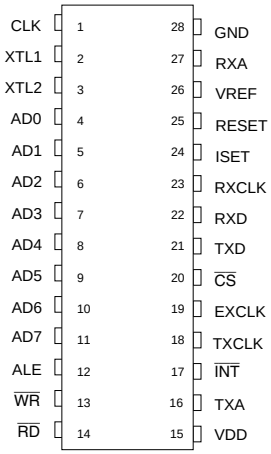
PACKAGE PIN DESIGNATIONS

(Top View)

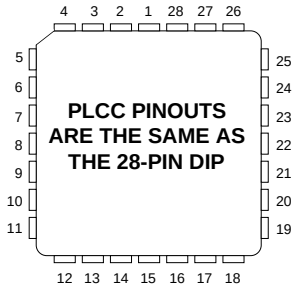
CAUTION: Use handling procedures necessary for a static sensitive component.



400-Mil 22-Pin DIP



600-Mil 28-Pin DIP



28-Pin PLCC

ORDERING INFORMATION

PART DESCRIPTION	ORDER NO.	PKG. MARK
SSI 73K221AL		
28-Pin Dual In-Line	73K221AL – IP	73K221AL – IP
28-Pin Plastic Leaded Chip Carrier	73K221AL – IH	73K221AL – IH
SSI 73K212AL		
22-Pin Dual In-Line	73K221ASL – IP	73K221ASL – IP

Silicon Systems, Inc., 14351 Myford Road, Tustin, CA 92680-7022, (714) 573-6000, FAX: (714) 573-6914

SSI 73K222AL
V.22, V.21, Bell 212A, 103 Single-Chip Modem

March 1996

DESCRIPTION

The SSI 73K222AL is a highly integrated single-chip modem IC which provides the functions needed to construct a CCITT V.22, V.21 and Bell 212A compatible modem, capable of 1200 bit/s full–duplex operation over dial-up lines. The SSI 73K222AL is an enhancement of the SSI 73K212L/AL single-chip modem which adds V.22 and V.21 modes to the Bell 212A and 103 operation of the SSI 73K212AL. In Bell 212A mode, the SSI 73K222AL provides the normal Bell 212A and 103 functions and employs a 2225 Hz answer tone. The SSI 73K222AL in V.22 mode produces either 550 or 1800 Hz guard tone, recognizes and generates a 2100 Hz answer tone, and allows 600 bit/s V.22 or 0-300 bit/s V.21 operation. The SSI 73K222AL integrates analog, digital, and switched-capacitor array functions on a single substrate, offering excellent performance and a high level of functional integration in a single 28- or 22-pin DIP configuration. The SSI 73K222AL operates from a single +5V supply. The SSI 73K222AL is a new version replacing the 73K222L. The SSI 73K2224AL should be specified for all new designs.

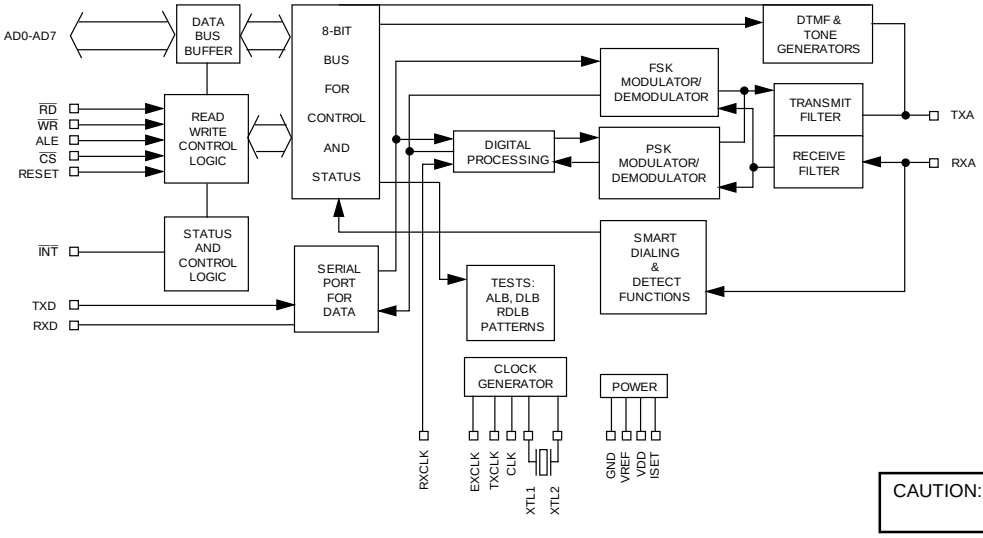
The SSI 73K222AL includes the DPSK and FSK modulator/demodulator functions, call progress and handshake tone monitor and a tone generator capable of

(continued)

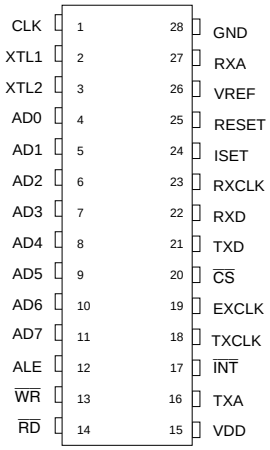
FEATURES

- **One-chip CCITT V.22, V.21, Bell 212A and 103 standard compatible modem data pump**
- **Full-duplex operation at 0-300 bit/s (FSK) or 600 and 1200 bit/s (DPSK)**
- **Pin and software compatible with other SSI K-Series 1-chip modems**
- **Interfaces directly with standard microprocessors (8048, 80C51 typical)**
- **Serial or parallel microprocessor bus for control**
- **Serial port for data transfer**
- **Both synchronous and asynchronous modes of operation including V.22 extended overspeed**
- **Call progress, carrier, precise answer tone (2100 or 2225 Hz), and long loop detectors**
- **DTMF, and 550 or 1800 Hz guard tone generators**
- **Test modes available: ALB, DL, RDL, Mark, Space, Alternating bit patterns**
- **Precise automatic gain control allows 45 dB dynamic range**
- **CMOS technology for low power consumption using 30 mW @ 5V**
- **Single +5 volt supply**

BLOCK DIAGRAM



PIN DIAGRAM



CAUTION: Use handling procedures necessary for a static sensitive component.

DESCRIPTION (continued)

tone required for European applications. This device supports V.22 (except mode v) and V. 21 modes of operation, allowing both synchronous and asynchronous communications. Test features such as analog loop, digital loop, and remote digital loopback are supported. Internal pattern generators are also included for self-testing. The SSI 73K222AL is designed to appear to the systems designer as a microprocessor peripheral, and will easily interface with popular one-chip microprocessors (80C51 typical) for control of modem functions through its 8-bit multiplexed address/data bus or serial control bus. An ALE control line simplifies address demultiplexing. Data communications occurs through a separate serial port only.

The SSI 73K222AL is ideal for use in either free standing or integral system modem products where full-duplex 1200 bit/s data communications over the 2-wire switched telephone network is desired. Its high functionality, low power consumption and efficient packaging simplify design requirements and increase system reliability. A complete modem requires only the addition of the phone line interface, a control microprocessor, and RS-232 level converter for a typical system. The SSI 73K222AL is part of Silicon Systems' K-Series family of pin and function compatible single-chip modem products. These devices allow systems to be configured for higher speeds and Bell or CCITT operation with only a single component change.

OPERATION

ASYNCHRONOUS MODE

Data transmission for the DPSK mode requires that data ultimately be transmitted in a synchronous fashion. The SSI 73K222AL includes ASYNC/SYNC and SYNC/ASYNC converters which delete or insert stop bits in order to transmit data within a ±0.01% rate. In asynchronous mode the serial data comes from the TXD pin into the ASYNC/SYNC converter. The ASYNC/SYNC converter accepts the data provided on the TXD pin which normally must be 1200 or 600 bit/s +1.0%, -2.5%. The converter will then insert or delete stop bits in order to output a signal which is 1200 or 600 bit/s ± 0.01% (± 0.01% is required synchronous data rate accuracy).

The serial data stream from the ASYNC/SYNC converter is passed through the data scrambler and onto the analog modulator. The data scrambler can be bypassed under processor control when unscrambled data must be transmitted. The ASYNC/SYNC converter and the data scrambler are bypassed in all FSK modes. If serial input data contains a break signal through one character (including start and stop bits) the break will be extended to at least 2 • N + 3 bits long (where N is the number of transmitted bits/character).

Serial data from the demodulator is passed first through the data descrambler and then through the SYNC/ASYNC converter. The SYNC/ASYNC convertor will reinsert any deleted stop bits and transmit output data at an intra-character rate (bit-to-bit timing) of no greater than 1219 bit/s. An incoming break signal (low through two characters) will be passed through without incorrectly inserting a stop bit.

The SYNC/ASYNC converter also has an extended overspeed mode which allows selection of an overspeed range of either +1% or +2.3%. In the extended overspeed mode, stop bits are output at 7/8 the normal width.

SYNCHRONOUS MODE

The CCITT V.22 standard defines synchronous operation at 600 and 1200 bit/s. The Bell 212A standard defines synchronous operation only at 1200 bit/s. Operation is similar to that of the asynchronous mode except that data must be synchronized to a provided clock and no variation in data transfer rate is allowable. Serial input data appearing at TXD must be valid on the rising edge of TXCLK.

TXCLK is an internally derived signal in internal mode and is connected internally to the RXCLK pin in slave mode. Receive data at the RXD pin is clocked out on the falling edge of RXCLK. The ASYNCH/SYNCH converter is bypassed when synchronous mode is selected and data is transmitted out at the same rate as it is input.

DPSK MODULATOR/DEMODULATOR

The SSI 73K222AL modulates a serial bit stream into di-bit pairs that are represented by four possible phase shifts as prescribed by the Bell 212A or V.22 standards. The baseband signal is then filtered to reduce intersymbol interference on the bandlimited 2-wire telephone line. Transmission occurs using either a

1200 Hz (originate mode) or 2400 Hz carrier (answer mode). Demodulation is the reverse of the modulation process, with the incoming analog signal eventually decoded into di-bits and converted back to a serial bit stream. The demodulator also recovers the clock which was encoded into the analog signal during modulation. Demodulation occurs using either a 1200 Hz carrier (answer mode or ALB originate mode) or a 2400 Hz carrier (originate mode or ALB answer mode). The SSI 73K222AL uses a phase locked loop coherent demodulation technique for optimum receiver performance.

FSK MODULATOR/DEMODULATOR

The FSK modulator produces a frequency modulated analog output signal using two discrete frequencies to represent the binary data. In Bell 103, the standard frequencies of 1270 and 1070 Hz (originate, mark and space) or 2225 and 2025 Hz (answer, mark and space) are used. V.21 mode uses 980 and 1180 Hz (originate, mark and space), or 1650 and 1850Hz (answer, mark and space). Demodulation involves detecting the received frequencies and decoding them into the appropriate binary value. The rate converter and scrambler/descrambler are bypassed in the 103 or V.21 modes.

PASSBAND FILTERS AND EQUALIZERS

High and low band filters are included to shape the amplitude and phase response of the transmit and receive signals and provide compromise delay equalization and rejection of out-of-band signals in the receive channel. Amplitude and phase equalization are necessary to compensate for distortion of the transmission line and to reduce intersymbol interference in the bandlimited receive signal. The transmit signal filtering approximates a 75% square root of raised Cosine frequency response characteristic.

AGC

The automatic gain control maintains a signal level at the input to the demodulators which is constant to within 1 dB. It corrects quickly for increases in signal which would cause clipping and provides a total receiver dynamic range of >45 dB.

PARALLEL BUS INTERFACE

Four 8-bit registers are provided for control, option select and status monitoring. These registers are addressed with the AD0, AD1, and AD2 multiplexed address lines (latched by ALE) and appear to a control microprocessor as four consecutive memory locations. Two control registers and the tone register are read/write memory. The detect register is read only and cannot be modified except by modem response to monitored parameters.

SERIAL COMMAND INTERFACE

The serial command interface allows access to the SSI 73K222AL control and status registers via a serial command port (22-pin version only). In this mode the A0, A1 and A2 lines provide register addresses for data passed through the data pin under control of the $\overline{RD}$ and $\overline{WR}$ lines. A read operation is initiated when the $\overline{RD}$ line is taken low. The first bit is available after $\overline{RD}$ is brought low and the next seven cycles of EXCLK will then transfer out seven bits of the selected address LSB first. A write takes place by shifting in eight bits of data LSB first for eight consecutive cycles of EXCLK. $\overline{WR}$ is then pulsed low and data transferred into the addressed register occurs on the rising edge of $\overline{WR}$. This interface mode is also supported in the 28-pin packages. See serial control interface pin description.

SPECIAL DETECT CIRCUITRY

The special detect circuitry monitors the received analog signal to determine status or presence of carrier, call-progress tones, answer tone and weak received signal (long loop condition). An unscrambled mark request signal is also detected when the received data out of the DPSK demodulator before the descrambler has been high for 165.5 ms $\pm$ 6.5 ms minimum. The appropriate detect register bit is set when one of these conditions changes and an interrupt is generated for all purposes except long loop. The interrupts are disabled (masked) when the enable interrupt bit is set to 0.

DTMF GENERATOR

The DTMF generator will output one of 16 standard tone pairs determined by a 4-bit binary value and TX DTMF mode bit previously loaded into the tone register. Tone generation is initiated when the DTMF mode is selected using the tone register and the transmit enable (CR0 bit D1) is changed from 0 to 1.

PIN DESCRIPTION

POWER

NAME	28-PIN	22-PIN	TYPE	DESCRIPTION
GND	28	1	I	System Ground.
VDD	15	11	I	Power supply input, 5V ±10%. Bypass with 0.1 and 22 µF capacitors to GND.
VREF	26	21	O	An internally generated reference voltage. Bypass with 0.1 µF capacitor to ground.
ISET	24	19	I	Chip current reference. Sets bias current for op-amps. The chip current is set by connecting this pin to VDD through a 2 MΩ resistor. ISET should be bypassed to GND with a 0.1 µF capacitor.

PARALLEL MICROPROCESSOR INTERFACE

ALE	12	-	I	Address latch enable. The falling edge of ALE latches the address on AD0-AD2 and the chip select on $\overline{CS}$.
AD0-AD7	4-11	-	I/O	Address/data bus. These bidirectional tri-state multiplexed lines carry information to and from the internal registers.
$\overline{CS}$	20	-	I	Chip select. A low on this pin during the falling edge of ALE allows a read cycle or a write cycle to occur. AD0-AD7 will not be driven and no registers will be written if $\overline{CS}$ (latched) is not active. The state of $\overline{CS}$ is latched on the falling edge of ALE.
CLK	1	2	O	Output clock. This pin is selectable under processor control to be either the crystal frequency (for use as a processor clock) or 16 x the data rate for use as a baud rate clock in DPSK modes only. The pin defaults to the crystal frequency on reset.
$\overline{INT}$	17	13	O	Interrupt. This open drain output signal is used to inform the processor that a detect flag has occurred. The processor must then read the detect register to determine which detect triggered the interrupt. $\overline{INT}$ will stay low until the processor reads the detect register or does a full reset.
$\overline{RD}$	14	-	I	Read. A low requests a read of the SSI 73K222AL internal registers. Data cannot be output unless both $\overline{RD}$ and the latched $\overline{CS}$ are active or low.
RESET	25	20	I	Reset. An active high signal on this pin will put the chip into an inactive state. All control register bits (CR0, CR1, Tone) will be reset. The output of the CLK pin will be set to the crystal frequency. An internal pull down resistor permits power on reset using a capacitor to VDD.

PARALLEL MICROPROCESSOR INTERFACE (continued)

NAME	28-PIN	22-PIN	TYPE	DESCRIPTION
$\overline{WR}$	13	-	I	Write. A low on this informs the SSI 73K222AL that data is available on AD0-AD7 for writing into an internal register. Data is latched on the rising edge of $\overline{WR}$. No data is written unless both $\overline{WR}$ and the latched $\overline{CS}$ are low.

SERIAL MICROPROCESSOR INTERFACE

A0-A2	-	5-7	I	Register Address Selection. These lines carry register addresses and should be valid during any read or write operation.
DATA	-	8	I/O	Serial Control Data. Data for a read/write operation is clocked in or out on the falling edge of the EXCLK pin. The direction of data flow is controlled by the $\overline{RD}$ pin. $\overline{RD}$ low outputs data. $\overline{RD}$ high inputs data.
$\overline{RD}$	-	10	I	Read. A low on this input informs the SSI 73K222AL that data or status information is being read by the processor. The falling edge of the $\overline{RD}$ signal will initiate a read from the addressed register. The $\overline{RD}$ signal must continue for eight falling edges of EXCLK in order to read all eight bits of the referenced register. Read data is provided LSB first. Data will not be output unless the $\overline{RD}$ signal is active.
$\overline{WR}$	-	9	I	Write. A low on this input informs the SSI 73K222AL that data or status information has been shifted in through the DATA pin and is available for writing to an internal register. The normal procedure for a write is to shift in data LSB first on the DATA pin for eight consecutive falling edges of EXCLK and then to pulse $\overline{WR}$ low. Data is written on the rising edge of $\overline{WR}$.

Note: In the serial, 22-pin version, the pins AD0-AD7, ALE and $\overline{CS}$ are removed and replaced with the pins; A0, A1, A2, DATA, and an unconnected pin. Also, the $\overline{RD}$ and $\overline{WR}$ controls are used differently.

The serial control mode is provided in the parallel control versions by tying ALE high and $\overline{CS}$ low. In this configuration AD7 becomes DATA and AD0, AD1 and AD2 become A0, A1 and A2, respectively.

PIN DESCRIPTION (continued)

DTE USER

NAME	28-PIN	22-PIN	TYPE	DESCRIPTION
EXCLK	19	15	I	External Clock. This signal is used in synchronous transmission when the external timing option has been selected. In the external timing mode the rising edge of EXCLK is used to strobe synchronous DPSK transmit data applied to on the TXD pin. Also used for serial control interface.
RXCLK	23	18	O	Receive Clock. The falling edge of this clock output is coincident with the transitions in the serial received data output. The rising edge of RXCLK can be used to latch the valid output data. RXCLK will be valid as long as a carrier is present.
RXD	22	17	O	Received Data Output. Serial receive data is available on this pin. The data is always valid on the rising edge of RXCLK when in synchronous mode. RXD will output constant marks if no carrier is detected.
TXCLK	18	14	O	Transmit Clock. This signal is used in synchronous transmission to latch serial input data on the TXD pin. Data must be provided so that valid data is available on the rising edge of the TXCLK. The transmit clock is derived from different sources depending upon the synchronization mode selection. In Internal Mode the clock is generated internally. In External Mode TXCLK is phase locked to the EXCLK pin. In Slave Mode TXCLK is phase locked to the RXCLK pin. TXCLK is always active.
TXD	21	16	I	Transmit Data Input. Serial data for transmission is applied on this pin. In synchronous modes, the data must be valid on the rising edge of the TXCLK clock. In asynchronous modes (1200/600 bit/s or 300 baud) no clocking is necessary. DPSK data must be 1200/600 bit/s +1%, -2.5% or +2.3%, -2.5 % in extended overspeed mode.

ANALOG INTERFACE AND OSCILLATOR

RXA	27	22	I	Received modulated analog signal input from the telephone line interface.
TXA	16	12	O	Transmit analog output to the telephone line interface.
XTL1 XTL2	2 3	3 4	I I	These pins are for the internal crystal oscillator requiring a 11.0592 MHz parallel mode crystal. Load capacitors should be connected from XTL1 and XTL2 to Ground. XTL2 can also be driven from an external clock.

REGISTER DESCRIPTIONS

Four 8-bit internal registers are accessible for control and status monitoring. The registers are accessed in read or write operations by addressing the A0, A1 and A2 address lines in serial mode, or the AD0, AD1 and AD2 lines in parallel mode. In parallel mode the address lines are latched by ALE. Register CR0 controls the method by which data is transferred over the phone line. CR1 controls the interface between the microprocessor and the SSI 73K222AL internal state. DR is a detect register which provides an indication of monitored modem status conditions. TR, the tone control register, controls the DTMF generator, answer and guard tones and RXD output gate used in the modem initial connect sequence. All registers are read/write except for DR which is read only. Register control and status bits are identified below:

REGISTER BIT SUMMARY

	ADDRESS	DATA BIT NUMBER							
REGISTER	AD2 - AD0	D7	D6	D5	D4	D3	D2	D1	D0
CONTROL REGISTER 0 CR0	000	MODULATION OPTION	0	TRANSMIT MODE 3	TRANSMIT MODE 2	TRANSMIT MODE 1	TRANSMIT MODE 0	TRANSMIT ENABLE	ANSWER/ ORIGINATE
CONTROL REGISTER 1 CR1	001	TRANSMIT PATTERN 1	TRANSMIT PATTERN 0	ENABLE DETECT INTERRUPT	BYPASS SCRAMBLER	CLK CONTROL	RESET	TEST MODE 1	TEST MODE 0
DETECT REGISTER DR	010	X	X	RECEIVE DATA	UNSCR. MARKS	CARRIER DETECT	ANSWER TONE	CALL PROGRESS	LONG LOOP
TONE CONTROL REGISTER TR	011	RXD OUTPUT CONTROL	TRANSMIT GUARD TONE	TRANSMIT ANSWER TONE	TRANSMIT DTMF	DTMF3	DTMF2	DTMF1/ OVERSPEED	DTMF0/ GUARD/ ANS TONE
CONTROL REGISTER 2 CR2	100	X	X	X	THESE REGISTER LOCATIONS ARE RESERVED FOR				X
CONTROL REGISTER 3 CR3	101	X	X	X	USE WITH OTHER K-SERIES FAMILY MEMBERS				X
ID REGISTER ID	110	ID	ID	ID	ID	X	X	X	X

NOTE: When a register containing reserved control bits is written into, the reserved bits must be programmed as 0's.

X = Undefined, mask in software

REGISTER ADDRESS TABLE

REGISTER	ADDRESS	DATA BIT NUMBER							
	AD2 - AD0	D7	D6	D5	D4	D3	D2	D1	D0
CONTROL REGISTER 0 CR0	000	MODULATION OPTION	0	TRANSMIT MODE 3	TRANSMIT MODE 2	TRANSMIT MODE 1	TRANSMIT MODE 0	TRANSMIT ENABLE	ORIGINATE/ ANSWER
		0=1200 BIT/S DPSK 1=600 BIT/S DPSK 0=BELL 103 FSK 1=V.21 FSK		0000=PWR DOWN 0001=INT SYNCH 0010=EXT SYNCH 0011=SLAVE SYNCH 0100=ASYNCH 8 BITS/CHAR 0101=ASYNCH 9 BITS/CHAR 0110=ASYNCH 10 BITS/CHAR 0111=ASYNCH 11 BITS/CHAR 1100=FSK				0=DISABLE TXA OUTPUT 1=ENABLE TXA OUTPUT	0=ANSWER 1=ORIGINATE
CONTROL REGISTER 1 CR1	001	TRANSMIT PATTERN 1	TRANSMIT PATTERN 0	ENABLE DETECT INTERRUPT	BYPASS SCRAMBLER	CLK CONTROL	RESET	TEST MODE 1	TEST MODE 0
		00=TX DATA 01=TX ALTERNATE 10=TX MARK 11=TX SPACE		0=DISABLE 1=ENABLE	0=NORMAL 1=BYPASS SCRAMBLER	0=XTAL 1=16 X DATA RATE OUTPUT AT CLK PIN IN DPSK MODE ONLY	0=NORMAL 1=RESET	00=NORMAL 01=ANALOG LOOPBACK 10=REMOTE DIGITAL LOOPBACK 11=LOCAL DIGITAL LOOPBACK	
DETECT REGISTER DR	010	X	X	RECEIVE DATA	UNSCR. MARKS	CARRIER DETECT	ANSWER TONE	CALL PROGRESS	LONG LOOP
				OUTPUTS RECEIVED DATA STREAM	0=CONDITION NOT DETECTED 1=CONDITION DETECTED				
TONE CONTROL REGISTER TR	011	RXD OUTPUT CONTROL	TRANSMIT GUARD/ TONE	TRANSMIT ANSWER TONE	TRANSMIT DTMF	DTMF3	DTMF2	DTMF1/ OVERSPEED	DTMF0/ GUARD/ ANSWER/ TONE
		RXD PIN 0=NORMAL 1=TRI STATE	0=OFF 1=ON	0=OFF 1=ON	0=DATA 1=TX DTMF	4 BIT CODE FOR 1 OF 16 DUAL TONE COMBINATIONS.			0=2225 Hz A.T. 1800 Hz G.T. 1=2100 Hz A.T. 500 Hz G.T.
ID REGISTER 10	110	ID	ID	ID	ID	X	X	X	X

00XX=73K212L/AL, 322L, 321L
01XX=73K221L/AL, 302L
10XX=73K222L/AL
1100=73K224L
1110=73K324L
1101=73K312L

X = Undefined, mask in software

CONTROL REGISTER 0

	D7	D6	D5	D4	D3	D2	D1	D0
CR0 000	MODUL. OPTION	0	TRANSMIT MODE 3	TRANSMIT MODE 2	TRANSMIT MODE 1	TRANSMIT MODE 0	TRANSMIT ENABLE	ANSWER/ ORIGINATE

BIT NO.	NAME	CONDITION	DESCRIPTION
D0	Answer/ Originate	0	Selects answer mode (transmit in high band, receive in low band).
		1	Selects originate mode (transmit in low band, receive in high band).
D1	Transmit Enable	0	Disables transmit output at TXA.
		1	Enables transmit output at TXA. Note: TX Enable must be set to 1 to allow Answer Tone and DTMF Transmiission.
D5, D4,D3, D2	Transmit Mode	D5 D4 D3 D2	
		0 0 0 0	Selects power down mode. All functions disabled except digital interface.
		0 0 0 1	Internal synchronous mode. In this mode TXCLK is an internally derived 1200 Hz signal. Serial input data appearing at TXD must be valid on the rising edge of TXCLK. Receive data is clocked out of RXD on the falling edge of RXCLK.
		0 0 1 0	External synchronous mode. Operation is identical to internal synchronous, but TXCLK is connected internally to EXCLK pin, and a 1200 Hz ± 0.01% clock must be supplied externally.
		0 0 1 1	Slave synchronous mode. Same operation as other synchronous modes. TXCLK is connected internally to the RXCLK pin in this mode.
		0 1 0 0	Selects PSK asynchronous mode - 8 bits/character (1 start bit, 6 data bits, 1 stop bit).
		0 1 0 1	Selects PSK asynchronous mode - 9 bits/character (1 start bit, 7 data bits, 1 stop bit).
		0 1 1 0	Selects PSK asynchronous mode - 10 bits/character (1 start bit, 8 data bits, 1 stop bit).
		0 1 1 1	Selects PSK asynchronous mode - 11 bits/character (1 start bit, 8 data bits, Parity and 1 or 2 stop bits).
		1 1 0 0	Selects FSK operation.
D6		0	Not used; must be written as a “0.”

CONTROL REGISTER 0 (continued)

	D7	D6	D5	D4	D3	D2	D1	D0
CR0 000	MODUL. OPTION	0	TRANSMIT MODE 3	TRANSMIT MODE 2	TRANSMIT MODE 1	TRANSMIT MODE 0	TRANSMIT ENABLE	ANSWER/ ORIGINATE

BIT NO.	NAME	CONDITION	DESCRIPTION
D7	Modulation Option	D7 D5 D4	Selects:
		0 0 X	DPSK mode at 1200 bit/s.
		1 0 X	DPSK mode at 600 bit/s.
		0 1 1	FSK Bell 103 mode.
		1 1 1	FSK CCITT V.21 mode.
			X = Don't care

CONTROL REGISTER 1

	D7	D6	D5	D4	D3	D2	D1	D0
CR1 001	TRANSMIT PATTERN 1	TRANSMIT PATTERN 0	ENABLE DETECT INTER.	BYPASS SCRAMB	CLK CONTROL	RESET	TEST MODE 1	TEST MODE 0

BIT NO.	NAME	CONDITION	DESCRIPTION
D1, D0	Test Mode	D1 D0	
		0 0	Selects normal operating mode.
		0 1	Analog loopback mode. Loops the transmitted analog signal back to the receiver, and causes the receiver to use the same center frequency as the transmitter. To squelch the TXA pin, transmit enable must be forced low.
		1 0	Selects remote digital loopback. Received data is looped back to transmit data internally, and RXD is forced to a mark. Data on TXD is ignored.
		1 1	Selects local digital loopback. Internally loops TXD back to RXD and continues to transmit carrier from TXA pin.
D2	Reset	0	Selects normal operation.
		1	Resets modem to power down state. All control register bits (CR0, CR1, Tone) are reset to zero. The output of the CLK pin will be set to the crystal frequency.
D3	CLK Control (Clock Control)	0	Selects 11.0592 MHz crystal echo output at CLK pin.
		1	Selects 16 X the data rate, output at CLK pin in DPSK modes only.

CONTROL REGISTER 1 (continued)

	D7	D6	D5	D4	D3	D2	D1	D0
CR1 001	TRANSMIT PATTERN 1	TRANSMIT PATTERN 0	ENABLE DETECT INTER.	BYPASS SCRAMB	CLK CONTROL	RESET	TEST MODE 1	TEST MODE 0

BIT NO.	NAME	CONDITION	DESCRIPTION
D4	Bypass Scrambler	0	Selects normal operation. DPSK data is passed through scrambler.
		1	Selects Scrambler Bypass. Bypass DPSK data is routed around scrambler in the transmit path.
D5	Enable Detect	0	Disables interrupt at $\overline{INT}$ pin.
		1	Enables $\overline{INT}$ output. An interrupts will be generated with a change in status of DR bits D1-D4. The answer tone and call progress detect interrupts are masked when the TX enable bit is set. Carrier detect is masked when TX DTMF is activated. All interrupts will be disabled if the device is in power down mode.
D7, D6	Transmit Pattern	D7 D6	
		0 0	Selects normal data transmission as controlled by the state of the TXD pin.
		0 1	Selects an alternating mark/space transmit pattern for modem testing.
		1 0	Selects a constant mark transmit pattern.
		1 1	Selects a constant space transmit pattern.

DETECT REGISTER

	D7	D6	D5	D4	D3	D2	D1	D0
DR 010	X	X	RECEIVE DATA	UNSCR. MARK	CARR. DETECT	ANSWER TONE	CALL PROG.	LONG LOOP

BIT NO.	NAME	CONDITION	DESCRIPTION
D0	Long Loop	0	Indicates normal received signal.
		1	Indicates low received signal level.
D1	Call Progress Detect	0	No call progress tone detected.
		1	Indicates presence of call progress tones. The call progress detection circuitry is activated by energy in the 350 to 620 Hz call progress band.

DETECT REGISTER (continued)

	D7	D6	D5	D4	D3	D2	D1	D0
DR 010	X	X	RECEIVE DATA	UNSCR. MARK	CARR. DETECT	ANSWER TONE	CALL PROG.	LONG LOOP

BIT NO.	NAME	CONDITION	DESCRIPTION
D2	Answer Tone Detect	0	No answer tone detected.
		1	Indicates detection of 2225 Hz answer tone in Bell mode or 2100 Hz in CCITT mode. The device must be in originate mode for detection of answer tone. For CCITT answer tone detection, bit D0 of the Tone Register must be set to a 1.
D3	Carrier Detect	0	No carrier detected in the receive channel.
		1	Indicates carrier has been detected in the receive channel.
D4	Unscrambled Mark Detect	0	No unscrambled mark.
		1	Indicates detection of unscrambled marks in the received data. A valid indication requires that unscrambled marks be received for > 165.5 ± 6.5 ms.
D5	Receive Data		Continuously outputs the received data stream. This data is the same as that output on the RXD pin, but it is not disabled when RXD is tri-stated.
D6, D7	Not Used	Undefined	Not used. Mask in software.

TONE REGISTER

	D7	D6	D5	D4	D3	D2	D1	D0
TR 011	RXD OUTPUT CONTR.	TRANSMIT GUARD TONE	TRANSMIT ANSWER TONE	TRANSMIT DTMF	DTMF 3	DTMF 2	DTMF 1/ OVER-SPEED	DTMF 0/ ANSWER/ GUARD

BIT NO.	NAME	CONDITION	DESCRIPTION
D0	DTMF 0/ Answer/ Guard Tone	D6 D5 D4 D0	D0 interacts with bits D6, D5, and D4 as shown.
		X X 1 X	Transmit DTMF tones.
		X 0 0 0	Detects 2225 Hz in originate mode.
		X 1 0 0	Transmits 2225 Hz in answer mode (Bell).
		X 0 0 1	Detects 2100 Hz in originate mode.
		X 1 0 1	Transmits 2100 Hz in answer mode (CCITT).
		1 0 0 0	Select 1800 Hz guard tone.
		1 0 0 1	Select 550 Hz guard tone.
D1	DTMF 1/ Overspeed	D4 D1	D1 interacts with D4 as shown.
		0 0	Asynchronous DPSK +1.0% -2.5%.
		0 1	Asynchronous DPSK +2.3% -2.5%.

TONE REGISTER

	D7	D6	D5	D4	D3	D2	D1	D0
TR 011	RXD OUTPUT CONTR.	TRANSMIT GUARD TONE	TRANSMIT ANSWER TONE	TRANSMIT DTMF	DTMF 3	DTMF 2	DTMF 1/ OVER-SPEED	DTMF 0/ ANSWER/ GUARD

BIT NO.	NAME	CONDITION	DESCRIPTION
D3, D2, D1, D0	DTMF 3, 2, 1, 0	D3 D2 D1 D0 0 0 0 0 - 1 1 1 1	Programs 1 of 16 DTMF tone pairs that will be transmitted when TX DTMF and TX enable bit (CR0, bit D1) are set. Tone encoding is shown below:
D4	Transmit DTMF	0	Disable DTMF.
		1	Activates DTMF. The selected DTMF tones are transmitted continuously when this bit is high. TX DTMF overrides all other transmit functions.
D5	Transmit Answer Tone	D5 D4 D0	D5 interacts with bits D4 and D0 as shown.
		0 0 X	Disables answer tone generator.
		1 0 0	Enables answer tone generator. A 2225 Hz answer tone will be transmitted continuously when the Transmit Enable bit is set in CR0. The device must be in answer mode.
		1 0 1	Likewise a 2100 Hz answer tone will be transmitted.

KEYBOARD EQUIVALENT	DTMF CODE D3 D2 D1 D0	TONES LOW HIGH
1	0 0 0 1	697 1209
2	0 0 1 0	697 1336
3	0 0 1 1	697 1477
4	0 1 0 0	770 1209
5	0 1 0 1	770 1336
6	0 1 1 0	770 1477
7	0 1 1 1	852 1209
8	1 0 0 0	852 1336
9	1 0 0 1	852 1477
0	1 0 1 0	941 1336
*	1 0 1 1	941 1209
#	1 1 0 0	941 1477
A	1 1 0 1	697 1633
B	1 1 1 0	770 1633
C	1 1 1 1	852 1633
D	0 0 0 0	941 1633

TONE REGISTER (continued)

	D7	D6	D5	D4	D3	D2	D1	D0
TR 011	RXD OUTPUT CONTR.	TRANSMIT GUARD TONE	TRANSMIT ANSWER TONE	TRANSMIT DTMF	DTMF 3	DTMF 2	DTMF 1/ OVER-SPEED	DTMF 0/ ANSWER/ GUARD

BIT NO.	NAME	CONDITION	DESCRIPTION
D6	Transmit Guard Tone	0	Disables guard tone generator.
		1	Enables guard tone generator (See D0 for selection of guard tones).
D7	RXD Output Control	0	Enables RXD pin. Receive data will be output on RXD.
		1	Disables RXD pin. The RXD pin reverts to a high impedance with internal weak pull-up resistor.

ID REGISTER

	D7	D6	D5	D4	D3	D2	D1	D0
ID 110	ID	ID	ID	ID	X	X	X	X

BIT NO.	NAME	CONDITION	DESCRIPTION
D7, D6, D5, D4	Device Identification Signature	D7 D6 D5 D4	Indicates Device:
		0 0 X X	SSI 73K212L/AL, 73K321L, 73K322L or 73K321L
		0 1 X X	SSI 73K221L/AL or 73K302L
		1 0 X X	SSI 73K222L/AL
		1 1 0 0	SSI 73K224L
		1 1 1 0	SSI 73K324L
		1 1 0 1	SSI 73K312L
D3-D0	Not Used	Undefined	Mask in software

ELECTRICAL SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING
VDD Supply Voltage	7V
Storage Temperature	-65 to 150°C
Soldering Temperature (10 sec.)	260°C
Applied Voltage	-0.3 to VDD + 0.3V
Note: All inputs and outputs are protected from static charge using built-in, industry standard protection devices and all outputs are short-circuit protected.	

RECOMMENDED OPERATING CONDITIONS

PARAMETER	CONDITION	MIN	NOM	MAX	UNIT
VDD Supply voltage		4.5	5	5.5	V
TA, Operating Free-Air Temperature		-40		+85	°C
Clock Variation	(11.0592 MHz) Crystal or external clock	-0.01		+0.01	%
External Components (Refer to Application section for placement.)					
VREF Bypass Capacitor	(External to GND)	0.1			µF
Bias setting resistor	(Placed between VDD and ISET pins)	1.8	2	2.2	MΩ
ISET Bypass Capacitor	(ISET pin to GND)	0.1			µF
VDD Bypass Capacitor 1	(External to GND)	0.1			µF
VDD Bypass Capacitor 2	(External to GND)	22			µF
XTL1 Load Capacitor	Depends on crystal characteristics;			40	pF
XTL2 Load Capacitor	from pin to GND			20	

ELECTRICAL SPECIFICATIONS (continued)

DC ELECTRICAL CHARACTERISTICS

(TA = -40°C to 85°C, VDD = recommended range unless otherwise noted.)

PARAMETER	CONDITION	MIN	NOM	MAX	UNIT
IDD, Supply Current	ISET Resistor = 2 MΩ				
IDDA, Active	CLK = 11.0592 MHz		8	12	mA
IDD1, Power-down	CLK = 11.0592 MHz			4	mA
IDD2, Power-down	CLK = 19.200 KHz			3	mA
Digital Inputs					
VIH, Input High Voltage					
Reset, XTL1, XTL2		3.0		VDD	V
All other inputs		2.0		VDD	V
VIL, Input Low Voltage		0		0.8	V
IIH, Input High Current	VI = VIH Max			100	µA
IIL, Input Low Current	VI = VIL Min	-200			µA
Reset Pull-down Current	Reset = VDD	1		50	µA
Input Capacitance	All Digital Input Pins			10	pF
Digital Outputs					
VOH, Output High Voltage	IOH MIN = -0.4 mA	2.4		VDD	V
VOL, Output Low Voltage	IO MAX = 1.6 mA			0.4	V
VOL, CLK Output	IO = 3.6 mA			0.6	V
RXD Tri-State Pull-up Curr.	RXD = GND	-1		-50	µA
CMAX, CLK Output	Maximum Capacitive Load			15	pF

ELECTRICAL SPECIFICATIONS (continued)

DYNAMIC CHARACTERISTICS AND TIMING
(TA = -40°C to +85°C, VDD = recommended range unless otherwise noted.)

PARAMETER	CONDITION	MIN	NOM	MAX	UNIT
PSK Modulator					
Carrier Suppression	Measured at TXA	55			dB
Output Amplitude	TX scrambled marks	-11.5	-10.0	-9	dBm0
FSK Mod/Demod					
Output Freq. Error	CLK = 11.0592 MHz	-0.35		+0.35	%
Transmit Level	Transmit Dotting Pattern	-11.5	-10.0	-9	dBm0
Harmonic Distortion in 700-2900 Hz band	THD in the alternate band DPSK or FSK		-60	-50	dB
Output Bias Distortion	Transmit Dotting Pattern in ALB @ RXD		±8		%
Total Output Jitter	Random Input in ALB @ RXD	-15		+15	%
DTMF Generator					
Freq. Accuracy		-0.25		+0.25	%
Output Amplitude	Low Band, DPSK Mode	-10	-9	-8	dBm0
Output Amplitude	High Band, DPSK Mode	-8	-7	-6	dBm0
Twist	High-Band to Low-Band, DPSK Mode	1.0	2.0	3.0	dB
Long Loop Detect	DPSK or FSK	-38		-28	dBm0
Dynamic Range	Refer to Performance Curves		45		dB
Call Progress Detector					
Detect Level	2-Tones in 350-600 Hz band	-34		0	dBm0
Reject Level	2-Tones in 350-600 Hz band			-41	dBm0
Delay Time	-70 dBm0 to -30 dBm0 STEP	27		80	ms
Hold Time	-30 dBm0 to -70 dBm0 STEP	27		80	ms
Hysteresis		2			dB

Note: Parameters expressed in dBm0 refer to the following definition:

0 dB loss in the Transmit path to the line.
2 dB gain in the Receive path from the line.

Refer to the Basic Box Modem diagram in the Applications section for the DAA design.

DYNAMIC CHARACTERISTICS AND TIMING (continued)

PARAMETER	CONDITION	MIN	NOM	MAX	UNIT
Carrier Detect	DPSK or FSK				
Threshold	receive data	-49		-42	dBm0
Delay Time	-70 dBm0 to -30 dBm0 STEP	15		45	ms
Hysteresis	Single tone detected	2	3.0		dB
Hold Time	-30 dBm0 to -70 dBm0 STEP	10		24	ms
Answer Tone Detector					
Detect Level	Not in V.21 mode	-49.5		-42	dBm0
Delay Time	-70 dBm0 to -30 dBm0 STEP	20		45	ms
Hold Time	-30 dBm0 to -70 dBm0 STEP	10		30	ms
Detect Freq. Range		-2.5		+2.5	%
Output Smoothing Filter					
Output load	TXA pin; FSK Single	10			kΩ
	Tone out for THD = -50 db in 0.3 to 3.4 kHz			50	pF
Spurious Freq. Comp.	Frequency = 76.8 kHz			-39	dBm0
	Frequency = 153.6 kHz			-45	dBm0
TXA pin Output Impedance			200	300	Ω
Clock Noise	TXA pin; 76.8 kHz			1.0	mVrms
Carrier VCO					
Capture Range	Originate or Answer	-10		+10	Hz
Capture Time	-10 Hz to +10 Hz Carrier Freq. Change Assum.		40	100	ms
Recovered Clock					
Capture Range	% of frequency center frequency (center at 1200 Hz)	-625		+625	ppm
Data Delay Time	Analog data in at RXA pin to receive data valid at RXD pin		30	50	ms

DYNAMIC CHARACTERISTICS AND TIMING (continued)

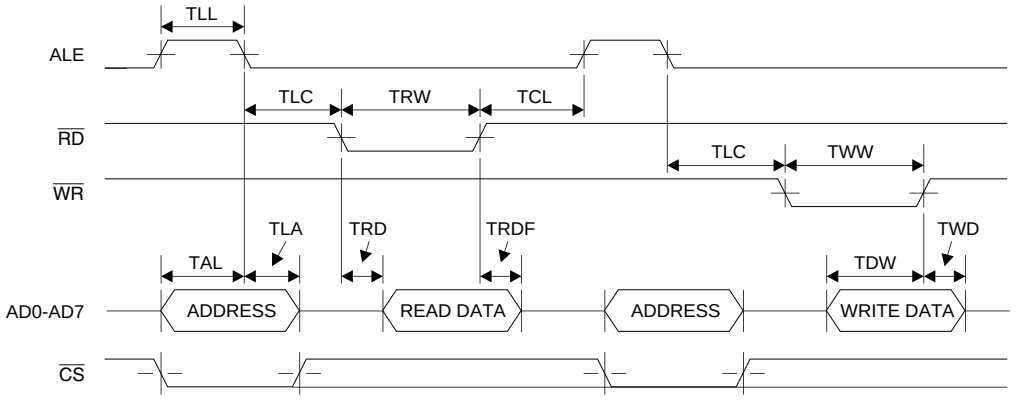
PARAMETER	CONDITION	MIN	NOM	MAX	UNIT
Guard Tone Generator					
Tone Accuracy	550 Hz				
	1800 Hz	-20		+20	Hz
Tone Level	550 Hz	-4.0	-3.0	-2.0	dB
(Below DPSK Output)	1800 Hz	-7.0	-6.0	-5.0	dB
Harmonic Distortion	550 Hz			-50	dB
700 to 2900 Hz	1800 Hz			-60	dB
Timing (Refer to Timing Diagrams)					
TAL	$\overline{CS}$/Addr. setup before ALE Low	30			ns
TLA	$\overline{CS}$/Addr. hold after ALE Low	20			ns
TLC	ALE Low to $\overline{RD}$/$\overline{WR}$ Low	40			ns
TCL	$\overline{RD}$/$\overline{WR}$ Control to ALE High	10			ns
TRD	Data out from $\overline{RD}$ Low	0		140	ns
TLL	ALE width	60			ns
TRDF	Data float after $\overline{RD}$ High	0		200	ns
TRW	$\overline{RD}$ width	200		25000	ns
TWW	$\overline{WR}$ width	140		25000	ns
TDW	Data setup before $\overline{WR}$ High	150			ns
TWD	Data hold after $\overline{WR}$ High	20			ns
TCKD	Data out after EXCLK Low			200	ns
TCKW	$\overline{WR}$ after EXCLK Low	150			ns
TDCK	Data setup before EXCLK Low	150			ns
TAC	Address setup before control*	50			ns
TCA	Address hold after control*	50			ns
TWH	Data Hold after EXCLK	20			

* Control for setup is the falling edge of $\overline{RD}$ or $\overline{WR}$.
Control for hold is the falling edge of $\overline{RD}$ or the rising edge of $\overline{WR}$.

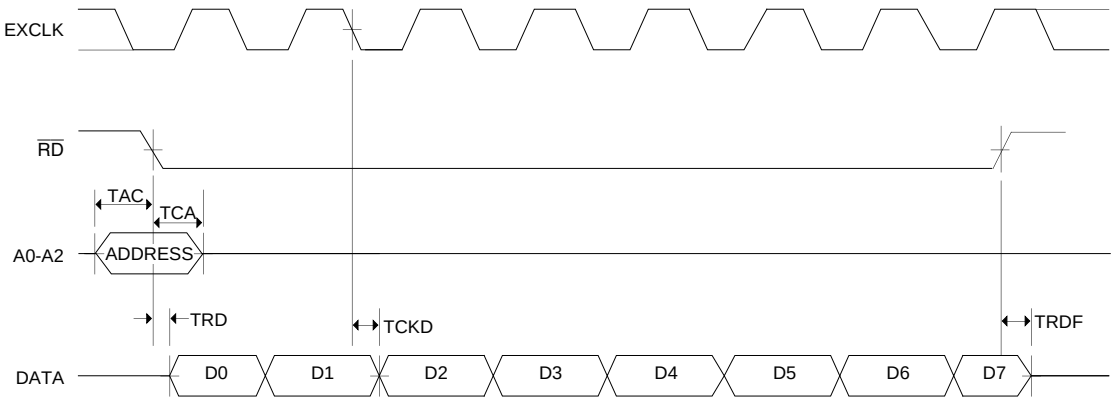
NOTE: Asserting ALE, $\overline{CS}$, and $\overline{RD}$ or $\overline{WR}$ concurrently can cause unintentional register accesses. When using non-8031 compatible processors, care must be taken to prevent this from occurring when designing the interface logic.

TIMING DIAGRAMS

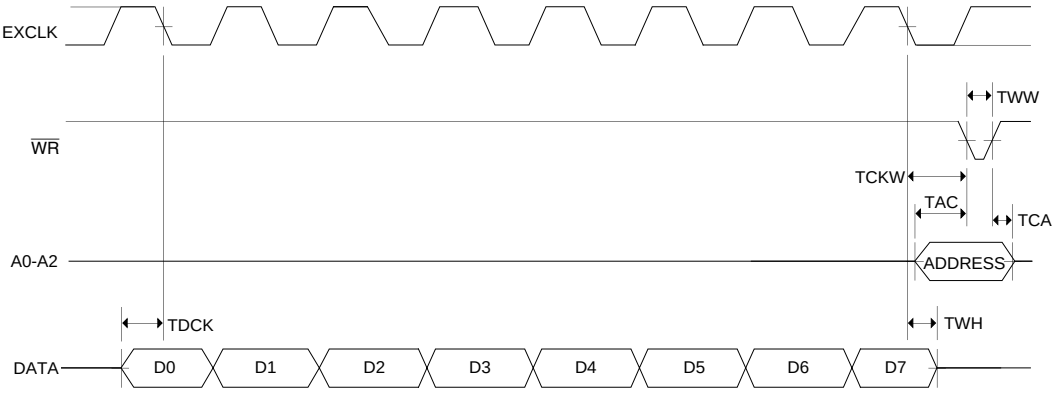
BUS TIMING DIAGRAM (PARALLEL VERSION)



READ TIMING DIAGRAM (SERIAL VERSION)



WRITE TIMING DIAGRAM (SERIAL VERSION)



APPLICATIONS INFORMATION

GENERAL CONSIDERATIONS

Figures 1 and 2 show basic circuit diagrams for K-Series modem integrated circuits. K-Series products are designed to be used in conjunction with a control processor, a UART or RS-232 serial data interface, and a DAA phone line interface to function as a typical intelligent modem. The K-Series ICs interface directly with Intel 8048 and 80C51 microprocessors for control and status monitoring purposes.Two typical DAA arrangements are shown: one for a split ±5 or ±12 volt design and one for a single 5 volt design. These diagrams are for reference only and do not represent production-ready modem designs.

K-Series devices are available with two control interface versions: one for a parallel multiplexed address/data interface, and one for a serial interface. The parallel version is intended for use with 8039/48 or 8031/51 microcontrollers from Intel or many other manufacturers. The serial interface 22-pin version can be used with other microcontrollers or in applications where only a limited number of port lines are available or the application does not lend itself to a multiplexed address/data interface. The parallel versions may also be used in the serial mode, as explained in the data sheet pin description.

In most applications the controller will monitor the serial data for commands from the DTE and the received data for break signals from the far end modem. In this way, commands to the modem are sent over the same line as the transmitted data. In other applications the RS-232 interface handshake lines are used for modem control.

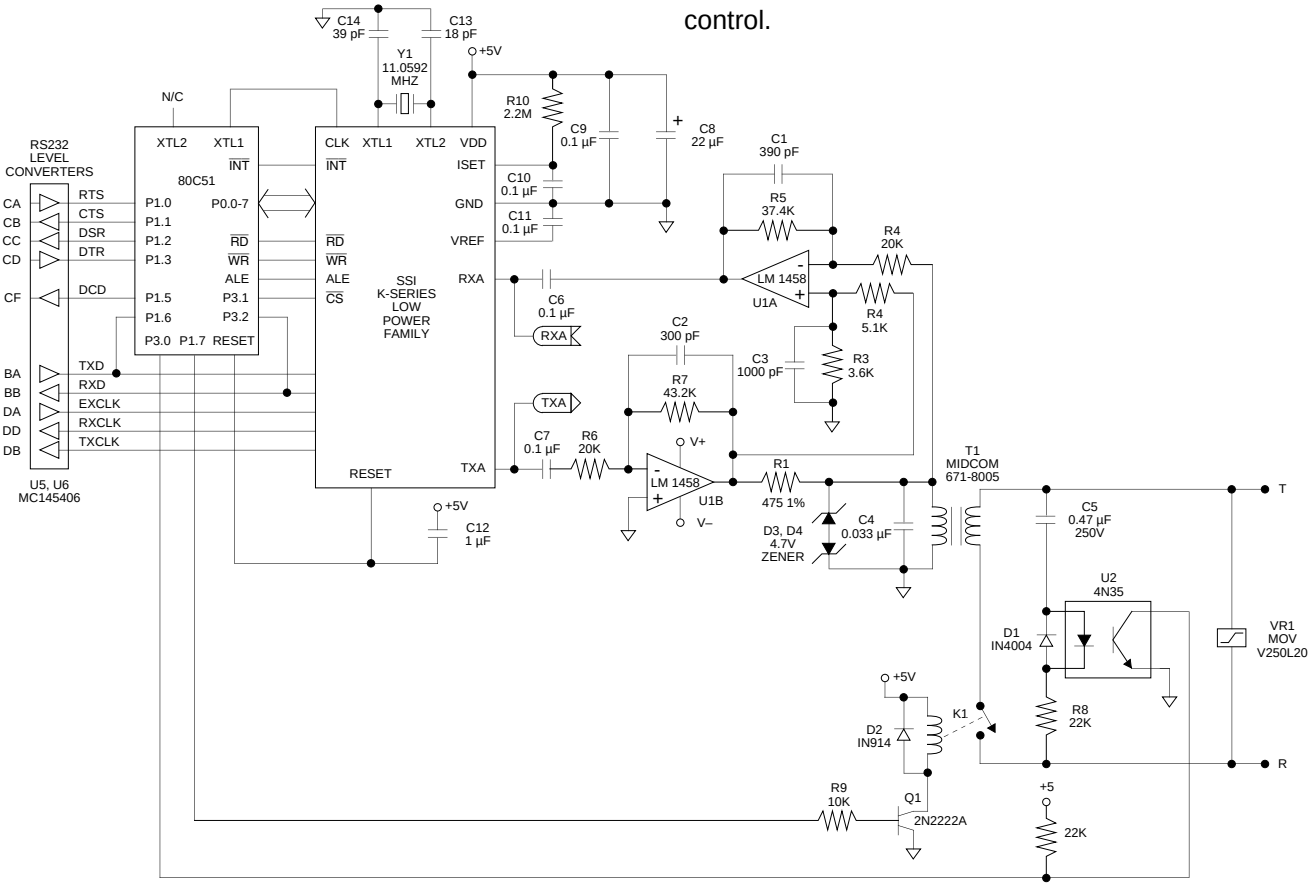


FIGURE 1: Basic Box Modem with Dual-Supply Hybrid

DIRECT ACCESS ARRANGEMENT (DAA)

The telephone line interfaces show two examples of how the "hybrid" may be implemented. The split supply design (Figure 1) is a typical two op-amp hybrid. The receive op-amp serves two purposes. It supplies gain to amplify the receive signal to the proper level for the modem's detectors and demodulator, and it removes the transmitted signal from the receive signal present at the transformer. This is done by supplying a portion of the transmitted signal to the non-inverting input of the receive op-amp at the same amplitude as the signal appearing at the transformer, making the transmit signal common mode.

The single-supply hybrid is more complex than the dual-supply version described above, but its use eliminates the need for a second power supply. This circuit (Figure 2) uses a bridged drive to allow undistorted signals to be sent with a single 5V supply. Because DTMF tones utilize a higher amplitude than data, these signals will clip if a single-ended drive approach is used. The bridged driver uses an extra op-amp (U1A) to invert the signal coming from the gain setting op-amp (U1B) before sending it to the other leg of the transformer. Each op-amp then supplies half the drive signal to the transformer. The receive amplifier (U1C) picks off its signal at the junction of the impedance matching resistor and the transformer. Because the bottom leg of the transformer is being driven in one direction by U1A and the resistor is driven in the opposite direction at the same time by U1B, the junction of the transformer and resistor remains relatively constant and the receive signal is unaffected.

DESIGN CONSIDERATIONS

Silicon Systems' 1-chip modem products include all basic modem functions. This makes these devices adaptable for use in a variety of applications, and as easy to control as conventional digital bus peripherals.

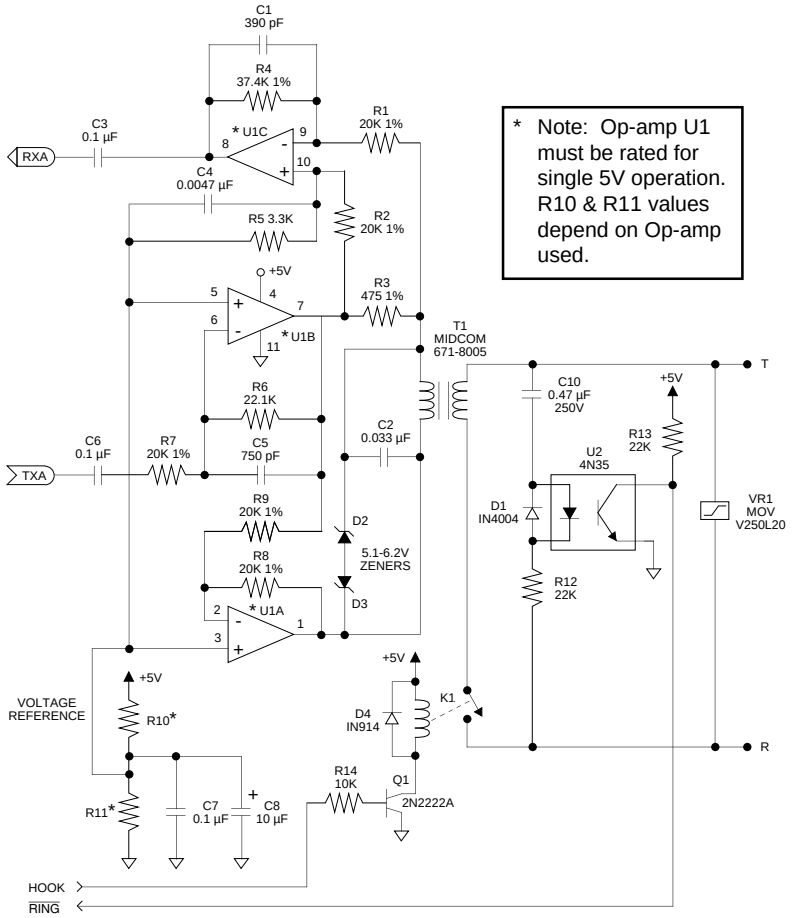


FIGURE 2: Single 5V Hybrid Version

Unlike digital logic circuitry, modem designs must properly contend with precise frequency tolerances and very low level analog signals, to ensure acceptable performance. Using good analog circuit design practices will generally result in a sound design. Following are additional recommendations which should be taken into consideration when starting new designs.

CRYSTAL OSCILLATOR

The K-Series crystal oscillator requires a parallel mode (antiresonant) crystal which operates at 11.0592 MHz. It is important that this frequency be maintained to within ±0.01% accuracy.

In order for a parallel mode crystal to operate correctly and to specification, it must have a load capacitor connected to the junction of each of the crystal and internal inverter connections, terminated to ground. The values of these capacitors depend primarily on the crystal's characteristics, and to a lesser degree on the internal inverter circuit. The values used affect the accuracy and start up characteristics of the oscillator.

LAYOUT CONSIDERATIONS

Good analog/digital design rules must be used to control system noise in order to obtain highest performance in modem designs. The more digital circuitry present on the PC board, the more this attention to noise control is needed. The modem should be treated as a high impedance analog device. A 22 µF electrolytic capacitor in parallel with a 0.1 µF ceramic capacitor between VDD and GND is recommended. Liberal use of ground planes and larger traces on power and ground are also highly favored. High speed digital circuits tend to generate a significant amount of EMI (Electro-Magnetic Interference) which must be minimized in order to meet regulatory agency limitations. To accomplish this, high speed digital devices should be locally bypassed, and the telephone line interface and K-Series device should be located close to each other near the area of the board where the phone line connection is accessed. To avoid problems, power supply and ground traces should be routed separately to the analog and digital functions on the board, and digital signals should not be routed near low level or high impedance analog traces. The analog and digital grounds should only connect at one point near the K-Series device ground pin to avoid ground loops. The K-Series modem IC's should have both high frequency and low frequency bypassing as close to the package as possible.

MODEM PERFORMANCE CHARACTERISTICS

The curves presented here define modem IC performance under a variety of line conditions while inducing disturbances that are typical of those encountered during data transmission on public service telephone lines. Test data was taken using an AEA Electronics' "Autotest I" modem test set and line simulator, operating under computer control. All tests were run full-duplex, using a Concord Data Systems 224 as the reference modem. A 511 pseudo-random-bit pattern was used for each data point. Noise was C-message weighted and all signal-to-noise (S/N) ratios reflect total power measurements similar to the CCITT V.56 measurement specification. The individual tests are defined as follows.

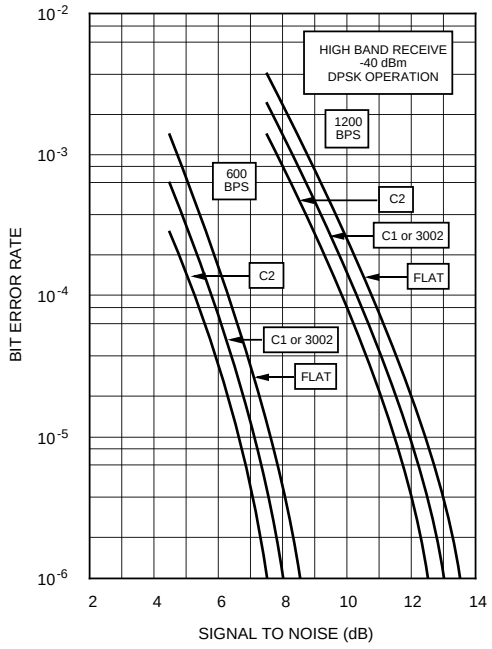
BER vs. S/N

This test measures the ability of the modem to operate over noisy lines with a minimum of data-transfer errors. Since some noise is generated in the best of dial-up lines, the modem must operate with the lowest S/N ratio possible. Better modem performance is indicated by test curves that are closest to the BER axis. A narrow spread between curves representing the four line parameters indicates minimal variation in performance while operating over a range of aberrant operating conditions. Typically, a DPSK modem will exhibit better BER-performance test curves receiving in the low band than in the high band.

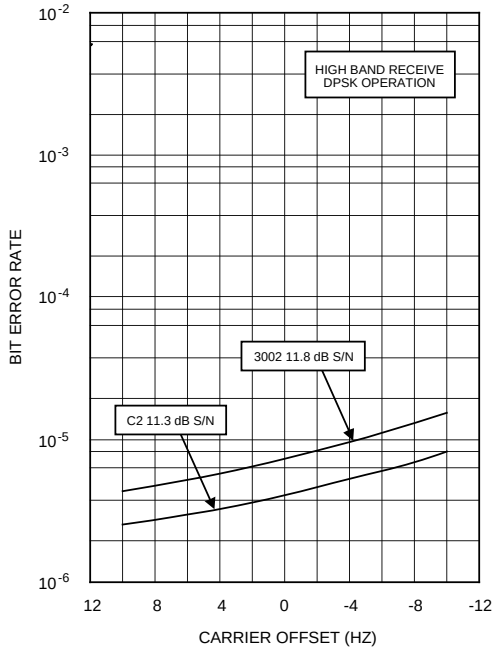
BER vs. Receive Level

This test measures the dynamic range of the modem. Because signal levels vary widely over dial-up lines, the widest possible dynamic range is desirable. The minimum Bell specification calls for 36 dB of dynamic range. S/N ratios are held constant at the indicated values while the receive level is lowered from a very high to very low signal levels. The width of the "bowl" of these curves, taken at the BER point, is the measure of dynamic range.

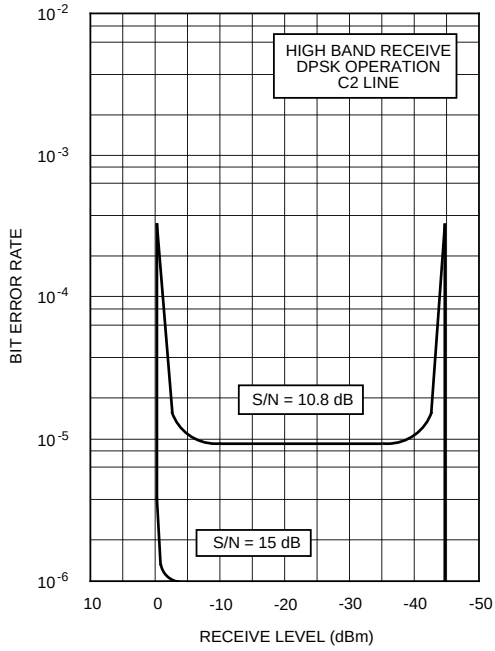
***SSI 73K222AL**
BER vs SIGNALTO NOISE



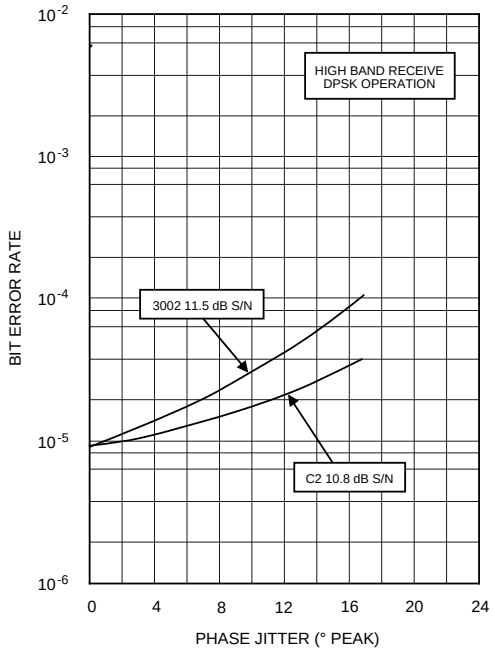
***SSI 73K222AL**
BER vs CARRIER OFFSET



***SSI 73K222AL**
BER vs RECEIVE LEVEL



***SSI 73K222AL**
BER vs PHASE JITTER

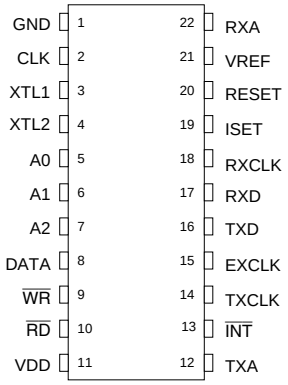


***** = "EQ On" Indicates bit CR1 D4 is set for additional phase equalization.

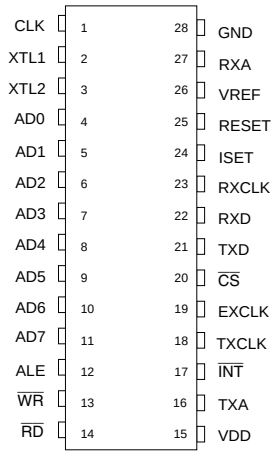
PACKAGE PIN DESIGNATIONS

(Top View)

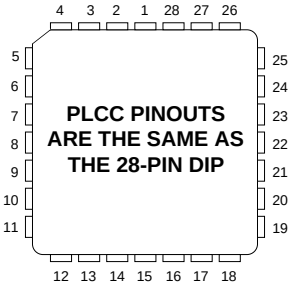
CAUTION: Use handling procedures necessary for a static sensitive component.



400-Mil 22-Pin DIP



600-Mil 28-Pin DIP



28-Pin PLCC

ORDERING INFORMATION

PART DESCRIPTION	ORDER NO.	PKG. MARK
SSI 73K222AL with Parallel Bus Interface 28-Pin Plastic Dual In-Line	73K222AL-IP	73K222AL-IP
28-Pin Plastic Leaded Chip Carrier	73K222AL-IH	73K222AL-IH
SSI 73K222AL with Serial Interface 22-Pin Plastic DIP	73K222ASL-IP	73K222ASL-IP

Silicon Systems, Inc., 14351 Myford Road, Tustin, CA 92680-7022, (714) 573-6000, FAX: (714) 573-6914

SSI 73K222BL

V.22, V.21, Bell 212A, 103 Single-Chip Modem with Integrated Hybrid

Advance Information

March 1996

DESCRIPTION

The SSI 73K222BL is a highly integrated single-chip modem IC which provides the functions needed to construct a CCITT V.22, V.21, Bell 212A and 103, compatible modem, capable of 1200 bit/s full–duplex operation over dial-up lines. The SSI 73K222BL is an enhancement of the SSI 73K222AL single-chip modem which adds the hybrid hook switch control, and driver to the SSI 73K222AL. In Bell 212A mode, the SSI 73K222BL provides the normal Bell 212A and 103 functions and employs a 2225 Hz answer tone. The SSI 73K222BL in V.22 mode produces either 550 or 1800 Hz guard tone, recognizes and generates a 2100 Hz answer tone, and allows 600 bit/s V.22 or 0-300 bit/s V.21 operation. The SSI 73K222BL integrates analog, digital, and switched-capacitor array functions on a single substrate, offering excellent performance and a high level of functional integration in a 28 PLCC, 32 PLCC, or 52-Lead QFP package. The SSI 73K222BL operates from a single +5V supply.

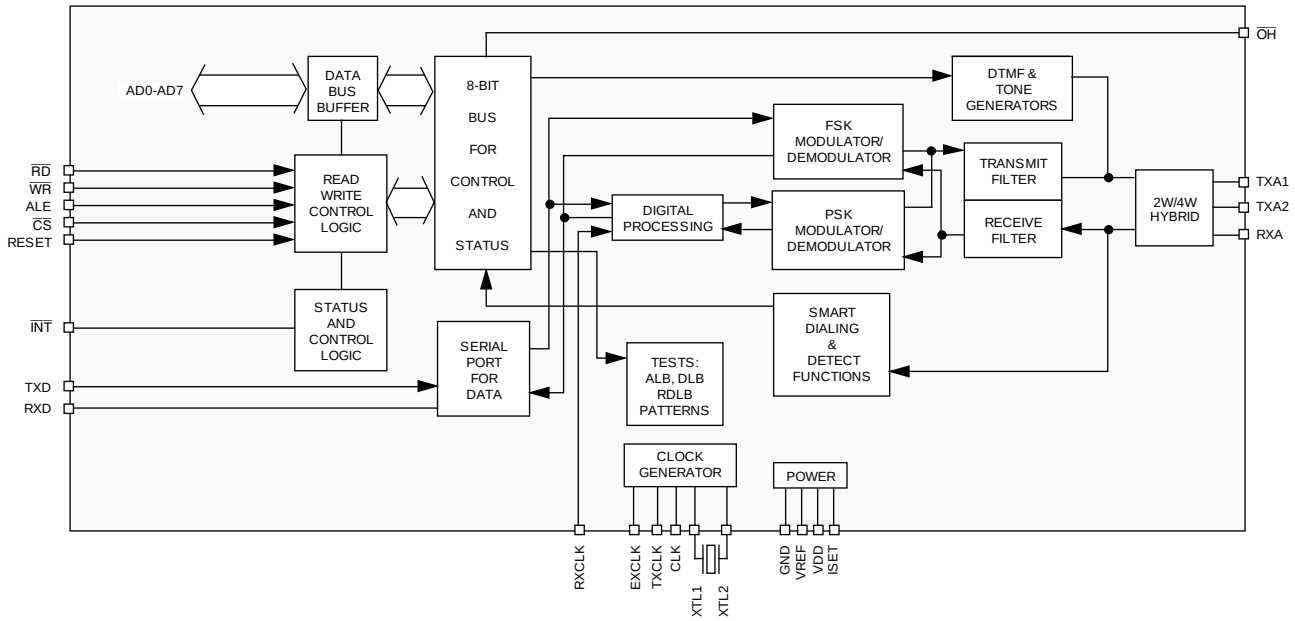
(continued)

FEATURES

- **Includes features of SSI 73K222AL single-chip modem plus Bell 103**
- **One-chip CCITT V.22, V.21, Bell 212A and 103 standard compatible modem data pump**
- **Full-duplex operation at 0-300 bit/s (FSK) or 600 and 1200 bit/s (DPSK)**
- **On chip 2-wire/4-wire hybrid driver and off-hook relay buffer**
- **Interfaces directly with standard microprocessors (8048, 80C51 typical)**
- **Serial or parallel microprocessor bus for control**
- **Serial port for data transfer**
- **Both synchronous and asynchronous modes of operation including V.22 extended overspeed**

(continued)

BLOCK DIAGRAM



DESCRIPTION (continued)

The SSI 73K222BL includes the DPSK and FSK modulator/demodulator functions, call progress and handshake tone monitor and a tone generator capable of tones required for European applications. This device supports V.22 (except mode v) and V. 21 modes of operation, allowing both synchronous and asynchronous communications. Test features such as analog loop, digital loop, and remote digital loopback are supported. Internal pattern generators are also included for self-testing. The SSI 73K222BL is designed to appear to the systems designer as a microprocessor peripheral, and will easily interface with popular one-chip microprocessors (80C51 typical) for control of modem functions through its 8-bit multiplexed address/data bus or serial control bus. An ALE control line simplifies address demultiplexing. Data communications occurs through a separate serial port only.

The SSI 73K222BL is ideal for use in either free standing or integral system modem products where full-duplex 1200 bit/s data communications over the 2-wire switched telephone network is desired. Its high functionality, low power consumption and efficient packaging simplify design requirements and increase system reliability. A complete modem requires only the addition of the phone line interface, a control microprocessor, and RS-232 level converter for a typical system. The SSI 73K222BL is part of Silicon Systems' K-Series family of single-chip modem products. These devices allow systems to be configured for higher speeds and Bell or CCITT operation with only a single component change.

FEATURES (continued)

- Call progress, carrier, precise answer tone (2100 or 2225 Hz), and long loop detectors
- DTMF, and 550 or 1800 Hz guard tone generators
- Test modes available: ALB, DL, RDL, Mark, Space, Alternating bit patterns
- Precise automatic gain control allows 45 dB dynamic range
- CMOS technology for low power consumption using 60 mW @ 5V
- Single +5 volt supply

FUNCTIONAL DESCRIPTION

HYBRID AND RELAY DRIVER

To make designs more cost effective and space efficient, the SSI 73K222BL includes the 2-wire to 4-wire hybrid with sufficient drive to interface directly to the telecom coupling transformers. In addition, an off hook relay driver with 40 mA drive capability is also included to allow use of commonly available mechanical telecom relays.

ASYNCHRONOUS MODE

Data transmission for the DPSK mode requires that data ultimately be transmitted in a synchronous fashion. The SSI 73K222BL includes ASYNC/SYNC and SYNC/ASYNC converters which delete or insert stop bits in order to transmit data within a±0.01% rate. In asynchronous mode the serial data comes from the TXD pin into the ASYNC/SYNC converter. The ASYNC/SYNC converter accepts the data provided on the TXD pin which normally must be 1200 or 600 bit/s +1.0%, -2.5%. The converter will then insert or delete stop bits in order to output a signal which is 1200 or 600 bit/s ± 0.01% (± 0.01% is required synchronous data rate accuracy).

The serial data stream from the ASYNC/SYNC converter is passed through the data scrambler and onto the analog modulator. The data scrambler can be bypassed under processor control when unscrambled data must be transmitted. The ASYNC/SYNC converter and the data scrambler are bypassed in all FSK modes. If serial input data contains a break signal through one character (including start and stop bits) the break will be extended to at least 2 • N + 3 bits long (where N is the number of transmitted bits/character).

Serial data from the demodulator is passed first through the data descrambler and then through the SYNC/ASYNC converter. The SYNC/ASYNC converter will re-insert any deleted stop bits and transmit output data at an intra-character rate (bit-to-bit timing) of no greater than 1219 bit/s. An incoming break signal (low through two characters) will be passed through without incorrectly inserting a stop bit.

The SYNC/ASYNC converter also has an extended overspeed mode which allows selection of an overspeed range of either +1% or +2.3%. In the extended overspeed mode, stop bits are output at 7/8 the normal width.

SYNCHRONOUS MODE

The CCITT V.22 standard defines synchronous operation at 600 and 1200 bit/s. The Bell 212A standard defines synchronous operation only at 1200 bit/s. Operation is similar to that of the asynchronous mode except that data must be synchronized to a provided clock and no variation in data transfer rate is allowable. Serial input data appearing at TXD must be valid on the rising edge of TXCLK.

TXCLK is an internally derived signal in internal mode and is connected internally to the RXCLK pin in slave mode. Receive data at the RXD pin is clocked out on the falling edge of RXCLK. The ASYNCH/SYNCH converter is bypassed when synchronous mode is selected and data is transmitted out at the same rate as it is input.

DPSK MODULATOR/DEMODULATOR

The SSI 73K222BL modulates a serial bit stream into di-bit pairs that are represented by four possible phase shifts as prescribed by the Bell 212A or V.22 standards. The baseband signal is then filtered to reduce intersymbol interference on the bandlimited 2-wire telephone line. Transmission occurs using either a 1200 Hz (originate mode) or 2400 Hz carrier (answer mode). Demodulation is the reverse of the modulation process, with the incoming analog signal eventually decoded into di-bits and converted back to a serial bit stream. The demodulator also recovers the clock which was encoded into the analog signal during modulation. Demodulation occurs using either a 1200 Hz carrier (answer mode or ALB originate mode) or a 2400 Hz carrier (originate mode or ALB answer mode). The SSI 73K222BL uses a phase locked loop coherent demodulation technique for optimum receiver performance.

FSK MODULATOR/DEMODULATOR

The FSK modulator produces a frequency modulated analog output signal using two discrete frequencies to represent the binary data. In Bell 103, the standard frequencies of 1270 and 1070 Hz (originate, mark and space) or 2225 and 2025 Hz (answer, mark and space) are used. V.21 mode uses 980 and 1180 Hz (originate, mark and space), or 1650 and 1850Hz (answer, mark and space). Demodulation involves detecting the received frequencies and decoding them into the appropriate binary value. The rate converter and scrambler/descrambler are bypassed in the 103 or V.21 modes.

FUNCTIONAL DESCRIPTION (continued)

PASSBAND FILTERS AND EQUALIZERS

High and low band filters are included to shape the amplitude and phase response of the transmit and receive signals and provide compromise delay equalization and rejection of out-of-band signals in the receive channel. Amplitude and phase equalization are necessary to compensate for distortion of the transmission line and to reduce intersymbol interference in the bandlimited receive signal. The transmit signal filtering approximates a 75% square root of raised Cosine frequency response characteristic.

AGC

The automatic gain control maintains a signal level at the input to the demodulators which is constant to within 1 dB. It corrects quickly for increases in signal which would cause clipping and provides a total receiver dynamic range of > 45 dB.

PARALLEL BUS INTERFACE

Four 8-bit registers are provided for control, option select and status monitoring. These registers are addressed with the AD0, AD1, and AD2 multiplexed address lines (latched by ALE) and appear to a control microprocessor as four consecutive memory locations. Two control registers and the tone register are read/write memory. The detect register is read only and cannot be modified except by modem response to monitored parameters.

SERIAL COMMAND INTERFACE

The serial command interface allows access to the SSI 73K222BL control and status registers via a serial command port (28-Pin version). In this mode the A0, A1 and A2 lines provide register addresses for data passed through the data pin under control of the $\overline{RD}$ and $\overline{WR}$ lines. A read operation is initiated when the $\overline{RD}$ line is taken low. The first bit is available after $\overline{RD}$ is brought low and the next seven cycles of EXCLK will then transfer out seven bits of the selected address LSB first. A write takes place by shifting in eight bits of data LSB first for eight consecutive cycles of EXCLK. $\overline{WR}$ is then pulsed low and data transferred into the addressed register occurs on the rising edge of $\overline{WR}$. This interface mode is also supported in the 32-Pin packages. See serial control interface pin description.

SPECIAL DETECT CIRCUITRY

The special detect circuitry monitors the received analog signal to determine status or presence of carrier, call-progress tones, answer tone and weak received signal (long loop condition). An unscrambled mark request signal is also detected when the received data out of the DPSK demodulator before the descrambler has been high for 165.5 ms ± 6.5 ms minimum. The appropriate detect register bit is set when one of these conditions changes and an interrupt is generated for all purposes except long loop. The interrupts are disabled (masked) when the enable interrupt bit is set to 0.

DTMF GENERATOR

The DTMF generator will output one of 16 standard tone pairs determined by a 4-bit binary value and TX DTMF mode bit previously loaded into the tone register. Tone generation is initiated when the DTMF mode is selected using the tone register and the transmit enable (CR0 bit D1) is changed from 0 to 1.

REGISTER DESCRIPTIONS

Four 8-bit internal registers are accessible for control and status monitoring. The registers are accessed in read or write operations by addressing the A0, A1 and A2 address lines in serial mode, or the AD0, AD1 and AD2 lines in parallel mode. In parallel mode the address lines are latched by ALE. Register CR0 controls the method by which data is transferred over the phone line. CR1 controls the interface between the microprocessor and the SSI 73K222BL internal state. DR is the Detect Register which provides an indication of monitored modem status conditions. TR, the Tone Control Register, controls the DTMF generator, answer and guard tones and RXD output gate used in the modem initial connect sequence. All registers are read/write except for DR which is read only. Register control and status bits are identified below:

REGISTER BIT SUMMARY

	ADDRESS	DATA BIT NUMBER							
REGISTER	AD2 - AD0	D7	D6	D5	D4	D3	D2	D1	D0
CONTROL REGISTER 0 CR0	000	MODULATION OPTION	0	TRANSMIT MODE 3	TRANSMIT MODE 2	TRANSMIT MODE 1	TRANSMIT MODE 0	TRANSMIT ENABLE	ANSWER/ ORIGINATE
CONTROL REGISTER 1 CR1	001	TRANSMIT PATTERN 1	TRANSMIT PATTERN 0	ENABLE DETECT INTERRUPT	BYPASS SCRAMBLER	CLK CONTROL	RESET	TEST MODE 1	TEST MODE 0
DETECT REGISTER DR	010	X	X	RECEIVE DATA	UNSCR. MARKS	CARRIER DETECT	ANSWER TONE	CALL PROGRESS	LONG LOOP
TONE CONTROL REGISTER TR	011	RXD OUTPUT CONTROL	TRANSMIT GUARD TONE	TRANSMIT ANSWER TONE	TRANSMIT DTMF	DTMF3	DTMF2	DTMF1/ OVERSPEED	DTMF0/ GUARD/ ANS TONE
CONTROL REGISTER 2 CR2	100	X	X	X	THESE REGISTER LOCATIONS ARE RESERVED FOR				X
CONTROL REGISTER 3 CR3	101	X	X	X	USE WITH OTHER K-SERIES FAMILY MEMBERS				X
ID REGISTER ID	110	1	0	X	$\overline{OH}$	X	X	X	X

NOTE: When a register containing reserved control bits is written into, the reserved bits must be programmed as 0's.

X = Undefined, mask in software

REGISTER DESCRIPTION (continued)

REGISTER ADDRESS TABLE

REGISTER	ADDRESS AD2 - AD0	DATA BIT NUMBER D7	D6	D5	D4	D3	D2	D1	D0
CONTROL REGISTER 0 CR0	000	MODULATION OPTION	0	TRANSMIT MODE 3	TRANSMIT MODE 2	TRANSMIT MODE 1	TRANSMIT MODE 0	TRANSMIT ENABLE	ORIGINATE/ ANSWER
		0 = 1200 BIT/S DPSK 1 = 600 BIT/S DPSK 0 = BELL 103 FSK 1 = V.21 FSK		0000 = PWR DOWN 0001 = INT SYNCH 0010 = EXT SYNCH 0011 = SLAVE SYNCH 0100 = ASYNCH 8 BITS/CHAR 0101 = ASYNCH 9 BITS/CHAR 0110 = ASYNCH 10 BITS/CHAR 0111 = ASYNCH 11 BITS/CHAR 1100 = FSK				0 = DISABLE TXA OUTPUT 1 = ENABLE TXA OUTPUT	0 = ANSWER 1 = ORIGINATE
CONTROL REGISTER 1 CR1	001	TRANSMIT PATTERN 1	TRANSMIT PATTERN 0	ENABLE DETECT INTERRUPT	BYPASS SCRAMBLER	CLK CONTROL	RESET	TEST MODE 1	TEST MODE 0
		00 = TX DATA 01 = TX ALTERNATE 10 = TX MARK 11 = TX SPACE		0 = DISABLE 1 = ENABLE	0 = NORMAL 1 = BYPASS SCRAMBLER	0 = XTAL 1 = 16 X DATA RATE OUTPUT AT CLK PIN IN DPSK MODE ONLY	0 = NORMAL 1 = RESET	00 = NORMAL 01 = ANALOG LOOPBACK 10 = REMOTE DIGITAL LOOPBACK 11 = LOCAL DIGITAL LOOPBACK	
DETECT REGISTER DR	010	X	X	RECEIVE DATA	UNSCR. MARKS	CARRIER DETECT	ANSWER TONE	CALL PROGRESS	LONG LOOP
				OUTPUTS RECEIVED DATA STREAM	0 = CONDITION NOT DETECTED 1 = CONDITION DETECTED				
TONE CONTROL REGISTER TR	011	RXD OUTPUT CONTROL	TRANSMIT GUARD/ TONE	TRANSMIT ANSWER TONE	TRANSMIT DTMF	DTMF3	DTMF2	DTMF1/ OVERSPEED	DTMF0/ GUARD/ ANSWER/ TONE
		RXD PIN 0 = NORMAL 1 =TRI ST ATE	0 = OFF 1 = ON	0 = OFF 1 = ON	0 = DATA 1 = TX DTMF	4 BIT CODE FOR 1 OF 16 DUAL TONE COMBINATIONS			0 = 2225 Hz A.T. 1800 Hz G.T. 1 = 2100 Hz A.T. 500 Hz G.T.
ID REGISTER 10	110	1	0	X	OH	X	X	X	X
		X = Undefined, mask in software			0 = OH Relay driver open 1 = OH Open drain driver pulling low				

CONTROL REGISTER 0

	D7	D6	D5	D4	D3	D2	D1	D0
CR0 000	MODUL. OPTION	0	TRANSMIT MODE 3	TRANSMIT MODE 2	TRANSMIT MODE 1	TRANSMIT MODE 0	TRANSMIT ENABLE	ANSWER/ ORIGINATE

BIT NO.	NAME	CONDITION	DESCRIPTION
D0	Answer/ Originate	0	Selects answer mode (transmit in high band, receive in low band).
		1	Selects originate mode (transmit in low band, receive in high band).
D1	Transmit Enable	0	Disables transmit output at TXA.
		1	Enables transmit output at TXA. Note: TX Enable must be set to 1 to allow Answer Tone and DTMF Transmission.
D5, D4,D3, D2	Transmit Mode	D5 D4 D3 D2 0 0 0 0	Selects power-down mode. All functions disabled except digital interface.
		0 0 0 1	Internal synchronous mode. In this mode TXCLK is an internally derived 1200 Hz signal. Serial input data appearing at TXD must be valid on the rising edge of TXCLK. Receive data is clocked out of RXD on the falling edge of RXCLK.
		0 0 1 0	External synchronous mode. Operation is identical to internal synchronous, but TXCLK is connected internally to EXCLK pin, and a 1200 Hz ± 0.01% clock must be supplied externally.
		0 0 1 1	Slave synchronous mode. Same operation as other synchronous modes. TXCLK is connected internally to the RXCLK pin in this mode.
		0 1 0 0	Selects PSK asynchronous mode - 8 bits/character (1 start bit, 6 data bits, 1 stop bit).
		0 1 0 1	Selects PSK asynchronous mode - 9 bits/character (1 start bit, 7 data bits, 1 stop bit).
		0 1 1 0	Selects PSK asynchronous mode - 10 bits/character (1 start bit, 8 data bits, 1 stop bit).
		0 1 1 1	Selects PSK asynchronous mode - 11 bits/character (1 start bit, 8 data bits, Parity and 1 or 2 stop bits).
		1 1 0 0	Selects FSK operation.
D6		0	Not used; must be written as a “0.”

CONTROL REGISTER 0 (continued)

	D7	D6	D5	D4	D3	D2	D1	D0
CR0 000	MODUL. OPTION	0	TRANSMIT MODE 3	TRANSMIT MODE 2	TRANSMIT MODE 1	TRANSMIT MODE 0	TRANSMIT ENABLE	ANSWER/ ORIGINATE

BIT NO.	NAME	CONDITION	DESCRIPTION
D7	Modulation Option	D7 D5 D4	Selects:
		0 0 X	DPSK mode at 1200 bit/s.
		1 0 X	DPSK mode at 600 bit/s.
		0 1 1	FSK Bell 103 mode.
		1 1 1	FSK CCITT V.21 mode.
			X = Don't care

CONTROL REGISTER 1

	D7	D6	D5	D4	D3	D2	D1	D0
CR1 001	TRANSMIT PATTERN 1	TRANSMIT PATTERN 0	ENABLE DETECT INTER.	BYPASS SCRAMB	CLK CONTROL	RESET	TEST MODE 1	TEST MODE 0

BIT NO.	NAME	CONDITION	DESCRIPTION
D1, D0	Test Mode	D1 D0	Selects normal operating mode.
		0 0	
		0 1	Analog loopback mode. Loops the transmitted analog signal back to the receiver, and causes the receiver to use the same center frequency as the transmitter. To squelch the TXA pin, transmit enable must be forced low.
		1 0	Selects remote digital loopback. Received data is looped back to transmit data internally, and RXD is forced to a mark. Data on TXD is ignored.
		1 1	Selects local digital loopback. Internally loops TXD back to RXD and continues to transmit carrier from TXA pin.
D2	Reset	0	Selects normal operation.
		1	Resets modem to power-down state. All control register bits (CR0, CR1, Tone) are reset to zero. The output of the CLK pin will be set to the crystal frequency.
D3	CLK Control (Clock Control)	0	Selects 11.0592 MHz crystal echo output at CLK pin.
		1	Selects 16 • the data rate, output at CLK pin in DPSK modes only.

CONTROL REGISTER 1 (continued)

	D7	D6	D5	D4	D3	D2	D1	D0
CR1 001	TRANSMIT PATTERN 1	TRANSMIT PATTERN 0	ENABLE DETECT INTER.	BYPASS SCRAMB.	CLK CONTROL	RESET	TEST MODE 1	TEST MODE 0

BIT NO.	NAME	CONDITION	DESCRIPTION
D4	Bypass Scrambler	0	Selects normal operation. DPSK data is passed through scrambler.
		1	Selects Scrambler Bypass. Bypass DPSK data is routed around scrambler in the transmit path.
D5	Enable Detect	0	Disables interrupt at $\overline{INT}$ pin.
		1	Enables $\overline{INT}$ output. An interrupts will be generated with a change in status of DR bits D1-D4. The answer tone and call progress detect interrupts are masked when the TX enable bit is set. Carrier detect is masked when TX DTMF is activated. All interrupts will be disabled if the device is in power-down mode.
D7, D6	Transmit Pattern	D7 D6	Selects normal data transmission as controlled by the state of the TXD pin.
		0 0	
		0 1	Selects an alternating mark/space transmit pattern for modem testing.
		1 0	Selects a constant mark transmit pattern.
		1 1	Selects a constant space transmit pattern.

DETECT REGISTER

	D7	D6	D5	D4	D3	D2	D1	D0
DR 010	X	X	RECEIVE DATA	UNSCR. MARK	CARR. DETECT	ANSWER TONE	CALL PROG.	LONG LOOP

BIT NO.	NAME	CONDITION	DESCRIPTION
D0	Long Loop	0	Indicates normal received signal.
		1	Indicates low received signal level.
D1	Call Progress Detect	0	No call progress tone detected.
		1	Indicates presence of call progress tones. The call progress detection circuitry is activated by energy in the 350 to 620 Hz call progress band.

DETECT REGISTER (continued)

	D7	D6	D5	D4	D3	D2	D1	D0
DR 010	X	X	RECEIVE DATA	UNSCR. MARK	CARR. DETECT	ANSWER TONE	CALL PROG.	LONG LOOP

BIT NO.	NAME	CONDITION	DESCRIPTION
D2	Answer Tone Detect	0	No answer tone detected.
		1	Indicates detection of 2225 Hz answer tone in Bell mode or 2100 Hz in CCITT mode. The device must be in originate mode for detection of answer tone. For CCITT answer tone detection, bit D0 of the Tone Register must be set to a 1.
D3	Carrier Detect	0	No carrier detected in the receive channel.
		1	Indicates carrier has been detected in the receive channel.
D4	Unscrambled Mark Detect	0	No unscrambled mark.
		1	Indicates detection of unscrambled marks in the received data. A valid indication requires that unscrambled marks be received for > 165.5 ± 6.5 ms.
D5	Receive Data		Continuously outputs the received data stream. This data is the same as that output on the RXD pin, but it is not disabled when RXD is tri-stated.
D6, D7	Not Used	Undefined	Not used. Mask in software.

TONE REGISTER

	D7	D6	D5	D4	D3	D2	D1	D0
TR 011	RXD OUTPUT CONTR.	TRANSMIT GUARD TONE	TRANSMIT ANSWER TONE	TRANSMIT DTMF	DTMF 3	DTMF 2	DTMF 1/ OVER-SPEED	DTMF 0/ ANSWER/ GUARD

BIT NO.	NAME	CONDITION	DESCRIPTION
D0	DTMF 0/ Answer/ Guard Tone	D6 D5 D4 D0	D0 interacts with bits D6, D5, and D4 as shown.
		X X 1 X	Transmit DTMF tones.
		X 0 0 0	Detects 2225 Hz in originate mode.
		X 1 0 0	Transmits 2225 Hz in answer mode (Bell).
		X 0 0 1	Detects 2100 Hz in originate mode.
		X 1 0 1	Transmits 2100 Hz in answer mode (CCITT).
		1 0 0 0	Select 1800 Hz guard tone.
		1 0 0 1	Select 550 Hz guard tone.
D1	DTMF 1/ Overspeed	D4 D1	D1 interacts with D4 as shown.
		0 0	Asynchronous DPSK +1.0% -2.5%.
		0 1	Asynchronous DPSK +2.3% -2.5%.

TONE REGISTER (continued)

	D7	D6	D5	D4	D3	D2	D1	D0
TR 011	RXD OUTPUT CONTR.	TRANSMIT GUARD TONE	TRANSMIT ANSWER TONE	TRANSMIT DTMF	DTMF 3	DTMF 2	DTMF 1/ OVER-SPEED	DTMF 0/ ANSWER/ GUARD

BIT NO.	NAME	CONDITION	DESCRIPTION
D3, D2, D1, D0	DTMF 3, 2, 1, 0	D3 D2 D1 D0 0 0 0 0 1 1 1 1	Programs 1 of 16 DTMF tone pairs that will be transmitted when TX DTMF and TX enable bit (CR0, bit D1) are set. Tone encoding is shown below:
D4	Transmit DTMF	0	Disable DTMF.
		1	Activates DTMF. The selected DTMF tones are transmitted continuously when this bit is high. TX DTMF overrides all other transmit functions.
D5	Transmit Answer Tone	D5 D4 D0	D5 interacts with bits D4 and D0 as shown.
		0 0 X	Disables answer tone generator.
		1 0 0	Enables answer tone generator. A 2225 Hz answer tone will be transmitted continuously when the transmit enable bit is set in CR0. The device must be in answer mode.
		1 0 1	Likewise a 2100 Hz answer tone will be transmitted.

KEYBOARD EQUIVALENT	DTMF CODE D3 D2 D1 D0	TONES LOW HIGH
1	0 0 0 1	697 1209
2	0 0 1 0	697 1336
3	0 0 1 1	697 1477
4	0 1 0 0	770 1209
5	0 1 0 1	770 1336
6	0 1 1 0	770 1477
7	0 1 1 1	852 1209
8	1 0 0 0	852 1336
9	1 0 0 1	852 1477
0	1 0 1 0	941 1336
*	1 0 1 1	941 1209
#	1 1 0 0	941 1477
A	1 1 0 1	697 1633
B	1 1 1 0	770 1633
C	1 1 1 1	852 1633
D	0 0 0 0	941 1633

TONE REGISTER (continued)

	D7	D6	D5	D4	D3	D2	D1	D0
TR 011	RXD OUTPUT CONTR.	TRANSMIT GUARD TONE	TRANSMIT ANSWER TONE	TRANSMIT DTMF	DTMF 3	DTMF 2	DTMF 1/ OVER-SPEED	DTMF 0/ ANSWER/ GUARD

BIT NO.	NAME	CONDITION	DESCRIPTION
D6	Transmit Guard Tone	0	Disables guard tone generator.
		1	Enables guard tone generator (See D0 for selection of guard tones).
D7	RXD Output Control	0	Enables RXD pin. Receive data will be output on RXD.
		1	Disables RXD pin. The RXD pin reverts to a high impedance with internal weak pull-up resistor.

ID REGISTER

	D7	D6	D5	D4	D3	D2	D1	D0
ID 110	1	0	X	OH	X	X	X	X

BIT NO.	NAME	CONDITION	DESCRIPTION
D7, D6	DEVICE ID	D7 D6 1 0	Indicates device type.
D3	OH	0	Relay driver open.
		1	Open drain driver pulling low.
D5, D3-D1	Not Used	NA	Mask in firmware.

PIN DESCRIPTION

POWER

NAME	28-PIN	32-PIN	TYPE	DESCRIPTION
GND	1	1	I	System Ground
VDD	14	16	I	Power supply input, 5V ±10% (SSI 73K222BL). Bypass with 0.1 and 22 μF capacitors to GND.
VREF	27	31	O	An internally generated reference voltage. Bypass with 0.1 μF capacitor to ground.
ISET	24	28	I	Chip current reference. Sets bias current for op-amps. The chip current is set by connecting this pin to VDD through a 2 MΩ resistor. ISET should be bypassed to GND with a 0.1 μF capacitor.

PARALLEL MICROPROCESSOR INTERFACE

ALE	-	13	I	Address latch enable. The falling edge of ALE latches the address on AD0-AD2 and the chip select on $\overline{CS}$.
AD0-AD7	-	5-12	I/O	Address/data bus. These bi-directional tri-state multi-plexed lines carry information to and from the internal registers.
$\overline{CS}$	-	23	I	Chip select. A low on this pin during the falling edge of ALE allows a read cycle or a write cycle to occur. AD0-AD7 will not be driven and no registers will be written if $\overline{CS}$ (latched) is not active. The state of $\overline{CS}$ is latched on the falling edge of ALE.
CLK	2	2	O	Output clock. This pin is selectable under processor control to be either the crystal frequency (for use as a processor clock) or 16 • the data rate for use as a baud rate clock in DPSK modes only. The pin defaults to the crystal frequency on reset.
$\overline{INT}$	17	19	O	Interrupt. This open drain output signal is used to inform the processor that a detect flag has occurred. The processor must then read the detect register to determine which detect triggered the interrupt. $\overline{INT}$ will stay low until the processor reads the detect register or does a full reset.
$\overline{RD}$	-	15	I	Read. A low requests a read of the SSI 73K222BL internal registers. Data cannot be output unless both $\overline{RD}$ and the latched $\overline{CS}$ are active or low.
RESET	26	30	I	Reset. An active high signal on this pin will put the chip into an inactive state. All control register bits (CR0, CR1, Tone) will be reset. The output of the CLK pin will be set to the crystal frequency. An internal pull-down resistor permits power-on-reset using a capacitor to VDD.

PARALLEL MICROPROCESSOR INTERFACE (continued)

NAME	28-PIN	32-PIN	TYPE	DESCRIPTION
$\overline{WR}$	-	14	I	Write. A low on this informs the SSI 73K222BL that data is available on AD0-AD7 for writing into an internal register. Data is latched on the rising edge of $\overline{WR}$. No data is written unless both $\overline{WR}$ and the latched $\overline{CS}$ are low.

SERIAL MICROPROCESSOR INTERFACE

A0-A2	5-7	5-7	I	Register Address Selection. These lines carry register addresses and should be valid during any read or write operation.
DATA	9	12	I/O	Serial Control Data. Data for a read/write operation is clocked in or out on the falling edge of the EXCLK pin. The direction of data flow is controlled by the $\overline{RD}$ pin. $\overline{RD}$ low outputs data. $\overline{RD}$ high inputs data.
$\overline{RD}$	13	15	I	Read. A low on this input informs the SSI 73K222BL that data or status information is being read by the processor. The falling edge of the $\overline{RD}$ signal will initiate a read from the addressed register. The $\overline{RD}$ signal must continue for eight falling edges of EXCLK in order to read all eight bits of the referenced register. Read data is provided LSB first. Data will not be output unless the $\overline{RD}$ signal is active.
$\overline{WR}$	12	14	I	Write. A low on this input informs the SSI 73K222BL that data or status information has been shifted in through the DATA pin and is available for writing to an internal register. The normal procedure for a write is to shift in data LSB first on the DATA pin for eight consecutive falling edges of EXCLK and then to pulse $\overline{WR}$ low. Data is written on the rising edge of $\overline{WR}$.

NOTE: In the serial, 28-Pin version, the pins AD0-AD7, ALE and $\overline{CS}$ are removed and replaced with the pins; A0, A1, A2, DATA, and an unconnected pin. Also, the $\overline{RD}$ and $\overline{WR}$ controls are used differently.

The serial control mode is provided in the parallel control version by tying ALE high and $\overline{CS}$ low. In this configuration AD7 becomes DATA and AD0, AD1 and AD2 become A0, A1 and A2, respectively.

DTE USER

NAME	28-PIN	32-PIN	TYPE	DESCRIPTION
EXCLK	19	22	I	External Clock. This signal is used in synchronous transmission when the external timing option has been selected. In the external timing mode the rising edge of EXCLK is used to strobe synchronous DPSK transmit data applied to on the TXD pin. Also used for serial control interface.
RXCLK	22	26	O	Receive Clock. The falling edge of this clock output is coincident with the transitions in the serial received data output. The rising edge of RXCLK can be used to latch the valid output data. RXCLK will be valid as long as a carrier is present.
RXD	21	25	O	Received Data Output. Serial receive data is available on this pin. The data is always valid on the rising edge of RXCLK when in synchronous mode. RXD will output constant marks if no carrier is detected.
TXCLK	18	21	O	Transmit Clock. This signal is used in synchronous transmission to latch serial input data on the TXD pin. Data must be provided so that valid data is available on the rising edge of the TXCLK. The transmit clock is derived from different sources depending upon the synchronization mode selection. In internal mode the clock is generated internally. In external mode TXCLK is phase locked to the EXCLK pin. In slave mode TXCLK is phase locked to the RXCLK pin. TXCLK is always active.
TXD	20	24	I	Transmit Data Input. Serial data for transmission is applied on this pin. In synchronous modes, the data must be valid on the rising edge of the TXCLK clock. In asynchronous modes (1200/600 bit/s or 300 baud) no clocking is necessary. DPSK data must be 1200/600 bit/s +1%, -2.5% or +2.3%, -2.5 % in extended over speed mode.

ANALOG INTERFACE AND OSCILLATOR

RXA	27	22	I	Received modulated analog signal input from the telephone line interface.
TXA1 TXA2	16 15	18 17	O	Transmit analog output to the telephone line interface.
XTL1 XTL2	3 4	3 4	I I	These pins are for the internal crystal oscillator requiring a 11.0592 MHz parallel mode crystal. Load capacitors should be connected from XTL1 and XTL2 to ground. XTL2 can also be driven from an external clock.
$\overline{OH}$	23	27	O	Off-hook relay driver. This signal is an open drain output capable of sinking 40 mA and is used for controlling a relay. The output is the complement of the OH register bit in the ID Register.

ELECTRICAL SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING
VDD Supply Voltage	14V
Storage Temperature	-65 to 150°C
Soldering Temperature (10 sec.)	260°C
Applied Voltage	-0.3 to VDD + 0.3V

NOTE: All inputs and outputs are protected from static charge using built-in, industry standard protection devices and all outputs are short-circuit protected.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	CONDITION	MIN	NOM	MAX	UNIT
VDD Supply Voltage		4.5	5	5.5	V
TA, Operating Free-Air		-40		+85	°C
Temperature					
Clock Variation	(11.0592 MHz) Crystal or external clock	-0.01		+0.01	%
External Components (Refer to Application section for placement.)					
VREF Bypass Capacitor	External to GND	0.1			µF
Bias Setting Resistor	Placed between VDD and ISET pins	1.8	2	2.2	MΩ
ISET Bypass Capacitor	ISET pin to GND	0.1			µF
VDD Bypass Capacitor 1	External to GND	0.1			µF
VDD Bypass Capacitor 2	External to GND	22	Note 1		µF
XTL1 Load Capacitor	Depends on crystal characteristics from pin to GND			40	pF
XTL2 Load Capacitor	Depends on crystal characteristics from pin to GND			40	
Hybrid Loading	See Figure 1		600		Ω
R1			600		Ω
C	TXA Hybrid Loading		0.033		µF

NOTE: Minimum for optimized system layout; may require higher values for noisy environments.

DC ELECTRICAL CHARACTERISTICS

(TA = -40°C to 85°C, VDD = recommended range unless otherwise noted.)

PARAMETER	CONDITION	MIN	NOM	MAX	UNIT
IDD, SUPPLY CURRENT	ISET Resistor = 2 MΩ				
IDDA, Active	CLK = 11.0592 MHz		8	12	mA
IDD1, Power-down	CLK = 11.0592 MHz			4	mA
IDD2, Power-down	CLK = 19.200 kHz			3	mA
DIGITAL INPUTS					
VIH, Input High Voltage					
Reset, XTL1, XTL2		3.0		VDD	V
All other inputs		2.0		VDD	V
VIL, Input Low Voltage		0		0.8	V
IIH, Input High Current	VI = VIH Max			100	µA
IIL, Input Low Current	VI = VIL Min	-200			µA
Reset Pull-down Current	Reset = VDD	1		50	µA
Input Capacitance	All Digital Input Pins			10	pF
DIGITAL OUTPUTS					
VOH, Output High Voltage	IOH MIN = -0.4 mA	2.4		VDD	V
VOL, Output Low Voltage	IO MAX = 1.6 mA			0.4	V
VOL, CLK Output	IO = 3.6 mA			0.6	V
RXD Tri-State Pull-up Current	RXD = GND	-1		-50	µA
CMAX, CLK Output	Maximum Capacitive Load			15	pF
OH Output VOL	IOUT = 40 mA			1.0	V
OH Output VOL	IOUT = 10 mA			0.5	V

ELECTRICAL SPECIFICATIONS (continued)

DYNAMIC CHARACTERISTICS AND TIMING

(TA = -40°C to +85°C, VDD = recommended range unless otherwise noted.)

PARAMETER	CONDITION	MIN	NOM	MAX	UNIT
PSK MODULATOR					
Carrier Suppression	Measured between TXA1 and TXA2	55			dB
Output Amplitude	TX scrambled marks	-11.5	-10.0	-9	dBm0
FSK MODULATOR/DEMODULATOR					
Output Frequency Error	CLK = 11.0592 MHz	-0.35		+0.35	%
Transmit Level	Transmit Dotting Pattern	-11.5	-10.0	-9	dBm0
Harmonic Distortion in 700-2900 Hz band	THD in the alternate band DPSK or FSK		-60	-50	dB
Output Bias Distortion	Transmit Dotting Pattern in ALB @ RXD		±8		%
Total Output Jitter	Random Input in ALB @ RXD	-15		+15	%
DTMF GENERATOR					
Frequency Accuracy		-0.25		+0.25	%
Output Amplitude	Low Tone , DPSK Mode	-10	-9	-8	dBm0
Output Amplitude	High Tone , DPSK Mode	-8	-7	-6	dBm0
Twist	High-Tone to Low-Tone , DPSK Mode	1.0	2.0	3.0	dB
Long Loop Detect	DPSK or FSK	-38		-28	dBm0
Dynamic Range	Refer to Performance Curves		45		dB
CALL PROGRESS DETECTOR					
Detect Level Range	2-Tones in 350 - 600 Hz band	-38		-3	dBm0
Reject Level	2-Tones in 350 - 600 Hz band	-43			dBm0
Delay Time	-70 dBm0 to -30 dBm0 STEP	27		80	ms
Hold Time	-30 dBm0 to -70 dBm0 STEP	27		80	ms
Hysteresis		2			dB

NOTE: All units in dBm0 are measured at the line input to the transformer. The interface circuit (Figure 1) inserts an 8 dB loss in the transmit path (TXA1 - TXA2 to line), and a 3 dB loss in the receive path (line to RXA).

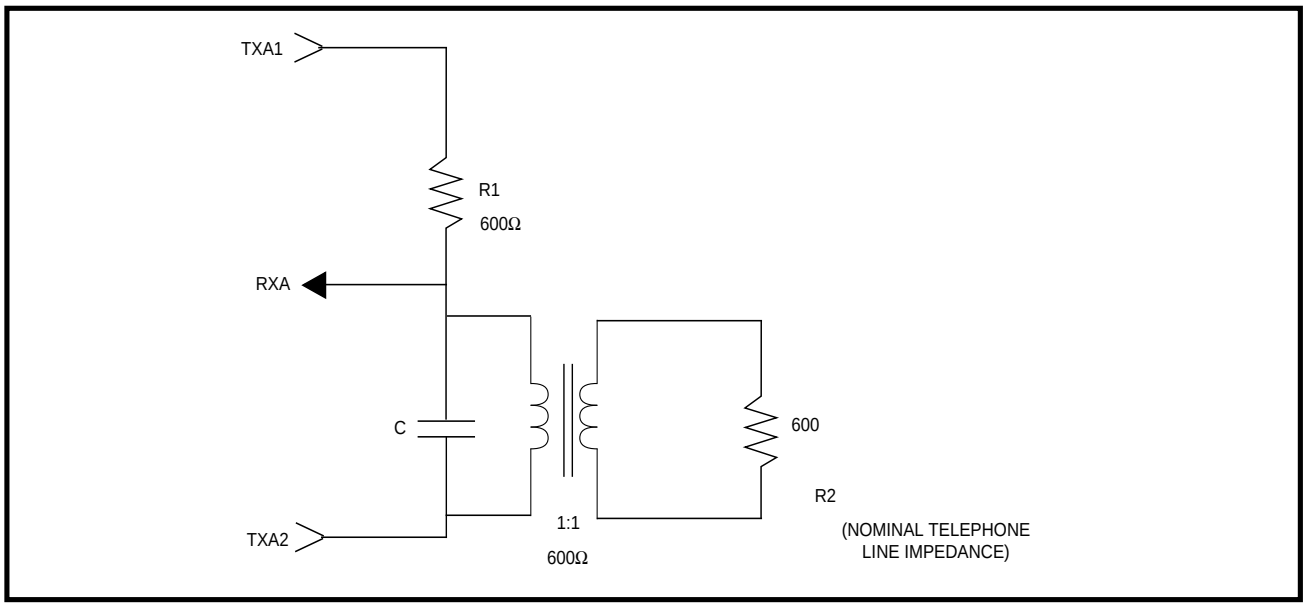


FIGURE 1: TXA Hybrid Loading Analog Interface Hybrid Loading

DYNAMIC CHARACTERISTICS AND TIMING (continued)

PARAMETER	CONDITION	MIN	NOM	MAX	UNIT
CARRIER DETECT	DPSK or FSK				
Threshold	receive data	-48		-43	dBm0
Delay Time	-70 dBm0 to -30 dBm0 STEP	15		45	ms
Hysteresis	Single tone detected	2	3.0		dB
Hold Time	-30 dBm0 to -70 dBm0 STEP	10		24	ms
ANSWER TONE DETECTOR					
Detect Level	Not in V.21 mode	-48		-42	dBm0
Delay Time	-70 dBm0 to -30 dBm0 STEP	20		45	ms
Hold Time	-30 dBm0 to -70 dBm0 STEP	10		30	ms
Detect Frequency Range		-2.5		+2.5	%
OUTPUT SMOOTHING FILTER					
Output	TXA1 to TXA2, loaded as shown in Figure 1 (2% THD)	±2.5			V
Spurious Frequency Components	Frequency = 76.8 kHz Frequency = 153.6 kHz			-39 -45	dBm0 dBm0
TXA pin Output Impedance			200	300	Ω
Clock Noise	TXA pin; 76.8 kHz			1.0	mVrms
CARRIER VCO					
Capture Range	Originate or Answer	-10		+10	Hz
Capture Time	-10 Hz to +10 Hz Carrier Frequency Change Assumption		40	100	ms
RECOVERED CLOCK					
Capture Range	% of frequency center frequency (center at 1200 Hz)	-625		+625	ppm
Data Delay Time	Analog data in at RXA pin to receive data valid at RXD pin		30	50	ms

DYNAMIC CHARACTERISTICS AND TIMING (continued)

PARAMETER	CONDITION	MIN	NOM	MAX	UNIT
GUARD TONE GENERATOR					
Tone Accuracy	550 Hz				
	1800 Hz	-20		+20	Hz
Tone Level	550 Hz	-4.0	-3.0	-2.0	dB
(Below DPSK Output)	1800 Hz	-7.0	-6.0	-5.0	dB
Harmonic Distortion	550 Hz			-50	dB
700 to 2900 Hz	1800 Hz			-60	dB
TIMING (Refer to Timing Diagrams)					
TAL	$\overline{CS}$/Address setup before ALE Low	30			ns
TLA	$\overline{CS}$/Address hold after ALE Low	20			ns
TLC	ALE Low to $\overline{RD}$/$\overline{WR}$ Low	40			ns
TCL	$\overline{RD}$/$\overline{WR}$ Control to ALE High	0			ns
TRD	Data out from $\overline{RD}$ Low	0		160	ns
TLL	ALE width	60			ns
TRDF	Data float after $\overline{RD}$ High	0		80	ns
TRW	$\overline{RD}$ width	200		25000	ns
TWW	$\overline{WR}$ width	140		25000	ns
TDW	Data setup before $\overline{WR}$ High	150			ns
TWD	Data hold after $\overline{WR}$ High	20			ns
TCKD	Data out after EXCLK Low			200	ns
TCKW (serial mode)	$\overline{WR}$ after EXCLK Low	150			ns
TDCK (serial mode)	Data setup before EXCLK Low	150			ns
TAC (serial mode)	Address setup before control*	50			ns
TCA (serial mode)	Address hold after control*	50			ns
TWH (serial mode)	Data Hold after EXCLK	20			

* Control for setup is the falling edge of $\overline{RD}$ or $\overline{WR}$. Control for hold is the falling edge of $\overline{RD}$ or the rising edge of $\overline{WR}$.

NOTE: Asserting ALE, $\overline{CS}$, and $\overline{RD}$ or $\overline{WR}$ concurrently can cause unintentional register accesses. When using non-8031 compatible processors, care must be taken to prevent this from occurring when designing the interface logic.

TIMING DIAGRAMS

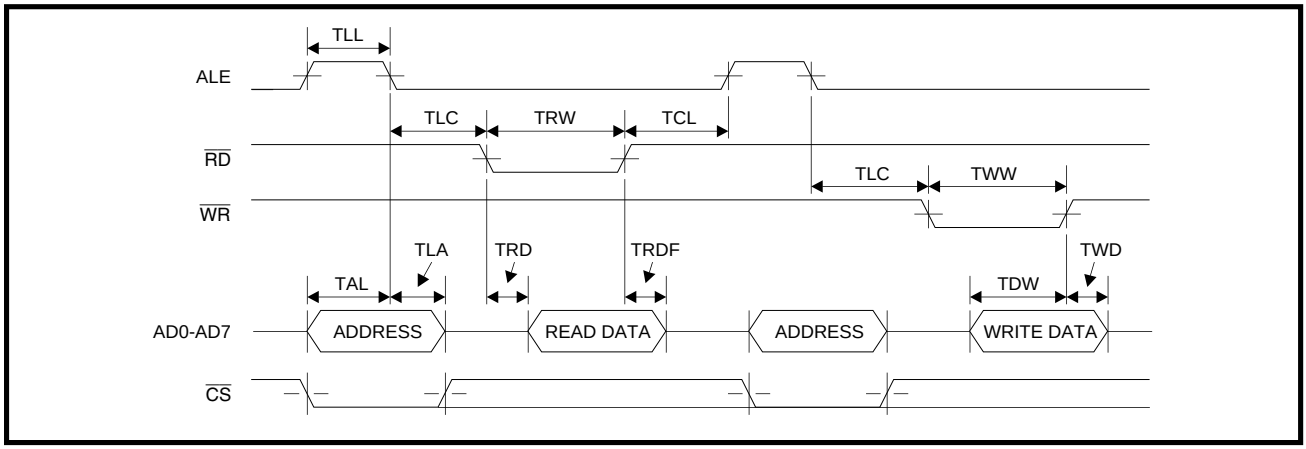


FIGURE 2: Bus Timing Diagram (Parallel Version)

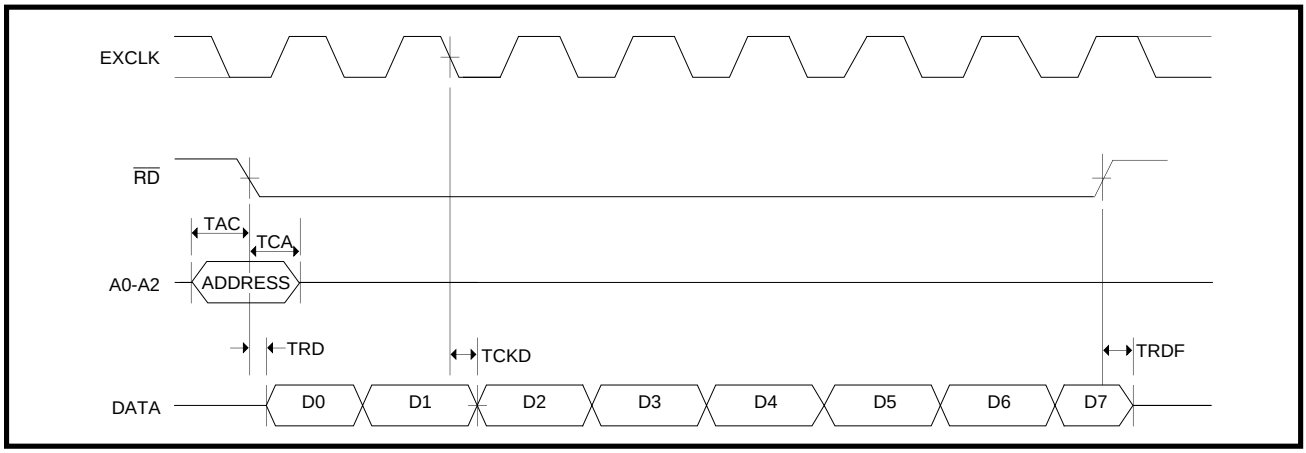


FIGURE 3: Read Timing Diagram (Serial Version)

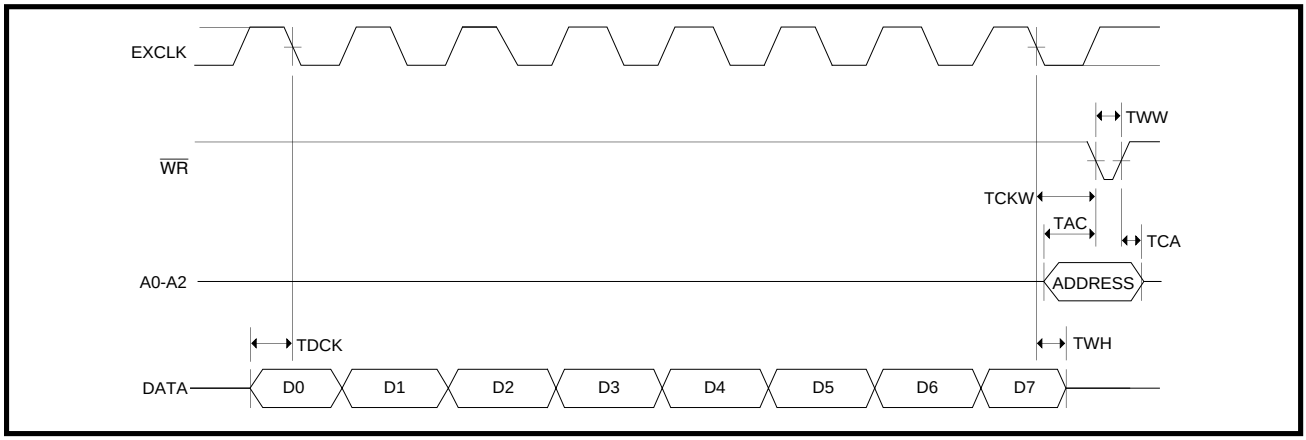


FIGURE 4: Write Timing Diagram (Serial Version)

APPLICATIONS INFORMATION

GENERAL CONSIDERATIONS

Figure 5 shows the basic circuit diagram for a SSI 73K222BL modem integrated circuit designed to be used in conjunction with a control processor, a UART or RS-232 serial data interface, and a DAA phone line interface to function as a typical intelligent modem. The K-Series ICs interface directly with Intel 8048 and 80C51 microprocessors for control and status monitoring purposes. A typical DAA arrangement is shown in Figure 5. This diagram is for reference only and does not represent a production-ready modem design.

The SSI 73K222BL is available with two control interface versions: one for a parallel multiplexed address/data interface, and one for a serial interface. The parallel version is intended for use with 8039/48 or 8031/51 microcontrollers from Intel or many other manufacturers. The serial interface 28-Pin version can be used with other microcontrollers or in applications where only a limited number of port lines are available or the application does not lend itself to a multiplexed address/data interface. The parallel versions may also be used in the serial mode, as explained in the data sheet pin description.

In most applications the controller will monitor the serial data for commands from the DTE and the received data for break signals from the far end modem. In this way, commands to the modem are sent over the same line as the transmitted data. In other applications the RS-232 interface handshake lines are used for modem control.

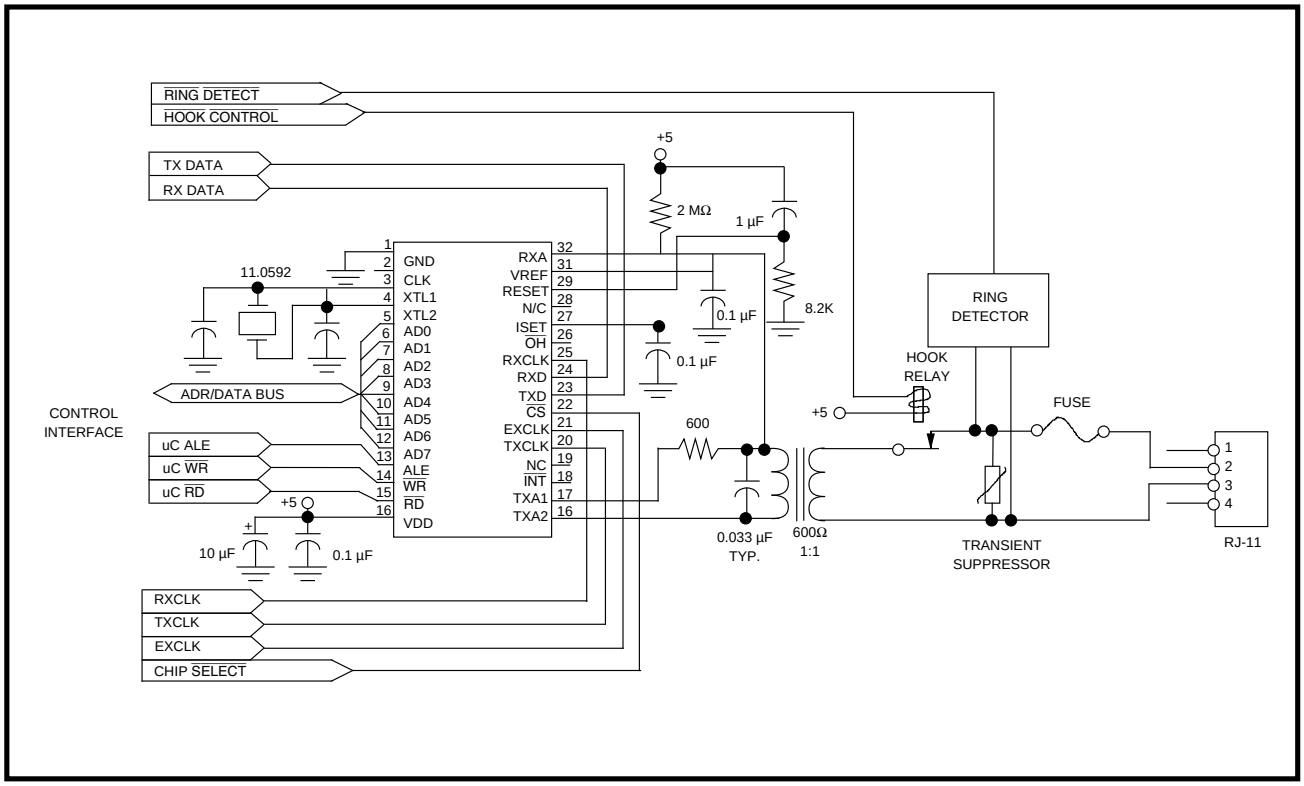


FIGURE 5: Typical SSI 73K222BL DAA Circuit

APPLICATIONS INFORMATION (continued)

DIRECT ACCESS ARRANGEMENT (DAA)

The DAA (Direct Access Arrangement) required for the SSI 73K222BL consists of an impedence matching resistor, telecom coupling transformer, and ring detection and fault protection circuitry.

The transformer specifications must comply with the impedance of the country in which the modem is being operated. Transformers designed specifically for use with the telephone network should be used. These may present a DC load to the network themselves (a "wet" transformer) or they may require AC coupling with a DC load provided by additional devices (a "dry" transformer). A dry transformer will generally provide higher performance and smaller size than a wet transformer. A wet transformer allows a simpler design, but must not saturate with the worst case DC current passing through it or distortion and poor performance will result.

The protection circuitry typically consists of a transient suppression device and current limiter to protect the user and the telephone network from hazardous voltages that can be present under fault conditions. The transient suppressor may be a MOV (metal oxide varistor), Sidactor (Teccor Electronics Inc.), spark gap device , or avalanche diode. Some devices clamp the transient to their specified break down voltage and others go into low impedance crowbar state. The latter require that the fault current cease before they can return to their inactive state.

Current limiting devices can consist of a resistor, Raychem PolySwitch resettable fuse, or slow blow optoisolator fuse that can withstand the transient tests without permenant damage or replacement.

Ring detection circuitry is not required by the FCC, but may be required by the application. The ring detector usually consists of an optoisolator, capacitor, and resistor to present the proper AC load to the network to meet the REN (Ring Equivalency Number) regulations of FCC Part 68. The K-Series Design Manual contains detailed information on the design of a ring detect circuits as well as the other topics concerning the DAA.

DESIGN CONSIDERATIONS

Silicon Systems' 1-chip modem products include all basic modem functions. This makes these devices adaptable for use in a variety of applications, and as easy to control as conventional digital bus peripherals. Unlike digital logic circuitry, modem designs must properly contend with precise frequency tolerances and very low level analog signals, to ensure acceptable performance. Using good analog circuit design practices will generally result in a sound design. Following are additional recommendations which should be taken into consideration when starting new designs.

CRYSTAL OSCILLATOR

The K-Series crystal oscillator requires a parallel mode (antiresonant) crystal which operates at 11.0592 MHz. It is important that this frequency be maintained to within ±0.01% accuracy.

In order for a parallel mode crystal to operate correctly and to specification, it must have a capacitor connected to the junction of each of the crystal and internal inverter connections, terminated to ground. The values of these capacitors depend primarily on the crystal's characteristics, and to a lesser degree on the internal inverter circuit. The values used affect the accuracy and start up characteristics of the oscillator.

LAYOUT CONSIDERATIONS

Good analog/digital design rules must be used to control system noise in order to obtain highest performance in modem designs. The more digital circuitry present on the PC board, the more this attention to noise control is needed. The modem should be treated as a high performance analog device. A 22 µF electrolytic capacitor in parallel with a 0.1 µF ceramic capacitor between VDD and GND is recommended. Liberal use of ground planes and larger traces on power and ground are also highly favored. High speed digital circuits tend to generate a significant amount of EMI (Electro-Magnetic Interference) which must be minimized in order to meet regulatory agency limitations. To accomplish this, high speed digital devices should be locally bypassed, and the telephone line interface and K-Series device should be located close to each other near the area of the board where the phone line connection is accessed. To avoid problems, power supply and ground traces should be routed separately to the analog and digital functions on the board, and digital signals should not be routed near low level or high impedance analog traces. The analog and digital grounds should only connect at one point near the K-Series device ground pin to avoid ground loops. The K-Series modem ICs should have both high frequency and low frequency bypassing as close to the package as possible.

MODEM PERFORMANCE CHARACTERISTICS

The curves presented here define modem IC performance under a variety of line conditions while inducing disturbances that are typical of those encountered during data transmission on public service telephone lines. Test data was taken using an AEA Electronics' "Autotest I" modem test set and line simulator, operating under computer control. All tests were run full-duplex, using a Concord Data Systems 224 as the reference modem. A 511 pseudo-random-bit pattern was used for each data point. Noise was C-message weighted and all signal-to-noise (S/N) ratios reflect total power measurements similar to the CCITT V.56 measurement specification. The individual tests are defined as follows.

BER VS. S/N

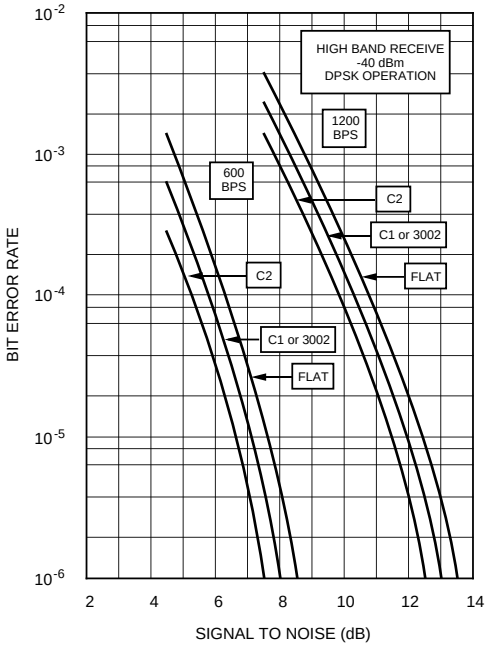
This test measures the ability of the modem to operate over noisy lines with a minimum of data-transfer errors. Since some noise is generated in the best of dial-up lines, the modem must operate with the lowest S/N ratio possible. Better modem performance is indicated by test curves that are closest to the BER axis. A narrow spread between curves representing the four line parameters indicates minimal variation in performance while operating over a range of operating conditions. Typically, a DPSK modem will exhibit better BER performance test curves receiving in the low band than in the high band.

BER VS. RECEIVE LEVEL

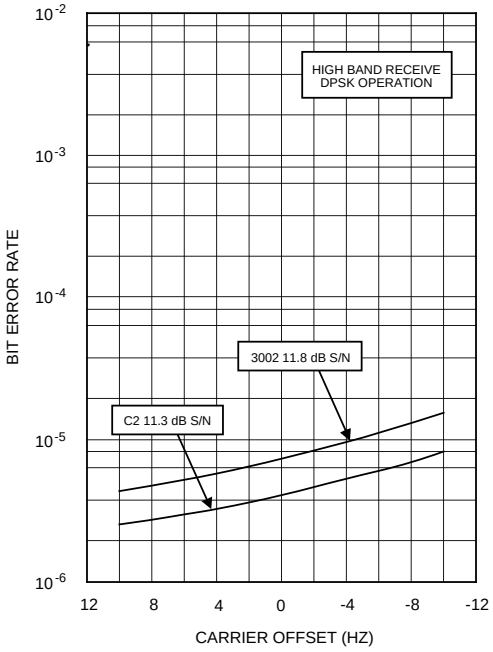
This test measures the dynamic range of the modem. Because signal levels vary widely over dial-up lines, the widest possible dynamic range is desirable. The minimum Bell specification calls for 36 dB of dynamic range. S/N ratios are held constant at the indicated values while the receive level is lowered from a very high to very low signal levels. The width of the "bowl" of these curves, taken at the BER point, is the measure of dynamic range.

APPLICATIONS INFORMATION (continued)

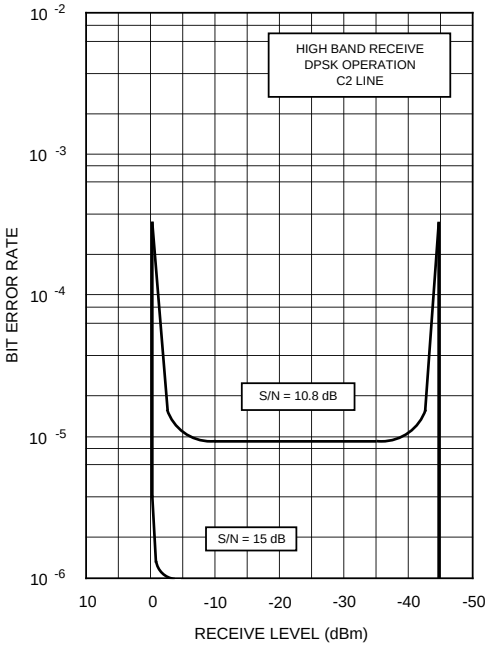
***SSI 73K222BL**
BER vs SIGNALTO NOISE



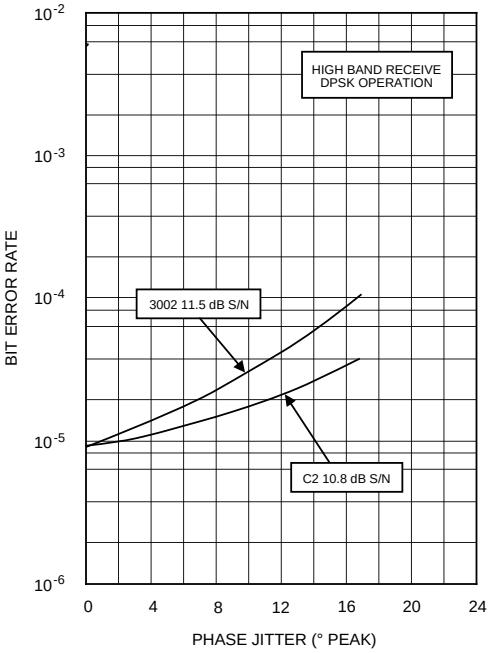
***SSI 73K222BL**
BER vs CARRIER OFFSET



***SSI 73K222BL**
BER vs RECEIVE LEVEL



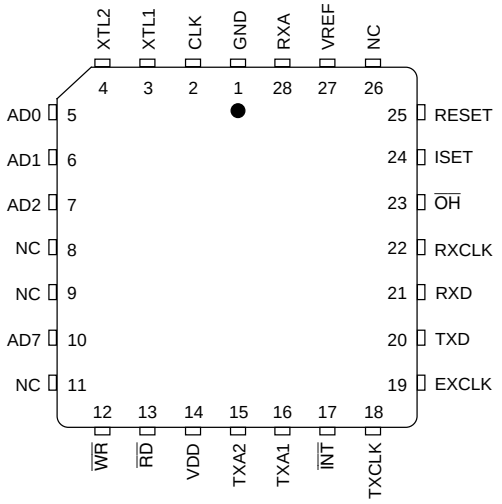
***SSI 73K222BL**
BER vs PHASE JITTER



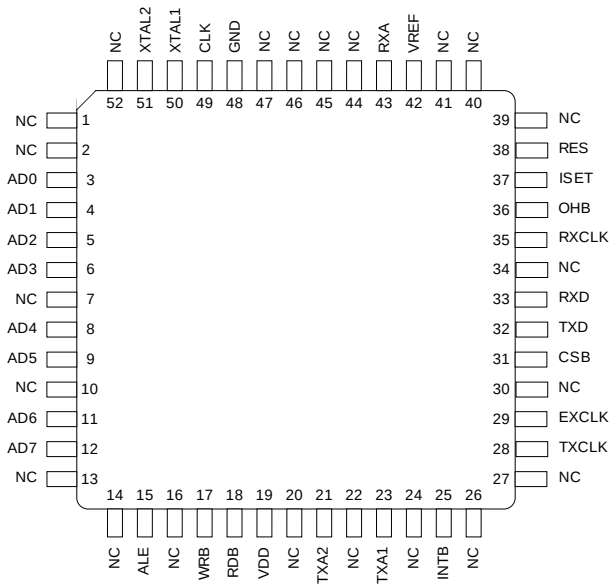
***** = "EQ On" Indicates bit CR1 D4 is set for additional phase equalization.

PACKAGE PIN DESIGNATIONS

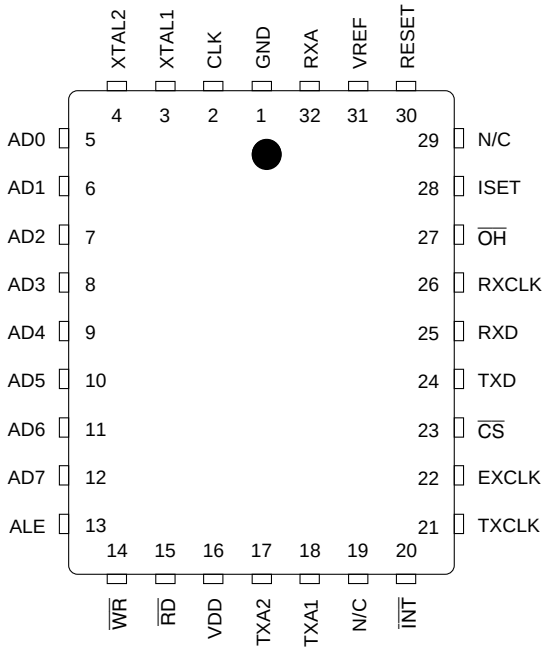
(Top View)



28-Lead PLCC
Serial Mode



52-Lead QFP
Parallel Mode



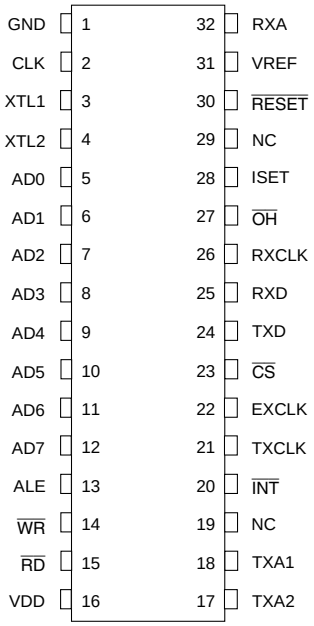
32-Lead PLCC
Parallel Mode

CAUTION: Use handling procedures necessary for a static sensitive component.

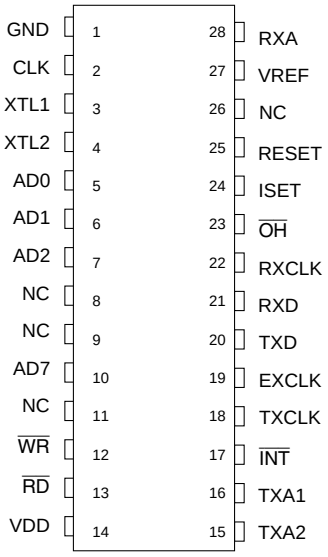
PACKAGE PIN DESIGNATIONS

(Top View)

CAUTION: Use handling procedures necessary for a static sensitive component.



600-Mil
32-Pin DIP
Parallel Mode



600-Mil
28-Pin DIP
Serial Mode

ORDERING INFORMATION

PART DESCRIPTION		ORDER NUMBER	PACKAGING MARK
SSI 73K222BL	Parallel Control Interface		
	32-Lead PLCC	73K222BL-IH	73K222BL-IH
	32-Pin DIP	73K222BL-IP	73K222BL-IP
	52-Lead Quad Flat Pack	73K222BL-IG	73K222BL-IG
SSI 73K222BSL	Serial Control Interface		
	28-Pin DIP	73K222BSL-IP	73K222BSL-IP
	28-Lead PLCC	73K222BSL-IH	73K222BSL-IH

Advance Information: Indicates a product still in the design cycle, and any specifications are based on design goals only. Do not use for final design.

Silicon Systems, Inc., 14351 Myford Road, Tustin, CA 92680-7022, (714) 573-6000, FAX: (714) 573-6914

silicon systems®
A TDK Group Company

SSI 73K222U
Single-Chip Modem with UART

March 1996

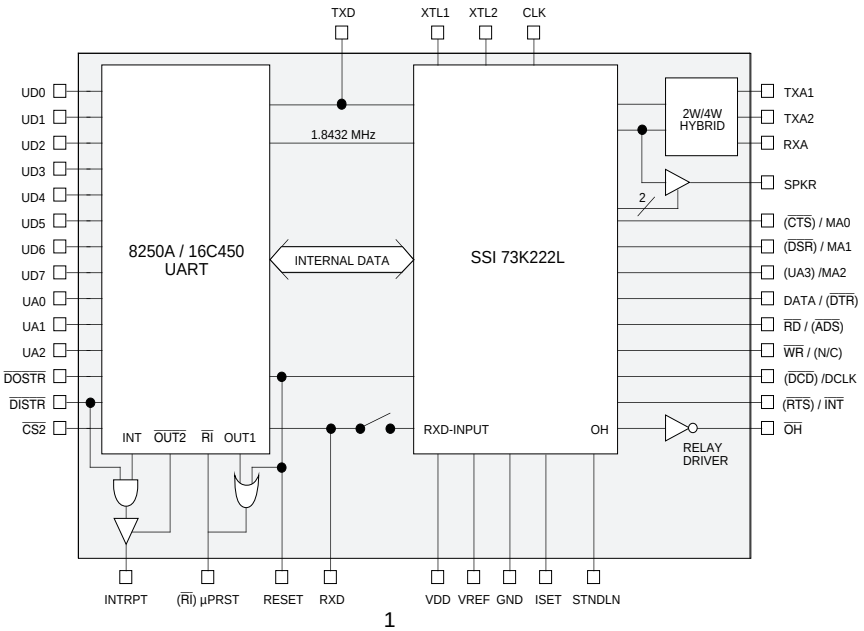
DESCRIPTION

The SSI 73K222U is a compact, high-performance modem which includes a 8250A/16C450 compatible UART with the 1200 bit/s modem function on a single chip. Based on the SSI 73K222L 5V low power CMOS modem IC, the SSI 73K222U is the perfect modem/ UART component for integral modem applications. It is ideal for applications such as portable terminals and laptop computers. The SSI 73K222U is the first fully featured modem IC which can function as an intelligent modem in integral applications without requiring a separate dedicated microcontroller. It provides for data communication at 1200, 600, and 300 bit/s in a multi-mode manner that allows operation compatible with both Bell 212A/103 and CCITT V.22/V.21 standards. The digital interface section contains a high speed version of the industrystandard 8250A/16C450 UART, commonly used in personal computer products. A unique feature of the SSI 73K222U is that the UART section can be used without the modem function, providing an additional asynchronous port at no added cost. The SSI 73K222U is designed in CMOS technology and operates from a single +5V supply. Available packaging includes 40-pin DIP or 44-pin PLCC for surface mount applications.

FEATURES

- **Modem/UART combination optimized for integral bus applications**
- **Includes features of SSI 73K222L single-chip modem**
- **Fully compatible 16C450/8250 UART with 8250B or 8250A selectable interrupt emulation**
- **High speed UART will interface directly with high clock rate bus with no wait states**
- **Single-port mode allows full modem and UART control from CPU bus, with no dedicated microprocessor required**
- **Dual-port mode suits conventional designs using local microprocessor for transparent modem operation**
- **Complete modem functions for 1200 bit/s (Bell 212A, V.22) and 0-300 bit/s (Bell 103, V.21)**
- **Includes DTMF generator, carrier, call-progress and precise answer-tone detectors for intelligent dialing capability**
- **On chip 2-wire/4-wire hybrid driver and off-hook relay buffer**
- **Speaker output with four-level software driven volume control**
- **Low power CMOS (40 mW) with power down mode (15 mW)**
- **Operates from single +5V supply**

BLOCK DIAGRAM



FUNCTIONAL DESCRIPTION

The SSI 73K222U integrates an industry standard 8250/16C450 UART function with the modem capability provided by the SSI 73K222L single chip modem IC. The SSI 73K222U is designed specifically for integral microprocessor bus intelligent modem products. These designs typically require the standard 8250 or higher speed 16450 UART to perform parallel-to-serial and serial-to-parallel conversion process necessary to interface a parallel bus with the inherently serial modem function. The SSI 73K222U provides a highly integrated design which can eliminate multiple components in any integral bus modem application, and is ideal for internal PC modem applications.

The SSI 73K222U includes two possible operating modes. In the dual-port mode, the device is suitable for conventional plug-in modem card designs which use a separate local microprocessor for command interpretation and control of the modem function. In this mode, a dedicated microcontroller communicates with the SSI 73K222U using a separate serial command port. In the single-port mode the main CPU can control both the UART and modem function using the parallel data bus.This allows very efficient modem design with no local microprocessor required for dedicated applications such as laptop PC's or specialized terminals.

To make designs more space efficient, the SSI 73K222U includes the 2-wire to 4-wire hybrid drivers, off-hook relay driver, and an audio monitor output with software volume control for audible call progress monitoring. As an added feature the UART function can be used independent of the modem function, providing an added asynchronous port in a typical PC application with no additional circuitry required.

UART FUNCTION (16C450)

The UART section of the SSI 73K222U is completely compatible with the industry standard 16C450 and the 8250 UART devices. The bus interface is identical to the 16450, except that only a single polarity for the control signals is supported. The register contents and addresses are also the same as the 16C450. To insure compatibility with all existing releases of the 8250 UART design, external circuitry normally used in PC applications to emulate 8250B or 8250A interrupt operation has been included on the SSI 73K222U. A select line is then provided to enable the desired interrupt operation. The UART used in the SSI 73K222U can be used with faster bus read and write cycles than a conventional 16C450 UART. This allows it to interface directly with higher clock rate microprocessors with no need for external circuitry to generate wait states.

The primary function of the UART is to perform parallel-to-serial conversion on data received from the CPU and serial-to-parallel conversion on data received from the internal modem or an external device. The UART can program the number of bits per character, parity bit generation and checking, and the number of stop bits. The UART also provides break generation and detection, detection of error conditions, and reporting of status at any time. A prioritized maskable interrupt is also provided.

The UART block has a progammable baud rate generator which divides an internal 1.8432 MHz clock to generate a clock at 16 x the data rate. The data rate for the transmit and receive sections must be the same. For DPSK modulation, the data rate must be 1200 Hz or 600 Hz. For FSK modulation, the data rate must be 300 Hz or less. The baud generator can create a clock that supports digital transfer at up to 115.2 kHz. The output of the baud generator can be made available at the CLK pin under program control.

MODEM FUNCTION (SSI 73K222L)

The modem section of the SSI 73K222U provides all necessary analog functions required to create a single chip Bell 212A/103 and CCITT V.22/V.21 modem, controlled by the system CPU or a local dedicated microprocessor. Asynchronous 1200 bit/s DPSK (Bell 212A and V.22) and 300 baud FSK (Bell 103 and V.21) modes are supported.

The modem portion acts as a peripheral to the microprocessor. In both modes of operation, control information is stored in register memory at specific address locations. In the single-port mode, the modem section can be controlled through the 16C450 interface, with no external microcontroller required. The primary analog blocks are the DPSK modulator/demodulator, the FSK modulator/demodulator, the high and low band filters, the AGC, the special detect circuitry, and the DTMF tone generator. The analog functions are performed with switched capacitor technology.

PSK MODULATOR / DEMODULATOR

The SSI 73K222U modulates a serial bit stream into dibit pairs that are represented by four possible phase shifts as prescribed by the Bell 212A or V.22 standard. The baseband signal is then filtered to reduce intersymbol interference on the band limited 2-wire PSTN line. Transmission occurs using either a 1200 Hz (originate mode) or 2400 Hz carrier (answer mode). Demodulation is the reverse of the modulation process, with the incoming analog signal eventually decoded into dibits and converted back to a serial bit stream. The demodulator also recovers the clock which was encoded into the analog signal during modulation. The demodulator decodes either a 1200 Hz carrier (originate carrier) or a 2400 Hz carrier (answer carrier). The SSI 73K222U uses a phase-locked-loop coherent demodulation technique that offers inherently better performance than typical DPSK demodulators used by other manufacturers.

FSK MODULATOR/DEMODULATOR

The FSK modulator frequency modulates the analog output signal using two discrete frequencies to represent the binary data. In Bell 103, the standard frequencies of 1270 Hz and 1070 Hz (originate mark and space) and 2225Hz and 2025 Hz (answer mark and space) are used. V.21 mode uses 980 Hz and 1180 Hz (originate, mark and space) or 1650 Hz and 1850 Hz (answer, mark and space). Demodulation involves detecting the received frequencies and decoding them into the appropriate binary value.

PASSBAND FILTERS AND EQUALIZERS

A high and low band filter is included to shape the amplitude and phase response of the transmit signal and provide compromise delay equalization and rejection of out-of-band signals in the receive channel. Amplitude and phase equalization is necessary to compensate for distortion of the transmission line and to reduce intersymbol interference in the band limited receive signal. The transmit signal filtering approximates a 75% square root of raised Cosine frequency response characteristic.

AGC

The automatic gain control maintains a signal level at the input to the demodulators which is constant to within 1 dB. It corrects quickly for increases in signal which would cause clipping, and provides a total dynamic range of >45 dB.

SPECIAL DETECT CIRCUITRY

The special detect circuitry monitors the received analog signal to determine status or presence of carrier, call-progress tones, answer tone, and weak received signal (long loop condition). An unscrambled mark signal is also detected when the received data out of the DPSK demodulator before the descrambler has been high for 165.5 mS ±13.5 mS. The appropriate status bit is set when one of these conditions changes and an interrupt is generated for all monitored conditions except long loop. The interrupts are disabled (masked) when the enable interrupt bit is set to a 0.

DTMF GENERATOR

The DTMF generator will output one of 16 standard dual-tones determined by a 4-bit binary value and TX DTMF mode bit previously loaded into the tone register. Tone generation is initiated when the DTMF mode is selected and the transmit enable (CR0 bit D1) is changed from a 0 to a 1.

TEST FEATURES

Test features such as analog loopback (ALB), remote digital loopback, local digital loopback, and internal pattern generators are also included.

LINE INTERFACE

The line interface of the SSI 73K222U consists of a two-to-four wire hybrid, and an off-hook relay driver.

The two-to-four wire converter has a differential transmit output and requires only a line transformer and an external impedance matching resistor. Four-wire operation is also available by simply using either of the transmit output signals.

The relay driver output of the SSI 73K222U is an open drain signal capable of sinking 20 mA, which can control a line closure relay used to take the line off hook and to perform pulse dialing.

AUDIO MONITOR

An audio monitor output is provided which has a software programmable volume control. Its output is the received signal. The audio monitor output can directly drive a high impedance load, but an external power amplifier is necessary to drive a low-impedance speaker.

PIN DESCRIPTION

GENERAL

NAME	DIP	PLCC	TYPE	DESCRIPTION
VDD	40	44	I	+5V Supply ±10%, bypass with a 0.1 and a 22 μF capacitor to GND
GND	20	22	I	System Ground
VREF	19	21	O	VREF is an internally generated reference voltage which is externally bypassed by a 0.1 μF capacitor to the system ground.
ISET	9	11	I	The analog current is set by connecting this pin to VDD through a 2 MΩ resistor. ISET should be bypassed to GND. Alternatively, an internal bias can be selected by connecting ISET to GND, which will result in a larger worst-case supply current due to the tolerance of on-chip resistors. Bypass with 0.1 μF capacitor if resistor is used.
XTL1 XTL2	25 24	27 26	I I	These pins are connections for the internal crystal oscillator requiring an 11.0592 MHz crystal (9216Hz x 1200). XTL2 can also be TTL driven from an external clock. Connect a 10 MΩ resistor from XTL1 to ground.
CLK	21	23	O	Output Clock. This pin is selectable under processor control to be either the crystal frequency (which might be used as a processor clock) or the output of the baud generator.
RESET	10	12	I	Reset. An active signal (high) on this pin will put the chip into an inactive state. The control register bits (except the Receiver Buffer, Transmitter Holding, and Divisor latches) will be reset. The output of the CLK pin will be set to the crystal frequency. An internal pull-down resistor permits power-on reset using a 0.1 μF capacitor connected to the 5V supply.
STNDLN	15	17	I	Single-port mode select (active high). In a single-port system there is no local microprocessor and all the modem control is done through the 16C450 parallel bus interface. The local microprocessor interface is replaced with UART control signals which allow the device to function as a digital UART as well as modem.

UART INTERFACE

NAME	DIP	PLCC	TYPE	DESCRIPTION
UA0-UA2 UA3	37-39 12	41-43 14	I I	UART Address. These pins determine which of the UART registers is being selected during a read or write on the UART data bus. The contents of the DLAB bit in the UART's Line Control Register also control which register is referenced. In single-port mode, UA0-UA3 are latched when $\overline{ADS}$ goes high. In dual-port, only UA0-UA2 are used.
UDO-UD7	27-34	30-37	I/O	(3 state) UART Data. Data or control information to the UART registers is carried over these lines.
$\overline{DISTR}$	35	38	I	Data Input Strobe. A low on this pin requests a read of the internal UART registers. Data is output on the D0-D7 lines if $\overline{DISTR}$ and $\overline{CS2}$ are active.
$\overline{DOSTR}$	36	39	I	Data Output Strobe. A low on this pin requests a write of the internal UART registers. Data on the D0-D7 lines are latched on the rising edge of $\overline{DOSTR}$. Data is only written if both $\overline{DOSTR}$ and $\overline{CS2}$ are active.
$\overline{CS2}$	1	2	I	Chip Select. A low on this pin allows a read or write to the UART registers to occur. In single port mode, $\overline{CS2}$ is latched on $\overline{ADS}$.
INTRPT	5	7	O	(3 state) UART Interrupt. This signal indicates that an interrupt condition on the UART side has occurred. If the Enable 8250A interrupt bit in the interrupt Enable Register is 0 the interrupt is gated by the $\overline{DISTR}$ signal to provide compatibility with the 8250B. The output can be put in a high impedance state with the OUT2 register bit in the Modem Control Register. In single-port mode, INTRPT also becomes valid when a modem interrupt signal is generated by the modem section's Detect Register.
RXD	6	8	I/O	Function is determined by STNDLN pin and bit 7, Tone Control Register:

STNDLN	D7	
0	0	RXD outputs data received by modem.
1	0	RXD is electrically an input but signal is ignored.
X	1	RXD is a serial input to UART.

UART INTERFACE (continued)

<table>
<tr><th>NAME</th><th>DIP</th><th>PLCC</th><th>TYPE</th><th>DESCRIPTION</th></tr>
<tr><td>TXD</td><td>7</td><td>9</td><td>O</td><td>Function is determined by STNDLN pin and bit 7, Tone Control Register:
<table>
<tr><td>STNDLN</td><td>D7</td><td></td></tr>
<tr><td>0</td><td>0</td><td>TXD is a serial output of UART.</td></tr>
<tr><td>1</td><td>0</td><td>TXD is forced to a mark.</td></tr>
<tr><td>X</td><td>1</td><td>TXD is a serial output of UART.</td></tr>
</table></td></tr>
</table>

ANALOG / LINE INTERFACE

TXA1 TXA2	3 4	4 5	O O	(differential) Transmitted Analog. These pins provide the analog output signals to be transmitted to the phone line. The drivers will differentially drive the impedance of the line transformer and the line matching resistor. An external hybrid can also be built using TXA1 as a single ended transmit signal.
RXA	16	18	I	Received Analog. This pin inputs analog information that is being received by the two-to-four wire hybrid. This input can also be taken directly from an external hybrid.
SPKR	17	19	O	Speaker Output. This pin outputs the received signal through a programmable attenuator stage, which can be used for volume control and disabling the speaker.
$\overline{OH}$	18	20	O	Off-hook relay driver. This signal is an open drain output capable of sinking 20 mA and is used for controlling a relay. The output is the complement of the $\overline{OH}$ register bit in CR3.

UART CONTROL INTERFACE (STNDLN = 1)
(See Figure 1: Single-port mode)

NAME	DIP	PLCC	TYPE	DESCRIPTION
$\overline{ADS}$	23	25	I	Address Strobe. $\overline{ADS}$ is used to latch address and chip select to simplify interfacing to a multiplexed Address/Data Bus. UA0-UA3 and $\overline{CS2}$ are latched when the $\overline{ADS}$ signal goes high.
UA3	12	14	I	UART Address Bit 3. UA3 is used in single-port mode to address the modem registers from the 16C450 interface. If UA3 is 0, the normal 16C450 registers are addressed by UA0-UA2 and if UA3 is 1, the modem registers are addressed. UA3 is latched when $\overline{ADS}$ goes high.
$\overline{CTS}$	14	16	I	Clear to Send. This pin is the complement of CTS bit in the Modem Status Register. The signal is used in modem handshake control to signify that communications have been established and that data can be transmitted.
$\overline{DSR}$	13	15	I	Data Set Ready.This pin is the complement of DSR bit in the Modem Status Register.The signal is used in modem handshake to signify that the modem is ready to establish communications.
$\overline{DCD}$	11	13	I	Data Carrier Detect. This pin is the complement of DCD bit in the Modem Status Register. The signal is used in modem control handshake to signify that the modem is receiving a carrier.
$\overline{DTR}$	22	24	O	Data Terminal Ready. The $\overline{DTR}$ output is programmed through a bit in the Modem Control Register. The signal is used in modem handshake to signify that the 16C450 is available to communicate.
$\overline{RTS}$	2	3	O	Request to Send. The $\overline{RTS}$ output is programmed through a bit in the Modem Control Register. The signal is used in modem handshake to signify that the 16C450 has data to transmit.
$\overline{RI}$	8	10	I	Ring Indicator. This Indicates that a telephone ringing signal is being received. This pin is the complement of the RI bit in the Modem Status Register.

PIN DESCRIPTION (continued)

MICROPROCESSOR INTERFACE (STNDLN = 0)
(See Figure 2: Dual-port mode)

NAME	DIP	PLCC	TYPE	DESCRIPTION
MA0-MA2	12-14	14-16	I	Modem Address Control. These lines carry register addresses for the modem registers and should be valid throughout any read or write operation.
DATA	22	24	I/O	Serial Control Data. Serial control data to be read/written is clocked in/out on the falling edge of the DCLK pin. The direction of data transfer is controlled by the state of the $\overline{RD}$ pin. If the $\overline{RD}$ pin is active (low) the DATA line is an output. Conversely, if the $\overline{RD}$ pin is inactive (high) the DATA line is an input.
$\overline{RD}$	23	25	I	Read. A low on this input informs the SSI 73K222U that control data or status information is being read by the processor from a modem register.
$\overline{WR}$	26	28	I	Write. A low on this input informs the SSI 73K222U that control data or status information is available for writing into a modem register. The procedure for writing is to shift in data LSB first on the DATA pin for eight consecutive cycles of DCLK and then to pulse $\overline{WR}$ low. Data is written on the rising edge of $\overline{WR}$.
DCLK	11	13	I	Data Clock. The falling edge of this clock is used to strobe control data for the modem registers in or out on the DATA pin. The normal procedure for a write is to shift in data LSB first on the DATA pin for eight consecutive cycles of DCLK and then to pulse $\overline{WR}$ low. Data is written on the rising edge of $\overline{WR}$. The falling edge of the $\overline{RD}$ signal must continue for eight cycles of DCLK in order to read all eight bits of the reference register. Read data is provided LSB first. Data will not be output unless the $\overline{RD}$ signal is active.
$\overline{INT}$	2	3	O	(with weak pull-up) Modem Interrupt. This output signal is used to inform the modem processor that a change in a modem detect flag has occurred. The processor must then read the Modem Detect Register to determine which detect triggered the interrupt. $\overline{INT}$ will stay active until the processor reads the Modem Detect Register or does a full reset.
MPRST*	8	10	O	Microprocessor Reset. This output signal is used to provide a hardware reset to the microprocessor. This signal is high if the RESET pin is high or the MCR bit D3 (OUT1) bit is set.
* NOTE: The µPRST pin is an upgraded function which was not included in the initial definition of the SSI 73K222U.				

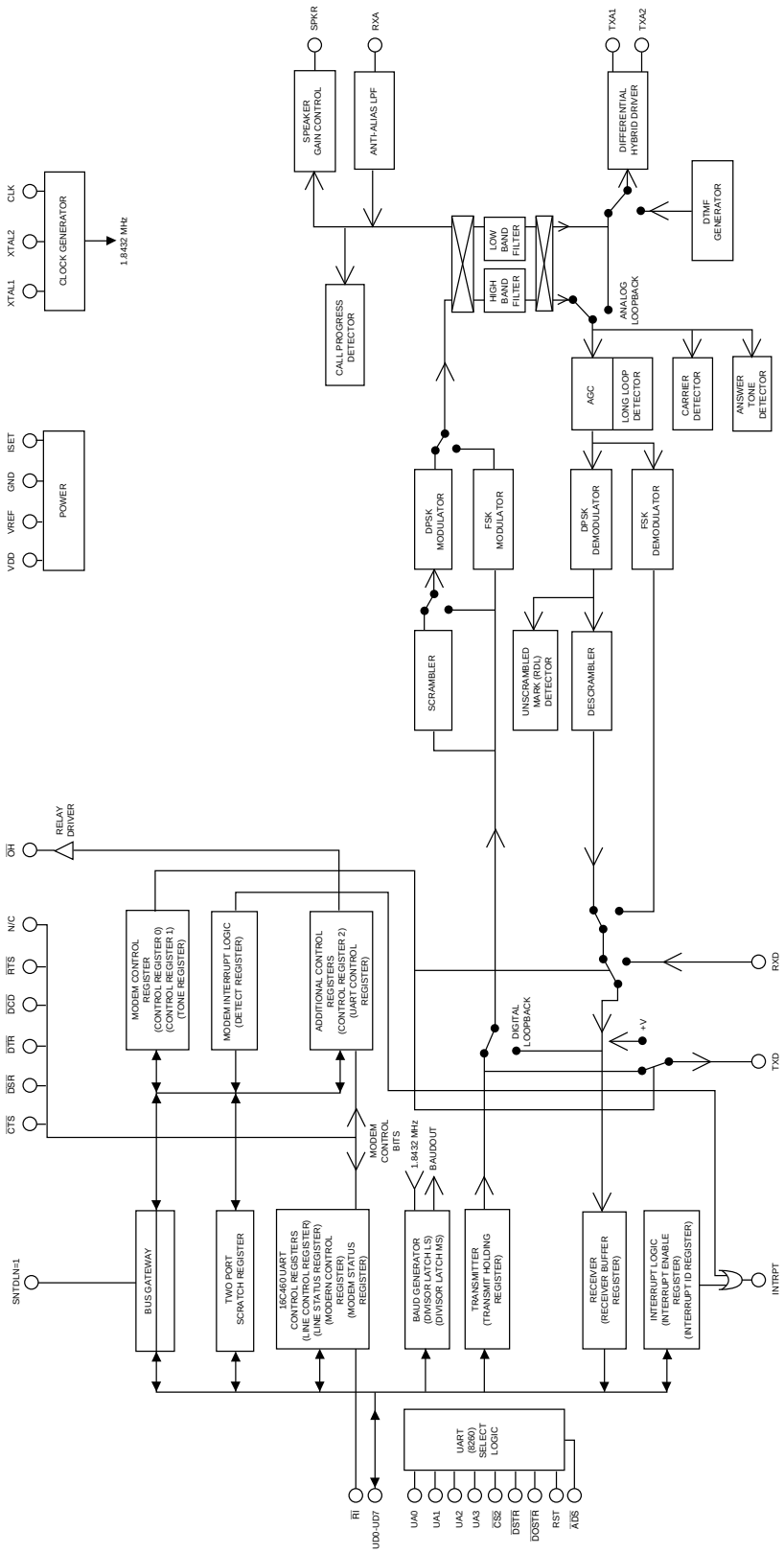


FIGURE 1:
Single-Port Mode

In the single-port mode, the SSI 73K222U is designed to be accessed only by the main CPU using the same parallel bus utilized for data transfer. This mode is enabled when the STNDLN pin is at a logic "1". In the single port mode, internal registers are accessed by the main CPU to configure both the UART section and the modem function, eliminating the need for a separate microcontroller. In this mode, multiplexed pins provide the $\overline{CTS}$, $\overline{DSR}$, $\overline{DTR}$, $\overline{DED}$ and $\overline{RI}$ signals normally associated with the UART function. A separate pin, $\overline{ADS}$, is used for bus control.

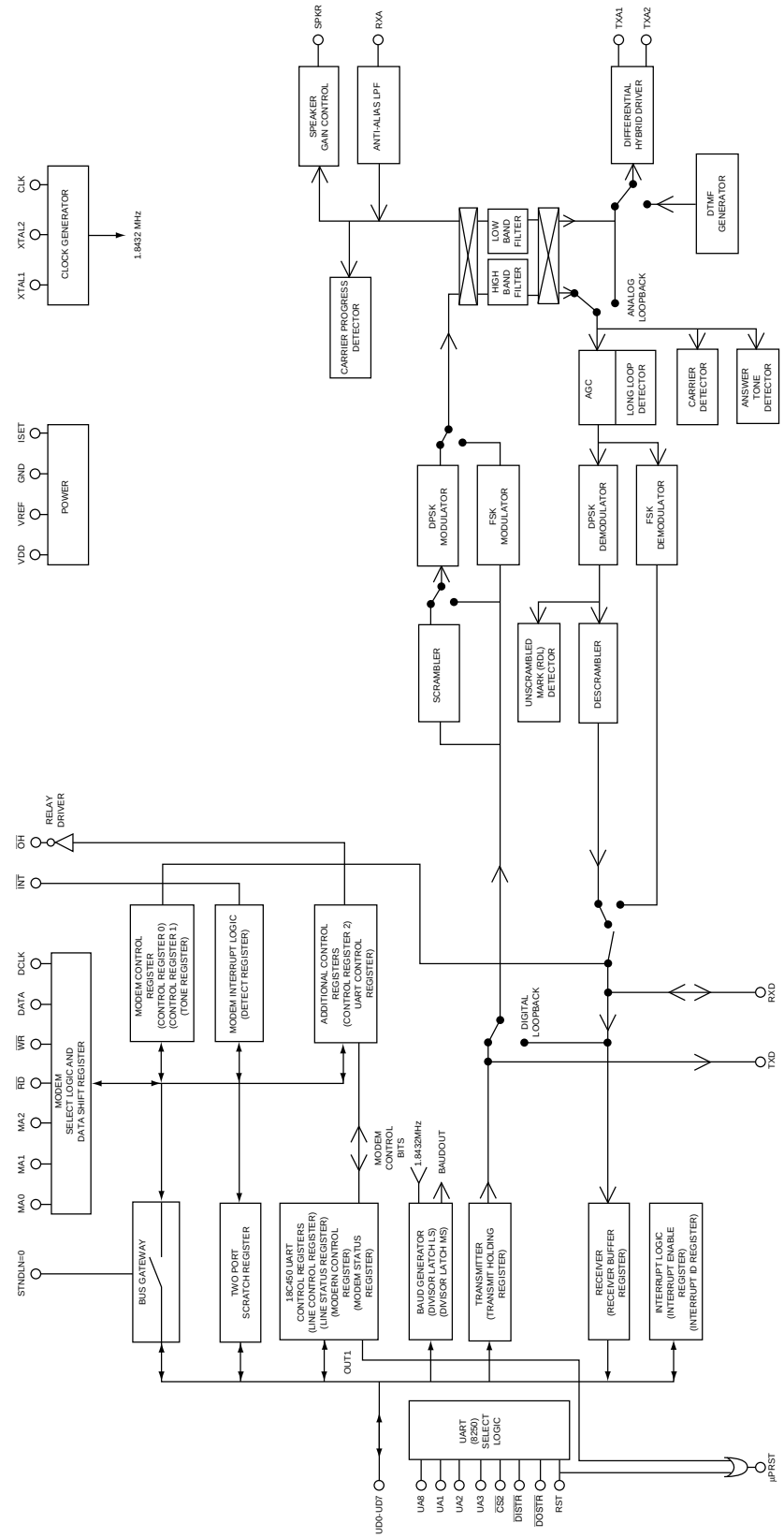


FIGURE 2:
Dual-Port Mode

The dual-port mode allows use of a dedicated microprocessor for control of the modem function, and is enabled when the STNDLN pin = "0". This mode is useful for conventional plug-in card modem designs where it is necessary to make the modem function transparent to the main CPU. In this mode, the SSI 73K222U's multiplexed pins form the serial command bus used to communicate with the external microprocessor. The $\overline{RI}$, $\overline{CTS}$, $\overline{DSR}$, $\overline{DTR}$, and $\overline{DCD}$ logic functions must then be implemented using ports from the dedicated microprocessor.

The serial control interface allows access to the control and status registers via a serial command port. In this mode the MA0, MA1, and MA2 lines provide register addresses for data passed through the DATA pin under control of the $\overline{RD}$ and $\overline{WR}$ lines. A read operation is initiated when the $\overline{RD}$ line is taken low. The next eight cycles of DCLK will then transfer out eight bits of the selected address location LSB first. A write takes place by shifting in eight bits of data LSB first for eight consecutive cycles of DCLK. $\overline{WR}$ is then pulsed low and data transfer into the selected register occurs on the rising edge of $\overline{WR}$.

UART CONTROL REGISTER OVERVIEW

REGISTER		UART ADDRESS UA3-UA0*	DATA BIT NUMBER D7	D6	D5	D4	D3	D2	D1	D0
RECEIVER BUFFER REGISTER (READ ONLY)	RBR	0000 DLAB = 0	BIT 7 (MSB)	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0 (LSB)
TRANSMIT HOLDING REGISTER (WRITE ONLY)	THR	0000 DLAB = 0	BIT 7 (MSB)	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0 (LSB)
INTERRUPT ENABLE REGISTER	IER	0001 DLAB = 0	0	0	0	ENABLE 8250A/ 16C450 INTERRUPT	ENABLE MODEM STATUS INTERRUPT	ENABLE REC. LINE STATUS INTERRUPT	ENABLE THR EMPTY INTERRUPT	ENABLE REC. DATA AVAILABLE INTERRUPT
INTERRUPT ID REGISTER (READ ONLY)	IIR	0010	0	0	0	0	0	INTERRUPT ID BIT 1	INTERRUPT ID BIT 0	"0" IF INTERRUPT PENDING
LINE CONTROL REGISTER	LCR	0011	DIVISOR LATCH ACCESS (DLAB)	SET BREAK	STICK PARITY	EVEN PARITY SELECT (EPS)	PARITY ENABLE (PEN)	NUMBER OF STOP BITS (STB)	WORD LENGTH SELECT 1 (WLS1)	WORD LENGTH SELECT 0 (WLS0)
MODEM CONTROL REGISTER	MCR	0100	0	0	0	LOOP	ENABLE INTERRUPT (OUT2 IN 16C450)	µPRST (OUT1 IN 16C450)	REQUEST TO SEND (RTS)	DATA TERMINAL READY (DTR)
LINE STATUS REGISTER	LSR	0101	0	TRANSMIT SHIFT REG. EMPTY (TSRE)	TRANSMIT HOLDING REGISTER EMPTY (THRE)	BREAK INTERRUPT (BI)	FRAMING ERROR (FE)	PARITY ERROR (PE)	OVERRUN ERROR (OE)	DATA READY (DR)
MODEM STATUS REGISTER (READ ONLY)	MSR	0110	DATA CARRIER DETECT (DCD)	RING INDICATOR (RI)	DATA SET READY (DSR)	CLEAR TO SEND (CTS)	DELTA DATA CARR. DETECT (DDCD)	TRAILING EDGE RING INDICATOR (TERI)	DELTA DATA SET READY (DDSR)	DELTA CLEAR TO SEND (DCTS)
SCRATCH REGISTER	SCR	0111	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
DIVISOR LATCH (LS)	DLL	0000 DLAB = 1	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
DIVISOR LATCH (MS)	DLM	0001 DLAB = 1	BIT 15	BIT 15	BIT 13	BIT 12	BIT 11	BIT 10	BIT 9	BIT 8

* In single-port mode (STNDLN pin = 1), all four address lines UA3-UA0 are used to address the UART Control Registers.

* In dual-port mode (STNDLN pin = 0), only three address lines UA2-UA0 are used to address the UART Control Registers; the UA3 pin becomes the MA2 pin in this mode.

MODEM CONTROL REGISTER OVERVIEW

REGISTER		ADDRESS STNDLN 0 MA2-MA0	ADDRESS STNDLN 1 UA3 UA0	DATA BIT NUMBER D7	D6	D5	D4	D3	D2	D1	D0
CONTROL REGISTER 0	CR0	000	1000	MODULATION OPTION	0	MODULATION MODE	POWER ON	CHARACTER SIZE 1 (READ ONLY)	CHARACTER SIZE 0 (READ ONLY)	TRANSMIT ENABLE	ORIGINATE/ ANSWER
CONTROL REGISTER 1	CR1	001	1001	TRANSMIT PATTERN 1	TRANSMIT PATTERN 0	ENABLE DETECT INTERRUPT	BYPASS SCRAMBLER	CLK CONTROL	RESET	TEST MODE 1	TEST MODE 0
DETECT REGISTER	DR	010	1001	DEVICE SIGNATURE 1	DEVICE SIGNATURE 0	RECEIVE DATA	UNSCR. MARK DETECT	CARRIER DETECT	ANSWER TONE DETECT	CALL PROGRESS DETECT	LONG LOOP DETECT
TONE CONTROL REGISTER	TONE	011	1011	RXD/TXD CONTROL	TRANSMIT GUARD TONE	TRANSMIT ANSWER TONE	TRANSMIT DTMF	DTMF 3	DTMF 3	DTMF 1	DTMF 0 GUARD/ANS. TONE
CONTROL REGISTER 2	CR2	100	1100								
CONTROL REGISTER 3	CR3	101	1101	SPEAKER VOLUME 1	SPEAKER VOLUME 0	OFF-HOOK	X	X	X	X	X
SCRATCH REGISTER	SCR	110	1110	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
UART CONTROL REGISTER	UCR	111	1111	TXCLK (READ ONLY)	X	REQUEST TO SEND (RTS) (READ ONLY)	DATA TERM. READY (DTR) (READ ONLY)	RING INDICATOR (RI)	DATA CARRIER DETECT (DCD)	DATA SET READY (DSR)	CLEAR TO SEND (CTS)

X = Undefined, mask in software
0 = Only write zero to this location

UART REGISTER BIT DESCRIPTIONS

UART SECTION

RECEIVER BUFFER REGISTER (RBR) (READ ONLY)

STNDLN:	**0**	**1**
ADDRESS:	**UA2 - UA0 = 000, DLAB = 0**	**UA3 - UA0 = 0000, DLAB = 0**

This read only register contains the parallel received data with start, stop, and parity bits (if any) removed. The high order bits for less than 8 data bits/character will be set to 0.

TRANSMIT HOLDING REGISTER (THR) (WRITE ONLY)

STNDLN:	**0**	**1**
ADDRESS:	**UA2 - UA0 = 000, DLAB = 0**	**UA3 - UA0 = 0000, DLAB = 0**

This write only register contains the parallel data to be transmitted. The data is sent LSB first with start, stop, and parity bits (if any) added to the serial bit stream as the data is transferred.

INTERRUPT ENABLE REGISTER (IER)

STNDLN:	**0**	**1**
ADDRESS:	**UA2 - UA0 = 001, DLAB = 0**	**UA3 - UA0 = 0001, DLAB = 0**

This 8-bit register enables the four types of interrupts of the UART to separately activate the chip Interrupt (INTRPT) output signal. It is possible to totally disable the interrupt system by resetting bits 0 through 3 of the Interrupt Enable Register. Similarly, by setting the appropriate bits of this register to a logic 1, selected interrupts can be enabled. Disabling the interrupt system inhibits the Interrupt Identification Register and the active (high) INTRPT output from the chip. All other system functions operate in their normal manner, including the setting of the Line Status and Modem Status Registers.

BIT NO.	NAME	CONDITION	DESCRIPTION
D0	Received Data	1	This bit enables the Received Data Available Interrupt when set to logic 1.
D1	Transmitter Holding Register Empty	1	This bit enables the Transmitter Holding Register Empty Interrupt, when set to logic 1.
D2	Receiver Line Status Interrupt	1	This bit enables the Receiver Line Status Interrupt, when set to logic 1.
D3	Modem Status	1	This bit enables the Modem Status Register Interrupt when set to interrupt logic 1.
D4	8250A/16450	1/0	Set for compatibility with 8250A/16C450 UARTS. Reset this bit to disable the gating of the INTRPT interrupt line with the $\overline{\text{DISTR}}$ signal which is needed for 8250B compatibility.
D5 - D7	Not Used	0	These three bits are always logic 0.

INTERRUPT ID REGISTER (IIR) (READ ONLY)

UART SECTION

STNDLN:	**0**	**1**
ADDRESS:	**UA2 - UA0 = 010**	**UA3 - UA0 = 0010**

The IIR register gives prioritized information as to the status of interrupt conditions. When accessed, the IIR freezes the highest priority interrupt pending and no other interrupts are acknowledged until the particular interrupt is serviced by the CPU.

BIT NO.	NAME	CONDITION	DESCRIPTION
D0	Interrupt Pending	0	This bit can be used in either a hardwired priortized or polled environment to indicate whether an interrupt is pending. When bit 0 is a logic 0, an interrupt is pending and the IIR contents may be used as a pointer to the appropriate interrupt service routine.
		1	When bit 0 is a logic 1, no interrupt is pending.
D1, D2	Interrupt ID bits 0, 1	Table below	These two bits of the IIR are used to identify the highest priority interrupt pending as indicated in the following table.
D3 - D7	Not Used	0	These five bits of the IIR are always logic 0.

INTERRUPT PRIORITY TABLE

D2	D1	D0	PRIORITY	TYPE	SOURCE	RESET
0	0	1	-	None	None	-
1	1	0	Highest	Receiver Line Status	Overrun Error, Parity Error, Framing Error or Break Interrupt	Reading the Line Status Register
1	0	0	Second	Receive Data Available	Receive Data Available	Reading the Rcvr. Buffer Register
0	1	0	Third	Transmit Holding Register Empty	Transmit Holding Register Empty	Reading IIR Register (if source of interrupt) or Writing to Transmit Holding Register
0	0	0	Fourth	Modem Status	Clear to Send or Data Set Ready or Ring Indicator or Data Carrier Det.	Reading the Modem Status Register

LINE CONTROL REGISTER (LCR)
STNDLN: 0 1
ADDRESS: UA2 - UA0 = 011 UA3 - UA0 = 0011

UART SECTION

The user specifies the format of the asynchronous data communications exchange via the Line Control Register. In addition to controlling the format, the user may retrieve the contents of the Line Control Register for inspection. This feature simplifies system programming and eliminates the need for separate storage in system memory of the line characteristics.

BIT NO.	NAME	CONDITION		DESCRIPTION
D0	Word Length Select 0			Bits D0 and D1 select the number of data bits per character as shown:
D1	Word Length Select 1	D1	D0	Word Length
		0	0	5 bits
		0	1	6 bits
		1	0	7 bits
		1	1	8 bits
D2	Number of Stop Bits	0 or 1		This bit specifies the number of stop bits in each transmitted character. If bit 2 is a logic 0, one stop bit is generated in the transmitted data. If bit 2 is a logic 1 when a 5-bit word length is selected via bits 0 and 1, one-and-a-half stop bits are generated. If bit 2 is a logic 1 when either a 6, 7, or 8-bit word length is selected, two stop bits are generated. The receiver checks the first stop bit only, regardless of the number of stop bits selected.
D3	Parity Enable	1		This bit is the Parity Enable bit. When bit 3 is a logic 1, a parity bit is generated (transmit data) or checked (receive data) between the last data word bit and stop bit of the serial data. (The parity bit is used to produce an even or odd number of 1's when the data word bits and the parity bit are summed).
D4	Even Parity Select	1 or 0		This bit is the Even Parity Select bit. When bit 3 is a logic 1 and bit 4 is a logic 0, an odd number of logic 1's are transmitted or checked in the data word bits and parity bit. When bit 3 is a logic 1 and bit 4 is a logic 1, an even number of logic 1's are transmitted or checked.

LINE CONTROL REGISTER (LCR) (continued)

UART SECTION

BIT NO.	NAME	CONDITION		DESCRIPTION
D5	Stick Parity	1 or 0		This bit is the Stick Parity bit. When bit 3 is a logic 1 and bit 5 is a logic 1, the parity bit is transmitted and checked by the receiver as a logic 0 if bit 4 is a logic 1 or as a logic 1 if bit 4 is a logic 0.
		D5	D4	Parity
		0	0	ODD Parity
		0	1	EVEN Parity
		1	0	MARK Parity
		1	1	SPACE Parity
D6	Set Break	1		Output of modem is set to a spacing state. When the modem is transmitting DPSK data if the Set Break bit is held for one full character (start, data, parity, stop) the break will be extended to 2 N + 3 space bits (where N = # data bits + parity bit + 1 start + 1 stop). Any data bits generated during this time will be ignored. See note below.
D7	Divisor Latch Access Bit (DLAB)	1		This bit is the Divisor Latch Access Bit (DLAB). It must be set high (logic 1) to access the Divisor Latches of the baud generator during a Read or Write operation. It must be set low (logic 0) to access the Receiver Buffer, the Transmitter Holding Register, or the Interrupt Enable Register.

NOTE: This feature enables the CPU to alert a terminal in a computer communications system. If the following sequence is followed, no erroneous or extraneous characters will be transmitted because of the break.

1. Load an all 0's pad character in response to THRE.
2. Set break in response to the next THRE.
3. Wait for the Transmitter to be idle. (TSRE = 1), and clear break when normal transmission has to be restored.

During the break, the Transmitter can be used as a character timer to accurately establish the break duration.

MODEM CONTROL REGISTER (MCR) **UART SECTION**

STNDLN:	**0**	**1**
ADDRESS:	**UA2 - UA0 = 100**	**UA3 - UA0 = 0100**

The MCR register controls the interface with the modem. Bits D1 and D0 are also available as read only bits in the UART Control Register in the Modem Registers. In single-port mode, bits D1 and D0 are available inverted at the $\overline{RTS}$ and $\overline{DTR}$ pins.

BIT NO.	NAME	CONDITION	DESCRIPTION
D0	DTR	1	This bit controls the Data Terminal Ready ($\overline{DTR}$) output. When bit 0 is set to a logic 1, the $\overline{DTR}$ output is forced to a logic 0. When bit 0 is reset to a logic 0, the $\overline{DTR}$ output is forced to a logic 1.
D1	RTS	1	This bit controls the Request to Send ($\overline{RTS}$) output. When bit 1 is set to a logic 1, the $\overline{RTS}$ output is forced to a logic 0. When bit 1 is reset to a logic 0, the $\overline{RTS}$ output is forced to a logic 1.
D2	µPRST* (OUT1 in 16C450)	1	In single-port mode inactive unless loop = 1, then functions as below (D4). In dual-port mode the mPRST pin is the logical OR of this bit and the RESET pin.
D3	Enable Interrupt (OUT2 in 16C450)	0	Sets INTRPT pin to high impedance if STNDLN = 1.
		1	INTRPT output enabled.
D4	LOOP	1	This bit provides a local loopback feature for diagnostic testing of the UART portion of the SSI 73K222U. When bit D4 is set to logic 1, the following occurs: 1. TXD is forced to mark, RXD is ignored. 2. The output of the Transmitter is looped to the Receiver. 3. The four modem control inputs to the UART ($\overline{CTS}$, $\overline{DSR}$, $\overline{DCD}$, and $\overline{RI}$) are ignored and the UART signals $\overline{RTS}$, $\overline{DTR}$, Enable Interrupt, and mPRST are forced inactive. 4. The UART signals RTS, DTR, Enable Interrupt, and mPRST are internally connected to the four control signals CTS, DSR, DCD and RI respectively. Note that the Modem Status Register Interrupts are now controlled by the lower four bits of the Modem Control Register. The interrupts are still controlled by the Interrupt Enable Register.
D5 - D7		0	These bits are permanently set to logic 0.

* Note: The µPRST bit has an upgraded function which was not included in the initial definition of the SSI 73K222U.

LINE STATUS REGISTER (LSR)
STNDLN: 0 1
ADDRESS: UA2 - UA0 = 101 UA3 - UA0 = 0101

UART SECTION

This register provides status information to the CPU concerning the data transfer.

BIT NO.	NAME	CONDITION	DESCRIPTION
D0	DR	1	The Data Ready (DR) bit is set to a 1 whenever a complete incoming character has been received and transferred into the Receiver Buffer Register. Data Ready is reset to 0 by reading the data in the Receiver Buffer Register or by writing a 0 into it from the processor.
D1	OE	1	The Overrun Error (OE) bit indicates that the data in the Receiver Buffer Register was not read by the CPU before the next character was transferred into the Receiver Buffer Register, thereby destroying the previous character. The OE indicator is reset whenever the CPU reads the contents of the Line Status Register.
D2	PE	1	The Parity Error (PE) bit indicates that the received character did not have the correct parity. The bit is reset to 0 whenever the CPU reads the Line Status Register.
D3	FE	1	The Framing Error (FE) bit indicates that the received character did not have a valid stop bit. The FE indicator is reset whenever the CPU reads the contents of the Line Status Register. A framing error will not occur in DPSK receive from the modem due to the fact that missing stop bits are reinserted.
D4	BI	1	The Break Interrupt (BI) bit indicates that a break has been received. A break occurs whenever the received data is held to 0 for a full data word (start + data + stop) or for two full data words when receiving in DPSK mode from the modem. The BI bit is reset to 0 whenever the CPU reads the Line Status Register.
D5	THRE	1	The Transmit Holding Register Empty (THRE) indicates that the Transmitter is ready to accept a new character for transmission. The THRE bit is reset when the CPU loads a character into the Transmit Holding Register.
D6	TSRE	1	The Transmit Shift Empty (TSRE) indicates that both the Transmit Holding Register and the Transmit Shift Registers are empty.
D7	-	0	Always zero.

MODEM STATUS REGISTER (MSR) (READ ONLY)

UART SECTION

STNDLN: 0 1

ADDRESS: UA2 - UA0 = 110 UA3 - UA0 = 0110

This register provides the current state of the control signals from the modem. In addition, four bits provide change information. The CTS, DSR, DCD, and RI signals come from the UART Control Register if STNDLN = 0 and from the $\overline{CTS}$, $\overline{DSR}$, $\overline{DCD}$ and $\overline{RI}$ pins (inverted) if STNDLN = 1. This register is READ ONLY. The delta bits indicate whether the inputs have changed since the last time the Modem Status Register has been read. In Loop Mode CTS, DSR, RI and DCD are taken from RTS, DTR, µPRST, and Enable Interrupt in the Modem Control Register respectively.

BIT NO.	NAME	CONDITION	DESCRIPTION
D0	DCTS	1	This bit is the Delta Clear to Send (DCTS) indicator. Bit 0 indicates that the $\overline{CTS}$ input to the chip has changed state since the last time it was read by the CPU.
D1	DDSR	1	This bit is the Delta Data Set Ready (DDSR) indicator. Bit 1 indicates that the $\overline{DSR}$ input to the chip has changed state since the last time it was read by the CPU.
D2	TERI	1	This bit is the Trailing Edge of the Ring Indicator (TERI) detector. Bit 2 indicates that the $\overline{RI}$ input to the chip has changed state.
D3	DDCD	1	This bit is the Delta Data Carrier Detect (DDCD) indicator. Bit 3 indicates that the $\overline{DCD}$ input to the chip has changed state.
D4	CTS	1	This bit is the complement of the Clear To Send ($\overline{CTS}$) input. If STNDLN = 0, this reflects the status of the UART Control Register bit. If bit 4 (loop) of the MCR is set to a 1, this bit is equivalent to RTS in the MCR.
D5	DSR	1	This bit is the complement of the Data Set Ready ($\overline{DSR}$) input. If STNDLN = 0, this reflects the status of the UART Control Register bit. If bit 4 of the MCR is set to a 1, this bit is the equivalent of DTR in the MCR.
D6	RI	1	This bit is the complement of the Ring Indicator ($\overline{RI}$) input. If STNDLN = 0, this reflects the status of the UART Control Register bit. If bit 4 of the MCR is set to a 1, this bit is equivalent to mPRST in the MCR.
D7	DCD	1	This bit is the complement of the Data Carrier Detect ($\overline{DCD}$) If STNDLN = 0, this reflects the status of the UART Control Register bit. If bit 4 of the MCR is set to a 1, this bit is equivalent to Enable Interrupt in the MCR.

SCRATCH REGISTER (SCR)

STNDLN:	**0**	**1**
ADDRESS:	**UA2 - UA0 = 111**	**UA3 - UA0 = 0111**

The Scratch Register is a dual port register which can be simultaneously accessed through both the UART bus and the modem bus.This provides the possibility for the modem controller to communicate directly with the central CPU. Note that if both processors write the Scratch Register, the data stored will be from whichever processor last wrote the register.

DIVISOR LATCH (Least significant byte) (DLL)

STNDLN:	**0**	**1**
ADDRESS:	**UA2 - UA0 = 000, DLAB = 1**	**UA3 - UA0 = 0000, DLAB = 1**

DIVISOR LATCH (Most significant byte) (DLM)

STNDLN:	**0**	**1**
ADDRESS:	**UA2 - UA0 = 001, DLAB = 1**	**UA3 - UA0 = 0001, DLAB = 1**

DIVISOR LATCH VALUE VS. DATA RATE

The Divisor Latch is two 8-bit write only registers which control the rate of the programmable baud generator. The programmable baud generator generates an output clock by dividing an internal 1.8432 MHz clock by the value stored in the divisor latch. This output clock has a value of 16X the data rate at which the modem will operate. This output clock is available at pin 21 under the control of bit 3 (D3) of the Modem Control Register 1. Upon loading either of the Divisor Latches the 16-bit device counter is immediately loaded, preventing long counts on initial load. The following table shows divisor values for common data rates.

DESIRED DATA RATE	DIVISOR USED FOR 16 x DATA RATE CLOCK	% ERROR GENERATED	DESIRED DATA RATE	DIVISOR USED FOR 16 x DATA RATE CLOCK	% ERROR GENERATED
50 [1]	2304		4800	24	
75 [1]	1536		7200	16	
110 [1]	1047		9600	12	
134.5 [1]	857	0.058	19200	6	
159 [1]	768		38400	3	
300 [1]	384		56000	2	2.86
600 [2]	192				
1200 [3]	96				
1800	64				
2000	58	0.69			
2400	48				
3600	32				

1. Data Rate valid for FSK transmission.
2. Data Rate valid for halfspeed DPSK transmission.
3. Data Rate valid for normal 1200 bit/s DPSK transmission.

MODEM REGISTER BIT DESCRIPTIONS

MODEM SECTION

CONTROL REGISTER (CR0)
STNDLN: 0 1
ADDRESS: MA2 - MA0 = 000 UA3 - UA0 = 1000

BIT NO.	NAME	CONDITION		DESCRIPTION
D0	Answer/Originate	0		Selects Answer Mode (transmit in high band, receive in low band).
		1		Selects Originate Mode (transmit in low band, receive in high band).
D1	Transmit Enable	0		Disables transmit output at TXA.
		1		Enables transmit output at TXA. NOTE: Answer tone and DTMF TX control require Transmit Enable. If Transmit Enable is on, call progress and answer tone detector interrupts are masked.
D2, D3	Character Size 0, 1			These bits are read only. These bits represent the character size. The character size is determined by the UART Line Control Register and includes data, parity (if used), one start bit, and one stop bit.
		D3	D2	Character length
		0	0	8-bit character
		0	1	9-bit character
		1	0	10-bit character
		1	1	11-bit character
D4	Power ON			This bit controls the power down mode of the SSI 73K222U, the analog, and most digital portions of the chip. The digital interface is active during power down.
		0		Power down mode.
		1		Normal operation.
D5	Modulation Mode	0		DPSK
		1		FSK
D6	Reserved	0		Must be written as zero.
D7	Modulation Option	0		DPSK: 1200 bit/s
		1		600 bit/s
		0		FSK: 103 mode
		1		V.21 mode

CONTROL REGISTER (CR1)
STNDLN: 0 1
ADDRESS: MA2 - MA0 = 001 UA3 - UA0 = 1001

MODEM SECTION

BIT NO.	NAME	CONDITION		DESCRIPTION
D0, D1	Test Mode	D1	D0	
		0	0	Selects normal operating mode.
		0	1	Analog Loopback Mode. Loops the transmitted analog signal back to the receiver, and causes the receiver to use the same center frequency as the Transmitter. To squelch the TXA pin, transmit enable bit must be forced low.
		1	0	Selects remote digital loopback. Received data is looped back to transmit data internally, and RXD is forced to a mark. Data in TXD is ignored.
		1	1	Selects half-duplex. Internally performs a logical AND of TXD and RXD to send to the UART receiver. Both transmit and receive characters will occur at the Receiver Buffer Register.
D2	Reset	0		Selects normal operation.
		1		Resets modem to power down state. All Control Register bits (CR0, CR1, TONE) are reset to zero. The output of the clock pin will be set to the crystal frequency.
D3	CLK Control (Clock Control)	0		CLK pin output is selected to be an 11.0592 MHz crystal echo output.
		1		CLK pin output is selected to be 16 x the Data Rate set by the UART divisor latch.
D4	Bypass Scrambler	0		Selects normal operation. DPSK data is passed through scrambler.
		1		Selects Scrambler Bypass. DPSK data is routed around scrambler in the transmit path.

CONTROL REGISTER (CR1) (continued)

MODEM SECTION

BIT NO.	NAME	CONDITION		DESCRIPTION
D5	Enable Detect Interrupt	0		Disables interrupts generated by Detect Register bits D1 - D4 at INT pin in dual-port mode, or at INTRPT pin in single-port mode. All interrupts normally disabled in power down modes.
		1		Enables interrupts generated by Detect Register bits D1 - D4 at $\overline{INT}$ pin in dual-port mode, or at INTRPT pin in single-port mode. An interrupt will be generated with a change in status of DR bits D1 - D4. The answer tone and call progress detect interrupts are masked when the TX enable bit is set. Carrier detect is masked when TX DTMF is activated. All interrupts will be disabled if the device is in power down mode. The interrupt is reset when the DR register is read.
D6, D7	Transmit Pattern	D7	D6	
		0	0	Selects normal data transmission as controlled by the state of the TXD pin.
		0	1	Selects an alternating mark/space transmit pattern for modem testing.
		1	0	Selects a constant mark transmit pattern.
		1	1	Selects a constant space transmit pattern.

DETECT REGISTER (DR)
STNDLN: 0 1
ADDRESS: MA2 - MA0 = 010 UA3 - UA0 = 1010

BIT NO.	NAME	CONDITION		DESCRIPTION
D0	Long Loop	0		Indicates normal received signal.
		1		Indicates low received signal level (< -38 dBm).
D1	Call Progress Detect	0		No call progress tone detected.
		1		Indicates presence of call progress tones. The call progress detection circuitry is activated by energy in the normal 350 to 620 Hz call progress bandwidth.
D2	Answer Tone Received	0		No answer tone detected.
		1		Indicates detection of 2225 Hz answer tone in Bell mode or 2100 Hz in CCITT mode. The device must be in Originate Mode for detection of answer tone for normal operation. For CCITT answer tone detection, bit D0 of the Tone Register must be set.
D3	Carrier Detect	0		No carrier detected in the receive channel.
		1		Carrier has been detected in the receive channel.
D4	Unscrambled Marks	0		No unscrambled mark detected.
		1		Indicates detection of unscrambled marks in the received data. A valid indication requires that unscrambled marks be received for > 165.5 ± 13.5 ms.
D5	Receive Data			Continuously outputs the received data stream. This data is the same as that output on the RXD pin, but it is not disabled when RXD is tri-stated.
D6, D7	Device Signature 0, 1	D7	D6	Product Identified
		0	0	SSI 73K212U (special order only)
		0	1	SSI 73K221U (special order only)
		1	0	SSI 73K222U

TONE CONTROL REGISTER (TONE)
STNDLN: 0 1
ADDRESS: MA2 - MA0 = 011 UA3 - UA0 = 1011

MODEM SECTION

The Tone Control Register contains information on the tones that are transmitted. Tones are transmitted only if the Transmit Enable bit is set. The priority of the transmit tones are: 1) DTMF, 2) Answer, 3) FSK, 4) Guard.

BIT NO.	NAME	CONDITION				DESCRIPTION
D0	DTMF 0 / Answer/ Guard Tone	D6	D5	D4	D0	D0 interacts with bits D6, D5, and D4 as shown:
		X	X	1	X	Transmit DTMF tones.
		X	1	0	0	Select 2225 Hz answer tone (Bell).
		X	1	0	1	Select 2100 Hz answer tone (CCITT).
		1	0	0	0	Select 1800 Hz guard tone.
		1	0	0	1	Select 550 Hz guard tone.
D0, D1, D2, D3	DTMF	Table below				Programs 1 of 16 DTMF tone pairs that will be transmitted when TX DTMF and TX enable bit (CR0, bit D1) is set. Tone encoding is shown below.

KEYBOARD EQUIVALENT	DTMF CODE D3 D2 D1 D0	TONES LOW	TONES HIGH
1	0 0 0 1	697	1209
2	0 0 1 0	697	1336
3	0 0 1 1	697	1477
4	0 1 0 0	770	1209
5	0 1 0 1	770	1336
6	0 1 1 0	770	1477
7	0 1 1 1	852	1209
8	1 0 0 0	852	1336
9	1 0 0 1	852	1477
0	1 0 1 0	941	1336
*	1 0 1 1	941	1209
#	1 1 0 0	941	1477
A	1 1 0 1	697	1633
B	1 1 1 0	770	1633
C	1 1 1 1	852	1633
D	0 0 0 0	941	1633

TONE CONTROL REGISTER (TONE) (continued)

BIT NO.	NAME	CONDITION		DESCRIPTION
D4	TX DTMF (Transmit DTMF)	0		Disable DTMF.
		1		Activates DTMF. The selected DTMF tones are transmitted continuously when this bit is high. TX DTMF overrides all other transmit functions.
D5	TX ANS (Transmit Answer Tone)	D5	D0	D5 interacts with bit D0 as shown.
		0	X	Disables answer tone generator.
		1	0	Enables answer tone generator. A 2225 Hz answer tone will be transmitted continuously when the transmit enable bit is set. The device must be in answer mode.
		1	1	Enables a 2100Hz answer tone generator, with operation same as above.
D6	TX Guard (Transmit Guard Tone)	0		Disables guard tone generator.
		1		Enables guard tone generator. (See D0 for selection of guard tones).
D7	RXD/TXD Control	STNDLN	D7	Function is dependant on status of STNDLN pin.
		0	0	RXD is output data received by modem, TXD is serial output of UART.
		1	0	RXD is electrically an input, but the signal is ignored, TXD is forced to a mark.
		X	1	RXD is serial input to UART, TXD is serial output of UART.

CONTROL REGISTER (CR3)
STNDLN: 0 1
ADDRESS: MA2 - MA0 = 101 UA3 - UA0 = 1101

D0 - D4	Not Used			Not presently used.
D5	Off Hook	0		Relay driver open.
		1		Open drain driver pulling low.
D6, D7	Speaker Volume 0, 1	D7	D6	Speaker volume control status.
		0	0	Speaker off
		0	1	-24 dB
		1	0	-12 dB
		1	1	0 dB

SCRATCH REGISTER (SCR)
STNDLN: 0 1
ADDRESS: MA2 - MA0 = 110 UA3 - UA0 = 1110

The Scratch Register is a dual-port register which can be accessed either through the UART bus or the modem bus. It can be used for a communication path outside the data stream.

UART CONTROL REGISTER (UCR)
STNDLN: 0 1
ADDRESS: MA2 - MA0 = 111 UA3 - UA0 = 1111

The UART Control Register contains the handshaking signals necessary for the microprocessor to communicate with the central CPU through the UART.

BIT NO.	NAME	CONDITION	DESCRIPTION
D0	CTS	1	In dual-port mode, CTS, DSR, DCD and RI are writeable locations which can be read through the 16C450 port in the Modem Status Register.
D1	DSR	1	
D2	DCD	1	In the single-port mode, D0 - D3 are ignored and the information for the Modem Status Register comes directly from the external pins.
D3	RI	1	
D4	DTR	1	
D5	RTS	1	DTR and RTS are read only versions of the same register bits in the Modem Contol Register.
D6	Not Used		
D7	TXCLK	Clock	TXCLK is the clock that the UART puts out with TXD. The falling edge of TXCLK is coincident with the transitions of data on TXD. TXCLK can also be used for the microprocessor to send synchronous data independent of the UART by forcing data patterns using CR1 bits 6 and 7 before the rising edge of TXCLK.
NOTE: Control Register 2 (CR2) is reserved for future products and is disabled.			

ELECTRICAL SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

TA = -40°C to 85°C, VDD = 5V ± 10%, unless otherwise noted.

PARAMETER	RATING	UNIT
VDD Supply Voltage	7	V
Storage Temperature	-65 to 150	°C
Soldering Temperature (10 sec.)	260	°C
Applied Voltage	-0.3 to VDD +0.3	V
NOTE: All inputs and outputs are protected from static charge using built-in, industry standard protection devices and all outputs are short-circuit protected.		

RECOMMENDED OPERATING CONDITIONS

PARAMETER	CONDITION	MIN	NOM	MAX	UNIT
VDD, Supply Voltage		4.5	5	5.5	V
TA, Operating Free-Air Temperature		-40		85	°C
External Component (Refer to application drawing for placement.)					
VREF Bypass Capacitor [2]	(VREF to GND)	0.1			µF
Bias Setting Resistor [1]	(Placed between VDD and ISET pins)	1.8	2	2.2	MΩ
ISET Bypass Capacitor [2]	ISET pin to GND	0.1			µF
VDD Bypass Capacitor [2]	(VDD to GND)	0.1			µF
XTL1 Load Capacitor	From pin to GND			40	pF
XTL2 Load Capacitor	From pin to GND			20	pF
Input Clock Variation	(11.0592 MHz)	-0.01		+0.01	%
Hybrid Loading					
R1	See Figure 3		600		Ω
R2			600		Ω
C	TXA Hybrid Loading		0.033		µF

1. Optional for minimum worst case current consumption.
2. Minimum for optimized system layout; may require higher values for noisy environments.

DC ELECTRICAL CHARACTERISTICS

TA = -40°C to +85 °C, VDD = 5V ± 10%, unless otherwise noted.

PARAMETER		CONDITION		MIN	NOM	MAX	UNIT
IDD, Supply Current							
IDDA, Active		ISET Resistor = 2 MΩ			8	12	mA
IDDA, Active		ISET = GND			8	15	mA
IDD1, Power-Down		CLK = 11.0592 MHz			3	4	mA
IDD2, Power-Down		CLK = 19.200 kHz			2	3	mA
Digital Inputs							
Input High Current	IIH	VI = VDD				100	µA
Input Low Current	IIL	VI = 0		-200			µA
Input Low Voltage	VIL					0.8	V
Input High Voltage	VIH	Except RESET & XTL1		2.0			V
Input High Voltage	VIH	RESET & XTL1		3.0			V
Pull Down Current	RESET PIN			5		30	µA
Input Capacitance						10	pF
Digital Outputs							
Output High Voltage	VOH	IOUT = - 1 mA		2.4		VDD	V
VOL UD0-UD7 and INTRPT		IOUT = 3.2 mA				0.4	V
VOL other outputs		IOUT = 1.6 mA				0.4	V
CLK Output	VOL	IOUT = 3.2 mA				0.6	V
OH Output	VOL	IOUT = 20 mA				1.0	V
OH Output	VOL	IOUT = 10 mA				0.5	V
Offstate Current INTRPT pin		VO = 0V		-20		20	µA
Capacitance							
Inputs		Input Capacitance				10	pF
CLK		Maximum capacitive load to pin				15	pF
Analog Pins							
RXA Input Resistance					200		kΩ
RXA Input Capacitance						25	pF

ELECTRICAL SPECIFICATIONS (continued)

DYNAMIC CHARACTERISTICS AND TIMING

TA = -40°C to +85°C, VDD = 5V ± 10%, unless otherwise noted.

PARAMETER	CONDITION	MIN	NOM	MAX	UNIT
DPSK Modulator					
Carrier Suppression	Measured at TXA	55			dB
Output Amplitude	ANS TONE 2225 or 2100 Hz	-11	-10.0	-9	dBm0[1]
	DPSK TX Scrambled Marks	-11	-10.0	-9	dBm0
	FSK Dotting Pattern	-11	-10.0	-9	dBm0
FSK Tone Error	Bell 103 or V.21			±5	Hz
DTMF Generator					
Freq. Accuracy		-.25		.25	%
Output Amplitude	Low Band, not in V.21 mode	-10	-9	-8	dBm0
Output Amplitude	High Band, not in V.21 mode	-8	-7	-6	dBm0
Long Loop Detect	DPSK or FSK	-40		-32	dBm0
Demodulator Dynamic Range	DPSK or FSK		45		dB
Call Progress Detector					
Detect Level	2-Tones in 350-600 Hz Band	-39		0	dBm0
Reject Level	2-Tones in 350-600 Hz Band			-46	dBm0
Delay Time	-70 dBm0 to -30 dBm0 Step	27		80	ms
Hold Time	-30 dBm0 to -70 dBm0 Step	27		80	ms
Hysteresis		2			dB
Carrier Detect					
Threshold	DPSK or FSK Receive Data	-49		-42	dBm0
Delay Time	-70 dBm0 to -30 dBm0 Step	15		45	ms
Hysteresis		2	3.0		dB
Hold Time	-30 dBm0 to -70 dBm0 Step	10		24	ms
Answer Tone Detector					
Detect Level Threshold	In FSK mode	-49.5		-42	dBm0
Delay Time	-70 dBm0 to -30 dBm0 Step	20		45	ms
Hold Time	-30 dBm0 to -70 dBm0 Step	10		30	ms
Detect Frequency Range		-2.5		+2.5	%

1. All units in dBm0 are measured at the line input to the transformer. The interface circuit inserts an 8 dB loss in the transmit path (TXA1 - TXA2 to line), and a 3 dB loss in the receive path (line to RXA).

DYNAMIC CHARACTERISTICS AND TIMING (continued)

PARAMETER	CONDITION	MIN	NOM	MAX	UNIT
Speaker Output					
Gain Error		-1		+1	dB
Output Swing SPKR	10K||50 pF LOAD 5% THD	2.75			VP
Carrier VCO					
Capture Range	Originate or Answer	-10		10	Hz
Capture Time	-10 Hz to +10 Hz Carrier Frequency change assumed		40	100	ms
Recovered Clock					
Capture Range	% of Center Frequency	-625		+625	ppm
Data Delay Time	Analog data in at RXA pin to receive data valid at RXD pin.		30	50	ms
Guard Tone Generator					
Tone Accuracy	550 or 1800 Hz	-20		+20	Hz
Tone Level	550 HZ	-4.0	-3.0	-2.0	dB
(Below DPSK Output)	1800 HZ	-7.0	-6.0	-5.0	dB
Harmonic Distortion	700 to 2900 HZ			-60	dB

SERIAL BUS INTERFACE (See Figure 4)
The following times are for CL = 100 pF.

PARAMETER		MIN	NOM	MAX	UNIT
TRD	Data out from Read	0		140	ns
TCKD	Data out after Clock			200	ns
TRDF	Data Float after Read	0		200	ns
TRCK	Clock High after Read	200			ns
TWW	Write Width	140		10000	ns
TDCK	Data Setup Before Clock	150			ns
TCKH	Data Hold after Clock	20			ns
TCKW	Write after Clock	150			ns
TACR	Address setup before Control [1]	50			ns
TCAR	Address Hold after Control [1]	50			ns
TACW	Address setup before Write	50			ns
TCAW	Address Hold after Write	50			ns

1. Control is later of falling edge of RD or DCLK.

ELECTRICAL SPECIFICATIONS (continued)

PARALLEL BUS INTERFACE (See Figure 5) The following times are for CI = 100 pF.

PARAMETER		MIN	MAX	MIN	MAX	UNIT
		Dual-Port Mode		Single-Port Mode		
RC	Read Cycle = TAD + TRC	240		340		ns
TDIW	DISTR Width	80		80		ns
TDDD	Delay DISTR to Data (read time)		80		80	ns
THZ**	DISTR to Floating Data Delay	0	50	0	50	ns
TRA	Address Hold after DISTR	20		5		ns
TRCS	Chip select hold after DISTR	20		20		ns
TAR*	DISTR Delay after Address	20		15		ns
TCSR	DISTR Delay after Chip Select	20		20		ns
WC	Write Cycle = TAW + TDOW + TWC	140		140		ns
TDOW	DOSTR Width	80		80		ns
TDS	Data Setup	30		50		ns
TDH**	Data Hold	20		20		ns
TWA	Address Hold after DOSTR	20		5		ns
TWCS	Chip select hold after DOSTR	20		20		ns
TAW*	DOSTR delay after Address	20		15		ns
TCSW	DOSTR delay after Chip Select	20		20		ns
TADS	Address Strobe Width			40		ns
TAS	Address Setup Time			30		ns
TAH	Address Hold Time			0		ns
TCS	Chip Select Setup Time			30		ns
TCH	Chip Select Hold Time			0		ns
TRC	Read Cycle Delay	40		40		ns
TWC	Write Cycle Delay	40		40		ns
TAD	Address to Read Data	200		300		ns

* TAR and TAW are referenced from the falling edge of either $\overline{CS2}$ or $\overline{DISTR}$ or $\overline{DOSTR}$, whichever is later.

** THZ and TDH are referenced from the rising edge of $\overline{CS2}$ or $\overline{DISTR}$ or $\overline{DOSTR}$, whichever is earlier.

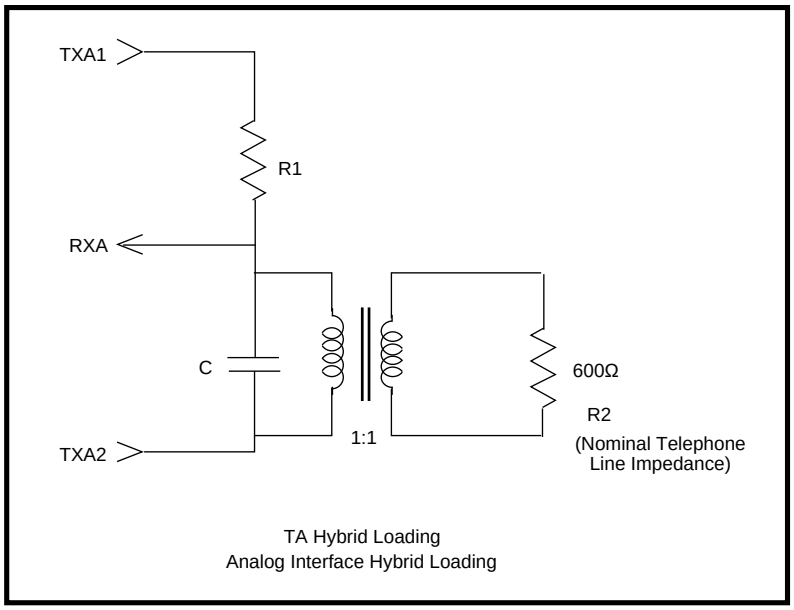


FIGURE 3: TXA Hybrid Loading Analog Interface Hybrid Loading

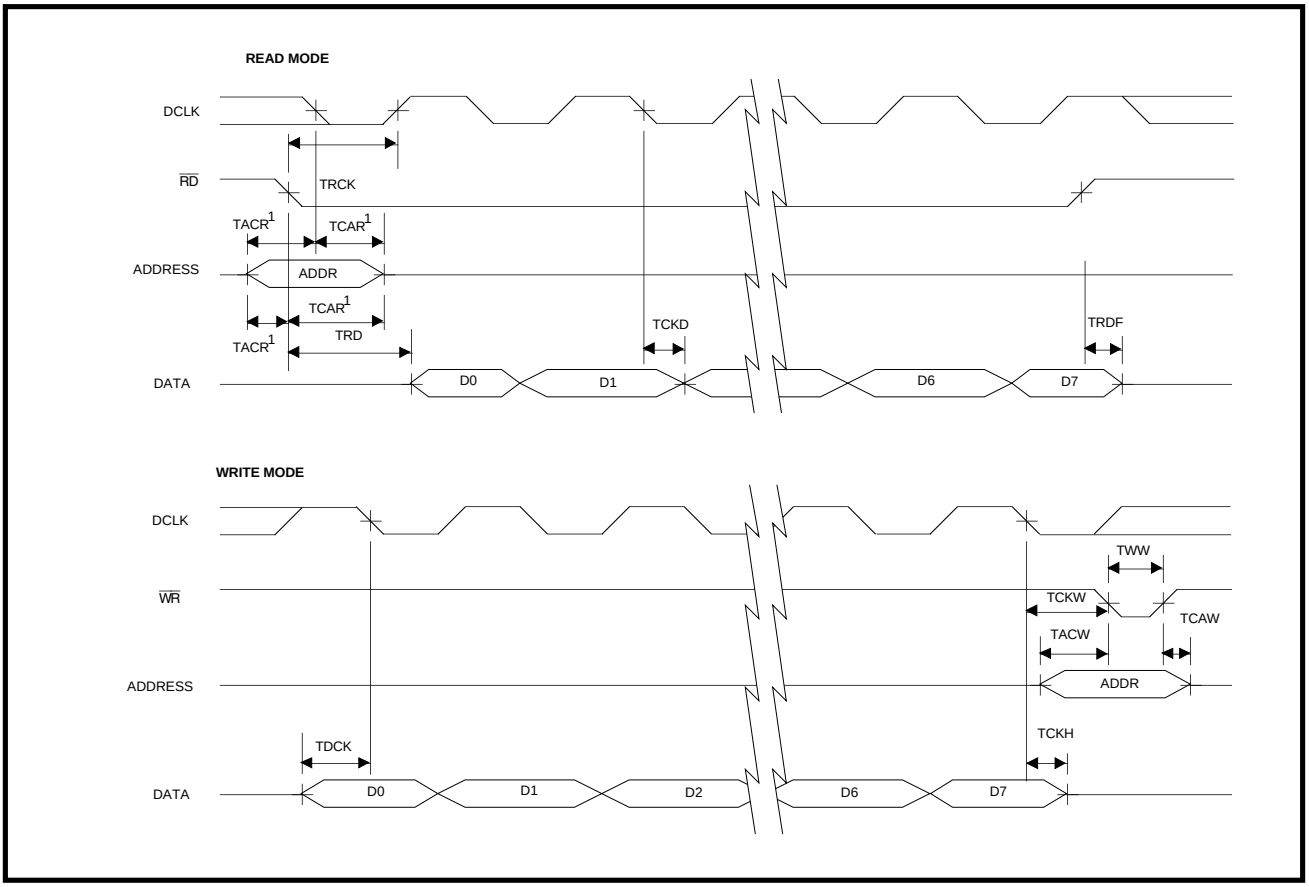


FIGURE 4: Modem Serial Bus Timing

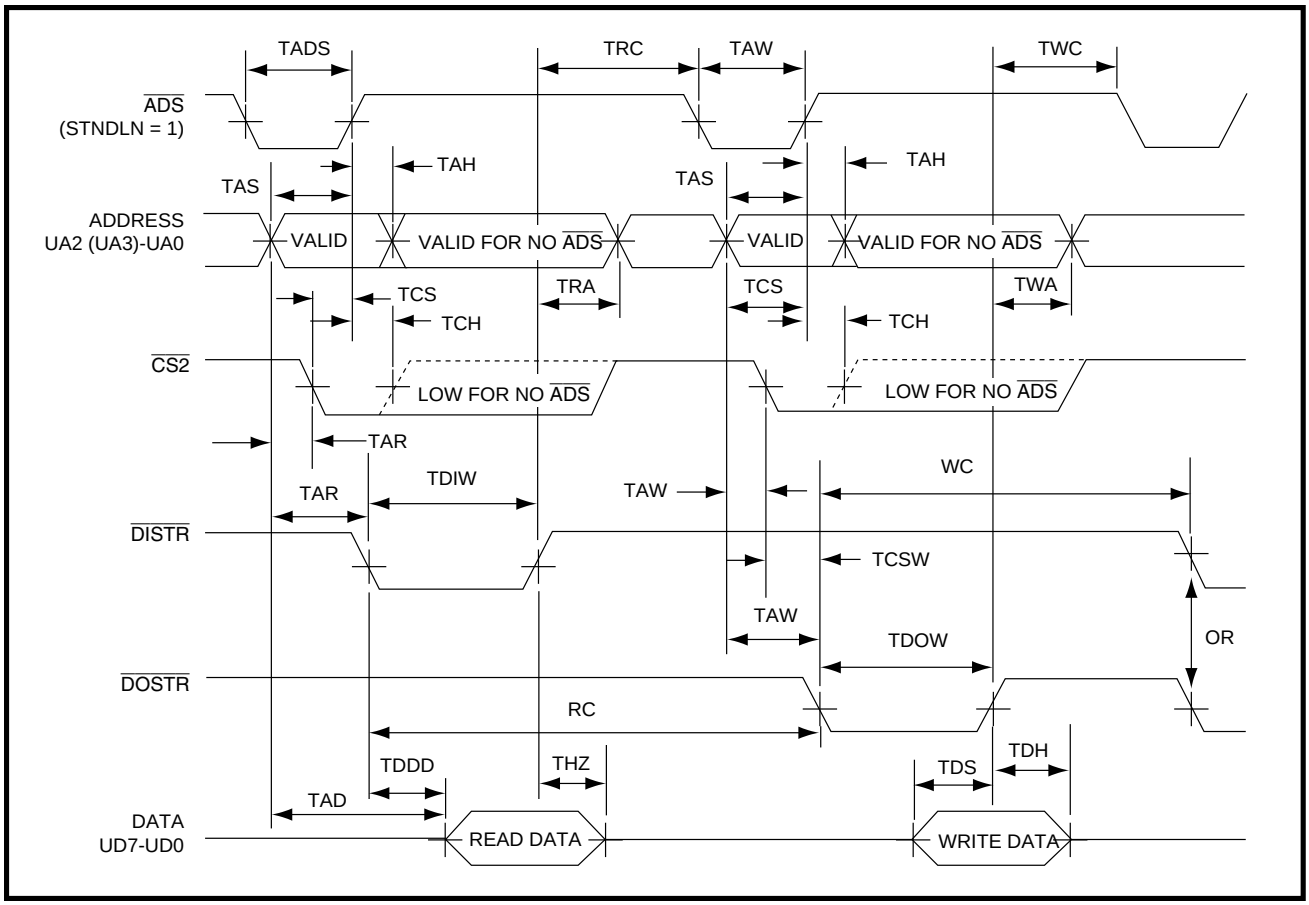


FIGURE 5: UART Bus Timing

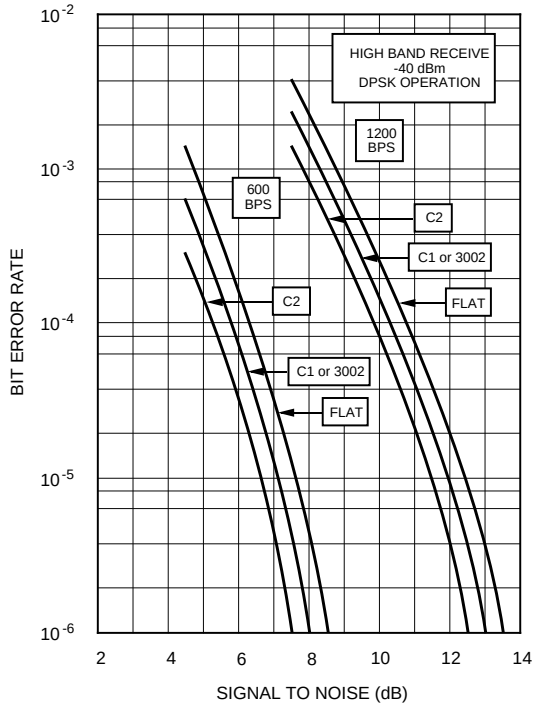
TYPICAL PERFORMANCE CHARACTERISTICS

The SSI 73K222U was designed using an integrated analog/digital architecture that offers optimum performance over a wide range of line conditions. The SSI 73K222U utilizes the circuit design proven in SSI's 73K222L one-chip modem, with added enhancements which extend low signal level performance and increase immunity to spurious noise typically encountered in integral bus applications. The SSI 73K222U provides excellent immunity to the types of disturbances present with usage of the dial-up telephone network. The following curves show representative Bit Error Rate performance under various line conditions.

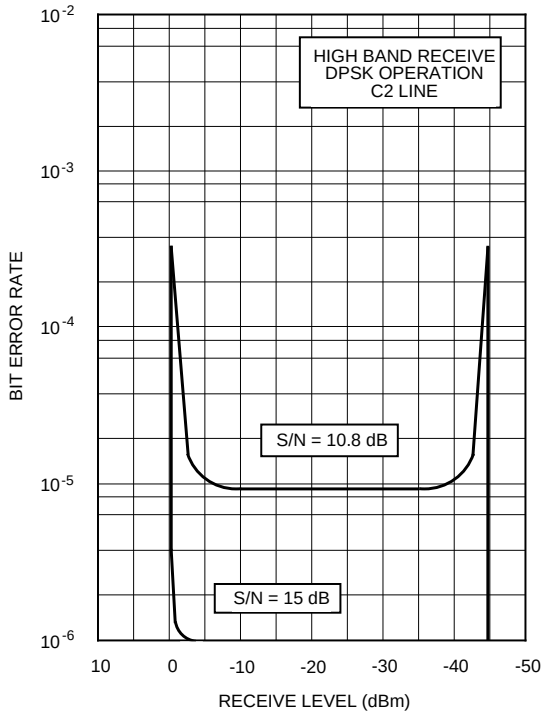
BER vs. S/N

This test measures the ability of the modem to function with minimum errors when operating over noisy lines. Since some noise is generated by even the best dial-up lines, the modem must operate with as low a S/N ratio as possible. Optimum performance is shown by curves that are closest to the zero axis. A narrow spread between curves for the four line conditions indicates minimal variation in performance when operating over a range of line qualities and is typical of high performance adaptive equalization receivers. High band receive data is typically better than low band due to the inherent design of PSK modems.

SSI 73K222U
BER vs S/N



SSI 73K222U
BER vs RECEIVE LEVEL

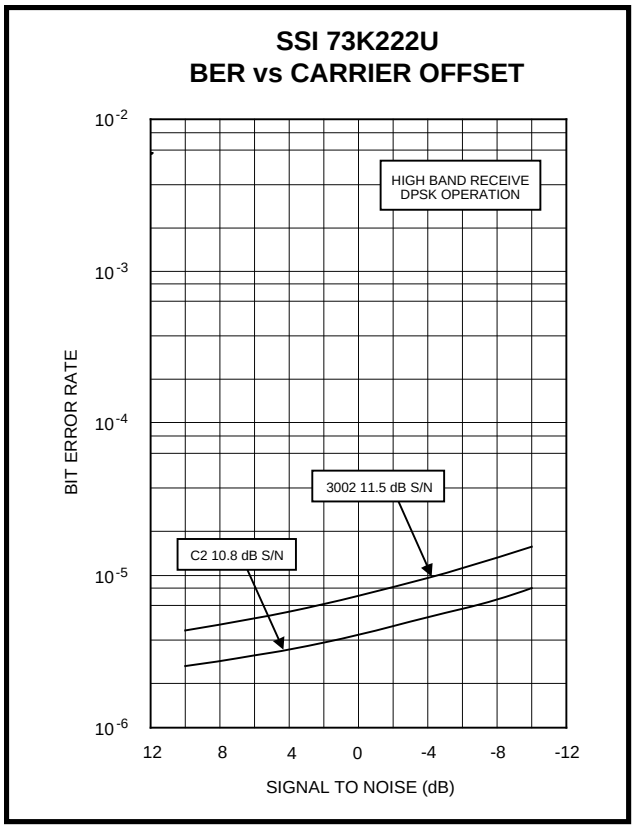


BER vs. Receive Level

This measures the dynamic range of the modem. As signal levels vary widely over dial-up lines, the widest dynamic range possible is desirable. The minimum Bell specification calls for 36 dB of dynamic range. S/N ratios were held constant at the indicated values while receive level was lowered from very high to very low signal levels. The "width of the bowl" of these curves taken at the 10^{-4} BER point is a measure of the dynamic range.

BER vs. Carrier Offset

This parameter indicates how the modem performance is impacted by frequency shifts encountered in normal PSTN operation. Flat curves show no performance degradation from frequency offsets. The SSI K-Series devices use a 2nd order carrier tracking phase-locked-loop, which is insensitive to carrier offsets in excess of 10 Hz. The Bell network specifications allow as much as 7 Hz offset, and the CCITT specifications require modems to operate with 7 Hz of offset.



APPLICATION

The SSI 73K222U includes additional circuitry to greatly simplify integral modem designs in either of two different configurations. The single-port mode represents the most efficient implementation for an integral modem. Figure 9 shows a typical schematic using this mode. In this configuration, the SSI 73K222U transfers data and commands through the single parallel port. All modem control is provided by the main CPU, eliminating the need for an external microcontroller and supporting components. The SSI 73K222U is unique in that access to both the UART and modem sections is possible through the UART port. Also shown is a separate serial port, which can be used independent of the modem function when the modem section is inactive. Figure 10 shows a more conventional integral modem design, in which a local microprocessor handles modem supervision, allowing the modem function to be transparent to the main processor. Inclusion of the hybrid drivers, audio volume control, and off hook relay driver reduces component count for a highly efficient design. In either mode of operation, the SSI 73K222U's ability to operate from a single +5 volt power supply eliminates the need for additional supply voltages and keeps power usage to a minimum.

(See Figure 9 & 10: Typical Integral Applications Single and Dual-Port Modes.)

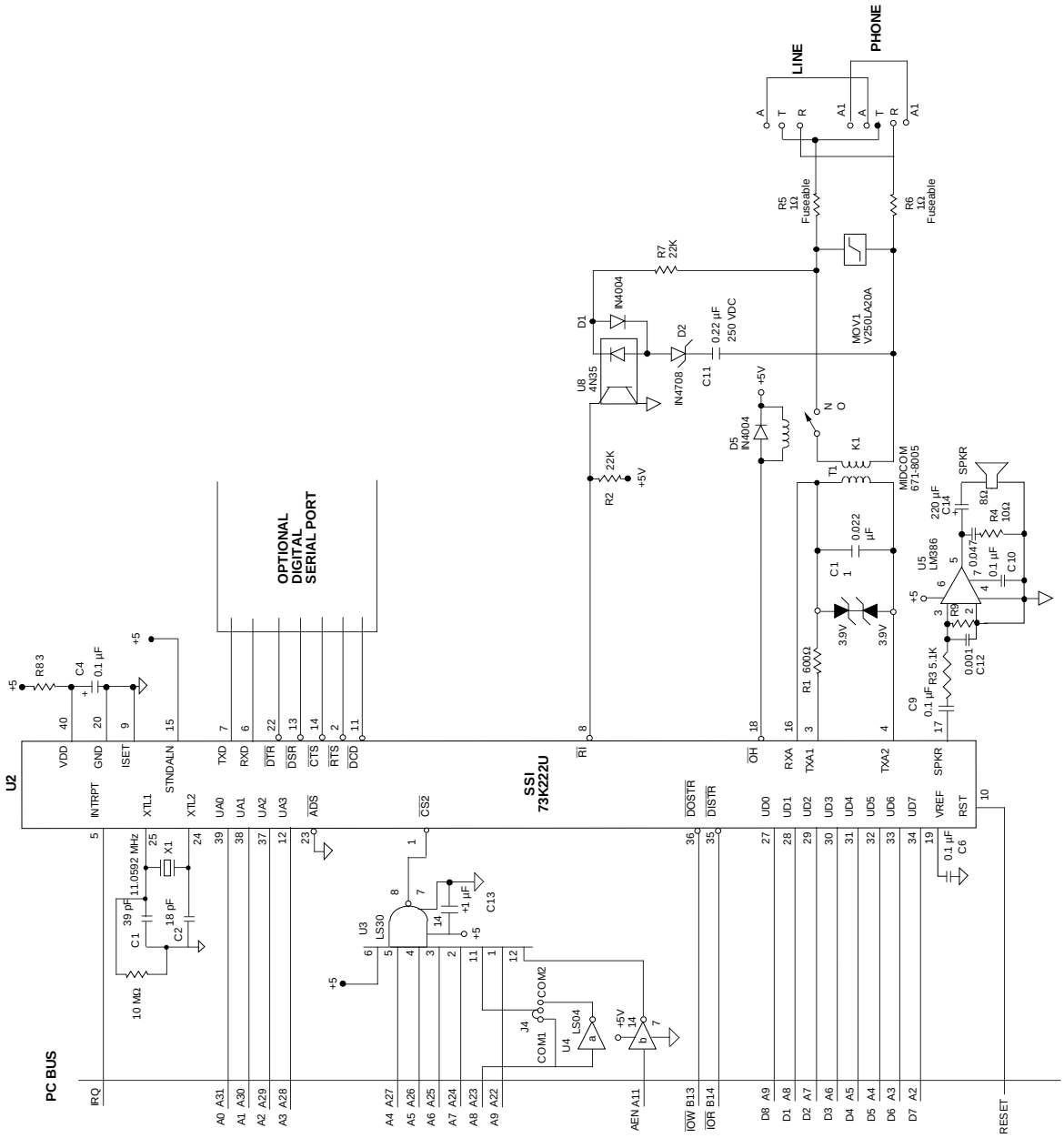


FIGURE 9: 73K222U Typical Integral Application Single-Port Mode

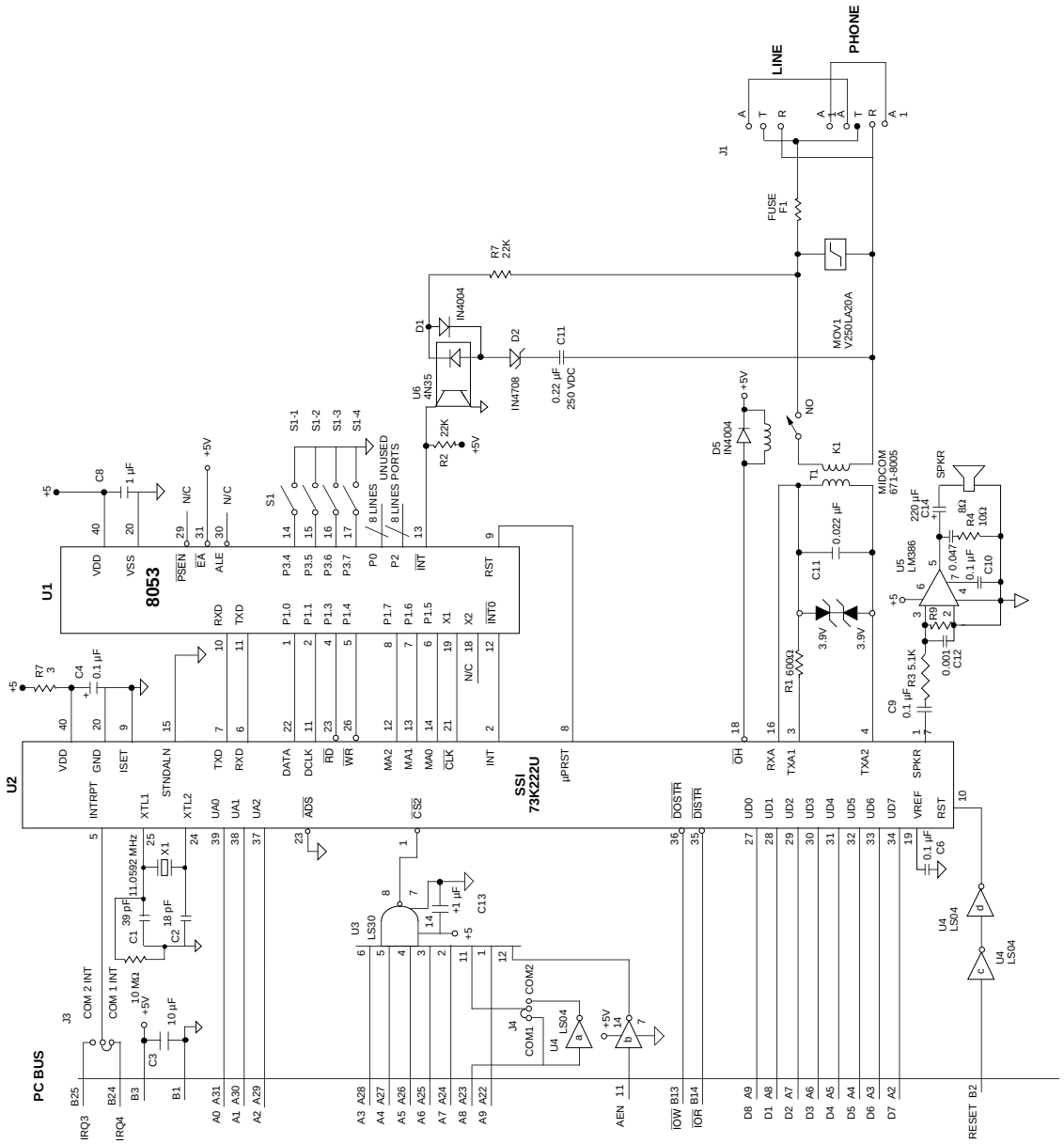
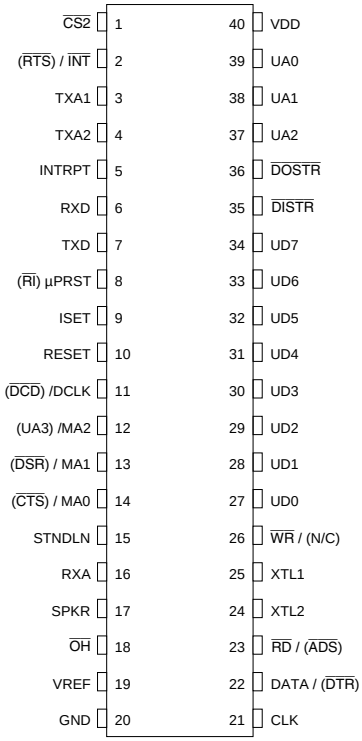


FIGURE 10: 73K222U Typical Integral Application Dual-Port Mode

PACKAGE PIN DESIGNATIONS

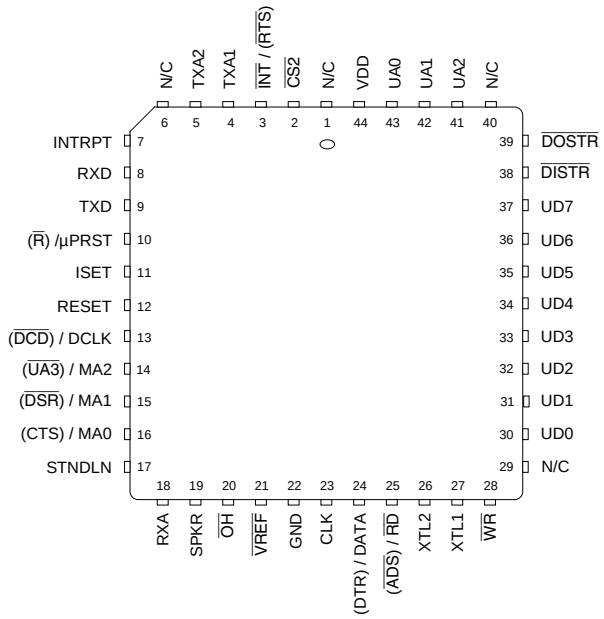
(Top View)



600-Mil
40-Pin DIP

CAUTION: Use handling procedures necessary for a static sensitive component.

Parentheses indicate single-port mode.



44-Pin
PLCC

ORDERING INFORMATION

PART DESCRIPTION	ORDER NO.	PKG. MARK
SSI 73K222U		
40-Pin Plastic Dual In-Line	73K222U-IP	73K222U-IP
44-Pin Plastic Leaded Chip Carrier	73K222U-IH	73K222U-IH

Silicon Systems, Inc. 14351 Myford Road, Tustin, CA 92680-7022, (714) 573-6000, FAX (714) 573-6914

SSI 73K224L
V.22bis/V.22/V.21, Bell 212A/103 Single-Chip Modem

January 1996

DESCRIPTION

The SSI 73K224L is a highly integrated single-chip modem IC which provides the functions needed to construct a V.22bis compatible modem, capable of 2400 bit/s full-duplex operation over dial-up lines. The SSI 73K224L offers excellent performance and a high level of functional integration in a single 28-pin DIP. This device supports V.22bis, V.22, V.21, Bell 212A and Bell 103 modes of operation, allowing both synchronous and asynchronous communication.The SSI 73K224L is designed to appear to the systems designer as a microprocessor peripheral, and will easily interface with popular single-chip microprocessors (80C51 typical) for control of modem functions through its 8-bit multiplexed address/data bus or via an optional serial control bus. An ALE control line simplifies address demultiplexing. Data communications normally occur through a separate serial port. The SSI 73K224L is pin and software compatible with the SSI 73K212L and SSI 73K222L single-chip modem ICs, allowing system upgrades with a single component change.

The SSI 73K224L operates from a single +5V supply for low power consumption.

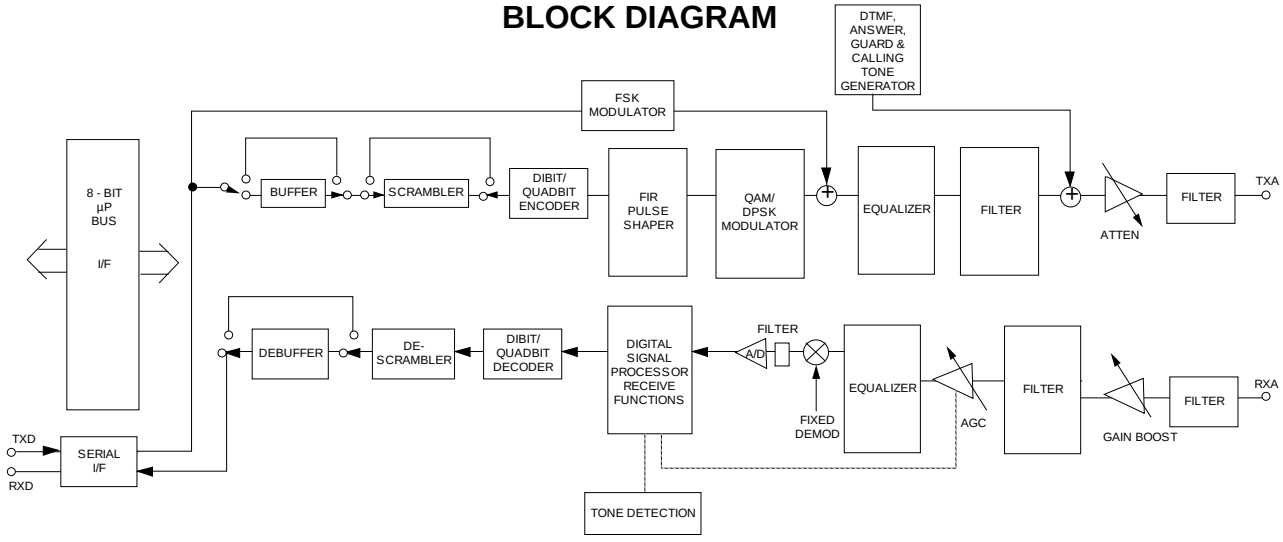
The SSI 73K224L is ideal for use in either free-standing or integral system modem products where full-duplex

(continued)

FEATURES

- **One-chip multi-mode V.22bis/V.22/V.21 and Bell 212A/103 compatible modem data pump**
- **FSK (300 bit/s), DPSK (600, 1200 bit/s), or QAM (2400 bit/s) encoding**
- **Pin and software compatible with other SSI K-Series 1-chip modems**
- **Interfaces directly with standard microprocessors (8048, 80C51 typical)**
- **Parallel microprocessor bus for control with a wide range of package options**
- **Selectable asynch/synch with internal buffer/ debuffer and scrambler/descrambler functions**
- **All synchronous and asynchronous operating modes (internal, external, slave)**
- **Adaptive equalization for optimum performance over all lines**
- **Programmable transmit attenuation (16 dB, 1 dB steps), selectable receive boost (+18 dB)**
- **Call progress, carrier, answer tone, unscrambled mark, S1, and signal quality monitors**
- **DTMF, answer and guard tone generators**
- **Test modes available: ALB, DL, RDL, Mark, Space, Alternating bit, S1 pattern**
- **CMOS technology for low power consumption (typically 100 mW @ 5V) with power-down mode (15 mW @ 5V)**
- **TTL and CMOS compatible inputs and outputs**

BLOCK DIAGRAM



DESCRIPTION (continued)

2400 bit/s data communications over the 2–wire switched telephone network is desired. Its high functionality, low power consumption, and efficient packaging simplify design requirements and increase system reliability.

The SSI 73K224L is designed to be a complete V.22bis compatible modem on a chip. The complete modem requires only the addition of the phone line interface, a control microprocessor, and RS-232 level converter for a typical system. Many functions were included to simplify implementation of typical modem designs. In addition to the basic 2400 bit/s QAM, 600/1200 bit/s DPSK and 300 bit/s FSK modulator/demodulator sections, the device also includes SYNCH/ASYNCH converters, scrambler/descrambler, call progress tone detect, DTMF tone generator capabilities and handshake pattern detectors. V.22bis, V.22, V.21 and Bell 212A/103 modes are supported (synchronous and asynchronous) and test modes are provided for diagnostics. Most functions are selectable as options and logical defaults are provided.

OPERATION

QAM MODULATOR/DEMODULATOR

The SSI 73K224L encodes incoming data into quad-bits represented by 16 possible signal points with specific phase and amplitude levels. The baseband signal is then filtered to reduce intersymbol interference on the bandlimited telephone network. The modulator transmits this encoded data using either a 1200 Hz (originate mode) or 2400 Hz (answer mode) carrier. The demodulator, although more complex, essentially reverses this procedure while also recovering the data clock from the incoming signal. Adaptive equalization corrects for varying line conditions by automatically changing filter parameters to compensate for line characteristics.

DPSK MODULATOR/DEMODULATOR

The SSI 73K224L modulates a serial bit stream into di-bit pairs that are represented by four possible phase shifts as prescribed by the Bell 212A/V.22 standards. The base-band signal is then filtered to reduce intersymbol interference on the bandlimited 2-wire PSTN line. Transmission occurs on either a 1200 Hz (originate mode) or 2400 Hz carrier (answer mode). Demodulation is the reverse of the modulation process, with the incoming analog signal eventually decoded into di-bits and converted back to a serial bit stream. The demodulator also recovers the clock which was encoded into the analog signal during modulation.Demodulation occurs using either a 1200 Hz carrier (answer mode or ALB originate mode) or a 2400 Hz carrier (originate mode or ALB answer mode). Adaptive equalization is also used in DPSK modes for optimum operation with varying line conditions.

FSK MODULATOR/DEMODULATOR

The FSK modulator produces a frequency modulated analog output signal using two discrete frequencies to represent the binary data. The Bell 103 standard frequencies of 1270 and 1070 Hz (originate mark and space) and 2225 and 2025 Hz (answer mark and space) are used when this mode is selected. V.21 mode uses 980 and 1180 Hz (originate, mark and space) or 1650 and 1850 Hz (answer, mark and space). Demodulation involves detecting the received frequencies and decoding them into the appropriate binary value. The rate converter and scrambler/ descrambler are automatically bypassed in the FSK modes.

PASSBAND FILTERS AND EQUALIZERS

High and low band filters are included to shape the amplitude and phase response of the transmit and receive signals and provide compromise delay equalization and rejection of out-of-band signals. Amplitude and phase equalization are necessary to compensate for distortion of the transmission line and to reduce intersymbol interference in the bandlimited receive signal. The transmit signal filtering corresponds to a 75% square root of raised Cosine frequency response characteristic.

ASYNCHRONOUS MODE

The Asynchronous mode is used for communication with asynchronous terminals which may communicate at 600,1200, or 2400 bit/s +1%, -2.5% even though the modem's output is limited to the nominal bit rate ±.01% in DPSK and QAM modes. When transmitting in this mode the serial data on the TXD input is passed through a rate converter which inserts or deletes stop bits in the serial bit stream in order to output a signal that is the nominal bit rate ±.01%. This signal is then

routed to a data scrambler and into the analog modulator where quad-bit/di-bit encoding results in the output signal. Both the rate converter and scrambler can be bypassed for handshaking, and synchronous operation as selected. Received data is processed in a similar fashion except that the rate converter now acts to reinsert any deleted stop bits and output data to the terminal at no greater than the bit rate plus 1%. An incoming break signal (low through two characters) will be passed through without incorrectly inserting a stop bit.

The SYNC/ASYNC converter also has an extended Overspeed mode which allows selection of an output overspeed range of either +1% or +2.3%. In the extended Overspeed mode, stop bits are output at 7/8 the normal width.

Both the SYNC/ASYNC rate converter and the data descrambler are automatically bypassed in the FSK modes.

SYNCHRONOUS MODE

Synchronous operation is possible only in the QAM or DPSK modes. Operation is similar to that of the Asynchronous mode except that data must be synchronized to a provided clock and no variation in data transfer rate is allowable. Serial input data appearing at TXD must be valid on the rising edge of TXCLK.

TXCLK is an internally derived 1200 or 2400 Hz signal in Internal mode and is connected internally to the RXCLK pin in Slave mode. Receive data at the RXD pin is clocked out on the falling edge of RXCLK. The asynch/synch converter is bypassed when Synchronous mode is selected and data is transmitted at the same rate as it is input.

PARALLEL BUS INTERFACE

Eight 8-bit registers are provided for control, option select, and status monitoring. These registers are addressed with the AD0, AD1, and AD2 multiplexed address lines (latched by ALE) and appear to a control microprocessor as seven consecutive memory locations. Six control registers are read/write memory. The detect and ID registers are read only and cannot be modified except by modem response to monitored parameters.

SERIAL CONTROL INTERFACE

The serial Command mode allows access to the SSI 73K224 control and status registers via a serial control port. In this mode the A0, A1, and A2 lines provide register addresses for data passed through the DATA pin under control of the $\overline{RD}$ and $\overline{WR}$ lines. A read operation is initiated when the $\overline{RD}$ line is taken low. The next eight cycles of EXCLK will then transfer out eight bits of the selected addresss location LSB first. A write takes place by shifting in eight bits of data LSB first for eight consectuive cycles of EXCLK. $\overline{WR}$ is then pulsed low and data transfer into the selected register occurs on the rising edge of $\overline{WR}$.

DTMF GENERATOR

The DTMF generator controls the sending of the sixteen standard DTMF tone pairs. The tone pair sent is determined by selecting TRANSMIT DTMF (bit D4) and the 4 DTMF bits (D0-D3) of the TONE register. Transmission of DTMF tones from TXA is gated by the TRANSMIT ENABLE bit of CR0 (bit D1) as with all other analog signals.

PIN DESCRIPTION

POWER

NAME	TYPE	DESCRIPTION
GND	I	System Ground.
VDD	I	Power supply input, 5V -5% +10%. Bypass with 0.22 µF and 22 µF capacitors to GND.
VREF	O	An internally generated reference voltage. Bypass with 0.22 µF capacitor to GND.
ISET	I	Chip current reference. Sets bias current for op-amps. The chip current is set by connecting this pin to VDD through a 2 MΩ resistor. Iset should be bypassed to GND with a 0.22 µF capacitor.

PARALLEL MICROPROCESSOR INTERFACE

ALE	I	Address latch enable. The falling edge of ALE latches the address on AD0-AD2 and the chip select on $\overline{CS}$.
AD0-AD7	I/O / Tristate	Address/data bus.These bidirectional tri-state multi-plexed lines carry information to and from the internal registers.
$\overline{CS}$	I	Chip select. A low on this pin allows a read cycle or a write cycle to occur. AD0-AD7 will not be driven and no registers will be written if $\overline{CS}$ (latched) is not active. $\overline{CS}$ is latched on the falling edge of ALE.
CLK	O	Output clock. This pin is selectable under processor control to be either the crystal frequency (for use as a processor clock) or 16 x the data rate for use as a baud rate clock in QAM/DPSK modes only. The pin defaults to the crystal frequency on reset.
$\overline{INT}$	O	Interrupt. This open drain weak pullup, output signal is used to inform the processor that a detect flag has occurred. The processor must then read the detect register to determine which detect triggered the interrupt. $\overline{INT}$ will stay active until the processor reads the detect register or does a full reset.
$\overline{RD}$	I	Read. A low requests a read of the SSI 73K224L internal registers. Data cannot be output unless both $\overline{RD}$ and the latched $\overline{CS}$ are active or low.
RESET	I	Reset. An active high signal on this pin will put the chip into an inactive state. All control register bits (CR0, CR1, CR2, CR3, Tone) will be reset. The output of the CLK pin will be set to the crystal frequency. An internal pull down resistor permits power on reset using a capacitor to VDD.
$\overline{WR}$	I	Write. A low on this informs the SSI 73K224L that data is available on AD0-AD7 for writing into an internal register. Data is latched on the rising edge of $\overline{WR}$. No data is written unless both $\overline{WR}$ and the latched $\overline{CS}$ are active (low).

Note: The serial control mode is provided in the parallel versions by tying ALE high and $\overline{CS}$ low. In this configuration AD7 becomes DATA and AD0, AD1 and AD2 become A0, A1 and A2, respectively.

DTE USER INTERFACE

NAME	TYPE	DESCRIPTION
EXCLK	I	External Clock. This signal is used in synchronous transmission when the external timing option has been selected. In the external timing mode the rising edge of EXCLK is used to strobe synchronous transmit data available on the TXD pin. Also used for serial control interface.
RXCLK	O/Tristate	Receive Clock. Tri-stateable. The falling edge of this clock output is coincident with the transitions in the serial received data output. The rising edge of RXCLK can be used to latch QAM or DPSK valid output data. RXCLK will be active as long as a carrier is present.
RXD	O / Weak Pull-up	Received Digital Data Output. Serial receive data is available on this pin. The data is always valid on the rising edge of RXCLK when in synchronous mode. RXD will output constant marks if no carrier is detected.
TXCLK	O/Tristate	Transmit Clock. Tri-stateable. This signal is used in synchronous transmission to latch serial input data on the TXD pin. Data must be provided so that valid data is available on the rising edge of the TXCLK. The transmit clock is derived from different sources depending upon the synchronization mode selection. In Internal Mode the clock is generated internally. In External Mode TXCLK is phase locked to the EXCLK pin. In Slave Mode TXCLK is phase locked to the RXCLK pin. TXCLK is always active.
TXD	I	Transmit Digital Data Input. Serial data for transmission is input on this pin. In synchronous modes, the data must be valid on the rising edge of the TXCLK clock. In asynchronous modes (2400/1200/600 bit/s or 300 baud) no clocking is necessary. DPSK data must be +1%, -2.5% or +2.3%, -2.5 % in extended overspeed mode.

ANALOG INTERFACE AND OSCILLATOR

RXA	I	Received modulated analog signal input from the phone line.
TXA	O	Transmit analog output to the phone line.
XTL1	I	These pins are for the internal crystal oscillator requiring a 11.0592 MHz parallel mode crystal. Two capacitors from these pins to ground are also required for proper crystal operation. Consult crystal manufacturer for proper values. XTL2 can also be driven from an external clock.
XTL2	I/O	

PIN DESCRIPTION (continued)

SERIAL MICROPROCESSOR INTERFACE

NAME	TYPE	DESCRIPTION
A0-A2	I	Register Address Selection. These lines carry register addresses and should be valid during any read or write operation.
DATA	I/O	Serial Control Data. Data for a read/write operation is clocked in or out on the falling edge of the EXCLK pin. The direction of data flow is controlled by the $\overline{RD}$ pin. $\overline{RD}$ low outputs data. $\overline{RD}$ high inputs data.
$\overline{RD}$	I	Read. A low on this input informs the SSI 73K322L that data or status information is being read by the processor. The falling edge of the $\overline{RD}$ signal will initiate a read from the addresses register. The $\overline{RD}$ signal must continue for eight falling edges of EXCLK in order to read all eight bits of the referenced register. Read data is provided LSB first. Data will not be output unless the $\overline{RD}$ signal is active.
$\overline{WR}$	I	Write. A low on this input informs the SSI 73K322L that data or status information has been shifted in through the DATA pin and is available for writing to an internal register. The normal procedure for a write is to shift in data LSB first on the DATA pin for eight consecutive falling edges of EXCLK and then to pulse $\overline{WR}$ low. Data is written on the rising edge of $\overline{WR}$.

Note: In the serial, 22-pin version, the pins AD0-AD7, ALE and $\overline{CS}$ are removed and replaced with the pins; A0, A1, A2, DATA, and an unconnected pin. Also, the $\overline{RD}$ and $\overline{WR}$ controls are used differently.

REGISTER DESCRIPTIONS

Eight 8-bit internal registers are accessible for control and status monitoring. The registers are accessed in read or write operations by addressing the A0, A1 and A2 address lines in serial mode, or the AD0, AD1 and AD2 lines in parallel mode. The address lines are latched by ALE. Register CR0 controls the method by which data is transferred over the phone line. CR1 controls the interface between the microprocessor and the SSI 73K224L internal state. DR is a detect register which provides an indication of monitored modem status conditions. TR, the tone control register, controls the DTMF generator, answer and guard tones and RXD output gate used in the modem initial connect sequence. CR2 is the primary DSP control interface and CR3 controls transmit attenuation and receive gain adjustments. All registers are read/write except for DR and ID which are read only. Register control and status bits are identified below:

REGISTER BIT SUMMARY

		ADDRESS	DATA BIT NUMBER							
REGISTER		AD - A0	D7	D6	D5	D4	D3	D2	D1	D0
CONTROL REGISTER 0	CR0	000	MODULATION OPTION	MODULATION TYPE 1	MODULATION TYPE 0	TRANSMIT MODE 2	TRANSMIT MODE 1	TRANSMIT MODE 0	TRANSMIT ENABLE	ANSWER/ ORIGINATE
CONTROL REGISTER 1	CR1	001	TRANSMIT PATTERN 1	TRANSMIT PATTERN 0	ENABLE DETECT INTERRUPT	BYPASS SCRAMBLER	CLK CONTROL	RESET	TEST MODE 1	TEST MODE 0
DETECT REGISTER	DR	010	RECEIVE LEVEL	PATTERN S1 DET	RECEIVE DATA	UNSCR. MARK DETECT	CARRIER DETECT	SPECIAL TONE DETECT	CALL PROGRESS DETECT	SIGNAL QUALITY
TONE CONTROL REGISTER	TR	011	RXD OUTPUT CONTROL	TRANSMIT GUARD TONE	TRANSMIT ANSWER TONE	TRANSMIT DTMF	DTMF3	DTMF2/ 4W/FDX	DTMF1/ EXTENDED OVERSPEED	DTMF0/GUARD/ ANSWER
CONTROL REGISTER 2	CR2	100	0	SPECIAL REGISTER ACCESS	CALL INITIALIZE	TRANSMIT S1	16 WAY	RESET DSP	TRAIN INHIBIT	EQUALIZER ENABLE
CONTROL REGISTER 3	CR3	101	TXDALT	TRISTATE TX/RXCLK	0	RECEIVE GAIN BOOST	TRANSMIT ATTEN. 3	TRANSMIT ATTEN. 2	TRANSMIT ATTEN. 1	TRANSMIT ATTEN. 0
SPECIAL REGISTER	SR	101	0	TX BAUD CLOCK	RX UNSCR. DATA	0	TXD SOURCE	SQ SELECT 1	SQ SELECT 0	0
ID REGISTER	ID	110	ID	ID	ID	ID	X	X	X	1

NOTE: When a register containing reserved control bits is written into, the reserved bits must be programmed as 0's.

X = Undefined, mask in software

REGISTER ADDRESS TABLE

REGISTER	ADDRESS AD2 - AD0	D7	D6	D5	D4	D3	D2	D1	D0
CONTROL REGISTER 0 CR0	000	MODULATION OPTION	MODULATION TYPE 1	MODULATION TYPE 0	TRANSMIT MODE 2	TRANSMIT MODE 1	TRANSMIT MODE 0	TRANSMIT ENABLE	ANSWER/ ORIGINATE
		QAM: 0=2400 BIT/S DPSK: 0=1200 BIT/S 1=600 BIT/S FSK: 0=103 MODE 1=V.21	10=QAM 00=DPSK 01=FSK	0000=PWR DOWN 0001=INT SYNCH 0010=EXT SYNCH 0011=SLAVE SYNCH 0100=ASYCH 8 BITS/CHAR 0101=ASYCH 9 BITS/CHAR 0110=ASYCH 10 BITS/CHAR 0111=ASYCH 11 BITS/CHAR 1X00=FSK				0=DISABLE TXA OUTPUT 1=ENABLE TXA OUTPUT	0=ANSWER 1=ORIGINATE
CONTROL REGISTER 1 CR1	001	TRANSMIT PATTERN 1	TRANSMIT PATTERN 0	ENABLE DETECT INTERRUPT	BYPASS SCRAMBLER	CLK CONTROL	RESET	TEST MODE 1	TEST MODE 0
			00=TX DATA 01=TX ALTERNATE 10=TX MARK 11=TX SPACE	0=DISABLE 1=ENABLE	0=NORMAL 1=BYPASS SCRAMBLER	0=XTAL 1=16 X DATA RATE OUTPUT AT CLK PIN IN QAM/DPSK MODE ONLY	0=NORMAL 1=RESET	00=NORMAL 01=ANALOG LOOPBACK 10=REMOTE DIGITAL LOOPBACK 11=LOCAL DIGITAL LOOPBACK	
DETECT REGISTER READ ONLY DR	010	RECEIVE LEVEL INDICATOR	S1 PATTERN DETECT	RECEIVE DATA	UNSCR. MARKS DETECT	CARRIER DETECT	ANSWER TONE DETECT	CP TONE DETECT	SIGNAL QUALITY INDICATOR
		0=SIGNAL BELOW THRESHOLD 1=ABOVE THRESHOLD	0=NOT PRESENT 1=PATTERN FOUND	OUTPUTS RECEIVED DATA STREAM		0=CONDITION NOT DETECTED 1=CONDITION DETECTED			0=GOOD 1=BAD
TONE CONTROL REGISTER TR	011	RXD OUTPUT CONTROL	TRANSMIT GUARD TONE	TRANSMIT ANSWER TONE	TRANSMIT DTMF	DTMF3	DTMF2/ 4W/FDX	DTMF1/ EXTENDED OVERSPEED	DTMF0/ GUARD/ ANSWER
		RXD PIN 0=NORMAL 1=OPEN	0=OFF 1=ON	0=OFF 1=ON	0=DATA 1=TX DTMF	4 BIT CODE FOR 1 OF 16 DUAL TONE COMBINATIONS			0=1800 Hz G.T. 2225 Hz ANS TONE GENERATED. 1=550 Hz G.T. 2100 Hz ANS TONE GENERATED & DETECTED (V.21, V.22)
CONTROL REGISTER 2 CR2	100	0	SPECIAL REGISTER ACCESS	CALL INITIALIZE	TRANSMIT S1	16 WAY	$\overline{\text{RESET}}$ DSP	TRAIN INHIBIT	EQUALIZER ENABLE
			0=ACCESS CR3 1=ACCESS SPECIAL REGISTER	0=DSP IN DEMOD MODE 1=DSP IN CALL PROGRESS MODE	0=NORMAL DOTTING 1=S1	0=RX=TX 1=RX=16 WAY	0=DSP INACTIVE 1=DSP ACTIVE	0=ADAPT EQ ACTIVE 1=ADAPT EQ FROZEN	0=ADAPT EQ IN INIT 1=ADAPT EQ OK TO ADAPT
CONTROL REGISTER 3 CR3	101	TXDALT	TRISTATE TX/RXCLK	0	RECEIVE GAIN BOOST	TRANSMIT ATTEN. 3	TRANSMIT ATTEN. 2	TRANSMIT ATTEN. 1	TRANSMIT ATTEN. 0
		ALTERNATE TRANSMIT DATA SOURCE	0=NORMAL 1=TRISTATE		0=NO BOOST 1=18 dB BOOST	0000-1111, SETS TRANSMIT ATTENUATOR 16 dB RANGE DEFAULT=0100 ≈ -10 dBm0			
SPECIAL REGISTER SR	101	0	TX BAUD CLOCK	RX UNSCR. DATA	0	TXD SOURCE	SQ SELECT1	SQ SELECT0	0
			OUTPUTS TXBAUD CLOCK	OUTPUTS UNSCR. DATA		0=TXD PIN 1=TXALT BIT	00≈ 10^{-5} BER 01≈ 10^{-6} BER 10≈ 10^{-4} BER 11≈ 10^{-3} BER		
ID REGISTER READ ONLY 10	110	ID	ID	ID	ID	X	X	X	1

00XX=73K212L, 322L, 321L
01XX=73K221L, 302L
10XX=73K222L
1100=73K224L
1110=73K324L

0 = Only write zeros to these locations
x = Undefined, mask in software

CONTROL REGISTER 0

	D7	D6	D5	D4	D3	D2	D1	D0
CR0 000	MODUL. OPTION	MODUL. TYPE 1	MODUL. TYPE 0	TRANSMIT MODE 2	TRANSMIT MODE 1	TRANSMIT MODE 0	TRANSMIT ENABLE	ANSWER/ ORIGINATE

BIT NO.	NAME	CONDITION	DESCRIPTION
D0	Answer/ Originate	0	Selects answer mode (transmit in high band, receive in low band).
		1	Selects originate mode (transmit in low band, receive in high band).
D1	Transmit Enable	0	Disables transmit output at TXA.
		1	Enables transmit output at TXA.
			Note: Transmit Enable must be set to 1 to allow activation of Answer Tone or DTMF.
D5, D4, D3, D2	Transmit Mode	D5 D4 D3 D2	
		0 0 0 0	Selects power down mode. All functions disabled except digital interface.
		0 0 0 1	Internal synchronous mode. In this mode TXCLK is an internally derived 600,1200 or 2400 Hz signal. Serial input data appearing at TXD must be valid on the rising edge of TXCLK. Receive data is clocked out of RXD on the falling edge of RXCLK.
		0 0 1 0	External synchronous mode. Operation is identical to internal synchronous, but TXCLK is connected internally to EXCLK pin, and a 600, 1200 or 2400 Hz clock must be supplied externally.
		0 0 1 1	Slave synchronous mode. Same operation as other synchronous modes. TXCLK is connected internally to the RXCLK pin in this mode.
		0 1 0 0	Selects asynchronous mode - 8 bits/character (1 start bit, 6 data bits, 1 stop bit).
		0 1 0 1	Selects asynchronous mode - 9 bits/character (1 start bit, 7 data bits, 1 stop bit).
		0 1 1 0	Selects asynchronous mode - 10 bits/character (1 start bit, 8 data bits, 1 stop bit).
		0 1 1 1	Selects asynchronous mode - 11 bits/character (1 start bit, 8 data bits, Parity and/or 1 or 2 stop bits).
		1 X 0 0	Selects FSK operation.
D6,D5	Modulation Type	D6 D5	
		1 0	QAM
		0 0	DPSK
		0 1	FSK

CONTROL REGISTER 0 (continued)

	D7	D6	D5	D4	D3	D2	D1	D0
CR0 000	MODUL. OPTION	MODUL. TYPE 1	MODUL. TYPE 0	TRANSMIT MODE 2	TRANSMIT MODE 1	TRANSMIT MODE 0	TRANSMIT ENABLE	ANSWER/ ORIGINATE

BIT NO.	NAME	CONDITION	DESCRIPTION
D7	Modulation Option	0	QAM selects 2400 bit/s. DPSK selects 1200 bit/s. FSK selects 103 mode.
		1	DPSK selects 600 bit/s. FSK selects V.21 mode.

CONTROL REGISTER 1

	D7	D6	D5	D4	D3	D2	D1	D0
CR1 001	TRANSMIT PATTERN 1	TRANSMIT PATTERN 0	ENABLE DETECT INT.	BYPASS SCRAMB	CLK CONTROL	RESET	TEST MODE 1	TEST MODE 0

BIT NO.	NAME	CONDITION	DESCRIPTION
D1, D0	Test Mode	D1 D0	
		0 0	Selects normal operating mode.
		0 1	Analog loopback mode. Loops the transmitted analog signal back to the receiver, and causes the receiver to use the same carrier frequency as the transmitter. To squelch the TXA pin, TRANSMIT ENABLE bit as well as Tone Reg bit D2 must be low.
		1 0	Selects remote digital loopback. Received data is looped back to transmit data internally, and RXD is forced to a mark. Data on TXD is ignored.
		1 1	Selects local digital loopback. Internally loops TXD back to RXD and continues to transmit data carrrier at TXA pin.
D2	Reset	0	Selects normal operation.
		1	Resets modem to power down state. All control register bits (CR0, CR1, CR2, CR3 and Tone) are reset to zero except CR3 bit D2. The output of the clock pin will be set to the crystal frequency.
D3	Clock Control	0	Selects 11.0592 MHz crystal echo output at CLK pin.
		1	Selects 16 X the data rate, output at CLK pin in DPSK/ QAM modes only.

CONTROL REGISTER 1 (continued)

	D7	D6	D5	D4	D3	D2	D1	D0
CR1 001	TRANSMIT PATTERN 1	TRANSMIT PATTERN 0	ENABLE DETECT INT.	BYPASS SCRAMB	CLK CONTROL	RESET	TEST MODE 1	TEST MODE 0

BIT NO.	NAME	CONDITION	DESCRIPTION
D4	Bypass Scrambler	0	Selects normal operation. DPSK and QAM data is passed through scrambler.
		1	Selects Scrambler Bypass. Bypass DPSK and QAM data is routed around scrambler in the transmit path.
D5	Enable Detect Interrupt	0	Disables interrupt at $\overline{INT}$ pin. All interrupts are normally disabled in power down mode.
		1	Enables $\overline{INT}$ output. An interrupt will be generated with a change in status of DR bits D1-D4 and D6. The answer tone and call progress detect interrupts are masked when the TX enable bit is set. Carrier detect is masked when TX DTMF is activated. All interrupts will be disabled if the device is in power down mode.
D7, D6	Transmit Pattern	D7 D6	
		0 0	Selects normal data transmission as controlled by the state of the TXD pin.
		0 1	Selects an alternating mark/space transmit pattern for modem testing and handshaking. Also used for S1 pattern generation. See CR2 bit D4.
		1 0	Selects a constant mark transmit pattern.
		1 1	Selects a constant space transmit pattern.

DETECT REGISTER

	D7	D6	D5	D4	D3	D2	D1	D0
DR 010	RECEIVE LEVEL INDICATOR	S1 PATTERN DETECT	RECEIVE DATA	UNSCR. MARK DETECT	CARR. DETECT	ANSWER TONE DETECT	CALL PROG. DETECT	SIGNAL QUALITY INDICATOR

BIT NO.	NAME	CONDITION	DESCRIPTION
D0	Signal Quality Indicator	0	Indicates normal received signal.
		1	Indicates low received signal quality (above average error rate). Interacts with special register bits D2, D1.
D1	Call Progress Detect	0	No call progress tone detected.
		1	Indicates presence of call progress tones. The call progress detection circuitry is activated by energy in the normal 350 to 620 Hz call progress bandwidth.

DETECT REGISTER (continued)

	D7	D6	D5	D4	D3	D2	D1	D0
DR 010	RECEIVE LEVEL INDICATOR	S1 PATTERN DETECT	RECEIVE DATA	UNSCR. MARK DETECT	CARR. DETECT	ANSWER TONE DETECT	CALL PROG.	SIGNAL QUALITY INDICATOR

BIT NO.	NAME	CONDITION	DESCRIPTION
D2	Answer Tone Received	0	No answer tone detected.
		1	In Call Init mode, indicates detection of 2225 Hz answer tone in Bell mode (TR bit D0=0) or 2100 Hz if in CCITT mode (TR bit D0=1). The device must be in originate mode for detection of answer tone. Both answer tones are detected in demod mode.
D3	Carrier Detect	0	No carrier detected in the receive channel.
		1	Indicated carrier has been detected in the received channel.
D4	Unscrambled Mark Detect	0	No unscrambled mark.
		1	Indicates detection of unscrambled marks in the received data. Should be time qualified by software.
D5	Receive Data		Continuously outputs the received data stream. This data is the same as that output on the RXD pin, but it is not disabled when RXD is tri-stated.
D6	S1 Pattern Detect	0	No S1 pattern being received.
		1	S1 pattern detected. Should be time qualified by software. S1 pattern is defined as a double di-bit (001100..) unscrambled 1200 bit/s DPSK signal. Pattern must be aligned with baud clock to be detected.
D7	Receive Level Indicator	0	Received signal level below threshold, (typical ≈ -25 dBm0); can use receive gain boost (+18 dB).
		1	Received signal above threshold.

TONE REGISTER

	D7	D6	D5	D4	D3	D2	D1	D0
TR 011	RXD OUTPUT CONTR.	TRANSMIT GUARD TONE	TRANSMIT ANSWER TONE	TRANSMIT DTMF	DTMF 3	DTMF 2	DTMF 1/ EXTENDED OVER-SPEED	DTMF 0/ ANSWER/ GUARD

BIT NO.	NAME	CONDITION	DESCRIPTION
D0	DTMF 0/ Answer/ Guard Tone	D6 D5 D4 D0	D0 interacts with bits D6, D5, and D4 as shown.
		X X 1 X	Transmit DTMF tones.
		X 1 0 0	Select Bell mode answer tone. Interacts with DR bit D2 and TR bit D5.
		X 1 0 1	Select CCITT mode answer tone. Interacts with DR bit D2 and TR bit D5.

TONE REGISTER (continued)

	D7	D6	D5	D4	D3	D2	D1	D0
TR 011	RXD OUTPUT CONTR.	TRANSMIT GUARD TONE	TRANSMIT ANSWER TONE	TRANSMIT DTMF	DTMF 3	DTMF 2/ 4 WIRE FDX	DTMF 1/ EXTENDED OVER-SPEED	DTMF 0/ ANSWER/ GUARD

BIT NO.	NAME	CONDITION	DESCRIPTION
D0	DTMF 0/ Answer/ Guard Tone	D6 D5 D4 D0	D0 interacts with bits D6, D5, and D4 as shown.
		1 0 0 0	Select 1800 Hz guard tone.
		1 0 0 1	Select 550 Hz guard tone.
D1	DTMF 1/ Extended Overspeed	D4 D1	D1 interacts with D4 as shown.
		0 0	Asynchronous QAM or DPSK +1.0% -2.5%. (normal)
		0 1	Asynchronous QAM or DPSK +2.3% -2.5%. (extended overspeed)
D2	DTMF 2/ 4 WIRE FDX	D4 D2	
		0 0	Selects 2 wire duplex or half duplex
		0 1	D2 selects 4 wire full duplex in the modulation mode selected. The receive path corresponds to the ANS/ ORIG bit CR0 D0 in terms of high or low band selection. The transmitter is in the same band as the receiver, but does not have magnitude filtering or equalization on its signal as in the receive path.

TONE REGISTER (continued)

	D7	D6	D5	D4	D3	D2	D1	D0
TR 011	RXD OUTPUT CONTR.	TRANSMIT GUARD TONE	TRANSMIT ANSWER TONE	TRANSMIT DTMF	DTMF 3	DTMF 2/ 4 WIRE FDX	DTMF 1/ EXTENDED OVER-SPEED	DTMF 0/ ANSWER/ GUARD

BIT NO.	NAME	CONDITION	DESCRIPTION
D3, D2, D1, D0	DTMF 3, 2, 1, 0	D3 D2 D1 D0 0 0 0 0 1 1 1 1	Programs 1 of 16 DTMF tone pairs that will be transmitted when TX DTMF and TX enable bit (CR0, bit D1) is set. Tone encoding is shown below:
D4	TX DTMF (Transmit DTMF)	0	Disable DTMF.
		1	Activate DTMF. The selected DTMF tones are transmitted continuously when this bit is high. TX DTMF overrides all other transmit functions.

KEYBOARD EQUIVALENT	DTMF CODE D3 D2 D1 D0	TONES LOW HIGH
1	0 0 0 1	697 1209
2	0 0 1 0	697 1336
3	0 0 1 1	697 1477
4	0 1 0 0	770 1209
5	0 1 0 1	770 1336
6	0 1 1 0	770 1477
7	0 1 1 1	852 1209
8	1 0 0 0	852 1336
9	1 0 0 1	852 1477
0	1 0 1 0	941 1336
*	1 0 1 1	941 1209
#	1 1 0 0	941 1477
A	1 1 0 1	697 1633
B	1 1 1 0	770 1633
C	1 1 1 1	852 1633
D	0 0 0 0	941 1633

Note: DTMF0 - DTMF2 should be set to an appropriate state after DTMF dialing to avoid unintended operation.

TONE REGISTER (continued)

D7	D6	D5	D4	D3	D2	D1	D0	
TR 011	RXD OUTPUT CONTR.	TRANSMIT GUARD TONE	TRANSMIT ANSWER TONE	TRANSMIT DTMF	DTMF 3	DTMF 2/ 4 WIRE FDX	DTMF 1/ EXTENDED OVER-SPEED	DTMF 0/ ANSWER/ GUARD

BIT NO.	NAME	CONDITION	DESCRIPTION
D5	Transmit Answer Tone	D5 D4 D0	D5 interacts with bits D4 and D0 as shown. Also interacts with DR bit D2 in originate mode. See Detect Register description.
		0 0 X	Disables answer tone generator.
		1 0 0	In answer mode, a Bell 2225 Hz tone is transmitted continuously when the Transmit Enable bit is set.
		1 0 1	Likewise, a CCITT 2100 Hz answer tone is transmitted.
D6	Transmit Guard Tone	0	Disables guard tone generator.
		1	Enables guard tone generator. (See D0 for selection of guard tones.) Bit D4 must be zero.
D7	RXD Output Control	0	Enables RXD pin. Receive data will be output on RXD.
		1	Disables RXD pin. The RXD pin reverts to a high impedance with internal weak pull-up resistor.

CONTROL REGISTER 2

	D7	D6	D5	D4	D3	D2	D1	D0
CR2 100	0	SPEC REG ACCESS	CALL INIT	TRANSMIT S1	16 WAY	$\overline{\text{RESET}}$ DSP	TRAIN INHIBIT	EQUALIZER ENABLE

BIT NO.	NAME	CONDITION	DESCRIPTION
D0	Equalizer Enable	0	The adaptive equalizer is in its initialized state.
		1	The adaptive equalizer is enabled. This bit is used in handshakes to control when the equalizer should calculate its coefficients.
D1	Train Inhibit	0	The adaptive equalizer is active.
		1	The adaptive equalizer coefficients are frozen.
D2	$\overline{\text{RESET}}$ $\overline{\text{DSP}}$	0	The DSP is inactive and all variables are initialized.
		1	The DSP is running based on the mode set by other control bits
D3	16 Way	0	The receiver and transmitter are using the same decision plane (based on the Modulator Control Mode).
		1	The receiver, independent of the transmitter, is forced into a 16 point decision plane. Used for QAM handshaking.

CONTROL REGISTER 2 (continued)

	D7	D6	D5	D4	D3	D2	D1	D0
CR2 100	0	SPEC REG ACCESS	CALL INIT	TRANSMIT S1	16WAY	$\overline{\text{RESET}}$ DSP	TRAIN INHIBIT	EQUALIZER ENABLE

BIT NO.	NAME	CONDITION	DESCRIPTION
D4	Transmit S1	0	The transmitter when placed in alternating mark/space mode transmits 0101..... scrambled or not dependent on the bypass scrambler bit.
		1	When this bit is 1 and only when the transmitter is placed in alternating mark/space mode by CR1 bits D7, D6, and in DPSK or QAM, an unscrambled repetitive double dibit pattern of 00 and 11 at 1200 bit/s (S1) is sent.
D5	Call Init	0	The DSP is setup to do demodulation and pattern detection based on the various mode bits. Both answer tones are detected in demod mode concurrently; TR-D0 is ignored.
		1	The DSP decodes unscrambled mark, answer tone and call progress tones.
D6	Special Register Access	0	Normal CR3 access.
		1	Setting this bit and addressing CR3 allows access to the SPECIAL REGISTER. See the SPECIAL REGISTER for details.
D7	Not used at this time	0	Only write zero to this bit.

CONTROL REGISTER 3

	D7	D6	D5	D4	D3	D2	D1	D0
CR3 101	TXDALT	TRISTATE TX/RXCLK	0	RECEIVE BOOST ENABLE	TRANSMIT ATTEN. 3	TRANSMIT ATTEN. 2	TRANSMIT ATTEN. 1	TRANSMIT ATTEN. 0

BIT NO.	NAME	CONDITION	DESCRIPTION
D3, D2, D1,D0	Transmit Attenuator	D3 D2 D1 D0 0 0 0 0 1 1 1 1	Sets the attenuation level of the transmitted signal in 1dB steps. The default (D3-D0=0100) is for a transmit level of -10 dBm0 on the line with the recommended hybrid transmit gain. The total range is 16 dB.
D4	Receive Gain Boost Not used at this time	0	18 dB receive front end boost is not used.
		1	Boost is in the path. This boost does not change reference levels. It is used to extend dynamic range by compensating for internally generated noise when receiving weak signals. The receive level detect signal and knowledge of the hybrid and transmit attenuator setting will determine when boost should be enabled.
D5		0	Only write zero to this bit.
D6	TRISTATE TXCLK/RXCLK	0	TXCLK and RXCLK are driven.
		1	TXCLK and RXCLK are tristated.
D7	TXDALT	Spec. Reg. Bit D3=1	Alternate TX data source. See Special Register.

SPECIAL REGISTER

	D7	D6	D5	D4	D3	D2	D1	D0
SR 101	0	TXBAUD CLOCK	RXUN-DSCR DATA	0	TXD SOURCE	SIGNAL QUALITY LEVEL SELECT1	SIGNAL QUALITY LEVEL SELECT0	0

BIT NO.	NAME	DESCRIPTION
D7, D4, D0		NOT USED AT THIS TIME. Only write ZEROs to these bits.
D6	TXBAUD CLK	TXBAUD clock is the transmit baud-synchronous clock that can be used to synchronize the input of arbitrary quad/di-bit patterns. The rising edge of TXBAUD signals the latching of a baud-worth of data internally. Synchronous data to be entered via the TXDALT bit, CR3 bit D7, should have data transitions that start 1/2 bit period delayed from the TXBAUD clock edges.
D5	RXUNDSCR DATA	This bit outputs the data received before going to the descrambler. This is useful for sending special unscrambled patterns that can be used for signaling.
D3	TXD SOURCE	This bit selects the transmit data source; either the TXD pin if ZERO or the TXDALT if this bit is a ONE. The TRANSMIT PATTERN bits D7 and D6 in CR1 override either of these sources.
D2, D1	SIGNAL QUALITY LEVEL SELECT	The signal quality indicator is a logical ZERO when the signal received is acceptable for low error rate reception. It is determined by the value of the Mean Squared Error (MSE) calculated in the decisioning process when compared to a given threshold. This threshold can be set to four levels of error rate. The SQI bit will be low for good or average connections. As the error rate crosses the threshold setting, the SQI bit will toggle at a 1.66 ms rate. Toggling will continue until the error rate indicates that the data pump has lost convergence and a retrain is required. At that point the SQI bit will be a ONE constantly. The SQI bit and threshold selection are valid for QAM and DPSK only and indicates typical error rate.

D2	D1	THRESHOLD VALUE	UNITS
0	0	10^{-5}	BER (default)
0	1	10^{-6}	BER
1	0	10^{-4}	BER
1	1	10^{-3}	BER

NOTE: This register is "mapped" and is accessed by setting CR2 bit D6 to a ONE and addressing CR3. This register provides functions to the 73K224L user that are not necessary in normal communications. Bits D7-D4 are read only, while D3-D0 are read/write. To return to normal CR3 access, CR2 bit D6 must be returned to a ZERO.

ID REGISTER

	D7	D6	D5	D4	D3	D2	D1	D0
ID 110	ID 3	ID 2	ID 1	ID 0	X	X	X	1

BIT NO.	NAME	CONDITION	DESCRIPTION
D7, D6, D5, D4	Device Identification Signature	D7 D6 D5 D4	Indicates Device:
		0 0 X X	SSI 73K212L, 73K321L or 73K322L
		0 1 X X	SSI 73K221L or 73K302L
		1 0 X X	SSI 73K222L
		1 1 0 0	SSI 73K224L
		1 1 1 0	SSI 73K324L
D3-D1	Not Used	Undefined	Mask in software
D0	Version	1	Indicates industrial temperature version

ELECTRICAL SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING
VDD Supply Voltage	7V
Storage Temperature	-65 to 150°C
Soldering Temperature (10 sec.)	260°C
Applied Voltage	-0.3 to VDD+0.3V
Note: All inputs and outputs are protected from static charge using built-in, industry standard protection devices and all outputs are short-circuit protected.	

RECOMMENDED OPERATING CONDITIONS

PARAMETER	CONDITION	MIN	NOM	MAX	UNIT
VDD Supply voltage		4.5	5	5.5	V
External Components (Refer to Application section for placement.)					
VREF Bypass capacitor	(VREF to GND)	0.22			µF
Bias setting resistor	(Placed between VDD and ISET pins)	1.8	2	2.2	MΩ
ISET Bypass capacitor	(ISET pin to GND)	0.22			µF
VDD Bypass capacitor 1	(VDD to GND)	0.22			µF
VDD Bypass capacitor 2	(VDD to GND)	22			µF
XTL1 Load Capacitance	Depends on crystal requirements		18	39	pF
XTL2 Load Capacitance	Depends on crystal requirements		18	27	pF
Clock Variation	(11.0592 MHz) Crystal or external clock	-0.01		+0.01	%
TA, Operating Free-Air Temperature		-40		85	°C

DC ELECTRICAL CHARACTERISTICS

(TA = -40°C to 85°C, VDD = recommended range unless otherwise noted.)

PARAMETER	CONDITION	MIN	NOM	MAX	UNIT
IDD, Supply Current	CLK = 11.0592 MHz				
	ISET Resistor = 2 MΩ				
IDD1, Active	Operating with crystal oscillator,		18	25	mA
IDD2, Idle	< 5 pF capacitive load on CLK pin		3	5	mA
Digital Inputs					
VIL, Input Low Voltage				0.8	V
VIH, Input High Voltage					
All Inputs except Reset XTL1, XTL2		2.0		VDD	V
Reset, XTL1, XTL2		3.0		VDD	V
IIH, Input High Current	VI = VDD			100	µA
IIL, Input Low Current	VI = 0V	-200			µA
Reset Pull-down Current	Reset = VDD	2		50	µA
Digital Outputs					
VOH, Output High Voltage	IO = IOH Min IOUT = -0.4 mA	2.4		VDD	V
VOL, Output Low Voltage	IO = IOUT = 1.6 mA			0.4	V
RXD Tri-State Pull-up Curr.	RXD = GND	-2		-50	µA
Capacitance					
CLK	Maximum permitted load			25	pF
Input Capacitance	All digital inputs			10	pF

ELECTRICAL SPECIFICATIONS (continued)

DYNAMIC CHARACTERISTICS AND TIMING

(TA = -40°C to +85°C, VDD = recommended range unless otherwise noted.)

PARAMETER	CONDITION	MIN	NOM	MAX	UNIT
QAM/DPSK Modulator					
Carrier Suppression	Measured at TXA	35			dB
Output Amplitude	TX scrambled marks ATT = 0100 (default)	-11.5	-10.0	-9	dBm0
FSK Modulator/Demodulator					
Output Freq. Error	CLK = 11.0592 MHz	-0.31		+0.20	%
Transmit Level	ATT = 0100 (Default) Transmit Dotting Pattern	-11.5	-10.0	-9	dBm0
TXA Output Distortion	All products through BPF			-45	dB
Output Bias Distortion at RXD	Dotting Pattern measured at RXD Receive Level -20 dBm, SNR 20 dB	-10		+10	%
Output Jitter at RXD	Integrated for 5 seconds	-15		+15	%
Sum of Bias Distortion and Output Jitter	Integrated for 5 seconds	-17		+17	%
Answer Tone Generator (2100 or 2225 Hz)					
Output Amplitude	ATT = 0100 (Default Level) Not in V.21	-11.5	-10	-9	dBm0
Output Distortion	Distortion products in receive band			-40	dB
DTMF Generator	Not in V.21				
Freq. Accuracy		-0.03		+0.25	%
Output Amplitude	Low Band, ATT = 0100, DPSK Mode	-10		-8	dBm0
Output Amplitude	High Band, ATT = 0100, DPSK Mode	-8		-6	dBm0
Twist	High-Band to Low-Band, DPSK Mode	1.0	2.0	3.0	dB
Receiver Dynamic Range	Refer to Performance Curves	-43		-3.0	dBm0
Call Progress Detector	In Call Init mode				
Detect Level	460 Hz test signal	-34		0	dBm0
Reject Level				-40	dBm0
Delay Time	-70 dBm0 to -30 dBm0 STEP			25	ms
Hold Time	-30 dBm0 to -70 dBm0 STEP			25	ms

NOTE: Parameters expressed in dBm0 refer to the following definition:

0 dB loss in the Transmit path to the line.

2 dB gain in the Receive path from the line.

Refer to the Basic Box Modem diagram in the Applications section for the DAA design.

DYNAMIC CHARACTERISTICS AND TIMING (continued)

PARAMETER		CONDITION	MIN	NOM	MAX	UNIT
Carrier Detect		**Receive Gain = On for lower input level measurements**				
Threshold		All Modes	-48		-43	dBm0
Hysteresis		All Modes		2		
Delay Time	FSK	70 dBm0 to -6 dBm0	25		37	ms
		70 dBm0 to -40 dBm0	25		37	ms
	DPSK	-70 dBm0 to -6 dBm0	7		17	ms
		-70 dBm0 to -40 dBm0	7		17	ms
	QAM	-70 dBm0 to -6 dBm0	25		37	ms
		-70 dBm0 to -40 dBm0	25		37	ms
Hold Time	FSK	-6 dBm0 to -70 dBm0	25		37	ms
		-40 dBm0 to -70 dBm0	15		30	ms
	DPSK	-6 dBm0 to -70 dBm0	20		29	ms
		-40 dBm0 to -70 dBm0	14		21	ms
	QAM	-6 dBm0 to -70 dBm0	25		32	ms
		-40 dBm0 to -70 dBm0	18		28	ms
Answer Tone Detectors		**DPSK Mode**				
Detect Level			-48		-43	dBm0
Detect Time		Call Init Mode, 2100 or 2225 Hz	6		50	ms
Hold Time			6		50	ms
Pattern Detectors		**DPSK Mode**				
S1 Pattern						
Delay Time		For signals from -6 to -40 dBm0,	10		55	ms
Hold Time		-6 to -40 dBm0, Demod Mode	10		45	ms
Unscrambled Mark						
Delay Time		For signals from -6 to -40	10		45	ms
Hold Time		call Init Mode	10		45	ms
Receive Level Indicator						
Detect On			-22		-28	dBm0
Valid after Carrier Detect		DPSK Mode	1	4	7	ms
Output Smoothing Filter						
Output Impedance		TXA pin		200	300	Ω
Output load		TXA pin; FSK Single	10			KΩ
		Tone out for THD = -50 dB in 0.3 to 3.4 kHz range			50	pF
Maximum Transmitted Energy		4 kHz, Guard Tones off			-35	dBm0
		10 kHz, Guard Tones off			-55	dBm0
		12 kHz, Guard Tones off			-65	dBm0

DYNAMIC CHARACTERISTICS AND TIMING (continued)

PARAMETER	CONDITION	MIN	NOM	MAX	UNIT
Anti Alias Low Pass Filter					
Out of Band Signal Energy (Defines Hybrid Trans-Hybrid loss requirements)	Level at RXA pin with receive Boost Enabled				
	Scrambled data at 2400 bit/s in opposite band		-14		dBm
	Sinusoids out of band		-9		dBm
Transmit Attenuator					
Range of Transmit Level	Default ATT=0100 (-10 dBm0) 1111-0000	-21		-6	dBm0
Step Accuracy		-0.15		+0.15	dB
Output Impedance			200	300	Ω
Clock Noise					
	TXA pin; 153.6 kHz			1.5	mVrms
Carrier Offset					
Capture Range	Originate or Answer		±5		Hz
Recovered Clock					
Capture Range	% of frequency (originate or answer)	-0.02		+0.02	%
Guard Tone Generator					
Tone Accuracy	550 Hz		+1.2		%
	1800 Hz		-0.8		
Tone Level	550 Hz	-4.5	-3.0	-1.5	dB
(Below QAM/DPSK Output)	1800 Hz	-7.5	-6.1	-4.5	dB
Harmonic Distortion	550 Hz			-50	dB
(700 to 2900 Hz)	1800 Hz			-50	dB
Timing (Refer to Timing Diagrams)					
Parallel Mode					
TAL	$\overline{CS}$/Addr. setup before ALE Low	30			ns
TLA	$\overline{CS}$/Addr. hold after ALE Low	6			ns
TLC	ALE Low to $\overline{RD}$/$\overline{WR}$ Low	40			ns
TCL	$\overline{RD}$/$\overline{WR}$ Control to ALE High	10			ns
TRD	Data out from $\overline{RD}$ Low			90	ns
TLL	ALE width	25			ns
TRDF	Data float after $\overline{RD}$ High			40	ns
TRW	$\overline{RD}$ width	70			ns

DYNAMIC CHARACTERISTICS AND TIMING (continued)

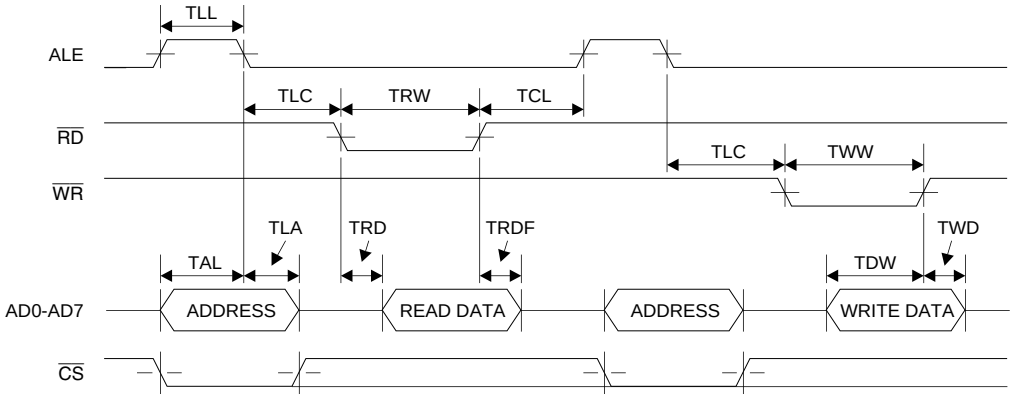
PARAMETER	CONDITION	MIN	NOM	MAX	UNIT
Parallel Mode (continued)					
TWW	$\overline{WR}$ width	70			ns
TDW	Data setup before $\overline{WR}$ High	70			ns
TWD	Data hold after $\overline{WR}$ High	20			ns
Serial Mode					
TRCK	Clock High after $\overline{RD}$ Low	250		T1	ns
TAR	Address setup before $\overline{RD}$ Low	0			ns
TRA	Address hold after $\overline{RD}$ Low	350			ns
TRD	$\overline{RD}$ to Data valid			300	ns
TRDF	Data float after $\overline{RD}$ High			40	ns
TCKDR	Read Data out after Falling Edge of EXCLK			300	ns
TWW	$\overline{WR}$ width	350			ns
TAW	Address setup before $\overline{WR}$ Low	50			ns
TWA	Address hold after Rising Edge of $\overline{WR}$	50			ns
TCKDW	Write Data hold after Falling Edge of EXCLK	200			ns
TCKW	$\overline{WR}$ High after Falling Edge of EXCLK	330		T1 + T2	ns
TDCK	Data setup before Falling Edge of EXCLK	50			ns
T1, T2	Minimum Period	500			ns

NOTE: T1 and T2 are the low/high periods, respectively, of EXCLK in serial mode.

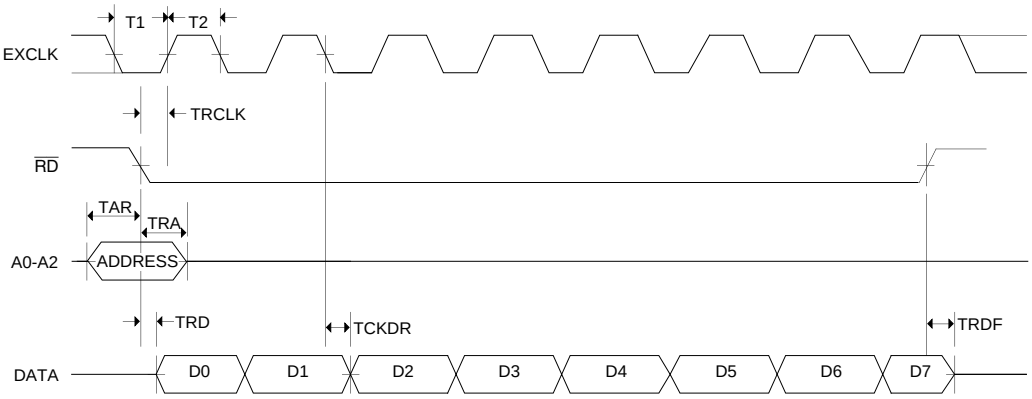
NOTE: Asserting ALE, $\overline{CS}$, and $\overline{RD}$ or $\overline{WR}$ concurrently can cause unintentional register accesses. When using non-8031 compatible processors, care must be taken to prevent this from occurring when designing the interface logic.

TIMING DIAGRAMS

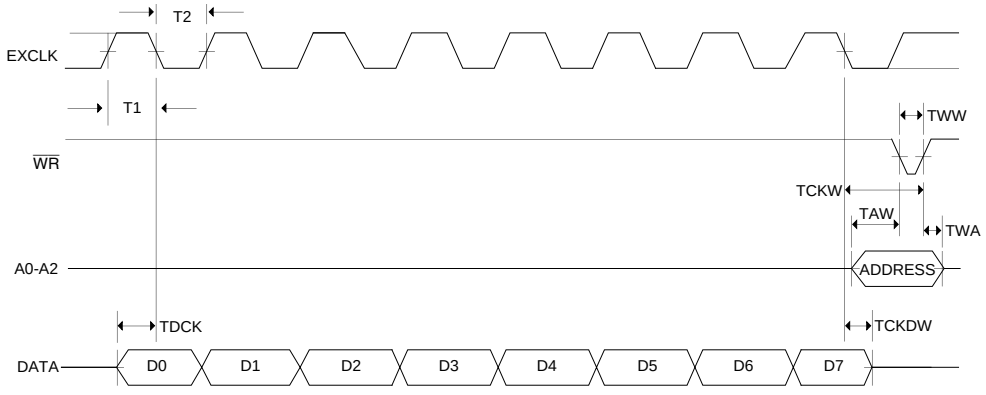
BUS TIMING DIAGRAM (PARALLEL VERSION)



READ TIMING DIAGRAM (SERIAL VERSION)



WRITE TIMING DIAGRAM (SERIAL VERSION)



APPLICATIONS INFORMATION

GENERAL CONSIDERATIONS

Figures 1 and 2 show basic circuit diagrams for K-Series modem integrated circuits. K-Series products are designed to be used in conjunction with a control processor, a UART or RS-232 serial data interface, and a DAA phone line interface to function as a typical intelligent modem. The K-Series ICs interface directly with Intel 8048 and 80C51 microprocessors for control and status monitoring purposes. Two typical DAA arrangements are shown: one for a split ±5 or ±12V design and one for a single 5V design. These diagrams are for reference only and do not represent production-ready modem designs.

K-Series devices are available with two control interface versions: one for a parallel multiplexed address/data interface, and one for a serial interface. The parallel version is intended for use with 8039/48 or 8031/51 microcontrollers from Intel or many other manufacturers. The serial interface 22-pin version can be used with other microcontrollers or in applications where only a limited number of port lines are available or the application does not lend itself to a multiplexed address/data interface. The parallel versions may also be used in the serial mode, as explained in the data sheet pin description.

In most applications the controller will monitor the serial data for commands from the DTE and the received data for break signals from the far end modem. In this way, commands to the modem are sent over the same line as the transmitted data. In other applications the RS-232 interface handshake lines are used for modem control.

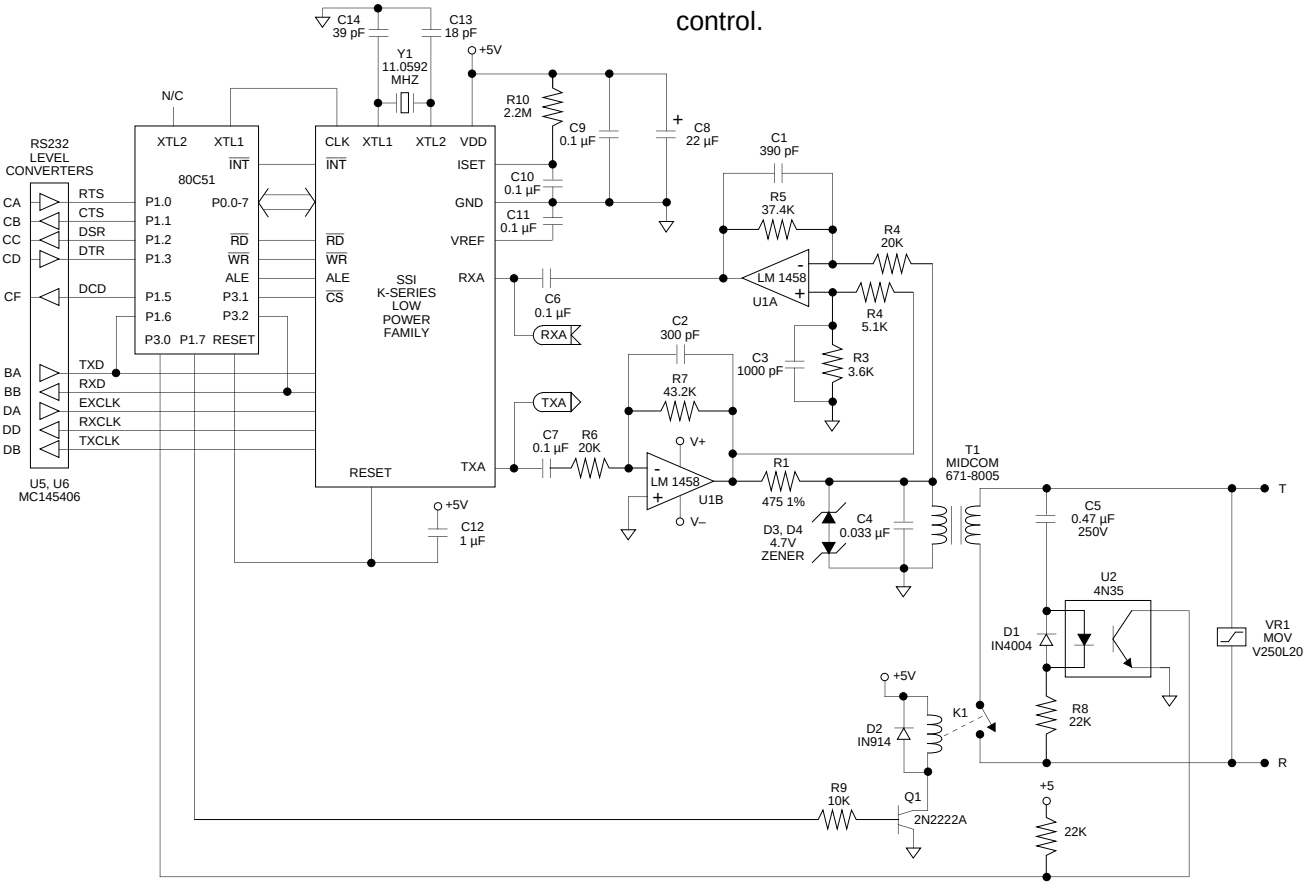


FIGURE 1: Basic Box Modem with Dual-Supply Hybrid

DIRECT ACCESS ARRANGEMENT (DAA)

The telephone line interfaces show two examples of how the "hybrid" may be implemented. The split supply design (Figure 1) is a typical two op-amp hybrid. The receive op-amp serves two purposes. It supplies gain to amplify the receive signal to the proper level for the modem's detectors and demodulator, and it removes the transmitted signal from the receive signal present at the transformer. This is done by supplying a portion of the transmitted signal to the non-inverting input of the receive op-amp at the same amplitude as the signal appearing at the transformer, making the transmit signal common mode.

The single-supply hybrid is more complex than the dual-supply version described above, but its use eliminates the need for a second power supply. This circuit (Figure 2) uses a bridged drive to allow undistorted signals to be sent with a single 5 volt supply. Because DTMF tones utilize a higher amplitude than data, these signals will clip if a single-ended drive approach is used. The bridged driver uses an extra op-amp (U1A) to invert the signal coming from the gain setting op-amp (U1B) before sending it to the other leg of the transformer. Each op-amp then supplies half the drive signal to the transformer. The receive amplifier (U1C) picks off its signal at the junction of the impedance matching resistor and the transformer. Because the bottom leg of the transformer is being driven in one direction by U1A and the resistor is driven in the opposite direction at the same time by U1B, the junction of the transformer and resistor remains relatively constant and the receive signal is unaffected.

DESIGN CONSIDERATIONS

Silicon Systems' 1-chip modem products include all basic modem functions. This makes these devices adaptable for use in a variety of applications, and as easy to control as conventional digital bus peripherals.

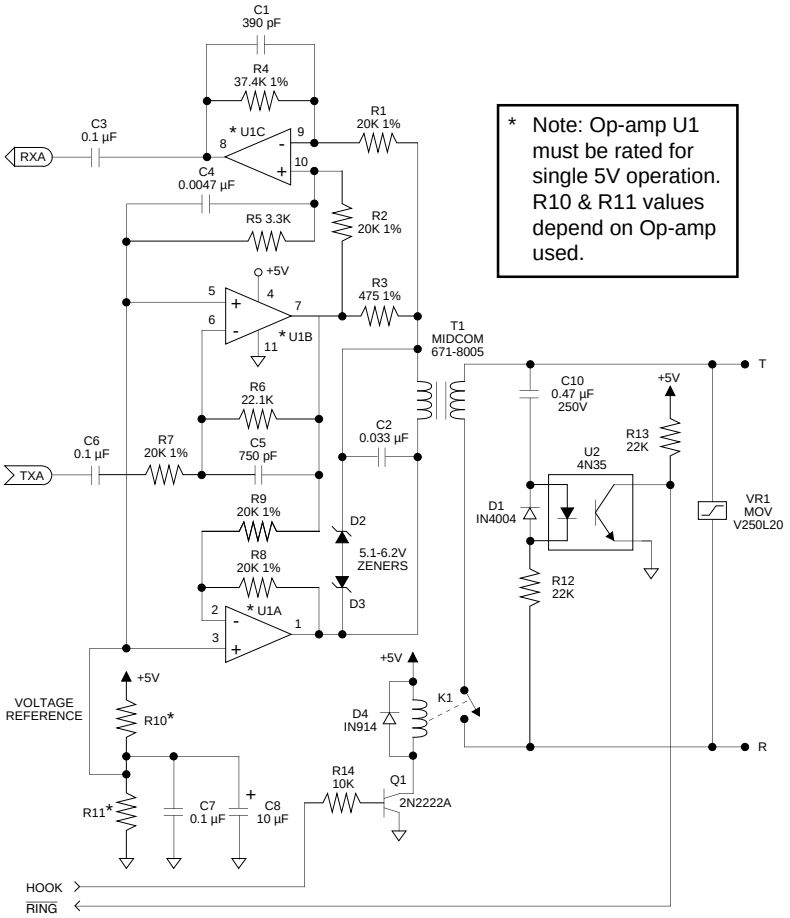


FIGURE 2: Single 5V Hybrid Version

Unlike digital logic circuitry, modem designs must properly contend with precise frequency tolerances and very low level analog signals, to ensure acceptable performance. Using good analog circuit design practices will generally result in a sound design. Following are additional recommendations which should be taken into consideration when starting new designs.

CRYSTAL OSCILLATOR

The K-Series crystal oscillator requires a parallel mode (antiresonant) crystal which operates at 11.0592 MHz. It is important that this frequency be maintained to within ±0.01% accuracy.

In order for a parallel mode crystal to operate correctly and to specification, it must have a load capacitor connected to the junction of each of the crystal and internal inverter connections, terminated to ground. The values of these capacitors depend primarily on the crystal's characteristics, and to a lesser degree on the internal inverter circuit. The values used affect the accuracy and start up characteristics of the oscillator.

LAYOUT CONSIDERATIONS

Good analog/digital design rules must be used to control system noise in order to obtain highest performance in modem designs. The more digital circuitry present on the PC board, the more this attention to noise control is needed. The modem should be treated as a high impedance analog device. A 22 µF electrolytic capacitor in parallel with a 0.22 µF ceramic capacitor between VDD and GND is recommended. Liberal use of ground planes and larger traces on power and ground are also highly favored. The ISET resistor and capacitor should be mounted near the ISET pin, away from digital signals. High speed digital circuits tend to generate a significant amount of EMI (Electro-Magnetic Interference) which must be minimized in order to meet regulatory agency limitations. To accomplish this, high speed digital devices should be locally bypassed, and the telephone line interface and K-Series device should be located close to each other near the area of the board where the phone line connection is accessed. To avoid problems, power supply and ground traces should be routed separately to the analog and digital functions on the board, and digital signals should not be routed near low level or high impedance analog traces. The analog and digital grounds should only connect at one point near the K-Series device ground pin to avoid ground loops. The K-Series modem IC's should have both high frequency and low frequency bypassing as close to the package as possible.

MODEM PERFORMANCE CHARACTERISTICS

The curves presented here define modem IC performance under a variety of line conditions while inducing disturbances that are typical of those encountered during data transmission on public service telephone lines. Test data was taken using an AEA Electronics' "Autotest I" modem test set and line simulator, operating under computer control. All tests were run full-duplex, using a Hayes SmartModem™ 2400 as the reference modem. A 511 pseudo-random-bit pattern was used for each data point. Noise was C-message weighted and all signal-to-noise (S/N) ratios reflect total power measurements similar to the CCITT V.56 measurement specification. The individual tests are defined as follows.

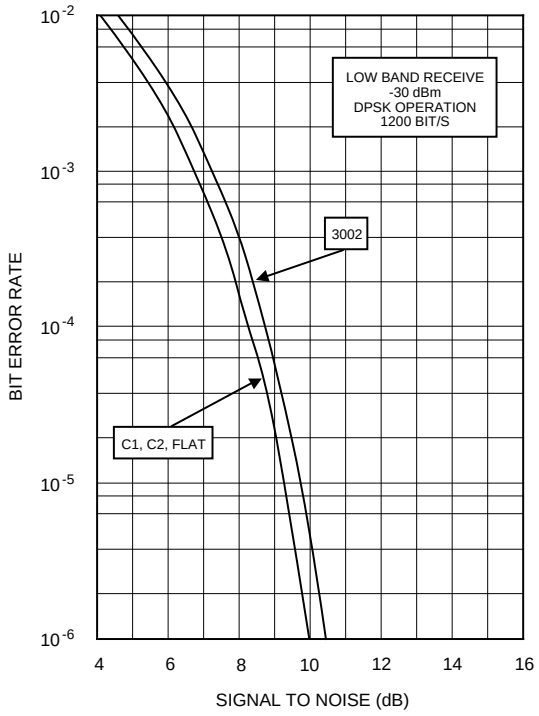
BER vs. S/N

This test measures the ability of the modem to operate over noisy lines with a minimum of data-transfer errors. Since some noise is generated in the best of dial-up lines, the modem must operate with the lowest S/N ratio possible. Better modem performance is indicated by test curves that are closest to the BER axis. A narrow spread between curves representing the four line parameters indicates minimal variation in performance while operating over a range of aberrant operating conditions. Typically, a modem will exhibit better BER-performance test curves receiving in the low band than in the high band.

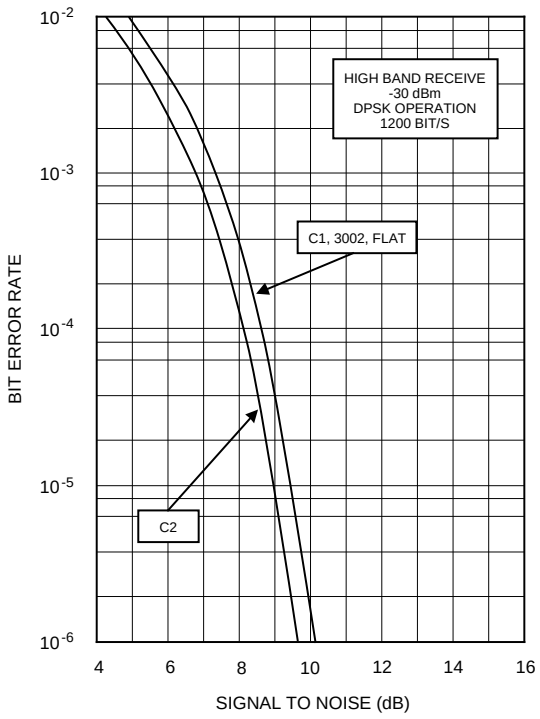
BER vs. Receive Level

This test measures the dynamic range of the modem. Because signal levels vary widely over dial-up lines, the widest possible dynamic range is desirable. The minimum Bell specification calls for 36 dB of dynamic range. S/N ratios are held constant at the indicated values while the receive level is lowered from a very high to very low signal levels. The width of the "bowl" of these curves, taken at the BER point, is the measure of dynamic range.

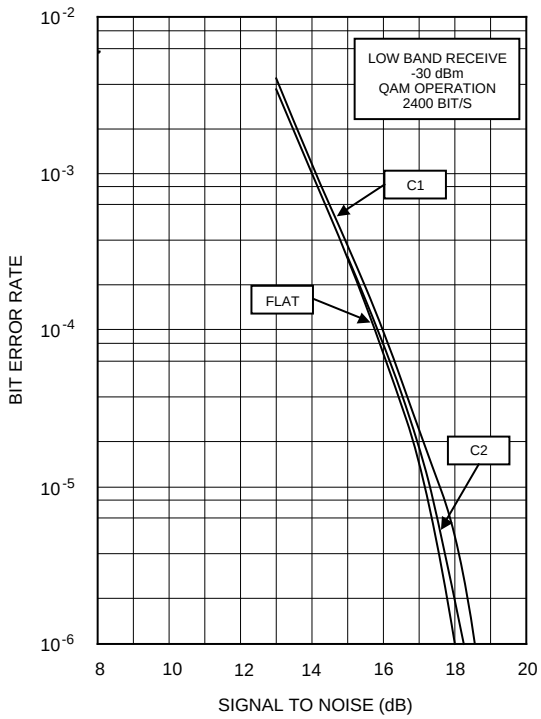
SSI 73K224L BER vs S/N-DPSK LOW BAND



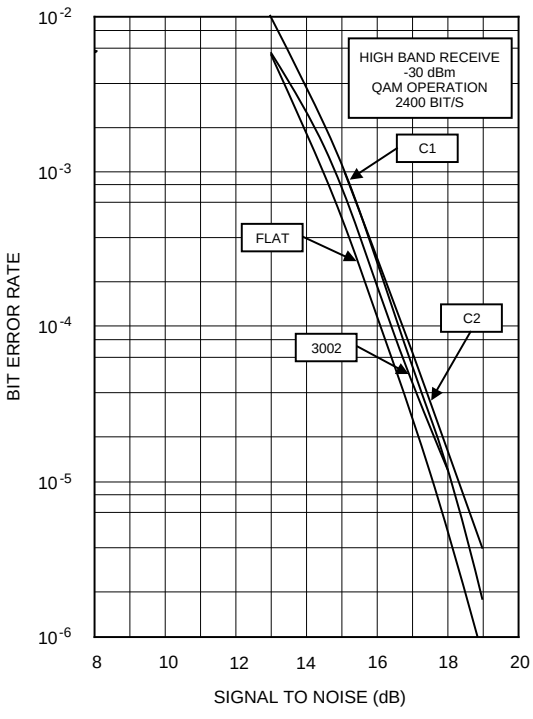
SSI 73K224L BER vs S/N-DPSK HIGH BAND

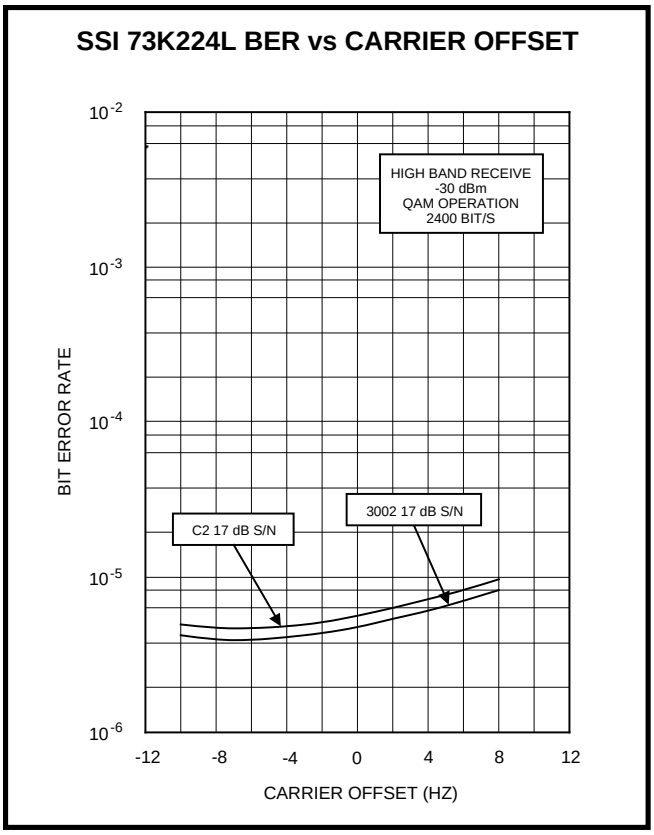


SSI 73K224L BER vs S/N-QAM-LOW BAND



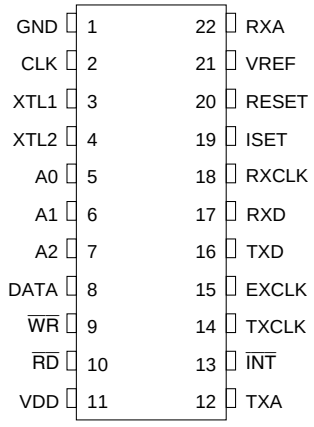
SSI 73K224L BER vs S/N-QAM-HIGH BAND



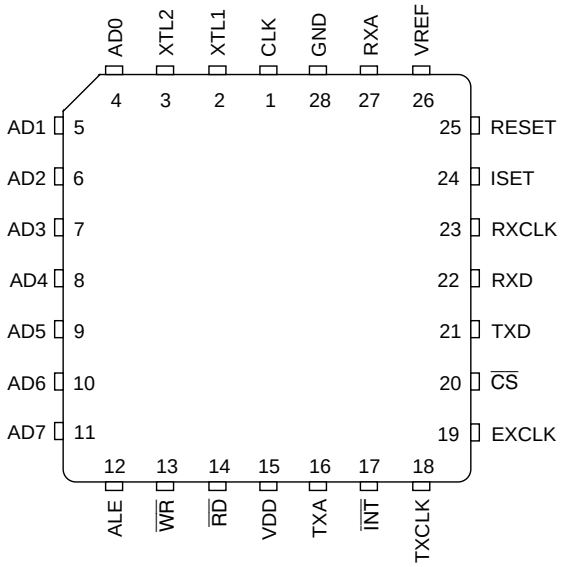

SSI 73K224L BER vs CARRIER OFFSET
HIGH BAND RECEIVE
-30 dBm
QAM OPERATION
2400 BIT/S
C2 17 dB S/N
3002 17 dB S/N
BIT ERROR RATE
10-2
10-3
10-4
10-5
10-6
-12
-8
-4
0
4
8
12
CARRIER OFFSET (HZ)

PACKAGE PIN DESIGNATIONS

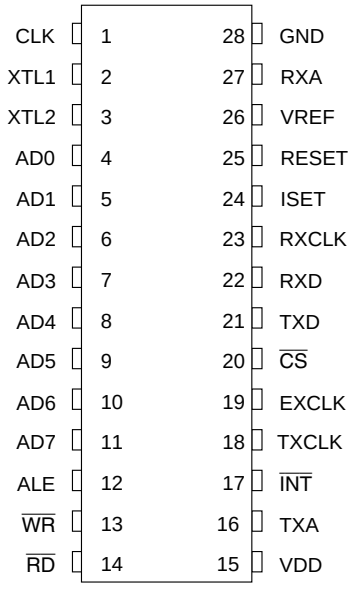
(Top View)



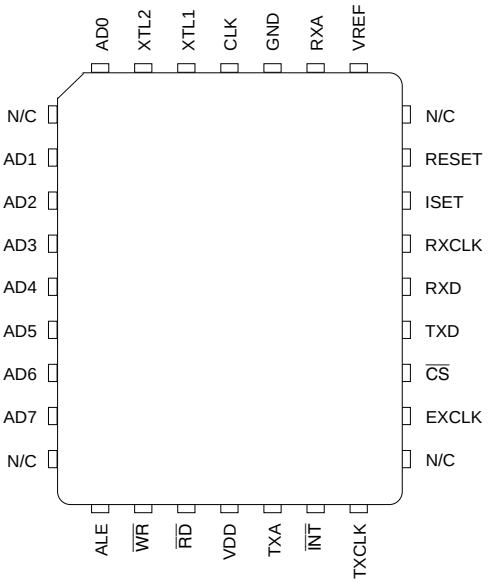
400-Mil
22-Pin DIP



28-Pin PLCC



600-Mil
28-Pin DIP

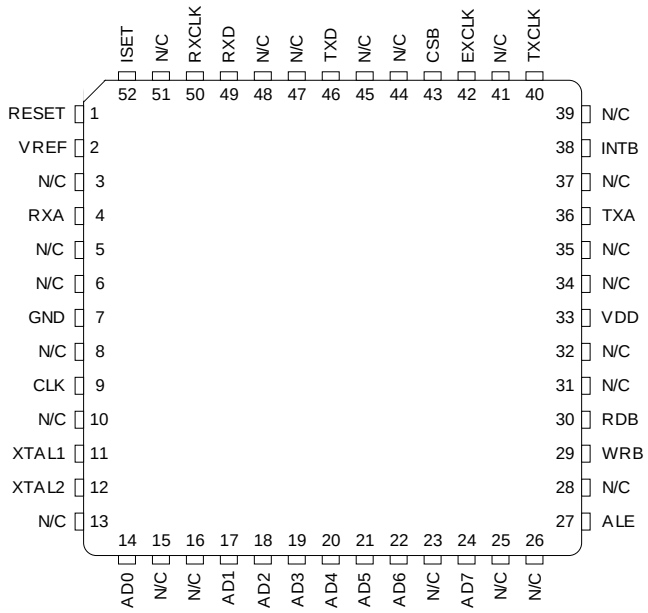


32-Pin PLCC

CAUTION: Use handling procedures necessary for a static sensitive component.

PACKAGE PIN DESIGNATIONS

(Top View)



52-Lead QFP

CAUTION: Use handling procedures necessary for a static sensitive component.

ORDERING INFORMATION

PART DESCRIPTION	ORDER NO.	PKG. MARK
SSI 73K224L		
22-Pin Plastic Dual In-Line	73K224LS-IP	73K224LS-IP
SSI 73K224L		
28-Pin Plastic Dual In-Line	73K224L-IP	73K224L-IP
28-Pin Plastic Leaded Chip Carrier	73K224L-28IH	73K224L-28IH
32-Pin Plastic Leaded Chip Carrier	73K224L-32IH	73K224L-32IH
52-Lead Quad Flat Pack Package	73K224L-IG	73K224L-IG

Silicon Systems, Inc. 14351 Myford Road, Tustin, CA 92680-7022, (714) 573-6000, FAX (714) 573-6914

SSI 73K302L
Bell 212A, 103, 202 Single-Chip Modem

February 1996

DESCRIPTION

The SSI 73K302L is a highly integrated single-chip modem IC which provides the functions needed to construct a Bell 202, 212A and 103 compatible modem. The SSI 73K302L is an enhancement of the SSI 73K212L single-chip modem with Bell 202 mode features added. The 73K302L is capable of 1200 or 0-300 bit/s full-duplex operation over dial-up lines. 4-wire full-duplex capability and a low speed back channel are also provided in Bell 202 mode. The SSI 73K302L recognizes and generates a 900 Hz soft carrier turn-off tone, and allows 103 for 300 bit/s FSK operation. The SSI 73K302L integrates analog, digital, and switched-capacitor array functions on a single substrate, offering excellent performance and a high level of functional integration in a single 28 or 22-pin DIP configuration. The SSI 73K302L operates from a single +5V supply with very low power consumption.

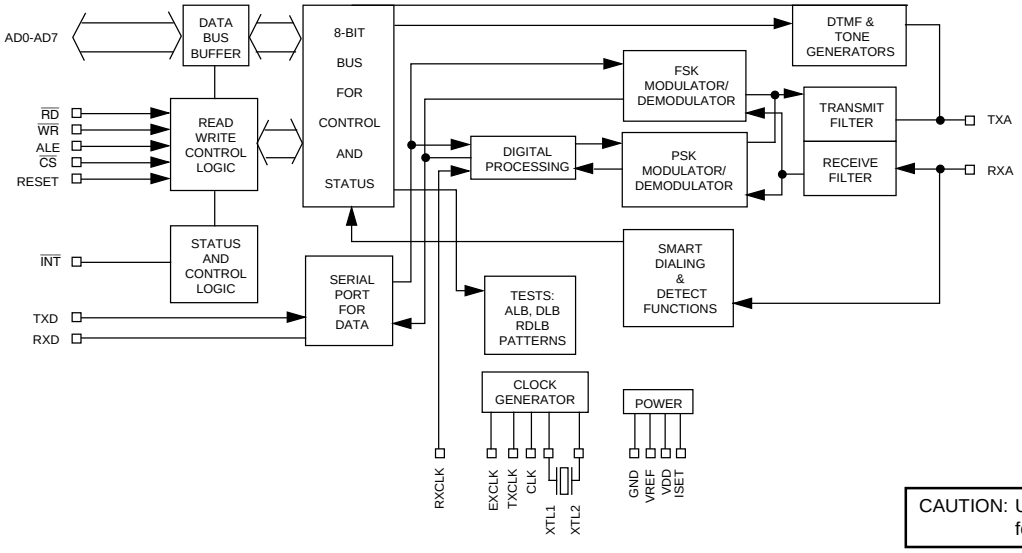
The SSI 73K302L includes the DPSK and FSK modulator/demodulator functions, call progress and handshake tone monitors, test modes, and a tone generator capable of producing DTMF, answer, and 900 Hz soft carrier turn-off tone. This device supports Bell 202, 212A and 103 modes of operation, allowing both

(continued)

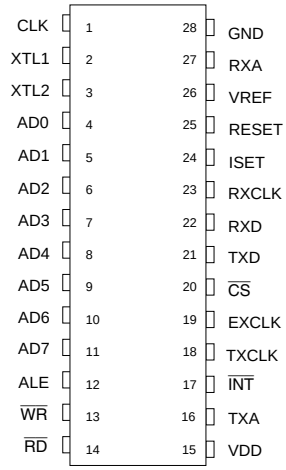
FEATURES

- **One-chip Bell 212A, 103 and 202S/T standard compatible modem data pump**
- **Full-duplex operation at 0-300 bit/s (FSK), 1200 bit/s (DPSK) or 0-1200 bit/s (FSK) forward channel with or without 0-150 bit/s back channel**
- **Full-duplex 4-wire operation in Bell 202 mode**
- **Pin and software compatible with other SSI K-Series 1-chip modems**
- **Interfaces directly with standard microprocessors (8048, 80C51 typical)**
- **Serial (22-pin DIP) or parallel microprocessor bus for control**
- **Serial port for data transfer**
- **Both synchronous and asynchronous modes of operation**
- **Call progress, carrier, precise answer tone (2225 Hz), soft carrier turn-off (SCT), and FSK mark detectors**
- **DTMF, answer, and SCT tone generators**
- **Test modes available: ALB, DL, RDL, Mark, Space, Alternating bit patterns**
- **CMOS technology for low power consumption using 35 mW @ 5V from a single power supply**

BLOCK DIAGRAM



PIN DIAGRAM



CAUTION: Use handling procedures necessary for a static sensitive component.

DESCRIPTION (continued)

synchronous and asynchronous communications. The SSI 73K302L is designed to appear to the systems designer as a microprocessor peripheral, and will easily interface with popular one-chip microprocessors (80C51 typical) for control of modem functions through its 8-bit multiplexed address/data bus or via an optional serial command bus. An ALE control line simplifies address demultiplexing. Data communications occurs through a separate serial port only.

The SSI 73K302L is ideal for use in either free standing or integral system modem products where multi-standard data communications is desired. Its high functionality, low power consumption and efficient packaging simplify design requirements and increase system reliability. A complete modem requires only the addition of the phone line interface, a modem controller, and RS232 level converter for a typical system.

Tri-mode capability in one-chip allows full-duplex Bell 212 and 103 operation or assymetrical Bell 202S operation over the 2-wire switched telephone network. 202T mode full-duplex operation at 1200 bit/s is also possible when operating on 4-wire leased lines.

A soft carrier turn-off feature facilitates fast line turn around when using the 202S mode for half-duplex applications.

The SSI 73K302L is part of Silicon Systems K-Series family of pin and function compatible single-chip modem products. These devices allow systems to be configured for higher speeds and Bell or CCITT operation with only a single component change.

OPERATION

ASYNCHRONOUS MODE

Data transmission for the DPSK mode requires that data ultimately be transmitted in a synchronous fashion. The SSI 73K302L includes ASYNC/SYNC and SYNC/ASYNC converters which delete or insert stop bits in order to transmit data at a regular rate. In asynchronous mode the serial data comes from the TXD pin into the ASYNC/SYNC converter. The ASYNC/SYNC converter accepts the data provided on the TXD pin which normally must be 1200 bit/s +1.0%, 2.5%. The rate converter will then insert or delete stop bits in order to output a signal which is 1200 bit/s ± .01% (±0.01% is the required synchronous data rate accuracy).

The SYNC/ASYNC converter also has an extended overspeed mode which allows selection of an output overspeed range of either +1% or +2.3%. In the extended overspeed mode, stop bits are output at 7/8 the normal width.

The serial data stream from the transmit buffer or the rate converter is passed through the data scrambler and onto the analog modulator. The data scrambler can be bypassed under processor control when unscrambled data must be transmitted. If serial input data contains a break signal through one character (including start and stop bits) the break will be extended to at least 2 • N + 3 bits long (where N is the number of transmitted bits/character).

Serial data from the demodulator is passed first through the data descrambler and then through the SYNC/ASYNC converter. The ASYNC/ASYNC converter will reinsert any deleted stop bits and output data at an intra-character rate (bit-to-bit timing) of no greater than 1219 bit/s. An incoming break signal (low through two characters) will be passed through without incorrectly inserting a stop bit.

SYNCHRONOUS MODE

The Bell 212A standard defines synchronous operation at 1200 bit/s. Operation is similar to that of the asynchronous mode except that data must be synchronized to a provided clock and no variation in data transfer rate is allowable. Serial input data appearing at TXD must be valid on the rising edge of TXCLK.

TXCLK is an internally derived signal in internal mode and is connected internally to the RXCLK pin in slave mode. Receive data at the RXD pin is clocked out on the falling edge of RXCLK. The ASYNCH/SYNCH converter is bypassed when synchronous mode is selected and data is transmitted out at the same rate as it is input.

DPSK MODULATOR/DEMODULATOR

In DPSK mode the SSI 73K302L modulates a serial bit stream into di-bit pairs that are represented by four possible phase shifts as prescribed by the Bell 212A standards. The base-band signal is then filtered to reduce intersymbol interference on the bandlimited 2-wire telephone line. Transmission occurs using either a 1200 Hz (originate mode) or 2400 Hz (answer mode) carrier. Demodulation is the reverse of the modulation process, with the incoming analog signal eventually

decoded into di-bits and converted back to a serial bit stream. The demodulator also recovers the clock which was encoded into the analog signal during modulation. Demodulation occurs using either a 1200 Hz carrier (answer mode or ALB originate mode) or a 2400 Hz carrier (originate mode or ALB answer mode). The SSI 73K302L uses a phase locked loop coherent demodulation technique for optimum receiver performance.

FSK MODULATOR/DEMODULATOR

The FSK modulator produces a frequency modulated analog output signal using two discrete frequencies to represent the binary data. Bell 103 mode uses 1270 and 1070 Hz (originate, mark and space) or 2225 and 2025 Hz (answer, mark and space). Bell 202 mode uses 1200 and 2200 Hz for the main channel and 387 and 487 Hz for the back channel. The modulation rate of the back channel is up to 150 baud. Demodulation involves detecting the received frequencies and decoding them into the appropriate binary value. The rate converter and scrambler/descrambler are automatically bypassed in the 103 or 202 modes.

PASSBAND FILTERS AND EQUALIZERS

High and low band filters are included to shape the amplitude and phase response of the transmit and receive signals and provide compromise delay equalization and rejection of out-of-band signals in the receive channel. Amplitude and phase equalization are necessary to compensate for distortion of the transmission line and to reduce intersymbol interference in the bandlimited receive signal. The transmit signal filtering approximates a 75% square root of raised Cosine frequency response characteristic.

AGC

The automatic gain control maintains a signal level at the input to the demodulators which is constant to within 1 dB. It corrects quickly for increases in signal which would cause clipping and provides a total receiver dynamic range of >45 dB.

PARALLEL BUS INTERFACE

Four 8-bit registers are provided for control, option select and status monitoring. These registers are addressed with the AD0, AD1, and AD2 multiplexed address lines (latched by ALE) and appear to a control microprocessor as four consecutive memory locations. Two control registers and the tone register are read/write memory. The detect register is read only and cannot be modified except by modem response to monitored parameters. The parallel bus interface is not available in the 22-pin package.

SERIAL COMMAND INTERFACE

The serial command interface allows access to the SSI 73K302L control and status registers via a serial command port. In this mode the A0, A1 and A2 lines provide register addresses for data passed through the data pin under control of the $\overline{RD}$ and $\overline{WR}$ lines. A read operation is initiated when the $\overline{RD}$ line is taken low. The first bit is available after $\overline{RD}$ is brough low and the next seven cycles of EXCLK will then transfer out seven bits of the selected address location LSB first. A write takes place by shifting in eight bits of data LSB first for eight consecutive cycles of EXCLK. $\overline{WR}$ is then pulsed low and data transfer into the selected register occurs on the rising edge of $\overline{WR}$.

SPECIAL DETECT CIRCUITRY

The special detect circuitry monitors the received analog signal to determine status or presence of carrier, answer tone and weak received signal (long loop condition), special tones such as FSK marking and the 900 Hz soft carrier turn-off tone are also detected. A highly frequency selective call progress detector provides adequate discrimination to accurately detect lower quality call progress signals.

DTMF GENERATOR

The DTMF generator will output one of 16 standard tone pairs determined by a 4-bit binary value and TX DTMF mode bit previously loaded into the tone register. Tone generation is initiated when the DTMF mode is selected using the tone register and the transmit enable (CR0 bit D1) is changed from 0 to 1.

SOFT CARRIER TURN-OFF TONE GENERATOR

The soft carrier turn-off tone generator will output a 900 Hz tone. When activated in Bell 202 main channel transmit mode, the output signal will shift to 900 Hz, maintaining phase continuity during the transition.

PIN DESCRIPTION

POWER

NAME	28-PIN	22-PIN	TYPE	DESCRIPTION
GND	28	1	I	System Ground.
VDD	15	11	I	Power supply input, 5V ±10%. Bypass with 0.1 and 22 µF capacitors to GND.
VREF	26	21	O	An internally generated reference voltage. Bypass with 0.1 µF capacitor to GND.
ISET	24	19	I	Chip current reference. Sets bias current for op-amps. The chip current is set by connecting this pin to VDD through a 2 MΩ resistor. ISET should be bypassed to GND with a 0.1 µF capacitor.

PARALLEL MICROPROCESSOR INTERFACE

ALE	12	-	I	Address latch enable. The falling edge of ALE latches the address on AD0-AD2 and the chip select on $\overline{CS}$.
AD0-AD7	4-11	-	I/O	Address/data bus. These bidirectional tri-state multi-plexed lines carry information to and from the internal registers.
$\overline{CS}$	20	-	I	Chip select. A low on this pin during the falling edge of ALE allows a read cycle or a write cycle to occur. AD0-AD7 will not be driven and no registers will be written if $\overline{CS}$ (latched) is not active. The state of $\overline{CS}$ is latched on the falling edge of ALE.
CLK	1	2	O	Output clock. This pin is selectable under processor control to be either the crystal frequency (for use as a processor clock) or 16 • the data rate for use as a baud rate clock in DPSK mode only. The pin defaults to the crystal frequency on reset.
$\overline{INT}$	17	13	O	Interrupt. This open drain output signal is used to inform the processor that a detect flag has occurred. The processor must then read the detect register to determine which detect triggered the interrupt. $\overline{INT}$ will stay low until the processor reads the detect register or does a full reset.
$\overline{RD}$	14	-	I	Read. A low requests a read of the SSI 73K302L internal registers. Data cannot be output unless both $\overline{RD}$ and the latched $\overline{CS}$ are active or low.
RESET	25	20	I	Reset. An active high signal on this pin will put the chip into an inactive state. All control register bits (CR0, CR1, Tone) will be reset. The output of the CLK pin will be set to the crystal frequency. An internal pull down resistor permits power on reset using a capacitor to VDD.

PARALLEL MICROPROCESSOR INTERFACE (continued)

NAME	28-PIN	22-PIN	TYPE	DESCRIPTION
$\overline{WR}$	13	-	I	Write. A low on this informs the SSI 73K302L that data is available on AD0-AD7 for writing into an internal register. Data is latched on the rising edge of $\overline{WR}$. No data is written unless both $\overline{WR}$ and the latched $\overline{CS}$ are active low.

SERIAL MICROPROCESSOR INTERFACE

A0-A2	-	5-7	I	Register Address Selection. These lines carry register addresses and should be valid during any read or write operation.
DATA	-	8	I/O	Serial Control Data. Data for a read/write operation is clocked in or out on the falling edge of the EXCLK pin. The direction of data flow is controlled by the $\overline{RD}$ pin. $\overline{RD}$ low outputs data. $\overline{RD}$ high inputs data.
$\overline{RD}$	-	10	I	Read. A low on this input informs the SSI 73K302L that data or status information is being read by the processor. The falling edge of the $\overline{RD}$ signal will initiate a read from the addressed register. The $\overline{RD}$ signal must continue for eight falling edges of EXCLK in order to read all eight bits of the referenced register. Read data is provided LSB first. Data will not be output unless the $\overline{RD}$ signal is active.
$\overline{WR}$	-	9	I	Write. A low on this input informs the SSI 73K302L that data or status information has been shifted in through the DATA pin and is available for writing to an internal register. The normal procedure for a write is to shift in data LSB first on the DATA pin for eight consecutive falling edges of EXCLK and then to pulse $\overline{WR}$ low. Data is written on the rising edge of $\overline{WR}$.

Note: In the serial, 22-pin version, the pins AD0-AD7, ALE and $\overline{CS}$ are removed and replaced with the pins; A0, A1, A2, DATA, and an unconnected pin. Also, the $\overline{RD}$ and $\overline{WR}$ controls are used differently.

The serial control mode is provided in the parallel control versions by tying ALE high and $\overline{CS}$ low. In this configuration AD7 becomes DATA and AD0, AD1 and AD2 become A0, A1 and A2, respectively.

PIN DESCRIPTION (continued)

DTE USER INTERFACE

NAME	28-PIN	22-PIN	TYPE	DESCRIPTION
EXCLK	19	15	I	External Clock. This signal is used only in synchronous DPSK transmission when the external timing option has been selected. In the external timing mode the rising edge of EXCLK is used to strobe synchronous DPSK transmit data available on the TXD pin. Also used for serial control interface.
RXCLK	23	18	O	Receive Clock. The falling edge of this clock output is coincident with the transitions in the serial received DPSK data output. The rising edge of RXCLK can be used to latch the valid output data. RXCLK will be valid as long as a carrier is present. In Bell 202 mode a clock which is 16 • 1200 or 16 • 150 baud data rate is output.
RXD	22	17	O/ Weak Pull-up	Received Data Output. Serial receive data is available on this pin. The data is always valid on the rising edge of RXCLK when in synchronous mode. RXD will output constant marks if no carrier is detected.
TXCLK	18	14	O	Transmit Clock.This signal is used only in synchronous DPSK transmission to latch serial input data on the TXD pin. Data must be provided so that valid data is available on the rising edge of the TXCLK. The transmit clock is derived from different sources depending upon the synchronization mode selection. In Internal Mode the clock is 1200 Hz generated internally. In External Mode TXCLK is phase locked to the EXCLK pin. In Slave Mode TXCLK is phase locked to the RXCLK pin. TXCLK is always active. In Bell 202 mode the output is a 16 • 1200 baud clock or 16 • 150 baud to drive a UART.
TXD	21	16	I	Transmit Data Input. Serial data for transmission is applied on this pin. In synchronous modes, the data must be valid on the rising edge of the TXCLK clock. In asynchronous modes (1200 or 300 baud) no clocking is necessary. DPSK must be 1200 bit/s +1%, -2.5% or +2.3%, -2.5% in extended overspeed mode.

ANALOG INTERFACE AND OSCILLATOR

RXA	27	22	I	Received modulated analog signal input from the telephone line interface.
TXA	16	12	O	Transmit analog output to the telephone line interface.
XTL1 XTL2	2 3	3 4	I I	These pins are for the internal crystal oscillator requiring a 11.0592 MHz parallel mode crystal and two load capacitors to Ground. XTL2 can also be driven from an external clock.

REGISTER DESCRIPTIONS

Four 8-bit internal registers are accessible for control and status monitoring. The registers are accessed in read or write operations by addressing the A0 and A1 address lines in serial mode, or the AD0 and AD1 lines in parallel mode. The AD0 and AD1 lines are latched by ALE. Register CR0 controls the method by which data is transferred over the phone line. CR1 controls the interface between the microprocessor and the SSI 73K302L internal state. DR is a detect register which provides an indication of monitored modem status conditions. TR, the tone control register, controls the DTMF generator, answer and guard tones and RXD output gate used in the modem initial connect sequence. All registers are read/write except for DR which is read only. Register control and status bits are identified below:

REGISTER BIT SUMMARY

	ADDRESS	DATA BIT NUMBER							
REGISTER	AD2 - AD0	D7	D6	D5	D4	D3	D2	D1	D0
CONTROL REGISTER 0 CR0	000	MODULATION OPTION	0	TRANSMIT MODE 3	TRANSMIT MODE 2	TRANSMIT MODE 1	TRANSMIT MODE 0	TRANSMIT ENABLE	ANSWER/ ORIGINATE
CONTROL REGISTER 1 CR1	001	TRANSMIT PATTERN 1	TRANSMIT PATTERN 0	ENABLE DETECT INTERRUPT	BYPASS SCRAMBLER/ ADD PH. EQ. 202	CLK CONTROL	RESET	TEST MODE 1	TEST MODE 0
DETECT REGISTER DR	010	X	X	RECEIVE DATA	UNSCR. MARKS	CARRIER DETECT	SPECIAL TONE	CALL PROGRESS	LONG LOOP
TONE CONTROL REGISTER TR	011	RXD OUTPUT CONTROL	TRANSMIT SCT TONE	TRANSMIT ANSWER TONE	TRANSMIT DTMF	DTMF3	DTMF/ 202T FDX	DTMF1/ OVERSPEED	DTMF0/ SPEC. TONE/ ANSWER TONE/ SELECT
ID REGISTER ID	110	ID	ID	ID	ID	X	X	X	X

NOTE: When a register containing reserved control bits is written into, the reserved bits must be programmed as 0's.

X = Undefined, mask in software

REGISTER ADDRESS TABLE

REGISTER	ADDRESS AD2 - AD0	DATA BIT NUMBER D7	D6	D5	D4	D3	D2	D1	D0
CONTROL REGISTER 0 CR0	000	MODULATION OPTION	0	TRANSMIT MODE 3	TRANSMIT MODE 2	TRANSMIT MODE 1	TRANSMIT MODE 0	TRANSMIT ENABLE	ORIGINATE/ ANSWER
CONTROL REGISTER 1 CR1	001	TRANSMIT PATTERN 1	TRANSMIT PATTERN 0	ENABLE DETECT INTERRUPT	BYPASS SCRAMBLER/ ADD PH. EQ.	CLK CONTROL	RESET	TEST MODE 1	TEST MODE 0
DETECT REGISTER DR	010	X	X	RECEIVE DATA	UNSCR. MARKS	CARRIER DETECT	SPECIAL TONE	CALL PROGRESS	LONG LOOP
TONE CONTROL REGISTER TR	011	RXD OUTPUT CONTROL	TRANSMIT SCT TONE	TRANSMIT ANSWER TONE	TRANSMIT DTMF	DTMF3	DTMF2/ 202T FDX	DTMF1/ OVERSPEED	DTMF0/ SPECIAL TONE
ID REGISTER 10	110	ID	ID	ID	ID	X	X	X	X

0=103 FSK
1=202 FSK

0000=PWR DOWN
1100=FSK
0010=EXT SYNCH
0011=SLAVE SYNCH
0100=ASYNCH 8 BITS/CHAR
0101=ASYNCH 9 BITS/CHAR
0110=ASYNCH 10 BITS/CHAR
0111=ASYNCH 11 BITS/CHAR
1100=FSK BELL 103 OR 202

0=DISABLE TXA OUTPUT
1=ENABLE TXA OUTPUT

IN 212, 103 MODES:
0=ANSWER
1=ORIGINATE

IN 202 MODE:
0=RECEIVE @ 1200 BIT/S, TRANSMIT @ 150 BIT/S
1=RECEIVE @ 150 BIT/S, TRANSMIT @ 1200 BIT/S

00=TX DATA
01=TX ALTERNATE
10=TX MARK
11=TX SPACE

0=DISABLE
1=ENABLE

0=NORMAL
1=BYPASS SCRAMBLER
1=ADD EXTRA PHASE EQ. IN 202 ONLY

0=XTAL
1=16 X DATA RATE OUTPUT AT CLK PIN IN DPSK MODE ONLY

0=NORMAL
1=RESET

00=NORMAL
01=ANALOG LOOPBACK
10=REMOTE DIGITAL LOOPBACK
11=LOCAL DIGITAL LOOPBACK

OUTPUTS RECEIVED DATA STREAM

0=CONDITION NOT DETECTED
1=CONDITION DETECTED

RXD PIN
0=NORMAL
1=TRI STATE

0=OFF
1=ON

0=OFF
1=ON

0=DATA
1=TX DTMF

4 BIT CODE FOR 1 OF 16 DUAL TONE COMBINATIONS.

0=NORMAL OPERATION
1=FULL DUPLEX IN 202 MODE

0=1%
1=2.5%

0=900 HZ SCT TONE IF IN ANSWER MODE
=2225 HZ ANSWER TONE IN 103 OR 212 ORIGINATE MODES
1=FSK MARK

00XX=73K212L, 322L, 321L
01XX=73K221L, 302L
10XX=73K222L
1100=73K224L
1110=73K324L

X = Undefined, mask in software
0 = Only write zeros to this location

CONTROL REGISTER 0

	D7	D6	D5	D4	D3	D2	D1	D0
CR0 000	MODUL. OPTION	0	TRANSMIT MODE 3	TRANSMIT MODE 2	TRANSMIT MODE 1	TRANSMIT MODE 0	TRANSMIT ENABLE	ANSWER/ ORIGINATE

BIT NO.	NAME	CONDITION	DESCRIPTION
D0	Answer/ Originate	0	Selects answer mode in 103 and 212A modes (transmit in high band, receive in low band) or in Bell 202 mode, receive at 1200 bit/s and transmit at 150 bit/s.
		1	Selects originate mode in 103 and 212A modes (transmit in low band, receive in high band) or in Bell 202 mode, receive at 150 bit/s and transmit at 1200 bit/s.
			Note: This bit works with TR bit D0 to program special tones detected in Tone Register. See detect and tone registers.
D1	Transmit Enable	0	Disables transmit output at TXA.
		1	Enables transmit output at TXA.
			Note: Answer tone and DTMF TX control require TX enable.
D5, D4,D3, D2	Transmit Mode	D5 D4 D3 D2	
		0 0 0 0	Selects power down mode. All functions disabled except digital interface.
		0 0 0 1	Internal synchronous mode. In this mode TXCLK is an internally derived 1200 Hz signal. Serial input data appearing at TXD must be valid on the rising edge of TXCLK. Receive data is clocked out of RXD on the falling edge of RXCLK.
		0 0 1 0	External synchronous mode. Operation is identical to internal synchronous, but TXCLK is connected internally to EXCLK pin, and a 1200 Hz $\pm$ 0.01% clock must be supplied externally.
		0 0 1 1	Slave synchronous mode. Same operation as other synchronous modes. TXCLK is connected internally to the RXCLK pin in this mode.
		0 1 0 0	Selects DPSK asynchronous mode - 8 bits/character (1 start bit, 6 data bits, 1 stop bit).
		0 1 0 1	Selects DPSK asynchronous mode - 9 bits/character (1 start bit, 7 data bits, 1 stop bit).
		0 1 1 0	Selects DPSK asynchronous mode - 10 bits/character (1 start bit, 8 data bits, 1 stop bit).
		0 1 1 1	Selects DPSK asynchronous mode - 11 bits/character (1 start bit, 8 data bits, Parity and 1 or 2 stop bits).
		1 1 0 0	Selects 103 or 202 FSK operation.

CONTROL REGISTER 0 (continued)

	D7	D6	D5	D4	D3	D2	D1	D0
CR0 000	MODUL. OPTION	0	TRANSMIT MODE 3	TRANSMIT MODE 2	TRANSMIT MODE 1	TRANSMIT MODE 0	TRANSMIT ENABLE	ANSWER/ ORIGINATE

BIT NO.	NAME	CONDITION	DESCRIPTION
D6		0	Not used; must be written as a "0."
D7	Modulation Option	D7 D5 D4	Selects:
		X 0 X	DPSK asynchronous mode at 1200 bit/s.
		0 1 1	FSK Bell 103 mode.
		1 1 1	FSK Bell 202 mode.

CONTROL REGISTER 1

	D7	D6	D5	D4	D3	D2	D1	D0
CR1 001	TRANSMIT PATTERN 1	TRANSMIT PATTERN 0	ENABLE DETECT INTER.	BYPASS SCRAMB/ ADD PH. EQ.	CLK CONTROL	RESET	TEST MODE 1	TEST MODE 0

BIT NO.	NAME	CONDITION	DESCRIPTION
D1, D0	Test Mode	D1 D0	
		0 0	Selects normal operating mode.
		0 1	Analog loopback mode. Loops the transmitted analog signal back to the receiver, and causes the receiver to use the same center frequency as the transmitter. To squelch the TXA pin, transmit enable must be forced low. Not supported in FDX202 mode.
		1 0	Selects remote digital loopback. Received data is looped back to transmit data internally, and RXD is forced to a mark. Data on TXD is ignored.
		1 1	Selects local digital loopback. Internally loops TXD back to RXD and continues to transmit carrier from TXA pin.
D2	Reset	0	Selects normal operation.
		1	Resets modem to power down state. All control register bits (CR0, CR1, Tone) are reset to zero. The output of the CLK pin will be set to the crystal frequency.

CONTROL REGISTER 1 (continued)

	D7	D6	D5	D4	D3	D2	D1	D0
CR1 001	TRANSMIT PATTERN 1	TRANSMIT PATTERN 0	ENABLE DETECT INTER.	BYPASS SCRAMB/ ADD PH. EQ.	CLK CONTROL	RESET	TEST MODE 1	TEST MODE 0

BIT NO.	NAME	CONDITION	DESCRIPTION
D3	CLK Control	0	Selects 11.0592 MHz crystal echo output at CLK pin.
		1	Selects 16 • the data rate, output at CLK pin in DPSK modes only.
D4*	Bypass Scrambler/ Add Phase Equalization	0	Selects normal operation. DPSK data is passed through scrambler.
		1	Selects Scrambler Bypass. DPSK data is routed around scrambler in the transmit path. In Bell 202 mode, additional phase equalization is added to the main channel filters when D4 is set to 1.
D5	Enable Detect Interrupt	0	Disables interrupt at $\overline{INT}$ pin.
		1	Enables $\overline{INT}$ output. An interrupt will be generated with a change in status of DR bits D1-D4. The special tone and call progress detect interrupts are masked when the TX enable bit is set. Carrier detect is masked when TX DTMF is activated. All interrupts will be disabled if the device is in power down mode.
D7, D6	Transmit Pattern	D7 D6	
		0 0	Selects normal data transmission as controlled by the state of the TXD pin.
		0 1	Selects an alternating mark/space transmit pattern for modem testing.
		1 0	Selects a constant mark transmit pattern.
		1 1	Selects a constant space transmit pattern.

* D4 should always be set to 1 when receiving 1200 bit/s data and to 0 when transmitting 1200 bit/s data in 202 mode.

DETECT REGISTER

	D7	D6	D5	D4	D3	D2	D1	D0
DR 010	X	X	RECEIVE DATA	UNSCR. MARK	CARR. DETECT	SPECIAL TONE	CALL PROG.	LONG LOOP

BIT NO.	NAME	CONDITION	DESCRIPTION
D0	Long Loop	0	Indicates normal received signal.
		1	Indicates low received signal level.
D1	Call Progress Detect	0	No call progress tone detected.
		1	Indicates presence of call progress tones. The call progress detection circuitry is activated by energy in the normal 350 to 620 Hz call progress band.
D2	Special Tone Detect	0	No special tone detected as programmed by CR0 bit D0 and Tone Register bit D0.
		1	Special tone detected. The detected tone is:
			(1) 2225 Hz answer tone if D0 of TR=0 and the device is in Bell 103 or 212A originate mode.
			(2) Soft carrier turn-off tone if D0 of TR=0 and the device is in Bell 202 answer mode.
			(3) an FSK mark in the mode the device is set to receive if D0 of TR is set to 1.
			Tolerance on special tones is ±3%.
D3	Carrier Detect	0	No carrier detected in the receive channel.
		1	Indicated carrier has been detected in the received channel.
D4	Unscrambled Mark Detect	0	No unscrambled mark.
		1	(DPSK only) Indicates detection of unscrambled marks in the received data. A valid indication requires that unscrambled marks be received for > 165.5 ±6.5 ms.
D5	Receive Data		Continuously outputs the received data stream. This data is the same as that output on the RXD pin, but it is not disabled when RXD is tri-stated.
D6, D7	Not Used	Undefined	Mask in software

TONE REGISTER

	D7	D6	D5	D4	D3	D2	D1	D0
TR 011	RXD OUTPUT CONTR.	TRANSMIT SOFT CARRIER TURN-OFF TONE	TRANSMIT ANSWER TONE	TRANSMIT DTMF	DTMF 3	DTMF 2/ 202 FDX	DTMF 1/ OVER-SPEED	DTMF 0/ SPECIAL TONE SEL

BIT NO.	NAME	CONDITION	DESCRIPTION
D0	DTMF 0/ Special Tone Detect/Select	D5 D4 D0	D0 interacts with bits D6, D4, and CR0 as shown.
		0 1 X	Transmit DTMF tones.
		0 0 0	2225 Hz answer tone will be detected in D2 of DR if originate mode is selected in CR0.
			900 Hz SCT tone will be detected in D2 of DR if Bell 202 answer mode is selected in CR0.
		X 0 1	Mark of an FSK mode selected in CR0 is to be detected in D2 of DR.
		1 0 0	2225 Hz answer tone will be generated when in answer mode and transmit enable is selected in CR0.
		1 0 1	2100 Hz answer tone will be generated when in answer mode and transmit enable is selected in CR0.
D1	DTMF 1/ Overspeed	D4 D1	D1 interacts with D4 as shown.
		0 0	Asynchronous DPSK 1200 bit/s +1.0% -2.5%.
		0 1	Asynchronous DPSK 1200 bit/s +2.3% -2.5%.
D2	DTMF2/202T	0	Enables 202 half-duplex operation if TR D4 = 0
	FDX	1	Enables 202 full-duplex operation if TR D4 = 0
D3, D2, D1, D0	DTMF 3, 2, 1, 0	D3 D2 D1 D0	
		0 0 0 0 - 1 1 1 1	Programs 1 of 16 DTMF tone pairs that will be transmitted when TX DTMF and TX enable bit (CR0, bit D1) are set. Tone encoding is shown below:

KEYBOARD EQUIVALENT	DTMF CODE D3 D2 D1 D0	TONES LOW HIGH
1	0 0 0 1	697 1209
2	0 0 1 0	697 1336
3	0 0 1 1	697 1477
4	0 1 0 0	770 1209
5	0 1 0 1	770 1336
6	0 1 1 0	770 1477
7	0 1 1 1	852 1209
8	1 0 0 0	852 1336
9	1 0 0 1	852 1477
0	1 0 1 0	941 1336

TONE REGISTER (continued)

	D7	D6	D5	D4	D3	D2	D1	D0
TR 011	RXD OUTPUT CONTR.	TRANSMIT SOFT CARRIER TURN-OFF TONE	TRANSMIT ANSWER TONE	TRANSMIT DTMF	DTMF 3	DTMF 2/ 202T FDX	DTMF 1/ OVER-SPEED	DTMF 0/ SPECIAL TONE SEL

BIT NO.	NAME	CONDITION	DESCRIPTION
D3, D2, D1, D0 (cont.)			KEYBOARD EQUIVALENT / DTMF CODE D3 D2 D1 D0 / TONES LOW HIGH * 1 0 1 1 941 1209 # 1 1 0 0 941 1477 A 1 1 0 1 697 1633 B 1 1 1 0 770 1633 C 1 1 1 1 852 1633 D 0 0 0 0 941 1633
D4	Transmit DTMF	0	Disable DTMF.
		1	Activate DTMF. The selected DTMF tones are transmitted continuously when this bit is high. TX DTMF overrides all other transmit functions.
D5	Transmit Answer Tone	0	Disables answer tone generator.
		1	Enables answer tone generator. A 2225 Hz answer tone will be transmitted continuously when the transmit enable bit is set. To transmit answer tone, the device must be in answer mode.
D6	Transmit SCT Tone	0	Disables SCT tone generator.
		1	Transmit SCT tone in Bell 202 mode.
D7	RXD Output Control	0	Enables RXD pin. Receive data will be output on RXD.
		1	Disables RXD pin. The RXD pin reverts to a high impedance with internal weak pull-up resistor.

Notes for Tone Register use:

1. To detect SCT tone, 202 answer mode must be selected. To transmit SCT tone, 202 originate mode must be selected.
2. For answer tone detection, 103 or 212 originate mode must be active. To transmit answer tone, the 73K302 must be in 103 or 212 answer mode.
3. After completion of DTMF dialing, bit D2 should be reset unless 202 full-duplex mode is selected.

ID REGISTER

	D7	D6	D5	D4	D3	D2	D1	D0
ID 110	ID	ID	ID	ID	X	X	X	X

BIT NO.	NAME	CONDITION	DESCRIPTION
D7, D6, D5, D4	Device Identification Signature	D7 D6 D5 D4	Indicates Device:
		0 0 X X	SSI 73K212L, 73K321L or 73K322L or 73K321L
		0 1 X X	SSI 73K221L or 73K302L
		1 0 X X	SSI 73K222L
		1 1 0 0	SSI 73K224L
		1 1 1 0	SSI 73K324L
D3-D0	Not Used	Undefined	Mask in software

ELECTRICAL SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING
VDD Supply Voltage	14V
Storage Temperature	-65 to 150°C
Soldering Temperature (10 sec.)	260°C
Applied Voltage	-0.3 to VDD + 0.3V
Note: All inputs and outputs are protected from static charge using built-in, industry standard protection devices and all outputs are short-circuit protected.	

RECOMMENDED OPERATING CONDITIONS

PARAMETER	CONDITION	MIN	NOM	MAX	UNIT
VDD Supply voltage		4.5	5	5.5	V
TA, Operating Free-Air Temp.		-40		+85	°C
Clock Variation	(11.0592 MHz) Crystal or external clock	-0.01		+0.01	%
External Components (Refer to Application section for placement.)					
VREF Bypass Capacitor	(External to GND)	0.1			µF
Bias setting resistor	(Placed between VDD and ISET pins)	1.8	2	2.2	MΩ
ISET Bypass Capacitor	(ISET pin to GND)	0.1			µF
VDD Bypass Capacitor 1	(External to GND)	0.1			µF
VDD Bypass Capacitor 2	(External to GND)	22			µF
XTL1 Load Capacitor	Depends on crystal characteristics;			40	pF
XTL2 Load Capacitor	from pin to GND			20	

ELECTRICAL SPECIFICATIONS (continued)

DC ELECTRICAL CHARACTERISTICS

(TA = -40°C to 85°C, VDD = recommended range unless otherwise noted.)

PARAMETER	CONDITION	MIN	NOM	MAX	UNIT
IDD, Supply Current	ISET Resistor = 2 MΩ				
IDDA, Active	CLK = 11.0592 MHz		8	12	mA
IDD1, Power-down	CLK = 11.0592 MHz			4	mA
IDD2, Power-down	CLK = 19.200 kHz			3	mA
Digital Inputs					
VIH, Input High Voltage					
Reset, XTL1, XTL2		3.0		VDD	V
All other inputs		2.0		VDD	V
VIL, Input Low Voltage		0		0.8	V
IIH, Input High Current	VI = VIH Max			100	µA
IIL, Input Low Current	VI = VIL Min	-200			µA
Reset Pull-down Current	Reset = VDD	1		50	µA
Input Capacitance	All Digital Input Pins			10	pF
Digital Outputs					
VOH, Output High Voltage	IOH MIN = -0.4 mA	2.4		VDD	V
VOL, Output Low Voltage	IO MAX = 1.6 mA			0.4	V
VOL, CLK Output	IO = 3.6 mA			0.6	V
RXD Tri-State Pull-up Curr.	RXD = GND	-1		-50	µA
CMAX, CLK Output	Maximum Capacitive Load			15	pF
Capacitance					
Inputs	Capacitance, all Digital Input pins			10	pF
XTL1, 2 Load Capacitors	Depends on crystal	15		60	pF
CLK	Maximum Capacitive Load			15	pF

DYNAMIC CHARACTERISTICS AND TIMING
(TA = -40°C to +85°C, VDD = recommended range unless otherwise noted.)

PARAMETER	CONDITION	MIN	NOM	MAX	UNIT
DPSK Modulator					
Carrier Suppression	Measured at TXA	45			dB
Output Amplitude	TX scrambled marks	-11	-10	-9	dBm0
FSK Modulator					
Output Freq. Error	CLK = 11.0592 MHz	-0.35		+0.35	%
Transmit Level	Transmit Dotting Pattern	-11	-10	-9	dBm0
Soft Carrier Turnoff Tone		-11.9	-10.9	-9.9	dBm0
Harmonic Distortion in 700-2900 Hz band	THD in the alternate band DPSK or FSK		-60	-50	dB
Output Bias Distortion	Transmit Dotting Pattern In ALB @ RXD		±3		%
Total Output Jitter	Random Input in ALB @ RXD	-10		+10	%
DTMF Generator	Must not be in 202 mode				
Freq. Accuracy		-0.25		+0.25	%
Output Amplitude, Low group	DPSK mode	-10	-9	-8	dBm0
Output Amplitude, High group	DPSK mode	-8	-7	-6	dBm0
Twist	High-Band to Low-Band	1.0	2.0	3.0	dB
Long Loop Detect	With Sinusoid	-38		-28	dBm0
Dynamic Range	Refer to Performance Curves		45		dB

Note: Parameters expressed in dBm0 refer to the following definition:

5V Version:
0 dB loss in the Transmit path to the line.
2 dB gain in the Receive path from the line.

Refer to the Basic Box Modem diagram in the Applications section for the DAA design.

DYNAMIC CHARACTERISTICS AND TIMING (continued)

PARAMETER	CONDITION	MIN	NOM	MAX	UNIT
Call Progress Detector					
Detect Level	-3 dB points in 285 and 675 Hz	-38			dBm0
Reject Level	Test signal is a 460 Hz sinusoid			-45	dBm0
Delay Time	-70 dBm0 to -30 dBm0 STEP	20		40	ms
Hold Time	-30 dBm0 to -70 dBm0 STEP	20		40	ms
Hysteresis		2			dB
Carrier Detect					
Threshold	DPSK or FSK receive data	-49		-42	dBm0
Delay Time					
Bell 103		8		20	ms
Bell 212A		15		32	ms
Bell 202 Forward Channel		6		12	ms
Bell 202 Back Channel		25		40	ms
Hold Time					
Bell 103		6		20	ms
Bell 212A		10		24	ms
Bell 202 Forward Channel		3		8	ms
Bell 202 Back Channel		10		25	ms
Hysteresis		2			dB
Special Tone Detectors					
Detect Level	See definitions for TR bit D0 mode	-49		-42	dBm0
Delay Time					
Answer tone		10		25	ms
900 Hz SCT tone	Preceded by valid carrier*	4		10	ms
202 Main Channel Mark		10		25	ms
202 Back Channel Mark		20		65	ms
1270 or 2225 Hz marks		10		25	ms

* If SCT duration >4ms, it is guaranteed to detect.

DYNAMIC CHARACTERISTICS AND TIMING (continued)

PARAMETER	CONDITION	MIN	NOM	MAX	UNIT
Special Tone Detectors (continued)					
Hold Time					
Answer tone		4		15	ms
900 Hz SCT tone		1		10	ms
202 Main Channel Mark		3		10	ms
202 Back Channel Mark		10		25	ms
1270 or 2225 Hz marks		5		15	ms
Hysteresis		2			dB
Detect Freq. Range	Any Special Tone	-3		+3	%
Output Smoothing Filter					
Output load	TXA pin; FSK Single Tone out for THD = -50 dB in 0.3 to 3.4 kHz	10			kΩ
				50	pF
Out of Band Energy	Frequency >12 kHz in all modes See Transmit Energy Spectrum			-60	dBm0
Output Impedance	TXA pin		20	50	Ω
Clock Noise	TXA pin; 76.8 kHz or 122.88 kHz in 202 main channel		0.1	0.4	mVrms
Carrier VCO					
Capture Range	Originate or Answer	-10		+10	Hz
Capture Time	-10 Hz to +10 Hz Carrier Frequency Change		40	100	ms
DPSK Recovered Clock					
Capture Range	% of data rate (center at 1200 Hz)	-625		+625	ppm
Data Delay Time	Analog data in at RXA pin to receive data valid at RXD pin		30	50	ms
Tone Generator					
Tone Accuracy	DTMF or FSK tones	-5		+5	Hz
Tone Level	For DTMF, must not be in 202 mode	-1		+1	dB

DYNAMIC CHARACTERISTICS AND TIMING (continued)

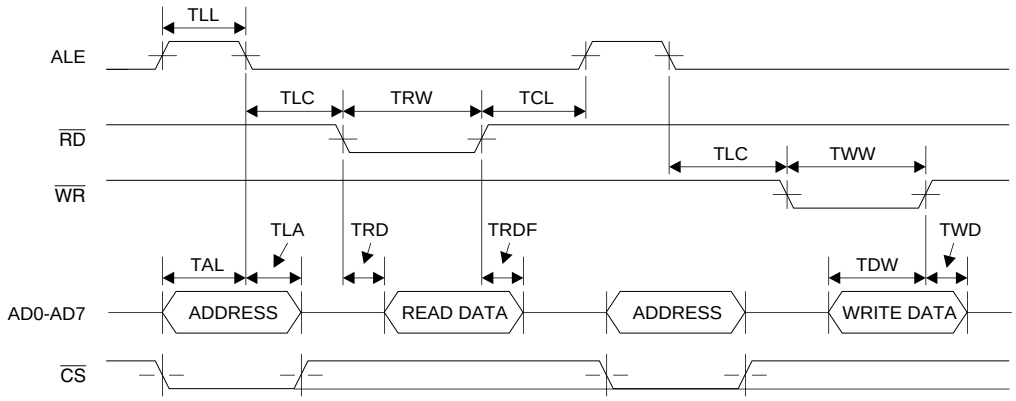
PARAMETER	CONDITION	MIN	NOM	MAX	UNIT
Timing (Refer to Timing Diagrams)					
TAL	$\overline{CS}$/Addr. setup before ALE Low	25			ns
TLA	$\overline{CS}$/Addr. hold after ALE Low	20			ns
TLC	ALE Low to $\overline{RD}$/$\overline{WR}$ Low	30			ns
TCL	$\overline{RD}$/$\overline{WR}$ Control to ALE High	-5			ns
TRD	Data out from $\overline{RD}$ Low	0		140	ns
TLL	ALE width	30			ns
TRDF	Data float after $\overline{RD}$ High	0		5	ns
TRW	$\overline{RD}$ width	200		25000	ns
TWW	$\overline{WR}$ width	140		25000	ns
TDW	Data setup before $\overline{WR}$ High	40			ns
TWD	Data hold after $\overline{WR}$ High	10			ns
TCKD	Data out after EXCLK Low			200	ns
TCKW	$\overline{WR}$ after EXCLK Low	150			ns
TDCK	Data setup before EXCLK Low	150			ns
TAC	Address setup before control*	50			ns
TCA	Address hold after control*	50			ns
TWH	Data Hold after EXCLK	20			

* Control for setup is the falling edge of $\overline{RD}$ or $\overline{WR}$.
Control for hold is the falling edge of $\overline{RD}$ or the rising edge of $\overline{WR}$.

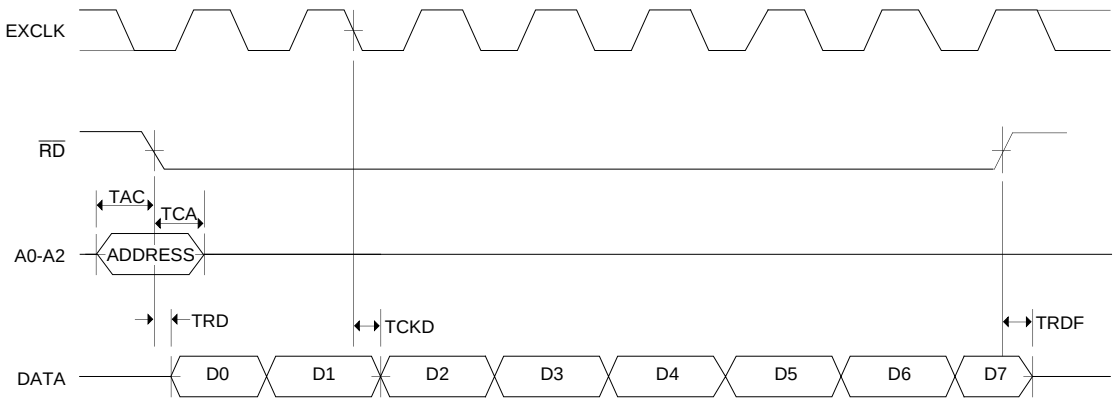
NOTE: Asserting ALE, $\overline{CS}$, and $\overline{RD}$ or $\overline{WR}$ concurrently can cause unintentional register accesses. When using non-8031 compatible processors, care must be taken to prevent this from occurring when designing the interface logic.

TIMING DIAGRAMS

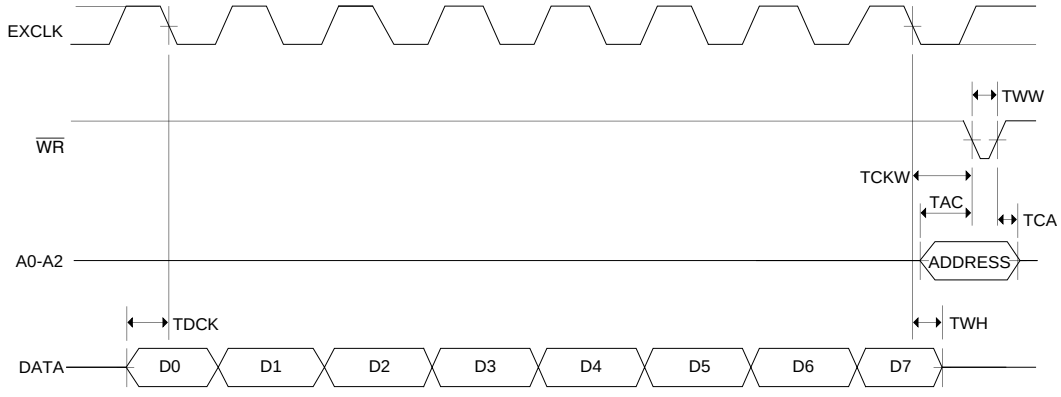
BUS TIMING DIAGRAM (PARALLEL VERSION)



READ TIMING DIAGRAM (SERIAL VERSION)



WRITE TIMING DIAGRAM (SERIAL VERSION)



APPLICATIONS INFORMATION

GENERAL CONSIDERATIONS

Figures 1 and 2 show basic circuit diagrams for K-Series modem integrated circuits. K-Series products are designed to be used in conjunction with a control processor, a UART or RS-232 serial data interface, and a DAA phone line interface to function as a typical intelligent modem. The K-Series ICs interface directly with Intel 8048 and 80C51 microprocessors for control and status monitoring purposes.Two typical DAA arrangements are shown: one for a split ±5 or ±12 volt design and one for a single 5V design. These diagrams are for reference only and do not represent production-ready modem designs.

K-Series devices are available with two control interface versions: one for a parallel multiplexed address/data interface, and one for a serial interface. The parallel version is intended for use with 8039/48 or 8031/51 microcontrollers from Intel or many other manufacturers. The serial interface 22-pin version can be used with other microcontrollers or in applications where only a limited number of port lines are available or the application does not lend itself to a multiplexed address/data interface. The parallel versions may also be used in the serial mode, as explained in the data sheet pin description.

In most applications the controller will monitor the serial data for commands from the DTE and the received data for break signals from the far end modem. In this way, commands to the modem are sent over the same line as the transmitted data. In other applications the RS-232 interface handshake lines are used for modem control.

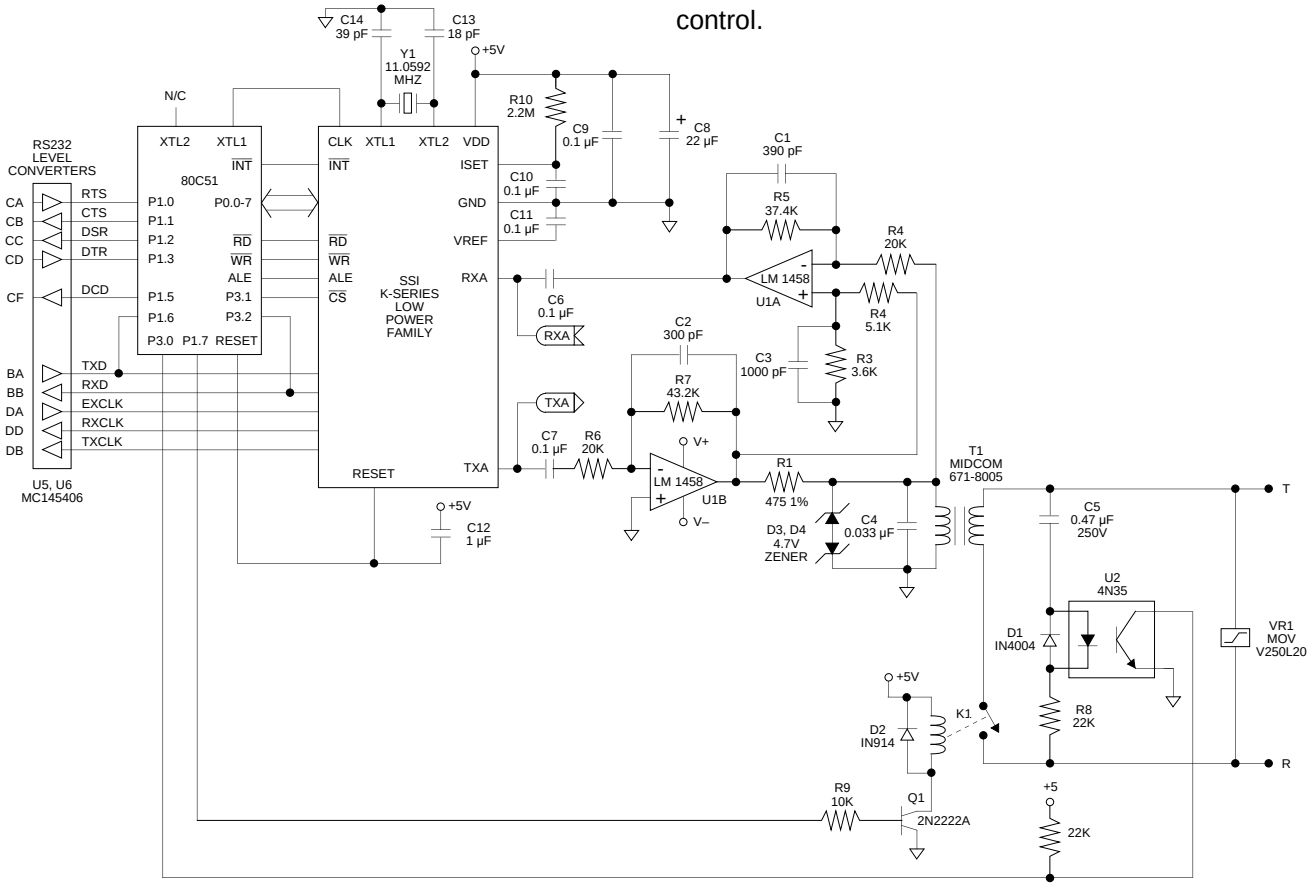


FIGURE 1: Basic Box Modem with Dual-Supply Hybrid

DIRECT ACCESS ARRANGEMENT (DAA)

The telephone line interfaces show two examples of how the "hybrid" may be implemented. The split supply design (Figure 1) is a typical two op-amp hybrid. The receive op-amp serves two purposes. It supplies gain to amplify the receive signal to the proper level for the modem's detectors and demodulator, and it removes the transmitted signal from the receive signal present at the transformer. This is done by supplying a portion of the transmitted signal to the non-inverting input of the receive op-amp at the same amplitude as the signal appearing at the transformer, making the transmit signal common mode.

The single-supply hybrid is more complex than the dual-supply version described above, but its use eliminates the need for a second power supply. This circuit (Figure 2) uses a bridged drive to allow undistorted signals to be sent with a single 5V supply. Because DTMF tones utilize a higher amplitude than data, these signals will clip if a single-ended drive approach is used. The bridged driver uses an extra op-amp (U1A) to invert the signal coming from the gain setting op-amp (U1B) before sending it to the other leg of the transformer. Each op-amp then supplies half the drive signal to the transformer. The receive amplifier (U1C) picks off its signal at the junction of the impedance matching resistor and the transformer. Because the bottom leg of the transformer is being driven in one direction by U1A and the resistor is driven in the opposite direction at the same time by U1B, the junction of the transformer and resistor remains relatively constant and the receive signal is unaffected.

DESIGN CONSIDERATIONS

Silicon Systems' 1-chip modem products include all basic modem functions. This makes these devices adaptable for use in a variety of applications, and as easy to control as conventional digital bus peripherals.

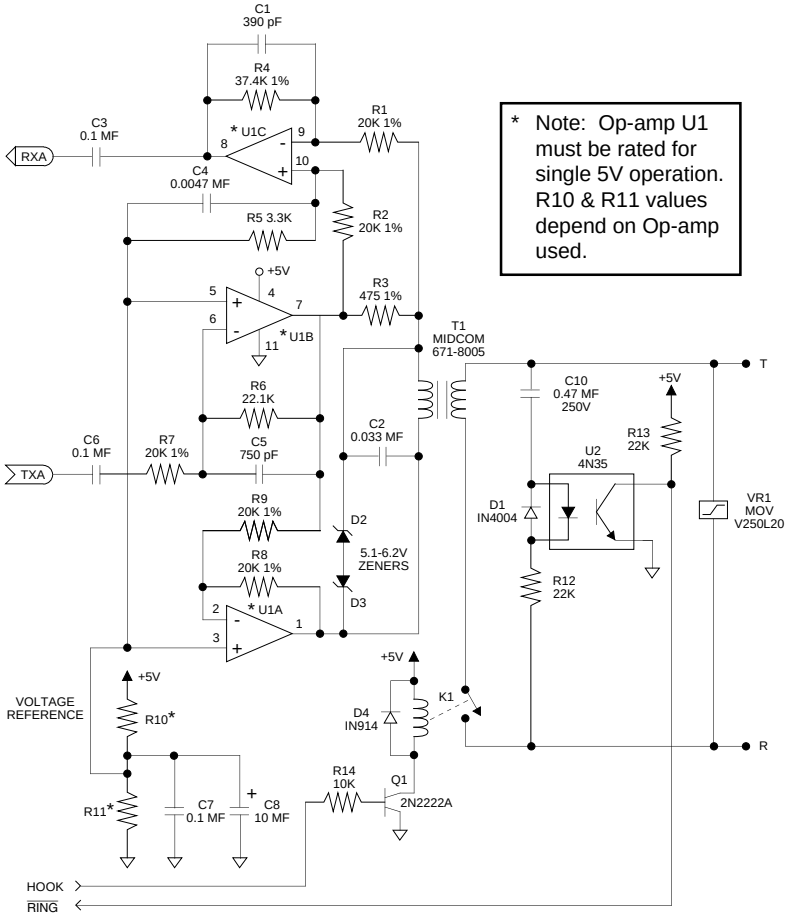


FIGURE 2: Single 5V Hybrid Version

Unlike digital logic circuitry, modem designs must properly contend with precise frequency tolerances and very low level analog signals, to ensure acceptable performance. Using good analog circuit design practices will generally result in a sound design. Following are additional recommendations which should be taken into consideration when starting new designs.

CRYSTAL OSCILLATOR

The K-Series crystal oscillator requires a parallel mode (antiresonant) crystal which operates at 11.0592 MHz. It is important that this frequency be maintained to within ±0.01% accuracy.

In order for a parallel mode crystal to operate correctly and to specification, it must have a load capacitor connected to the junction of each of the crystal and internal inverter connections, terminated to ground. The values of these capacitors depend primarily on the crystal's characteristics, and to a lesser degree on the internal inverter circuit. The values used affect the accuracy and start up characteristics of the oscillator.

LAYOUT CONSIDERATIONS

Good analog/digital design rules must be used to control system noise in order to obtain highest performance in modem designs. The more digital circuitry present on the PC board, the more this attention to noise control is needed. The modem should be treated as a high impedance analog device. A 22 µF electrolytic capacitor in parallel with a 0.1 µF ceramic capacitor between VDD and GND is recommended. Liberal use of ground planes and larger traces on power and ground are also highly favored. High speed digital circuits tend to generate a significant amount of EMI (Electro-Magnetic Interference) which must be minimized in order to meet regulatory agency limitations. To accomplish this, high speed digital devices should be locally bypassed, and the telephone line interface and K-Series device should be located close to each other near the area of the board where the phone line connection is accessed. To avoid problems, power supply and ground traces should be routed separately to the analog and digital functions on the board, and digital signals should not be routed near low level or high impedance analog traces. The analog and digital grounds should only connect at one point near the K-Series device ground pin to avoid ground loops. The K–Series modem IC's should have both high frequency and low frequency bypassing as close to the package as possible.

MODEM PERFORMANCE CHARACTERISTICS

The curves presented here define modem IC performance under a variety of line conditions while inducing disturbances that are typical of those encountered during data transmission on public service telephone lines. Test data was taken using an AEA Electronics' "Autotest I" modem test set and line simulator, operating under computer control. All tests were run full-duplex, using a Concord Data Systems 224 as the reference modem. A 511 pseudo-random-bit pattern was used for each data point. Noise was C-message weighted and all signal-to-noise (S/N) ratios reflect total power measurements similar to the CCITT V.56 measurement specification. The individual tests are defined as follows.

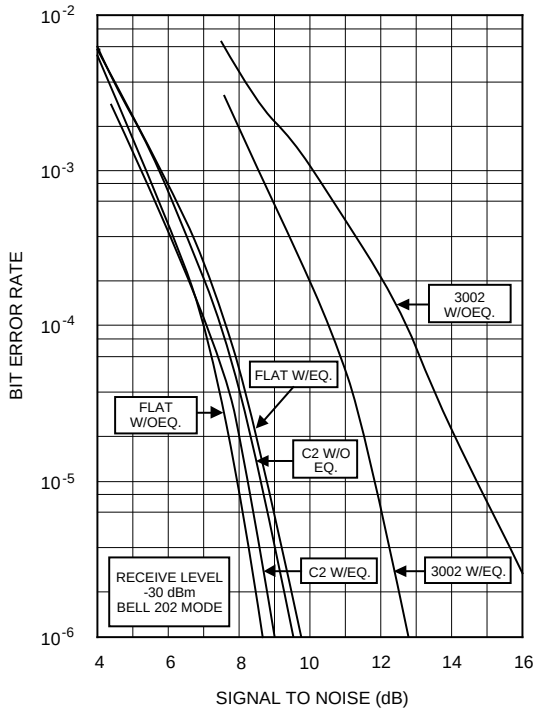
BER vs. S/N

This test measures the ability of the modem to operate over noisy lines with a minimum of data-transfer errors. Since some noise is generated in the best of dial-up lines, the modem must operate with the lowest S/N ratio possible. Better modem performance is indicated by test curves that are closest to the BER axis. A narrow spread between curves representing the four line parameters indicates minimal variation in performance while operating over a range of aberrant operating conditions. Typically, a DPSK modem will exhibit better BER-performance test curves receiving in the low band than in the high band.

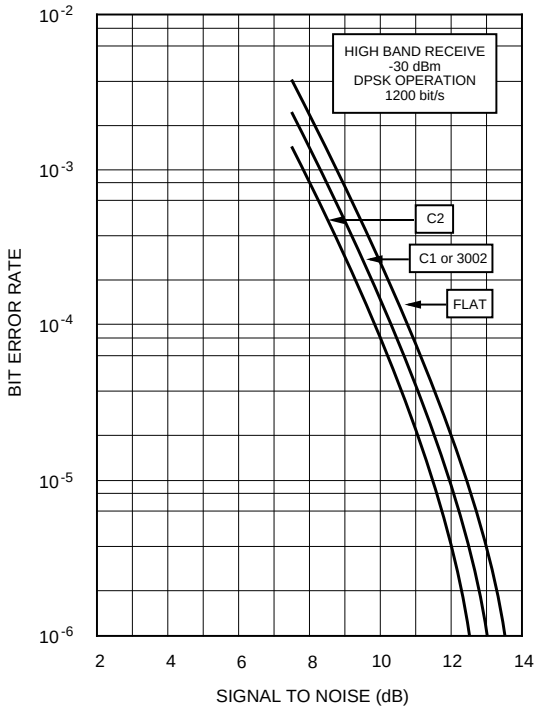
BER vs. Receive Level

This test measures the dynamic range of the modem. Because signal levels vary widely over dial-up lines, the widest possible dynamic range is desirable. The minimum Bell specification calls for 36 dB of dynamic range. S/N ratios are held constant at the indicated values while the receive level is lowered from a very high to very low signal levels. The width of the "bowl" of these curves, taken at the BER point, is the measure of dynamic range.

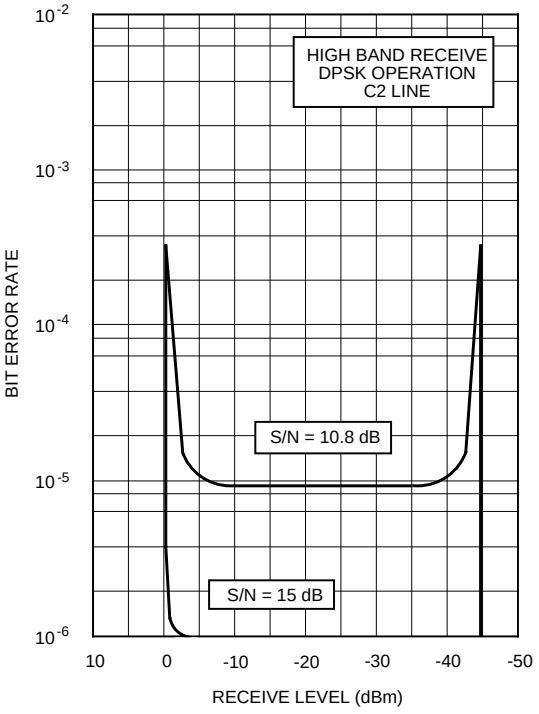
SSI 73K302L
BER vs S/N



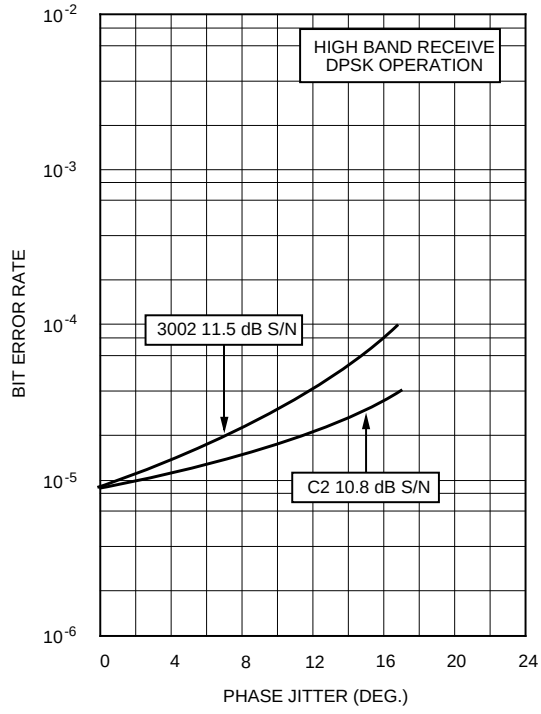
SSI 73K302L
BER vs S/N

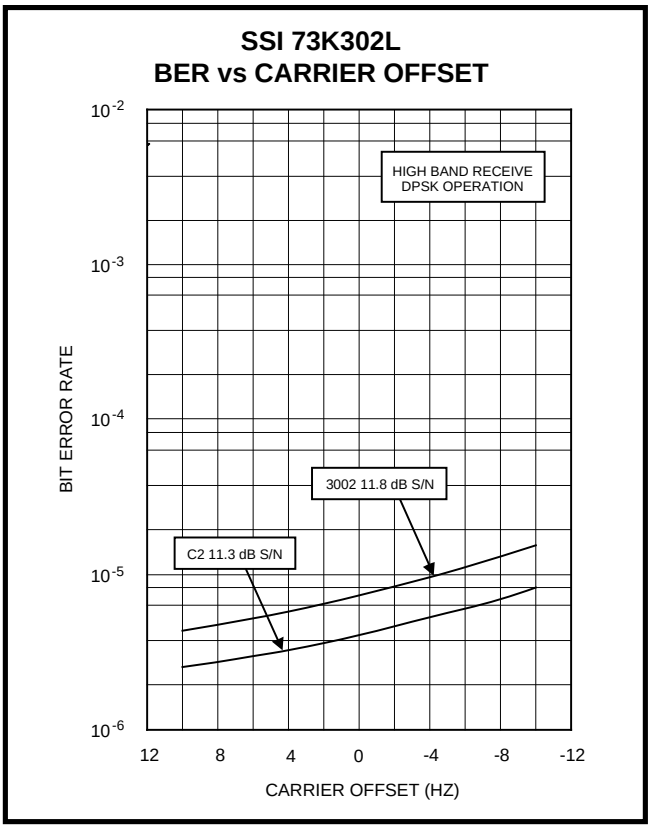


SSI 73K302L
BER vs RECEIVE LEVEL



SSI 73K302L
BER vs PHASE JITTER

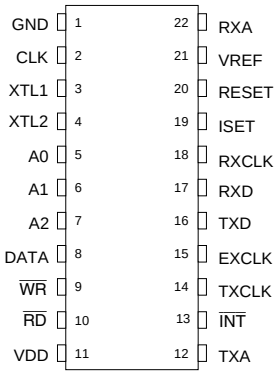



SSI 73K302L
BER vs CARRIER OFFSET
HIGH BAND RECEIVE
DPSK OPERATION
3002 11.8 dB S/N
C2 11.3 dB S/N
BIT ERROR RATE
10-2
10-3
10-4
10-5
10-6
12
8
4
0
-4
-8
-12
CARRIER OFFSET (HZ)

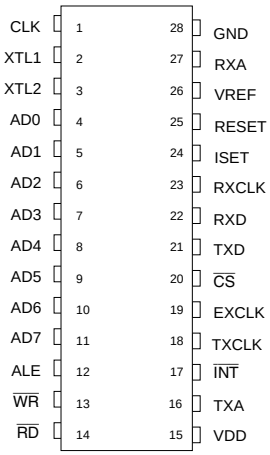
PACKAGE PIN DESIGNATIONS

(Top View)

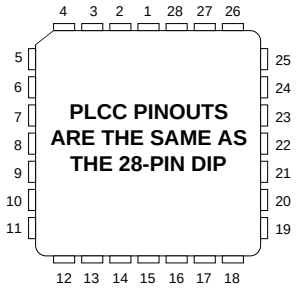
CAUTION: Use handling procedures necessary for a static sensitive component.



400-Mil 22-Pin DIP



600-Mil 28-Pin DIP



28-Pin PLCC

ORDERING INFORMATION

PART DESCRIPTION	ORDER NO.	PKG. MARK
SSI 73K302L		
28-Pin Plastic Dual In-Line	73K302L-IP	73K302L-IP
28-Lead Plastic Leaded Chip Carrier	73K302L-IH	73K302L-IH
SSI 73K302L with Serial Interface		
22-pin Plastic Dual In-Line	73K302SL-IP	73K302SL-IP

Preliminary Data: Indicates a product not completely released to production. The specifications are based on preliminary evaluations and are not guaranteed. Small quantities are available, and Silicon Systems should be consulted for current information.

Silicon Systems, Inc., 14351 Myford Road, Tustin, CA 92680-7022, (714) 573-6000, FAX: (714) 573-6914

SSI 73K321L
CCITT V.23, V.21
Single-Chip Modem

March 1996

DESCRIPTION

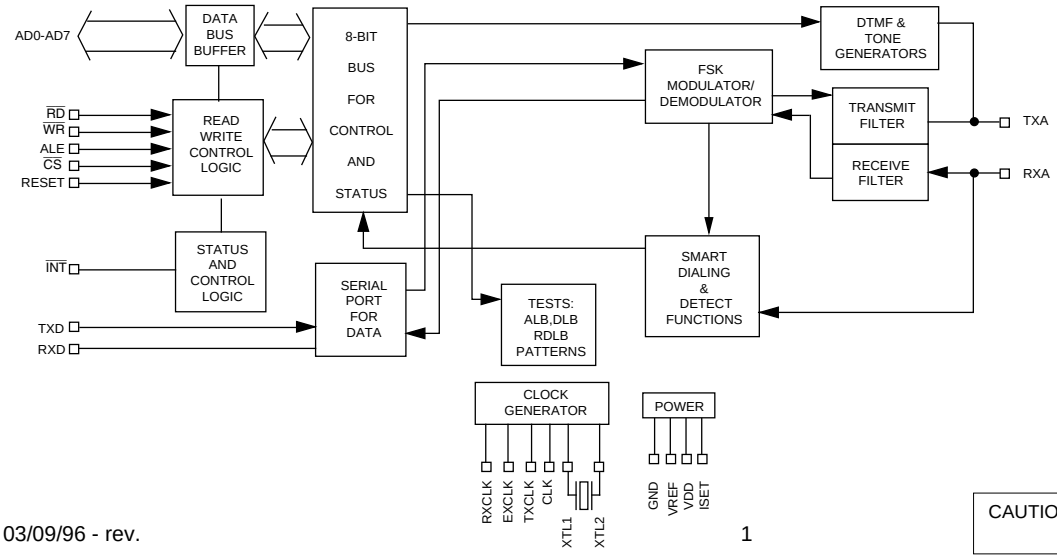
The SSI 73K321L is a highly integrated single-chip modem IC which provides the functions needed to construct a CCITT V.23 and V.21 compatible modem, capable of 0-300 bit/s full-duplex or 0-1200 bit/s half-duplex operation over dial-up telephone lines. The 73K321L provides 1200 bit/s operation in V.23 mode and 300 bit/s in V.21 mode. The SSI 73K321L also can both detect and generate the 2100 Hz answer tone needed for call initiation. The SSI 73K321L integrates analog, digital, and switched-capacitor array functions on a single substrate,offering excellent performance and a high level of functional integration in a single 28- or 22-pin DIP configuration. The SSI 73K321L operates from a single +5V supply with very low power consumption.

The SSI 73K321L includes the FSK modulator/ demodulator functions, call progress and handshake tone monitor test modes, and a tone generator capable of producing DTMF, answer, calling tones. The SSI 73K321L is designed to appear to the systems designer as a microprocessor peripheral, and will easily interface with popular one-chip microprocessors (80C51 typical) for control of modem functions through its 8-bit multiplexed address/data bus or via an optional serial control bus. An ALE control line simplifies address demultiplexing. Data communications occurs through a separate serial port only. (continued)

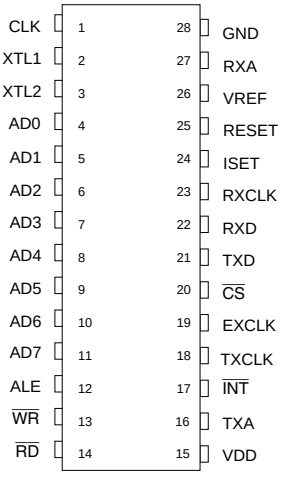
FEATURES

- **One-chip CCITT V.23 and V.21 standard compatible modem data pump**
- **Full-duplex operation at 0-300 bit/s (V.21) or 0-1200 bit/s (V.23) forward channel with or without 0–75 bits/s back channel**
- **Full Duplex 0-1200 bit/s (V.23) in 4-wire mode**
- **Pin and software compatible with other SSI K-Series 1-chip modems**
- **Interfaces directly with standard microprocessors (8048, 80C51 typical)**
- **Serial or parallel microprocessor bus for control**
- **Serial port for data transfer**
- **Call progress, carrier, precise answer tone (2100 Hz), calling tone (1300 Hz) and FSK mark detectors**
- **DTMF generator**
- **Test modes available: ALB, DL, RDL, Mark, Space, Alternating bit patterns**
- **Precise automatic gain control allows 45 dB dynamic range**
- **Space efficient 28-pin PLCC package available**
- **CMOS technology for low power consumption using 30 mW @ 5V from a single power supply**

BLOCK DIAGRAM



PIN DIAGRAM



CAUTION: Use handling procedures necessary for a static sensitive component.

DESCRIPTION (continued)

The SSI 73K321L is ideal for either free standing or integral system modem applications where multi-standard data communications over the 2-wire switched telephone network is desired. Typical uses include videotex terminals, low-cost integral modems and built-in diagnostics for office automation or industrial control systems. The 73K321L's high functionality, low power consumption and efficient packaging simplify design requirements and increase system reliability in these applications. A complete modem requires only the addition of the phone line interface, a control microprocessor, and RS-232 level converter for a typical system. The SSI 73K321L is part of Silicon Systems K-Series family of pin and function compatible single-chip modem products. These devices allow systems to be configured for higher speeds and Bell or CCITT operation with only a single component change.

OPERATION

FSK MODULATOR/DEMODULATOR

The FSK modulator produces a frequency modulated analog output signal using two discrete frequencies to represent the binary data. V.21 mode uses 980 and 1180 Hz (originate, mark and space) or 1650 and 1850 Hz (answer, mark and space). V.23 mode uses 1300 and 2100 Hz for the main channel and 390 and 450 Hz for the back channel. The modulation rate of the back channel is up to 75 baud. Demodulation involves detecting the received frequencies and decoding them into the appropriate binary value.

PASSBAND FILTERS AND EQUALIZERS

High and low band filters are included to shape the amplitude and phase response of the transmit and receive signals and provide compromise delay equalization and rejection of out-of-band signals in the receive channel. Amplitude and phase equalization are necessary to compensate for distortion of the transmission line and to reduce intersymbol interference in the bandlimited receive signal.

AGC

The automatic gain control maintains a signal level at the input to the demodulators which is constant to within 1 dB. It corrects quickly for increases in signal which would cause clipping and provides a total receiver dynamic range of >45 dB.

PARALLEL BUS INTERFACE

Four 8-bit registers are provided for control, option select and status monitoring. These registers are addressed with the AD0, AD1, and AD2 multiplexed address lines (latched by ALE) and appear to a control microprocessor as four consecutive memory locations. Two control registers and the tone register are read/write memory. The detect register is read only and cannot be modified except by modem response to monitored parameters. The parallel bus interface is not available with the 22-pin package.

SERIAL COMMAND INTERFACE

The Serial Command mode allows access to the SSI 73K321L control and status registers via a serial command port. In this mode the A0, A1 and A2 lines provide register addresses for data passed through the data pin under control of the $\overline{RD}$ and $\overline{WR}$ lines. A read operation is initiated when the $\overline{RD}$ line is taken low. The first bit is available after RD is brought low and the next seven cycles of EXCLK will then transfer out seven bits of the selected address location LSB first. A write takes place by shifting in eight bits of data LSB first for eight consecutive cycles of EXCLK. $\overline{WR}$ is then pulsed low and data transferred into the selected register occurs on the rising edge of $\overline{WR}$.

SPECIAL DETECT CIRCUITRY

The special detect circuitry monitors the received analog signal to determine status or presence of carrier, answer tone and weak received signal (long loop condition). Special tones such as FSK marking and the 1300 Hz calling tone are also detected. A highly frequency selective call progress detector provides adequate discrimination to accurately detect European call progress signals.

DTMF GENERATOR

The DTMF generator will output one of 16 standard tone-pairs determined by a 4-bit binary value and TX DTMF mode bit previously loaded into the tone register. Dialing is initiated when the DTMF mode is selected using the tone register and the transmit enable (CR0 bit D1) is changed from 0 to 1.

PIN DESCRIPTION

POWER

NAME	28-PIN	22-PIN	TYPE	DESCRIPTION
GND	28	1	I	System Ground.
VDD	15	11	I	Power supply input, 5V ±10%. Bypass with 0.1 and 22 µF capacitors to GND.
VREF	26	21	O	An internally generated reference voltage. Bypass with 0.1 µF capacitor to GND.
ISET	24	19	I	Chip current reference. Sets bias current for op-amps. The chip current is set by connecting this pin to VDD through a 2 MΩ resistor. ISET should be bypassed to GND with a 0.1 µF capacitor.

PARALLEL MICROPROCESSOR INTERFACE

ALE	12	-	I	Address latch enable. The falling edge of ALE latches the address on AD0-AD2 and the chip select on $\overline{CS}$.
AD0-AD7	4-11	-	I/O	Address/data bus. These bidirectional tri-state multiplexed lines carry information to and from the internal registers.
$\overline{CS}$	20	-	I	Chip select. A low during the falling edge of ALE on this pin allows a read cycle or a write cycle to occur. AD0-AD7 will not be driven and no registers will be written if $\overline{CS}$ (latched) is not active. The state of $\overline{CS}$ is latched on the falling edge of ALE.
CLK	1	2	O	Output clock. This pin is the output of the crystal oscillator frequency only in the SSI 73K321.
$\overline{INT}$	17	13	O	Interrupt. This open drain output signal is used to inform the processor that a detect flag has occurred. The processor must then read the detect register to determine which detect triggered the interrupt. $\overline{INT}$ will stay low until the processor reads the detect register or does a full reset.
$\overline{RD}$	14	-	I	Read. A low requests a read of the SSI 73K321L internal registers. Data cannot be output unless both $\overline{RD}$ and the latched $\overline{CS}$ are active or low.
RESET	25	20	I	Reset. An active high signal high on this pin will put the chip into an inactive state. All control register bits (CR0, CR1, Tone) will be reset. The output of the CLK pin will be set to the crystal frequency. An internal pull down resistor permits power on reset using a capacitor to VDD.

PARALLEL MICROPROCESSOR INTERFACE (continued)

NAME	28-PIN	22-PIN	TYPE	DESCRIPTION
$\overline{WR}$	13	-	I	Write. A low on this informs the SSI 73K321L that data is available on AD0-AD7 for writing into an internal register. Data is latched on the rising edge of $\overline{WR}$. No data is written unless both $\overline{WR}$ and the latched $\overline{CS}$ are low.

SERIAL MICROPROCESSOR INTERFACE

A0-A2	-	5-7	I	Register Address Selection. These lines carry register addresses and should be valid during any read or write operation.
DATA	-	8	I/O	Serial Control Data. Data for a read/write operation is clocked in or out on the falling edge of the EXCLK pin. The direction of data flow is controlled by the $\overline{RD}$ pin. $\overline{RD}$ low outputs data. $\overline{RD}$ high inputs data.
$\overline{RD}$	-	10	I	Read. A low on this input informs the SSI 73K321L that data or status information is being read by the processor. The falling edge of the $\overline{RD}$ signal will initiate a read from the addressed register. The $\overline{RD}$ signal must continue for eight falling edges of EXCLK in order to read all eight bits of the referenced register. Read data is provided LSB first. Data will not be output unless the $\overline{RD}$ signal is active.
$\overline{WR}$	-	9	I	Write. A low on this input informs the SSI 73K321L that data or status information has been shifted in through the DATA pin and is available for writing to an internal register. The normal procedure for a write is to shift in data LSB first on the DATA pin for eight consecutive falling edges of EXCLK and then to pulse $\overline{WR}$ low. Data is written on the rising edge of $\overline{WR}$.
Note:	In the serial, 22-pin version, the pins AD0-AD7, ALE and $\overline{CS}$ are removed and replaced with the pins; A0, A1, A2, DATA, and an unconnected pin. Also, the $\overline{RD}$ and $\overline{WR}$ controls are used differently. The Serial Control mode is provided in the 28-pin version by tying ALE high and $\overline{CS}$ low. In this configuration AD7 becomes DATA and AD0, AD1 and AD2 become A0, A1 and A2, respectively.			

DTE USER INTERFACE

NAME	28-PIN	22-PIN	TYPE	DESCRIPTION
EXCLK	19	15	I	External Clock. Used for serial control interface to clock control data in or out of the 73K321L.
RXCLK	23	18	O	Receive Clock. A clock which is 16 x1200, or 16 x 75 in V.23 mode, or 16 x 300 baud data rate is output in V.21.
RXD	22	17	O/ Weak Pull-up	Received Digital Data Output. Serial receive data is available on this pin. The data is always valid on the rising edge of RXCLK when in Synchronous mode. RXD will output constant marks if no carrier is detected.
TXCLK	18	14	O	Transmit Clock. TXCLK is always active. In V.23 mode the output is either a 16 x 1200 baud clock or 16 x 75 baud, in V.21 mode the clock is 16 x 300 baud.
TXD	21	16	I	Transmit Digital Data Input. Serial data for transmission is input on this pin. In Asynchronous modes (1200 or 300 baud) no clocking is necessary.

ANALOG INTERFACE AND OSCILLATOR

RXA	27	22	I	Received modulated analog signal input from the phone line.
TXA	16	12	O	Transmit analog output to the phone line.
XTL1 XTL2	2 3	3 4	I I	These pins are for the internal crystal oscillator requiring a 11.0592 MHz Parallel mode crystal and two load capacitors to Ground. XTL2 can also be driven from an external clock.

REGISTER DESCRIPTIONS

Four 8-bit internal registers are accessible for control and status monitoring. The registers are accessed in read or write operations by addressing the A0 and A1 address lines in Serial mode, or the AD0 and AD1 lines in Parallel mode. The AD0 and AD1 lines are latched by ALE. Register CR0 controls the method by which data is transferred over the phone line. CR1 controls the interface between the microprocessor and the SSI 73K321L internal state. DR is a detect register which provides an indication of Monitored modem status conditions. TR, the tone control register, controls the DTMF generator, answer and guard tones and RXD output gate used in the modem initial connect sequence. All registers are read/write except for DR which is read only. Register control and status bits are identified below:

REGISTER BIT SUMMARY

	ADDRESS	DATA BIT NUMBER							
REGISTER	AD2 - AD0	D7	D6	D5	D4	D3	D2	D1	D0
CONTROL REGISTER 0 CR0	000	TRANSMIT MODE 4	0	TRANSMIT MODE 3	TRANSMIT MODE 2	TRANSMIT MODE 1	TRANSMIT MODE 0	TRANSMIT ENABLE	ANSWER/ ORIGINATE
CONTROL REGISTER 1 CR1	001	TRANSMIT PATTERN 1	TRANSMIT PATTERN 0	ENABLE DETECT INTERRUPT	ADD PH. EQ. (V.23)	CLK CONTROL	RESET	TEST MODE 1	TEST MODE 0
DETECT REGISTER DR	010	X	X	RECEIVE DATA	X	CARRIER DETECT	SPECIAL TONE	CALL PROGRESS	LONG LOOP
TONE CONTROL REGISTER TR	011	RXD OUTPUT CONTROL	TRANSMIT CALLING TONE	TRANSMIT ANSWER TONE	TRANSMIT DTMF	DTMF3	DTMF2/ V.23 FDX	DTMF1	DTMF0/ ANSWER/SPEC. TONE SELECT
ID REGISTER ID	110	ID	ID	ID	ID	X	X	X	X

NOTE: When a register containing reserved control bits is written into, the reserved bits must be programmed as 0's.

X = Undefined, mask in software

REGISTER ADDRESS TABLE

REGISTER	ADDRESS	DATA BIT NUMBER							
	AD2 - AD0	D7	D6	D5	D4	D3	D2	D1	D0
CONTROL REGISTER 0 CR0	000	TRANSMIT MODE 4	0	TRANSMIT MODE 3	TRANSMIT MODE 2	0	TRANSMIT MODE 0	TRANSMIT ENABLE	ORIGINATE/ ANSWER
		0=V.23 FSK 1=V.21 FSK		0000=PWR DOWN 1100=FSK 0001=TRANSMIT DTMF, CALL PROGRESS DETECTION				0=DISABLE TXA OUTPUT 1=ENABLE TXA OUTPUT	IN V.21 MODE: 0=ANSWER 1=ORIGINATE IN V.23 MODE : 0=RECEIVE @ 1200 BIT/S, TRANSMIT @ 75 BIT/S 1=RECEIVE @ 75 BIT/S, TRANSMIT @ 1200 BIT/S
CONTROL REGISTER 1 CR1	001	TRANSMIT PATTERN 1	TRANSMIT PATTERN 0	ENABLE DETECT INTERRUPT	ADD PH. EQ.	CLK CONTROL	RESET	TEST MODE 1	TEST MODE 0
		00=TX DATA 01=TX ALTERNATE 10=TX MARK 11=TX SPACE		0=DISABLED 1=ENABLED	0=NORMAL EQ. 1=ADD EXTRA PHASE EQ. IN V.23	0=XTAL 1= NOT SUPPORTED IN THIS DEVICE	0=NORMAL 1=RESET	00=NORMAL 01=ANALOG LOOPBACK 10=REMOTE DIGITAL LOOPBACK 11=LOCAL DIGITAL LOOPBACK	
DETECT REGISTER DR	010	X	X	RECEIVE DATA	X	CARRIER DETECT	SPECIAL TONE	CALL PROGRESS	LONG LOOP
				OUTPUTS RECEIVED DATA STREAM		0=CONDITION NOT DETECTED 1=CONDITION DETECTED			
TONE CONTROL REGISTER TR	011	RXD OUTPUT CONTROL	TRANSMIT CALLING TONE	TRANSMIT ANSWER TONE	TRANSMIT DTMF	DTMF3	DTMF2/ V.23 FDX	DTMF1	DTMF0/ SPECIAL TONE
		RXD PIN 0=NORMAL 1=TRI STATE	0=OFF 1=ON	0=OFF 1=ON	0=DATA 1=TX DTMF	4 BIT CODE FOR 1 OF 16 DUAL TONE COMB-INATIONS. OVERIDES OTHER TRANSMIT MODES 0=HALF DUPLEX V.23 1=ALLOWS V.23 FULL DUPLEX OPERATION			0=ANSWER TONE FREQ.=2225 Hz FSK MARK WILL BE INDICATED BY SPECIAL TONE BIT IN DR 1=ANSWER TONE FREQ.=2100 Hz EITHER 2100 Hz (IN ORIG.) OR 1300 Hz (IN ANS.) WILL BE INDICATED BY SPECIAL TONE BIT IN DR
ID REGISTER 10	110	ID	ID	ID	ID	X	X	X	X

00XX=73K212L, 322L, 321L
01XX=73K221L, 302L
10XX=73K222L
1100=73K224L
1110=73K324L

X = Undefined, mask in software
0 = Only write zero to these locations

CONTROL REGISTER 0

	D7	D6	D5	D4	D3	D2	D1	D0
CR0 000	TRANSMIT MODE 4	0	TRANSMIT MODE 3	TRANSMIT MODE 2	0	TX DTMF	TRANSMIT ENABLE	ANSWER/ ORIGINATE

BIT NO.	NAME	CONDITION	DESCRIPTION
D0	Answer/ Originate	0	Selects Answer mode in V.21 (transmit in high band, receive in low band) or in V.23 mode, receive at 1200 bit/s and transmit at 75 bit/s.
		1	Selects Originate mode in V.21 (transmit in low band, receive in high band) or in V.23 mode, receive at 75 bit/s and transmit at 1200 bit/s. If in V.23 and D2 of TR=1, selects V.23 full duplex operation in 4-wire configuration.
			Note: This bit works with TR bit D0 to program special tones detected in Tone Register. See detect and tone registers.
D1	Transmit Enable	0	Disables transmit output at TXA.
		1	Enables transmit output at TXA.
			Note: Answer tone and DTMF TX control require TX enable.
D7, D5, D4, D2	Transmit Mode	D7 D5 D4 D2	
		0 0 0 0	Power Down
		0 0 0 1	Transmit DTMF
		0 1 1 0	V.23 Mode
		1 1 1 0	V.21 Mode
D6, D3	Unused	N/A	Not used; must be written as “0”

CONTROL REGISTER 1

	D7	D6	D5	D4	D3	D2	D1	D0
CR1 001	TRANSMIT PATTERN 1	TRANSMIT PATTERN 0	ENABLE DETECT INTER.	ADD PH. EQ.	CLK CONTROL (WRITE 0)	RESET	TEST MODE 1	TEST MODE 0

BIT NO.	NAME	CONDITION	DESCRIPTION
D1, D0	Test Mode	D1 D0	
		0 0	Selects Normal Operating mode.
		0 1	Analog Loopback mode. Loops the transmitted analog signal back to the receiver, and causes the receiver to use the same center frequency as the transmitter. To squelch the TXA pin, transmit enable must be forced low.
		1 0	Not used.
		1 1	Selects local digital loopback. Internally loops TXD back to RXD and continues to transmit data from TXA pin.
D2	Reset	0	Selects normal operation.
		1	Resets modem to power down state. All control register bits (CR0, CR1, Tone) are reset to zero. The output of the clock pin will be set to the crystal frequency.
D3	CLK Control (Clock Control)	Program as 0	Not supported in the SSI 73K321.See the TXCLK and RXCLK pin descriptions for 16x the data rate clocks.
D4	Add Ph. Eq.	0	Selects normal equalization.
		1	In V.23 mode, additional phase equalization is added to the main channel filters when D4 is set to 1.
D5	Enable Detect Interrupt	0	Disables interrupt at $\overline{INT}$ pin. All interrupts are normally disabled in Power Down modes.
		1	Enables $\overline{INT}$ output. An interrupt will be generated with a change in status of DR bits D1-D3. The special tone and call progress detect interrupts are masked when the TX enable bit is set. Carrier detect is masked when TX DTMF is activated. All interrupts will be disabled if the device is in Power Down mode.
D7, D6	Transmit Pattern	D7 D6	
		0 0	Selects normal data transmission as controlled by the state of the TXD pin.
		0 1	Selects an alternating mark/space transmit pattern for modem testing.
		1 0	Selects a constant mark transmit pattern.
		1 1	Selects a constant space transmit pattern.

DETECT REGISTER

	D7	D6	D5	D4	D3	D2	D1	D0
DR 010	X	X	RECEIVE DATA	X	CARR. DETECT	SPECIAL TONE	CALL PROG.	LONG LOOP

BIT NO.	NAME	CONDITION	DESCRIPTION
D0	Long Loop	0	Indicates normal received signal.
		1	Indicates low received signal level.
D1	Call Progress Detect	0	No call progress tone detected.
		1	Indicates presence of call progress tones. The call progress detection circuitry is activated by energy in the normal 350 to 620 Hz call progress band when CR0 D2 =1.
D2	Special Tone Detect	0	No special tone detected as programmed by CR0 bit D0 and Tone Register bit D0.
		1	Special tone detected. The detected tone is:
			(1) 2100 Hz answer tone if D0 of TR=1 and the device is in V.21 Originate mode.
			(2) 1300 Hz calling tone if D0 of TR=1 and the device is in V.21 or V.23 Answer mode.
			(3) an FSK mark for the mode the device is set to receive in if D0 of TR = 0.
			NOTE: Tolerance on special tones is ±3%.
D3	Carrier Detect	0	No carrier detected in the receive channel.
		1	Indicated carrier has been detected in the received channel.
D4	Unused	Undefined	Not used in the 73K321L. Mask in software.
D5	Receive Data		Continuously outputs the received data stream. This data is the same as that output on the RXD pin, but it is not disabled when RXD is tri-stated.
D6, D7	Not Used	Undefined	Mask in software.

TONE REGISTER

	D7	D6	D5	D4	D3	D2	D1	D0
TR 011	RXD OUTPUT CONTR.	TRANSMIT CALLING TONE	TRANSMIT ANSWER TONE	TRANSMIT DTMF	DTMF 3	DTMF 2/ V.23 4W/FDX	DTMF 1	DTMF 0/ ANS. TONE/ SPECIAL TONE/ SEL

BIT NO.	NAME	CONDITION	DESCRIPTION
D0	DTMF 0/ Answer Tone/ Special Tone/ Detect/Select	D6 D5 D4 D0	D0 interacts with bits D6, D5, D4, and CR0 as shown.
		X X 1 X	Transmit DTMF tones.
		X X 0 0	Mark of an FSK mode selected in CR0 is to be detected in D2 of DR.
		X X 0 1	2100 Hz answer tone will be detected in D2 of DR if V.21 Originate mode is selected in CR0.
			1300 Hz calling tone will be detected in D2 of DR if V.21 or V.23 Answer mode is selected in CR0.
		X 1 0 0	Transmit 2225 Hz answer tone in Answer mode.
		X 1 0 1	Transmit 2100 Hz answer tone in Answer mode.
D2	DTMF2/ V.23 4W/FDX	CR0 D7 D5 D4 D2 / TR D2	
		0 1 1 0 / 0	2-wire half duplex
		0 1 1 0 / 1	4-wire full duplex
D3, D2, D1, D0	DTMF 3, 2, 1, 0	D3 D2 D1 D0: 0 0 0 0 - 1 1 1 1	Programs 1 of 16 DTMF tone pairs that will be transmitted when TX DTMF (TR bit D4) and TX enable bit (CR0, bit D2) are set. Tone encoding is shown below:

KEYBOARD EQUIVALENT	DTMF CODE D3 D2 D1 D0	TONES LOW	TONES HIGH
1	0 0 0 1	697	1209
2	0 0 1 0	697	1336
3	0 0 1 1	697	1477
4	0 1 0 0	770	1209
5	0 1 0 1	770	1336
6	0 1 1 0	770	1477
7	0 1 1 1	852	1209
8	1 0 0 0	852	1336
9	1 0 0 1	852	1477
0	1 0 1 0	941	1336

TONE REGISTER (continued)

BIT NO.	NAME	CONDITION	DESCRIPTION
D3, D2, D1, D0 (cont.)			KEYBOARD EQUIVALENT / DTMF CODE D3 D2 D1 D0 / TONES LOW HIGH
			* 1 0 1 1 941 1209
			# 1 1 0 0 941 1477
			A 1 1 0 1 697 1633
			B 1 1 1 0 770 1633
			C 1 1 1 1 852 1633
			D 0 0 0 0 941 1633
D4	Transmit DTMF	0	Disabled DTMF.
		1	Activates DTMF. The selected DTMF tones are transmitted continuously when this bit is high. TX DTMF overrides all other transmit functions.
D5	Transmit Answer Tone	0	Disables answer tone generator.
		1	Enables answer tone generator. A 2100 Hz answer tone will be transmitted continuously when the transmit enable bit is set. The device must be in Answer mode.
D6	Transmit Calling Tone	0	Disables calling tone generator.
		1	Transmit calling tone in either mode.
D7	RXD Output Control	0	Enables RXD pin. Receive data will be output on RXD.
		1	Disables RXD pin. The RXD pin reverts to a high impedance with internal weak pull-up resistor.

ID REGISTER

	D7	D6	D5	D4	D3	D2	D1	D0
ID 110	ID	ID	ID	ID	X	X	X	X

BIT NO.	NAME	CONDITION	DESCRIPTION
D7, D6, D5 D4	Device Identification Signature	D7 D6 D5 D4	Indicates Device:
		0 0 X X	SSI 73K212L, 73K321L or 73K322L
		0 1 X X	SSI 73K221L or 73K302L
		1 0 X X	SSI 73K222L
		1 1 0 0	SSI 73K224L
		1 1 1 0	SSI 73K324L
D3-D0	Not Used	Undefined	Mask in software.

ELECTRICAL SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING
VDD Supply Voltage	14V
Storage Temperature	-65 to 150°C
Soldering Temperature (10 sec.)	260°C
Applied Voltage	-0.3 to VDD + 0.3V
Note: All inputs and outputs are protected from static charge using built-in, industry standard protection devices and all outputs are short-circuit protected.	

RECOMMENDED OPERATING CONDITIONS

PARAMETER	CONDITION	MIN	NOM	MAX	UNIT
VDD Supply voltage		4.5	5	5.5	V
TA, Operating Free-Air Temperature		-40		+85	°C
Clock Variation	(11.0592 MHz) Crystal or external clock	-0.01		+0.01	%
External Components (Refer to Application section for placement.)					
VREF Bypass Capacitor	(External to GND)	0.1			µF
Bias setting resistor	(Placed between VDD and ISET pins)	1.8	2	2.2	MΩ
ISET Bypass Capacitor	(ISET pin to GND)	0.1			µF
VDD Bypass Capacitor 1	(External to GND)	0.1			µF
VDD Bypass Capacitor 2	(External to GND)	22			µF
XTL1 Load Capacitor	Depends on crystal characteristics;			40	pF
XTL2 Load Capacitor	from pin to GND			20	

DC ELECTRICAL CHARACTERISTICS
(TA = -40°C to 85°C, VDD = recommended range unless otherwise noted.)

PARAMETER	CONDITION	MIN	NOM	MAX	UNIT
IDD, Supply Current	ISET Resistor = 2 MΩ				
IDDA, Active	CLK = 11.0592 MHz		8	12	mA
IDD1, Power-down	CLK = 11.0592 MHz			4	mA
IDD2, Power-down	CLK = 19.200 kHz			3	mA
Digital Inputs					
VIH, Input High Voltage					
Reset, XTL1, XTL2		3.0		VDD	V
All other inputs		2.0		VDD	V
VIL, Input Low Voltage		0		0.8	V
IIH, Input High Current	VI = VIH Max			100	µA
IIL, Input Low Current	VI = VIL Min	-200			µA
Reset Pull-down Current	Reset = VDD	1		50	µA
Input Capacitance	All Digital Input Pins			10	pF
Digital Outputs					
VOH, Output High Voltage	IOH MIN = -0.4 mA	2.4		VDD	V
VOL, Output Low Voltage	IO MAX = 1.6 mA			0.4	V
VOL, CLK Output	IO = 3.6 mA			0.6	V
RXD Tri-State Pull-up Curr.	RXD = GND	-1		-50	µA
CMAX, CLK Output	Maximum Capacitive Load			15	pF

DYNAMIC CHARACTERISTICS AND TIMING
(TA = -40°C to +85°C, VDD = Recommended range unless otherwise noted.)

PARAMETER	CONDITION	MIN	NOM	MAX	UNIT
FSK Modulator					
Output Freq. Error	CLK = 11.0592 MHz	-0.35		+0.35	%
Transmit Level	Transmit Dotting Pattern	-11	-10	-9	dBm0
Harmonic Distortion in 700-2900 Hz band	THD in the alternate band FSK		-60	-50	dB
Output Bias Distortion	Transmit Dotting Pattern in ALB @ RXD		±3		%
Total Output Jitter	Random Input in ALB @ RXD	-10		+10	%
NOTE: Parameters expressed in dBm0 refer to the following definition: 0 dB loss in the Transmit path to the line. 2 dB gain in the Receive path from the line. Refer to the Basic Box Modem diagram in the Applications section for the DAA design.					
DTMF Generator					
Freq. Accuracy		-0.25		+0.25	%
Output Amplitude	Low Band, CR0 bit D2=1	-10	-9	-8	dBm0
Output Amplitude	High Band, CR0 bit D2=1	-8	-7	-6	dBm0
Twist	High-Band to Low-Band, as above	1.0	2.0	3.0	dB
Long Loop Detect	Not valid for V.23 back channel	-38		-28	dBm0
Dynamic Range	Refer to Performance Curves		43		dB
Call Progress Detector					
Detect Level	-3 dB points in 285 and 675 Hz	-38			dBm0
Reject Level	Test signal is a 460 Hz sinusoid			-45	dBm0
Delay Time	-70 dBm0 to -30 dBm0 STEP			40	ms
Hold Time	-30 dBm0 to -70 dBm0 STEP			40	ms
Hysteresis		2			dB
Carrier Detect					
Threshold	Single Tone	-48		-43	dBm0
Delay Time					
V.21		10		20	ms
V.23 Forward Channel		6		12	ms
V.23 Back Channel		25		40	ms
Hold Time					
V.21		6		20	ms
V.23 Forward Channel		3		8	ms
V.23 Back Channel		10		25	ms
Hysteresis		2			dB

DYNAMIC CHARACTERISTICS AND TIMING (continued)

PARAMETER	CONDITION	MIN	NOM	MAX	UNIT
Special Tone Detectors					
Detect Level	See definitions for TR bit D0 mode	-48		-43	dBm0
Delay Time	-70 dBm0 to -30 dBm0 Step				
2100 Hz answer tone		10		25	ms
1300 Hz calling tone		10		25	ms
390 Hz V.23 back channel mark		20		65	ms
980 or 1650 Hz V.21 marks		10		25	ms
Hold Time	-30 dBm0 to -70 dBm0 Step				
2100 Hz answer tone		4		15	ms
1300 Hz calling tone		3		10	ms
390 Hz V.23 back channel mark		10		25	ms
980 or 1650 Hz V.21 marks		5		15	ms
Hysteresis		2			dB
Detect Freq. Range	Any Special Tone	-3		+3	%
Output Smoothing Filter					
Output load	TXA pin; FSK Single Tone out for THD = -50 dB in 0.3 to 3.4 kHz	10		 50	kΩ pF
Out of Band Energy	Frequency >12 kHz in all modes			-60	dBm0
Output Impedance	TXA pin, TXA Enabled		20	50	Ω
Clock Noise	TXA pin; 76.8 kHz or 122.88 kHz in V.23 main channel		0.1	0.4	mVrms

DYNAMIC CHARACTERISTICS AND TIMING (continued)

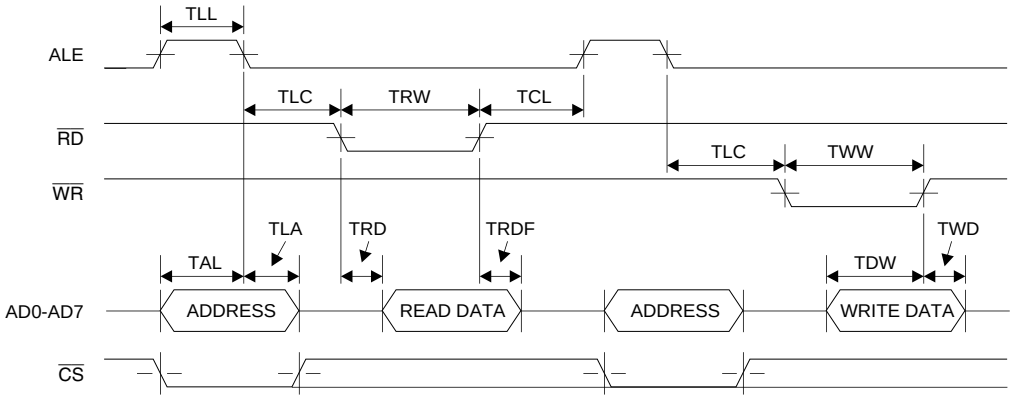
PARAMETER	CONDITION	MIN	NOM	MAX	UNIT
Timing (Refer to Timing Diagrams)					
TAL	$\overline{CS}$/Addr. setup before ALE Low	25			ns
TLA	$\overline{CS}$/Addr. hold after ALE Low	20			ns
TLC	ALE Low to $\overline{RD}$/$\overline{WR}$ Low	30			ns
TCL	$\overline{RD}$/$\overline{WR}$ Control to ALE High	-5			ns
TRD	Data out from $\overline{RD}$ Low	0		140	ns
TLL	ALE width	30			ns
TRDF	Data float after $\overline{RD}$ High	0		5	ns
TRW	$\overline{RD}$ width	200		25000	ns
TWW	$\overline{WR}$ width	140		25000	ns
TDW	Data setup before $\overline{WR}$ High	40			ns
TWD	Data hold after $\overline{WR}$ High	10			ns
TCKD	Data out after EXCLK Low			200	ns
TCKW	$\overline{WR}$ after EXCLK Low	150			ns
TDCK	Data setup before EXCLK Low	150			ns
TAC	Address setup before control*	50			ns
TCA	Address hold after control*	50			ns
TWH	Data Hold after EXCLK	20			

* Control for setup is the falling edge of $\overline{RD}$ or $\overline{WR}$.
Control for hold is the falling edge of $\overline{RD}$ or the rising edge of $\overline{WR}$.

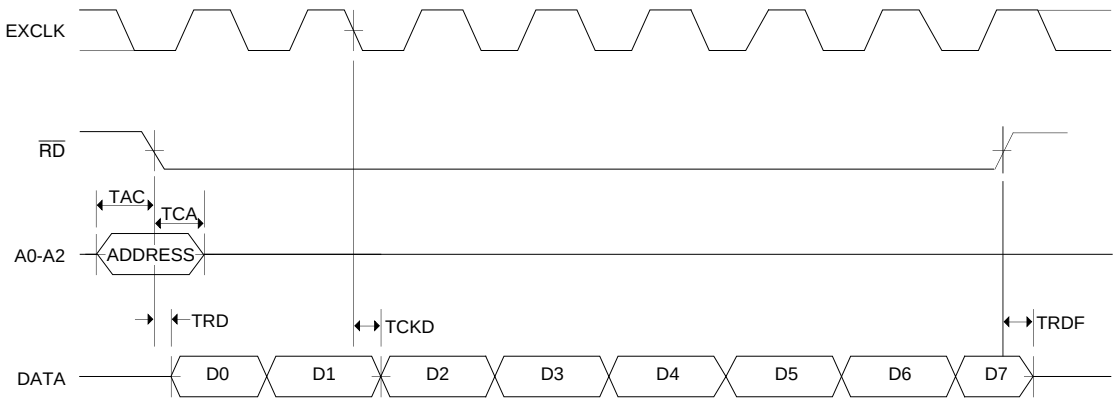
NOTE: Asserting ALE, $\overline{CS}$, and $\overline{RD}$ or $\overline{WR}$ concurrently can cause unintentional register accesses. When using non-8031 compatible processors, care must be taken to prevent this from occurring when designing the interface logic.

TIMING DIAGRAMS

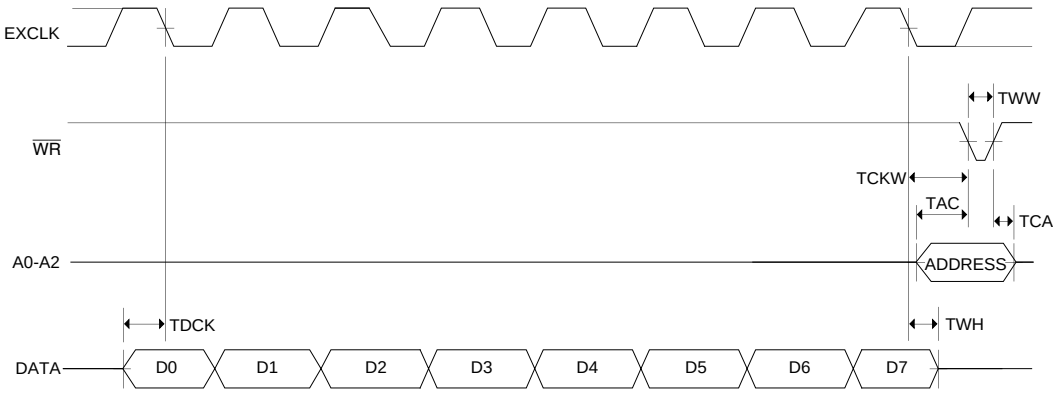
BUS TIMING DIAGRAM (PARALLEL VERSION)



READ TIMING DIAGRAM (SERIAL VERSION)



WRITE TIMING DIAGRAM (SERIAL VERSION)



APPLICATIONS INFORMATION

GENERAL CONSIDERATIONS

Figures 1 and 2 show basic circuit diagrams for K-Series modem integrated circuits. K-Series products are designed to be used in conjunction with a control processor, a UART or RS-232 serial data interface, and a DAA phone line interface to function as a typical intelligent modem. The K-Series ICs interface directly with Intel 8048 and 80C51 microprocessors for control and status monitoring purposes.Two typical DAA arrangements are shown: one for a split ±5 or ±12 volt design and one for a single 5 volt design. These diagrams are for reference only and do not represent production-ready modem designs.

K-Series devices are available with two control interface versions: one for a parallel multiplexed address/data interface, and one for a serial interface. The parallel version is intended for use with 8039/48 or 8031/51 microcontrollers from Intel or many other manufacturers. The serial interface 22-pin version can be used with other microcontrollers or in applications where only a limited number of port lines are available or the application does not lend itself to a multiplexed address/data interface. The parallel versions may also be used in the Serial mode, as explained in the data sheet pin description.

In most applications the controller will monitor the serial data for commands from the DTE and the received data for break signals from the far end modem. In this way, commands to the modem are sent over the same line as the transmitted data. In other applications the RS-232 interface handshake lines are used for modem control.

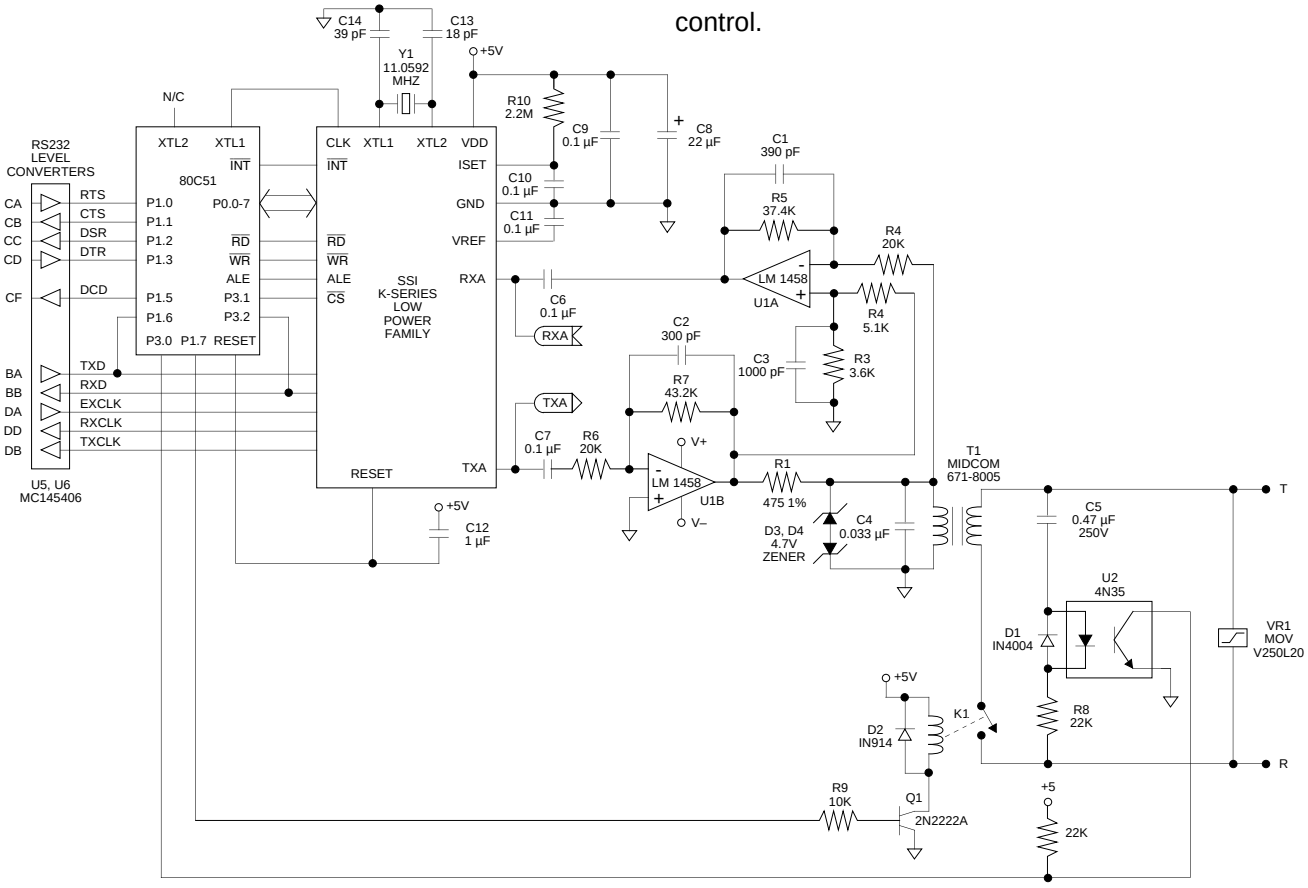


FIGURE 1: Basic Box Modem with Dual-Supply Hybrid

DIRECT ACCESS ARRANGEMENT (DAA)

The telephone line interfaces show two examples of how the "hybrid" may be implemented. The split supply design (Figure 1) is a typical two op-amp hybrid. The receive op-amp serves two purposes. It supplies gain to amplify the receive signal to the proper level for the modem's detectors and demodulator, and it removes the transmitted signal from the receive signal present at the transformer. This is done by supplying a portion of the transmitted signal to the non-inverting input of the receive op-amp at the same amplitude as the signal appearing at the transformer, making the transmit signal Common mode.

The single-supply hybrid is more complex than the dual-supply version described above, but its use eliminates the need for a second power supply. This circuit (Figure 2) uses a bridged drive to allow undistorted signals to be sent with a single 5V supply. Because DTMF tones utilize a higher amplitude than data, these signals will clip if a single-ended drive approach is used. The bridged driver uses an extra op-amp (U1A) to invert the signal coming from the gain setting op-amp (U1B) before sending it to the other leg of the transformer. Each op-amp then supplies half the drive signal to the transformer. The receive amplifier (U1C) picks off its signal at the junction of the impedance matching resistor and the transformer. Because the bottom leg of the transformer is being driven in one direction by U1A and the resistor is driven in the opposite direction at the same time by U1B, the junction of the transformer and resistor remains relatively constant and the receive signal is unaffected.

DESIGN CONSIDERATIONS

Silicon Systems' 1-chip modem products include all basic modem functions. This makes these devices adaptable for use in a variety of applications, and as easy to control as conventional digital bus peripherals.

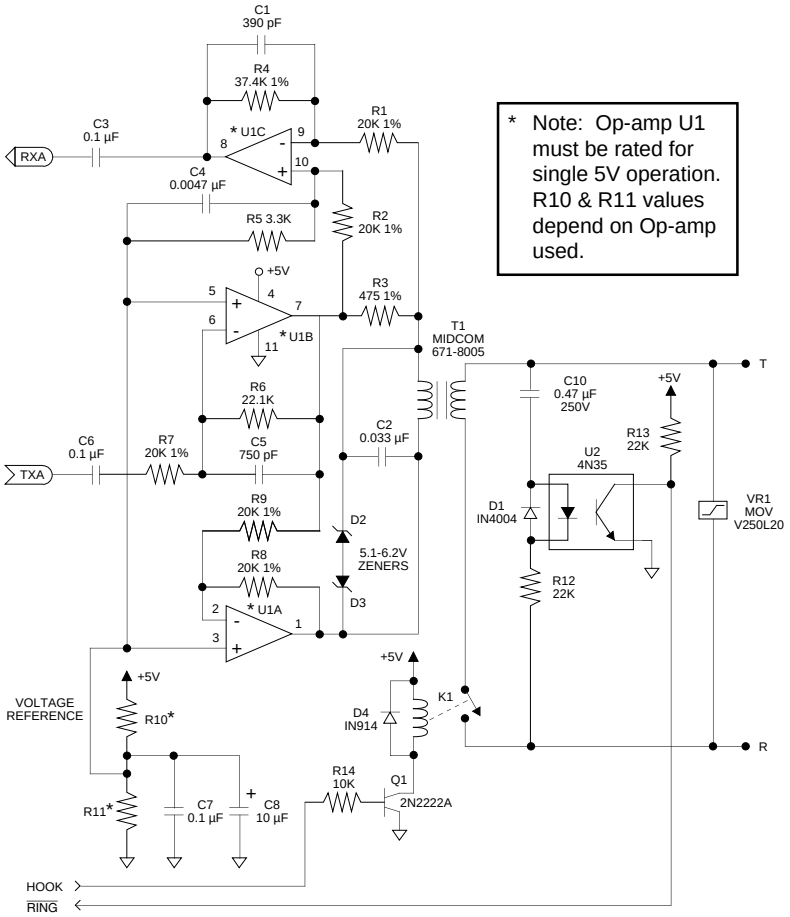


FIGURE 2: Single 5V Hybrid Version

Unlike digital logic circuitry, modem designs must properly contend with precise frequency tolerances and very low level analog signals, to ensure acceptable performance. Using good analog circuit design practices will generally result in a sound design. Following are additional recommendations which should be taken into consideration when starting new designs.

CRYSTAL OSCILLATOR

The K-Series crystal oscillator requires a Parallel mode (antiresonant) crystal which operates at 11.0592 MHz. It is important that this frequency be maintained to within ±0.01% accuracy.

In order for a Parallel mode crystal to operate correctly and to specification, it must have a load capacitor connected to the junction of each of the crystal and internal inverter connections, terminated to ground. The values of these capacitors depend primarily on the crystal's characteristics, and to a lesser degree on the internal inverter circuit. The values used affect the accuracy and start up characteristics of the oscillator.

LAYOUT CONSIDERATIONS

Good analog/digital design rules must be used to control system noise in order to obtain highest performance in modem designs. The more digital circuitry present on the PC board, the more this attention to noise control is needed. The modem should be treated as a high impedance analog device. A 22 µF electrolytic capacitor in parallel with a 0.1 µF ceramic capacitor between VDD and GND is recommended. Liberal use of ground planes and larger traces on power and ground are also highly favored. High speed digital circuits tend to generate a significant amount of EMI (Electro-Magnetic Interference) which must be minimized in order to meet regulatory agency limitations. To accomplish this, high speed digital devices should be locally bypassed, and the telephone line interface and K-Series device should be located close to each other near the area of the board where the phone line connection is accessed. To avoid problems, power supply and ground traces should be routed separately to the analog and digital functions on the board, and digital signals should not be routed near low level or high impedance analog traces. The analog and digital grounds should only connect at one point near the K-Series device ground pin to avoid ground loops. The K-Series modem IC's should have both high frequency and low frequency bypassing as close to the package as possible.

MODEM PERFORMANCE CHARACTERISTICS

The curves presented here define modem IC performance under a variety of line conditions while inducing disturbances that are typical of those encountered during data transmission on public service telephone lines. Test data was taken using an AEA Electronics' "Autotest I" modem test set and line simulator, operating under computer control. All tests were run full-duplex, using a Concord Data Systems 224 as the reference modem. A 511 pseudo-random-bit pattern was used for each data point. Noise was C-message weighted and all signal-to-noise (S/N) ratios reflect total power measurements similar to the CCITT V.56 measurement specification. The individual tests are defined as follows.

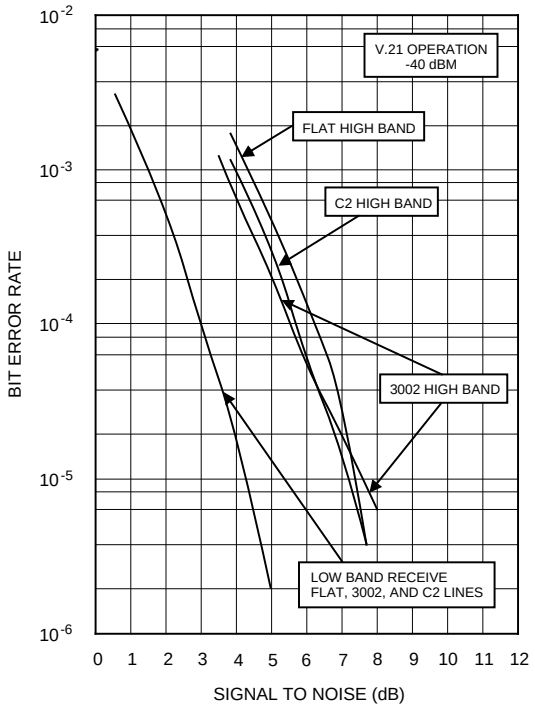
BER vs. S/N

This test measures the ability of the modem to operate over noisy lines with a minimum of data-transfer errors. Since some noise is generated in the best of dial-up lines, the modem must operate with the lowest S/N ratio possible. Better modem performance is indicated by test curves that are closest to the BER axis. A narrow spread between curves representing the four line parameters indicates minimal variation in performance while operating over a range of aberrant operating conditions. Typically, a DPSK modem will exhibit better BER-performance test curves receiving in the low band than in the high band.

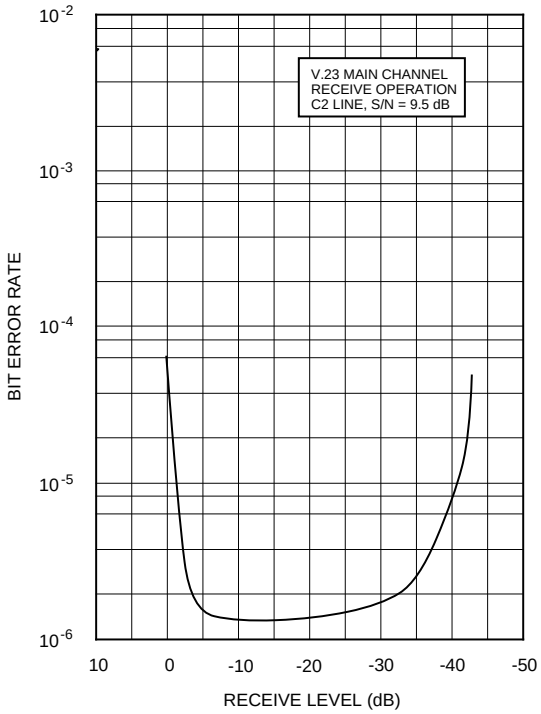
BER vs. Receive Level

This test measures the dynamic range of the modem. Because signal levels vary widely over dial-up lines, the widest possible dynamic range is desirable. The minimum Bell specification calls for 36 dB of dynamic range. S/N ratios are held constant at the indicated values while the receive level is lowered from a very high to very low signal levels. The width of the "bowl" of these curves, taken at the BER point, is the measure of dynamic range.

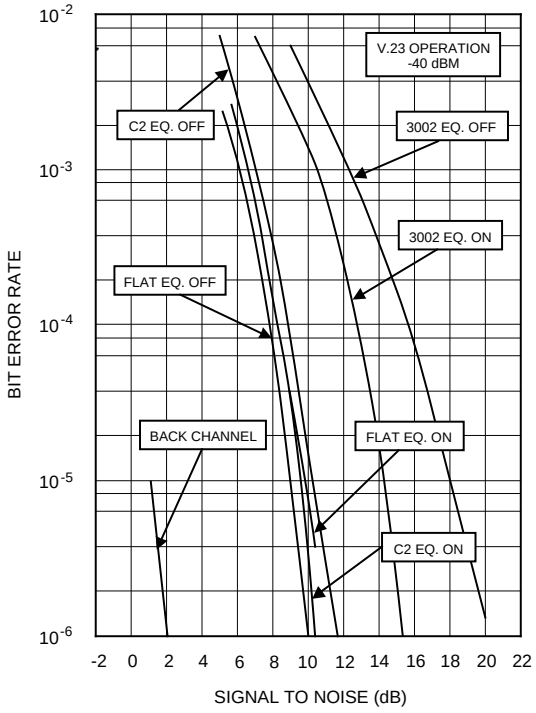
SSI 73K321L
BER vs SIGNAL TO NOISE



*SSI 73K321L
BER vs RECEIVE LEVEL (V.23)



*SSI 73K321L
BER vs S/N (V.23 ONLY)**



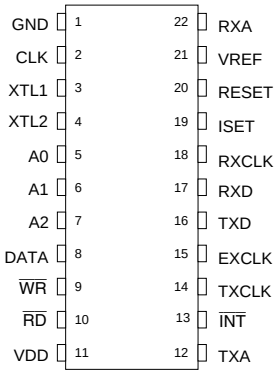
* = "EQ On" Indicates bit CR1 D4 is set for additional phase equalization.

** = 73K302L performance is similar to that of the 73K322L. V.23 operation corresponds to Bell 202.

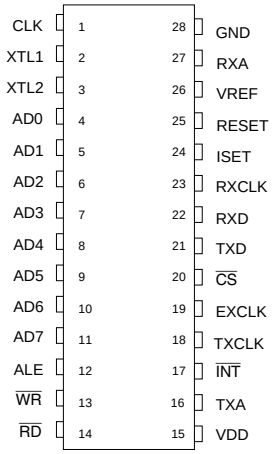
PACKAGE PIN DESIGNATIONS

(TOP VIEW)

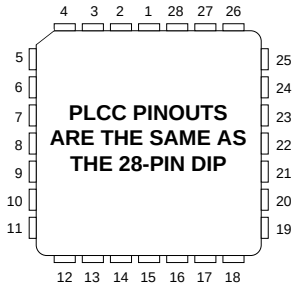
CAUTION: Use handling procedures necessary for a static sensitive component.



400-Mil 22-Pin DIP



600-Mil 28-Pin DIP



28-Pin PLCC

ORDERING INFORMATION

PART DESCRIPTION	ORDER NO.	PKG. MARK
SSI 73K321L 28-Pin 5V Supply Plastic Dual-In-Line	73K321L-IP	73K321L-IP
Plastic Leaded Chip Carrier	73K321L-IH	73K321L-IH
SSI 73K321L 22-Pin 5V Supply Plastic Dual-In-Line	73K321SL-IP	73K321SL-IP

Silicon Systems, Inc., 14351 Myford Road, Tustin, CA 92680-7022, (714) 573-6000, FAX: (714) 573-6914

SSI 73K322L
CCITT V.23, V.22, V.21 Single-Chip Modem

February 1996

DESCRIPTION

The SSI 73K322L is a highly integrated single-chip modem IC which provides the functions needed to construct a CCITT V.23, V.22 and V.21 compatible modem, capable of 1200 or 0-300 bit/s full-duplex operation or 0-1200 bit/s half-duplex operation with or without the back channel over dial-up lines. The SSI 73K322L is an enhancement of the SSI 73K221L single-chip modem with performance characteristics suitable for European and Asian telephone systems. The SSI 73K322L produces either 550 or 1800 Hz guard tone, recognizes and generates a 2100 Hz answer tone, and supports V.21 for 300 Hz FSK operation. It also operates in V.23, 1200 bit/s FSK mode. The SSI 73K322L integrates analog, digital, and switched-capacitor array functions on a single substrate,offering excellent performance and a high level of functional integration in a single 28- or 22-pin DIP configuration. The SSI 73K322L operates from a single +5V supply with very low power consumption.

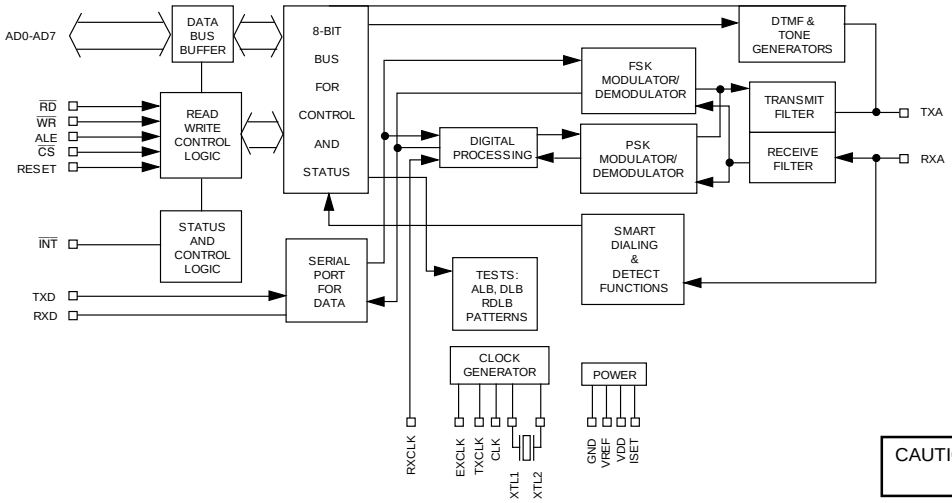
The SSI 73K322L includes the DPSK and FSK modulator/demodulator functions, call progress and handshake tone monitor test modes, and a tone generator capable of producing DTMF, answer, calling and 550 or 1800 Hz guard tone. This device supports V.23, V.22 (except mode v) and V.21 modes of operation, allowing both synchronous and

(continued)

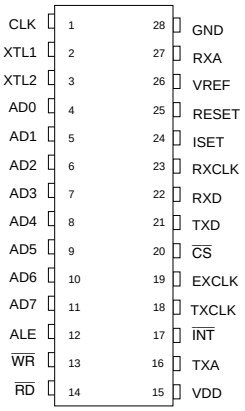
FEATURES

- **One-chip CCITT V.23, V.22 and V.21 standard compatible modem data pump**
- **Full-duplex operation at 0-300 bit/s (FSK) or 600 and 1200 bit/s (DPSK) or 0-1200 bit/s (FSK) forward channel with or without 0-75 bit/s back channel**
- **Interfaces directly with standard microprocessors (8048, 80C51 typical)**
- **Serial or parallel microprocessor bus for control**
- **Serial port for data transfer**
- **Both synchronous and asynchronous modes of operation**
- **Call progress, carrier, precise answer tone (2100 Hz), calling tone (1300 Hz) and FSK mark detectors**
- **DTMF and 550 or 1800 Hz guard tone generators**
- **Test modes available: ALB, DL, RDL, Mark, Space, Alternating bit patterns**
- **Precise automatic gain control allows 45 dB dynamic range**
- **CMOS technology for low power consumption using 30 mW @ 5V from a single power supply**
- **Surface mount PLCC package available**

BLOCK DIAGRAM



PIN DIAGRAM



CAUTION: Use handling procedures necessary for a static sensitive component.

DESCRIPTION (continued)

asynchronous communications. The SSI 73K322L is designed to appear to the systems designer as a microprocessor peripheral, and will easily interface with popular one-chip microprocessors (80C51 typical) for control of modem functions through its 8-bit multiplexed address/data bus or via an optional serial control bus. An ALE control line simplifies address demultiplexing. Data communications occurs through a separate serial port only.

The SSI 73K322L is ideal for use in either free standing or integral system modem products where multi-standard data communications over the 2-wire switched telephone network is desired. Its high functionality, low power consumption and efficient packaging simplify design requirements and increase system reliability. A complete modem requires only the addition of the phone line interface, a control microprocessor, and RS-232 level converter for a typical system. The SSI 73K322L is part of Silicon Systems K-Series family of pin and function compatible single-chip modem products. These devices allow systems to be configured for higher speeds and Bell or CCITT operation with only a single component change.

OPERATION

ASYNCHRONOUS MODE

Data transmission for the DPSK mode requires that data ultimately be transmitted in a synchronous fashion. The SSI 73K322L includes ASYNC/SYNC and SYNC/ASYNC converters which delete or insert stop bits in order to transmit data at a regular rate. In Asynchronous mode the serial data comes from the TXD pin into the ASYNC/SYNC converter. The ASYNC/SYNC converter accepts the data provided on the TXD pin which normally must be 1200 or 600 bit/s +1.0%, -2.5%. The rate converter will then insert or delete stop bits in order to output a signal which is 1200 or 600 bit/s ± 0.01% (± 0.01% is the crystal tolerance).

The SYNC/ASYNC converter also has an extended overspeed mode which allows selection of an output overspeed range of either +1% or +2.3%. In the extended overspeed mode, stop bits are output at 7/8 the normal width.

The serial data stream from the transmit buffer or the rate converter is passed through the data scrambler and onto the analog modulator. The data scrambler can be bypassed under processor control when unscrambled data must be transmitted. If serial input data contains a break signal through one character (including start and stop bits) the break will be extended to at least 2 • N + 3 bits long (where N is the number of transmitted bits/character).

Serial data from the demodulator is passed first through the data descrambler and then through the SYNC/ASYNC converter. The ASYNC/ASYNC converter will reinsert any deleted stop bits and output data at an intra-character rate (bit-to-bit timing) of no greater than 1219 bit/s. An incoming break signal (low through two characters) will be passed through without incorrectly inserting a stop bit.

SYNCHRONOUS MODE

The CCITT V.22 standard defines synchronous operation at 600 and 1200 bit/s. Operation is similar to that of the Asynchronous mode except that data must be synchronized to a provided clock and no variation in data transfer rate is allowable. Serial input data appearing at TXD must be valid on the rising edge of TXCLK.

TXCLK is an internally derived signal in Internal mode and is connected internally to the RXCLK pin in Slave mode. Receive data at the RXD pin is clocked out on the falling edge of RXCLK. The ASYNCH/SYNCH converter is bypassed when Synchronous mode is selected and data is transmitted out at the same rate as it is input.

DPSK MODULATOR/DEMODULATOR

In DPSK mode the SSI 73K322L modulates a serial bit stream into di-bit pairs that are represented by four possible phase shifts as prescribed by the V.22 standards. The base-band signal is then filtered to reduce intersymbol interference on the bandlimited 2-wire telephone line. Transmission occurs using either a 1200 Hz (Originate mode) or 2400 Hz carrier (Answer mode). Demodulation is the reverse of the modulation process, with the incoming analog signal eventually decoded into di-bits and converted back to a serial bit stream. The demodulator also recovers the clock which was encoded into the analog signal during modulation. Demodulation occurs using either a 1200 Hz carrier (Answer mode or ALB Originate mode) or a 2400 Hz carrier (Originate mode or ALB Answer mode). The SSI 73K322L uses a phase locked loop coherent demodulation technique for optimum receiver performance.

FSK MODULATOR/DEMODULATOR

The FSK modulator produces a frequency modulated analog output signal using two discrete frequencies to represent the binary data. V.21 mode uses 980 and 1180 Hz (originate, mark and space) or 1650 and 1850 Hz (answer, mark and space). V.23 mode uses 1300 and 2100 Hz for the main channel and 390 and 450 Hz for the back channel. The modulation rate of the back channel is up to 75 baud. Demodulation involves detecting the received frequencies and decoding them into the appropriate binary value. The rate converter and scrambler/descrambler are automatically bypassed in the V.21 or V.23 modes.

PASSBAND FILTERS AND EQUALIZERS

High and low band filters are included to shape the amplitude and phase response of the transmit and receive signals and provide compromise delay equalization and rejection of out-of-band signals in the receive channel. Amplitude and phase equalization are necessary to compensate for distortion of the transmission line and to reduce intersymbol interference in the bandlimited receive signal. The transmit signal filtering approximates a 75% square root of raised Cosine frequency response characteristic.

AGC

The automatic gain control maintains a signal level at the input to the demodulators which is constant to within 1 dB. It corrects quickly for increases in signal which would cause clipping and provides a total receiver dynamic range of >45 dB.

PARALLEL BUS INTERFACE

Four 8-bit registers are provided for control, option select and status monitoring. These registers are addressed with the AD0, AD1, and AD2 multiplexed address lines (latched by ALE) and appear to a control microprocessor as four consecutive memory locations. Two control registers and the tone register are read/write memory. The detect register is read only and cannot be modified except by modem response to monitored parameters.

SERIAL COMMAND INTERFACE

The serial command interface allows access to the SSI 73K322L control and status registers via a serial command port (22-pin version only). In this mode the A0 , A1 and A2 lines provide register addresses for data passed through the data pin under control of the $\overline{RD}$ and $\overline{WR}$ lines. A read operation is initiated when the $\overline{RD}$ line is taken low. The first bit is available after $\overline{RD}$ is brought low and the next seven cycles of EXCLK will then transfer out seven bits of the selected address location LSB first. A write takes place by shifting in eight bits of data LSB first for eight consecutive cycles of EXCLK. $\overline{WR}$ is then pulsed low and data transferred into the selected register occurs on the rising edge of $\overline{WR}$.

SPECIAL DETECT CIRCUITRY

The special detect circuitry monitors the received analog signal to determine status or presence of carrier, answer tone and weak received signal (long loop condition), special tones such as FSK marking and the 1300 Hz calling tone are also detected. A highly frequency selective call progress detector provides adequate discrimination to accurately detect European call progress signals.

DTMF GENERATOR

The DTMF generator will output one of 16 standard tone pairs determined by a 4-bit binary value and TX DTMF mode bit previously loaded into the tone register. Tone generation is initiated when the DTMF mode is selected using the tone register and the transmit enable (CR0 bit D1) is changed from 0 to 1.

PIN DESCRIPTION

POWER

NAME	28-PIN	22-PIN	TYPE	DESCRIPTION
GND	28	1	I	System Ground.
VDD	15	11	I	Power supply input, 5V ±10%. Bypass with 0.1 and 22 µF capacitors to GND.
VREF	26	21	O	An internally generated reference voltage. Bypass with 0.1 µF capacitor to GND.
ISET	24	19	I	Chip current reference. Sets bias current for op-amps. The chip current is set by connecting this pin to VDD through a 2 MΩ resistor. ISET should be bypassed to GND with a 0.1 µF capacitor.

PARALLEL MICROPROCESSOR INTERFACE

ALE	12	-	I	Address latch enable. The falling edge of ALE latches the address on AD0-AD2 and the chip select on $\overline{CS}$.
AD0-AD7	4-11	-	I/O	Address/data bus. These bidirectional tri-state multiplexed lines carry information to and from the internal registers.
$\overline{CS}$	20	-	I	Chip select. A low on this pin during the falling edge of ALE allows a read cycle or a write cycle to occur. AD0-AD7 will not be driven and no registers will be written if $\overline{CS}$ (latched) is not active. The state of $\overline{CS}$ is latched on the falling edge of ALE.
CLK	1	2	O	Output clock. This pin is selectable under processor control to be either the crystal frequency (for use as a processor clock) or 16 x the data rate for use as a baud rate clock in DPSK modes only. The pin defaults to the crystal frequency on reset.
$\overline{INT}$	17	13	O	Interrupt. This open drain output signal is used to inform the processor that a detect flag has occurred. The processor must then read the detect register to determine which detect triggered the interrupt. $\overline{INT}$ will stay low until the processor reads the detect register or does a full reset.
$\overline{RD}$	14	-	I	Read. A low requests a read of the SSI 73K322L internal registers. Data cannot be output unless both $\overline{RD}$ and the latched $\overline{CS}$ are active or low.
RESET	25	20	I	Reset. An active high signal on this pin will put the chip into an inactive state. All control register bits (CR0, CR1, Tone) will be reset. The output of the CLK pin will be set to the crystal frequency. An internal pull down resistor permits power on reset using a capacitor to VDD.

PARALLEL MICROPROCESSOR INTERFACE (continued)

NAME	28-PIN	22-PIN	TYPE	DESCRIPTION
$\overline{WR}$	13	-	I	Write. A low on this informs the SSI 73K322L that data is available on AD0-AD7 for writing into an internal register. Data is latched on the rising edge of $\overline{WR}$. No data is written unless both $\overline{WR}$ and the latched $\overline{CS}$ are low.

SERIAL MICROPROCESSOR INTERFACE

A0-A2	-	5-7	I	Register Address Selection. These lines carry register addresses and should be valid during any read or write operation.
DATA	-	8	I/O	Serial Control Data. Data for a read/write operation is clocked in or out on the falling edge of the EXCLK pin. The direction of data flow is controlled by the $\overline{RD}$ pin. $\overline{RD}$ low outputs data. $\overline{RD}$ high inputs data.
$\overline{RD}$	-	10	I	Read. A low on this input informs the SSI 73K322L that data or status information is being read by the processor. The falling edge of the $\overline{RD}$ signal will initiate a read from the addressed register. The $\overline{RD}$ signal must continue for eight falling edges of EXCLK in order to read all eight bits of the referenced register. Read data is provided LSB first. Data will not be output unless the $\overline{RD}$ signal is active.
$\overline{WR}$	-	9	I	Write. A low on this input informs the SSI 73K322L that data or status information has been shifted in through the DATA pin and is available for writing to an internal register. The normal procedure for a write is to shift in data LSB first on the DATA pin for eight consecutive falling edges of EXCLK and then to pulse $\overline{WR}$ low. Data is written on the rising edge of $\overline{WR}$.
Note:	In the serial, 22-pin version, the pins AD0-AD7, ALE and $\overline{CS}$ are removed and replaced with the pins; A0, A1, A2, DATA, and an unconnected pin. Also, the $\overline{RD}$ and $\overline{WR}$ controls are used differently. The Serial Control mode is provided in the parallel control versions by tying ALE high and $\overline{CS}$ low. In this configuration AD7 becomes DATA and AD0, AD1 and AD2 become A0, A1 and A2, respectively.			

DTE USER INTERFACE

NAME	28-PIN	22-PIN	TYPE	DESCRIPTION
EXCLK	19	15	I	External Clock. This signal is used only in synchronous DPSK transmission when the external timing option has been selected. In the External Timing mode the rising edge of EXCLK is used to strobe synchronous DPSK transmit data available on the TXD pin. Also used for serial control interface.

RS-232 INTERFACE (continued)

NAME	28-PIN	22-PIN	TYPE	DESCRIPTION
RXCLK	23	18	O	Receive Clock. The falling edge of this clock output is coincident with the transitions in the serial received DPSK data output. The rising edge of RXCLK can be used to latch the valid output data. RXCLK will be valid as long as a carrier is present. In V.23 or V.21 mode a clock which is 16 x1200 (or 16 x 75) or 16 x 300 Hz baud data rate is output, respectively, for driving a UART.
RXD	22	17	O	Received Data Output. Serial receive data is available on this pin. The data is always valid on the rising edge of RXCLK when in Synchronous mode. RXD will output constant marks if no carrier is detected.
TXCLK	18	14	O	Transmit Clock.This signal is used only in synchronous DPSK transmission to latch serial input data on the TXD pin. Data must be provided so that valid data is available on the rising edge of the TXCLK. The transmit clock is derived from different sources depending upon the Synchronization mode selection. In Internal Mode the clock is 1200 Hz generated internally. In External Mode TXCLK is phase locked to the EXCLK pin. In Slave Mode TXCLK is phase locked to the RXCLK pin. TXCLK is always active. In V.23 or V.21 mode the output is a 16 x 1200 (or 16 x 75) or 16 x 300 Hz baud clock, respectively for driving a UART.
TXD	21	16	I	Transmit Data Input. Serial data for transmission is applied on this pin. In Synchronous modes, the data must be valid on the rising edge of the TXCLK clock. In Asynchronous modes (1200 or 300 baud) no clocking is necessary. DPSK must be 1200/600 bit/s +1%, -2.5% or +2.3%, -2.5% in Extended Overspeed mode.

ANALOG INTERFACE AND OSCILLATOR

RXA	27	22	I	Received modulated analog signal input from the telephone line interface.
TXA	16	12	O	Transmit analog output to the telephone line interface.
XTL1 XTL2	2 3	3 4	I I	These pins are for the internal crystal oscillator requiring a 11.0592 MHz Parallel mode crystal and two load capacitors to Ground. XTL2 can also be driven from an external clock.

REGISTER DESCRIPTIONS

Four 8-bit internal registers are accessible for control and status monitoring. The registers are accessed in read or write operations by addressing the A0 and A1 address lines in Serial mode, or the AD0 and AD1 lines in Parallel mode. The AD0 and AD1 lines are latched by ALE. Register CR0 controls the method by which data is transferred over the phone line. CR1 controls the interface between the microprocessor and the SSI 73K322L internal state. DR is a detect register which provides an indication of monitored modem status conditions. TR, the tone control register, controls the DTMF generator, answer and guard tones and RXD output gate used in the modem initial connect sequence. All registers are read/write except for DR which is read only. Register control and status bits are identified below:

REGISTER BIT SUMMARY

	ADDRESS	DATA BIT NUMBER							
REGISTER	AD2 - AD0	D7	D6	D5	D4	D3	D2	D1	D0
CONTROL REGISTER 0 CR0	000	MODULATION OPTION		TRANSMIT MODE 3	TRANSMIT MODE 2	TRANSMIT MODE 1	TRANSMIT MODE 0	TRANSMIT ENABLE	ANSWER/ ORIGINATE
CONTROL REGISTER 1 CR1	001	TRANSMIT PATTERN 1	TRANSMIT PATTERN 0	ENABLE DETECT INTERRUPT	BYPASS SCRAMBLER/ ADD PH. EQ. (V.23)	CLK CONTROL	RESET	TEST MODE 1	TEST MODE 0
DETECT REGISTER DR	010			RECEIVE DATA	UNSCR. MARKS	CARRIER DETECT	SPECIAL TONE	CALL PROGRESS	LONG LOOP
TONE CONTROL REGISTER TR	011	RXD OUTPUT CONTROL	TRANSMIT GUARD/ CALLING TONE	TRANSMIT ANSWER TONE	TRANSMIT DTMF	DTMF3	DTMF2/ V.23 FDX	DTMF1/ OVERSPEED	DTMF0/GUARD/ ANSWER/SPEC. TONE SELECT
CONTROL REGISTER 2 CR2	100				THESE REGISTER LOCATIONS ARE RESERVED FOR				
CONTROL REGISTER 3 CR3	101				USE WITH OTHER K-SERIES FAMILY MEMBERS				
ID REGISTER ID	110	ID	ID	ID	ID				

NOTE: When a register containing reserved control bits is written into, the reserved bits must be programmed as 0's.

REGISTER ADDRESS TABLE

REGISTER	ADDRESS AD2 - AD0	DATA BIT NUMBER D7	D6	D5	D4	D3	D2	D1	D0
CONTROL REGISTER 0 CR0	000	MODULATION OPTION		TRANSMIT MODE 3	TRANSMIT MODE 2	TRANSMIT MODE 1	TRANSMIT MODE 0	TRANSMIT ENABLE	ORIGINATE/ ANSWER
		0=1200 BIT/S DPSK 1=600 BIT/S DPSK 0=V.23 FSK 1=V.21 FSK		0000=PWR DOWN 0001=INT SYNCH 0010=EXT SYNCH 0011=SLAVE SYNCH 0100=ASYNCH 8 BITS/CHAR 0101=ASYNCH 9 BITS/CHAR 0110=ASYNCH 10 BITS/CHAR 0111=ASYNCH 11 BITS/CHAR 1100=FSK				0=DISABLE TXA OUTPUT 1=ENABLE TXA OUTPUT	IN V.21 OR V.22 MODE: 0=ANSWER 1=ORIGINATE IN V.23 MODE : 0=RECEIVE @ 1200 BIT/S, TRANSMIT @ 75 BIT/S 1=RECEIVE @ 75 BIT/S, TRANSMIT @ 1200 BIT/S
CONTROL REGISTER 1 CR1	001	TRANSMIT PATTERN 1	TRANSMIT PATTERN 0	ENABLE DETECT INTERRUPT	BYPASS SCRAMBLER/ ADD PH. EQ.	CLK CONTROL	RESET	TEST MODE 1	TEST MODE 0
		00=TX DATA 01=TX ALTERNATE 10=TX MARK 11=TX SPACE		0=DISABLE 1=ENABLE	0=NORMAL 1=BYPASS SCRAMBLER 1=ADD EXTRA PHASE EQ. IN V.23 ONLY	0=XTAL 1=16 X DATA RATE OUTPUT AT CLK PIN IN DPSK MODE ONLY	0=NORMAL 1=RESET	00=NORMAL 01=ANALOG LOOPBACK 10=REMOTE DIGITAL LOOPBACK 11=LOCAL DIGITAL LOOPBACK	
DETECT REGISTER DR	010			RECEIVE DATA	UNSCR. MARK DETECT	CARRIER DETECT	SPECIAL TONE	CALL PROGRESS	LONG LOOP
				OUTPUTS RECEIVED DATA STREAM		0=CONDITION NOT DETECTED 1=CONDITION DETECTED			
TONE CONTROL REGISTER TR	011	RXD OUTPUT CONTROL	TRANSMIT GUARD/ CALLING TONE	TRANSMIT ANSWER TONE	TRANSMIT DTMF	DTMF3	DTMF2 V.23 FDX	DTMF1/ OVERSPEED	DTMF0/GUARD/ ANSWER/ SPECIAL TONE
		RXD PIN 0=NORMAL 1=TRI STATE	0=OFF 1=ON	0=OFF 1=ON	0=DATA 1=TX DTMF	4 BIT CODE FOR 1 OF 16 DUAL TONE COMBINATIONS.	0=NORMAL 1=ALLOWS V.23 FULL DUPLEX OPERATION		0=1800 Hz G.T. (V.22). 2225 Hz ANS TONE GENERATED, FSK MARK DETECT SELECTED 1=550 Hz G.T. (V.22) 2100 Hz ANS TONE GENERATED & DETECTED (V.21, V.22) 1300 Hz DETECTED (V.23)
ID REGISTER 10	110	ID	ID	ID	ID				

00XX=73K212L, 322L, 321L
01XX=73K221L, 302L
10XX=73K222L
1100=73K224L
1110=73K324L
1101=73K312L

CONTROL REGISTER 0

	D7	D6	D5	D4	D3	D2	D1	D0
CR0 000	MODUL. OPTION		TRANSMIT MODE 3	TRANSMIT MODE 2	TRANSMIT MODE 1	TRANSMIT MODE 0	TRANSMIT ENABLE	ANSWER/ ORIGINATE

BIT NO.	NAME	CONDITION	DESCRIPTION
D0 high	Answer/	0 Originate	Selects Answer mode in V.21 and V.22 (transmit in band), receive in low band or in V.23 HDX mode, receive at 1200 bit/s and transmit at 75 bit/s.
		1	Selects Originate mode in V.21 and V.22 (transmit in low band), receive in high band or in V.23 HDX mode, receive at 75 bit/s and transmit at 1200 bit/s.
			Note: This bit works with TR bit D0 to program special tones detected in Tone Register. See detect and tone registers.
D1	Transmit Enable	0	Disables transmit output at TXA.
		1	Enables transmit output at TXA.
			Note: Answer tone and DTMF TX control require TX enable.
D5, D4,D3, D2	Transmit Mode	D5 D4 D3 D2	
		0 0 0 0	Selects Power Down mode. All functions disabled except digital interface.
		0 0 0 1	Internal Synchronous mode. In this mode TXCLK is an internally derived 1200 Hz signal. Serial input data appearing at TXD must be valid on the rising edge of TXCLK. Receive data is clocked out of RXD on the falling edge of RXCLK.
		0 0 1 0	External Synchronous mode. Operation is identical to internal synchronous, but TXCLK is connected internally to EXCLK pin, and a 1200 Hz ± 0.01% clock must be supplied externally.
		0 0 1 1	Slave Synchronous mode. Same operation as other Synchronous modes. TXCLK is connected internally to the RXCLK pin in this mode.
		0 1 0 0	Selects DPSK Asynchronous mode - 8 bits/character (1 start bit, 6 data bits, 1 stop bit).
		0 1 0 1	Selects DPSK Asynchronous mode - 9 bits/character (1 start bit, 7 data bits, 1 stop bit).
		0 1 1 0	Selects DPSK Asynchronous mode - 10 bits/character (1 start bit, 8 data bits, 1 stop bit).
		0 1 1 1	Selects DPSK Asynchronous mode - 11 bits/character (1 start bit, 8 data bits, Parity and 1 or 2 stop bits).
		1 1 0 0	Selects FSK operation.

CONTROL REGISTER 0 (continued)

	D7	D6	D5	D4	D3	D2	D1	D0
CR0 000	MODUL. OPTION		TRANSMIT MODE 3	TRANSMIT MODE 2	TRANSMIT MODE 1	TRANSMIT MODE 0	TRANSMIT ENABLE	ANSWER/ ORIGINATE

BIT NO.	NAME	CONDITION	DESCRIPTION
D6		0	Not used; must be written as a "0."
D7	Modulation Option	D7 D5 D4	Selects:
		0 0 X	PSK Asynchronous mode at 1200 bit/s.
		1 0 X	PSK Asynchronous mode at 600 bit/s.
		0 1 1	FSK CCITT V.23 mode.
		1 1 1	FSK CCITT V.21 mode.

CONTROL REGISTER 1

	D7	D6	D5	D4	D3	D2	D1	D0
CR1 001	TRANSMIT PATTERN 1	TRANSMIT PATTERN 0	ENABLE DETECT INTER.	BYPASS SCRAMB/ ADD PH. EQ.	CLK CONTROL	RESET	TEST MODE 1	TEST MODE 0

BIT NO.	NAME	CONDITION	DESCRIPTION
D1, D0	Test Mode	D1 D0	
		0 0	Selects normal operating mode.
		0 1	Analog Loopback mode. Loops the transmitted analog signal back to the receiver, and causes the receiver to use the same center frequency as the transmitter. To squelch the TXA pin, transmit enable must be forced low.
		1 0	Selects remote digital loopback. Received data is looped back to transmit data internally, and RXD is forced to a mark. Data on TXD is ignored.
		1 1	Selects local digital loopback. Internally loops TXD back to RXD and continues to transmit carrier from TXA pin.
D2	Reset	0	Selects normal operation.
		1	Resets modem to power down state. All control register bits (CR0, CR1, Tone) are reset to zero. The output of the CLK pin will be set to the crystal frequency.

CONTROL REGISTER 1 (continued)

	D7	D6	D5	D4	D3	D2	D1	D0
CR1 001	TRANSMIT PATTERN 1	TRANSMIT PATTERN 0	ENABLE DETECT INTER.	BYPASS SCRAMB/ ADD PH. EQ.	CLK CONTROL	RESET	TEST MODE 1	TEST MODE 0

BIT NO.	NAME	CONDITION	DESCRIPTION
D3	CLK Control	0	Selects 11.0592 MHz crystal echo output at CLK pin.
		1	Selects 16 X the data rate, output at CLK pin in DPSK modes only.
D4	Bypass Scrambler/ Add Phase Equalization	0	Selects normal operation. DPSK data is passed through scrambler.
		1	Selects Scrambler Bypass. DPSK data is routed around scrambler in the transmit path. In V.23 mode, additional phase equalization is added to the main channel filters when D4 is set to 1.
D5	Enable Detect	0	Disables interrupt at $\overline{INT}$ pin.
		1	Enables $\overline{INT}$ output. An interrupts will be generated with a change in status of DR bits D1-D4. The special tone and call progress detect interrupts are masked when the TX enable bit is set. Carrier detect is masked when TX DTMF is activated. All interrupts will be disabled if the device is in power down mode.
D7, D6	Transmit Pattern	D7 D6	
		0 0	Selects normal data transmission as controlled by the state of the TXD pin.
		0 1	Selects an alternating mark/space transmit pattern for modem testing.
		1 0	Selects a constant mark transmit pattern.
		1 1	Selects a constant space transmit pattern.

DETECT REGISTER

	D7	D6	D5	D4	D3	D2	D1	D0
DR 010			RECEIVE DATA	UNSCR. MARK	CARR. DETECT	SPECIAL TONE	CALL PROG.	LONG LOOP

BIT NO.	NAME	CONDITION	DESCRIPTION
D0	Long Loop	0	Indicates normal received signal.
		1	Indicates low received signal level.
D1	Call Progress Detect	0	No call progress tone detected.
		1	Indicates presence of call progress tones. The call progress detection circuitry is activated by energy in the normal 350 to 620 Hz call progress band.
D2	Special Tone Detect	0	No special tone detected as programmed by CR0 bit D0 and Tone Register bit D0.
		1	Special tone detected. The detected tone is:
			(1) 2100 Hz answer tone if D0 of TR=1 and the device is in V.21 or V.22 originate mode.
			(2) 1300 Hz calling tone if D0 of TR=1 and the device is in V.21, or V.22 answer mode.
			(3) An FSK mark if D0 of TR = 0.
			Tolerance on special tones is ±3%.
D3	Carrier Detect	0	No carrier detected in the receive channel.
		1	Indicated carrier has been detected in the received channel.
D4	Unscrambled Mark	0	No unscrambled mark.
		1	Indicates detection of unscrambled marks in the received data. A valid indication requires that unscrambled marks be received for > 165.5 ± 6.5 ms.
D5	Receive Data		Continuously outputs the received data stream. This data is the same as that output on the RXD pin, but it is not disabled when RXD is tri-stated.
D6, D7			Not used.

TONE REGISTER

	D7	D6	D5	D4	D3	D2	D1	D0
TR 011	RXD OUTPUT CONTR.	TRANSMIT GUARD/ CALLING TONE	TRANSMIT ANSWER TONE	TRANSMIT DTMF	DTMF 3	DTMF 2/ V.23 FDX	DTMF 1/ OVER-SPEED	DTMF 0/ G.T./ANSW./ SP. TONE/ SELECT

BIT NO.	NAME	CONDITION	DESCRIPTION
D0	DTMF 0	D6 D5 D4 D0	D0 interacts with bits D6, D4, and CR0 as shown.
		X X 1 X	Transmit DTMF tones.
	Guard Tone/ Answer Tone	1 X 0 0	Select 1800 Hz guard tone if in V.22 and Answer mode in CR0.
	Special Tone/ Detect/Select	1 X 0 1	Select 550 Hz guard tone if in V.22 and Answer mode in CR0.
		X X 0 0	Mark of an FSK mode selected in CR0 is to be detected in D2 of DR.
		X X 0 1	2100 Hz answer tone will be detected in D2 of DR if V.21 or V.22 Originate mode is selected in CR0.
			1300 Hz calling tone will be detected in D2 of DR if V.21, or V.22 Answer mode is selected in CR0.
		X 1 0 0	Transmit 2225 Hz Answer Tone
		X 1 0 1	Transmit 2100 Hz Answer Tone
D1	DTMF 1/ Overspeed	D4 D1	D1 interacts with D4 as shown.
		0 0	Asynchronous DPSK 1200 or 600 bit/s +1.0% -2.5%.
		0 1	Asynchronous DPSK 1200 or 600 bit/s +2.3% -2.5%.
D2	DTMF 2/ V.23 FDX	0	Half-duplex asymetric operation in V.23 mode.
		1	Full-duplex (4-wire) operation in V.23 mode.
D3, D2, D1, D0	DTMF 3, 2, 1, 0	D3 D2 D1 D0	
		0 0 0 0 - 1 1 1 1	Programs 1 of 16 DTMF tone pairs that will be transmitted when TX DTMF and TX enable bit (CR0, bit D1) are set. Tone encoding is shown below:

KEYBOARD EQUIVALENT	DTMF CODE D3 D2 D1 D0	TONES LOW HIGH
1	0 0 0 1	697 1209
2	0 0 1 0	697 1336
3	0 0 1 1	697 1477
4	0 1 0 0	770 1209
5	0 1 0 1	770 1336
6	0 1 1 0	770 1477
7	0 1 1 1	852 1209

TONE REGISTER (continued)

	D7	D6	D5	D4	D3	D2	D1	D0
TR 011	RXD OUTPUT CONTR.	TRANSMIT GUARD/ CALLING TONE	TRANSMIT ANSWER TONE	TRANSMIT DTMF	DTMF 3	DTMF 2/ V.23 FDX	DTMF 1/ OVER-SPEED	DTMF 0/ GUARD/ SPECIAL TONE SEL

BIT NO.	NAME	CONDITION	DESCRIPTION
D3, D2, D1, D0 (cont.)			KEYBOARD EQUIVALENT / DTMF CODE D3 D2 D1 D0 / TONES LOW HIGH 8 — 1 0 0 0 — 852 1336 9 — 1 0 0 1 — 852 1477 0 — 1 0 1 0 — 941 1336 * — 1 0 1 1 — 941 1209 # — 1 1 0 0 — 941 1477 A — 1 1 0 1 — 697 1633 B — 1 1 1 0 — 770 1633 C — 1 1 1 1 — 852 1633 D — 0 0 0 0 — 941 1633
D4	Transmit DTMF	0	Disable DTMF.
		1	Activate DTMF.The selected DTMF tones are transmitted continuously when this bit is high. TX DTMF overrides all other transmit functions.
D5	Transmit Answer Tone	0	Disables answer tone generator.
		1	Enables answer tone generator. A 2100 Hz answer tone will be transmitted continuously when the transmit enable bit is set. The device must be in Answer mode. To transmit answer tone, the device must be in DPSK Answer mode.
D6	TX Guard or Calling Tone	0	Disables guard/calling tone generator.
		1	Transmit guard tone if in V.22 and answering; otherwise transmit calling tone, in any other mode including V.23 mode.
D7	RXD Output Control	0	Enables RXD pin. Receive data will be output on RXD.
		1	Disables RXD pin. The RXD pin reverts to a high impedance with internal weak pull-up resistor.

ID REGISTER

	D7	D6	D5	D4	D3	D2	D1	D0
ID 110	ID	ID	ID	ID				

BIT NO.	NAME	CONDITION	DESCRIPTION
D7, D6, D5 D4	Device Identification Signature	D7 D6 D5 D4	Indicates Device:
		0 0 X X	SSI 73K212L, 73K321L or 73K322L or 73K321L
		0 1 X X	SSI 73K221L or 73K302L
		1 0 X X	SSI 73K222L
		1 1 0 0	SSI 73K224L
		1 1 1 0	SSI 73K324L
		1 1 0 1	SSI 73K312L

ELECTRICAL SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT
VDD Supply Voltage	14	V
Storage Temperature	-65 to 150	°C
Soldering Temperature (10 sec.)	260	°C
Applied Voltage	-0.3 to VDD+0.3	V
Note: All inputs and outputs are protected from static charge using built-in, industry standard protection devices and all outputs are short-circuit protected.		

RECOMMENDED OPERATING CONDITIONS

PARAMETER	CONDITION	MIN	NOM	MAX	UNIT
VDD Supply voltage		4.5	5	5.5	V
TA, Operating Free-Air Temp.		-40		+85	°C
Clock Variation	(11.0592 MHz) Crystal or external clock	-0.01		+0.01	%
External Components (Refer to Application section for placement.)					
VREF Bypass Capacitor	(External to GND)	0.1			µF
Bias setting resistor	(Placed between VDD and ISET pins)	1.8	2	2.2	MΩ
ISET Bypass Capacitor	(ISET pin to GND)	0.1			µF
VDD Bypass Capacitor 1	(External to GND)	0.1			µF
VDD Bypass Capacitor 2	(External to GND)	22			µF
XTL1 Load Capacitor	Depends on crystal characteristics;			40	pF
XTL2 Load Capacitor	from pin to GND			20	

DC ELECTRICAL CHARACTERISTICS
(TA = -40°C to 85°C, VDD = recommended range unless otherwise noted.)

PARAMETER	CONDITION	MIN	NOM	MAX	UNIT
IDD, Supply Current	ISET Resistor = 2 MΩ				
IDDA, Active	CLK = 11.0592 MHz		8	12	mA
IDD1, Power-down	CLK = 11.0592 MHz			4	mA
IDD2, Power-down	CLK = 19.200 KHz			3	mA
Digital Inputs					
VIH, Input High Voltage					
Reset, XTL1, XTL2		3.0		VDD	V
All other inputs		2.0		VDD	V
VIL, Input Low Voltage		0		0.8	V
IIH, Input High Current	VI = VIH Max			100	µA
IIL, Input Low Current	VI = VIL Min	-200			µA
Reset Pull-down Current	Reset = VDD	1		50	µA
Input Capacitance	All Digital Input Pins			10	pF
Digital Outputs					
VOH, Output High Voltage	IOH MIN = -0.4 mA	2.4		VDD	V
VOL, Output Low Voltage	IO MAX = 1.6 mA			0.4	V
VOL, CLK Output	IO = 3.6 mA			0.6	V
RXD Tri-State Pull-up Curr.	RXD = GND	-1		-50	µA
CMAX, CLK Output	Maximum Capacitive Load			15	pF
Capacitance					
Inputs	Capacitance, all Digital Input pins			10	pF
XTAL1, 2 Load Capacitors	Depends on crystal characteristics	15		60	pF
CLK	Maximum Capacitive Load			15	pF

DYNAMIC CHARACTERISTICS AND TIMING

(TA = -40°C to +85°C, VDD = Recommended range unless otherwise noted.)

PARAMETER	CONDITION	MIN	NOM	MAX	UNIT
DPSK Modulator					
Carrier Suppression	Measured at TXA	45			dB
Output Amplitude	TX scrambled marks	-11	-10	-9	dBm0
FSK Modulator					
Output Freq. Error	CLK = 11.0592 MHz	-0.35		+0.35	%
Transmit Level	Transmit Dotting Pattern	-11	-10	-9	dBm0
Harmonic Distortion in 700-2900 Hz band	THD in the alternate band DPSK or FSK		-60	-50	dB
Output Bias Distortion	Transmit Dotting Pattern In ALB @ RXD		±3		%
Total Output Jitter	Random Input in ALB @ RXD	-10		+10	%
DTMF Generator					
Freq. Accuracy	Must be in V.22 mode	-0.25		+0.25	%
Output Amplitude	Low Band, V.22 mode	-10	-9	-8	dBm0
Output Amplitude	High Band, V.22 mode	-8	-7	-6	dBm0
Twist	High-Band to Low-Band, V.22 mode	1.0	2.0	3.0	dB
Long Loop Detect	With Sinusoid	-38		-28	dBm0
Dynamic Range	Refer to Performance Curves		45		dB

Note: Parameters expressed in dBm0 refer to the following definition:

0 dB loss in the Transmit path to the line.

2 dB gain in the Receive path from the line.

Refer to the Basic Box Modem diagram in the Applications section for the DAA design.

DYNAMIC CHARACTERISTICS AND TIMING (continued)

PARAMETER	CONDITION	MIN	NOM	MAX	UNIT
Call Progress Detector					
Detect Level	-3 dB points in 285 and 675 Hz	-38			dBm0
Reject Level	Test signal is a 460 Hz sinusoid			-45	dBm0
Delay Time	-70 dBm0 to -30 dBm0 STEP			40	ms
Hold Time	-30 dBm0 to -70 dBm0 STEP			40	ms
Hysteresis		2			dB
Carrier Detect					
Threshold	DPSK or FSK receive data	-48		-43	dBm0
Delay Time					
V.21		10		20	ms
V.22		15		32	ms
V.23 Forward Channel		6		12	ms
V.23 Back Channel		25		40	ms
Hold Time					
V.21		6		20	ms
V.22		10		24	ms
V.23 Forward Channel		3		8	ms
V.23 Back Channel		10		25	ms
Hysteresis		2			dB
Special Tone Detectors					
Detect Level	See definitions for TR bit D0 mode	-48		-43	dBm0
Delay Time					
2100 Hz answer tone		10		25	ms
1300 Hz calling tone		10		25	ms
390 Hz V.23 back channel mark		20		65	ms

DYNAMIC CHARACTERISTICS AND TIMING (continued)

PARAMETER	CONDITION	MIN	NOM	MAX	UNIT
Special Tone Detectors (continued)					
980 or 1650 Hz V.21 marks		10		25	ms
Hold Time					
2100 Hz answer tone		4		15	ms
1300 Hz calling tone		3		10	ms
390 Hz V.23 back channel mark		10		25	ms
980 or 1650 Hz V.21 marks		5		15	ms
Hysteresis		2			dB
Detect Freq. Range	Any Special Tone	-3		+3	%
Output Smoothing Filter					
Output load	TXA pin; FSK Single Tone out for THD = -50 dB in 0.3 to 3.4 kHz	10		 50	kΩ pF
Out of Band Energy	Frequency >12 kHz in all modes			-60	dBm0
Output Impedance	TXA pin, TXA enabled		20	50	Ω
Clock Noise	TXA pin; 76.8 kHz or 122.88 kHz in V.23 main channel		0.1	0.4	mVrms
Carrier VCO					
Capture Range	Originate or Answer	-10		+10	Hz
Capture Time	-10 Hz to +10 Hz Carrier Freq. Change Assum.		40	100	ms
Recovered Clock					
Capture Range	% of frequency center frequency (center at 1200 Hz)	-625		+625	ppm
Data Delay Time	Analog data in at RXA pin to receive data valid at RXD pin		30	50	ms

DYNAMIC CHARACTERISTICS AND TIMING (continued)

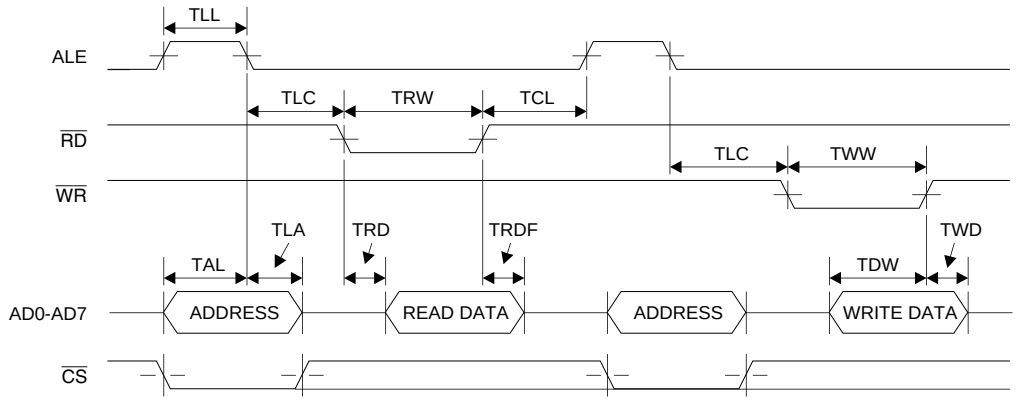
PARAMETER	CONDITION	MIN	NOM	MAX	UNIT
Guard Tone Generator					
Tone Accuracy	550 or 1800 Hz	-20		+20	Hz
Tone Level	550 Hz	-4.0	-3.0	-2.0	dB
(Below DPSK Output)	1800 Hz	-7.0	-6.0	-5.0	dB
Harmonic Distortion 700 to 2900 Hz	550 Hz			-50	dB
Timing (Refer to Timing Diagrams)					
TAL	$\overline{CS}$/Addr. setup before ALE Low	25			ns
TLA	$\overline{CS}$/Addr. hold after ALE Low	20			ns
TLC	ALE Low to $\overline{RD}$/$\overline{WR}$ Low	30			ns
TCL	$\overline{RD}$/$\overline{WR}$ Control to ALE High	-5			ns
TRD	Data out from $\overline{RD}$ Low	0		140	ns
TLL	ALE width	30			ns
TRDF	Data float after $\overline{RD}$ High	0		5	ns
TRW	$\overline{RD}$ width	200		25000	ns
TWW	$\overline{WR}$ width	140		25000	ns
TDW	Data setup before $\overline{WR}$ High	40			ns
TWD	Data hold after $\overline{WR}$ High	10			ns
TCKD	Data out after EXCLK Low			200	ns
TCKW	$\overline{WR}$ after EXCLK Low	150			ns
TDCK	Data setup before EXCLK Low	150			ns
TAC	Address setup before control*	50			ns
TCA	Address hold after control*	50			ns
TWH	Data Hold after EXCLK	20			

* Control for setup is the falling edge of $\overline{RD}$ or $\overline{WR}$.
Control for hold is the falling edge of $\overline{RD}$ or the rising edge of $\overline{WR}$.

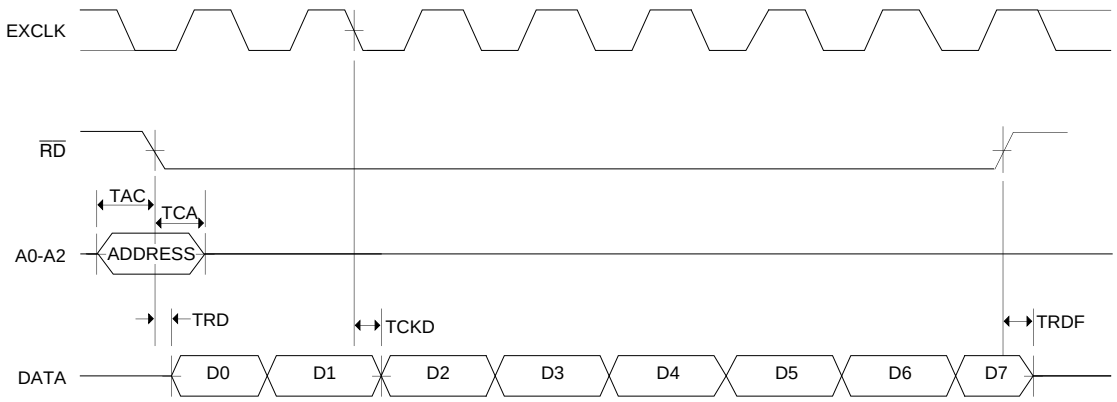
NOTE: Asserting ALE, $\overline{CS}$, and $\overline{RD}$ or $\overline{WR}$ concurrently can cause unintentional register accesses. When using non-8031 compatible processors, care must be taken to prevent this from occurring when designing the interface logic.

TIMING DIAGRAMS

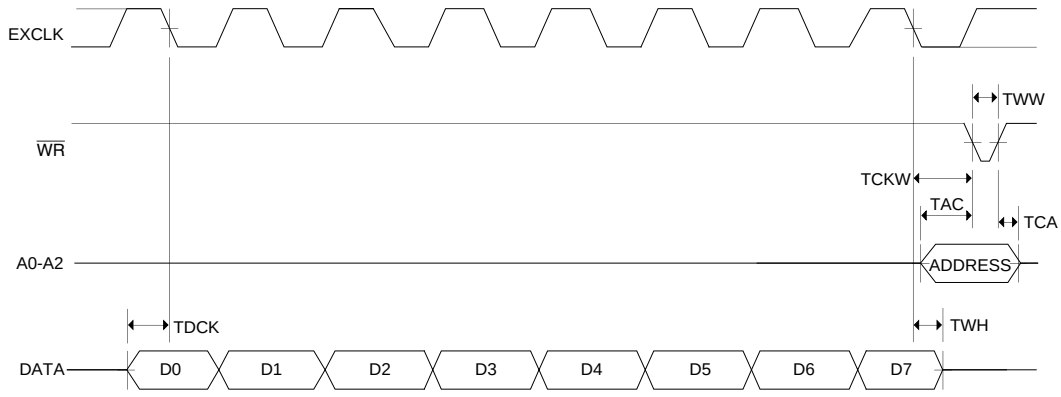
BUS TIMING DIAGRAM (PARALLEL VERSION)



READ TIMING DIAGRAM (SERIAL VERSION)



WRITE TIMING DIAGRAM (SERIAL VERSION)



APPLICATIONS INFORMATION

GENERAL CONSIDERATIONS

Figures 1 and 2 show basic circuit diagrams for K-Series modem integrated circuits. K-Series products are designed to be used in conjunction with a control processor, a UART or RS-232 serial data interface, and a DAA phone line interface to function as a typical intelligent modem. The K-Series ICs interface directly with Intel 8048 and 80C51 microprocessors for control and status monitoring purposes.Two typical DAA arrangements are shown: one for a split ±5 or ±12 volt design and one for a single 5 volt design. These diagrams are for reference only and do not represent production-ready modem designs.

K-Series devices are available with two control interface versions: one for a parallel multiplexed address/data interface, and one for a serial interface. The parallel version is intended for use with 8039/48 or 8031/51 microcontrollers from Intel or many other manufacturers. The serial interface 22-pin version can be used with other microcontrollers or in applications where only a limited number of port lines are available or the application does not lend itself to a multiplexed address/data interface. The parallel versions may also be used in the Serial mode, as explained in the data sheet pin description.

In most applications the controller will monitor the serial data for commands from the DTE and the received data for break signals from the far end modem. In this way, commands to the modem are sent over the same line as the transmitted data. In other applications the RS-232 interface handshake lines are used for modem control.

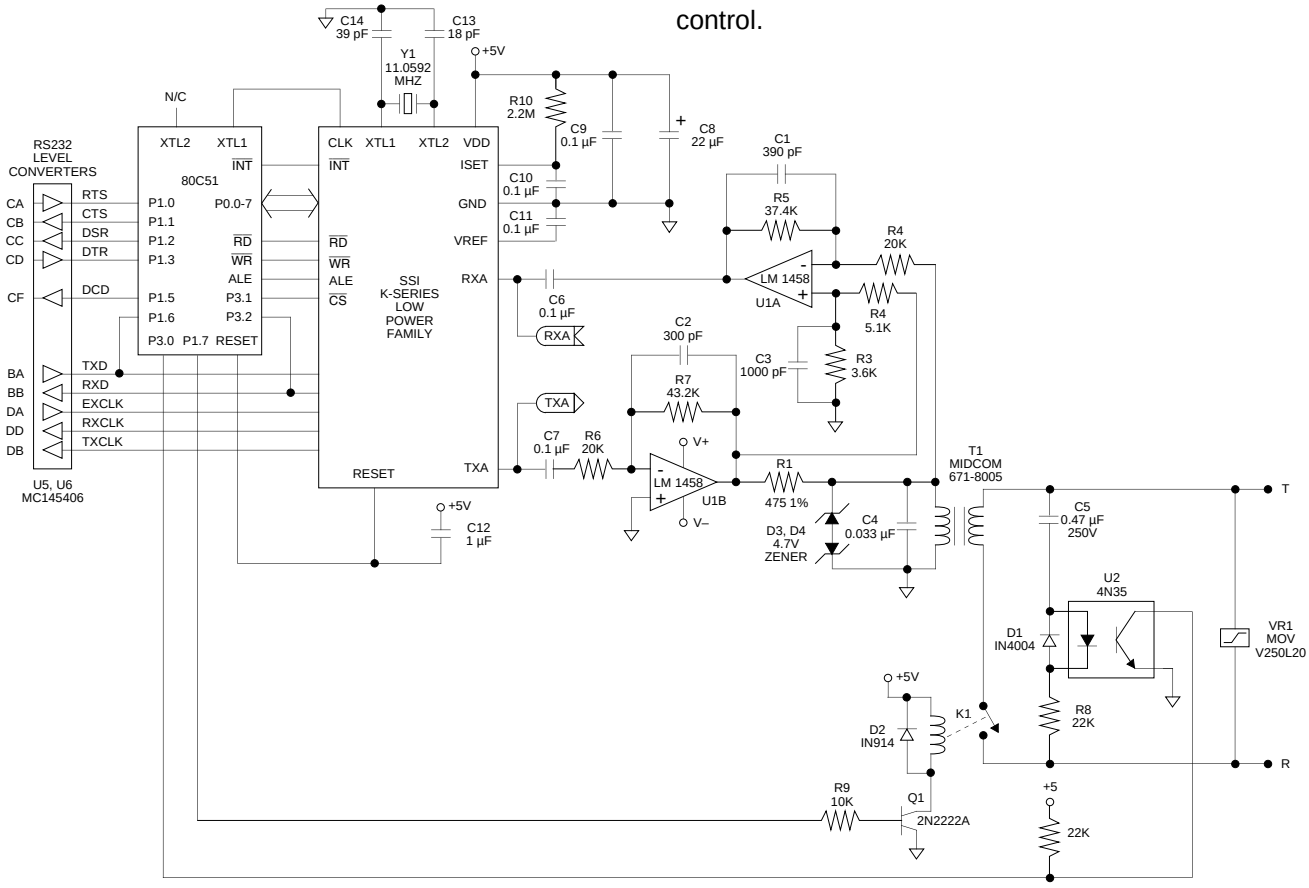


FIGURE 1: Basic Box Modem with Dual-Supply Hybrid

DIRECT ACCESS ARRANGEMENT (DAA)

The telephone line interfaces show two examples of how the "hybrid" may be implemented. The split supply design (Figure 1) is a typical two op-amp hybrid. The receive op-amp serves two purposes. It supplies gain to amplify the receive signal to the proper level for the modem's detectors and demodulator, and it removes the transmitted signal from the receive signal present at the transformer. This is done by supplying a portion of the transmitted signal to the non-inverting input of the receive op-amp at the same amplitude as the signal appearing at the transformer, making the transmit signal Common mode.

The single-supply hybrid is more complex than the dual-supply version described above, but its use eliminates the need for a second power supply. This circuit (Figure 2) uses a bridged drive to allow undistorted signals to be sent with a single 5 volt supply. Because DTMF tones utilize a higher amplitude than data, these signals will clip if a single-ended drive approach is used. The bridged driver uses an extra op-amp (U1A) to invert the signal coming from the gain setting op-amp (U1B) before sending it to the other leg of the transformer. Each op-amp then supplies half the drive signal to the transformer. The receive amplifier (U1C) picks off its signal at the junction of the impedance matching resistor and the transformer. Because the bottom leg of the transformer is being driven in one direction by U1A and the resistor is driven in the opposite direction at the same time by U1B, the junction of the transformer and resistor remains relatively constant and the receive signal is unaffected.

DESIGN CONSIDERATIONS

Silicon Systems' 1-chip modem products include all basic modem functions. This makes these devices adaptable for use in a variety of applications, and as easy to control as conventional digital bus peripherals.

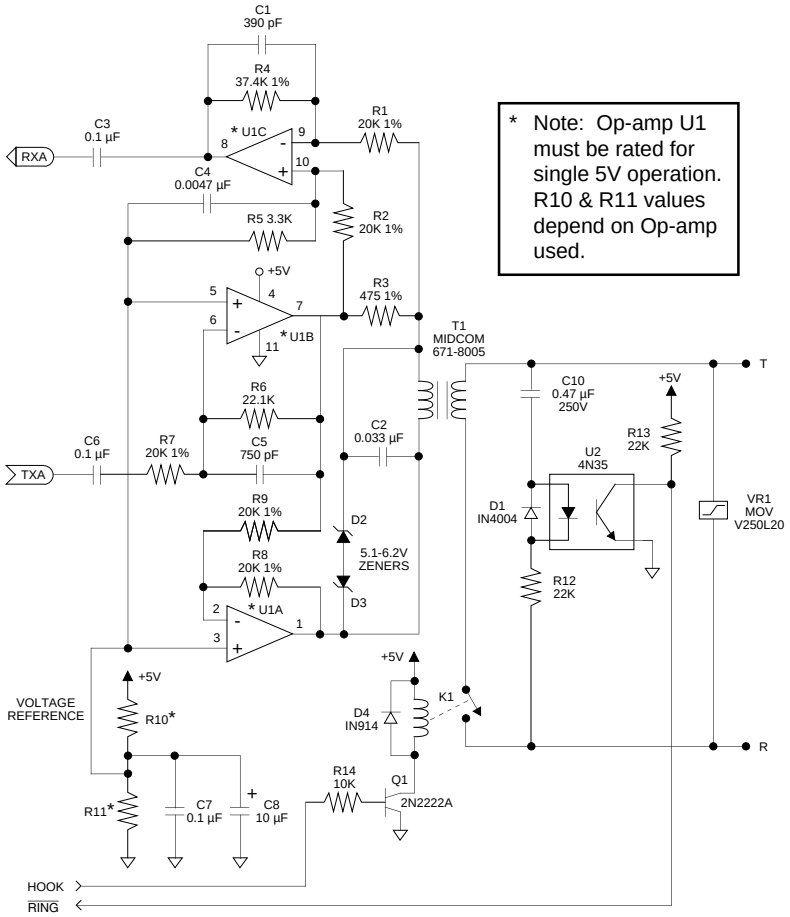


FIGURE 2: Single 5V Hybrid Version

Unlike digital logic circuitry, modem designs must properly contend with precise frequency tolerances and very low level analog signals, to ensure acceptable performance. Using good analog circuit design practices will generally result in a sound design. Following are additional recommendations which should be taken into consideration when starting new designs.

CRYSTAL OSCILLATOR

The K-Series crystal oscillator requires a Parallel mode (antiresonant) crystal which operates at 11.0592 MHz. It is important that this frequency be maintained to within ±0.01% accuracy.

In order for a Parallel mode crystal to operate correctly and to specification, it must have a load capacitor connected to the junction of each of the crystal and internal inverter connections, terminated to ground. The values of these capacitors depend primarily on the crystal's characteristics, and to a lesser degree on the internal inverter circuit. The values used affect the accuracy and start up characteristics of the oscillator.

LAYOUT CONSIDERATIONS

Good analog/digital design rules must be used to control system noise in order to obtain highest performance in modem designs. The more digital circuitry present on the PC board, the more this attention to noise control is needed. The modem should be treated as a high impedance analog device. A 22 µF electrolytic capacitor in parallel with a 0.1 µF ceramic capacitor between VDD and GND is recommended. Liberal use of ground planes and larger traces on power and ground are also highly favored. High speed digital circuits tend to generate a significant amount of EMI (Electro-Magnetic Interference) which must be minimized in order to meet regulatory agency limitations. To accomplish this, high speed digital devices should be locally bypassed, and the telephone line interface and K-Series device should be located close to each other near the area of the board where the phone line connection is accessed. To avoid problems, power supply and ground traces should be routed separately to the analog and digital functions on the board, and digital signals should not be routed near low level or high impedance analog traces. The analog and digital grounds should only connect at one point near the K-Series device ground pin to avoid ground loops. The K-Series modem IC's should have both high frequency and low frequency bypassing as close to the package as possible.

MODEM PERFORMANCE CHARACTERISTICS

The curves presented here define modem IC performance under a variety of line conditions while inducing disturbances that are typical of those encountered during data transmission on public service telephone lines. Test data was taken using an AEA Electronics' "Autotest I" modem test set and line simulator, operating under computer control. All tests were run full-duplex, using a Concord Data Systems 224 as the reference modem. A 511 pseudo-random-bit pattern was used for each data point. Noise was C-message weighted and all signal-to-noise (S/N) ratios reflect total power measurements similar to the CCITT V.56 measurement specification. The individual tests are defined as follows.

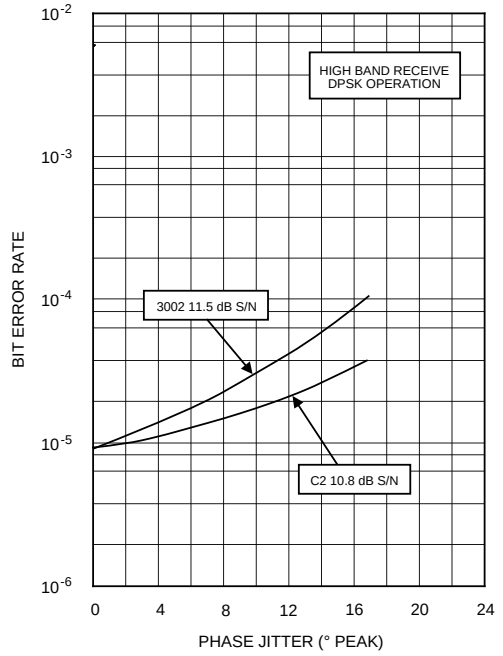
BER vs. S/N

This test measures the ability of the modem to operate over noisy lines with a minimum of data-transfer errors. Since some noise is generated in the best of dial-up lines, the modem must operate with the lowest S/N ratio possible. Better modem performance is indicated by test curves that are closest to the BER axis. A narrow spread between curves representing the four line parameters indicates minimal variation in performance while operating over a range of aberrant operating conditions. Typically, a DPSK modem will exhibit better BER-performance test curves receiving in the low band than in the high band.

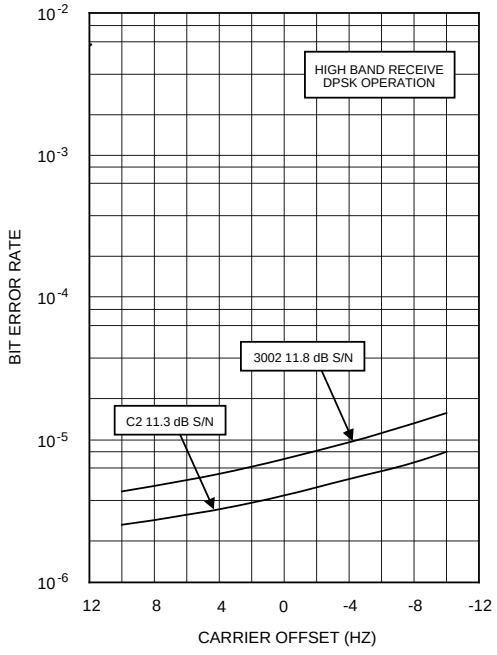
BER vs. Receive Level

This test measures the dynamic range of the modem. Because signal levels vary widely over dial-up lines, the widest possible dynamic range is desirable. The minimum Bell specification calls for 36 dB of dynamic range. S/N ratios are held constant at the indicated values while the receive level is lowered from a very high to very low signal levels. The width of the "bowl" of these curves, taken at the BER point, is the measure of dynamic range.

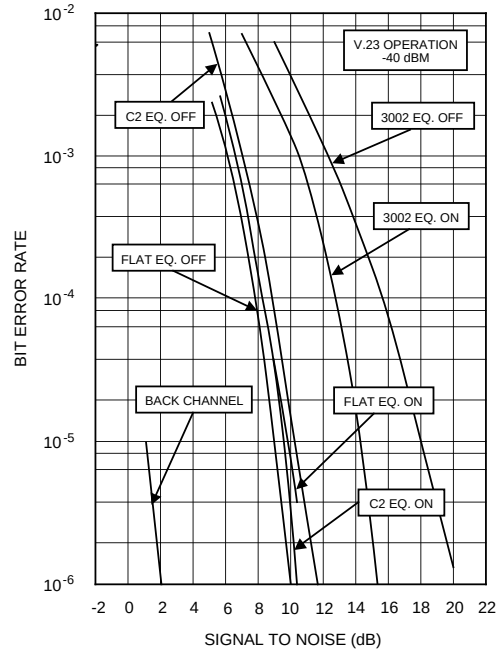
***SSI 73K322L**
BER vs PHASE JITTER



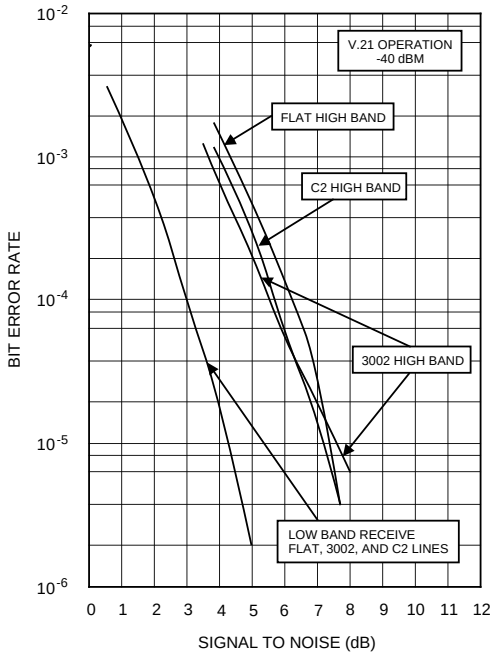
SSI 73K322L
BER vs CARRIER OFFSET



***SSI 73K322L**
BER vs S/N (V.23 ONLY)

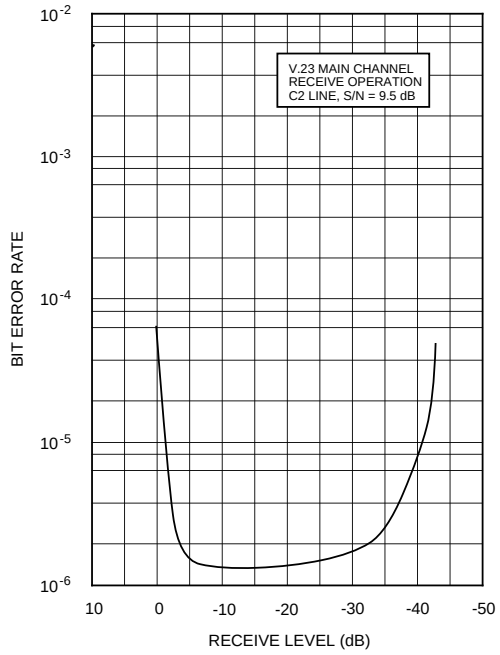


SSI 73K322L
BER vs SIGNAL TO NOISE

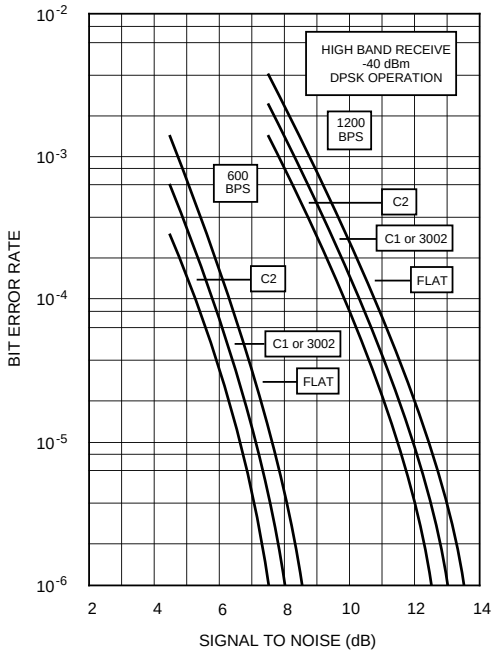


***** = "EQ On" Indicates bit CR1 D4 is set for additional phase equalization.

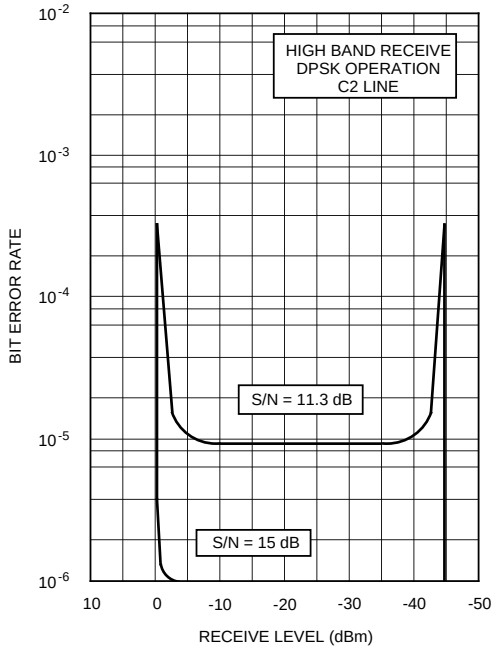
***SSI 73K322**
BER vs RECEVE LEVEL (V.23)



***SSI 73K322L**
BER vs SIGNAL TO NOISE



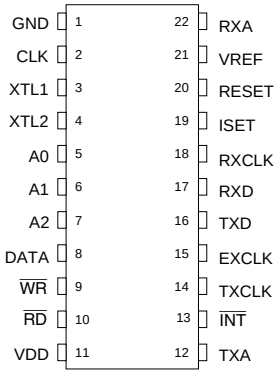
***SSI 73K322**
BER vs RECEVE LEVEL



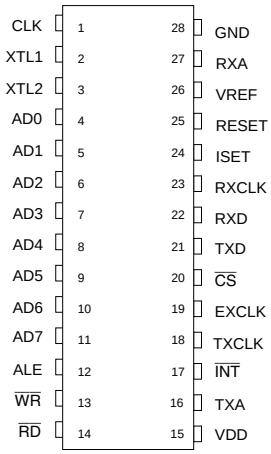
***** = "EQ On" Indicates bit CR1 D4 is set for additional phase equalization.

PACKAGE PIN DESIGNATIONS

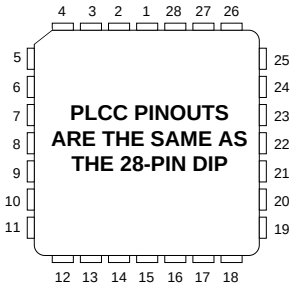
(Top View)



400-Mil
22-Pin DIP



600-Mil
28-Pin DIP



28-Pin
PLCC

CAUTION: Use handling procedures necessary for a static sensitive component.

ORDERING INFORMATION

PART DESCRIPTION	ORDER NO.	PKG. MARK
SSI 73K322L 28-Pin 5V Supply Plastic Dual-In-Line	73K322L-IP	73K322L-IP
Plastic Leaded Chip Carrier	73K322L-IH	73K322L-IH
SSI 73K322L 22-Pin 5V Supply Plastic Dual-In-Line	73K322SL-IP	73K322SL-IP

Silicon Systems, Inc., 14351 Myford Road, Tustin, CA 92680-7022, (714) 573-6000, FAX: (714) 573-6914

SSI 73K324L

CCITT V.22bis, V.22, V.21, V.23, Bell 212A Single-Chip Modem

January 1996

DESCRIPTION

The SSI 73K324L is a highly integrated single-chip modem IC which provides the functions needed to design a Quad-mode CCITT and Bell 212A compatible modem capable of operation over dial-up lines. The SSI 73K324L adds V.23 capability to the CCITT modes of Silicon Systems' 73K224 one-chip modem, allowing a one-chip implementation in designs intended for European markets which require this added Modulation mode. The SSI 73K324L offers excellent performance and a high level of functional integration in a single IC. The device supports V.22bis, V.22, Bell 212A, V.21, and V.23 operating modes, allowing both synchronous and asynchronous operation as defined by the appropriate standard.

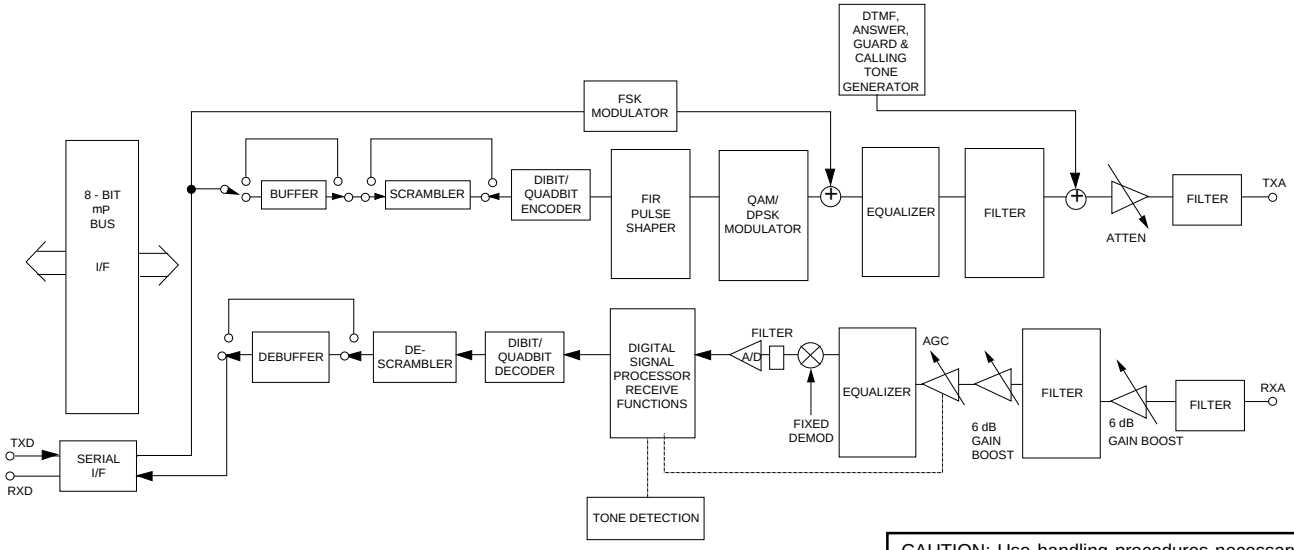
The SSI 73K324L is designed to appear to the Systems Engineer as a microprocessor peripheral, and will easily interface with popular one-chip microcontrollers (80C51 typical) for control of modem functions through its 8-bit multiplexed address/data bus. A serial control bus is available for applications not requiring a parallel interface. An optional package with only the serial control bus is also available. Data communications occurs through a separate serial port.

(continued)

FEATURES

- **One chip Multi-mode CCITT V.22bis, V.22, V.21, V.23 and Bell 212A compatible modem data pump**
- **FSK (75, 300, 1200 bit/s), DPSK (600, 1200 bit/s), or QAM (2400 bit/s) encoding**
- **Pin and software compatible with other SSI K-Series family one-chip modems**
- **Interfaces directly with standard microprocessors (8048, 80C51 typical)**
- **Serial and parallel microprocessor bus for control**
- **Selectable asynch/synch with internal buffer/ debuffer and scrambler/descrambler functions**
- **All synchronous (internal, external, slave) and Asynchronous Operating modes**
- **Adaptive equalization for optimum performance over all lines**
- **Programmable transmit attenuation (16 dB, 1 dB steps), and selectable receive boost (+18 dB)**
- **Call progress, carrier, answer tone, unscrambled mark, S1, and signal quality monitors**
- **DTMF, answer, calling, SCT and guard tone generators**
- **Test modes available: ALB, DL, RDL; Mark, Space and Alternating bit pattern generators**
- **CMOS technology for low power consumption**
- **4-wire full duplex operation in all modes**

BLOCK DIAGRAM



CAUTION: Use handling procedures necessary for a static sensitive component.

DESCRIPTION (continued)

The SSI 73K324L offers full hardware and software compatibility with other products in Silicon Systems' K-Series family of single-chip modems, allowing system upgrades with a single component change. The SSI 73K324L is ideal for use in free-standing or integral system modem products where full-duplex 2400 bit/s operation with Alternate mode capability is required. Its high functionality, low power consumption, and efficient packaging simplify design requirements and increase system reliability. A complete modem requires only the addition of the phone line interface, a control microprocessor, and RS-232 level converters for a typical system.

The SSI 73K324L is designed to provide a complete V.22bis, V.22, Bell 212A, V.21, and V.23 compatible modem on a chip. Many functions were included to simplify implementation in typical modem designs. In addition to the basic 2400 bit/s QAM, 1200/600 bit/s DPSK and 1200/300/75 bit/s FSK modulator/demodulator sections, the device also includes synch/asynch buffering, DTMF, answer, soft carrier, guard, and calling tone generator capabilities. Handshake pattern detectors simplify control of connect sequences, and precise tone detectors allow accurate detection of call progress, answer, calling, and soft carrier turn off tones. All Operating modes defined by the incorporated standards are included, and Test modes are provided. Most functions are selectable as options, and logical defaults are provided. The device can be directly interfaced to a microprocessor via its 8-bit multiplexed address/data bus for control and status monitoring. Data communications takes place through a separate serial port. Data may also be sent and received through the control registers. This simplifies designs requiring speed buffering, error control and compression.

FUNCTIONAL DESCRIPTION

QAM MODULATOR/DEMODULATOR

The SSI 73K324L encodes incoming data into quadbits represented by 16 possible signal points with specific phase and amplitude levels. The baseband signal is then filtered to reduce intersymbol interference on the bandlimited telephone network. The modulator transmits this encoded data using either a 1200 Hz (Originate mode) or 2400 Hz (Answer mode) carrier. The demodulator, although more complex, essentially reverses this procedure while also recovering the data clock from the incoming signal. Adaptive equalization corrects for varying line conditions by automatically changing filter parameters to compensate for line characteristics.

DPSK MODULATOR/DEMODULATOR

The SSI 73K324L modulates a serial bit stream into di-bit pairs that are represented by four possible phase shifts as prescribed by the Bell 212A/V.22 standards. The baseband signal is then filtered to reduce intersymbol interference on the bandlimited 2-wire PSTN line. Transmission occurs on either a 1200 Hz (Originate mode) or 2400 Hz carrier (Answer mode). Demodulation is the reverse of the modulation process, with the incoming analog signal eventually decoded into di-bits and converted back to a serial bit stream. The demodulator also recovers the clock which was encoded into the analog signal during modulation. Demodulation occurs using either a 1200 Hz carrier (Answer mode or ALB Originate mode) or a 2400 Hz carrier (Originate mode or ALB Answer mode). The SSI 73K324L use a phase locked loop coherent demodulation technique that offers excellent performance. Adaptive equalization is also used in DPSK modes for optimium operation with varying lines.

FSK MODULATOR/DEMODULATOR

The FSK modulator/demodulator produces a frequency modulated analog output signal using two discrete frequencies to represent the binary data. V.21 frequencies of 980 and 1180 Hz (originate mark and space), or 1650 and 1850 Hz (answer mark and space) are used in V.21 mode. V.23 mode uses 1300 and 2100 Hz for the main channel or 390 and 450 Hz for the back channel. Demodulation involves detecting the received frequencies and decoding them into the appropriate binary value. The rate converter and scrambler/descrambler are automatically bypassed in the FSK modes.

PASSBAND FILTERS AND EQUALIZERS

High and low band filters are included to shape the amplitude and phase response of the transmit and receive signals and to provide compromise delay equalization as well as rejection of out-of-band signals. The transmit signal filtering corresponds to a $\sqrt{75\%}$ raised cosine frequency response characteristic.

ASYNCHRONOUS MODE

The Asynchronous mode is used for communication with asynchronous terminals which may transfer data at 600, 1200, or 2400 bit/s +1%, -2.5% even though the modem's output is limited to the nominal bit rate ±0.01% in DPSK and QAM modes. When transmitting in this mode the serial data on the TxD input is passed through a rate converter which inserts or deletes stop bits in the serial bit stream in order to output a signal that is the nominal bit rate ±0.01%. This signal is then routed to a data scrambler and into the analog modulator where di-bit or quad-bit encoding results in the output signal. Both the rate converter and scrambler can be bypassed for handshaking and synchronous operation as selected. Received data is processed in a similar fashion except that the rate converter now acts to reinsert any deleted stop bits and output data to the terminal at no greater than the bit rate plus 1%. An incoming break signal (low through two characters) will be recognized and passed through without incorrectly inserting a stop bit.

The SYNC/ASYNC converter has an extended Overspeed mode which allows selection of an output speed range of either +1% or +2.3%. In the extended Overspeed mode, some stop bits are output at 7/8 the normal width.

Both the SYNC/ASYNC rate converter and the data descrambler are automatically bypassed in the FSK modes.

SYNCHRONOUS MODE

Synchronous operation is possible only in the QAM or DPSK modes. Operation is similar to that of the Asynchronous mode except that data must be synchronized to a clock and no variation in data transfer rate is allowable. Serial input data appearing at TXD must be valid on the rising edge of TXCLK.

TXCLK is an internally derived 1200 or 2400 Hz signal in Internal mode and is connected internally to the RXCLK pin in Slave mode. Receive data at the RXD pin is clocked out on the falling edge of RXCLK. The asynch/synch converter is bypassed when Synchronous mode is selected and data is transmitted out at essentially the same rate as it is input.

PARALLEL CONTROL INTERFACE

Eight 8-bit registers are provided for control, option select, and status monitoring. These registers are addressed with the AD0, AD1, and AD2 multiplexed address lines (latched by ALE) and appear to a control microprocessor as seven consecutive memory locations. Six contol registers are read/write. The detect and ID registers are read only and cannot be modified except by modem response to monitored parameters.

SERIAL CONTROL INTERFACE

The Serial Command mode allows access to the SSI 73K324L control and status registers via a serial control port. In this mode the A0, A1, and A2 lines provide register addresses for data passed through the DATA pin under control of the $\overline{RD}$ and $\overline{WR}$ lines. A read operation is initiated when the $\overline{RD}$ line is taken low. The next eight cycles of EXCLK will then transfer out eight bits of the selected addresss location LSB first. A write takes place by shifting in eight bits of data LSB first for eight consectuive cycles of EXCLK. $\overline{WR}$ is then pulsed low and data transfer into the selected register occurs on the rising edge of $\overline{WR}$.

TONE GENERATOR

The DTMF generator controls the sending of the sixteen standard DTMF tone pairs. The tone pair sent is determined by selecting TRANSMIT DTMF (bit D4) and the 4 DTMF bits (D0-D3) of the TONE register. Transmission of DTMF tones from TXA is gated by the TRANSMIT ENABLE bit of CR0 (bit D1) as with all other analog signals.

FULL DUPLEX OPERATION

Four-wire full duplex operation is allowed in all modes. This feature allows transmission and reception in the same band for four wire applications only.

PIN DESCRIPTION

POWER

NAME	TYPE	DESCRIPTION
GND	I	System Ground.
VDD	I	Power supply input, 5V -5% +10%. Bypass with 0.22 µF and 22 µF capacitors to GND.
VREF	O	An internally generated reference voltage. Bypass with 0.22 µF capacitor to GND.
ISET	I	Chip current reference. Sets bias current for op-amps. The chip current is set by connecting this pin to VDD through a 2 MΩ resistor. Iset should be bypassed to GND with a 0.22 µF capacitor.

PARALLEL MICROPROCESSOR INTERFACE

ALE	I	Address latch enable. The falling edge of ALE latches the address on AD0-AD2 and the chip select on $\overline{CS}$.
AD0-AD7	I/O / Tristate	Address/data bus.These bidirectional tri-state multi-plexed lines carry information to and from the internal registers.
$\overline{CS}$	I	Chip select. A low on this pin allows a read cycle or a write cycle to occur. AD0-AD7 will not be driven and no registers will be written if $\overline{CS}$ (latched) is not active. $\overline{CS}$ is latched on the falling edge of ALE.
CLK	O	Output clock. This pin is selectable under processor control to be either the crystal frequency (for use as a processor clock) or 16 x the data rate for use as a baud rate clock in QAM/DPSK modes only. The pin defaults to the crystal frequency on reset.
$\overline{INT}$	O	Interrupt. This open drain weak pullup, output signal is used to inform the processor that a detect flag has occurred. The processor must then read the detect register to determine which detect triggered the interrupt. $\overline{INT}$ will stay active until the processor reads the detect register or does a full reset.
$\overline{RD}$	I	Read. A low requests a read of the SSI 73K324L internal registers. Data cannot be output unless both $\overline{RD}$ and the latched $\overline{CS}$ are active or low.
RESET	I	Reset. An active high signal on this pin will put the chip into an inactive state. All control register bits (CR0, CR1, CR2, CR3, Tone) will be reset. The output of the CLK pin will be set to the crystal frequency. An internal pull down resistor permits power on reset using a capacitor to VDD.
$\overline{WR}$	I	Write. A low on this informs the SSI 73K324L that data is available on AD0-AD7 for writing into an internal register. Data is latched on the rising edge of $\overline{WR}$. No data is written unless both $\overline{WR}$ and the latched $\overline{CS}$ are low.

Note: The Serial Control mode is provided in the parallel versions by tying ALE high and $\overline{CS}$ low. In this configuration AD7 becomes DATA and AD0, AD1 and AD2 become A0, A1 and A2, respectively.

RS-232 INTERFACE

NAME	TYPE	DESCRIPTION
EXCLK	I	External Clock. This signal is used in synchronous transmission when the external timing option has been selected. In the External Timing mode the rising edge of EXCLK is used to strobe synchronous transmit data available on the TXD pin. Also used for serial control interface.
RXCLK	O/Tristate	Receive Clock Tri-statable. The falling edge of this clock output is coincident with the transitions in the serial received DPSK/QAM data output. The rising edge of RXCLK can be used to latch the valid output data. RXCLK will be valid as long as a carrier is present. In V.23 or V.21 mode a clock which is 16 x 1200/ 75 or 16 x 300 Hz data rate is output, respectively.
RXD	O/ Weak Pull-up	Received Data Output. Serial receive data is available on this pin. The data is always valid on the rising edge of RXCLK when in Synchronous mode. RXD will output constant marks if no carrier is detected.
TXCLK	O/Tristate	Transmit Clock Tri-statable. This signal is used in synchronous DPSK/QAM transmission to latch serial input data on the TXD pin. Data must be provided so that valid data is available on the rising edge of the TXCLK. The transmit clock is derived from different sources depending upon the Synchronization mode selection. In Internal Mode the clock is generated internally (2400 Hz for QAM, 1200 Hz for DPSK or 600 Hz for half-speed DPSK). In External Mode TXCLK is phase locked to the EXCLK pin. In Slave Mode TXCLK is phase locked to the RXCLK pin. TXCLK is always active. In V.23 or V.21 mode the output is a 16 x 1200/75 or 16 x 300 Hz clock, respectively.
TXD	I	Transmit Data Input. Serial data for transmission is input on this pin. In Synchronous modes, the data must be valid on the rising edge of the TXCLK clock. In Asynchronous modes (2400/1200/600 bit/s, or 75/300 baud) no clocking is necessary. DPSK/QAM data must be +1%, -2.5% or +2.3%, -2.5 % in Extended Overspeed mode.

ANALOG INTERFACE

RXA	I	Received modulated analog signal input from the phone line.
TXA	O	Transmit analog output to the phone line.
XTL1	I	These pins are for the internal crystal oscillator requiring a 11.0592 MHz Parallel mode crystal. Two capacitors from these pins to ground are also required for proper crystal operation. Consult crystal manufacturer for proper values. XTL2 can also be driven from an external clock.
XTL2	I/O	

PIN DESCRIPTION (continued)

SERIAL MICROPROCESSOR INTERFACE

NAME	TYPE	DESCRIPTION
A0-A2	I	Register Address Selection. These lines carry register addresses and should be valid during any read or write operation.
DATA	I/O	Serial Control Data. Data for a read/write operation is clocked in or out on the falling edge of the EXCLK pin. The direction of data flow is controlled by the $\overline{RD}$ pin. $\overline{RD}$ low outputs data. $\overline{RD}$ high inputs data.
$\overline{RD}$	I	Read. A low on this input informs the SSI 73K324L that data or status information is being read by the processor. The falling edge of the $\overline{RD}$ signal will initiate a read from the addressed register. The $\overline{RD}$ signal must continue for eight falling edges of EXCLK in order to read all eight bits of the referenced register. Read data is provided LSB first. Data will not be output unless the $\overline{RD}$ signal is active.
$\overline{WR}$	I	Write. A low on this input informs the SSI 73K324L that data or status information has been shifted in through the DATA pin and is available for writing to an internal register. The normal procedure for a write is to shift in data LSB first on the DATA pin for eight consecutive falling edges of EXCLK and then to pulse $\overline{WR}$ low. Data is written on the rising edge of $\overline{WR}$.

Note: In the serial, 22-pin version, the pins AD0-AD7, ALE and $\overline{CS}$ are removed and replaced with the pins; A0, A1, A2, DATA, and EXCLK. Also, the $\overline{RD}$ and $\overline{WR}$ controls are used differently.

REGISTER DESCRIPTIONS

Eight 8-bit internal registers are accessible for control and status monitoring. The registers are accessed in read or write operations by addressing the A0, A1 and A2 address lines in Serial mode, or the AD0, AD1 and AD2 lines in Parallel mode. The address lines are latched by ALE. Register CR0 controls the method by which data is transferred over the phone line. CR1 controls the interface between the microprocessor and the SSI 73K324L internal state. DR is a detect register which provides an indication of monitored modem status conditions. TR, the tone control register, controls the DTMF generator, answer, guard tones, SCT, calling tone, and RXD output gate used in the modem initial connect sequence. CR2 is the primary DSP control interface and CR3 controls transmit attenuation and receive gain adjustments. All registers are read/write except for DR and ID which are read only. Register control and status bits are identified below:

REGISTER BIT SUMMARY

		ADDRESS	DATA BIT NUMBER							
REGISTER		AD - A0	D7	D6	D5	D4	D3	D2	D1	D0
CONTROL REGISTER 0	CR0	000	MODULATION OPTION	MODULATION TYPE 1	MODULATION TYPE 0	TRANSMIT MODE 2	TRANSMIT MODE 1	TRANSMIT MODE 0	TRANSMIT ENABLE	ANSWER/ ORIGINATE
CONTROL REGISTER 1	CR1	001	TRANSMIT PATTERN 1	TRANSMIT PATTERN 0	ENABLE DETECT INTERRUPT	BYPASS SCRAMBLER/ ADD PH. EQ. (V.23)	CLK CONTROL	RESET	TEST MODE 1	TEST MODE 0
DETECT REGISTER	DR	010	RECEIVE LEVEL	PATTERN S1 DET	RECEIVE DATA	UNSCR. MARK DETECT	CARRIER DETECT	SPECIAL TONE DETECT	CALL PROGRESS DETECT	SIGNAL QUALITY
TONE CONTROL REGISTER	TR	011	RXD OUTPUT CONTROL	TRANSMIT GUARD TONE/ SCT/CALLING TONE	TRANSMIT ANSWER TONE	TRANSMIT DTMF	DTMF3	DTMF2/ 4 WIRE FDX	DTMF1/ OVERSPEED	DTMF0/GUARD/ ANSWER/ CALLING/SCT
CONTROL REGISTER 2	CR2	100	0	SPECIAL REGISTER ACCESS	CALL INITIALIZE	TRANSMIT S1	16 WAY	RESET DSP	TRAIN INHIBIT	EQUALIZER ENABLE
CONTROL REGISTER 3	CR3	101	TXDALT	TRISTATE TX/RXCLK	0	RECEIVE GAIN BOOST	TRANSMIT ATTEN. 3	TRANSMIT ATTEN. 2	TRANSMIT ATTEN. 1	TRANSMIT ATTEN. 0
SPECIAL REGISTER	SR	101	0	TX BAUD CLOCK	RX UNSCR. DATA	0	TXD SOURCE	SQ SELECT 1	SQ SELECT 0	0
ID REGISTER	ID	110	1	1	1	0	X	X	X	X

NOTE: When a register containing reserved control bits is written into, the reserved bits must be programmed as 0's.

X = Undefined, mask in software.

REGISTER ADDRESS TABLE

REGISTER	ADDRESS AD2 - AD0	DATA BIT NUMBER D7	D6	D5	D4	D3	D2	D1	D0
CONTROL REGISTER 0 CR0	000	MODULATION OPTION	MODULATION TYPE 1	MODULATION TYPE 0	TRANSMIT MODE 2	TRANSMIT MODE 1	TRANSMIT MODE 0	TRANSMIT ENABLE	ANSWER/ ORIGINATE
		QAM: 0=2400 BIT/S DPSK: 0=1200 BIT/S 1=600 BIT/S FSK: 0=V.23 1=V.21	10=QAM 00=DPSK 01=FSK	0000=PWR DOWN 0001=INT SYNCH 0010=EXT SYNCH 0011=SLAVE SYNCH 0100=ASYCH 8 BITS/CHAR 0101=ASYCH 9 BITS/CHAR 0110=ASYCH 10 BITS/CHAR 0111=ASYCH 11 BITS/CHAR 1X00=FSK				0=DISABLE TXA OUTPUT 1=ENABLE TXA OUTPUT	0=ANSWER 1=ORIGINATE in V.23 0=BC xmit 1=MC xmit
CONTROL REGISTER 1 CR1	001	TRANSMIT PATTERN 1	TRANSMIT PATTERN 0	ENABLE DETECT INTERRUPT	BYPASS SCRAMBLER/ ADD PH. EQ. (V.23)	CLK CONTROL	RESET	TEST MODE 1	TEST MODE 0
		00=TX DATA 01=TX ALTERNATE 10=TX MARK 11=TX SPACE		0=OFF 1=ON	0=NORMAL 1=BYPASS SCRAMBLER	0=XTAL 1=16 X DATA RATE OUTPUT AT CLK PIN IN QAM/DPSK MODE ONLY	0=NORMAL 1=RESET	00=NORMAL 01=ANALOG LOOPBACK 10=REMOTE DIGITAL LOOPBACK 11=LOCAL DIGITAL LOOPBACK	
DETECT REGISTER DR	010	RECEIVE LEVEL INDICATOR	S1 PATTERN DETECT	RECEIVE DATA	UNSCR. MARKS DETECT	CARRIER DETECT	SPECIAL TONE DETECT	CP TONE DETECT	SIGNAL QUALITY INDICATOR
		0=SIGNAL BELOW THRESHOLD 1=ABOVE THRESHOLD	0=NOT PRESENT 1=PATTERN FOUND	OUTPUTS RECEIVED DATA STREAM		0=CONDITION NOT DETECTED 1=CONDITION DETECTED			0=GOOD 1=BAD
TONE CONTROL REGISTER TR	011	RXD OUTPUT CONTROL	TRANSMIT GUARD/ CALLING/ SCT TONE	TRANSMIT ANSWER TONE	TRANSMIT DTMF	DTMF3	DTMF2/ 4 WIRE FDX	DTMF1/ OVERSPEED	DTMF0/ GUARD/ ANSWER/ CALLING/SCT
		RXD PIN 0=NORMAL 1=TRI-STATE	0=OFF 1=ON	0=OFF 1=ON	1=TX DTMF	4 BIT CODE FOR 1 OF 16 DUAL TONE COMBINATIONS	0=NORMAL OPERATION 1=ALLOWS V.23 FULL DUPLEX OPERATION		GUARD: 0 - 1800 HZ 1 - 550 HZ ANSWER: 0 - 2225 HZ 1 - 2100 HZ CALLING: 0 - 1300 HZ SCT: 1 - 900 HZ
CONTROL REGISTER 2 CR2	100	MUST BE 0	SPECIAL REGISTER ACCESS	CALL INITIALIZE	TRANSMIT S1	16 WAY	$\overline{\text{RESET}}$ DSP	TRAIN INHIBIT	EQUALIZER ENABLE
			0=ACCESS CR3 1=ACCESS SPECIAL REGISTER	0=DSP IN DEMOD MODE 1=DSP IN CALL PROGRESS MODE	0=NORMAL DOTTING 1=S1	0=RX=TX 1=RX=16 WAY	0=DSP INACTIVE 1=DSP ACTIVE	0=ADAPT EQ ACTIVE 1=ADAPT EQ FROZEN	0=ADAPT EQ IN INIT 1=ADAPT EQ OK TO ADAPT
CONTROL REGISTER 3 CR3	101	TXDALT	TRISTATE TX/RXCLK	0	RECEIVE GAIN BOOST	TRANSMIT ATTEN. 3	TRANSMIT ATTEN. 2	TRANSMIT ATTEN. 1	TRANSMIT ATTEN. 0
		ALTERNATE TRANSMIT DATA SOURCE	0=CLOCK DRIVEN 1=CLOCK TRISTATE		0=NO BOOST 1=18 dB BOOST	0000-1111, SETS TRANSMIT ATTENUATOR 16 dB RANGE DEFAULT=0100 ≈ -10 dbM0			
SPECIAL REGISTER SR	101	0	TX BAUD CLOCK	RX UNSCR. DATA	0	TXD SOURCE	SQ SELECT1	SQ SELECT0	0
			OUTPUTS TXBAUD CLOCK	OUTPUTS UNSCR. DATA		0=TXD PIN 1=TX DATA CR3-D7	00= 10^{-5} BER 01= 10^{-6} BER 10= 10^{-4} BER 11= 10^{-3} BER		
ID REGISTER 10	110	1	1	1	0	X	X	X	X

00XX=73K212L, 322L, 321L
01XX=73K221L, 302L
10XX=73K222L
1100=73K224L
1110=73K324L

0 = Only write zero to these locations

x = Undefined-mask in software

CONTROL REGISTER 0

	D7	D6	D5	D4	D3	D2	D1	D0
CR0 000	MODUL. OPTION	MODUL. TYPE 1	MODUL. TYPE 0	TRANSMIT MODE 2	TRANSMIT MODE 1	TRANSMIT MODE 0	TRANSMIT ENABLE	ANSWER/ ORIGINATE

BIT NO.	NAME	CONDITION	DESCRIPTION
D0	Answer/ Originate	0	Selects Answer mode (transmit in high band, receive in low band) or in V.23 HDX mode, receive at 1200 bit/s and transmit at 75 bit/s.
		1	Selects Originate mode (transmit in low band,receive in high band) or in V.23 HDX mode, receive at 75 bit/s and transmit at 1200 bit/s.
			Note: This bit works with Tone Register bits D0 and D6 to program special tones detected in the Detect Register. See Detect and Tone Registers.
D1	Transmit Enable	0	Disables transmit output at TXA.
		1	Enables transmit output at TXA.
			Note: Transmit Enable must be set to 1 to allow activation of Answer Tone, DTMF, or Carrier.
D5, D4, D3, D2	Transmit Mode	D5 D4 D3 D2	
		0 0 0 0	Selects Power Down mode. All functions disabled except digital interface.
		0 0 0 1	Internal Synchronous mode. In this mode TXCLK is an internally derived 600, 1200 or 2400 Hz signal. Serial input data appearing at TXD must be valid on the rising edge of TXCLK. Receive data is clocked out of RXD on the falling edge of RXCLK.
		0 0 1 0	External Synchronous mode. Operation is identical to internal synchronous, but TXCLK is connected internally to EXCLK pin, and a 600, 1200 or 2400 Hz clock must be supplied externally.
		0 0 1 1	Slave Synchronous mode. Same operation as other Synchronous modes. TXCLK is connected internally to the RXCLK pin in this mode.
		0 1 0 0	Selects Asynchronous mode - 8 bits/character (1 start bit, 6 data bits, 1 stop bit).
		0 1 0 1	Selects Asynchronous mode - 9 bits/character (1 start bit, 7 data bits, 1 stop bit).
		0 1 1 0	Selects Asynchronous mode - 10 bits/character (1 start bit, 8 data bits, 1 stop bit).
		0 1 1 1	Selects Asynchronous mode - 11 bits/character (1 start bit, 8 data bits, Parity and/or 1 or 2 stop bits).
		1 X 0 0	Selects FSK operation.

CONTROL REGISTER 0 (continued)

BIT NO.	NAME	CONDITION	DESCRIPTION
D6,D5	Modulation Type	D6 D5	
		1 0	QAM
		0 0	DPSK
		0 1	FSK
D7	Modulation Option	0	QAM selects 2400 bit/s. DPSK selects 1200 bit/s. FSK selects V.23 mode.
		1	DPSK selects 600 bit/s. FSK selects V.21 mode.

CONTROL REGISTER 1

	D7	D6	D5	D4	D3	D2	D1	D0
CR1 001	TRANSMIT PATTERN 1	TRANSMIT PATTERN 0	ENABLE DETECT INT.	BYPASS SCRAMB/ ADD PH.EQ	CLK CONTROL	RESET	TEST MODE 1	TEST MODE 0

BIT NO.	NAME	CONDITION	DESCRIPTION
D1, D0	Test Mode	D1 D0	
		0 0	Selects Normal Operating mode.
		0 1	Analog Loopback mode. Loops the transmitted analog signal back to the receiver, and causes the receiver to use the same carrier frequency as the transmitter. To squelch the TXA pin, transmit enable bit must be low. Tone Register bit D2 must be zero.
		1 0	Selects remote digital loopback. Received data is looped back to transmit data internally, and RXD is forced to a mark. Data on TXD is ignored.
		1 1	Selects local digital loopback. Internally loops TXD back to RXD and continues to transmit data carrrier at TXA pin.
D2	Reset	0	Selects normal operation.
		1	Resets modem to power down state. All control register bits (CR0, CR1, CR2, CR3 and Tone) are reset to zero except CR3 bit D2. The output of the clock pin will be set to the crystal frequency.
D3	CLK Control (Clock Control)	0	Selects 11.0592 MHz crystal echo output at CLK pin.
		1	Selects 16 X the data rate output at CLK pin in QAM and DPSK only.

CONTROL REGISTER 1 (continued)

	D7	D6	D5	D4	D3	D2	D1	D0
CR1 001	TRANSMIT PATTERN 1	TRANSMIT PATTERN 0	ENABLE DETECT INT.	BYPASS SCRAMB/ ADD PH.EQ.	CLK CONTROL	RESET	TEST MODE 1	TEST MODE 0

BIT NO.	NAME	CONDITION	DESCRIPTION
D4	Bypass Scrambler/ Add Ph. Eq.	0	Selects normal operation. DPSK and QAM data is passed through scrambler.
		1	Selects Scrambler Bypass. DPSK and QAM data is routed around scrambler in the transmit path. In the V.23 mode, additional phase equalization is added to the main channel filters when D4 is set to 1.
D5	Enable Detect Interrupt	0	Disables interrupt at $\overline{INT}$ pin. All interrupts are normally disabled in Power Down mode.
		1	Enables $\overline{INT}$ output. An interrupt will be generated with a change in status of DR bits D1-D4 and D6. The answer tone and call progress detect interrupts are masked when the TX enable bit is set. Carrier detect is masked when TX DTMF is activated. All interrupts will be disabled if the device is in Power Down mode.
D7, D6	Transmit Pattern	D7 D6	
		0 0	Selects normal data transmission as controlled by the state of the TXD pin.
		0 1	Selects an alternating mark/space transmit pattern for modem testing and handshaking. Also used for S1 pattern generation. See CR2 bit D4.
		1 0	Selects a constant mark transmit pattern.
		1 1	Selects a constant space transmit pattern.

DETECT REGISTER

	D7	D6	D5	D4	D3	D2	D1	D0
DR 010	RECEIVE LEVEL INDICATOR	S1 PATTERN DETECT	RECEIVE DATA	UNSCR. MARK DETECT	CARRIER DETECT	SPECIAL TONE DETECT	CALL PROG. DETECT	SIGNAL QUALITY INDICATOR

BIT NO.	NAME	CONDITION			DESCRIPTION
D0	Signal Quality Indicator	0			Indicates normal received signal.
		1			Indicates low received signal quality (above average error rate). Interacts with Special Register SQ bits D2, D1.
D1	Call Progress Detect	0			No call progress tone detected.
		1			Indicates presence of call progress tones. The call progress detection circuitry is activated by energy in the normal 350 to 620 Hz call progress band.
D2	Special Tone Detect	0			Condition not detected
		1			Condition detected
		CR0 D0	TR D0	CR2 D5	
		1	0	1	2225 Hz ±10 Hz answer tone detected in V.22bis, V.22 modes.
		1	1	1	2100 Hz ±21 Hz answer tone detected in V.22bis, V.22 modes.
		0	X	0	900 Hz SCT tone detected in V.23 mode.
		1	X	0	2100 Hz or 2225 Hz answer tone detected in QAM, DPSK mode.
D3	Carrier Detect	0			No carrier detected in the receive channel.
		1			Indicated carrier has been detected in the received channel. Should be time qualified by software.
D4	Unscr. Mark Detect	0			No unscrambled mark being received.
		1			Indicates detection of unscrambled marks in the received data. Should be time qualified by software.
D5	Receive Data				Continuously outputs the received data stream. This data is the same as that output on the RXD pin, but it is not disabled when RXD is tri-stated.
D6	S1 Pattern Detect	0			No S1 pattern being received.
		1			S1 pattern detected. Should be time qualified by software. S1 is an unscrambled double dibit (11001100...) sent in DPSK 1200 bit/s mode. Generated pattern must be properly aligned to transmitter baud clock to be detected.
D7	Receive Level Indicator	0			Received signal level below threshold, (≈ -25 dBm0);can use receive gain boost (+18 dB)
		1			Received signal above threshold.

TONE REGISTER

	D7	D6	D5	D4	D3	D2	D1	D0
TR 011	RXD OUTPUT CONTR.	TRANSMIT GUARD/ CALLING/SCT TONE	TRANSMIT ANSWER TONE	TRANSMIT DTMF	DTMF 3	DTMF 2/ WIRE FDX	DTMF 1/ OVER-SPEED	DTMF 0/ G.T./ANSW./ CALLING/SCT TONE/SEL

BIT NO.	NAME	CONDITION	DESCRIPTION
D0, D4, D5, D6	DTMF 0/ Guard Tone/ Answer Tone/ Calling/SCT Tone/ Transmit Select	D6 D5 D4 D0	D0 interacts with bits D6, D5, D4, and CR0 as shown.
		X X 1 X	Transmit DTMF tones (overides all other functions).
		1 0 0 0	Select 1800 Hz guard tone if in V.22bis or V.22 and Answer mode in CR0.
		1 0 0 1	Select 550 Hz guard tone if in V.22bis or V.22 and Answer mode in CR0.
		Note: Bit D0 also selects the answer tone detected in Originate mode, see Detect Register Special Tone Detect (bit D2) for details.	
		1 0 0 0	1300 Hz calling tone will be transmittted if V.22, V.22bis or V.23 Originate mode is selected in CR0.
		X 1 0 0	Transmit 2225 Hz Answer Tone. Must be in DPSK Answer mode.
		X 1 0 1	Transmit 2100 Hz Answer Tone. Must be in DPSK Answer mode.
		1 0 0 1	900 Hz SCT (soft carrier turnoff) tone transmitted in V.23 75 bit/s Receive mode. (CR0 bit D0 = 1).
D1	DTMF 1/ Overspeed	D4 D1	D1 interacts with D4 as shown.
		0 0	Asynchronous QAM/DPSK +1% -2.5%. (Normal).
		0 1	Asynchronous QAM/DPSK, 2400, 1200 or 600 bit/s +2.3% -2.5%. (Extended overspeed).
D2	DTMF 2/ 4 WIRE FDX	D4 D2	
		0 0	Selects 2-wire full-duplex or half-duplex.
		0 1	D2 selects 4 wire full duplex in the Modulation mode selected. The receive path corresponds to the ANS/ ORIG bit CR0 D0 in terms of high or low band selection. The transmitter is in the same band as the receiver, but does not have magnitude filtering or equalization on its signal as in the receive path.

Note: DTMF0 - DTMF2 should be set to an appropriate state after DTMF dialing to avoid unintended operation.

TONE REGISTER (continued)

	D7	D6	D5	D4	D3	D2	D1	D0
TR 011	RXD OUTPUT CONTR.	TRANSMIT GUARD/ CALLING/SCT TONE	TRANSMIT ANSWER TONE	TRANSMIT DTMF	DTMF 3	DTMF 2/ WIRE FDX	DTMF 1/ OVER-SPEED	DTMF 0/ GUARD/ CALLING/SCT TONE SEL

BIT NO.	NAME	CONDITION	DESCRIPTION
D3, D2, D1, D0	DTMF 3, 2, 1, 0	D4 = 1	Programs 1 of 16 DTMF tone pairs that will be transmitted when TX DTMF and TX enable bit (CR0, bit D1) is set. Tone encoding is shown below:

KEYBOARD EQUIVALENT	DTMF CODE D3	D2	D1	D0	TONES LOW	HIGH
1	0	0	0	1	697	1209
2	0	0	1	0	697	1336
3	0	0	1	1	697	1477
4	0	1	0	0	770	1209
5	0	1	0	1	770	1336
6	0	1	1	0	770	1477
7	0	1	1	1	852	1209
8	1	0	0	0	852	1336
9	1	0	0	1	852	1477
0	1	0	1	0	941	1336
*	1	0	1	1	941	1209
#	1	1	0	0	941	1477
A	1	1	0	1	697	1633
B	1	1	1	0	770	1633
C	1	1	1	1	852	1633
D	0	0	0	0	941	1633

D7	RXD Output Control	0	Enables RXD pin. Receive data will be output on RXD.
		1	Disables RXD pin.The RXD pin reverts to a high impedance with internal weak pull-up resistor.

CONTROL REGISTER 2

	D7	D6	D5	D4	D3	D2	D1	D0
CR2 100	0	SPEC REG ACCESS	CALL INIT	TRANSMIT S1	16 WAY	$\overline{\text{RESET}}$ DSP	TRAIN INHIBIT	EQUALIZER ENABLE

BIT NO.	NAME	CONDITION	DESCRIPTION
D0	Equalizer Enable	0	The adaptive equalizer is in its initialized state.
		1	The adaptive equalizer is enabled. This bit is used in handshakes to control when the equalizer should calculate its coefficients.
D1	Train Inhibit	0	The adaptive equalizer is active.
		1	The adaptive equalizer coefficients are frozen.
D2	$\overline{\text{RESET}}$ $\overline{\text{DSP}}$	0	The DSP is inactive and all variables are initialized.
		1	The DSP is running based on the mode set by other control bits
D3	16 Way	0	The receiver and transmitter are using the same decision plane (based on the Modulator Control Mode).
		1	The receiver, independent of the transmitter, is forced into a 16 point decision plane. Used for QAM handshaking.
D4	Transmit S1	0	The transmitter when placed in alternating Mark/Space mode transmits 0101 . . . . scrambled or not dependent on the bypass scrambler bit and Modulation mode.
		1	When this bit is 1 and only when the transmitter is placed in alternating Mark/Space mode by CR1 bits D7, D6, an unscrambled repetitive double dibit pattern of 00 and 11 at 1200 bit/s (S1) is sent.
D5	Call Init	0	The DSP is setup to do demodulation and pattern detection based on the Various mode bits. Both answer tones are detected in Demod Mode concurrently; TR D0 is ignored.
		1	The DSP decodes call progress, calling tones, unscrambled mark, and 2100 Hz and 2225 Hz answer tones.
D6	Special Register Access	0	Normal CR3 access.
		1	Setting this bit and addressing CR3 allows access to the SPECIAL REGISTER. See the SPECIAL REGISTER for details.
D7	N/A	0	Must be 0 for normal operation.

CONTROL REGISTER 3

	D7	D6	D5	D4	D3	D2	D1	D0
CR3 101	TXDALT	TRISTATE TX/RXCLK	0	RECEIVE ENABLE BOOST	TRANSMIT ATTEN. 3	TRANSMIT ATTEN. 2	TRANSMIT ATTEN. 1	TRANSMIT ATTEN. 0

BIT NO.	NAME	CONDITION	DESCRIPTION
D3, D2, D1,D0	Transmit Attenuator	D3 D2 D1 D0 0 0 0 0 - 1 1 1 1	Sets the attenuation level of the transmitted signal in 1 dB steps. The default (D3-D0=0100) is for a transmit level of -10 dBm0. The total range is 16 dB.
D4	Receive Gain Boost (18 dB)	0	18 dB receive front end boost is not used.
		1	Boost is in the path. This boost does not change reference levels. It is used to extend dynamic range by compensating for internally generated noise when receiving weak signals. The receive level detect signal and knowledge of the hybrid and transmit attenuator setting will determine when boost should be enabled.
D5	Not Used	0	Not used. Only write zeros this location.
D6	Tristate TXCLK/RXCLK	0	TXCLK, RXCLK outputs driven
		1	TXCLK, RXCLK outputs in Tristate mode
D7	TXDALT	Spec. Reg. bit D3=1	Alternate TX data source. See Special Register.

ID REGISTER

SPECIAL REGISTER

	D7	D6	D5	D4	D3	D2	D1	D0
SR 101	0	TXBAUD CLOCK	RXUN- DSCR DATA	0	TXD SOURCE	SIGNAL QUALITY LEVEL SELECT1	SIGNAL QUALITY LEVEL SELECT0	0

BIT NO.	NAME	DESCRIPTION
D7, D4, D0		NOT USED AT THIS TIME. Only write ZEROs to these bits.
D6	TXBAUD CLK	TXBAUD clock is the transmit baud-synchronous clock that can be used to synchronize the input of arbitrary quad/di-bit patterns. The rising edge of TXBAUD signals the latching of a baud-worth of data internally. Synchronous data to be entered via the TXDALT bit, CR3 bit D7, should have data transitions that start 1/2 bit period delayed from the TXBAUD clock edges.
D5	RXUNDSCR DATA	This bit outputs the data received before going to the descrambler. This is useful for sending special unscrambled patterns that can be used for signaling.

SPECIAL REGISTER (continued)

BIT NO.	NAME	DESCRIPTION
D3	TXD SOURCE	This bit selects the transmit data source; either the TXD pin if ZERO or the TXDALT if this bit is a ONE. The TRANSMIT PATTERN bits D7 and D6 in CR1 override either of these sources.
D2, D1	SIGNAL QUALITY LEVEL SELECT	The signal quality indicator is a logical zero when the signal received is acceptable for low error rate reception. It is determined by the value of the Mean Squared Error (MSE) calculated in the decisioning process when compared to a given threshold. This threshold can be set to four levels of error rate. The SQI bit will be low for good or average connections. As the error rate crosses the threshold setting, the SQI bit will toggle at a 1.66 ms rate. Toggling will continue until the error rate indicates that the data pump has lost convergence and a retrain is required. At that point the SQI bit will be a ONE constantly. The SQI bit and threshold selection are valid for QAM and DPSK only.

D2	D1	TYPICAL THRESHOLD VALUE	UNITS
0	0	10^{-5}	BER (default)
0	1	10^{-6}	BER
1	0	10^{-4}	BER
1	1	10^{-3}	BER

NOTE: This register is "mapped" and is accessed by setting CR2 bit D6 to a ONE and addressing CR3. This register provides functions to the 73K324L user that are not necessary in normal communications. Bits D7-D4 are read only, while D3-D0 are read/write. To return to normal CR3 access, CR2 bit D6 must be returned to a ZERO.

	D7	D6	D5	D4	D3	D2	D1	D0
ID 110	ID 3	ID 2	ID 1	ID 0	X	X	X	X

BIT NO.	NAME	CONDITION	DESCRIPTION
		D7 D6 D5 D4	Indicates Device:
D7, D6, D5, D4	Device Identification Signature	0 0 X X	SSI 73K212L or 73K322L or 73K321L
		0 1 X X	SSI 73K221L or 73K302L
		1 0 X X	SSI 73K222L
		1 1 0 0	SSI 73K224L
		1 1 1 0	SSI 73K324L
D3-D0	Undefined	NAMask in software	

ELECTRICAL SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING
VDD Supply Voltage	7V
Storage Temperature	-65 to 150°C
Soldering Temperature (10 sec.)	260°C
Applied Voltage	-0.3 to VDD+0.3V
Note: All inputs and outputs are protected from static charge using built-in, industry standard protection devices and all outputs are short-circuit protected.	

RECOMMENDED OPERATING CONDITIONS

PARAMETER	CONDITION	MIN	NOM	MAX	UNIT
VDD Supply voltage		4.5	5	5.5	V
External Components (Refer to Application section for placement.)					
VREF Bypass capacitor	(VREF to GND)	0.22			µF
Bias setting resistor	(Placed between VDD and ISET pins)	1.8	2	2.2	MΩ
ISET Bypass capacitor	(ISET pin to GND)	0.22			µF
VDD Bypass capacitor 1	(VDD to GND)	0.22			µF
VDD Bypass capacitor 2	(VDD to GND)	22			µF
XTL1 Load Capacitance	Depends on crystal requirements		18	39	pF
XTL2 Load Capacitance	Depends on crystal requirements		18	27	pF
Clock Variation	(11.0592 MHz) Crystal or external clock	-0.01		+0.01	%
TA, Operating Free-Air Temperature		-40		85	°C

DC ELECTRICAL CHARACTERISTICS

(TA = -40°C to 85°C, VDD = recommended range unless otherwise noted)

PARAMETER	CONDITION	MIN	NOM	MAX	UNIT
IDD, Supply Current	CLK = 11.0592 MHz				
	ISET Resistor = 2 MΩ				
IDD1, Active	Operating with crystal oscillator		18	25	mA
IDD2, Idle	< 5 pF capacitive load on CLK pin			5	mA
Digital Inputs					
VIL, Input Low Voltage				0.8	V
VIH, Input High Voltage					
All Inputs except Reset XTL1, XTL2		2.0		VDD	V
Reset, XTL1, XTL2		3.0		VDD	V
IIH, Input High Current	VI = VDD			100	µA
IIL, Input Low Current	VI = 0V	-200			µA
Reset Pull-down Current	Reset = VDD	-2	-30	-70	µA
Digital Outputs					
VOH, Output High Voltage	IO = IOH Min IOUT = -0.4 mA	2.4		VDD	V
VOL, Output Low Voltage	IO = IOUT = 1.6 mA			0.4	V
RXD Tri-State Pull-up Curr.	RXD = GND	-2		-50	µA
Capacitance					
Maximum Capacitive Load					
CLK				25	pF
Input Capacitance	All Digital Inputs			10	pF

DYNAMIC CHARACTERISTICS AND TIMING

(TA = -40°C to +85°C, VDD = recommended range unless otherwise noted)

PARAMETER	CONDITION	MIN	NOM	MAX	UNIT
QAM/DPSK Modulator					
Carrier Suppression	Measured at TXA	35			dB
Output Amplitude	TX scrambled marks ATT= 0100 (default)	-11.5	-10.0	-9	dBm0
FSK Modulator/Demodulator					
Output Freq. Error	CLK = 11.0592 MHz	-.31		+0.20	%
Transmit Level	ATT = 0100 (Default) Transmit Dotting Pattern	-11.5	-10.0	-9	dBm0
TXA Output Distortion	All products through BPF			-45	dB
Output Bias Distortion at RXD	Dotting Pattern measured at RXD Receive Level -20 dBm, SNR 20 dB	-10		+10	%
Output Jitter at RXD	Integrated for 5 seconds	-15		+15	%
Sum of Bias Distortion and Output Jitter at RXD	Integrated for 5 seconds	-15		+15	%
2100 Hz Answer Tone Generator					
Output Amplitude	ATT = 0100 (Default Level) Not in V.21 or V.23 Mode	-11.5	-10	-9	dBm0
Output Distortion	Distortion products in receive band			-40	dB
DTMF Generator	Not in V.21 or V.23 mode				
Freq. Accuracy		-0.03		+0.25	%
Output Amplitude	Low Band, ATT = 0100	-10		-8	dBm0
Output Amplitude	High Band, ATT = 0100	-8		-6	dBm0
Twist	High-Band to Low-Band	1.0	2.0	3.0	dB
Receiver Dynamic Range	Refer to Performance Curves	-43		-3.0	dBm0
Call Progress Detector	In Call Init mode				
Detect Level	460 Hz input signal	-34		0	dBm0
Reject Level				-40	dBm0
Delay Time	-70 dBm0 to -30 dBm0 STEP			25	ms
Hold Time	-30 dBm0 to -70 dBm0 STEP			25	ms
Hysteresis	@ 460 Hz input signal	2			dB

NOTE: Parameters expressed in dBm0 refer to the following definition:

0 dB loss in the Transmit path to the line

2 dB gain in the Receive path from the line

Refer to the Basic Box Modem diagram in the Applications section for the DAA design.

DYNAMIC CHARACTERISTICS AND TIMING (continued)

PARAMETERS		CONDITIONS	MIN	NOM	MAX	UNITS
Carrier Detect Receive Gain Boost "On" for Lower Input Level Measurements						
Threshold		QAM/DPSK or FSK receive data	-48		-43	dBm0
Hysteresis		All Modes	2			dB
Delay Time	FSK	70 dBm0 to -6 dBm0	25		37	ms
		70 dBm0 to -40 dBm0	25		37	ms
	DPSK	-70 dBm0 to -6 dBm0	7		17	ms
		-70 dBm0 to -40 dBm0	7		17	ms
	QAM	-70 dBm0 to -6 dBm0	25		37	ms
		-70 dBm0 to -40 dBm0	25		37	ms
Hold Time	FSK	-6 dBm0 to -70 dBm0	25		37	ms
		-40 dBm0 to -70 dBm0	15		30	ms
	DPSK	-6 dBm0 to -70 dBm0	20		29	ms
		-40 dBm0 to -70 dBm0	14		21	ms
	QAM	-6 dBm0 to -70 dBm0	25		32	ms
		-40 dBm0 to -70 dBm0	8		28	ms
Special Tone Detectors						
Detect Level		See definitions for D0 of Tone Register	-48		-43	dBm0
Delay and Hold Time						
2225 or 2100 Hz answer tone		Call INIT mode 2225 ± 10 Hz 2100 ± 21 Hz	6		50	ms
900 Hz SCT Receive V.23 main channel		Tone Accuracy ±9 Hz	10		45	ms
Hysteresis			2			dB
Pattern Detectors		DPSK Mode				
S1 Pattern						
Delay Time		For signals from -6 to -40 dBm0,	10		55	ms
Hold Time		Demod Mode	10		45	ms
Unscrambled Mark						
Delay Time		For signals from -6 to -40	10		45	ms
Hold Time		Demod or call Init Mode	10		45	ms
Receive Level Indicator						
Detect On			-22		-28	dBm0
Valid after Carrier Detect		DPSK Mode	1	4	7	ms

DYNAMIC CHARACTERISTICS AND TIMING (continued)

PARAMETER	CONDITION	MIN	NOM	MAX	UNIT
Output Smoothing Filter					
Output Impedance	TXA pin		200	300	Ω
Output Load	TXA pin; FSK Single	10			kΩ
	Tone out for THD = -50 dB in 0.3 to 3.4 kHz range			50	pF
Maximum Transmitted Energy	4 kHz, Guard Tones off			-35	dBm0
	10 kHz, Guard Tones off			-55	dBm0
	12 kHz, Guard Tones off			-65	dBm0
Anti Alias Low Pass Filter					
Maximum allowed Out-of-Band Signal Energy (Defines Hybrid Trans-Hybrid loss requirements)	Scrambled data at 2400 bit/s in opposite band		-14		dBm
	Sinusoids out of band		-9		dBm
Transmit Attenuator					
Range of Transmit Level	1111-0000 Default ATT = 0100 (-10 dBm0)	-21		-6	dBm0
Step Accuracy		-0.15		+0.15	dB
Clock Noise	TXA pin; 153.6 kHz		1.5		mV rms
Carrier Offset					
Capture Range	Originate or Answer		±5		Hz
Recovered Clock					
Capture Range	% of data rate originate or answer	-.02		+.02	%
Guard Tone Generator					
Tone Accuracy	550 Hz		+1.2		%
	1800 Hz		-0.8		%
Tone Level	550 Hz	-4.5	-3.0	-1.5	dB
(Below QAM/DPSK Output)	1800 Hz	-7.5	-6.1	-4.5	dB
Harmonic Distortion (700 to 2900 Hz)	550 or 1800 Hz			-50	dB

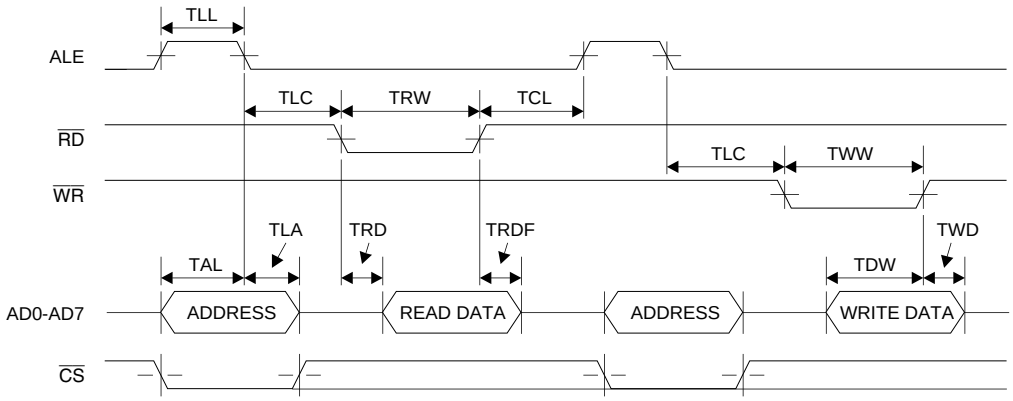
DYNAMIC CHARACTERISTICS AND TIMING (continued)

PARAMETER	CONDITION	MIN	NOM	MAX	UNIT
Timing (Refer to Timing Diagrams)					
Parallel Mode:					
TAL	$\overline{CS}$/Addr. setup before ALE Low	30			ns
TLA	$\overline{CS}$/Addr. hold after ALE Low	6			ns
TLC	ALE Low to $\overline{RD}$/$\overline{WR}$ Low	40			ns
TCL	$\overline{RD}$/$\overline{WR}$ Control to ALE High	10			ns
TRD	Data out from $\overline{RD}$ Low			90	ns
TLL	ALE width	25			ns
TRDF	Data float after $\overline{RD}$ High			40	ns
TRW	$\overline{RD}$ width	70			ns
TWW	$\overline{WR}$ width	70			ns
TDW	Data setup before $\overline{WR}$ High	70			ns
TWD	Data hold after $\overline{WR}$ High	20			ns
Serial Mode:					
TRCK	Clock high after $\overline{RD}$	250		T1	ns
TAR	Address setup before $\overline{RD}$ low	0			ns
TRA	Address hold after $\overline{RD}$ low	350			ns
TRD	$\overline{RD}$ to data valid			110	ns
TRDF	Data float after $\overline{RD}$ high			50	ns
TCKDR	Read data out after falling edge of EXCLK			300	ns
TWW	$\overline{WR}$ width	350			ns
TAW	Address setup before $\overline{WR}$	50			ns
TWA	Address hold after rising edge of $\overline{WR}$	50			ns
TCKDW	Write data hold after falling edge of EXCLK	200			ns
TCKW	$\overline{WR}$ high after falling edge of EXCLK	330		T1& T2	ns
TDCK	Data setup before falling edge of EXCLK	50			ns
T1, T2	Minimum period	500			ns
Note: T1 and T2 are the low/high periods, respectively, of EXCLK in Serial mode.					

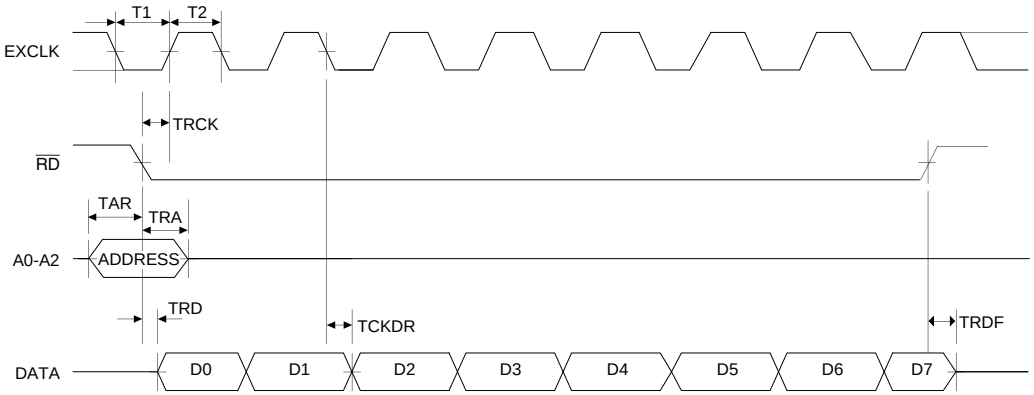
NOTE: Asserting ALE, $\overline{CS}$, and $\overline{RD}$ or $\overline{WR}$ concurrently can cause unintentional register accesses. When using non-8031 compatible processors, care must be taken to prevent this from occurring when designing the interface logic.

TIMING DIAGRAMS

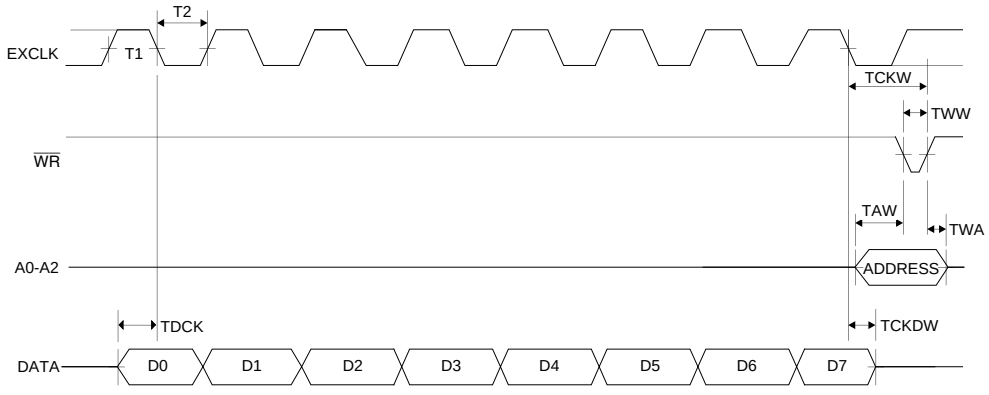
BUS TIMING DIAGRAM (PARALLEL VERSION)



READ TIMING DIAGRAM (SERIAL VERSION)



WRITE TIMING DIAGRAM (SERIAL VERSION)



APPLICATIONS INFORMATION

GENERAL CONSIDERATIONS

Figures 1 and 2 show basic circuit diagrams for K-Series modem integrated circuits. K-Series products are designed to be used in conjunction with a control processor, a UART or RS-232 serial data interface, and a DAA phone line interface to function as a typical intelligent modem. The K-Series ICs interface directly with Intel 8048 and 80C51 microprocessors for control and status monitoring purposes.Two typical DAA arrangements are shown: one for a split ±5 or ±12 volt design and one for a single 5 volt design. These diagrams are for reference only and do not represent production-ready modem designs.

K-Series devices are available with two control interface versions: one for a parallel multiplexed address/data interface, and one for a serial interface. The parallel version is intended for use with 8039/48 or 8031/51 microcontrollers from Intel or many other manufacturers. The serial interface 22-pin version can be used with other microcontrollers or in applications where only a limited number of port lines are available or the application does not lend itself to a multiplexed address/data interface. The parallel versions may also be used in the Serial mode, as explained in the data sheet pin description.

In most applications the controller will monitor the serial data for commands from the DTE and the received data for break signals from the far end modem. In this way, commands to the modem are sent over the same line as the transmitted data. In other applications the RS-232 interface handshake lines are used for modem control.

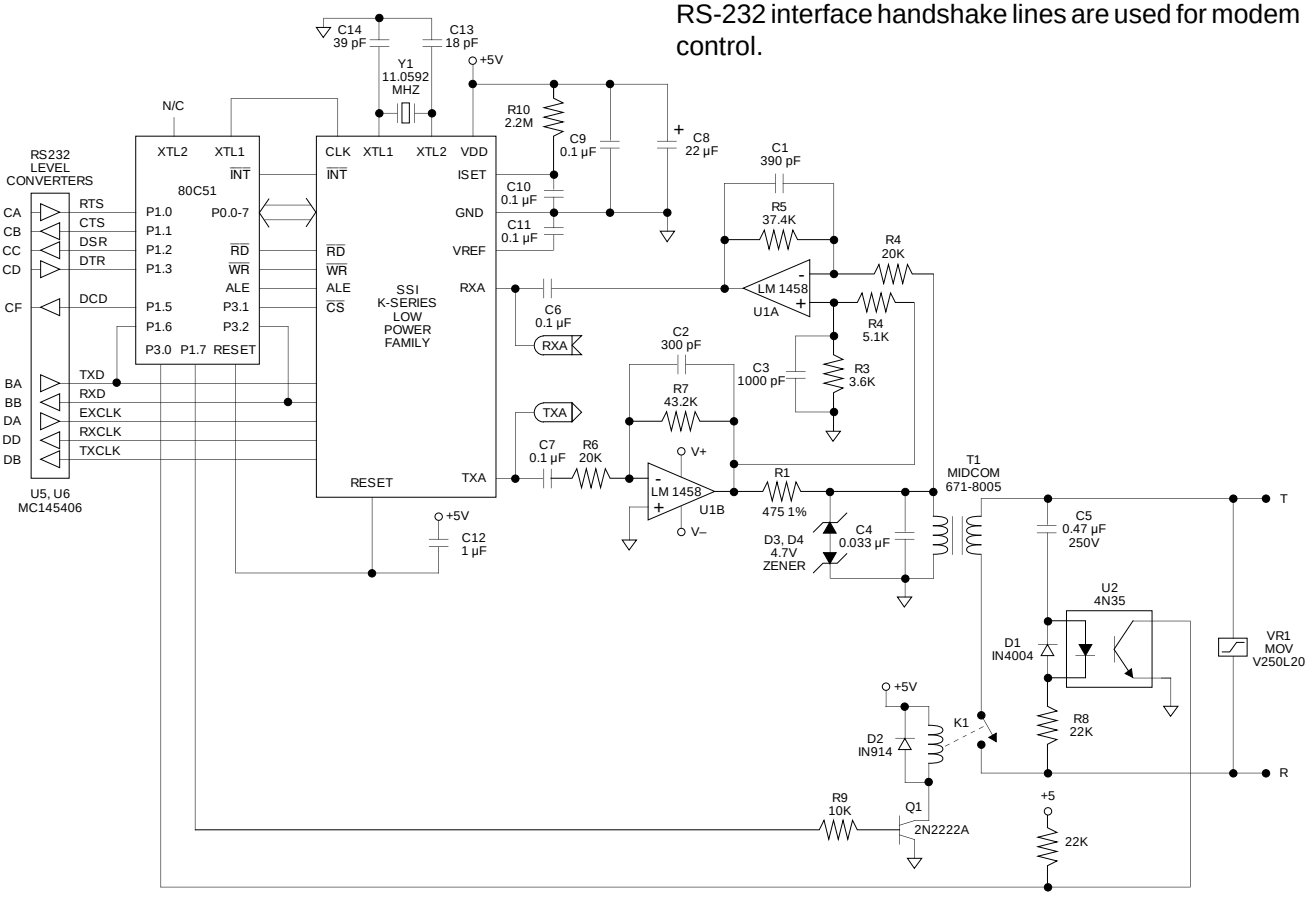


FIGURE 1: Basic Box Modem with Dual-Supply Hybrid

DIRECT ACCESS ARRANGEMENT (DAA)

The telephone line interfaces show two examples of how the "hybrid" may be implemented. The split supply design (Figure 1) is a typical two op-amp hybrid. The receive op-amp serves two purposes. It supplies gain to amplify the receive signal to the proper level for the modem's detectors and demodulator, and it removes the transmitted signal from the receive signal present at the transformer. This is done by supplying a portion of the transmitted signal to the non-inverting input of the receive op-amp at the same amplitude as the signal appearing at the transformer, making the transmit signal Common mode.

The single-supply hybrid is more complex than the dual-supply version described above, but its use eliminates the need for a second power supply. This circuit (Figure 2) uses a bridged drive to allow undistorted signals to be sent with a single 5 volt supply. Because DTMF tones utilize a higher amplitude than data, these signals will clip if a single-ended drive approach is used. The bridged driver uses an extra op-amp (U1A) to invert the signal coming from the gain setting op-amp (U1B) before sending it to the other leg of the transformer. Each op-amp then supplies half the drive signal to the transformer. The receive amplifier (U1C) picks off its signal at the junction of the impedance matching resistor and the transformer. Because the bottom leg of the transformer is being driven in one direction by U1A and the resistor is driven in the opposite direction at the same time by U1B, the junction of the transformer and resistor remains relatively constant and the receive signal is unaffected.

DESIGN CONSIDERATIONS

Silicon Systems' 1-chip modem products include all basic modem functions. This makes these devices adaptable for use in a variety of applications, and as easy to control as conventional digital bus peripherals.

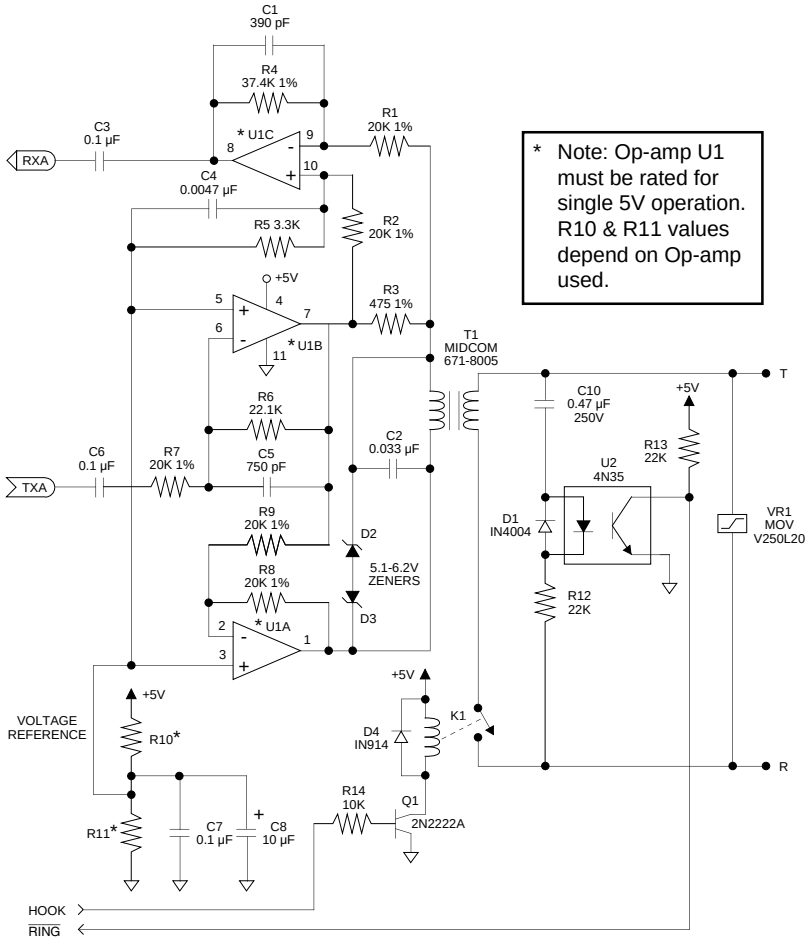


FIGURE 2: Single 5V Hybrid Version

Unlike digital logic circuitry, modem designs must properly contend with precise frequency tolerances and very low level analog signals, to ensure acceptable performance. Using good analog circuit design practices will generally result in a sound design. Following are additional recommendations which should be taken into consideration when starting new designs.

CRYSTAL OSCILLATOR

The K-Series crystal oscillator requires a Parallel mode (antiresonant) crystal which operates at 11.0592 MHz. It is important that this frequency be maintained to within ±0.01% accuracy.

In order for a Parallel mode crystal to operate correctly and to specification, it must have a load capacitor connected to the junction of each of the crystal and internal inverter connections, terminated to ground. The values of these capacitors depend primarily on the crystal's characteristics, and to a lesser degree on the internal inverter circuit. The values used affect the accuracy and start up characteristics of the oscillator.

LAYOUT CONSIDERATIONS

Good analog/digital design rules must be used to control system noise in order to obtain highest performance in modem designs. The more digital circuitry present on the PC board, the more this attention to noise control is needed. The modem should be treated as a high impedance analog device. A 22 µF electrolytic capacitor in parallel with a 0.22 µF ceramic capacitor between VDD and GND is recommended. Liberal use of ground planes and larger traces on power and ground are also highly favored. High speed digital circuits tend to generate a significant amount of EMI (Electro-Magnetic Interference) which must be minimized in order to meet regulatory agency limitations. To accomplish this, high speed digital devices should be locally bypassed, and the telephone line interface and K-Series device should be located close to each other near the area of the board where the phone line connection is accessed. To avoid problems, power supply and ground traces should be routed separately to the analog and digital functions on the board, and digital signals should not be routed near low level or high impedance analog traces. The analog and digital grounds should only connect at one point near the K-Series device ground pin to avoid ground loops. The K-Series modem IC's should have both high frequency and low frequency bypassing as close to the package as possible. The ISET resistor and bypass capacitor need to be as close to device as possible.

MODEM PERFORMANCE CHARACTERISTICS

The curves presented here define modem IC performance under a variety of line conditions while inducing disturbances that are typical of those encountered during data transmission on public service telephone lines. Test data was taken using an AEA Electronics' "Autotest I" modem test set and line simulator, operating under computer control. All tests were run full-duplex, using a Hayes 2400 Smartmodem™ as the reference modem. A 511 pseudo-random-bit pattern was used for each data point. Noise was C-message weighted and all signal-to-noise (S/N) ratios reflect total power measurements similar to the CCITT V.56 measurement specification. The individual tests are defined as follows.

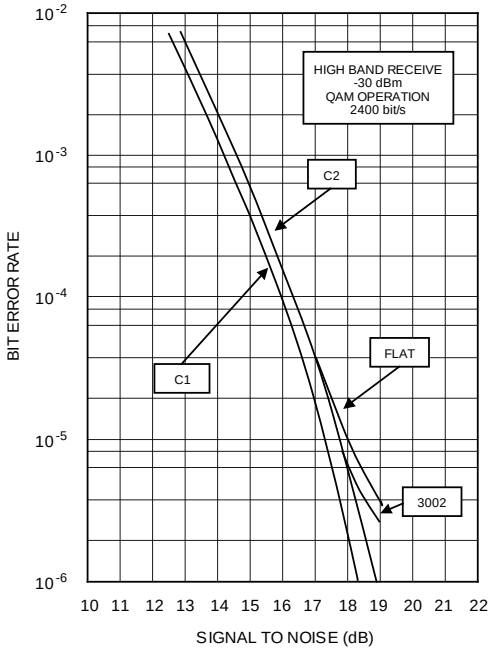
BER vs. S/N

This test measures the ability of the modem to operate over noisy lines with a minimum of data-transfer errors. Since some noise is generated in the best of dial-up lines, the modem must operate with the lowest S/N ratio possible. Better modem performance is indicated by test curves that are closest to the BER axis. A narrow spread between curves representing the four line parameters indicates minimal variation in performance while operating over a range of aberrant operating conditions. Typically, a modem will exhibit better BER-performance test curves receiving in the low band than in the high band.

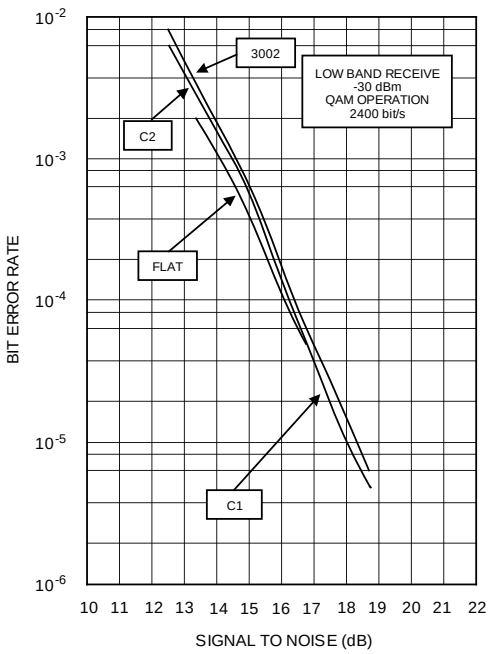
BER vs. Receive Level

This test measures the dynamic range of the modem. Because signal levels vary widely over dial-up lines, the widest possible dynamic range is desirable. The minimum Bell specification calls for 36 dB of dynamic range. S/N ratios are held constant at the indicated values while the receive level is lowered from a very high to very low signal levels. The width of the "bowl" of these curves, taken at the BER point, is the measure of dynamic range.

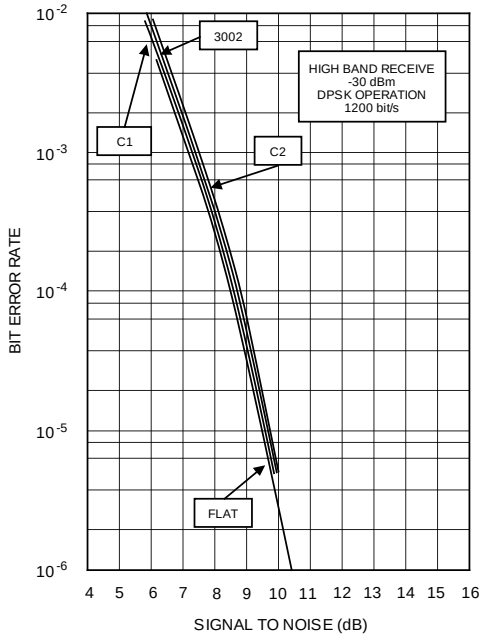
SSI 73K324L BER vs S/N
PRELIMINARY



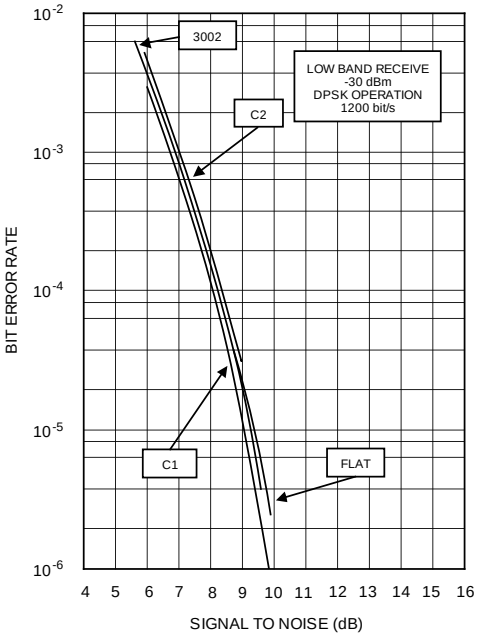
SSI 73K324L BER vs S/N
PRELIMINARY

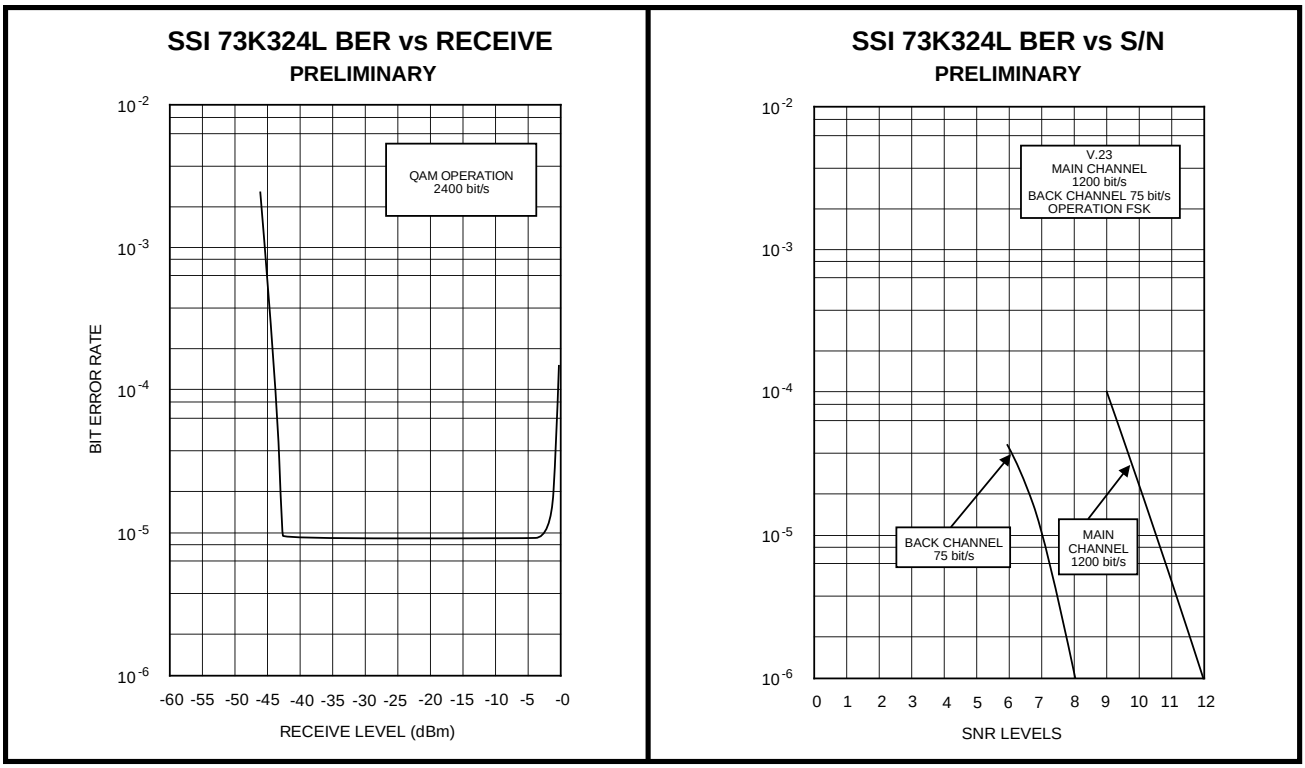


SSI 73K324L BER vs S/N
PRELIMINARY



SSI 73K324L BER vs S/N
PRELIMINARY

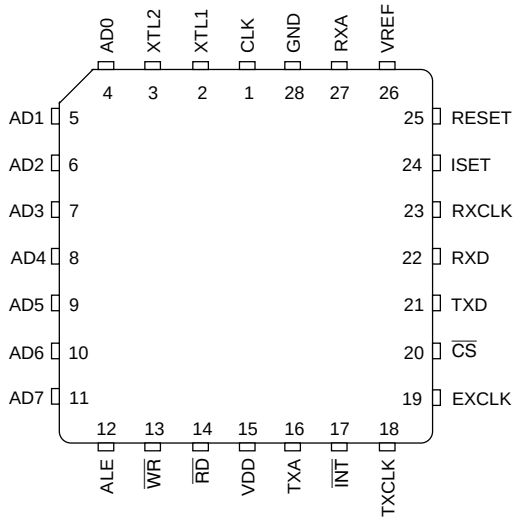



SSI 73K324L BER vs RECEIVE
PRELIMINARY
BIT ERROR RATE
10-2
10-3
10-4
10-5
10-6
QAM OPERATION
2400 bit/s
-60 -55 -50 -45 -40 -35 -30 -25 -20 -15 -10 -5 -0
RECEIVE LEVEL (dBm)
SSI 73K324L BER vs S/N
PRELIMINARY
V.23
MAIN CHANNEL
1200 bit/s
BACK CHANNEL 75 bit/s
OPERATION FSK
BACK CHANNEL
75 bit/s
MAIN
CHANNEL
1200 bit/s
0 1 2 3 4 5 6 7 8 9 10 11 12
SNR LEVELS

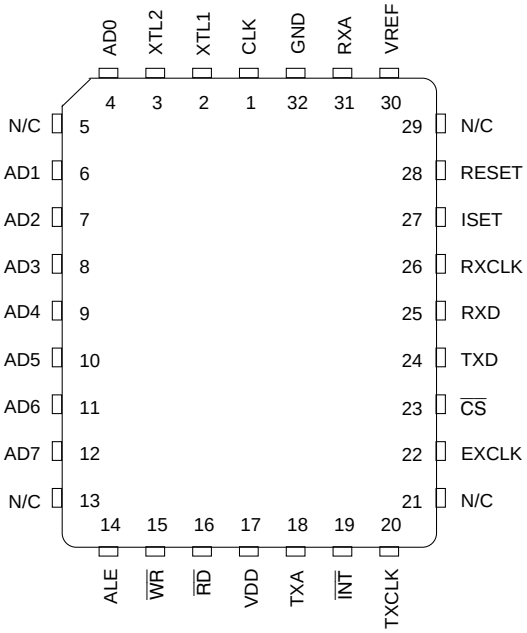
SSI 73K324L
CCITT V.22bis, V.22, V.21, V.23, Bell 212A
Single-Chip Modem

PACKAGE PIN DESIGNATIONS

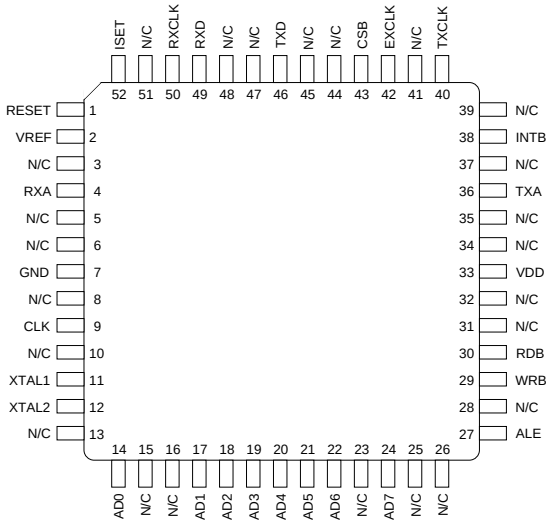
(Top View)



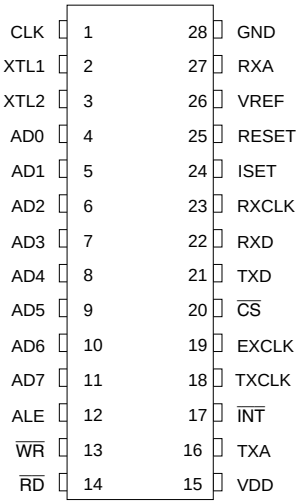
28-Pin PLCC



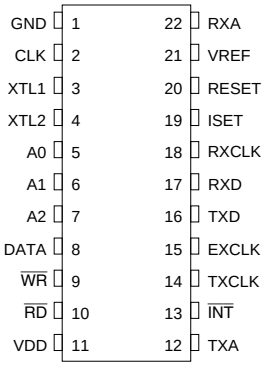
32-Pin PLCC



52-Lead QFP



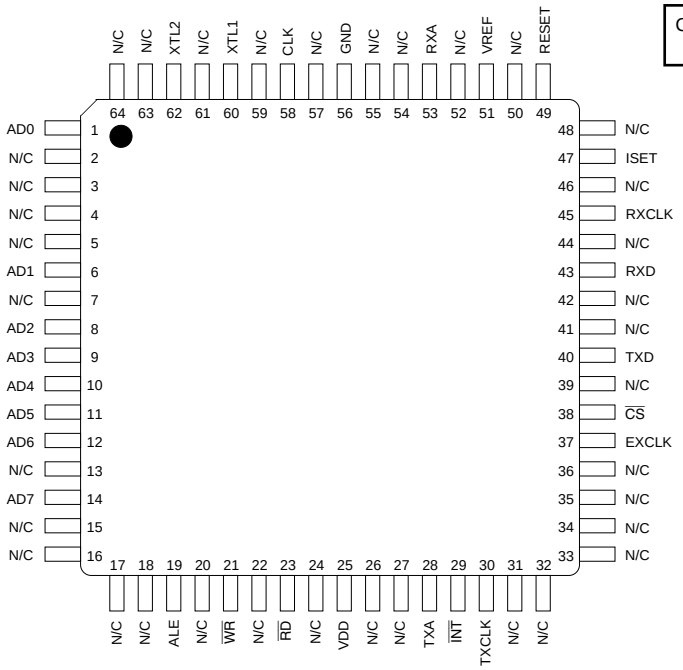
28-Pin DIP



400-Mil
22-Pin DIP

CAUTION: Use handling procedures necessary for a static sensitive component.

CAUTION: Use handling procedures necessary for a static sensitive component.



64-Lead TQFP

ORDERING INFORMATION

PART DESCRIPTION	ORDER NO.	PKG. MARK
SSI 73K324L		
22-Pin Plastic Dual-In-Line	73K324LS-IP	73K324LS-IP
SSI 73K324L		
28-Pin Plastic Dual-In-Line	73K324L-IP	73K324L-IP
28-Pin Plastic Leaded Chip Carrier	73K324L-28IH	73K324L-28IH
32-Pin Plastic Leaded Chip Carrier	73K324L-32IH	73K324L-32IH
44-Pin Plastic Leaded Chip Carrier	73K324L-IH	73K324L-IH
52-Pin Quad Flat Pack Package	73K324L-IG	73K324L-IG
64-Lead Thin Quad Flat Pack Package	73K324L-IGT	73K324L-IGT

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Section 4

CONTROLLERS, UARTs & MODEM PRODUCTS

We are sorry, the 73M223 data sheet is not available in an electronic format. Please contact your local Sales office for more information or contact Silicon Systems directly to obtain a paper version.

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SSI 73D2248A/2348A
MNP5, V.42bis Datacom Modem Device Set
Advance Information

January 1996

DESCRIPTION

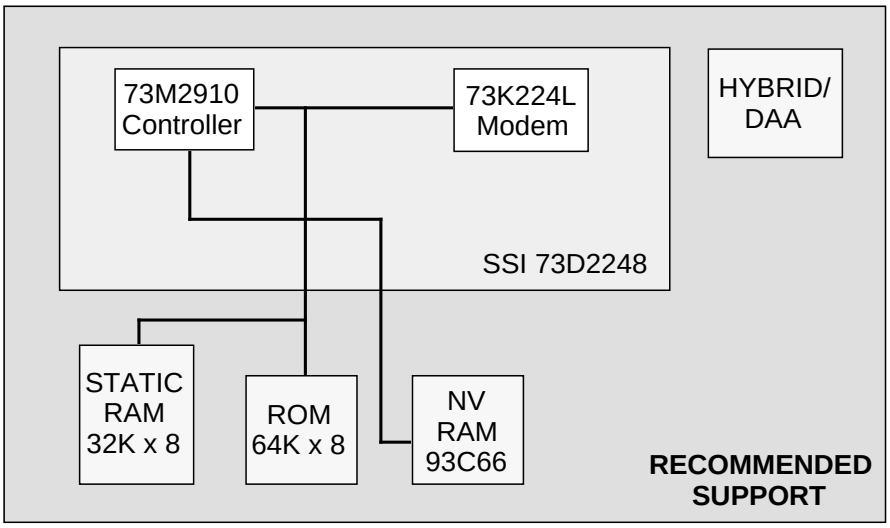
The SSI 73D2248A/2348A Chip Sets consists of two CMOS integrated circuits which provide the data pump and protocol functions required to implement a high performance 2400 bit/s modem with error control and data compression. The 73D2248A basic modem function is provided by the SSI 73K224L modem chip and is compatible with CCITT V.21, V.22, V.22bis and Bell 103 and 212A protocols. The error control functions are provided by modular software running in the SSI 73M2910 controller. Modules are available for MNP4, and V.42. compression software modules can be can be added to the controller; MNP5 and V.42bis are available. Provisions for customization of the command set are provided, forming the basis for an international modem.

The 73D2348 differs from the 73D2248A in that it uses the 73K324L instead of the 73K224L for the data pump. The 73K324L replaces the Bell 103 300 baud FSK mode of operation with the CCITT V.23 1200 baud FSK mode. The software is also modified to support V.23. The two products are otherwise identical.

FEATURES

- **Combines modem and protocol controller**
- **Supports 0 - 300, 1200 and 2400 bit/s with both sync and async modes**
- **Modular software design allows customization**
- **Modem protocols:**
  - **Bell 103, 212A**
  - **CCITT V.22, V.22bis**
- **Error control/compression protocols Available: MNP4, MNP5, CCITT V.42, V.42bis**
- **Supports non-volatile memory to store user configurations and phone numbers**
- **CMOS design for low power consumption**
- **TQFP packages available for PCMCIA applications**

MNP5, V.42bis Datacom Modem Device Set



FUNCTIONAL DESCRIPTION

The SSI 73D2248A/2348A chip set forms the basis for an international modem design incorporating the most advanced error control and compression algorithms. The set consists of two chips, the SSI 73K224L (73K324L) modem and the 73M2910 controller. Customization of the controller is one of the features of this chip set; software modules allow the modem vendor to provide a range of features from a standard hardware platform.

The 73K224L (73K324L) provides the QAM, PSK and FSK modulator and demodulator functions, call progress and handshake tone monitors, test modes and a tone generator capable of producing DTMF, answer and CCITT guardtones. This single-chip modem supports the V.22bis, V.22, V.21 and Bell 103/CCITT V.23/212A operating protocols in both sync and async modes. Low level functions of the controller provide for automatic detection of DTE speed, auto-dial, auto-answer, handshake with fallback and call progress detection.

The 73M2910 controller handles both the low level modem functions as well as protocol negotiation and protocol operation. Software modules can be chosen to provide the desired protocols for product customization and differentiation. In addition, the "AT" command set source code will be available for those desiring to provide unique or country dependent features.

Basic capabilities of the modem are those found in the 73K224L (73K324L) single-chip modem and are listed in the separate 73K224L (73K324L) data sheet.

AUTOMATIC HANDSHAKE

The 73D2248A/2348A will automatically perform a complete handshake with a called or calling modem and enter the data transfer mode. After the link between the two modems has been established, the modems may remain in the normal data mode or negotiate a link which has error control and data compression. Commands are provided to inform the modem which action is appropriate.

TEST MODES

The 73D2248A/2348A chip set has provisions for three test modes: analog loopback, digital loopback and remote digital loopback. Analog loopback allows data to be sent into the local modem, have it modulated and then demodulated and returned to the local terminal. Digital loopback requires the cooperation of the user at the remote end and allows data to be sent to the remote modem, demodulated, then remodulated and returned to the local end. Remote digital loopback allows the same capability, without the need for a remote operator; signals are sent to the remote modem which perform the switching task that a remote operator would have done.

AT COMMAND INTERPRETER

The SSI 73D2248A/2348A includes an AT Command Interpreter which is a superset of the Hayes 2400 Smartmodem™ command set. Common application software will be able to control the modem though this interpreter. Additional commands have been added to provide for control of the MNP and CCITT V.42 modes.

NON-VOLATILE MEMORY

A serial NVRAM provides 256 bytes of storage for configuration information and telephone numbers. Current hardware provides for a 2K bit memory of which about 400 bytes are used for setup and telephone number storage. The remaining 1600 bytes are avaliable. Memory address space allocated to non-volatile RAM is 8K, so an expansion factor of 4 is available. Alternatively, the address space could be decoded for more hardware functionality.

PROTOCOLS

Microcom Networking Protocol (MNP)

MNP4 is a protocol offering error control while MNP5 offers data compression. Data to be transmitted is broken into blocks of varying sizes, depending on line conditions, and sent to the remote modem along with a 16-bit Cyclic Redundancy Check word. If the algorithm used to derive the CRC word at the transmitter does not produce an identical word when exercised on the received data, a line error is assumed, and the block is repeated. Data compression is obtained by transmitting a short set of characters for a longer redundant set. At the receiver, the short string is replaced with the longer string that it represented, and the data stream is returned to its original state.

CCITT V.42 AND V.42BIS

The CCITT has ratified a set of protocols which operate in a manner similar to MNP. MNP4 corresponds to V.42 while MNP5 corresponds with V.42bis. Greater efficiency is offered, but the tradeoff is a larger memory space requirement. MNP5 requires an 8K buffer, while V.42bis requires 32K. Data files which show compression ratios approaching 2:1 with MNP5 may show ratios of nearly 4:1 with V.42bis.

ADDITIONAL INFORMATION

The Silicon Systems 73D2248/2348 Design Manual defines the AT commands. Please contact your local Silicon Systems sales office or Silicon Systems headquarters in Tustin for a copy of the SSi Protocol Design Manual.

AT COMMAND SUMMARY

Command	Description
AT	command prefix – precedes command line
<CR>	carriage return character – terminates command line
A	go into answer mode; attempt to go to on-line state
A/	re-execute previous command line; not preceded by AT nor followed by <CR>
B0	select CCITT V.22 standard for 1200 bit/s communication
B1	***select Bell 212A standard for 1200 bit/s communication***
D	dial number that follows; attempt to go to on-line state, originate mode
DS=n	dial stored number in location “n” (0-3)
E0	Disable character echo in command state
E1	***Enable character echo in command state***
H0	go on hook (hang up)
H1	go off hook; operate auxiliary relay
I0	request product indentification code
I1	perform checksum on firmware ROM; return checksum
I2	perform checksum on firmware ROM; returns OK or ERROR result codes
L0 or L1	low speaker volume
L2	***medium speaker volume***
L3	high speaker volume
M0	speaker off
M1	***speaker on until carrier detected***
M2	speaker always on
M3	speaker on until carrier detected, except during dialing
O0	go to on-line state
O1	go to on-line state and initiate equalizer retrain at 2400 bit/s
Q0	***modem returns result codes***
Q1	modem does not return result codes
Sr	set pointer to register “r”
Sr=n	set register “r” to value “n”
Sr?	display value stored in register “r”
V0	display result codes in numeric form
V1	***display result codes in verbose form (as words)***
W0	***negotiation progress result codes not returned***
W1	negotiation progress result codes returned
X0	enable features represented by result codes 0-4
X1	enable features represented by result codes 0-5, 10-12
X2	enable features represented by result codes 0-6, 10-12
X3	enable features represented by result codes 0-5, 7, 10-12

Command	Description
X4	***enable features represented by result codes 0-7, 10-12***
Y0	***disable long space disconnect***
Y1	enable long space disconnect
Z0	reset modem
&C0	***assume data carrier always present***
&C1	track presence of data carrier
&D0	***ignore DTR signal***
&D1	assume command state when an on-to-off transition of DTR occurs
&D2	hang up and assume command state when an on-to-off transition of DTR occurs
&D3	reset when an on-to-off transition of DTR occurs
&F	recall factory settings as active configuration
&G0	***no guard tone***
&G1	550 Hz guard tone
&G2	1800 Hz guard tone
&K	flow control method
&M0	***asynchronous mode***
&M1	synchronous mode 1
&M2	synchronous mode 2
&M3	synchronous mode 3
&Q5	error control mode
&Q6	automatic speed buffering (ASB)
&T0	terminate test in progress
&T1	initiate local analog loopback
&T3	initiate local digital loopback
&T4	***grant request from remote modem for RDL***
&T5	deny request from remote modem for RDL
&T6	initiate remote digital loopback
&T7	initiate remote digital loopback with self test
&T8	initiate local analog loopback with self test
&V	view active configuration, user profiles, and stored numbers
&W0	save storable parameters of active configuration
&X0	***modem provides transmit clock signal***
&X1	data terminal provides transmit clock signal
&X2	receive carrier provides transmit clock signal
&Zn=x	store phone number “x” in location “n” (0-3)

Dial string arguments:

, = delay	@ = silent answer	! = flash	
; = return to command	s = dial stored number	W = wait for tone	R=reverse mode

If the NovRAM has not been initialized it may be necessary to power down/power up and type *AT&F&W<cr>* to properly initialize modem state.

TABLE 1: Result Codes

Xn	VERBOSE/TERSE RESULT CODES
X0	OK/0, CONNECT/1, RING/2, NO CARRIER/3, ERROR/4
X1	All functions of X0 + CONNECT (RATE)/1 = 300, 5 = 1200, 10 = 2400
X2	All functions of X1 + NO DIAL TONE/6
X3	All functions of X1 + BUSY/7
X4	All functions of X3 + NO DIAL TONE/6, NO ANSWER/8

TABLE 2: S Registers Supported

Sn	FUNCTION	UNITS	DEFAULT
S0[1]	Answer on ring	No. of rings on which to answer	000[2]
S1	Ring counter	No. of rings accumulated	000
S2	Escape code	ASCII CHR Decimal 0-127	043
S3	Carriage return	ASCII CHR Decimal 0-127	013
S4	Line feed	ASCII CHR Decimal 0-127	010
S5	Back space	ASCII CHR	008
S6	Wait for dial tone	Seconds	002
S7	Wait for carrier	Seconds	030
S8	Pause time	Seconds	002
S9	Carrier valid	100 milliseconds (0.1 sec)	006
S10	Carrier drop out	100 milliseconds (0.1 sec)	014
S11	DTMF tone duration	1 millisecond (0.001 sec)	070
S12	Escape guard time	20 milliseconds (0.05 sec)	050
S13	Unused		N/A
*S14[1]	Bit mapped register	Decimal 0-255	170

[1] Stored in NVRAM with &W command.

[2] Modem will not answer until value is changed to 1 or greater.

TABLE 2: S Registers Supported (Continued)

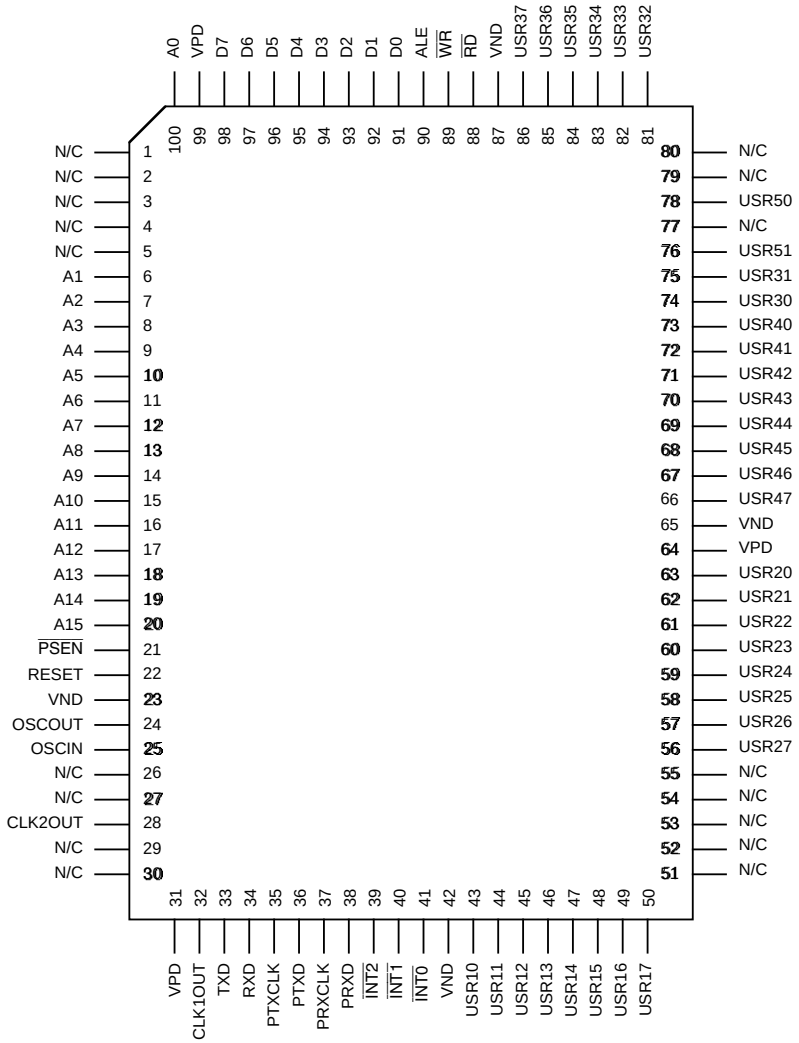
NUMBER	FUNCTION	UNITS	DEFAULT
S15	Unused		N/A
S16	Test register	Decimal #	000
S17	Special test register	Decimal 0-255	096
S18	Test timer	Decimal 0-255	000
S19	Unused		N/A
S20	Unused		N/A
*S21[1]	Bitmapped register	Decimal 0-255	000
*S22[1]	Bitmapped register	Decimal 0-255	118
*S23[1]	Bitmapped register	Decimal 0-255	007
S24	Unused		N/A
S25[1]	DTR delay	10 milliseconds (0.01 sec)	005
S26[1]	CTS delay	10 milliseconds (0.01 sec)	001
*S27[1]	Bitmapped register	Decimal 0-255	064
S36	Negotiation failure treatment		5
S37	Desired modem line speed	Decimal 0-9	000
S38	Hang-up timeout		20
S39	Current flow control setting		3
S43	Current DCE speed		0
S46	Protocol/Compression selection		2
S48	Feature negotiation action		7
S49	ASB Buffer low limit	1-249	8
S50	ASB Buffer high limit	2-250	16
S82	Break select register		128
S95	Extended result code bit map		0

*The bitmapped register functions are equivalent to normal “AT” command modem registers.

[1] Stored in NVRAM with &W command

PACKAGE PIN DESIGNATIONS

(Top View)

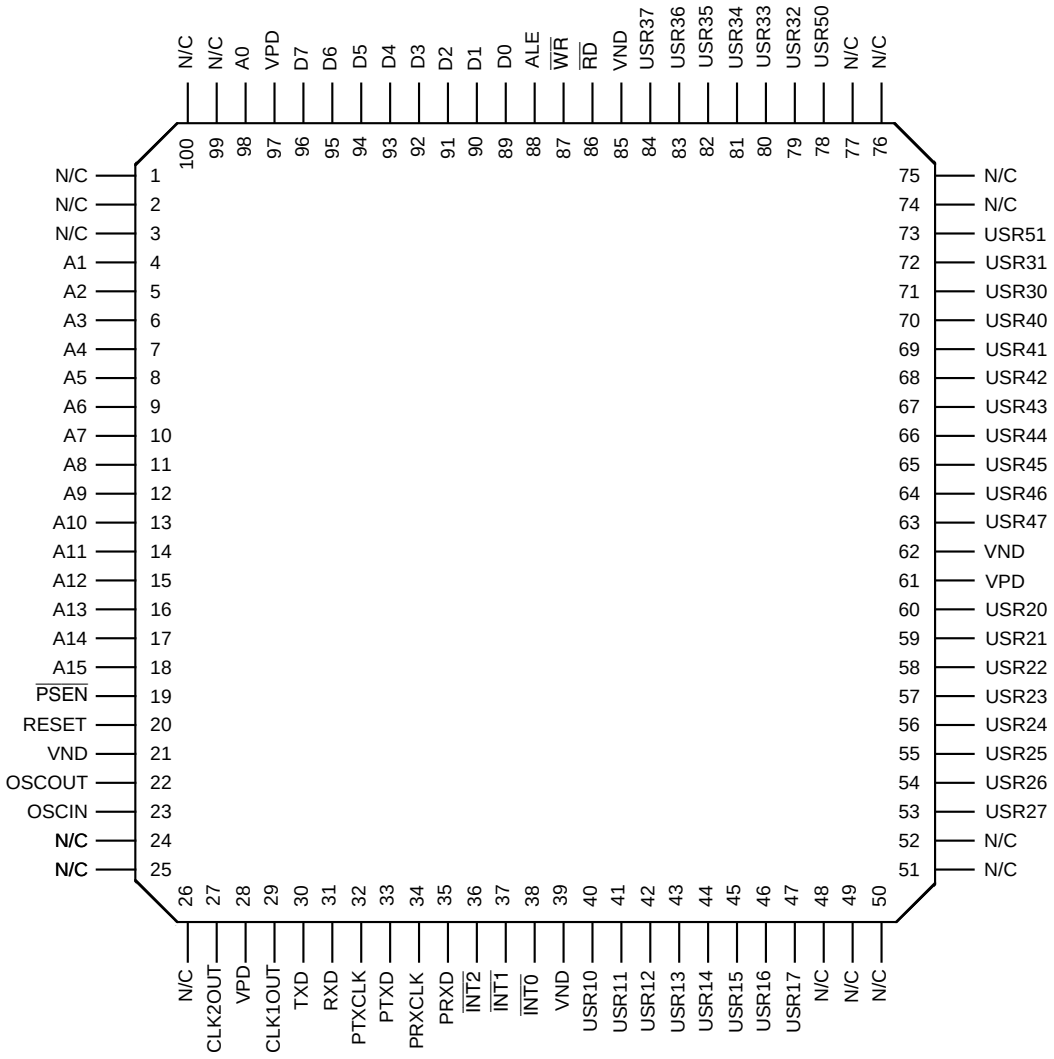


SSI 73M2910
Controller
100-Lead QFP

CAUTION: Use handling procedures necessary for a static sensitive component.

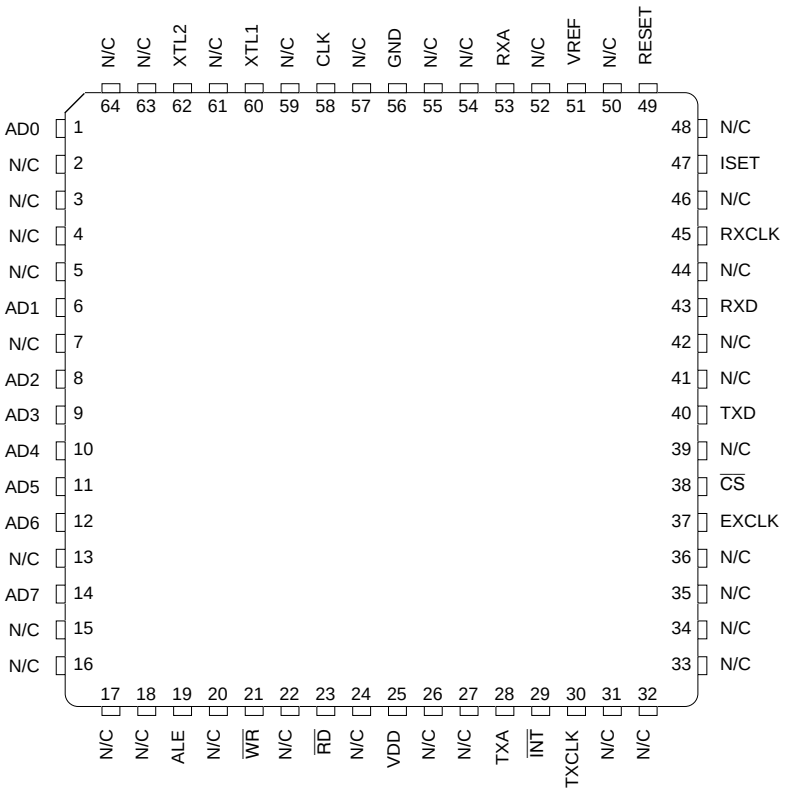
PACKAGE PIN DESIGNATIONS (continued)

(Top View)

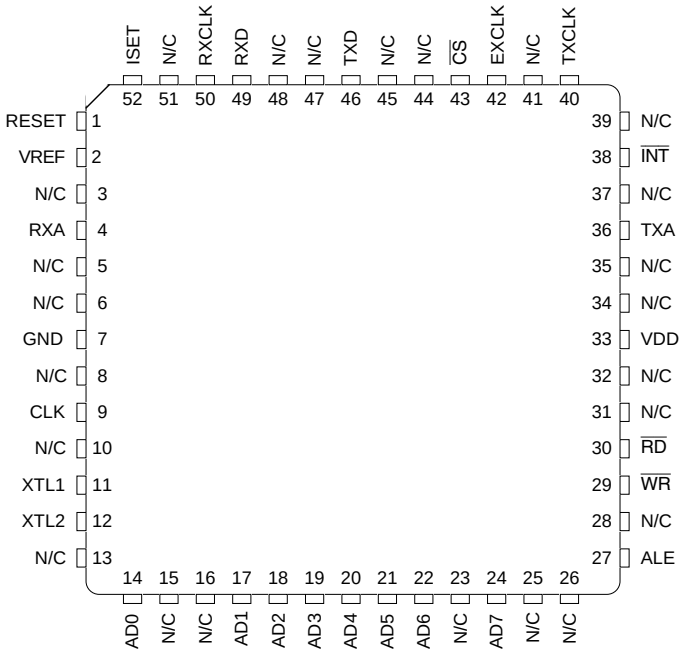


SSI 73M2910
Controller
100-Lead TQFP

CAUTION: Use handling procedures necessary for a static sensitive component.



SSI 73K224L
Single Chip Modem
64-Lead TQFP

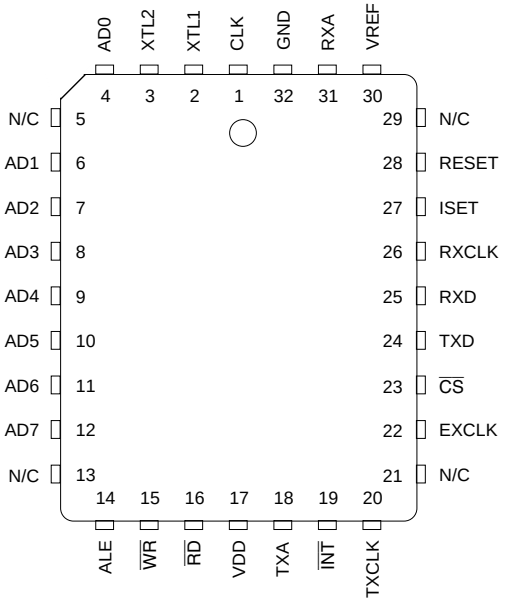


SSI 73K224L
Single Chip Modem
52-Lead QFP

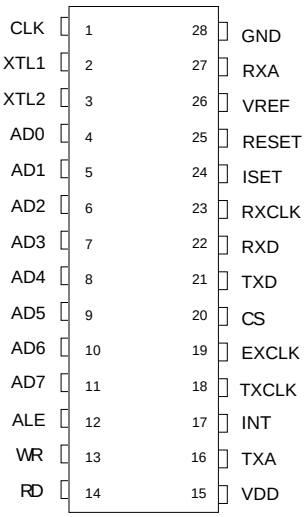
CAUTION: Use handling procedures necessary for a static sensitive component.

PACKAGE PIN DESIGNATIONS (continued)

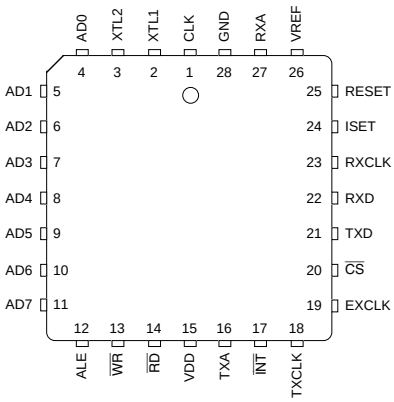
(Top View)



SSI 73K224L
Single Chip Modem
32-Pin PLCC



SSI 73K224L
Single Chip Modem
28-Pin DIP



SSI 73K224L
Single Chip Modem
28-Pin PLCC

CAUTION: Use handling procedures necessary for a static sensitive component.

Advance Information: Indicates a product still in the design cycle, and any specifications are based on design goals only. Do not use for final design.

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Thank you.

SSI 73M2910/2910A
Microcontroller

March 1996

DESCRIPTION

The SSI 73M2910/2910A high performance microcontroller is based on the industry standard 8-bit 8032 implemented in Silicon Systems' advanced submicron CMOS process. The processor has the same attributes of the 8032 including Instruction cycle time, UART, timers, interrupts, 256 bytes of on-chip RAM and programmable I/O. The architecture has been optimized for low power portable modem or communication applications by integrating unique features with the core CPU.

The main feature is a user friendly HDLC Packetizer, accessed through the special function registers. It has a serial I/O, hardware support for 16 and 32-bit CRC, zero insert/delete control, a dedicated interrupt and a clear channel mode for by-passing the packetizer.

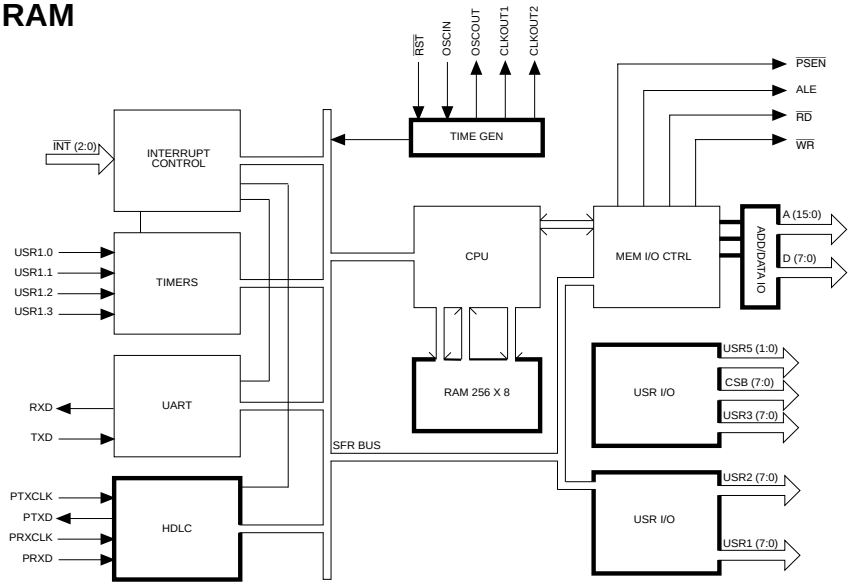
Other features include additional user programmable I/O with programmable bank select and chip select logic, designed to eliminate board level glue logic. It also includes two general purpose input ports with programmable wakeup capability.

For devices that require non-multiplexed address and data buses, eight latched outputs for the low byte of the address are available. (continued)

FEATURES

- **8032 compatible instruction set**
- **34 MHz Operation @ 4.5 – 5.5V**
- **44 MHz Operation @ 4.75 – 5.5V (2910A)**
- **22 MHz Operation @ 3.3 – 5.5V**
- **HDLC support logic (Packetizer, 16 and 32 CRC, zero ID)**
- **24 pins for user programmable I/O ports**
- **8 pins programmable chip select logic or I/O for memory mapped peripheral eliminating glue logic**
- **3 external interrupt sources (programmable polarity)**
- **16 dedicated latched address pins**
- **Multiplexed data/address bus**
- **Instruction cycle time identical to 8032**
- **Buffered oscillator (or OSC/2) output pin**
- **1.8432 MHz UART clock available**
- **Bank select circuitry to support up to 128k of external program memory**
- **100-Lead TQFP package available for PCMCIA applications**
- **Also available in 100-Lead QFP and 100-Pin PGA packages**

BLOCK DIAGRAM



DESCRIPTION (continued)

The SSI 73M2910/2910A has two extra interrupt sources, an external interrupt and a HDLC interrupt. The HDLC interrupt has two registers associated with it; the HDLC Interrupt Register which is used to determine the source of the interrupt, and the HDLC Interrupt Enable Register that enables the source of the interrupt.

The state of the external interrupts can be read through a register allowing the interrupt pins to be used as inputs. The interrupt pins INT0 and INT1 can be either negative edge, positive edge or level triggered. The INT2 pin is always edge triggered.

Two buffered clock outputs have been added to support peripheral functions such as UARTs, modems and other clocked devices. The main internal processor clock frequency can be divided by 2 for power conservation in functional modes that only require half the clock speed.

Additional internal special function registers are used for firmware control over the HDLC Packetizer, the clocks and the programmable I/O ports.

To accommodate processor peripherals when operating at 22 MHz the processor's timing has been altered somewhat to allow more address setup time for slower peripheral program ROM and memory mapped peripherals. This can offer the system designers an advantage when using higher (22 MHz) oscillator frequencies.

For low power applications the SSI 73M2910/2910A operates from 3 to 5 volts at 22 MHz and supports two power conservation modes: idle and power-down. In the power-down state the total current consumption is less than 10 μA at room temperature.

This device is offered in small form factor 100-Lead TQFP packages for PCMCIA applications and 100-Lead QFP packages.

DEVELOPER'S NOTE:

The SSI 73M2910/2910A is also available in a 100-Pin PGA package for system developers. The PGA package is more convenient and reliable for development emulation systems than the other package styles. Emulation systems for the SSI 73M2910/2910A are available through Signum Systems, 171 E. Thousand Oaks Blvd., #202, Thousand Oaks, CA 91360 (805) 371-4608.

8032 REFERENCE

This Document will describe the features unique to the SSI 73M2910/2910A. Please refer to an 8032 Programmer's Guide, Architectural Overview and Hardware Description for details on the instruction set, timers, UART, interrupt control, and memory structure.

REGISTER DESCRIPTION

INTERRUPTS

The core chip provides 8 sources of interrupt; 3 external interrupts, 3 timer interrupts, a serial port interrupt, and an HDLC interrupt. An external interrupt and an HDLC interrupt are unique to the SSI 73M2910/2910A. They do not exist in a normal 8032 product. Previously unused bits in the IE and IP registers are now serving functions for these additional interrupt sources. The interrupt vector addresses are as follows:

SOURCE	VECTOR ADDRESS
$\overline{\text{INT0}}$ (IE0)	003H
TF0	00BH
$\overline{\text{INT1}}$ (IE1)	013H
TF1	01BH
RI + TI	023H
TF2 + EXF2	02BH
$\overline{\text{INT2}}$ - ADDED INTERRUPT	033H
HDLC - ADDED INTERRUPT	03BH

The external interrupt sources, INT(2:0), come from dedicated input pins. The apparent polarity of these pins is individually controlled by bits in a special interrupt direction register, IDIR (address A9). The interrupt pins $\overline{\text{INT1}}$ and $\overline{\text{INT0}}$ can be either edge or level generated interrupts as indicated by bits 1 and 3 in the TCON Register (address 88). Pin $\overline{\text{INT2}}$ is always an edge generated interrupt. A flag is set when a falling transition (rising if IDIR bit 2 is set) on this pin is detected. This flag is automatically cleared when the interrupt is processed.

INTERRUPT ENABLE REGISTER (IE) SFR ADDRESS 0A8h
Bit Addressable
Reset State 00h

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
EA	EX2	ET2	ES	ET1	EX1	ET0	EX0

NOTE: Bit 6 differs from the 8032. This is a reserved bit in the 8032 and is used as a mask bit for external interrupt 2 in the core implementation. When bit 6 is set to a 0, external interrupt 2 is disabled.

The mask bit for the HDLC interrupt source is bit 0 of the HDLC Control Register.

INTERRUPT PRIORITY REGISTER (IP) SFR ADDRESS 0B8h
Bit Addressable
Reset State 00h

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
PHDLC	PX2	PT2	PS	PT1	PX1	PT0	PX0

NOTE: Bit 6 and bit 7 differ from the 8032. These are reserved bits in the 8032 and are used to determine the priority of external interrupt 2 and the HDLC in the core implementation. When bit 6 is set to a 1, the interrupt is set to the higher priority level.

INTERRUPTS (continued)

EXTERNAL INTERRUPT DIRECTION REGISTER (IDIR) SFR ADDRESS 092h
Byte Addressable
Reset State 00h

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
0	0	$\overline{INT2}$	$\overline{INT1}$	$\overline{INT0}$	INTD2	INTD1	INTD0

These bits determine the polarity of the corresponding external signals INT(2:0) which will result in an interrupt and will also allow the user to directly read the logic level at the pads INT(2:0).

BITS (5:3) INT(2:0)

Bits (5:3) are read only bits that reflect the logic value at the corresponding pin. The value is not affected by bits (2:0).

BITS (2:0) Interrupt Polarity Control

If the bit is set to a 0, a falling edge will trigger the interrupt. If the bit is set to a 1, a rising edge will trigger the interrupt. Also, if the bit is set to a 1, level generated interrupts will occur when the corresponding pin is high and the internal pin signal to the timer controls will be inverted.

Bits 6 and 7 will always be read as 0's.

CLOCK CONTROL REGISTER SFR ADDRESS 0DAh
Byte Addressable
Reset State 00h

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Activity	CLK1 CTRL1	MCLK CTRL	CLK2EN	CLK2 CTRL1	CLK2 CTRL0	CLK1EN	CLK1 CTRL0

These bits determine the behavior at the CLK1OUT and CLK2OUT pins and allow the user to divide the main internal processor clock frequency by two for power conservation.

BIT 7

Bit 7 is an activity bit. It is cleared by a read of this register. If the activity bit is set it will prevent the SSI 73M2910/2910A from entering sleep mode.

BIT 6

When bit 6 = 1, CLK1OUT will be OSC/1.5 if bit 1 is a 1 and bit 0 is 0.

BIT 5	CLOCK OUT
0	OSC
1	OSC/2

BIT 5 Master Clock Control

When bit 5 is set to a 1 the internal processor clock is the oscillator frequency divided by 2. If this bit is a 0, the processor clock is the same frequency as the oscillator's.

BIT 4 Clock 2 Output Enable

Bit 4 enables the clock at the CLOCK 2 output pin if it is set to a 1. The CLOCK 2 pin output is held to a 0, by writing this bit to a 0. This will reduce system power if the clock pin is not used or if a power reduction mode is required.

BITS 3,2 Clock 2 Output Control

These bits determine the oscillator divisor for the CLOCK 2 output pin. They were designed to provide a 1.8432 MHz clock for an external UART given an oscillator frequency of 11.0592 MHz, 22.1184 MHz, 18.432 MHz, or 13.824 MHz.

BIT 3	BIT 2	CLK 2 OUT	OSC FREQUENCY
0	0	OSC/7.5	13.824 MHz
0	1	OSC/6	11.059 MHz
1	0	OSC/12	22.118 MHz
1	1	OSC/10	18.432 MHz

BIT 1 Clock 1 Output Enable

Bit 1 enables the clock at the clock 1 output pin if it is set to a 1. The clock pin output is held to a 0, by writing a 0 to this bit. This will reduce system power if the clock pin is not used or if a power reduction mode is required.

Bit 6 is cleared to a 0 upon a reset.

BIT 0 Clock 1 Output Control

Bit 0 controls the frequency of the clock 1 output pin. The clock output is either the oscillator's output signal divided by two or a buffered oscillator output signal.

POWER SAVING MODES

Low Power Modes

The SSI 73M2910/2910A supports two power conservation modes, which are controlled by the PCON.1 and PCON.0 control bits of the PCON Register.

If PCON.0 is set, the SSI 73M2910/2910A will go into a power saving mode where the oscillator is running, clocks are supplied to the UART, timers, HDLC, and interrupt blocks, but no clocks are supplied to the CPU. Instruction processing and activity on the address and data ports is halted. Normal operation is resumed when an unmasked interrupt is requested or when a reset occurs.

If PCON.1 is set, the SSI 73M2910/2910A goes into its lowest power mode where the oscillator is halted. The total current consumption in this state should be less than 10 μa. The SSI 73M2910/2910A will start its oscillator and begin to return to normal operation when either a reset occurs, when a falling (rising if corresponding direction bit is set) edge of an unmasked external interrupt from pins $\overline{\text{INT}}$(2:0) is detected, or when the USR5 (1:0) pins change to a state according to the USR5 port register. Edges used in wakeup modes are not filtered in the SSI 73M2910/2910A, so the user must be cautious of noise or small glitches inadvertently waking up the chip. From the time the edge that results in the wake up occurs, to the point at which an instruction is executed, depends on the oscillator start-up time. Three good oscillator pulses must be detected before the main internal clocks are generated.

During power-down mode, both the ALE and $\overline{\text{PSEN}}$ pins are pulled high since these signals often provide the output enable and chip enable for the ROM (active low). This ensures that the external components are in their lowest power state.

REGISTER DESCRIPTION (continued)

USR PROGRAMMABLE I/O

Port Control USR1, USR2, USR3, USR4, USR5

The core chip provides 32 user I/O pins. Each pin is programmed separately as either an input or as an output by a bit in a direction register. If the bit in the direction register is set to a 1, the I/O control will treat the corresponding pin as an input. If it is a 0, the pin will be treated as an output whose value is determined by the port data register. The USR1 and USR2 port registers are accessed through the internal SFR bus. The USR3 and USR4 ports are accessed through the external memory bus by a MOVX instruction. The USR4 port provides the user with an automatic chip select function if selected by the user. If the user does not require some (or any) of the chip select pin options, he may program the USR4 port pins to operate in the same way as USR3 port pins.

The USR Data Register contents determine pin values if chosen as an output. When reading from the data register's SFR address, the pin logic values are returned as data except when the port address is the destination address for a read-modify-write instruction. In this case, the latched register values are returned as data. When reading data from a data register that is mapped in the external memory space, the pin values are always returned as data.

The USR5 Register allows for 2 additional input pins. In normal operation these pins can be used as general purpose inputs. In power-down mode, the user can program either rising or falling transitions or logical combinations of these pins to wake up the chip.

USR 1 PORT

USR1 DATA SFR Address 90h
Bit Addressable
Reset State 00h

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
USR1.7	USR1.6	USR1.5	USR1.4	USR1.3	USR1.2	USR1.1	USR1.0

Bits in this register will be asserted on the USR1(7:0) pins if the corresponding direction register bit is a 0. Reading this SFR's address will return data reflecting the values of pins USR1(7:0) except when address 90h is the destination address for a read-modify-write instruction. In this case, the latched register values are returned as data.

USR1 port signals are also used as timer controls. In applications where the external signals are required for timer count modes, the corresponding port pin should be configured as an input.

USR1.0 bit = TIMER0 T0 PIN
USR1.1 bit = TIMER1 T1 PIN
USR1.2 bit = TIMER2 T2 EX PIN
USR1.3 bit = TIMER2 T2 PIN

USR1 Port Direction (DIR1) SFR Address 91h
Byte Addressable
Reset State FFh

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
DIR1.7	DIR1.6	DIR1.5	DIR1.4	DIR1.3	DIR1.2	DIR1.1	DIR1.0

This register is used to designate the USR1 pins as either inputs or outputs. If the register bit is reset to a 0, the corresponding USR1 pin is programmed as an output that will be driven by the corresponding USR1 data register bit. If the register bit is a 1, the corresponding pin will be treated as an input.

After a reset, the USR1 pins will present a high impedance output state and the input values will not be driven from the pin, but will be driven to a 1 internally. The pins will assume normal I/O operation once the processor has written the port direction register. This feature will ensure a low current state at reset (you don't want to drive out against external inputs, and you don't want floating inputs).

USR2 PORT

USR2 Port Data SFR Address 0D8H
Bit Addressable
Reset State 00h

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
USR2.7	USR2.6	USR2.5	USR2.4	USR2.3	USR2.2	USR2.1	USR2.0

Bits in this register will be asserted on the USR2(7:0) pins if the corresponding direction register bit is a 0. Reading this SFR's address will return data reflecting the values of pins USR2(7:0) except when address 0D8h is the destination address for a read-modify-write instruction. In this case, the latched register values are returned as data.

USR2 Port Direction (DIR2) SFR Address 0D9H
Byte Addressable
Reset State FFh

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
DIR2.7	DIR2.6	DIR2.5	DIR2.4	DIR2.3	DIR2.2	DIR2.1	DIR2.0

This register is used to designate the USR2 pins as either inputs or outputs. If the register bit is reset to a 0, the corresponding USR2 pin is programmed as an output that will be driven by the corresponding USR2 I/O data register bit. If the register bit is a 1, the corresponding pin will treated as an input.

After a reset, the USR2 pins will present a high impedance output state and the input values will not be driven from the pin, but will be driven to a 1 internally. The pins will assume normal I/O operation once the processor has written the port direction register. This feature will ensure a low current state at reset (you don't want to drive out against external inputs, and you don't want floating inputs).

USR3 PORT

USR3 Port Data External address 0000h
Byte Addressable
Reset State 00h

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
USR3.7	USR3.6	USR3.5	USR3.4	USR3.3	USR3.2	USR3.1	USR3.0

Bits in this register will be asserted on the USR3(7:0) pins if the corresponding direction register bit is a 0. Reading this SFR's address will return data reflecting the values of pins USR3(7:0).

If the bank select feature is chosen, the USR3.7 pin acts as address bit 17 and USR3 data bit 7 is ignored.

USR3 PORT (continued)

USR3 I/O Port Direction (DIR3) External Address 0001h
Byte Addressable
Reset State FFh

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
DIR3.7	DIR3.6	DIR3.5	DIR3.4	DIR3.3	DIR3.2	DIR3.1	DIR3.0

This register is used to designate the USR3 pins as either inputs or outputs. If the register bit is reset to a 0, the corresponding USR3 pin is programmed as an output that will be driven by the corresponding USR3 data register bit. If the register bit is a 1, the corresponding pin will be treated as an input.

After a reset, the USR3 pins will present a high impedance output state and the input values will not be driven from the pin, but will be driven to a 1 internally. The pins will assume normal I/O operation once the processor has written the USR3 port direction register. This feature will ensure a low current state at reset.

If the bank select feature is chosen, USR3.7 pin is forced to be an output.

BANK SELECT (BNKSEL) EXTERNAL ADDRESS 0002h
Byte Addressable
Reset State 00h

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
B7	B6	B5	B4	B3	BSEN	BS1	BS0

This register is used to accommodate systems where more than 64 kBytes (up to 128 kBytes) of program memory are required. Pin USR3.7 acts as an address pin, A16, if BSEN is set to a 1 and the processor is fetching an instruction and not data memory. If BSEN is set to a 1, A15 is also modified during instruction fetches as shown below. If BSEN is a 0, no alterations to address bit A15 are made, and pin USR3.7 is a function of USR3 bit 7 and DIR3 bit 7.

Bits (7:3) are general purpose read/write register bits.

A15	Value of the 16th address bit as it appears at pin A15.
A15'	Address from port 2 internal logic, the value that will appear as the most significant address bit if no bank select feature is chosen.
A16	Value of the 17th and MSB of the instruction address seen at the USR3.7 port pin, if the bank select feature is selected. If the bank select feature is not selected, USR3.7 acts as a normal USR3 I/O port pin.

BSEN	BS1	BS0	A15'	A15	A16	ADDRESS
0	*	*	0	0	USR3.7	0K - 32K
0	*	*	1	1	USR3.7	32K - 64K
1	0	0	0	0	0	0K- 32K
1	0	0	1	1	0	32K - 64K
1	0	1	0	0	0	0K - 32K
1	0	1	1	0	1	64K - 96K
1	1	0	0	0	0	0K - 32K
1	1	0	1	1	1	96K- 128K
1	1	1	0	0	0	0K- 32K
1	1	1	1	0	1	64K - 96K

* = Don't care

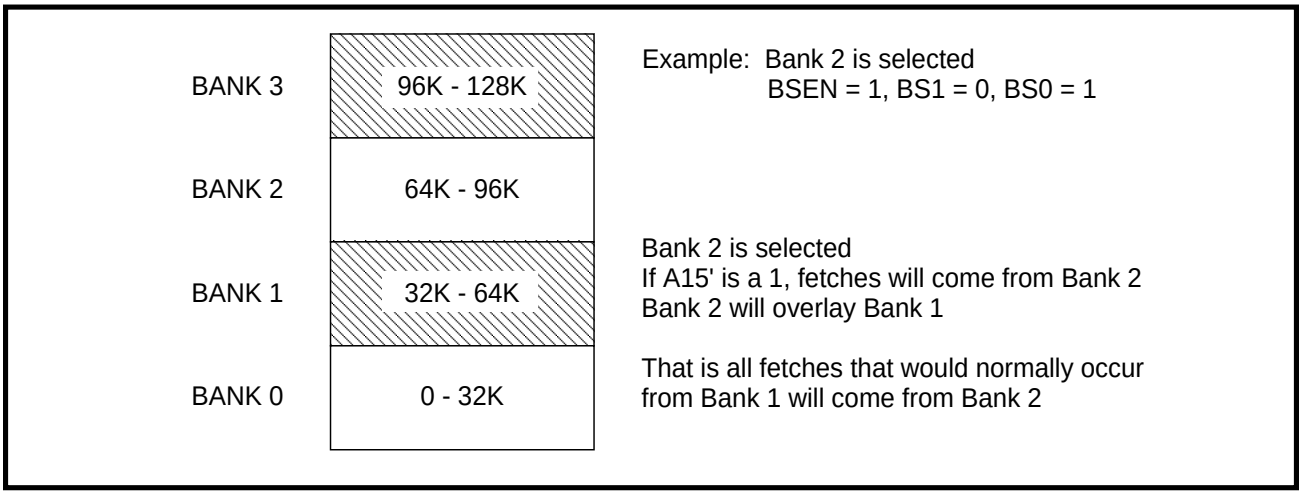


FIGURE 1: Bank Select

USR PROGRAMMABLE I/O (continued)

USR4 PORT

USR4 Port Data External Address 0003h
Byte Addressable
Reset State 00h

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
USR4.7	USR4.6	USR4.5	USR4.4	USR4.3	USR4.2	USR4.1	USR4.0

Bits in this register will be asserted on the USR4(7:0) pins if the corresponding direction register bit is a 0 and if the corresponding bit in the Chip Select Enable Register, 0005, is set to a 0. Reading this register will return data reflecting the values of pins USR4(7:0).

USR4 I/O Port Direction (DIR4) External Address 0004h
Byte Addressable
Reset State FFh

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
DIR4.7	DIR4.6	DIR4.5	DIR4.4	DIR4.3	DIR4.2	DIR4.1	DIR4.0

This register is used to designate the USR4 pins as either inputs or outputs. If the register bit is reset to a 0, the corresponding USR4 pin is programmed as an output that will be driven by the corresponding USR4 I/O data register bit if the corresponding bit in the Chip Select Enable Register, 0005, is set to a 0. If the register bit is a 1, the corresponding pin will treated as an input only if the corresponding bit in register 0005 is set to a 0.

After a reset, the USR4 pins will act as chip select outputs.

USR4 Port Chip Select Enable (CSEN) External Address 0005h
Byte Addressable
Reset State FFh

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
CSEN 7	CSEN 6	CSEN 5	CSEN 4	CSEN 3	CSEN 2	CSEN 1	CSEN 0

This register is used to designate the USR4 pins as either user programmable I/Os or as chip select (CS0B - CS7B) functions on a pin by pin basis. This feature is designed to help reduce external glue logic for peripheral memory mapped devices. The chip select function is programmed by setting the appropriate bits in the CSEN Register. When a chip select pin is enabled by setting the corresponding CSEN bit to a 1, all data and direction information from registers 0003 and 0004 for this bit are ignored and the selected port becomes an output. If the bit is reset to a 0, the pin will be treated as a normal programmable user I/O pin as defined by registers 0003 and 0004.

The chip select pins have a defined memory map. The intent is that the outputs can be wire OR'ed together for a flexible selection of peripheral chip selects. All chip selects will be disabled (forced to a logic 1. It is assumed that all chip selects are active low) after the read or write is completed, and the appropriate chip select will be enabled as the next new external addresses is asserted. After a reset, the CSB pull-up devices are all enabled, that is, all chip select outputs are high. Users must account for this if these pins are intended to be general purpose I/Os.

The chip selects partition a 64K memory space as follows:

CHIP SELECT PIN	ADDRESS	# BYTES
RESERVED FOR INTERNAL USE	0000H - 00FFH	256
CS0 (USR4.0)	0100H - 01FFH	256
CS1 (USR4.1)	0200H - 03FFH	512
CS2 (USR4.2)	0400H - 07FFH	1K
CS3 (USR4.3)	0800H - 0FFFH	2K
CS4 (USR4.4)	1000H - 1FFFH	4K
CS5 (USR4.5)	2000H - 3FFFH	8K
CS6 (USR4.6)	4000H - 7FFFH	16K
CS7 (USR4.7)	8000H - FFFFH	32K

NOTE: External addresses 0000H-00FFH may not be read. These are reserved for SSI 73M2910/2910A internally defined registers

USR5 PORT

USR5 Port Register External Address 0006h
Byte Addressable
Reset State 60h

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
USR5EN	USR5.0	USR5.1	POL5.0	POL5.1	ACTE0	ACTE1	AND01

This register allows user programmable wakeup capability. If this is not required, this register can be used to read external signals at the USR5.1 and USR5.0 pins.

Bit 7 USR5 Input Port Enable

Bit 7 is used to enable the USR5.1 and USR5.0 input circuitry. If this bit is a 0, the USR5 pin output circuitry is driven to a known level internally and any signal level at the pin is ignored. When set to a 1 the pin input circuitry is enabled and the values of these pins are reflected in bits 6 and 7. If these pins are not connected at the board level, this bit should remain at a 0 to keep the pin input circuitry from drawing unnecessary current.

The USR5 Register can be programmed such that a transition (bit 4 determines rising or falling) of USR5.0, a transition (bit 3 determines rising or falling) of USR5.1, or the logical combination of USR5.0 (bit 4 determines high or low level) AND USR5.1 (bit 3 determines high or low level) can wakeup the processor from its power-down mode.

BIT 6 USR5.0

Bit 6 reflects the value of chip pin USR5.0 if the USR5EN bit is set to a 1.

BIT 5 USR5.1

Bit 5 reflects the value of chip pin USR5.1 if the USR5EN bit is set to a 1.

USR5 PORT (continued)

BIT 4 USR5.0 Polarity

Bit 4 determines which edge or level is used in the wakeup detection circuit. A low level selects a rising transition and the true pin value of USR5.0 to the wakeup detection circuit. When this bit is set to a 1, a falling transition and complemented USR5.0 value is presented to the wakeup detection circuit.

BIT 3 USR5.1 Polarity

Bit 3 determines which edge or level is used in the wakeup detection circuit. A low level selects a rising transition and the true pin value of USR5.1 to the wakeup combinatorial circuit. When this bit is set to a 1, a falling transition and complemented USR5.1 value is presented to the wakeup detection circuit.

BIT 2 USR5.0 Edge Activity Enabled

When bit 2 is set to a 1, a transition of USR5.0 of the appropriate level as dictated by bit 4, will wake up the processor. If this bit is reset to a 0, edge activity on this pin is ignored.

BIT 1 USR5.1 Edge Activity Enabled

When bit 1 is set to a 1, a transition of USR5.0 of the appropriate level as dictated by bit 3, will wake up the processor. If this bit is reset to a 0, edge activity on this pin is ignored.

BIT 0 Combinatorial AND of USR5.0 and USR5.1 Level Enabled

When bit 0 is set to a 1, the value USR5.0 or its complimented value as dictated by bit 3, AND'ed with the value USR5.1 or its complimented value as dictated by bit 2, will wake up the processor. If this bit is reset to a 0, the levels of USR5.0 and USR5.1 are ignored.

USR5.0	USR5.1	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0	WAKEUP
*	*	*	*	0	0	0	NO
0-1	*	0	*	1	*	*	YES
1-0	*	1	*	1	*	*	YES
*	0-1	*	0	*	1	*	YES
*	1-0	*	1	*	1	*	YES
0	0	1	1	*	*	1	YES
1	0	0	1	*	*	1	YES
0	1	1	0	*	*	1	YES
1	1	0	0	*	*	1	YES

* = Don't care

HDLC PACKETIZER

REGISTER	ADDRESS	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
HDLC CONTROL 0 (HDLC0)	C0	WRXD	WPTXD	TXD	PRXD	RXD CTRL1	RXD CTRL0	PTXD CTRL1	PTX CTRL0
HDLC CONTROL 1 (HDLC1)	C1	RESET	CCIT	CRC PRE	RXCRC32	RXCRC16	TXCRC32	ZERO ID	HDLC INTEN
HDLC TX CONTROL (HTXC)	C2	0	0	0	DIV16 CLK	SEND ABORT	SEND CRC	SEND DATA	SEND FLAG
HDLC STATUS (HSTAT)	C3	INVAL CRC32	INVAL CRC16	TX UNDERRUN	RX UNDERRUN	INVAL FLAG	ABORT DETECT	IDLE DETECT	FLAG DETECT
HDLC INT ENABLE (HIE)	C4	TX RDY IE	RX RDY IE	TX RDY EN	RX RDY EN	INVAL FLAG IE	ABORT IE	IDLE IE	FLAG IE
HDLC INT SOURCE (HINT)	C5	0	0	0	0	0	NEW STATUS	RX READY	TX READY
RX DATA (RXD)	C6	RXDAT7	RXDAT6	RXDAT5	RXDAT4	RXDAT3	RXDAT2	RXDAT1	RXDAT0
TX DATA (TXD)	C7	TXDAT7	TXDAT6	TXDAT5	TXDAT4	TXDAT3	TXDAT2	TXDAT1	TXDAT0

FIGURE 2: HDLC SFR Registers

HDLC CONTROL REGISTERS

HDLC CONTROL REGISTER 0 (HDLC0) SFR ADDRESS 0C0h

Bit Addressable Reset State 00XX 0000 b
Bits 5 and 4 are read only bits

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
WRXD	WPTXD	TXD R	PRXD R	RXD CTRL1	RXD CTRL0	PTX CTRL1	PTX CTRL0

This register controls the basic set-up of the DTE and modem pins RXD, TXD, PRXD, and PTXD.

BIT 7 WRXD

Bit 7 allows the processor to write directly to the SSI 73M2910/2910A RXD output pin. The value of bit 7 will appear at the RXD pin only if bit 3 is a 1 and bit 2 is a 1.

BIT 6 WPTXD

Bit 6 allows the processor to write directly to the SSI 73M2910/2910A PTXD output pin. The value of bit 6 will appear at the PTXD pin only if bit 1 is a 1 and bit 0 is a 0.

BIT 5 TXD

Bit 5 is a read only bit that reflects the value at the SSI 73M2910/2910A TXD input pin.

BIT 4 PRXD

Bit 4 is a read only bit that reflects the value at the SSI 73M2910/2910A PRXD input pin.

HDLC CONTROL REGISTER 0 (HDLC0) SFR ADDRESS 0C0h (continued)

BITS 3,2 RXD Control

Bit 3 and bit 2 control the source of the SSI 73M2910/2910A RXD output pin. This output goes to the DTE's RS232 interface. The source of this signal can be the core's UART TXD output, the PRXD output from a modem peripheral (clear channel), the DTE's TXD (echo), or the value written into bit 7 of this register.

BIT 3	BIT 2	RXD OUTPUT
0	0	UART TXD Output
0	1	PRXD Buffered (clear channel)
1	0	TXD Buffered (echo)
1	1	WRXD (bit 7)

BITS 1,0 PTXD Control

Bit 1 and bit 0 control the source of the SSI 73M2910/2910A PTXD output pin. This output goes to the modem's TX data input. The source of this signal can be the core's HDLC TX output, the DTE's TXD output (clear channel), or the value written into bit 6 of this register.

BIT 1	BIT 0	PTXD OUTPUT
0	0	HDLC TX Output
0	1	TXD Buffered (clear channel)
1	0	WPTXD (bit 6)
1	1	0

HDLC CONTROL REGISTER 1 (HDLC1) SFR ADDRESS 0C1h
Byte Addressable
Reset State 00h

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
HDLC RST	CCITT	CRC PRE	RXCRC 32	RXCRC 16	TXCRC CTRL	ZERO ID	HDLC INTEN

This register controls the basic set-up of the HDLC block. This register will be written during initialization and not during normal message processing.

BIT 7 HDLC Software Reset

When bit 7 is a 1, the HDLC circuit is reset and held in a low power state and no interrupts from the HDLC circuitry will be generated. When a 0 is written to this bit, the HDLC circuit will behave according to its control bits. Bit 7 and the power-on-reset signal are OR'ed together to form a reset signal for the HDLC block.

Bit 7 is cleared to a 0 upon a power-up-reset.

BIT 6 CRC Type Control

Bit 6 selects the CRC algorithm used in the 16-bit CRC calculation. There are two types of 16-bit CRCs commonly used, CRC16 and the CCITT 16-bit CRC. If this bit is set to a 1, the CCITT type is selected.

Bit 6 is cleared to a 0 upon a reset.

BIT 5 CRC Preset Value

Bit 5 selects the reset value for the CRC generator and receiver. If this bit is set to a 1, the CRC generator and receiver are initialized to ones and if this bit is reset to a 0, they are initialized to 0s. This bit should be set to a 1 for most CCITT polynomials.

Bit 5 is cleared to a 0 upon a reset.

BITS 4,3 RX CRC Control

Bit 4 and bit 3 determine the type of CRC remainder that will be checked at the end of a received frame. There is a 16-bit CRC, and a 32-bit CRC that the HDLC block can support. If both bit 4 and bit 3 are reset, bits 7 and 6 of the HDLC Status Register will be held to a 0. If both bit 4 and bit 3 are 1s, a special CRC search mode is enabled where both bits 7 and 6 of the HDLC Status Register are enabled. This mode is used during a connection to determine which CRC is used by the initiating modem. If the 16-bit CRC remainder is not matched at the end of the received frame, then bit 6 of the HDLC Status Register is set. If the 32-bit CRC remainder is not matched at the end of the received frame, then bit 7 of the HDLC Status Register is set. Once the correct CRC type is established during a connection, either bit 4 or bit 3 should be set to a 1 enabling the appropriate invalid CRC status bit.

BIT 4	BIT 3	CRC TYPE
0	0	NO CRC Check
0	1	Enable CRC16 Status
1	0	Enable CRC32 Status
1	1	Enable CRC16 Status and CRC32 Status

BIT 2 TXCRC Control

Bit 2 controls the CRC type to be transmitted. If bit 2 is reset to a 0, a 16-bit CRC will be transmitted with the SEND CRC command. If bit 2 is set to a 1, a 32-bit CRC will be transmitted.

BIT 1 Zero Insert/Delete Control

When bit 1 is set to a 1, a 0 will be transmitted if either the send data or send CRC bits of the HDLCTX control are set after five consecutive 1s have been transmitted. Also, when this bit is set, a 0 will be removed from the received data stream if it immediately follows a pattern of a 0 followed by five consecutive ones. If bit 1 is reset to a 0, no 0s will be inserted during transmission, and no 0s will be deleted during reception.

Bit 1 is cleared to a 0 upon a reset.

BIT 0 HDLC Interrupt Enable

When bit 0 is reset to a 0, the HDLC will be prevented from generating an interrupt. The status bits that indicate the source of the interrupt can still be set allowing the HDLC block to be serviced in a polled mode.

Bit 0 is cleared to a 0 upon reset.

HDLC CONTROL REGISTERS (continued)

HDLC TX CONTROL REGISTER (HTXC) SFR ADDRESS 0C2h
Byte Addressable
Reset State 00h

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
0	0	0	DIV16 CLK	SEND ABORT	SEND CRC	SEND DATA	SEND FLAG

This register is used to control the source of data that appears on the PTXD pin. Bits are shifted out on every rising edge of the PTXCLK pin input. If no control bits are set, or more than one TX control bit is set, the PTXD pin will go to a binary 1.

BITS 7-5 Always 0

BIT 4 16X Clock Select

Under normal synchronous operation, the PTXCLK and PRXCLK are used to receive and transmit data PRXD and PTXD. The clock rate is equal to the data rate. In asynchronous modes, a clock 16 times the bit rate is provided at PTXCLK and PRXCLK.

When bit 4 is set to a 1 during asynchronous operation, the clocks at the PTXCLK and PRXCLK input pins are divided by 16 to provide transmit and receive shift clocks. An internal clock for sampling incoming PRXD data is synchronized by detecting any edge on the PRXD data pin. The rising edge of this internal clock, used to sample incoming data, is delayed from the falling data edge by 8 PRXCLK periods and will continue at this phase and at a PRXCLK/16 frequency until another PRXD edge is detected.

If bit 4 is reset to a 0, the rising edge of PTXCLK is used to sample the data at PRXD, and the falling edge of PTXCLK is used to shift new data onto PTXD.

BIT 3 Abort

When bit 3 is set to a 1, a series of consecutive ones will immediately be transmitted through the PTXD pin on every falling edge of PTXCLK. The message will have been aborted after 2 TX ready interrupts are received. No zeros will be inserted during the abort transmission.

BIT 2 Send CRC

When bit 2 is set, the bytes in the TX CRC generator will be inverted and serially transmitted to the PTXD output on the falling edge on PTXCLK as soon as the present data byte transmission is completed. If bit 1 of the HDLC Control Register is a 0, a 0 will be inserted into the CRC data stream after five consecutive ones are transmitted. As soon as the last bit of the CRC is sent, a series of flags will be automatically sent until another TX control bit is set. No TX ready interrupts will be generated during the transmission of the CRC bytes. A TX ready interrupt will be generated as the first bit of each flag byte is transmitted indicating that the CRC transmission has been completed. This should be cleared by a dummy write to the TX Data Register.

BIT 1 Send Data

When bit 1 is set, the data is the TX Data Register will be serially transmitted through the PTXD pin on every falling edge of PTXCLK, LSB first. If bit 1 ofthe HDLC Control Register is a 0, a 0 will be inserted into the data stream after five consecutive 1s are transmitted. After all eight data register bits have been sent, the HDLC will continue to send data by loading the parallel serial transmit register with new transmit register data, unless either a TX underrun is detected or one of the other TX control bits has been set. This bit will be cleared by the HDLC circuitry as soon as a TX underrun is detected. A TXRDY interrupt will be generated as the first data of each data byte is transmitted. Bit 1 will be cleared to a 0 upon a reset.

BIT 0 Send Flag

When bit 0 is set, a pattern of 7E will be transmitted to the PTXD output as soon as either the next data byte or CRC has completed transmission. No 0s will be inserted during the flag transmission. When bit 0 is reset back to a 0, the HDLC circuitry will complete the flag byte in progress and then transmit according to bits in the TX Control Register. TX ready interrupts will be generated as each byte of flag transmission is initiated.

HDLC STATUS REGISTER (HSTAT) SFR ADDRESS 0C3h
Byte Addressable
Read Only Register
Reset State 00h

If any of the HDLC status bits are set, bit 1 of the HDLC Interrupt Register (new status) will be set if the corresponding bit in the HDLC Interrupt Enable Register is set.

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
INVAL CRC32	INVAL CRC16	TX UNDRN	RX OVRN	INVAL FLAG	ABORT DET	IDLE DET	FLAG DET

BIT 7 Invalid CRC 32

Bit 7 will be set if the CRC search mode or the 32-bit CRC is enabled by the HDLC Control Register and an incorrect remainder for the 32-bit CRC is detected at the last received byte prior to receiving a flag.

Bit 7 will by cleared upon a reset and is cleared by a read of the HDLC Stat Register.

BIT 6 Invalid CRC 16

Bit 6 will be set if the CRC search mode or the 16-bit CRC is enabled by the HDLC Control Register and an incorrect remainder for the 16-bit CRC is detected at the last received byte prior to receiving a flag.

Bit 6 will by cleared upon a reset and is cleared by a read of the HDLC Stat Register.

BIT 5 TX Underrun

When Bit 5 is set, a transmit underrun condition has been detected. This is a condition where the HDLC has finished transmitting a message byte, but no new data has been loaded into the TX Data Register, and no other transmit control bit has been set. This bit will be set only if the send data bit, bit 1 of the TX Control Register is set. The transmit data is double buffered since the TX Data Register is downloaded into a TX Serial Register when the HDLC begins to transmit a new data byte. At the time of loading the TX Serial Register, a TX ready interrupt is generated. This interrupt must be serviced by either loading a new data byte (the next data byte to be transmitted) into the TX Data Register, or by setting another TX control bit, before the current data byte has completed transmission (at which point another TX ready interrupt would be generated). If a TX underrun is detected, the HDLC will abort the current transmission by sending continuous ones and will reset the send data control bit in the TX Control Register.

Bit 5 will by cleared upon a reset and is cleared by a read of the HDLC Stat Register.

HDLC STATUS REGISTER (HSTAT) SFR ADDRESS 0C3h (continued)

BIT 4 RX Overrun

When bit 4 is set, a receive overrun condition has been detected. This is a condition where the HDLC has received a new byte, but the last received data byte has not yet been read from the RX Data Register. As soon as a new data byte has been received in an eight-bit serial register, it is loaded into the RX Data Register and a new RX data interrupt is generated. If this interrupt is not serviced by reading the RX Data Register during the time another new data byte is received, the RX overrun status bit will be set. The new received data will not overwrite the older unread data.

Bit 4 will by cleared upon a reset and is cleared by a read of the HDLC Stat Register.

BIT 3 Invalid Flag

When bit 3 is set, an invalid flag has been detected. This is a condition where a 7E pattern with no inserted 0s is detected, and this pattern did not originate on a byte boundary. Note, two consecutive flags may share a 0, so that the second (or subsequent) flag may not appear to be on a byte boundary. This condition does not result in an invalid flag indication.

Bit 3 will by cleared upon a reset and is cleared by a read of the HDLC Stat Register.

BIT 2 Abort Detect

When bit 2 is set, an abort condition has been detected. This is a condition where seven consecutive ones, with no inserted zeros, are received after an active state. Bit 2 will be cleared upon a reset and is cleared by a read of the HDLC Stat Register.

BIT 1 Idle Detect

When bit 1 is set, the first indication of an idle state is detected. An idle state is declared when 15 consecutive ones, with no inserted zeros, are received after an active state.

Bit 1 will be cleared upon a reset and is cleared by a read of the HDLC Stat Register.

BIT 0 Flag Detect

When bit 0 is set, the HDLC has received a 7E pattern with no inserted 0's. Bit 0 will by cleared upon a reset and is cleared by a read of the HDLC Stat Register.

HDLC INTERRUPT ENABLE REGISTER (HIE) SFR ADDRESS 0C4h
Byte Addressable
Reset State 00h

If the bit is set, the corresponding interrupt source is enabled.

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
TX RDY IE	RX RDY IE	TX RDY EN	RX RDY EN	INVAL FLG IE	ABORT IE	IDLE IE	FLAG IE

BIT 7 Transmitter Ready Interrupt Enable

When bit 7 is set, an HDLC interrupt will be generated if bit 0 (TX RDY) of the HDLC Interrupt Register is also set. If bit 7 is reset to a 0, no HDLC interrupt indication will be given as TX RDY is set. This interrupt enable allows the TX RDY to be a polled bit. Note that bit 5 of this register is a pre-mask to the TX RDY bit, that is, it will prevent the TX RDY bit from ever being set.

BIT 6 Receiver Ready Interrupt Enable

When bit 6 is set, an HDLC interrupt will be generated if bit 1 (RX RDY) of the HDLC Interrupt (HINT) Register is also set. If bit 6 is reset to a 0, no HDLC interrupt indication will be given as RX RDY is set. This interrupt enable allows the RX RDY to be a polled bit. Note that bit 4 of this register is a pre-mask to the RX RDY bit, that is, it will prevent the RX RDY bit from ever being set.

BIT 5 Transmit Ready Enable

Bit 5 is used to enable the TX RDY and TX underrun interrupt sources. When bit 5 is set, the transmitter ready indication will set bit 0 of the HDLC Interrupt Register. The TX RDY indication will go active as the first bit of a message byte is being transmitted, except during CRC transmission. Also, if this bit is set, the TX underrun condition will result in a new status interrupt. If bit 5 is reset to a 0, bit 0 of the HDLC Interrupt Register will not be set, and no corresponding HDLC interrupt will be generated. Also, a TX underrun condition, as indicated by bit 5 of the HDLC Status Register, will not result in an HDLC interrupt or in setting the new status interrupt bit.

BIT 4 Receiver Ready Enable

Bit 4 is used to enable the RX RDY and RX overrun interrupt sources. When bit 4 is set, the receiver ready indication will set bit 1 of the HDLC Interrupt (HINT) Register. The RX RDY indication will go active when a data byte (a byte that is not a flag, idle, or an abort pattern) is loaded into the RX Data Register. Also, if this bit is set, the RX overrun condition will result in a new status interrupt. If bit 4 is reset to a 0, bit 1 of the HDLC Interrupt Register will not be set, and no corresponding HDLC interrupt will be generated. Also, a RX overrun condition, as indicated by bit 4 of the HDLC Status (HSTAT) Register, will not result in a HDLC interrupt or in setting the new status interrupt bit.

BIT 3 Invalid Flag Interrupt Enable

When bit 3 is set, a HDLC interrupt will be generated if bit 3 (INVALID FLAG) of the HDLC Status (HSTAT) Register is also set. If bit 3 is reset to a 0, bit 2 (NEW STATUS) of the HDLC Interrupt (HINT) Register will not be set as a result of an invalid flag boundary detection and no HDLC interrupt will be generated.

BIT 2 Abort Detect Interrupt Enable

When bit 2 is set, a HDLC interrupt will be generated if bit 2 (ABORT DETECT) of the HDLC Status (HSTAT) Register is also set. If bit 2 is reset to a 0, bit 2 (NEW STATUS) of the HDLC Interrupt (HINT) Register will not be set as a result of an abort pattern detection and no HDLC interrupt will be generated.

BIT 1 Idle Detect Interrupt Enable

When bit 1 is set, an HDLC interrupt will be generated if bit 1 (IDLE DETECT) of the HDLC Status (HSTAT) Register is also set. If bit 1 is reset to a 0, bit 2 (NEW STATUS) of the HDLC Interrupt (HINT) Register will not be set as a result of an idle pattern detection and no HDLC interrupt will be generated.

HDLC INTERRUPT ENABLE REGISTER (HIE) SFR ADDRESS 0C4h (continued)

BIT 0 Flag Detect Interrupt Enable

When bit 0 is set, a HDLC interrupt will be generated if bit 0 (FLAG DETECT) of the HDLC Status (HSTAT) Register is also set. If bit 0 is reset to a 0, bit 2 (NEW STATUS) of the HDLC Interrupt (HINT) Register will not be set as a result of a flag pattern detection and no HDLC interrupt will be generated.

HDLC INTERRUPT SOURCE REGISTER (HINT) SFR ADDRESS 0C5h
Byte Addressable
Read Only Register
Reset State 00h

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
0	0	0	0	0	NEW STATUS	RXRDY	TX RDY

This register is used to determine the source of HDLC interrupts. If one or more of these register bits are set, the corresponding HDLC interrupt will go active if bit 0 of the HDLC Control 1 (HDLC1) Register is set to a 1.

BIT 2 New Status

When bit 2 is set, an unmasked HDLC status bit from the HDLC Status (HSTAT) Register is set.

Bit 2 will by cleared upon a reset and is cleared by a read of the HDLC Status Register.

BIT 1 RX Ready

When bit 1 is set, a new received byte has been loaded into the RX Data (RXD) Register. Note, received bits that are flag, abort, or idle patterns are not considered data, and will not be loaded into the RX Data Register. All inserted 0s have been removed from this byte. The RX Data Register must be read prior to the completed reception of the next data byte.

Bit 1 will by cleared upon a reset and is cleared by a read of the RX Data Register.

BIT 0 TX Ready

Bit 0 is set if any HDLC TX control (HTXC) bits 3:0 are set as the first bit of data, flag or an idle byte is being transmitted. While transmitting the current byte, the HDLC state machines are ready for commands pertaining to the next byte to be transmitted. A new data byte must be loaded into the TX Data (TXD) Register to clear the TX ready status bit.

Bit 0 will by cleared upon a reset and is cleared by writing to the TX Data Register.

RX DATA REGISTER (RXD) SFR ADDRESS 0C6h
Byte Addressable
Read Only Register
Reset State XXh

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
RX DAT7	RX DAT6	RX DAT5	RX DAT4	RX DAT3	RX DAT2	RX DAT1	RX DAT0

BITS 7-0 Received Data Byte

Bit 7 through bit 0 is the received data byte (LSB is received first) with all inserted 0s removed. A data ready interrupt will be generated when a new data byte is received. Reading this register will clear the data ready interrupt.

TX DATA REGISTER (TXD) SFR ADDRESS 0C7h
Byte Addressable
Write Only Register
Reset State XXh

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
TX DAT7	TX DAT6	TX DAT5	TX DAT4	TX DAT3	TX DAT2	TX DAT1	TX DAT0

BITS 7-0 Transmit Data Byte

Bit 7 through bit 0 will be transmitted at the next byte boundary (LSB first) if the HDLC TX control send data bit is set. The HDLC will insert all necessary 0s. A TX ready interrupt will be generated when a new data byte can be loaded into the TX Data Register. Writing this register will clear the TX ready interrupt.

REGISTER DESCRIPTION (continued)

CRC GENERATION

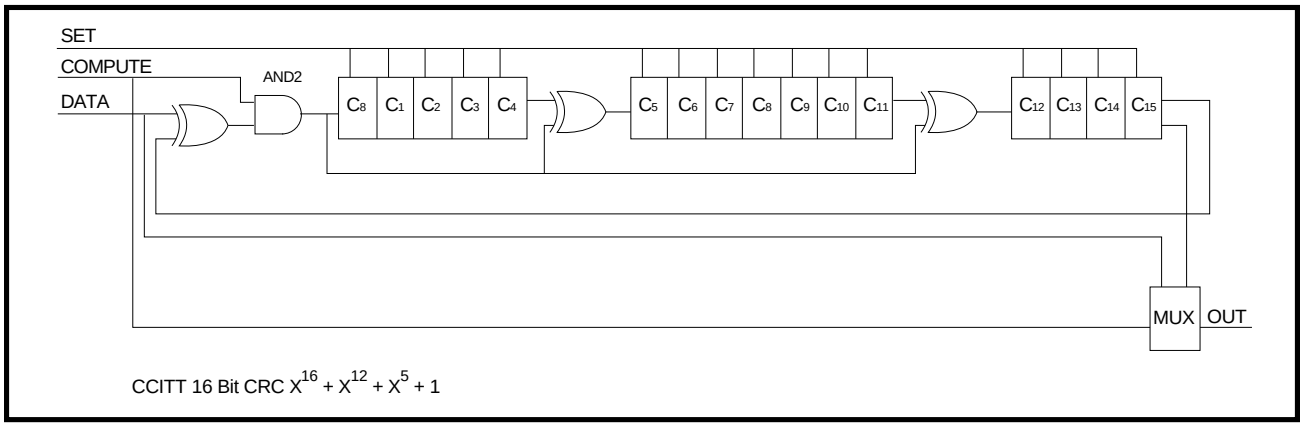


FIGURE 3: CCITT Type

CCITT Type

The CRC check field is generated by the transmitter. The computation starts with the first transmitted bit after the opening flag and stops at the last data bit prior to the frame check sequence bytes, and excludes inserted 0s. The CRC generating logic is initialized to all ones. The bits are shifted in and operated on by the generating polynomial, $X^{16} + X^{12} + X^5 + 1$. During CRC transmission, the bytes in the CRC generating logic are inverted and transmitted, high order bit first.

The receiver also initializes its CRC computation logic to all ones after the beginning flag. Its polynomial generator (also $X^{16} + X^{12} + X^5 + 1$) should see the same value as the transmitter's polynomial generator as the last data bit is received. Note the receiver's polynomial generator does not process inserted 0s. After the bytes are received in the frame check sequence, a remainder of 1111 0000 1011 1000 (X^0 through X^{15}, respectively) should be detected in the receiver's polynomial generator. If this is not the case, it is assumed that the preceding frame was in error and an invalid CRC is declared.

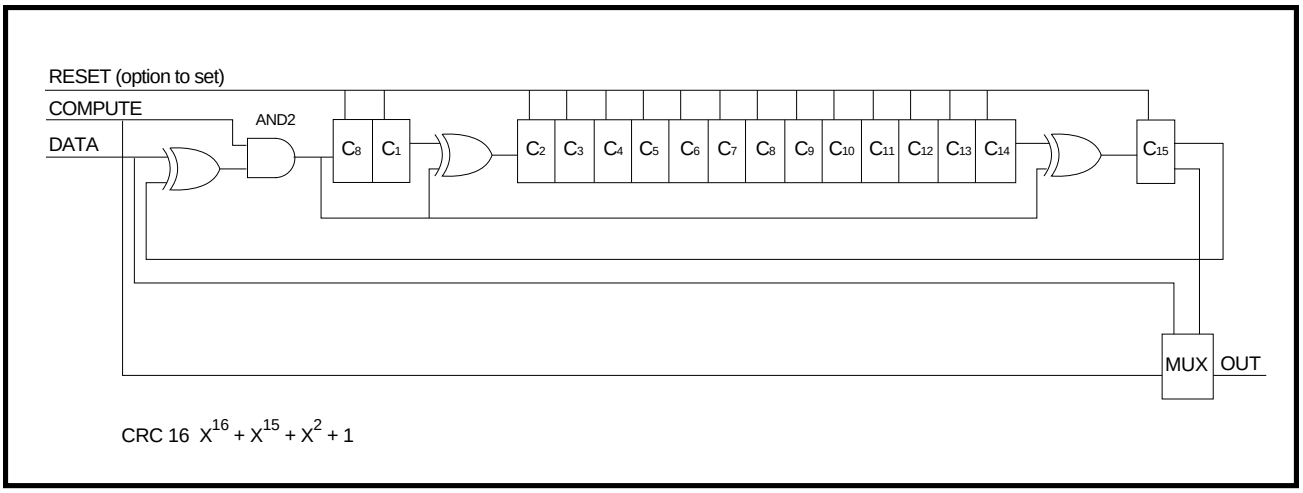


FIGURE 4: CRC 16

CRC 16

The CRC check field is generated by the transmitter. The computation starts with the first transmitted bit after the opening flag and stops at the last data bit prior to the frame check sequence bytes, and excludes inserted 0s. The CRC generating logic is initialized to all 0s. The bits are shifted in and operated on by the generating polynomial, $X^{16} + X^{12} + X^5 + 1$. During CRC transmission, the bytes in the CRC generating logic are transmitted, high order bit first.

The receiver also initializes its CRC computation logic to all ones after the beginning flag. Its polynomial generator (also $X^{16} + X^{12} + X^5 + 1$) should see the same value as the transmitter's polynomial generator as the last data bit is received. Note the receiver's polynomial generator does not process inserted 0s. After the bytes are received in the frame check sequence, a remainder of 1111 0000 1011 1000 should be detected in the receiver's polynomial generator. If this is not the case, it is assumed that the preceding frame was in error and an invalid CRC is declared.

CRC GENERATION (continued)

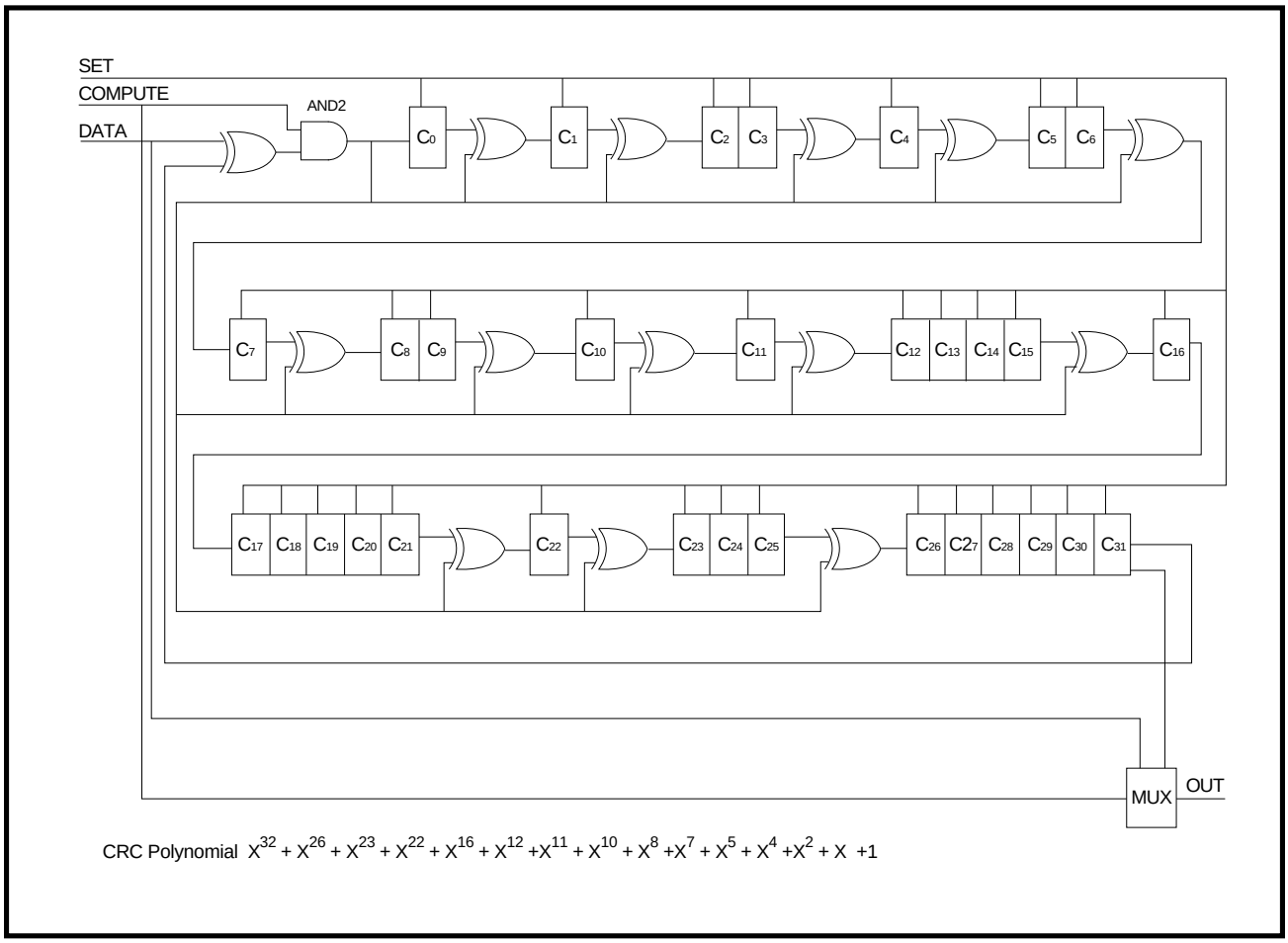


FIGURE 5: 32-Bit CRC

CRC 32

The CRC check field is generated by the transmitter. The computation starts with the first transmitted bit after the opening flag and stops at the last data bit prior to the frame check sequence bytes, and excludes inserted 0s. The CRC generating logic is initialized to all ones. The bits are shifted in and operated on by the generating polynomial, $X^{32} + X^{26} + X^{23} + X^{22} + X^{16} + X^{12} + X^{11} + X^{10} + X^8 + X^7 + X^5 + X^4 + X^2 + X + 1$. During CRC transmission, the bytes in the CRC generating logic are inverted and transmitted, high order bit first. The receiver also initializes its CRC computation logic to all ones after the beginning flag. Its polynomial generator should see the same value as the transmitter's polynomial generator as the last data bit is received. Note the receiver's polynomial generator does not process inserted 0s. After the bytes are received in the frame check sequence, a remainder of 1101 1110 1011 1011 0010 0000 1110 0011 (X^0 through X^{32}, respectively) should be detected in the receiver's polynomial generator. If this is not the case, it is assumed that the preceding frame was in error and an invalid CRC is declared.

PIN DESCRIPTION

NAME	TYPE	DESCRIPTION
$\overline{\text{PSEN}}$	O	Program store enable. This output occurs only during a fetch to external program memory.
RESET	I	Input which is used to initialize the processor.
VND	GND	Negative digital voltage ground
OSCIN	I	Crystal input for internal oscillator, also input for external source.
OSCOUT	O	Crystal oscillator output.
VPD	I	Positive digital voltage (+5V Digital Supply)
CLKOUT1	O	Clock output programmable either OSC/2, OSC/1 or logic 0.
CLKOUT2	O	Clock output 1.8432 MHz clock for an external UART given an oscillator frequency of 11.0592 MHz, 22.1184 MHz, 18.432 MHz, or 13.824 MHz.
TXD	I	Serial input port to 73M2910/2910A from DTE same as RXD UART input.
RXD	O	Serial output port of 73M2910/2910A UART to DTE.
PTXCLK	I	Input clock used to transmit data PTXD.
PTXD	O	HDLC Packetizer TX output. This pin can also be programmed to the DTE's TXD output (clear channel) or the value written into bit 6 of the HDLC Control Register. Connects to modem device TXD.
PRXCLK	I	Input clock used to receive data PRXD.
PRXD	I	Serial input port (from modem device) to HDLC Packetizer.
$\overline{\text{INT}}(\overline{0})$-$\overline{\text{INT}}(\overline{2})$	I	External interrupt 0,1 and 2.
USR1.0 - USR1.7	I/O	USR programmable I/O port.
USR2.0 - USR2.7	I/O	USR programmable I/O port.
USR3.0 - USR3.7	I/O	USR programmable I/O port. If the bank select feature is chosen, USR (7) acts as address bit 17 and USR3 data bit 7 is ignored. Register BNKSEL bit 2 (BSEN) enables bank select, bit 1 (BS1) and bit 0 (BS0) select the appropriate bank.
USR4.0 - USR4.7	I/O	USR programmable I/O port also chip select enable.
USR5.0 - USR5.1	I/O	General purpose input port, can also be used for wakeup.
$\overline{\text{RD}}$	O	Output strobe activated during a bus read. Can be used to enable data onto the bus from an external device. Used as a read strobe to external data memory.
$\overline{\text{WR}}$	O	Output strobe during a bus write. Used as a write strobe to external data memory.
ALE	O	Address Latch Enable output pulse for latching the low byte of the address during accesses to external memory.
AD(0)-AD(7)	I/O	Data bus lines-I/O for devices that require multiplexed address and data bus.
A(0)-A(15)	O	Address bus lines-output latched address for devices that require separate data and address bus.
NO CONNECTS(NC)		No connections, leave open. Not a user pin.

MEMORY MAPS

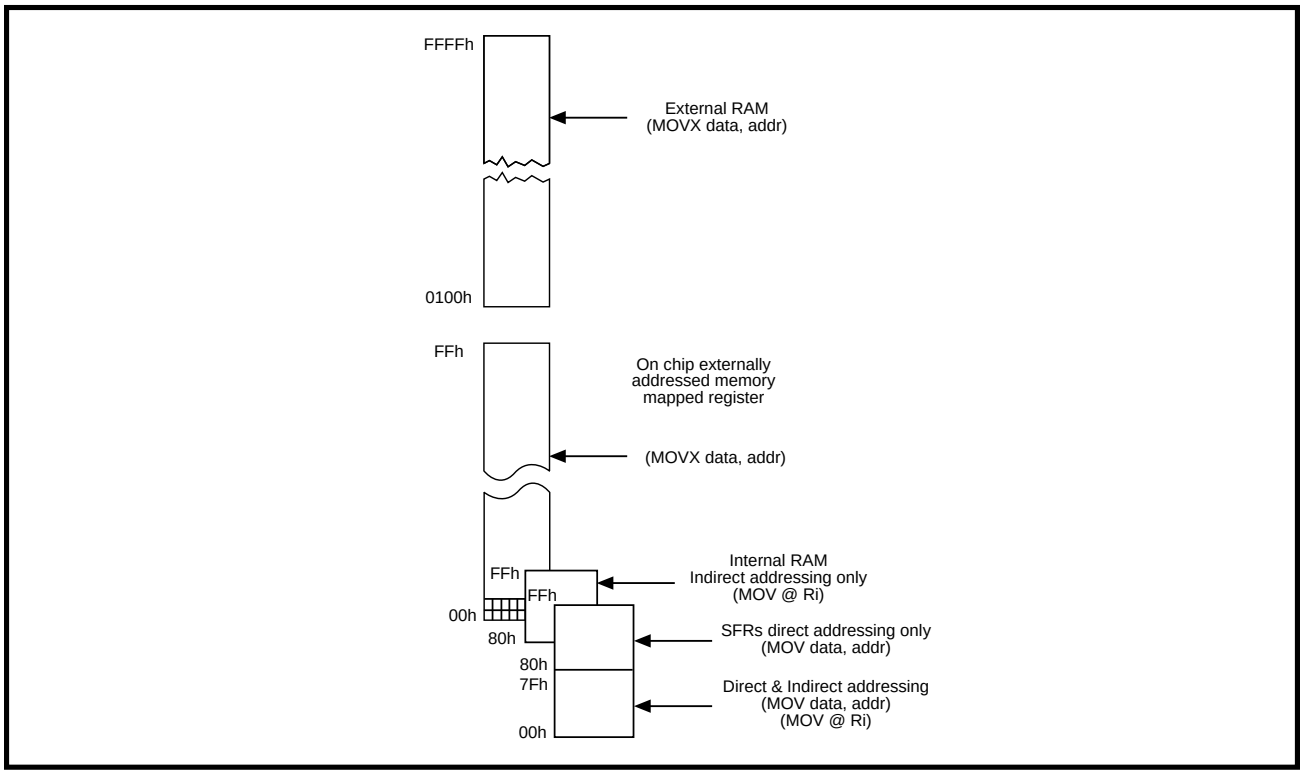


FIGURE 6: Memory Map

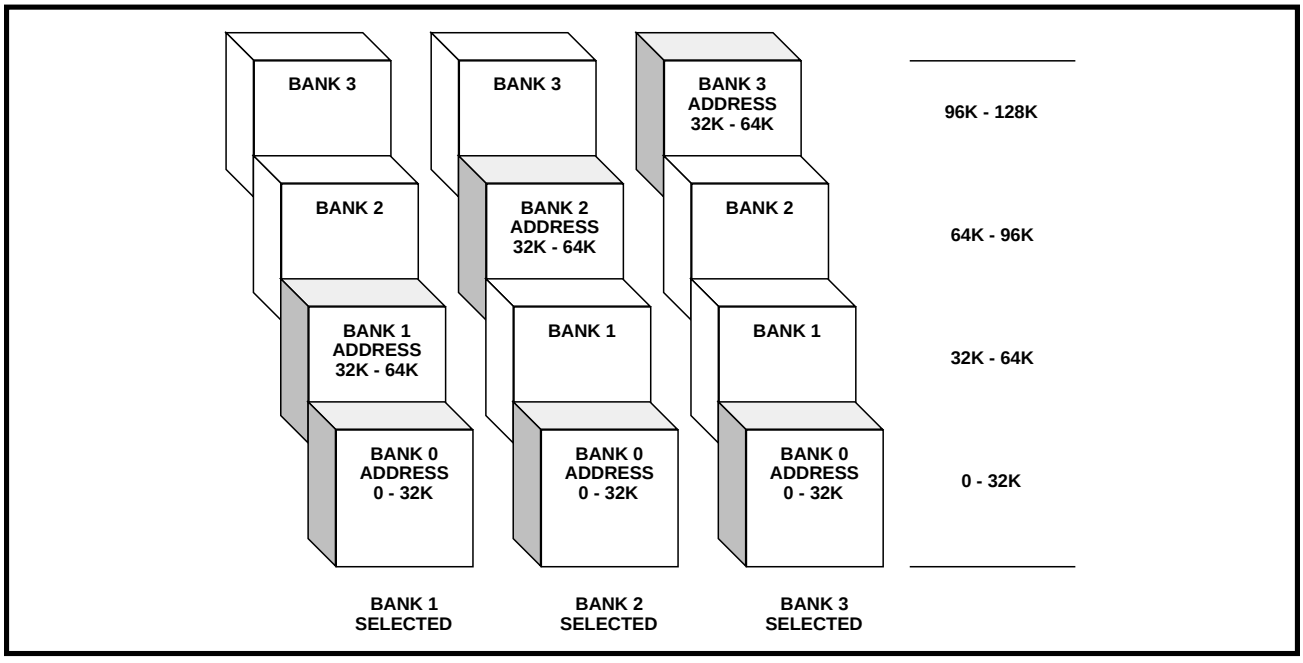


FIGURE 7: 128K of Bank-Selected Program Memory

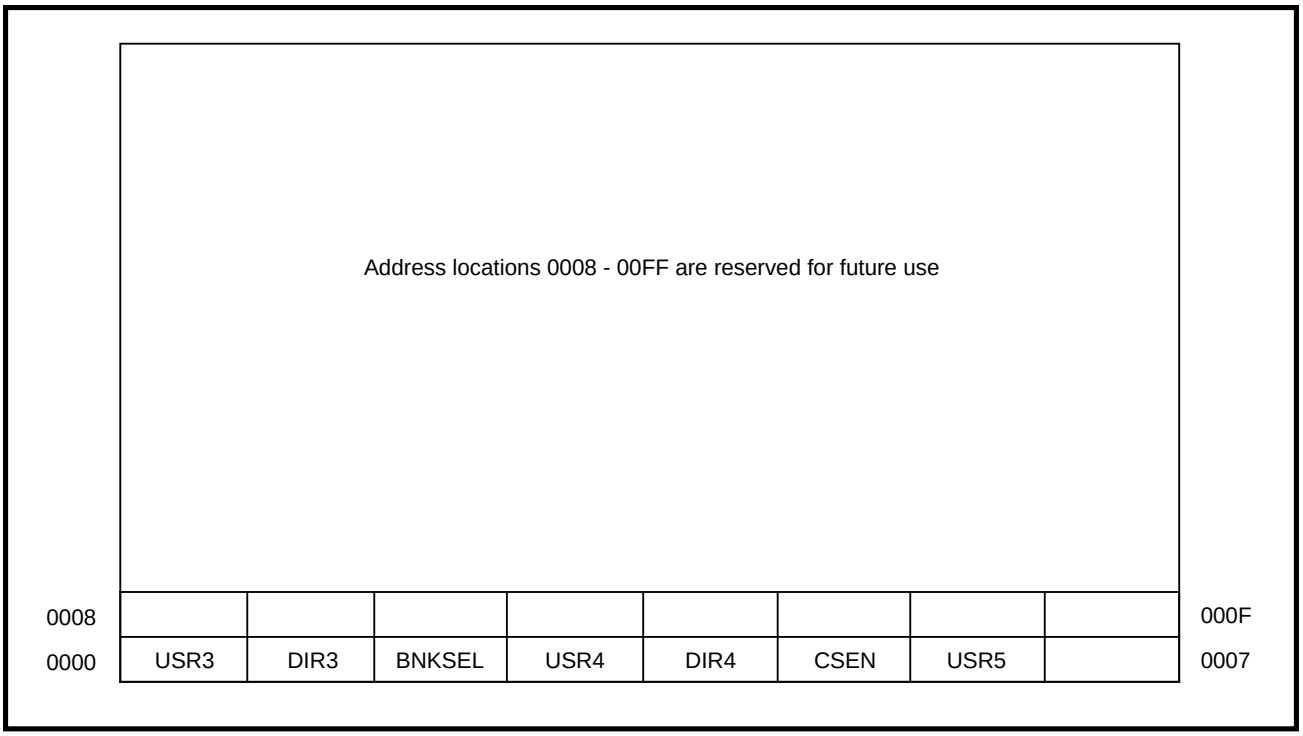


FIGURE 8: Memory Mapped Registers

F8									FF
F0	B								F7
E8									EF
E0	ACC								E7
D8	*USR2	*DIR2	CLK CTRL						DF
D0	PSW								D7
C8	T2CON		RCAP2L	RCAP2H	TL2	TH2			CF
C0	*HDLC0	*HDLC1	*TXC	*HSTAT	*HIE	*HINT	*HRXD	*HTXD	C7
B8	IP								BF
B0									B7
A8	IE								AF
A0	P2								A7
98	SCON	SBUF							9F
90	*USR1	*DIR1	*IDIR						97
88	TCON	TMOD	TL0	TL1	TH0	TH1			8F
80	P0	SP	DPL	DPH				PCON	87

* Unique to the SSI 73M2910. There may not be an equivalent function on an 8032.

Bit Addressable in this column

FIGURE 9: 73M2910/2910A SFR Map

ELECTRICAL SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Recommended conditions apply unless otherwise specified.

PARAMETER	RATING
Supply Voltage	-0.5 to +7.0V
Pin Input Voltage	-0.5 to Vcc +0.5V
Storage Temperature	-55 to +150°C

RECOMMENDED OPERATING CONDITIONS

Supply Voltage	4.5 to 5.5V
Oscillator Frequency	DC to 33 MHz
Supply Voltage	4.75 to 5.5V
Oscillator Frequency	DC to 44 MHz
Supply Voltage	3.0 to 5.5V
Oscillator Frequency	DC to 22 MHz
Operating Temperature	-40 to +85°C

DC CHARACTERISTICS

PARAMETER		CONDITION	MIN	NOM	MAX	UNIT
Input Low Voltage (Except OSCIN, RESET, TEST)	V_{IL}		-0.5		0.2 Vcc - 0.1	V
Input Low Voltage OSCIN, RESET, TEST	V_{IL}		-0.5		0.2 Vcc	V
Input High Voltage (Except OSCIN, RESET, TEST)	V_{IH}		0.5 Vcc		Vcc + 0.5	V
Input High Voltage OSCIN, RESET, TEST	V_{IH}		0.7 Vcc		Vcc + 0.5	V
Output Low Voltage (Except OSCOUT)	V_{OL}	Iol = 3.2 mA			0.45	V
Output Low Voltage OSCOUT	V_{OLOSC}	Iol = 1.5 mA			0.7	V
Output High Voltage (Except OSCOUT)	V_{OH}	Ioh = -3.2 mA	Vcc - 0.45			V
Output High Voltage OSCOUT	V_{OHOSC}	Ioh = 1.5 mA	Vcc - 0.7			V
Input Leakage Current	I_{IL}	Vss < Vin < Vcc			±10	µA
Maximum Power Supply Normal Operation	$I_{DD}1$	22 MHz 30 pF/pin			40	mA
Maximum Power Supply idle mode	$I_{DD}2$	22 MHz			10	mA

DC CHARACTERISTICS

PARAMETER		CONDITION	MIN	NOM	MAX	UNIT
Maximum Power Supply power-down mode	IDD3				10	µA
Pin Capacitance	CIO	@1 MHz			10	pF

AC TIMING

The SSI 73M2910/2910A timing is very similar to the 8032 except in AD(7:0), the multiplexed address data port known as port 0 in the 8032. Its timing has been altered somewhat to allow more address setup time for peripheral program ROM and memory mapped peripherals. This is important for operation above 22 MHz. The 8032 has a “dead” cycle of one oscillator period between the time PSEN goes high, indicating that the instruction ROM will release the AD(7:0) bus, to the time the processor will assert address on the AD(7:0) bus. This dead time of one whole oscillator cycle has been shortened to approximately 15 ns after the PSEN (or RD) signal is sensed to be high.

The timing specification for TPXIZ and TRHDZ of a maximum of 20 ns can be violated at the expense of increased operating current. The SSI 73M2910/2910A will begin asserting the AD(7:0) bus approximately 20 ns after PSEN or RD go high. This should be ample time for the control signals in the peripheral device to turn off their pad drivers. If the peripheral device does not release the bus promptly, there will be a short time where there is contention on the AD(7:0) bus between the processor and peripheral. This should not prevent proper operation, but it will increase operating current slightly.

Oscillator Frequency	FOSC	2910A @ 4.75 - 5.5V	0		44	MHz
		2910 @ 4.5 - 5.5V	0		34	MHz
		2910 @ 3.3 - 5.5V	0		22.2	MHz
Oscillator Period	TOSC	2910 @ 22.2 MHz	45			ns
		2910 @ 34 MHz	29.4			ns
		2910A @ 44 MHz	22.7			ns
ALE Pulse Width	TLHLL		2TOSC - 10			ns
Address Valid To ALE Low	TAVLL		TOSC			ns
Address Valid ALE Low	TLLAX		TOSC - 10			ns
ALE Low to $\overline{\text{PSEN}}$ Low	TLLPL		TOSC - 10			ns
$\overline{\text{PSEN}}$ Pulse Width Low	TPLPH		3TOSC - 20			ns
$\overline{\text{PSEN}}$ Low to Valid Inst In	TPLIV				3TOSC - 50	ns
Address to Valid Inst In	TAVIV	2910			6TOSC - 50	ns
		2910A			6TOSC - 32	ns
Input Instr Hold-$\overline{\text{PSEN}}$ High	TPXIX		0			ns
PSEN Instr Float-$\overline{\text{PSEN}}$ High	TPXIZ				20+	ns
$\overline{\text{PSEN}}$ Low to Address HighZ	TPLAZ				10	ns

AC TIMING (continued)

PARAMETER		CONDITION	MIN	NOM	MAX	UNIT
$\overline{RD}$ Pulse Width	TRLRH		6TOSC - 20			ns
$\overline{WR}$ Pulse Width	TWLWH		6TOSC - 20			ns
$\overline{RD}$ Low to Valid Data In	TRLDV				5TOSC - 50	ns
Data Hold After $\overline{RD}$	TRHDX		0			ns
Data Float After $\overline{RD}$	TRHDZ				20+	ns
ALE Low to Valid Data In	TLLDV				8TOSC - 50	ns
ALE Low to $\overline{RD}$ or $\overline{WR}$ Low	TLLWL		3TOSC - 20		3TOSC + 20	ns
Data Valid to $\overline{WR}$ Low	TQVWX		TOSC			ns
Data Hold After $\overline{WR}$ High	TWHQX		TOSC - 10			ns
$\overline{RD}$ Low to Address Float	TRLAZ				10	ns

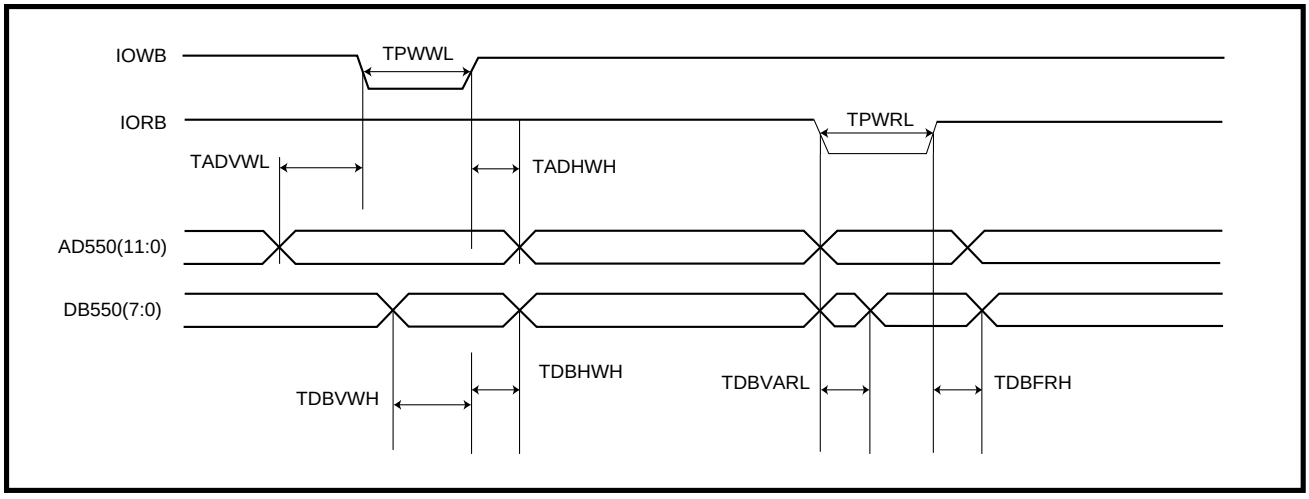


FIGURE 10: AC Timing

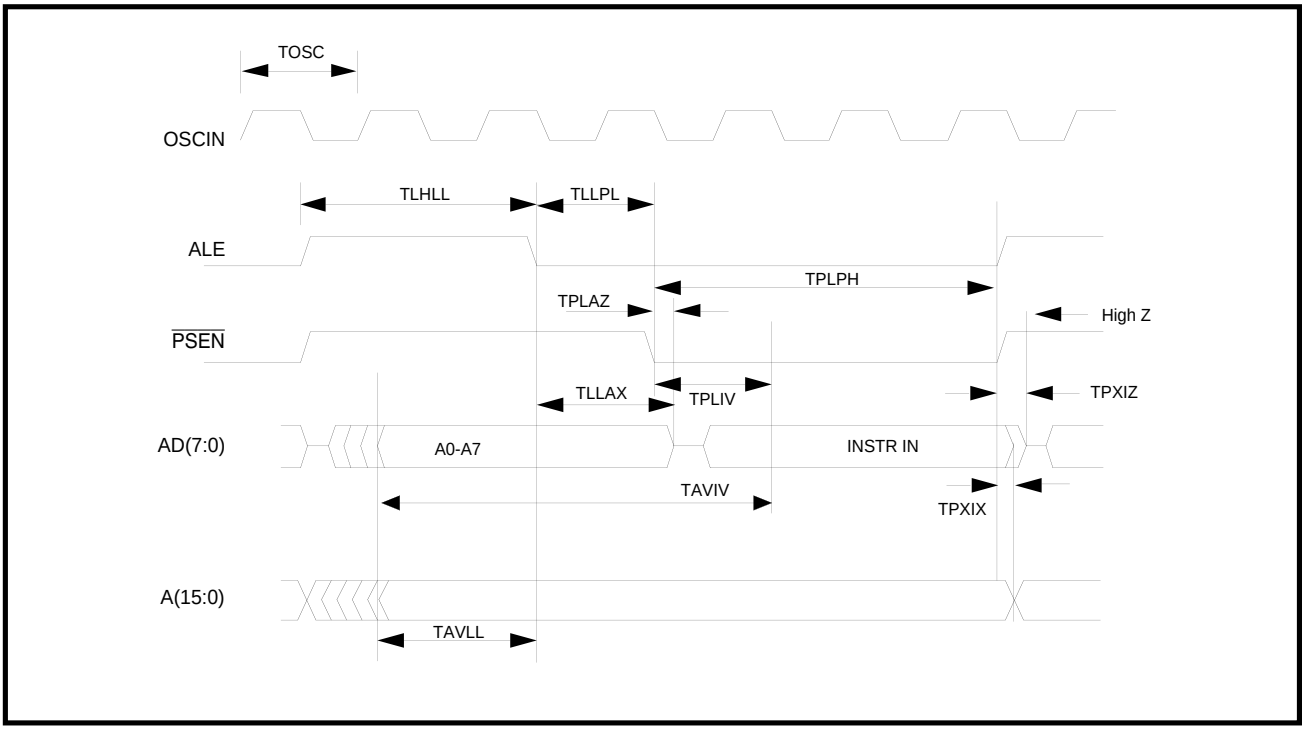


FIGURE 11: External Program Memory Read Cycle

ELECTRICAL SPECIFICATIONS (continued)

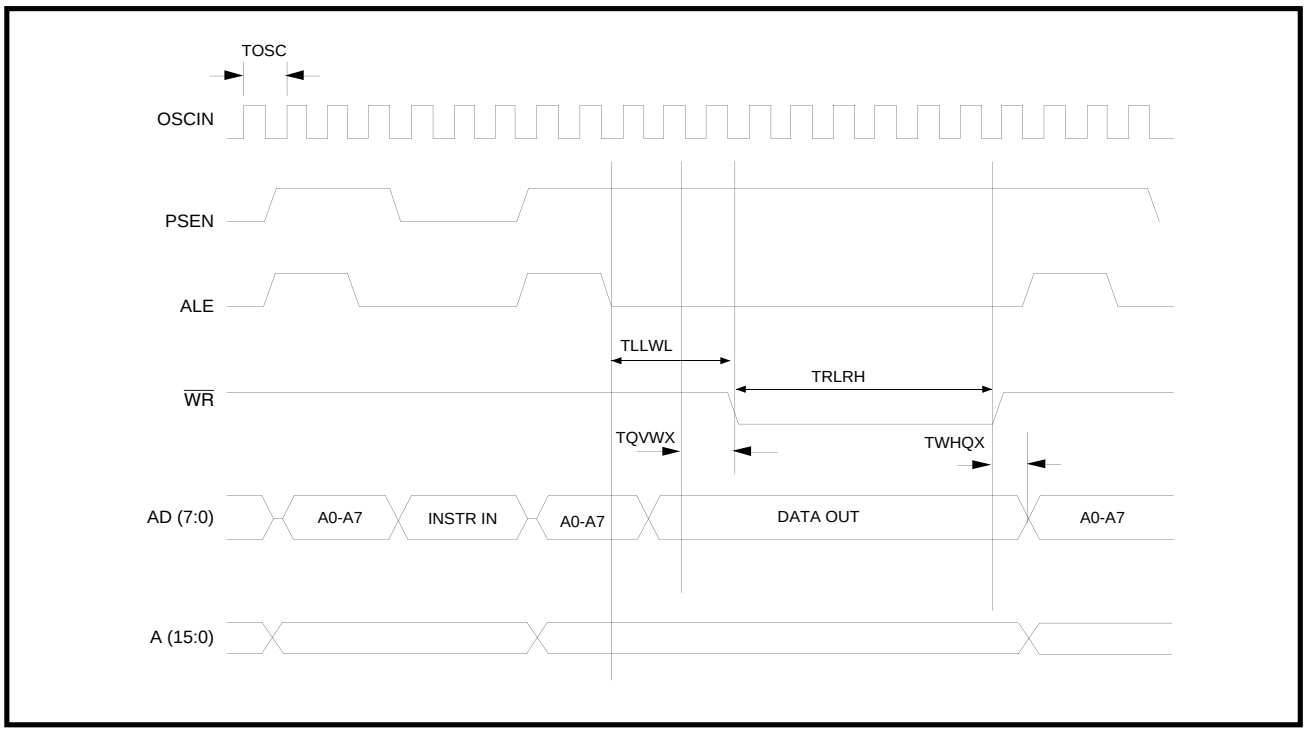


FIGURE 12: External Data Memory Write Cycle

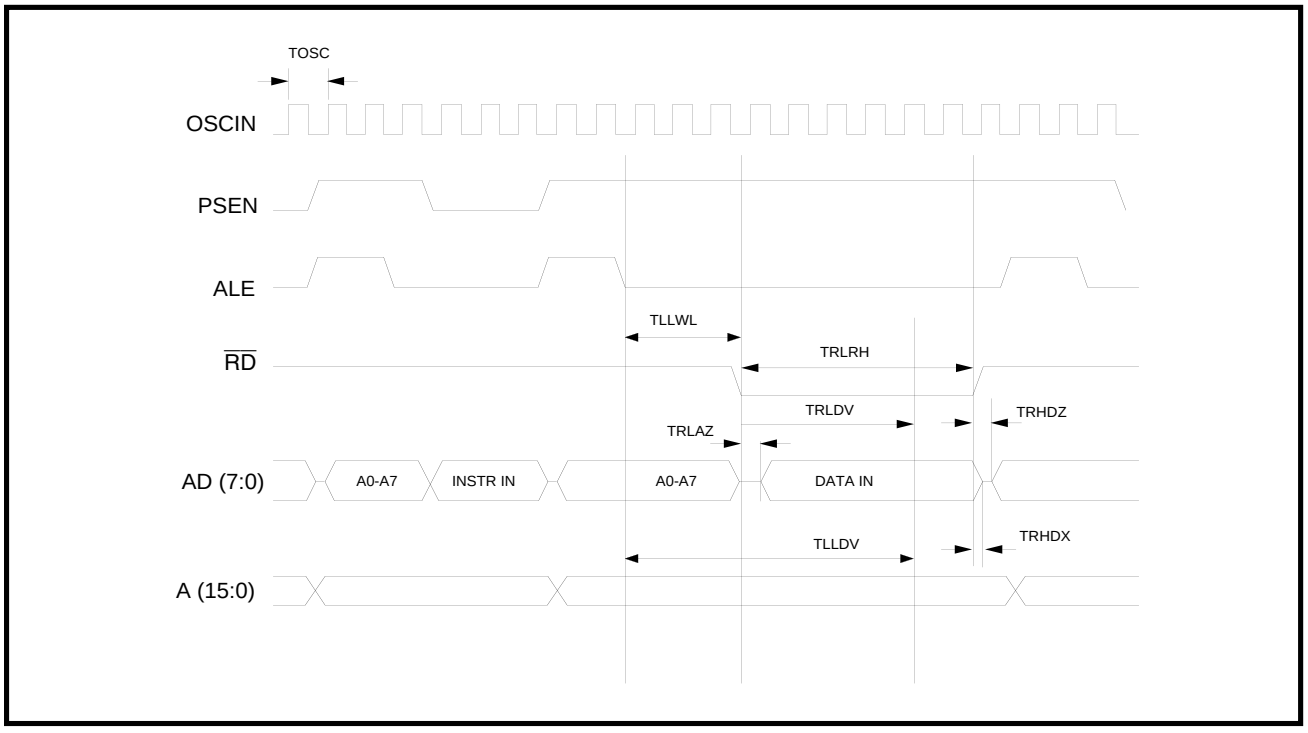


FIGURE 13: External Data Memory Read Cycle

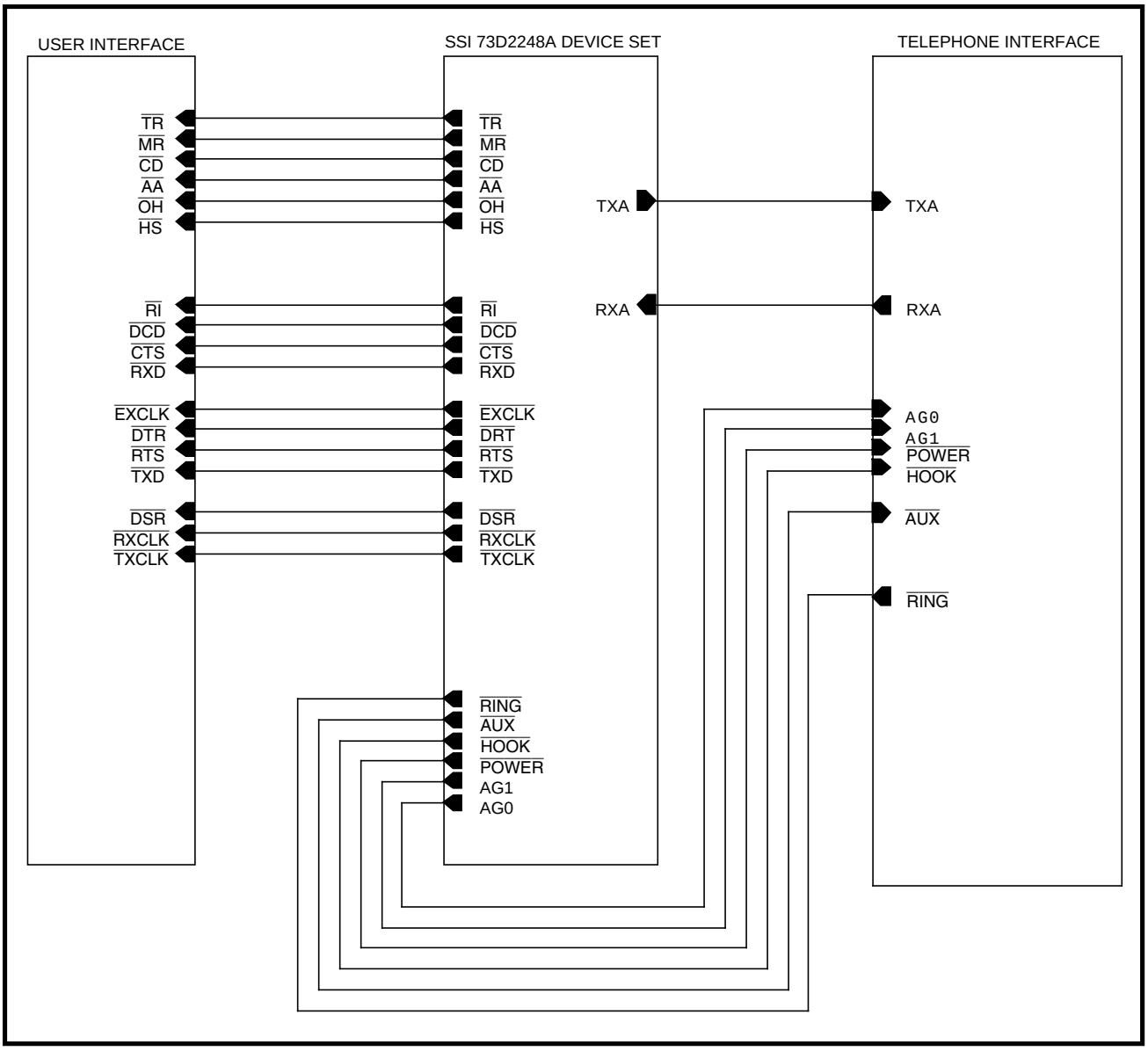


FIGURE 14: Modem Block Diagram

ELECTRICAL SPECIFICATIONS (continued)

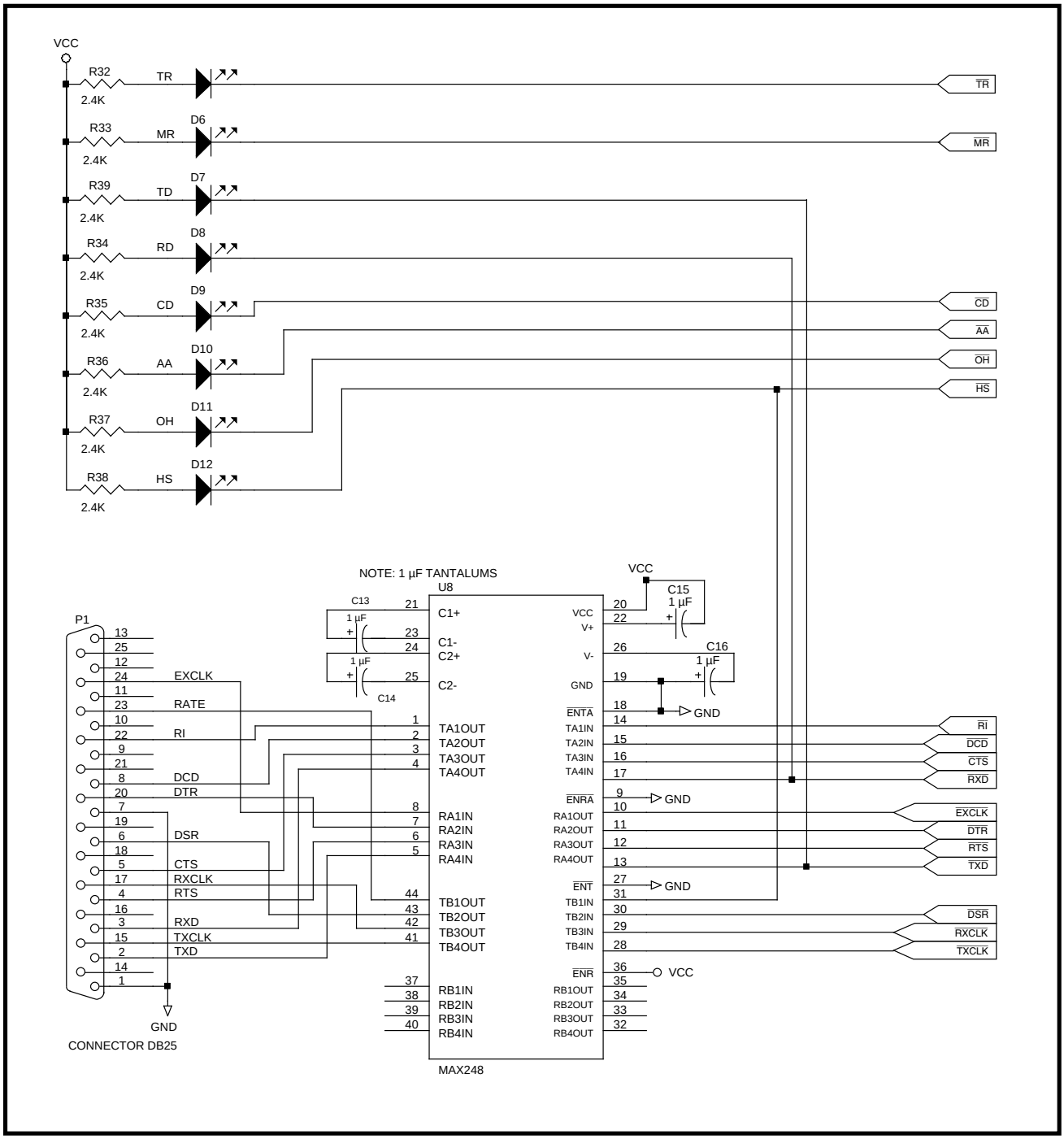


FIGURE 15: Display and User Interface

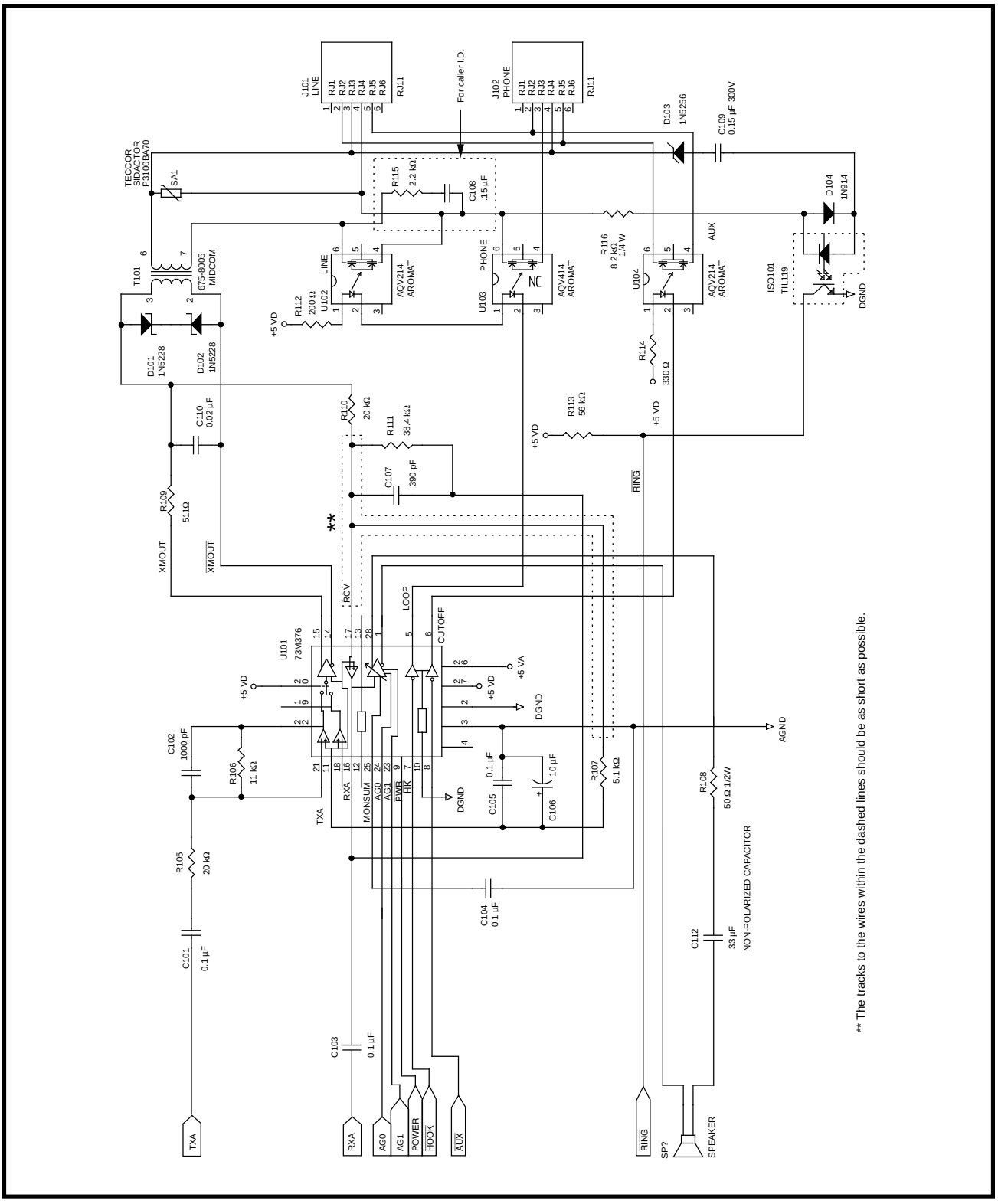


FIGURE 16: Telephone Interface

ELECTRICAL SPECIFICATIONS (continued)

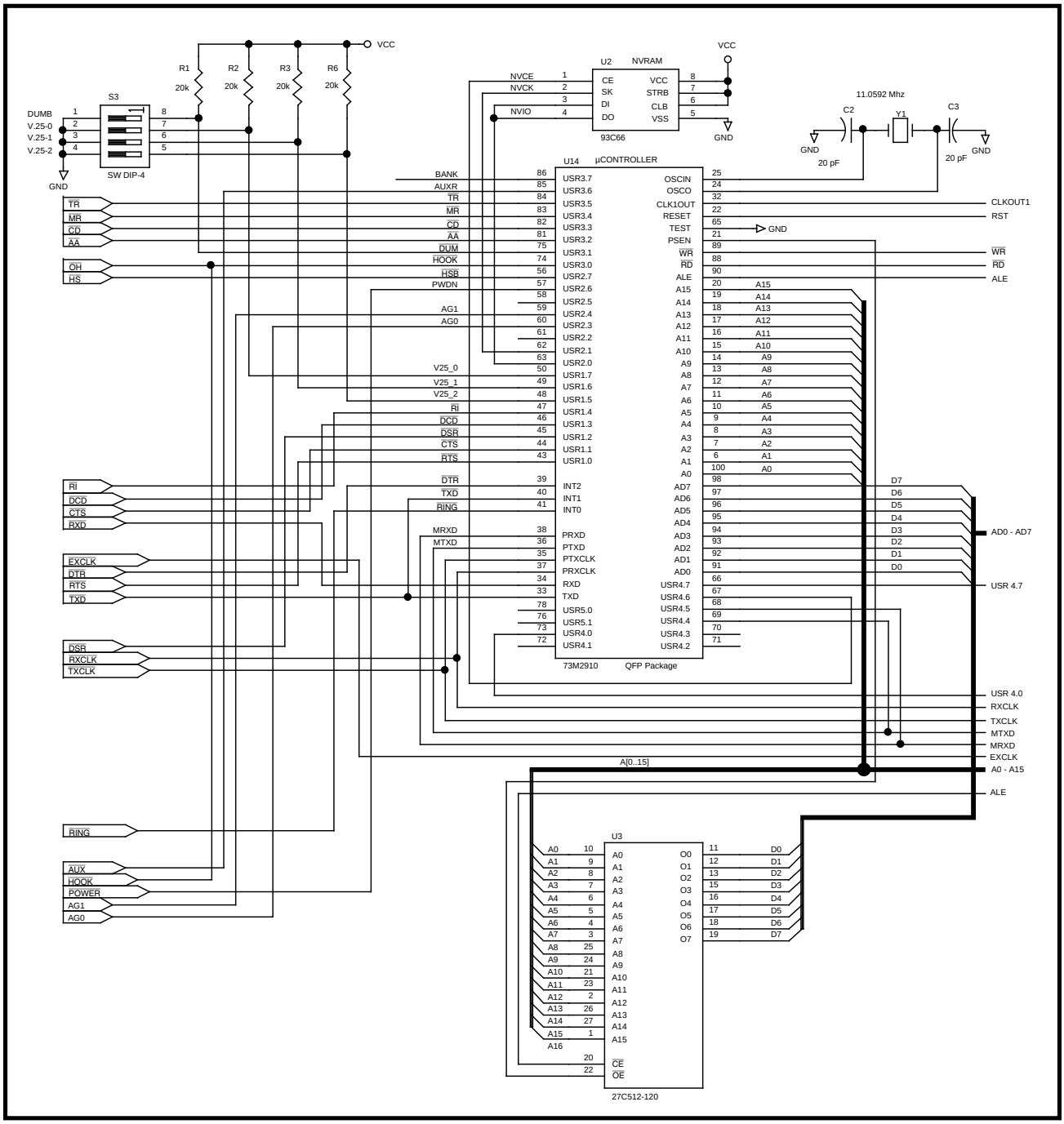


FIGURE 17A: Modem System Interconnect - Front End

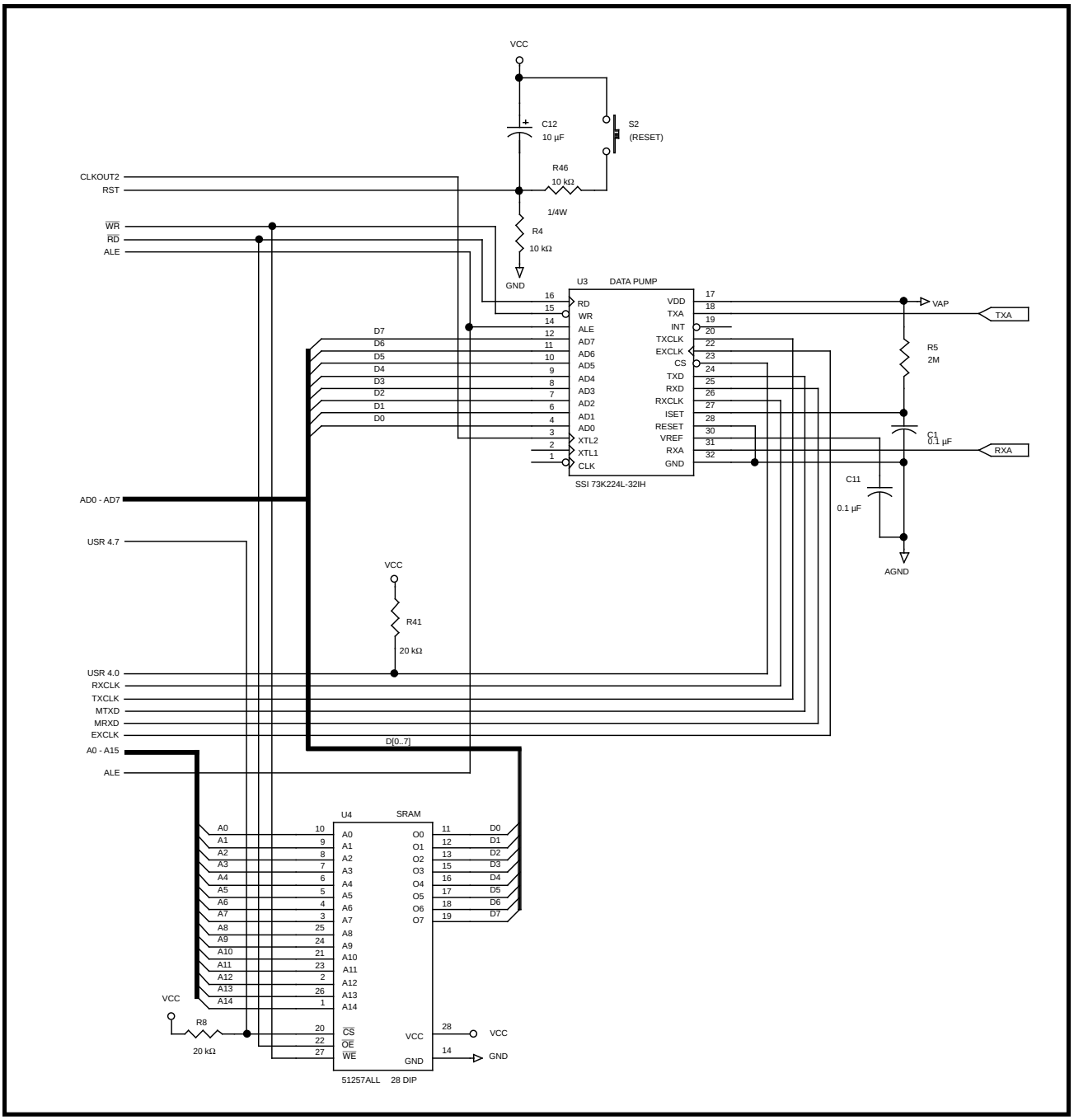


FIGURE 17B: Modem System Interconnect - Back End

ELECTRICAL SPECIFICATIONS (continued)

100-Pin PGA
(For development purposes only; not a production package.)

PIN #	SIGNAL NAME
B2	NO CONNECT
B1	NO CONNECT
C1	USR2.6
C2	USR2.7
D2	USR2.5
D1	USR2.4
E2	USR2.3
E1	USR2.2
F3	USR2.1
F2	USR2.0
F1	VPD
G2	GND
G3	USR4.7
G1	USR4.6
H1	USR4.5
H2	USR4.4
H3	USR4.3
J1	USR4.2
J2	USR4.1
K1	USR4.0
K2	USR3.0
L1	USR3.1
M1	USR5.1
L2	NO CONNECT
N1	NO CONNECT
M2	NO CONNECT
N2	NO CONNECT
M3	USR5.0
N3	USR3.2
M4	USR3.3
N4	USR3.4
M5	USR3.5
N5	USR3.6
L6	USR3.7
M6	GND
N6	$\overline{RD}$

PIN #	SIGNAL NAME
M7	$\overline{WR}$
L7	ALE
N7	D0
N8	D1
M8	D2
L8	D3
N9	D4
M9	D5
N10	D6
M10	D7
N11	VPD
N12	A0
M11	NO CONNECT
N13	NO CONNECT
M12	NO CONNECT
M13	NO CONNECT
L12	NO CONNECT
L13	A1
K12	A2
K13	A3
J12	A4
J13	A5
H11	A6
H12	A7
H13	A8
G12	A9
G11	A10
G13	A11
F13	A12
F12	A13
F11	A14
E13	A15
E12	$\overline{PSEN}$
D13	RESET
D12	GND
C13	OSCOUT

100-Pin PGA (continued)

(For development purposes only; not a production package.)

PIN #	SIGNAL NAME
B13	OSCIN
C12	NO CONNECT
A13	NO CONNECT
B12	NO CONNECT
A12	CLK2OUT
B11	VPD
A11	CLK1OUT
B10	TXD
A10	RXD
B9	PTXCLK
A9	PTXD
C8	PRXCLK
B8	PRXD
A8	$\overline{INT}2$

PIN #	SIGNAL NAME
B7	$\overline{INT}1$
C7	$\overline{INT}0$
A7	GND
A6	USR1.0
B6	USR1.1
C6	USR1.2
A5	USR1.3
B5	USR1.4
A4	USR1.5
B4	USR1.6
A3	USR1.7
A2	NO CONNECT
B3	NO CONNECT
A1	NO CONNECT

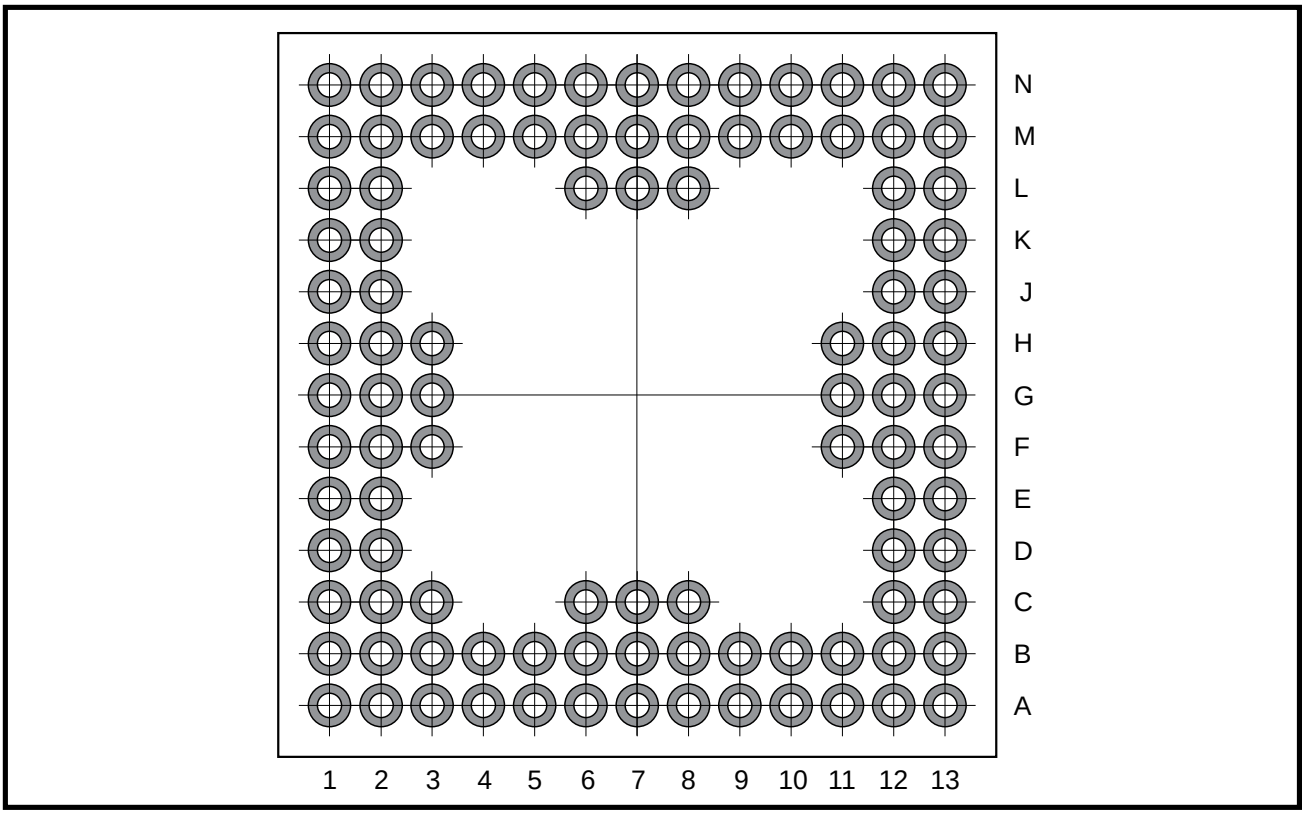
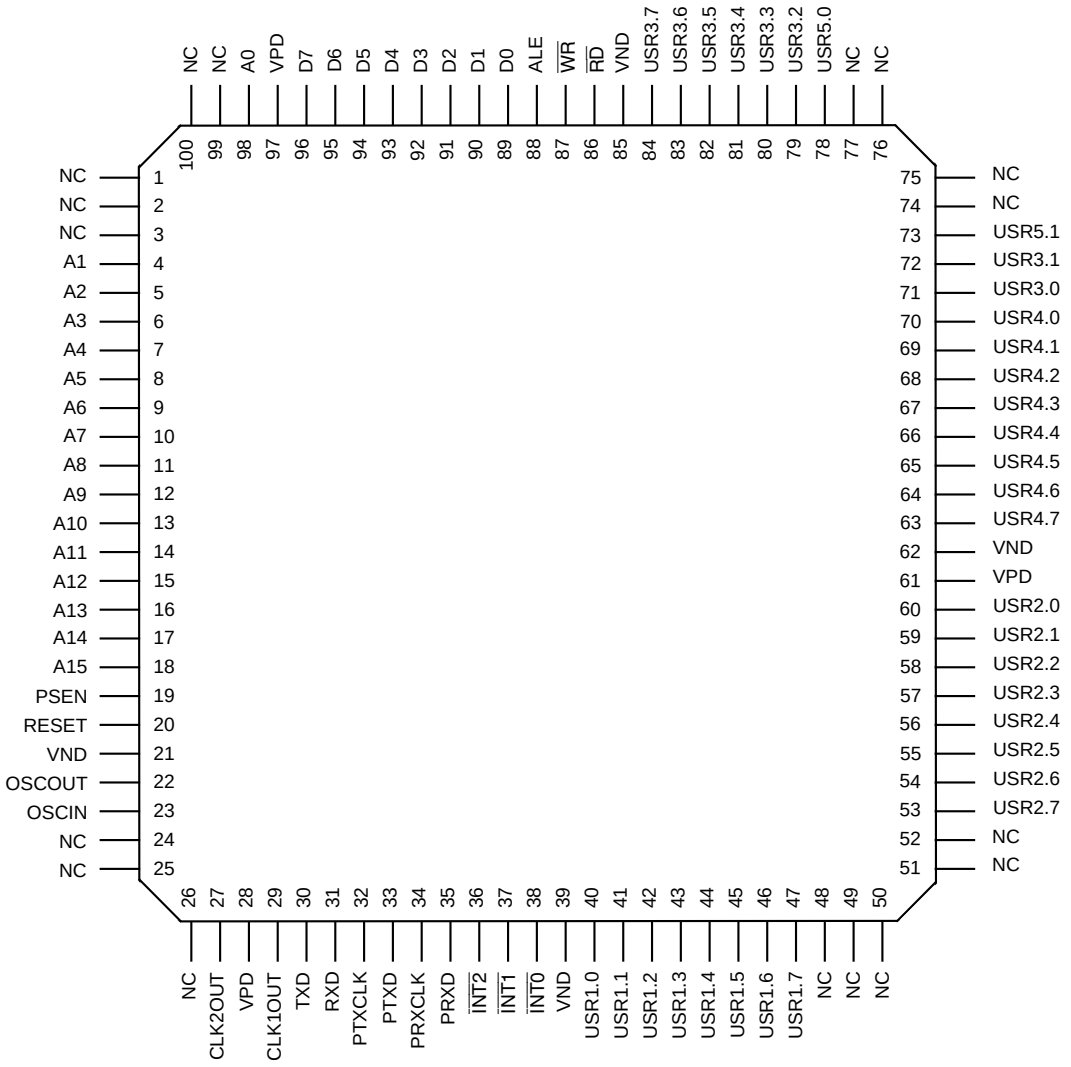


FIGURE 18: 100-Pin Grid Array (PGA) Package (Bottom View)

PACKAGE PIN DESIGNATIONS

(Top View)

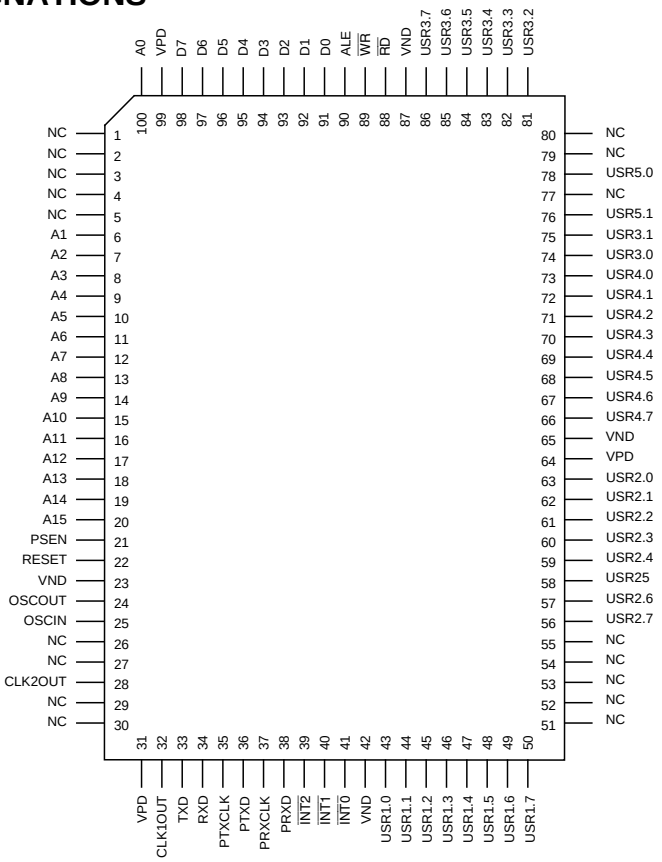


100-Lead TQFP

CAUTION: Use handling procedures necessary for a static sensitive component.

PACKAGE PIN DESIGNATIONS

(Top View)



CAUTION: Use handling procedures necessary for a static sensitive component.

100-Lead QFP

ORDERING INFORMATION

PART DESCRIPTION		ORDER NUMBER	PACKAGE MARK
SSI 73M2910	100-Lead QFP	73M2910-IG	73M2910-IG
	100-Lead TQFP	73M2910-IGT	73M2910-IGT
	100-Pin PGA	73M2910-IA	73M2910-IA
SSI 73M2910A	100-Lead QFP	73M2910A-IG	73M2910-IG
	100-Lead TQFP	73M2910A-IGT	73M2910-IGT
	100-Pin PGA	73M2910A-IA	73M2910-IA

Silicon Systems, Inc., 14351 Myford Road, Tustin, CA 92680-7022 (714) 573-6000, FAX (714) 573-6914

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SSI 73M2917/2917A
Microcontroller and UART
Advance Information

March 1996

DESCRIPTION

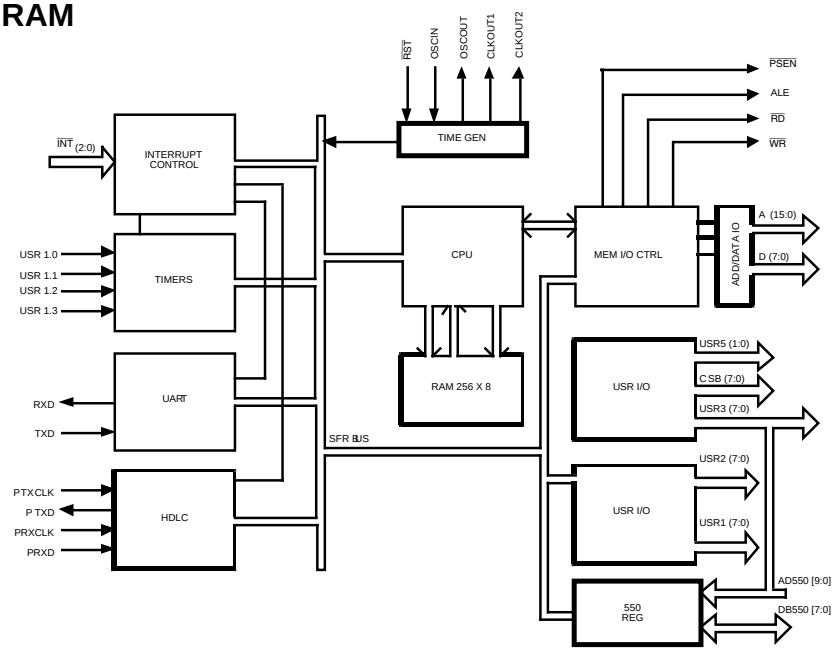
The SSI 73M2917/2917A is a combination of the SSI 73M2910 modem microcontroller and a virtual 550 UART, implemented in Silicon Systems advanced sub micron CMOS process. The 8-bit processor has the same attributes of the 8032 including instruction cycle time, UART, timers, interrupts, 256 bytes of on-chip RAM and programmable I/O. The virtual 550 UART utilizes proprietary technology, which results in a complete emulation of the industry standard 550 UART, and adds significant features. The 550 UART emulator provides familiar 550 functionality to the PC and replaces the serial link between the PC and the dedicated processor with a parallel data interface. The architecture results in a very high-performance system solution, that is also optimized for low power portable modem applications.

The SSI 73M2917/2917A also includes the user friendly HDLC Packetizer that is available in the SSI 73M2910. It has a serial I/O, hardware support for 16 and 32-bit CRC, zero insert/delete control, a dedicated interrupt and a clear channel mode for by-passing the packetizer. (continued)

FEATURES

- **8032 compatible instruction set**
- **Virtual 550 UART**
- **33 MHz operation (2917); 44 MHz (2917A)**
- **Operates at 3.3V and 5V**
- **HDLC support logic (Packetizer, 16 and 32 CRC, zero ID)**
- **24 pins for user programmable I/O ports**
- **8 pins programmable chip select logic for memory mapped peripheral eliminating glue logic**
- **3 external interrupt sources (programmable polarity)**
- **16 dedicated latched address pins**
- **Multiplexed data/address bus**
- **Instruction cycle time identical to 8032**
- **Buffered oscillator (or OSC/2, OSC/1.5) output pin** (continued)

BLOCK DIAGRAM



DESCRIPTION (continued)

Other features include additional user programmable I/O with programmable bank select and chip select logic, designed to eliminate board level glue logic. It also includes two general purpose input ports with programmable wakeup capability.

For devices that require non-multiplexed address and data buses, eight latched outputs for the low byte of the address are available.

The SSI 73M2917/2917A has two extra interrupt sources, an external interrupt and an HDLC interrupt. The HDLC interrupt has two registers associated with it: the HDLC Interrupt Register which is used to determine the source of the interrupt, and the HDLC Interrupt Enable Register that enables the source of the interrupt.

The state of the external interrupts can be read through a register allowing the interrupt pins to be used as inputs. The interrupt pins $\overline{INT0}$ and $\overline{INT1}$ can be either negative edge, positive edge or level triggered. $\overline{INT2}$ pin is always edge triggered.

Two buffered clock outputs have been added to support peripheral functions such as UARTs, modems and other clocked devices. The main internal processor clock frequency can be divided by 2 for power conservation in functional modes that only require half the clock speed.

Additional internal special function registers are used for firmware control over the HDLC Packetizer, the clocks and the programmable I/O ports.

To accommodate processor peripherals when operating at 33 MHz the processor's timing has been altered somewhat to allow more address setup time for slower peripheral program ROM and memory mapped peripherals. This can offer the system designers an advantage when using higher (33 MHz) oscillator frequency.

For low power applications the SSI 73M2917/2917A operates from 3 to 5 volts at 33 MHz and supports two power conservation modes: idle and power-down. In the power-down state the total current consumption is less than 1 µA at room temperature.

This device is offered in small form factor 100-Lead TQFP package for PCMCIA applications and a 100-Lead QFP package.

DEVELOPER'S NOTE

The SSI 73M2917/2917A is also available in a 100-Pin PGA package for system developers. The PGA package is more convenient and reliable for development emulation systems than the other package styles. Emulation systems for the SSI 73M2917/2917A are available through Signum Systems,171 E. Thousand Oaks Blvd., # 202, Thousand Oaks, CA 91360 (805) 371-4608.

8032 REFERENCE

This Document will describe the features unique to the SSI 73M2917/2917A. Please refer to an 8032 Programmer's Guide, Architectural Overview and Hardware Description for details on the SSI 73M2917/2917A core processor instruction set, timers, UART, interrupt control, and memory structure.

FEATURES (continued)

- 1.8432 MHz UART clock available if crystal frequencies 11.0592 MHz, 22.1184 MHz, 18.432 MHz, or 13.824 MHz are used
- Bank select circuitry to support up to 128K of external program memory
- 100-Lead QFP, 100-Lead TQFP and 100-Pin PGA packages

Silicon Systems, Inc., 14351 Myford Road, Tustin, CA 92680-7022 (714) 573-6000, FAX (714) 573-6914

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A TDK Group Company

SSI 73M2918/2918A
Plug and Play Microcontroller and UART

Preliminary Data

March 1996

DESCRIPTION

The SSI 73M2918/2918A is a combination of the SSI 73M2910 modem microcontroller, a virtual 550 UART, and built in hardware to support the Plug and Play ISA standard, implemented in Silicon Systems' advanced sub micron CMOS process. The 8-bit processor has the same attributes as the 8032 including instruction cycle time, UART, timers, interrupts, 256 bytes of on-chip RAM and programmable I/O. The virtual 550 UART utilizes proprietary technology, which results in complete emulation of the industry standard 550 UART, and adds significant features. The 550 UART emulator provides familiar 550 functionality to the PC and replaces the serial link between the PC and the dedicated processor with a parallel data interface. The architecture results in a high-performance system solution that is optimized for low power portable modem applications.

The SSI 73M2918/2918A also includes the user friendly HDLC Packetizer that is available in the SSI 73M2910. It has serial I/O, hardware support for 16-bit and 32-bit CRC, zero insert/delete control, a dedicated interrupt and a clear channel mode for by-passing the packetizer.

Other features include additional user programmable I/O with programmable bank select and chip select logic, designed to eliminate board level glue logic. It also includes two general purpose input pins with programmable wakeup capability.

For devices that require non-multiplexed address and data buses, eight latched outputs for the low byte of the address are available.

The SSI 73M2918/2918A has two extra interrupt sources, an external interrupt and an HDLC interrupt. The HDLC interrupt has two registers associated with it: the HDLC Interrupt Register which is used to determine the source of the interrupt, and the HDLC Interrupt Enable Register that enables the source of the interrupt.

The state of the external interrupts can be read through a register allowing the interrupt pins to be used as inputs. The interrupt pins INT0 and INT1 can be either negative edge, positive edge, or level triggered. INT2 pin is always edge triggered.

(continued)

FEATURES

- **8032 compatible instruction set**
- **Virtual 550 UART**
- **Dedicated Plug and Play ISA Bus Hardware**
- **33 MHz Operation (SSI 73M2918) and 44 MHz (SSI 73M2918A)**
- **+ 5V power supply**
- **HDLC support logic (Packetizer, 16 and 32 CRC, zero ID)**
- **24 pins of user programmable I/O ports**
- **8 pins of programmable chip select logic for memory mapped peripherals**
- **3 external interrupt sources (programmable polarity)**
- **16 dedicated latched address pins**
- **Multiplexed data/address bus**
- **Instruction cycle time identical to 8032**
- **Buffered oscillator (OSC/2 or OSC/1.5) output pin**
- **1.8432 MHz UART clock available if crystal frequencies of 11.0592 MHz, 22.1184 MHz, 18.432 MHz, or 13.824 MHz are used**
- **Bank select circuitry to support up to 128K of external program memory**
- **Available in 100-Lead QFP, 100-Lead TQFP and 100-Pin PGA packages**

DESCRIPTION (continued)

Two buffered clock outputs have been added to support peripheral functions such as UARTs, modem and other clocked devices. The main internal processor clock frequency can be divided by 2 for power conservation in modes that only require half the clock speed.

Additional internal special function registers are used for firmware control over the HDLC Packetizer, the clocks, and the programmable I/O ports.

The processor's timing has been altered slightly to allow more address setup time for slower peripheral program ROM and memory mapped peripherals. This can offer system designers an advantage when using higher oscillator frequencies.

For low power applications the SSI 73M2918/2918A supports two power conservation modes: idle and power-down. In the Power-down state the total current consumption is less than 10 μA at room temperature.

This device is offered in 100-Lead QFP and TQFP packages.

DEVELOPER'S NOTE:

The SSI 73M2918/2918A is also available in a 100-Pin PGA package for system developers. The PGA package is more convenient and reliable for development emulation systems than other package styles. Emulation systems for the SSI 73M2918/2918A are available through Signum Systems, 171 E. Thousand Oaks Blvd., # 202, Thousand Oaks, CA 91360 (805) 371-4608.

8032 REFERENCE

This Document will describe the features unique to the SSI 73M2918/2918A. Please refer to an 8032 Programmer's Guide, Architectural Overview and Hardware Description for details on the SSI 73M2918/2918A core processor instruction set, timers, UART, interrupt control, and memory structure.

FUNCTIONAL DESCRIPTION

PLUG AND PLAY IMPLEMENTATION

The SSI 73M2918/2918A Plug and Play circuitry provides a hardware and software mechanism for implementing the Plug and Play ISA standard for automatic configuration of ISA bus resources. The PC Bus interface includes hardware for implementing the Address, Read_Data and Write_Data ports, the Initiation Key protocol, Plug and Play card control registers, Logical Device control registers and appropriate configuration registers. The core microcontroller firmware is used to access the card's ID number needed in the Isolation state and for handling resource data requests.

PLUG AND PLAY INTERFACE DESCRIPTION

The Plug and Play communication to the PC is accomplished through three ports accessed through on-chip 12-bit ISA address decode: the Address port, the Write_Data port, and the Read_Data port. The Address and Write_Data ports are located at fixed addresses. The Read_Data port is re-locatable within an I/O range from 0x0203h to 0x03FFh.

Plug and Play (PnP) registers are accessed by the host PC by first writing the address of the desired register to the Address port. Once the address is written, access to the internal register is accomplished by reading from the Read_Data port or writing to the Write_Data port. The Address port does not need to be written each time the host performs sequential reads or writes from the same PnP Register.

The PnP Registers allow the host to isolate each card, assign a card select number (CSN), gather card resource data, assign interrupt levels and card I/O base addresses for the 550 resister set, check for memory range conflicts, and activate the card.

The SSI 73M2918/2918A firmware accesses state information, status, interrupt configuration, and data ports through several additional 8032 special function registers (SFR).

PLUG AND PLAY OPERATION

The SSI 73M2918/2918A defaults to a non Plug and Play device upon power-up. The firmware should enable the PnP function immediately following power-up if its card is installed in a Plug and Play host computer or host software support is provided in a pseudo-Plug and Play mode in a non PnP host.

If PnP mode is enabled, the 550 register set will not respond to reads or writes on the ISA bus until the host sets the PnP Activate register bit.

The major steps in the auto-configuration process are:

- Put all Plug and Play cards in the Isolation state.
- Isolate one Plug and Play card at a time.
- Assign a handle (card select number, CSN) and read the card's resource data structure.
- After the resource requirements and capabilities are determined for all cards, assign conflict free resources to each card.
- Activate all Plug and Play ISA cards and remove them from their configuration mode.

The SSI 73M2918/2918A will enter the Wait for Key state when the PnP mode is enabled.

Wait-for-Key State

The SSI 73M2918/2918A will not respond to any ISA accesses to its PnP interface until a defined sequence of writes to the Address port, referred to as the initiation key, is received. This "unlocking" procedure is required in order to protect against inadvertent writes by the host to the PnP configuration registers during normal operation.

An 8-bit linear feedback shift register (LFSR) that is initialized to 6Ah by a reset into the Wait for Key state, or whenever the Address port value written by the host does not match the current LFSR value in the Wait for Key state. The input to the MSB of the LFSR is the exclusive OR of its two LSBs. The host performs a sequence of 2 writes of 00h to the Address port to ensure a reset state prior to sending the initiation key. The host then writes the initial key value, 6Ah, to the Address port. For each write to the Address port, the contents of the LFSR are compared with the Address port. If they are equal, the LFSR is shifted to its next value. If the results differ, the LFSR is reset to its initial state of 6A.

The Initiation Key sequence is:

6A, B5, DA, ED, F6, FB, 7D, BE,
DF, 6F, 37, 1B, 0D, 86, C3, 61
B0, 58, 2C, 16, 8B, 45, A2, D1,
E8, 74, 3A, 9D, CE, E7, 73, 39

If 32 consecutive writes successfully compare, the SSI 73M2918/2918A is "unlocked" and enters the Sleep state. Upon transition to the Sleep state, the core microcontroller and the 550 UART register set are reset.

Sleep State

In the Sleep state, the SSI 73M2918/2918A waits for a Wake[CSN] command by the host. If its card select number (CSN) is a zero, and the data value written during the Wake[CSN] command is also a zero, the SSI 73M2918/2918A will enter the Isolation state. If the data value written during Wake[CSN] command is non zero and matches the SSI 73M2918/2918A's CSN, the SSI 73M2918/2918A will enter the Configuration state. The SSI 73M2918/2918A will transition to the Sleep state whenever a Wake[CSN] command is issued by the host and the data value does not match the SSI 73M2918/2918A's CSN.

Isolation State

Since all PnP cards respond to the same I/O port addresses, the host needs a mechanism to address only one particular card at a time during configuration modes. The Isolation state is used by the host to identify each Plug and Play card and assign each card a unique handle, its CSN. Each card must have a unique 72-bit identification number. The SSI 73M2918/2918A firmware will provide the PnP interface with each bit of serial card ID when required by the isolation protocol.

The first time the card enters the Isolation state, the host must write to the Rd_Data PnP Register to set the base ISA address for the Read_Data port. The set Rd_Data PnP Register can only be written to if the SSI 73M2918/2918A is in the Isolation state.

Isolation State (continued)

The host will initiate 72 pairs of read accesses of the Serial Isolation PnP Register to isolate a card. During each pair of reads, the SSI 73M2918/2918A will asset a 55h during the first read cycle followed by a AAh during the second read cycle, if the current bit in its serial identifier is a one. If the current ID bit is a zero, the SSI 73M2918/2918A will not drive onto the buss, but will look for a 01 followed by a 10 pattern for D[1:0] during the read pair to sense if another card is driving. If another card is driving, it has a higher ID number, and the SSI 73M2918/2918A losses arbitration. If the card's ID bit was a one or if no other card was detected forcing the buss, the next ID bit is examined and the card will continue to arbitrate during the next read pair. When the SSI 73M2918/2918A losses arbitration it will return to the Sleep state and will begin the arbitration process again on the next iteration of 72 read pairs only after the host writes another Wake[CSN] command with data equal to 00h.

Cards arbitrate on each bit, MSB first, during each read pair until only one card remains at the end of the 72-bit pair reads. When a card wins arbitration on all of its 72 ID bits, its CSN PnP Register will be written with its unique card select number and it will enter the Configuration state.

The host must delay 1 ms prior to starting the first pair of isolation reads, and must wait 250 µs between each subsequent pair of isolation reads. This allows the SSI 73M2918/2918A firmware plenty of time to write the next bit of serial identification to the PnP interface.

Configuration State

Card resource data may only be read during the Configuration state. The SSI 73M2918/2918A can get into the Configuration state by winning arbitration in the Isolation state and having a CSN assigned, or as a response to a Wake[CSN] command that matches the SSI 73M2918/2918A's CSN PnP Register value (CSN must be non zero). The host reads the card resource data by first polling a status bit in the Resource Status PnP Register to see if the next byte of resource data is available, and then reading the Resource Data PnP Register. A host read of the Resource Data Register will reset the resource status bit. The SSI 73M2918/2918A firmware is responsible for supplying the resource data bytes to the PnP Data Register.

If the SSI 73M2918/2918A enters the Configuration state from a Wake[CSN] command, it must supply 9 bytes of the serial identifier before the first byte of card resource data can be read. If the Configuration state is entered directly from the Isolation state, the SSI 73M2918/2918A will return resource data during the first read of the Resource Data PnP Register.

The host will also program the SSI 73M2918/2918A's PnP configuration registers that assign the card an interrupt level and set the I/O base address for the 550 registers while in the Configuration state (ie., Com1 or Com2).

While in the Configuration state, the host may initiate an I/O Range Check function to ensure that there are no conflicts for its programmed I/O range, and finally, activate the SSI 73M2918/2918A's 550 register set so it responds to reads and writes on the ISA buss.

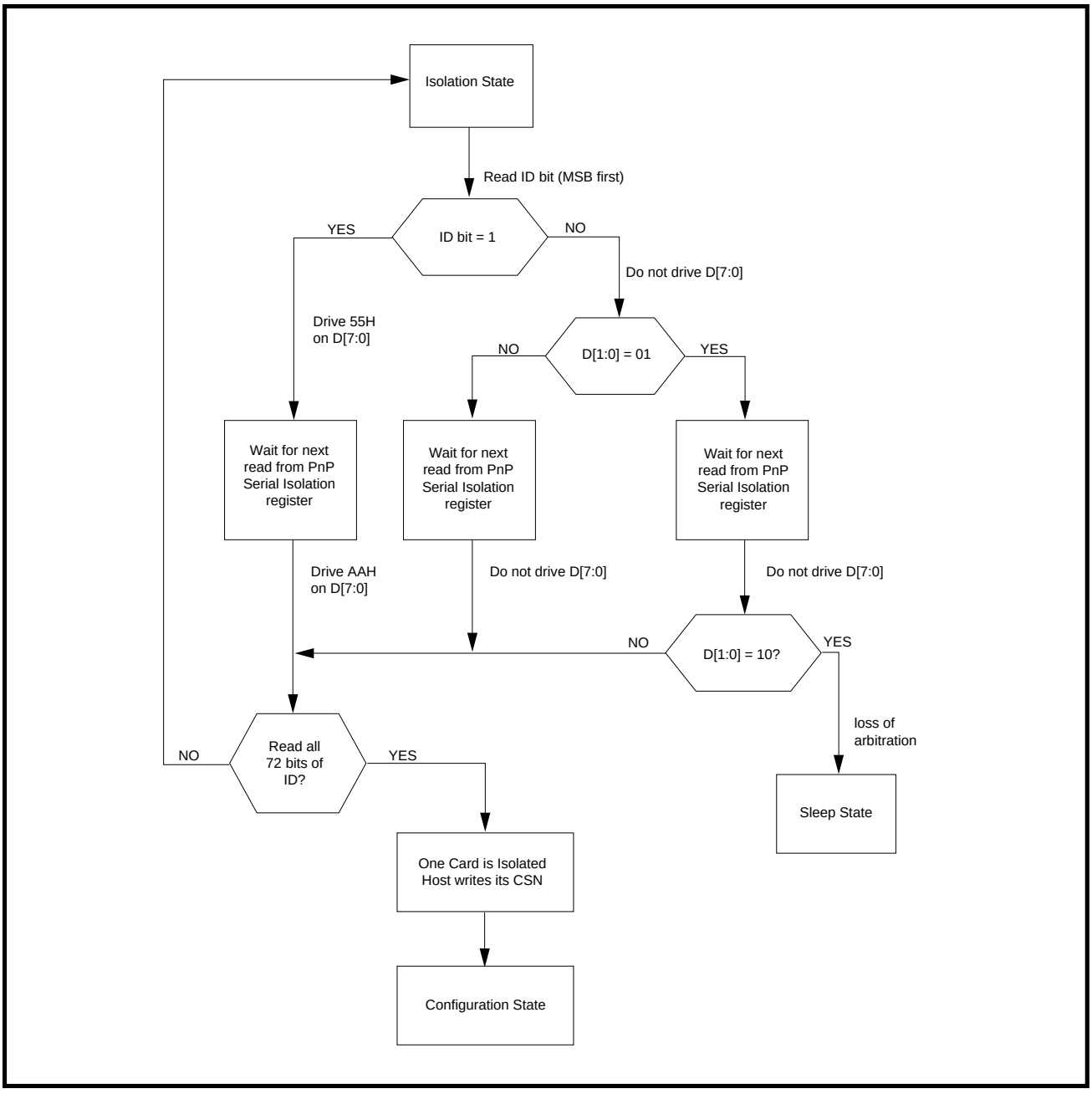


FIGURE 1: Isolation Protocol

REGISTER DESCRIPTION

AUTO-CONFIGURATION PORTS

Three 8-bit ports are used by the host PC to access the Plug and Play register set.

Address Port ISA Address 0279h

Reset State 00h

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
AD7	AD6	AD5	AD4	AD3	AD2	AD1	AD0

Write_Data Port ISA Address 0A79H

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
WD7	WD6	WD5	WD4	WD3	WD2	WD1	WD0

Data written to the Write_Data port is written to the PnP Register pointed to by the Address Register.

Read_Data Port ISA Address 00 (RD_Port Plug and Play)11B

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
RD7	RD6	RD5	RD4	RD3	RD2	RD1	RD0

Data read from the Read_Data port is provided by the PnP Register pointed to by the Address Register. The address of the Read_Data port is set by writing to the Set Rd_Data Port PnP Register during the Isolation state.

PLUG AND PLAY REGISTERS

ADDRESS	REGISTER/COMMAND	ACTIVE STATE	ACCESS
00h	Set Rd_Data Port	ISO	Write Only
01h	Serial Isolation	ISO	Read Only
02h	Configuration Control	ISO/Sleep/Configuration	Write Only
03h	Wake[CSN]	ISO/Sleep/Configuration	Write Only
04h	Resource Data	Configuration	Read Only
05h	Resource Status	Configuration	Read Only
06h	CSN (card select number)	ISO	Read/Write
07h	LDN (logical device number)	Configuration	Read Only
20h	Card Level Vendor Defined	Configuration	Read/Write
30h	Activate	Configuration	Read/Write
31h	I/O Range Check	Configuration	Read/Write (Bits 7:2 read back 0)
60h	I/O Base Address(High)	Configuration	Read/Write
61h	I/O Base Address(Low)	Configuration	Read/Write
70h	Interreupt Level	Configuration	Read/Write
71h	Interrupt Type	Configuration	Read/Write

PLUG AND PLAY REGISTER SUMMARY

Set Rd_Data Port This register sets the base address of the Read_Data Port. Bits [7:0] are used as I/O read port address bits [9:2]. This register can only be written during the Isolation state.

Serial Isolation In the Isolation state, reads of this register will yield an AAh, a 55h, or a high impedance response, depending upon the current value of the serial isolation bit and whether it is the first or second serial isolation register read operation on a given ID bit.

Configuration Control If the host writes a one to bit [0] of this register, the SSI 73M2918/2918A PnP interrupt and base address configuration registers will be reset to their power-up default states. The CSN is preserved.

If the host writes a one to bit [1] of this register, the SSI 73M2918/2918A will return to the Wait for Key state and all SSI 73M2918/2918A PnP registers are preserved.

A host write to bit [2] of this register will cause all cards to reset their CSN to zero.This register is write only. These values are not sticky, that is, the SSI 73M2918/2918A will clear these bits automatically.

Wake[CSN] Writing to this address when the SSI 73M2918/2918A is in the Sleep state will cause the SSI 73M2918/2918A to enter the Isolation state if its CSN is zero and the write data [7:0] is zero. If the hardware is in Sleep state and the CSN matches the write data and the write data isnot zero, the SSI 73M2918/2918A enters the Configuration state.

Resource Data When in the Configuration state, a read from this register retrieves the next byte of resource data.

Resource Status The host polls bit [0] of this register until it detects a one before a new byte is read from the Resource Data PnP Register. This bit is set when the SSI 73M2918/2918A firmware writes the Resource Data SFR Register. A host read of the Resource Data PnP Register will reset this bit.

CSN Card Select Number. Writing to this address sets the CSN, which is assigned to the card following the isolation process. This register is reset to 00h upon a power-up reset or when the host writes a one to bit [2] of the Configuration Control PnP Register.

LDN Host read of this register will return a value of 00h indicating that one logical device is supported.

Activate Bit [0], when set by the PC, enables the 550 UART interface if I/O Range Check is disabled. Bits [7:1] must return 0 on reads.

PLUG AND PLAY REGISTER SUMMARY (continued)

I/O Range Check	This register is used for performing a conflict check with the programmed I/O range for the 550 registers. Bit [1] enables the I/O range check mode if the activate bit is not set. In this mode, the SSI 73M2918/2918A will return a 55h if bit [0] is set whenever it detects a 550 register read. If bit [0] is a zero, an 0AAh will be returned during a 550 register read. If the I/O Range Check Register is read by the host, bits [7:2] must be return 0.
I/O Base Address	The I/O base registers occupy two bytes which are used to select the lower limit for the 550 UART register set address space. Since 10-bit decoding is used, only bits [9:3] are used for address decoding. Bits [2:0] of the low I/O base register are unused since the I/O addresses are assumed to be aligned to an 8-bit boundary.
Interrupt Level	Indicates the selected interrupt level. Bits [3:0] select which interrupt level is used for interrupt 0. A value of 01h selects IRQL 1 and a value of FFh selects IRQL fifteen. A value of 00h represents no interrupt selection.
Interrupt Type	Indicates which type of interrupt is used for the requested interrupt level. Bit [1] when high indicates an active high interrupt, and when low indicates an active low interrupt. The host sets bit [0] high for a level sensitive interrupt and low for an edge sensitive interrupt. Edge triggered interrupts are not supported by the SSI 73M2918, so bit [0] always returns a one.
Card Level	This register is available in Configuration state for communicating vendor specific information to and from the microcontroller firmware. All eight bits are accessable by the core microcontroller by reading the 550 UART Scratch Register.

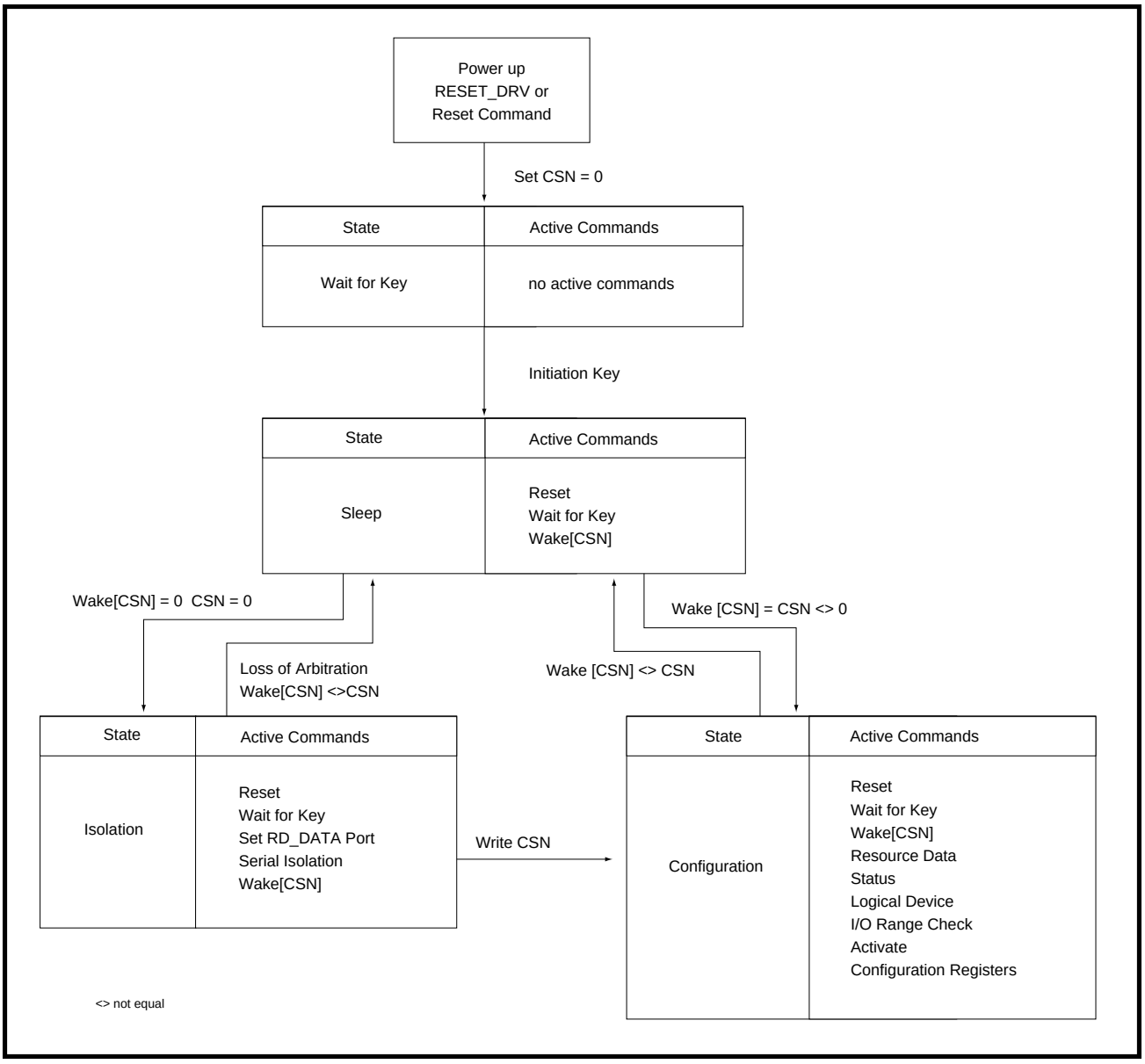


FIGURE 2: Plug and Play Configuration Flow Chart

PLUG AND PLAY REGISTERS (continued)

SSI 73M2918/2918A PLUG AND PLAY MICROCONTROLLER INTERFACE

The microcontroller interface provides PnP state information for the SSI 73M2918/2918A firmware through the addition special function registers that are unused in a normal 8032. The SSI 73M2918/2918A firmware is responsible for loading the next bit of the card's ID during the Isolation state and to load the next byte of the resource data during the Configuration state. The SSI 73M2918/2918A uC special function registers are also used in the interrupt level assignment. An interrupt level assignment register is used to determine which one of four possible IRQ pins has been assigned by the host.

PLUG AND PLAY STATUS REGISTER SFR ADDRESS 0BCh

Read Only Register
Reset = 20h

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Reset Configuration Flag	ISO State	W4 Key State	T2 CFG T2 ISO	Wk2 CFG	Active	RSRC Data Req.	ISO bit Data Req.

Bit 0 ISO Data Request Bit

This bit indicates that the Plug and Play hardware requires the next isolation ID bit and the SSI 73M2918/2918A is in the Isolation state. This bit gets reset following a write of the isolation ID bit and set after each pair of host reads of the Isolation PnP Register.

Bit 1 Resource Data Request Bit

This bit is set when the host first polls the Resource Status PnP Register if the resource status PnP bit [0] is a zero and the SSI 73M2918/2918A is in the Configuration state. This request bit will be reset when the SSI 73M2918/2918A firmware writes to the Resource Data SFR Register.

Bit 2 Active

This bit reflects the value of the PnP register's activate bit. If the activate bit is set, the 550 registers respond normally on the ISA bus and the SSI 73M2918/2918A firmware should begin its logical device function.

Bit 3 Wake[CSN] to Configuration State Transition Flag

This bit is set when the SSI 73M2918/2918A detects a Wake[CSN] command which is non-zero and matches the card's assigned CSN. The firmware will respond by writing the card's ID bytes for the first 9 host requests for resource data. This bit is reset when either the SSI 73M2918/2918A firmware writes to the Resource Data Register, by a PnP reset command, or by a hardware reset.

Bit 4 Configuration or Isolation State Transition Flag

This bit is set when the SSI 73M2918/2918A receives a Wake[CSN] command equal to zero if the Destination state is isolation, when the SSI 73M2918/2918A enters the Configuration state from Sleep state, or by a write to its CSN after winning arbitration.

When a resource data bye is requested, the firmware should first look to see if the Wake[CSN] to Configuration state flag (bit 3) is set. If this is a zero, then then the Configuration Isolation state transition flag should be examined. If this bit is set, and bit 3 is a zero, then the Configuration state was entered by a host assignment of the CSN at the end of arbitration. This indicates to the firmware that the resource data pointer should skip the ID bytes. If both bit 3 and bit 4 are zeros, the firmware gets the next byte of resource data and increments the resource data pointer.

This bit is reset when either the SSI 73M2918/2918A firmware writes to the Resource Data SFR Register, the firmware writes to the Isolation bit, or when a reset occurs.

Bits 6:5 Plug and Play State Bits

A 1 in a given state bit indicates that the Plug and Play hardware is currently in that state.

Bit 7 Reset Configuration Flag

This bit is set when the host executes a reset configuration command by writing a one to bit zero of the Configuration Control PNP Register. This bit is reset following a write to the Interrupt Line Select SFR Register.

PLUG AND PLAY CONTROL REGISTER SFR ADDRESS 0BCh
Write Only Register
Reset state = 00h

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
0	0	0	0	0	0	Activate	PnP Hardware Enable

Bit 0 Plug and Play Enable

Writing a logic 1 to this bit enables the Plug and Play hardware. This bit is reset following a hardware reset.

Bit 1 Activate

The value written to this bit is copied to the activate bit of the Plug and Play Activate Register.

Bits 7:2 Unused

RESOURCE/ISO DATA REGISTER SFR ADDRESS 0BDh
Write Only Register

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
RSRC7	RSRC6	RSRC5	RSRC4	RSRC3	RSRC2	RSRC1	RSRC0 ISO ID

Bits 7:0 Resource and ISO Data

The SSI 73M2918/2918A firmware writes PnP resource data to this register according to the resource data request, transition to Configuration state, and Sleep to Configuration state PnP status bits. In Isolation state, bit 0 is also the isolation serial ID bit. The SSI 73M2918/2918A firmware will write the card's serial ID into this bit as a response to the isolation data request and the transition to isolation status bits.

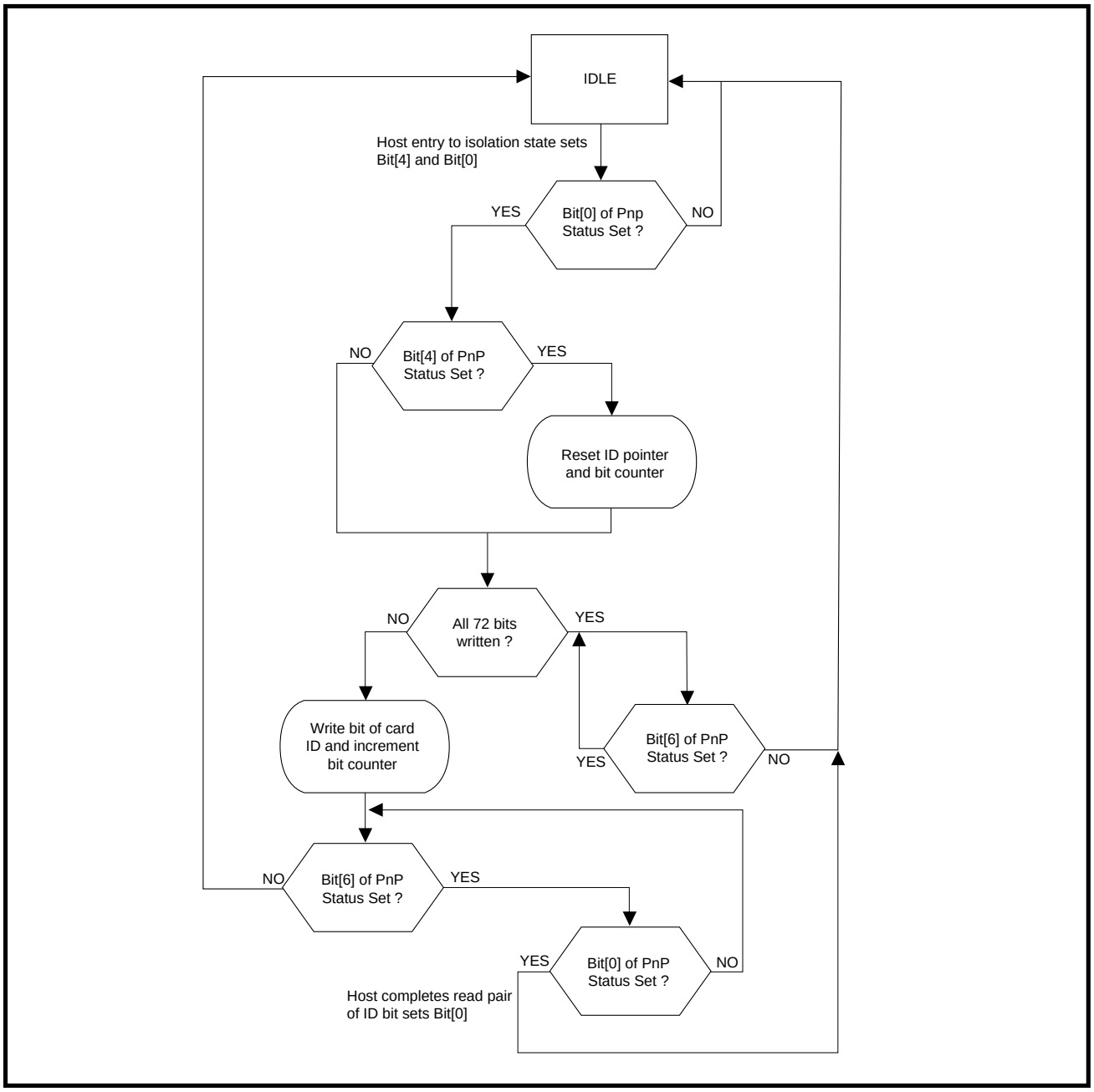


FIGURE 3: Isolation Data Algorithm

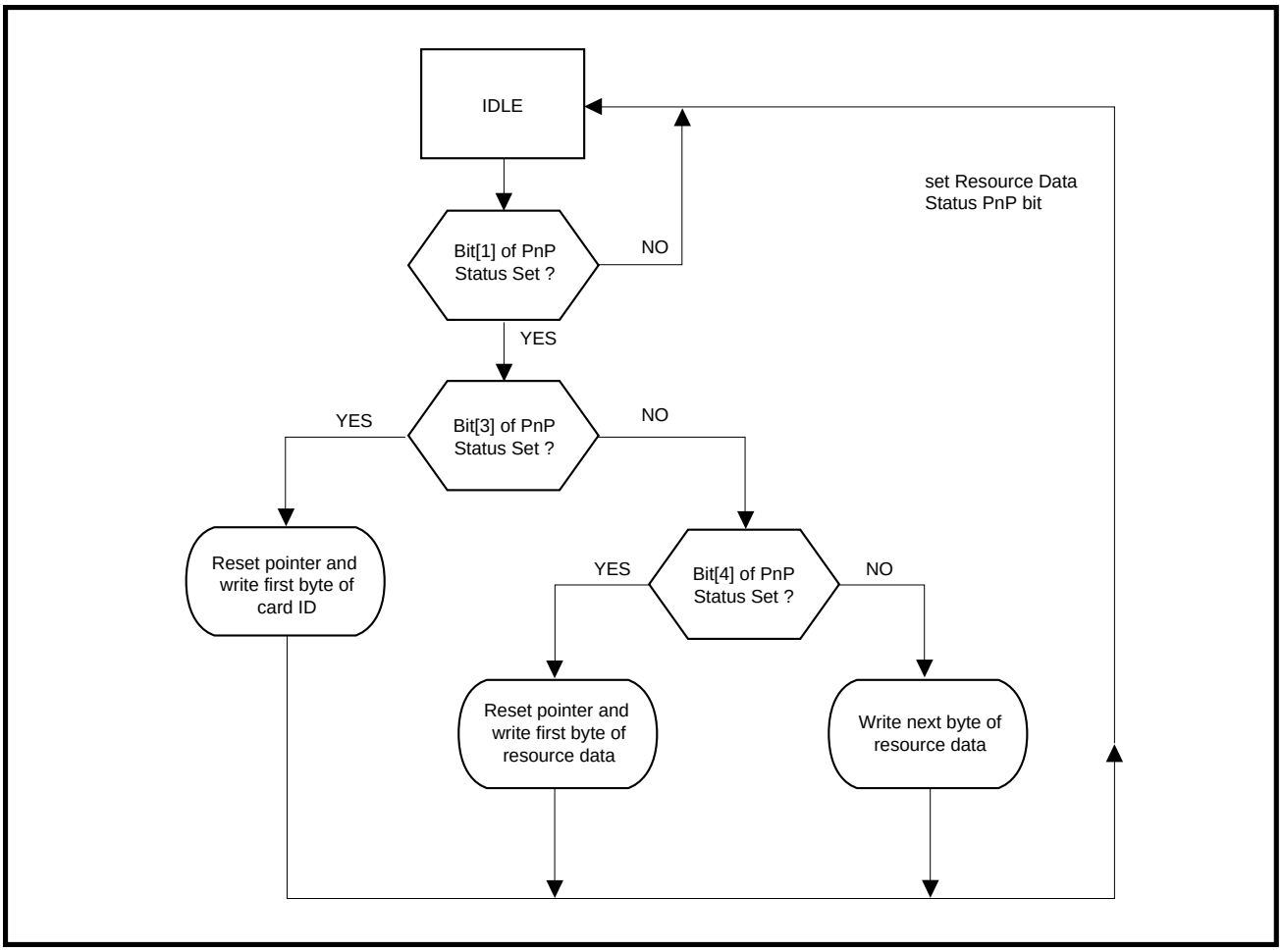


FIGURE 4: Resource Data Algorithm

REGISTER DESCRIPTION (continued)

73M2918 ISOLATION DATA ALGORITHM

When the microcontroller firmware detects a transition to the Isolation state, by polling the state bits (PNP Status Register, bits 7-4) and detecting a one in bit [4], the SSI 73M2918/2918A firmware writes the first bit of the card's unique ID number to the PNP Data SFR Register, bit [0]. When the host reads the Serial Isolation PnP Register, the SSI 73M2918/2918A drives the D[7:0] according to the Plug and Play specification for the isolation protocol. After each host read pair, the ISO data request bit, bit [0] is automatically set. This bit is polled by the core microcontroller firmware. When the firmware sees that this bit is set, it writes the next serial ID bit to PNP data register bit [0] which automatically resets the ISO data request bit. If the SSI 73M2918/2918A loses arbitration, it returns to the Sleep state. When the Isolation state is re-entered, bit [4] of the PNP Status Register will be set indicating to the SSI 73M2918/2918A firmware that it should begin again at the MSB of the card's ID.

73M2918 RESOURCE DATA ALGORITHM

While in the Configuration state, the host will read the card's resource data. The host will read the PnP Resource Status Register to see if data is available. A host read of this register will set the resource data request bit that is polled by the microprocessor firmware. When the SSI 73M2918/2918A firmware detects a resource data request, it will load a byte of resource data which will reset the resource data request bit and set the PnP resource status bit. The host then polls this bit, sees that data is now available, and reads the Resource Data PnP Register. The next time the host reads the data request status bit to see if the next byte of resource data is available, the resource data request bit will be set. This cycle is repeated until the host has read all of the resource data bytes and no longer polls the Resource Status PnP Register.

The SSI 73M2918/2918A firmware must also examine the Transition to Configuration state and the Wake to Configuration state transition bits. If the Wake to Configuration state bit is set, the firmware must start with the 9 bytes of card ID. If only the transition to configuration bit is set, it should skip the ID bytes and begin by sending the first byte of resource data.

73M2918 HOST INTERRUPTS

INTERRUPT LINE SELECT REGISTER SFR ADDRESS 0BEh

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
0	0	0	0	ID	IC	IB	IA

In Plug and Play mode the SSI 73M2918/2918A firmware writes the four bits represented in this register to determine which user selectable IRQ output pin, IRQA, IRQB, IRQC, or IRQD is active. When the host assigns an interrupt level during the configuration mode, the firmware can read the interrupt configuration via the Interrupt Configuration SFR Register and set these bits so that the correct SSI 73M2918/2918A IRQ output pin is driven. When bit 0 of the PnP data register is zero, the 550 UART interrupt is automatically connected to the IRQA output pin. When bit 0 of the PnP data register is set to a logic 1, the selection is as follows:

BIT 3	BIT 2	BIT 1	BIT 0	IRQ LINE
0	0	0	0	None
0	0	0	1	IRQA
0	0	1	0	IRQB
0	1	0	0	IRQC
1	0	0	0	IRQD

Bits 3:0 Interrupt Level Select

In Plug and Play mode, setting bits 3-0 cause the 550 UART interrupt to be connected to IRQD, IRQC, IRQB, IRQA respectively. Any given interrupt output pin is disabled when its corresponding bit is reset to zero. When bit 0 of the PnP data register is reset to a logic 0, these bits are disabled.

Bits 7:4 Unused

INTERRUPT CONFIGURATION SFR REGISTER SFR ADDRESS 0BFh
Read/Write Register

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
0	0	IT2	IT1	IL3	IL2	IL1	IL0

The core microcontroller firmware can read or write the pertinent bits of the Plug and Play interrupt level and interrupt type configuration registers via this register. In a Plug and Play system, the firmware can read the values programmed by the host software and configure the interrupt output pins accordingly by setting the appropriate bit in the Interrupt Line Select Special Function Register. In non Plug and Play systems, the microcontroller can load a pre-determined interrupt configuration by writing to this register.

Bits 3:0 Interrupt Level Value

These bits reflect the value stored in the least significant four bits of the PnP Interrupt Level Configuration Register.

INTERRUPT CONFIGURATION SFR REGISTER SFR ADDRESS 0BFh (continued)

Bits 5:4 Interrupt Type Value

These bits reflect the value stored in the least significant two bits of the PnP Interrupt Type Configuration Register.

Bits 7:6 Unused

IO BASE ADDRESS REGISTER SFR ADDRESS 0ACh
Read/Write Register

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
0	IOH1	IOH0	IOL7	IOL6	IOL5	IOL4	IOL3

The core microcontroller firmware can read or write the Plug and Play I/O Base Address configuration registers via this register. In non Plug and Play systems, the microcontroller can load a pre-determined I/O base address configuration by writing to this register.

Bits 4:0 IOL 7:3

These bits reflect the value stored in the most significant five bits of the PnP Lower I/O Base Address Configuration Register.

Bits 6:5 IOH 1:0

These bits reflect the value stored in the least significant two bits of the PnP Upper I/O Base Address Configuration Register.

Bit 7 Unused

If the PnP mode bit is reset to a 0, the base addresses for the 550 register set are determined by the COMSEL(2:1) pins as shown in the table below.

COMSEL2	COMSEL1	ALE550	ADDRESS RANGE
X	X	1	None
0	0	0	03F8-03FF
0	1	0	03E8-03EF
1	0	0	02F8-02FF
1	1	0	02F8-02EF

550 UART REGISTER DESCRIPTION

The 550 emulation circuitry includes two register sets, one for the host PC interface, referred to as Channel A, and one for the core microcontroller, referred to as Channel B. The host 550 emulation register set (Channel A) is compatible with the industry standard 550 UART register set. The function of the bits are identical to those of the 550 with the following exceptions:

1. The addition of the Silicon Systems enable bit (IER D5). This bit is write only. A read of this bit will always return a logic 0 value.
2. The RX timeout function is based on the bit rate clock from the SSI 73M2918/2918A core processor as controlled by the timeout clock source bits, MSR D(3:0), of the core microcontroller's 550 interface register set.
3. The loop bit (MCR D4) will loop transmit data into the receive FIFO (in parallel) every character period as controlled by the timeout clock source bits, MSR D(3:0), of the core microcontroller's 550 interface register set.
4. A transmit FIFO trigger-level feature has been added. This is available only if the Silicon Systems enable bit is set (IER D5) and FIFO mode (FCR D0) are set to a 1.
5. The 550 register bits OUT1 and OUT2 are used as uPRST and IE550 respectively and no longer connect to output pins.
6. The addition of an Silicon Systems mode bit to bit 7 of the modem control register, MCR. This bit can only be read and written if the Silicon Systems mode bit is enabled. This bit is used to identify the SSI 73M2918/2918A so communications software can take advantage of the special Silicon Systems modes.

REGISTER DESCRIPTION (continued)

SSI 73M550 UART EMULATION REGISTERS (CHANNEL A)

REGISTER		ADDRESS	D7	D6	D5	D4	D3	D2	D1	D0
Receive Buffer Register	RBR	0 (DLAB=0) (Rd Only)	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Transmit Holding Register	THR	0 (DLAB=0) (Wr Only)	Bit7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Interrupt Enable Register	IER	1 (DLAB=0)	0	0	Silicon Systems Enable (WrOnly)	0	Enable Modem Status	Enable Receiver Status	Enable THRE	Enable RDA
Interrupt ID Register	IIR	2 (Rd Only)	FIFOs Enabled	FIFOs Enabled	RX RDY (Silicon Systems Mode)	TX RDY (Silicon Systems Mode)	Interrupt ID 2	Interrupt ID 1	Interrupt ID 0	Interrupt Pending
FIFO Control Register	FCR	2 (Wr Only)	RX FIFO Trigger 1	Rs FIFO Trigger 0	TX FIFO Trigger 1	TX FIFO Trigger 0	DMA Mode Select	TX FIFO Reset	RX FIFO Reset	FIFO Enable
Line Control Register	LCR	3	Divisor Latch Access	Set Break	Stick Parity	Even Parity	Parity Enable	Number Stop	Word Length Select 1	Word Length Select 0
Modem Control Register	MCR	4	Silicon Systems Mode	0	0	Loop	Enable Interrupt	uPRST	RTS	DRT
Line Status Register	LSR	5	Error in RX FIFO	TX FIFO Empty	Transmit Holding Empty	Break Interrupt (BI)	Framing Error (FE)	Parity Error (PE)	Overrun Error (OE)	Data Ready (DR)
Modem Status Register	MSR	6 (Rd Only)	DCD	RI	DSR	CTS	Delta DCD (DDCD)	Trailing Edge RI (TERI)	Delta DSR (DDSR)	Delta CTS (DCTS)
Octet Scratch Register	SCR	7	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Divisor Latch (LS)	DLL	0 (DLAB=1)	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Divisor Latch (MS)	DLM	1 (DLAB=1)	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0

CORE MICROCONTROLLER 550 REGISTER SET (CHANNEL B)

The following table is the register set facing the SSI 73M2918/2918A core processor that is used for 550 emulation. The addresses are encoded into the SFR register block within the SSI 73M2918/2918A core processor's memory map. All registers are byte addressable. The Line Status Register is both byte and bit addressable.

REGISTER		ADDRESS	D7	D6	D5	D4	D3	D2	D1	D0
TX FIFO Output Register	TOR	B1 (Rd Only)	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
RX FIFO Input Register	RIR	B1 (Wr Only)	Bit7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Interrupt Enable Register	IER	B2	Rx FIFO Ready Mode	Enable TX FIFO Full	Enable RX FIFO Ready	Enable UART Interrupt	Enable MCR/SCR Status	Enable Divisor LCR stat	Enable RX FIFO Empty	Enable TX FIFO Data Available
Interrupt ID Register	IIR	B3 (Rd Only)	FIFOs Enabled	UART Interrupt Pending	B-Ch Interrupt Pending	0	0	Interrupt ID 2	Interrupt ID 1	Interrupt ID 0
Line Control Register	LCR	B4 (Rd Only)	Divisor Latch Access	Set Break	Stick Parity	Even Parity	Parity Enable	Number Stop	Word Length Select 1	Word Length Select 0
Modem Control Register	MCR	B5 (Rd Only)	MCR Status Change	RX Trigger 1	RX Trigger 0	Loop	Enable Interrupt	uPRST	RTS	DTR
Line Status Register	LSR	B0	RX FIFO Full	RX FIFO Ready	RX FIFO Empty	Break Interrupt (B)	Framing Error (FE)	Parity Error (PE)	Overrun Error (OE)	TX FIFO Not Empty
Modem Status Register	MSR	B6	DCD	RI	DSR	CTS	Timeout Pace Clk Src B1	Timeout Pace Clk Src B0	Manual RX FIFO Timeout	0
Octet Scratch Register	SCR	B7	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Divisor Latch (LS)	DLL	BA (Rd Only)	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Divisor Latch (MS)	DLM	BB (Rd Only)	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Character Pacing Register	CPR	B9	0	0	Alt2	Alt	RX Pace Clock Overflow	TX Pace Clock Overflow	RX Pace Enable	TX Pace Enable

REGISTER DESCRIPTION (continued)

RECEIVER BUFFER (READ),TRANSMITTER HOLDING REGISTER (WRITE) ADDRESS 0 (DLAB=0)

Reset State 00h

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
DAT7	DAT6	DAT5	DAT4	DAT3	DAT2	DAT1	DAT0

When this register address is read, it contains the parallel received data. Data to be transmitted is written to this register address.

INTERRUPT ENABLE REGISTER (IER) ADDRESS 1

Reset State 00h

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
0	0	Silicon Systems Mode Enable (Read = 0)	0	Enable MODEM Status Interrupt	Enable Line Status Interrupt	Enable THRE Interrupt	Enable RX Data Interrupt

This 8-bit register enables the five types of interrupts described below. Each interrupt source can activate the IRQ output signal if enabled by this register. Resetting bits 0 through 3 will disable all 550 interrupts.

Bit 0 Enable Received Data Available Interrupt

Writing a 1 to this bit enables the received data available interrupt, and timeout interrupts in FIFO mode.

The received data available interrupt is issued when either the FIFO has reached its programmed trigger level if FIFO mode is enabled. It is cleared as soon as the FIFO drops below its programmed trigger level. If FIFO mode is not enabled, a received data available interrupt will occur if the receive FIFO has data and will be cleared when this data is read and the FIFO is empty.

The timeout interrupt will occur if the following conditions exist:

1. At least one character is in the FIFO.
2. The RX FIFO has not been written to or read from in a specified timeout period. This timeout period is controlled by the microprocessor software through its Channel B MSR register bits D(3:1).

Bit 1 Enable Transmitter Holding Register Empty Interrupt

Writing a 1 to this bit enables the Transmitter Holding Register empty interrupt. This interrupt is issued when the TX FIFO is at or below the programmed trigger level if Silicon Systems mode is enabled. If Silicon Systems mode is not enabled, this interrupt occurs when the FIFO is empty if the ALT2 bit is low , or when the second byte in the TX FIFO is empty if the ALT2 bit is set. It is cleared as soon as the transmit FIFO is above the trigger level in Silicon Systems mode or when the FIFO is written if not in Silicon Systems mode. If the ALT2 bit is set, and the TX FIFO is empty, there is a 1 to 2 bit period delay from when the THRE interrupt is asserted after the first byte is written. This imitates the behavior of a traditional 550 device, where the transmit holding register contents are transferred to the TX Serial Shift Register. There is at least 1 bit period between the transmit holding register write and another THRE interrupt.

Bit 2 Enable Receiver Line Status Interrupt

Writing a 1 to this bit enables the receiver line status Interrupt. This interrupt is generated whenever Line Status Register error conditions (LSR bits D1-D4) occur. This interrupt is cleared by reading the Line Status Register.

Bit 3 Enable Modem Status Interrupt

Writing a 1 to this bit enables the modem status interrupt. This interrupt is generated if either bits D0, D1, D2 or D3 of the Modem Status Register are set to a logic 1. This interrupt is cleared by reading the Modem Status Register.

Bit 4 Unused

Bit 5 Silicon Systems Enable

Writing a 1 to this bit enables Silicon Systems mode in which the transmit THRE trigger level is set via bits D4 and D5 of the FIFO Control Register. This bit is returned as a 0 when read.

Bits 6:7 Unused

INTERRUPT ID REGISTER (IIR) ADDRESS 2
Read Only Register
Reset State 01h

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
FIFOs Enable	FIFOs Enable	RXRDY (Silicon Systems Mode)	TXRDY (Silicon Systems Mode)	INTID2	INTID1	INTID0	INT PEND

The IIR Register gives prioritized information as to the status of interrupt conditions. When accessed, the IIR indicates the highest priority interrupt that is pending as indicated by bits INTD(2-0).

Bit 0 Interrupt Pending

This bit can be used in either a prioritized interrupt or in a polled environment to indicate whether an interrupt is pending. When bit 0 is a logic 0, an interrupt is pending and bits INTD(2-0) may be used as a pointer to the appropriate interrupt service routine. When bit 0 is a logic 1, no interrupt is pending.

Bits 1:3 Interrupt ID Bits

These three bits of the IIR are used to identify the highest priority interrupt pending as indicated in the following table. Bit D3 is reset to logic 0 when FIFO mode is disabled.

INTERRUPT ID REGISTER (IIR) ADDRESS 2 (continued)

Bit 4 Silicon Systems Mode TX RDY

If Silicon Systems mode (IER-D5) is set to logic 0, TX RDY is forced to logic 0. If Silicon Systems mode (IER-D5) is set to logic 1, and the TX FIFO is enabled, and DMA mode select is enabled, TX RDY is set when the level in the TX FIFO drops to the trigger level. It is reset when the FIFO is filled. If the TX FIFO is not enabled or DMA mode is not enabled, TX RDY is set when the transmit FIFO is empty.

Bit 5 Silicon Systems Mode RX RDY

A logic 0 indicates that the RX FIFO is empty. If Silicon Systems mode (IER-D5) is set to logic 1, and FIFOs are enabled (FCRD0), and DMA mode select is enabled (FCR-D3), this bit is set to a logic 1 when the FIFO reaches the trigger level, or a programmable timeout occurs, and cleared when the FIFO is empty. If FIFOs are not enabled or DMA mode select is not enabled, RX RDY is cleared when the RX FIFO is empty and set when it is not empty.

Bits 6:7 FIFOs Enabled

These two bits are set to logic 1 when FCR-D0 is set to 1 (FIFO mode enabled). They are reset to logic 0 when FCRD0 is reset to logic 0 (FIFO mode disabled).

D3	D2	D1	D0	PRIORITY	TYPE	SOURCE	RESET
0	0	0	1		None	None	N/A
0	1	1	0	Highest	Receiver Line Status	Overrun Error, Parity Error, Framing Error or Break Interrupt	Reading the Line Status Register
1	1	0	1	Second	Receive Data Indicator	Receive Data Avaliable or RX FIFO trigger level reached	Reading the Receiver Buffer Register, or when the RX FIFO drops below the trigger level
1	1	0	0	Second	Character Timeout Indicator	No chartacters have been read from or written to the RX FIFO during a programmed time interval and the RX FIFO is not empty	Reading the Receiver Buffer Register
0	0	1	0	Third	Transmit Holding Register Empty	Transmit Holding Register Empty or below TX FIFO trigger level	Reading IIR Register (if source of interrupt) or trigger level reached
0	0	0	0	Fourth	Modem Status	Clear to Send or Data Set Ready or Ring Indicator or Data Carrier Set	Reading the Modem Status Register

FIFO CONTROL REGISTER (FCR) ADDRESS 2
Write Only Register
Reset State 00h

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
RCV TRIG 1	RCV TRIG 0	XMT TRIG 1	XMT TRIG 0	DMA MODE	TX FIFO RST	RX FIFO RST	FIFO ENBL

This is a write only register at the same address as the IIR read only register. This register is used to enable the FIFOs, clear the FIFOs, set the TX and RX FIFO trigger level, and select the type of DMA signaling.

Bit 0 FIFO Enable

Writing a logic1 to this bit enables the transmit and receive FIFOs. The RX FIFO is always enabled to accept data from microcontroller writes but the RX data available interrupts are generated as if this was a single byte buffer if FIFO mode is disabled. Writing a logic 0 clears all bytes in both FIFOs.

Bit 1 RX FIFO Reset

Writing a logic1 to this bit clears the RX FIFO. The bit clears itself upon clearing the FIFO.

Bit 2 TX FIFO Reset

Writing a logic1 to this bit clears the TX FIFO. The bit clears itself upon clearing the FIFO.

Bit 3 DMA Mode Select

Writing a logic1 to this bit enables DMA mode 1. In this mode, bits D4 and D5 in IIR support multiple DMA transfers. Resetting this bit to a logic 0 will enable bits D4 and D5 to support single DMA transfers.

Bits 4:5 Silicon Systems Mode TX Trigger

These bits determine the TX FIFO trigger level as described in the table below. The THRE interrupt will occur if the TX FIFO is below the trigger level and will reset when the TX FIFO is filled to the trigger level is Silicon Systems mode is enabled. If Silicon Systems mode is not enabled, these bits are ignored.

BIT 5	BIT 4	TX FIFO TRIGGER LEVEL
0	0	1 byte
0	1	4 bytes
1	0	8 bytes
1	1	14 bytes

FIFO CONTROL REGISTER (FCR) ADDRESS 2 (continued)

Bits 6:7 RCV Trigger

These bits determine the RX FIFO trigger level as described in the table below. The received data available interrupt will occur if the RX FIFO is filled to or above the trigger level and will reset when the RX FIFO drops below the trigger level.

BIT 7	BIT 6	RX FIFO TRIGGER LEVEL
0	0	1 byte
0	1	4 bytes
1	0	8 bytes
1	1	14 bytes

LINE CONTROL REGISTER (LCR) ADDRESS 3
Reset State 00h

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
DLAB	SBRK	STP	EPS	PEN	STB	WLS1	WLS0

This register is available to maintain compatibility with the standard 550 register set and provides information to the internal hardware that is used to determine the number of bits per character. The word length and parity bits are used in determining character time for timeout, character pacing, and loopback functions. All of these bits can be read by the microcontroller through the Channel B LCR Register.

Bits 0:1 Word Length Select

These bits specify the number of bits in each transmitted or received character. This does not affect data transfers into or out of the RX and TX FIFOs. The encoding is as follows:

BIT 7	BIT 6	CHARACTER LENGTH
0	0	5 bits
0	1	6 bits
1	0	7 bits
1	1	8 bits

Bit 2 Stop Bit Control

Indicates a request by the PC to specify the number of stop bits in each transmitted character. If bit 2 is a logic 0, one stop bit is requested in each transmitted character. A logic 1 indicates a request for one and a half stop bits to be generated when a 5 bit word length is selected. When a 6, 7, or 8 bit word length is selected, a logic 1 indicates a request for two stop bits to be generated.

Bit 3 Parity Enable Bit

A logic 1 indicates that the PC has enabled parity generation and checking.

Bit 4 Even Parity Select Bit

A logic 1 indicates that the PC is requesting that even number of logic 1s be transmitted or checked. A logic 0 indicates that the PC is requesting odd parity generation and checking.

Bit 5 Stick Parity Bit

If bits 3 and 4 are logic 1, bit 5 set to logic 1 indicates that the PC is requesting that the parity bit be checked or transmitted as a logic 0. If bit 3 is set to logic 1 and bit 4 is set to logic 0, then the PC is requesting that the parity bit is transmitted and checked as a logic 1. If bit 5 is logic 0, then stick parity is disabled.

Bit 6 Break Control Bit

When set to a logic 1, a break condition is indicated.

Bit 7 Divisor Latch Access Bit

The divisor latch access bit must be set to logic 1 to access the divisor latches of the baud generator during a read or write operation. It must be set to logic 0 to access the receiver buffer, the Transmitter Holding Register, or the Interrupt Enable Register.

MODEM CONTROL REGISTER (MCR) ADDRESS 4
Reset State 00h

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Silicon Systems Mode	0	0	LOOP	IE550	µPRST	RTS	DTR

Bit 0 Data Terminal Ready (DTR)

This bit asserts a data terminal ready condition that is readable by the SSI 73M2918/2918A core processor, via the Channel B register bit (MCR-D0).

Bit 1 Request to Send (RTS)

This bit asserts a request to send condition that is readable by the SSI 73M2918/2918A core processor, via the Channel B register bit (MCR-D1).

Bit 2 Microprocessor Reset (µPRST)

Writing a logic 1 to this bit generates a reset pulse to the SSI 73M2918/2918A core processor. The reset is released a few microseconds after the write occurs. Channel A registers are not affected by this reset.

Bit 3 Interrupt Enable 550

When bit 3 is set to a logic 1, interrupt output is enabled on the IRQ pin. When set to a logic 0, the IRQ pin is forced into a high impedance state.

Bit 4 Loop

This bit provides a local loopback feature for testing the host transmit and receive datapaths. When set to a 1, the transmit data is loaded into the receive FIFO every character time. The number of bits per character is determined by the LCR(D3-D0). Bit rate is controlled by one of the programmable timers (Timer0, Timer1 or Timer2), as selected by the timeout clock source bit (MSR D3) of the core-processor interface register set. Also, the four modem status register bits CTS(MSR0), DSR(MSR1), RI(MSR2), and DCD(MSR3) are internally connected to the modem control register bits RTS(MCR1), DTR(MCR0), uPRST(MCR2), and interrupt enable(MCR3) respectively. The IRQ pin is forced into a high impedance state and the microprocessor reset bit (D2) will not result in a microprocessor reset if set.

Bits 5:6 Unused

MODEM CONTROL REGISTER (MCR) ADDRESS 4 (continued)

Bit 7 Silicon Systems Mode Identification

This bit can only be written and read if the enable Silicon Systems mode bit, bit 5 of the IER Register, is set. Otherwise, this bit is read as a 0. This bit is used by communications software packages to identify chips with the special Silicon Systems modes.

LINE STATUS REGISTER (LSR) ADDRESS 5
Reset State 60h

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
RCVE	TEMT	THRE	BI	FE	PE	OE	DR

This register provides status information to the host PC concerning the data transfer. Bits D1-D4 are the error conditions that produce a receiver line status interrupt whenever any of the corresponding conditions are detected. The Line Status Register is intended for read operation only.

Bit 0 Receiver Data Ready Indicator

Set to logic 1 when a received character is available in the RX FIFO. This bit is reset to logic 0 when the RX FIFO is empty.

Bit 1 Overrun Error Indicator

An overrun error will occur only after the RX FIFO is full and the next character has overwritten unread FIFO data. The bit is reset upon reading the Line Status Register.

Bit 2 Parity Error Indicator

A value of logic 1 indicates that a received character does not have the correct even or odd parity as selected by the even parity select bit. This error is set when the corresponding character is at the top of the RX FIFO It will remain set until the host reads the LSRI. The parity error indication is written into the RX FIFO by the Channel B LSR register bit 2 with its corresponding data byte.

Bit 3 Framing Error Indicator

A value of logic 1 indicates that the stop bit, following the parity bit, or the last data bit, is detected to be a logic 0. This bit is set to logic 1 when the character containing the framing error is at the top of the receive FIFO. It will remain set until the host PC reads the LSR. The framing error indication is written into the receive FIFO by the Channel B LSR register bit 3 with its corresponding data byte.

Bit 4 Break Interrupt Indicator

A value of logic 1 indicates that the received character contains more than a full word transmission time of logic 0 (Spacing state). This bit is set to logic 1 when the character containing the break interrupt indication is at the top of the RX FIFO. It will remain set until the host PC reads the LSR. The break interrupt indication is written into the receive FIFO by the Channel B LSR register bit 4 with its corresponding data byte.

Bit 5 Transmitter Holding Register Empty Indicator

A logic 1 indicates that the SSI 73M2918/2918A is ready for a new character for transmission. Bit 5 is reset to logic 0 when the host CPU loads a character into the TX FIFO. If the ALT2 mode bit in the character pacing SFR is set, the THRE indication will be asserted again in 1 to 2 bit periods (as dictated by the pacing timer) if the first 2 locations of the TX FIFO are not full and the device is not in FIFO mode. This imitates the behavior of a traditional 550 device where there is a Transmit Holding Register and a Serial TX Shift Register. The contents of the holding register are transferred to the TX Shift Register when it is empty. The THRE indication will remain low for at least one bit period from the time the TX Holding Register is written.

If FIFO mode and Silicon Systems mode are enabled, this bit is set when the TX FIFO is filled below the trigger level and reset when the FIFO is filled to the trigger level.

Bit 6 Transmitter Empty Indicator

Set to a logic 1 whenever the transmit FIFO is empty. It is reset to 0 when the transmit FIFO contains a character.

Bit 7 Receive FIFO Error Indicator

Set to logic one if there is at least one parity error, framing error, or break indication in the receive FIFO.

MODEM STATUS REGISTER (MSR) ADDRESS 6
Read Only Register
Reset State 00h

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
DCD	RI	DSR	CTS	DDCD	TERI	DDSR	DCTS

This register provides the current state of the control signals from the modem or peripheral device. In addition, four bits provide change information. Whenever bit D0, D1, D2 or D3 are set to logic 1, a modem status interrupt is generated. The status change indicators (bits 3-0) are reset to logic 0 after this register is read. In loop mode, CTS, DSR, RI and DCD are taken from RTS, DTR, uPRST, and IE550 of the Modem Control Register, respectively.

Bit 0 Delta Clear to Send (DCTS)

This bit is set when the CTS bit from the Channel B Modem Status Register (MSR-D4) has changed since the last time it was read by the host PC. This bit is cleared following a read of the MSR Register.

Bit 1 Delta Data Set Ready (DDSR)

This bit is set when the DSR bit from the Channel B Modem Status Register (MSR-D5) has changed since the last time it was read by the host PC. This bit is cleared following a read of the MSR Register.

Bit 2 Trailing Edge of the Ring Indicator (TERI)

This bit is set when a falling edge of the RI bit from the Channel B Modem Status Register (MSR-D6) has been detected since the last time it was read by the host PC. This bit is cleared following a read of the MSR Register.

Bit 3 Delta Data Carrier Detect (DDCD)

This bit is set when the DCD bit from the Channel B Modem Status Register (MSR-D7) has been set since the last time it was read by the host PC. This bit is cleared following a read of the MSR Register.

MODEM STATUS REGISTER (MSR) ADDRESS 6 (continued)

Bit 4 Clear to Send (CTS)

This bit reflects the value of the CTS bit from the Channel B Modem Status Register (MSR-D4).

Bit 5 Data Set Ready (DSR)

This bit reflects the value of the DSR bit from the Channel B Modem Status Register (MSR-D5).

Bit 6 Ring Indicator (RI)

This bit reflects the value of the RI bit from the Channel B Modem Status Register (MSR-D6).

Bit 7 Data Carrier Detect (DCD)

This bit reflects the value of the DCD bit from the Channel B Modem Status Register (MSR-D7).

SCRATCH REGISTER (SCR) ADDRESS 7
Reset State 00h

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
DAT7	DAT6	DAT5	DAT4	DAT3	DAT2	DAT1	DAT0

This 8-bit read/write register does not control the circuit operation in any way. It is intended as a scratch pad register to be used by the programmer to hold data temporarily. This register can also be written or read by the core microcontroller.

DIVISOR LATCH (DLL) ADDRESS 0 (DLAB=1)
Reset State 00h

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
DAT7	DAT6	DAT5	DAT4	DAT3	DAT2	DAT1	DAT0

This register contains baud rate information from the host PC. The PC sets the Divisor Latch Register values.

DIVISOR LATCH (DLM) ADDRESS 1 (DLAB=1)
Reset State 00h

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
DAT7	DAT6	DAT5	DAT4	DAT3	DAT2	DAT1	DAT0

This register contains baud rate information from the host PC.

CORE PROCESSOR - 550 REGISTERS (CHANNEL B)

The following registers are accessed by the SSI 73M2918/2918A core microcontroller. The addresses are encoded into the SFR register block within the microcontroller's memory map. All the registers are byte addressable. The Line Status Register is both byte and bit addressable.

The Channel B Register set allows communication to and from the DTE. Interrupts to the microprocessor can be generated by the following conditions:

-The RX FIFO is empty

-The RX FIFO is not full

-The TX FIFO is full

-The TX FIFO is not empty

-The TX FIFO is full and has been overwritten

-TXFIFO timeout - the TX FIFO is not empty and no characters have been read or written in one character time

-The host PC has written either the MCR or the SCR Register

-The host PC has written either the DLL/DLM or the LCR Register

The interrupt sources are enabled by the Channel B Interrupt Enable Register. The interrupt generated by the 550 register set is shared with the normal 8032 serial UART interrupt. The UART interrupt is enabled by bit 4 of the Channel B Interrupt Enable Register. The microprocessor must determine if the interrupt was generated by the serial UART or by the 550 register set if both are used. Bit 6 of the Channel B Interrupt ID Register is set if the serial UART interrupt is pending.

The SSI 73M2918/2918A parallel interface eliminates the need for parallel to serial or serial to parallel conversion of data to the PC and microprocessor. Many applications require a time base for loopback, RX FIFO and TX FIFO timeouts and pacing of interrupts from the 550 register set. This time base can come from either Timer0, Timer1 or Timer2 overflow outputs as selected by bits 2 and 3 of the MSR Register. It is assumed that these timers are set to 16x the bit rate as specified in the DLL and DLM Registers.

Since there is no serial to parallel or parallel to serial conversion of data from the PC to the microprocessor, interrupts can be generated immediately from when the host PC reads or writes data to the FIFOs. This allows bursts of data to be transferred. For some applications this can be a problem if the time in interrupt routines is too long or if the host PC is overwhelmed with data. The SSI 73M2918/2918A offers a pacing mode which limits the rate of RX FIFO and TX FIFO available interrupts to the microprocessor. The programmer can set up the 550 interface to get interrupts at exactly the same rate as if a serial UART was used by programming an available timer and setting up the SSI 73M2918/2918A's character pacing register. The programmer can also use the FIFOs in a burst mode, reading or writing 16 characters at a time from the FIFOs, and use the character timers to space RX FIFO empty and TX FIFO full interrupts.

REGISTER DESCRIPTION (continued)

TRANSMIT FIFO OUTPUT (READ), RECEIVER FIFO INPUT REGISTER (WRITE) ADDRESS 0B1

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
DAT7	DAT6	DAT5	DAT4	DAT3	DAT2	DAT1	DAT0

When this register address is read, it accesses the Transmit FIFO Output Register. When the SSI 73M2918/2918A core microcontroller writes data to this register address, it is loading data into the receive FIFO.

INTERRUPT ENABLE REGISTER (IER) ADDRESS 0B2

Reset State 10h

This register contains enable bits for interrupts to the SSI 73M2918/2918A core microcontroller.

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
RX FIFO Ready Mode	Enable TX FIFO Full	Enable RX FIFO Ready	Enable UART Interrupt	Enable mcr/scr Status	Enable Divisor LCR Status	Enab RX FIFO Empty	Enable TX FIFO Data Availiable

Bit 0 Enable TX FIFO Data Available Interrupt

Writing a 1 to this bit enables an interrupt to the SSI 73M2918/2918A core microcontroller when the transmit FIFO is not empty.

Bit 1 Enable Receive FIFO Empty Interrupt

Writing a 1 to this bit enables an interrupt to the SSI 73M2918/2918A core microcontroller when the receive FIFO is empty. After the interrupt is serviced, further interrupts are disabled by hardware while it remains empty. This interrupt is automatically re-enabled by hardware following a write to the RX FIFO or when the interrupt enable register is written. This circuitry allows a receive FIFO empty interrupt to occur only when the receive FIFO transitions to the empty state, thereby eliminating a continuous stream of unnecessary interrupts.

Bit 2 Enable Divisor/LCR Status Interrupt

Writing a 1 to this bit enables an interrupt to the SSI 73M2918/2918A core microcontroller when the registers DLL, DLM, or LCR of the Channel A 550 register set are written.

Bit 3 Enable MCR/SCR Status Interrupt

Writing a 1 to this bit enables an interrupt to the SSI 73M2918/2918A core microcontroller when either the MCR or SCR Register of the Channel A 550 register set is written.

Bit 4 Enable UART Interrupt

The 550 interrupt to the core microcontroller is shared with the normal UART 8032 interrupt vector. A logic 1 value for this bit enables an interrupt from the core microcontroller's UART. This bit is automatically set following a hardware reset. Clearing this bit disables the interrupt from the microcontroller's UART.

Bit 5 Receive FIFO Ready Interrupt

Writing a 1 to this bit enables an interrupt to the SSI 73M2918/2918A core microcontroller when the receive FIFO is below the trigger level and the receive FIFO ready mode bit (IER-7) is a logic 0 or when the receive FIFO is not full and the receive FIFO rready mode bit is set to a logic 1.

Bit 6 Enable Transmit FIFO Full Interrupt

Writing a 1 to this bit enables an interrupt to the SSI 73M2918/2918A core microcontroller when the transmit FIFO is full or when a transmit FIFO timeout has occurred.

Bit 7 Receive FIFO Ready Mode

When this bit is set to a logic 1, a receive FIFO ready interrupt will occur if the receive FIFO is not full. When this bit is logic 0, this interrupt will occur only when the receive FIFO is below the trigger level.

INTERRUPT ID REGISTER (IIR) ADDRESS 0B3
Read Only Register
Reset State 07h

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
FIFOs Enabled	UART Interrupt Pending	B-CH Interrupt Pending	0	0	INTID2	INTID1	INTID0

The IIR register provides prioritized information as to the status of interrupt conditions listed in the description of the Channel B Interrupt Enable Register.

Bits 0:2 Interrupt ID bits

These three bits of the IIR are used to identify the highest priority interrupt pending as indicated in the following table.

D2	D1	D0	PRIORITY	TYPE	SOURCE	RESET
0	0	0	Highest	TX FIFO Timeout	No characters have been read from or written to the TX FIFO in a character time and the TX FIFO is not empty.	Reading the TX FIFO Output Register
0	0	1	Second	TX FIFO Overrun Error		Reading the linr Status Register
0	1	0	Third	TX FIFO Full		Reading the TX FIFO Output Register
1	0	0	Fourth	TX FIFO Data Avaliable		Empty the TX FIFO
1	0	0	Fifth	RX FIFO Empty	RX FIFO empty	Write to RX FIFO input register or read interrupt ID Register (if source of interrupt)
1	0	1	Sixth	RX FIFO Ready	RX FIFO below trigger level or is not full	Fill RX FIFO input trigger level or fill the RX FIFO
1	1	0	Seventh	MCR/SCR Written	Host PC writes to MCR or SCR	Read IIR (if source of interrupt)
1	1	1	Eight	Divisor/LCR Written	Host PC write to DLL, DLM or LCR	Read IR (if source of interrupt)

INTERRUPT ID REGISTER (IIR) ADDRESS 0B3 (continued)

Bits 3:4 Reserved

Bit 5 Channel B Interrupt Pending

When asserted, this bit indicates one of the above interrupts is pending.

Bit 6 UART Interrupt Pending

When asserted, this bit indicates that an interrupt is pending from the core processor's UART. This bit will be held to a 0 if the enable external interrupt, bit 6 of the IER, is a zero.

Bit 7 FIFOs enabled

This bit indicates that the TX FIFO is enabled.

CHARACTER PACING REGISTER (CPR) ADDRESS 0B9
Reset State 00h

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
0	0	ALT2	ALT	RX Pace Count Overflow	TX Pace Count Overflow	RX Pace Enable	TX Pace Enable

When character pacing is enabled, interrupts to the microcontroller that are related to characters being transmitted and received are synchronized to a clock in which the period can be set to be the length of one character time. This time is determined by the number of bits per character specified in the Line Control Register (Channel A side) and the frequency of the bit clock. The frequency of the bit clock is the frequency of the overflow of the chosen timer (Timer0, Timer1, or Timer2) divided by 16. The timer source is selected by register bits MSR(D3) and MSR(D2). The auto reload value of the chosen timer can be set based upon the contents of the Divisor Latch Registers so that accurate character times can be achieved. The timers would be set up just as if they were used as the UART baud rate clock (overflow rate = 16x bit rate). Transmit and receive character pacing can be enabled independently through bits CPR(D1-D0) and the timer overflow status can be monitored in CPR(D3-D2).

Bit 0 TX Pace Enable

This bit enables character pacing in the transmit direction (with respect to the PC). The TX character pacing counter begins counting when the TX FIFO is not empty. The counter overflow causes a TX FIFO data available interrupt if the TX FIFO is not empty at the time of the counter overflow. The overflow condition is reset when the TX FIFO output register is read. TX FIFO full interrupts are also paced by the character pacing counter. The TX FIFO not empty status starts the timer. If the TX FIFO is filled before the counter overflows, the TX FIFO full status is prevented from causing an interrupt until the counter overflow occurs.

Bit 1 RX Pace Enable

This bit enables character pacing in the receive direction. The RX character pacing counter is reset by a write to the RX FIFO if the ALT bit is a 0 or free runs and gives an indication every character period if the ALT bit is set to a 1. If RX data available mode is selected (IERB-D7), the RX data available interrupt is masked until an RX character pacing counter overflow occurs. If RX data available mode is not selected, the RX data available interrupt is set following the overflow only if the RX FIFO is below the specified trigger level. RX FIFO empty interrupts are also masked until the RX character pacing counter overflows. These interrupts are reset when the RX FIFO is written.

Bit 2 TX Pace Clock Overflow

This bit is set when the transmit character pacing counter overflows. The TX character pacing timer begins counting as soon as the TX FIFO is not empty. This bit is reset when the TX FIFO is read or a master reset occurs.

Bit 3 RX Pace Clock Overflow

This bit is set when the receive character pacing counter overflows. The RX character pacing timer begins counting as soon as the RX FIFO is written if ALT is a zero or free runs causing the overflow to be exactly 1 character period. This bit is reset when the RX FIFO is written or a master reset occurs.

Bit 4 ALT Mode

This bit allows the receive character pacing counter overflow to occur at a fixed 1 character period interval. If this bit is a zero, the pacing timer is reset until the RX FIFO is written. This gives an indication 1 character time after the RX FIFO is written. If the ALT bit is a one, the pacing timer free runs and its overflow occurs at the character period and is independent of when the RX FIFO was written. If the latency to service the RX available interrupt exceeds 1 bit time, the ALT mode bit should be set to prevent poor throughput in non FIFO modes.

Bit 5 ALT2 Mode

This bit allows the TX FIFO to look like it has a transmit holding register and a TX Serial Shift Register if the 550 is not in a FIFO mode. If this bit is set, a THRE indication is given to the host if the are fewer than 2 bytes in the TX FIFO. The THRE indication will go low after an empty TX FIFO is written. It will remain low for 1 to 2 bit periods as dictated by the pacing timer. This imitates the behavior of a traditional 550 where it takes 1 to 2 bit times to load the Holding Register contents into the TX Shift Register.

If the ALT2 bit is 0, the THRE and TX FIFO empty indications will be identical. This limits the host processor since the THRE interrupt must be serviced within 1 bit time to prevent a diminished throughput in a non FIFO 550 mode. It can be beneficial for the microcontroller firmware to empty the TX FIFO during the RX available interrupt to prevent an abnormal behavior when the host polls for THRE.

LINE CONTROL REGISTER (LCR) ADDRESS 0B4 READ ONLY
Reset State 00h

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
DLAB	SBRK	STP	EPS	PEN	STB	WLS1	WLS0

This register reflects the value of the Line Control Register from the Channel A register set.

MODEM CONTROL REGISTER (MCR) ADDRESS 0B5
Reset State 00h

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
MCR Status Change	RCVR Trigger 1	RCVR Trigger 0	LOOP	Enable Interrupt	uPRST	RTS	DTR

This register is a copy of Channel A register bits with the exception of bit 7.

MODEM CONTROL REGISTER (MCR) ADDRESS 0B5 (continued)

Bit 0 Data Terminal Ready (DTR)

This bit is a copy of the host (Channel A) register bit MCR-D0.

Bit 1 Request to Send (RTS)

This bit is a copy of the host (Channel A) register bit MCR-D1.

Bit 2 µPRST

This bit is a copy of the host (Channel A) register bit MCR-D2.

Bit 3 Enable Interrupt

This bit is a copy of the host (Channel A) register bit MCR-D3.

Bit 4 Loop

This bit is a copy of the host (Channel A) register bit MCR-D4.

Bit 5 RCVR Trigger 0

This bit is a copy of the host (Channel A) register bit FCR-D6.

Bit 6 RCVR Trigger 1

This bit is a copy of the host (Channel A) register bit FCR-D7.

Bit 7 MCR Status Change

This bit is set when the Modem Control Register of the Channel A register set is written. It is cleared when the Modem Control Register of Channel B is read.

LINE STATUS REGISTER (LSR) ADDRESS 0B0
Reset State 60h

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
RCV FIFO Full	RCV FIFO Ready	RCV FIFO Empty	(BI)	(FE)	(PE)	(OE)	TX FIFO Not Empty

Bits 0,5,6,and 7 of this register provides status information to the core microcontroller concerning the data transfer to the host. Bits 1-4 of this register may be used to convey line status information to the host for emulation purposes.

Bit 0 Transmit FIFO Not Empty

This bit is set to logic 1 when valid data is available to the core processor in the transmit FIFO. This bit may be used in polled mode to indicate when valid data is available.

Bit 1 Overrun Error Indicator

This bit is set to logic 1 when a transmit FIFO overrun has occurred. This bit is cleared upon reading the Line Status Register.

Bit 2 Parity Error

A parity error indication is written into the receive FIFO if this bit is set to a 1 when the microcontroller writes data into the receive FIFO.

Bit 3 Framing Error

A framing error indication is written into the receive FIFO if this bit is set to a 1 when the microcontroller writes data into the receive FIFO.

Bit 4 Break Interrupt Indicator

A break Interrupt indication is written into the receive FIFO if this bit is set to a 1 when the microcontroller writes data into the receive FIFO.

Bit 5 Receive FIFO Empty (Read Only)

This bit is set to logic 1 when receive FIFO is empty.

Bit 6 Receive FIFO Ready (Read Only)

This bit is set to logic 1 when the receive FIFO is not filled to the trigger level programmed by the host in the Channel A FCR bits (D7 and D6).

Bit 7 Receive FIFO Full

This bit is set to logic 1 when the receive FIFO is full.

MODEM STATUS REGISTER (MSR) ADDRESS 0B6
Reset State 00h

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
DCD	RI	DSR	CTS	TCS2	TCS1	MRXTO	0

Bit 0 Not Used

Bit 1 Manual Receive FIFO Timeout (MRXTO)

This bit enables a receive FIFO timeout under program control if no timer is selected. If no reads or writes of the receive FIFO occur within four writes of a logic 1 to this bit, and the receive FIFO is not empty, a receive FIFO timeout is indicated to the host PC.

MODEM STATUS REGISTER (MSR) ADDRESS 0B6 (continued)

Bits 3:2 Bit Clock Source

These bit determines the clock source for FIFO timeout events and character pacing as shown in the following table. The clock source is provided by either Timer0, Timer1 or Timer2, of the core microcontroller overflow outputs. The clock rates are generated assuming the timer overflow frequency is set to the bit rate as indicated in the divisor latch values set in the DLL and DLM Registers.

The timeout clock source is used for loopback, receive FIFO timeout, transmit FIFO timeout, and character pacing. In loopback mode, the transmit data written by the host PC is automatically written to the receive FIFO in one character period, where one character period is N clock periods of the selected timer, where N is the number of bits per character as defined by the LCR. The receive FIFO timeout period is set to be 4 character periods of the selected timer. The transmit FIFO timeout is set to be one character period.

In the state where no timeout source is selected (bit 3 = 1, bit 2 = 1), loading of the transmit FIFO in loopback mode is done in firmware by writing to the receive FIFO (transmit FIFO data is automatically looped to the receive FIFO), no transmit FIFO timeout interrupt is provided, and the receive FIFO timeout must be provided by a firmware. The receive time out is set if no reads or writes of the FIFO occurred between four consecutive writes of a one to bit 1 of this register, and the receive FIFO is not empty.

BIT 3	BIT 2	TIMER SOURCE
0	0	Manual Mode
0	1	Timer0
1	0	Timer1
1	1	Timer2

Bit 4 Clear to Send (CTS)

This bit causes the CTS bit to be set in the Channel A Modem Status Register (MSR-D4).

Bit 5 Data Set Ready (DSR)

This bit causes the DSR bit to be set in the Channel A Modem Status Register (MSR-D5).

Bit 6 Ring Indicator (RI)

This bit causes the RI bit to be set in the Channel A Modem Status Register (MSR-D6)

Bit 7 Data Carrier Detect (DCD)

This bit causes the DCD bit to be set in the Channel A Modem Status Register (MSR-D7).

SCRATCH REGISTER (SCR) ADDRESS 0B7
Reset State 00h

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
DAT7	DAT6	DAT5	DAT4	DAT3	DAT2	DAT1	DAT0

This 8-bit read/write register is a general purpose register for communicating with the host processor (Channel A). The handshake controls must be implemented by the software programmer.

DIVISOR LATCH (DLL) ADDRESS 0BA
Reset State 00h

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
DAT7	DAT6	DAT5	DAT4	DAT3	DAT2	DAT1	DAT0

This register contains the least significant byte of the divisor from the Channel A DLL Register.

DIVISOR LATCH (DLM) ADDRESS 0BB
Reset State 00h

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
DAT7	DAT6	DAT5	DAT4	DAT3	DAT2	DAT1	DAT0

This register contains the most significant byte of the divisor from the Channel A DLM Register.

INTERRUPTS
The core chip provides 8 sources of interrupt; 3 external interrupts, 3 timer interrupts, a serial port interrupt, and an HDLC interrupt. An external interrupt and an HDLC interrupt are unique to the 73M2918. They do not exist in a normal 8032 product. Previously unused bits in the IE and IP Registers are now serving functions for these additional interrupt sources. The interrupt vector addresses are as follows:

SOURCE	VECTOR ADDRESS
INT0 (IE0)	003H
TF0	00BH
INT1 (IE1)	013H
TF1	01BH
RI + TI+ 500REG	023H
TF2 + EXF2	02BH
INT2 - Added Interrupt	033H
HDLC - Added Interrupt	03BH

The external interrupt sources, INT(2:0), come from dedicated input pins. The apparent polarity of these pins is individually controlled by bits in a special interrupt direction register, IDIR (address A9). The interrupt pins INT1 and INT0 can be either edge or level generated interrupts as indicated by bits 0 and 2 in the TCON Register (address 88h). Pin INT2 is always an edge generated interrupt. A flag is set when a falling transition (rising if IDIR bit 2 is set) on this pin is detected. This flag is automatically cleared when the interrupt is processed.

INTERRUPT ENABLE REGISTER (IE) SFR ADDRESS A8
Bit Addressable
Reset State 00h

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
EA	EX2	ET2	ES	ET1	EX1	ET0	EX0

NOTE: Bit 6 differs from the 8032. In the 8032 this is a reserved bit. In the SSI 73M2918/2918A it is used as a mask bit for external interrupt 2. When bit 6 is set to a 0, external interrupt 2 is disabled.

The mask bit for the HDLC interrupt source is bit 0 of the HDLC Control Register.

INTERRUPT ENABLE REGISTER (IE) SFR ADDRESS A8 (continued)

INTERRUPT PRIORITY REGISTER (IP) SFR ADDRESS B8
Bit Addressable
Reset State 00h

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
PHDLC	PX2	PT2	PS	PT1	PX1	PT0	PX0

NOTE: Bit 6 and bit 7 differ from the 8032. In the 8032 these are reserved bits. In the SSI 73M2918/2918A they are used to determine the priority of external interrupt 2 and the HDLC. When bit 6 is set to a 1, the interrupt is set to the higher priority level.

EXTERNAL INTERRUPT DIRECTION REGISTER (IDIR) SFR ADDRESS 92
Byte Addressable
Reset State 00h

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
0	0	INT2	INT1	INT0	INTD2	INTD1	INTD0

The contents of this register determine the polarity of the corresponding external signals Int 2:0 which will result in an interrupt. It also reflects the logic level at Int 2:0 and thus allows the user to directly read their logic level via register.

Bits 5:3 Int 2:0

Bits 5:3 are read only bits that reflect the logic value at the corresponding pin. The value is not affected by bits 2:0.

Bits 2:0 Interrupt Polarity Control

If the bit is set to a 0, a falling edge will trigger the interrupt. If the bit is set to a 1, a rising edge will trigger the interrupt. Also, if the bit is set to a 1, level generated interrupts will occur when the corresponding pin is high and the internal pin signal to the timer controls will be inverted.

Bits 6 and 7 will always be read as 0's.

CLOCK CONTROL REGISTER SFR ADDRESS DA
Byte Addressable
Reset State 00h

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Activity	CLK1 CTRL1	MCLK CTRL	CLK2 EN	CLK2 CTRL1	CLK2 CTRL0	CLK1 EN	CLK1 CTRL

These bits determine the behavior at the CLK1OUT and CLK2OUT pins and allow the user to divide the main internal processor clock frequency by two for power conservation.

Bit 7 Activity Bit

Bit 7 is set when an unmasked interrupt, a reset, or programmed COMSEL port activity is detected. When this bit is set the core microcontroller is prevented from entering the power-down mode. It is cleared by a read of this register.

Bit 6 Clock 1 Control Bit 1

If bit 1 of this register is set to logic 1, this bit, along with bit 0, determine the frequency of the CLK1OUT signal. If bit 6 = 1, and bit 0 = 0, the CLK1OUT frequency will be the oscillator frequency divided by 1.5. If this bit is a logic 1 and bit 0 = 1, the CLK1OUT signal will be disabled. If bit 6 = 0, the CLK1OUT frequency depends upon the logic level of bit 0.

Bit 5 Master Clock Control

When bit 5 is set to a 1 the internal processor clock is the oscillator frequency divided by 2. If this bit is a 0, the processor clock is the same frequency as the oscillator's.

BIT 5	CLOCK OUT
0	OSC
1	OSC/2

Bit 4 Clock 2 Output Enable

Bit 4 enables the clock at the CLOCK 2 output pin if it is set to a 1. The clock pin output can be held to a 0, without halting the oscillator, by writing this bit to a 0. This will reduce system power if the clock pin is not used or if a power reduction mode is required.

Bit 3:2 Clock 2 Output Control

These bits determine the oscillator divisor for the CLOCK 2 output pin. They were designed to provide a 1.8432 MHz clock for an external UART given an oscillator frequency of 11.0592 MHz, 22.1184 MHz, 18.432 MHz, or 13.824 MHz.

BIT 3	BIT 2	CLK 2 OUT	OSC FREQUENCY
0	0	OSC/7.5	13.824 MHz
0	1	OSC/6	11.059 MHz
1	0	OSC/12	22.118 MHz
1	1	OSC/10	18.432 MHz

Bit 1 Clock 1 Output Enable

Bit 1 enables the clock at the clock output pin if it is set to a 1. The clock pin output can be held to a 0, without halting the oscillator, by writing a logic 0 to this bit. This will reduce system power if the clock pin is not used or if a power reduction mode is required.

Bit 0 Clock 1 Output Control

Bit 0 controls the frequency of the clock 1 output pin. If bit 6 = 0 and bit 1 = 1, the clock output is either the oscillator's output signal divided by two or a buffered oscillator output signal. All of the CLK1OUT options are shown in the following chart:

BIT 6	BIT 1	BIT 0	CLK1OUT
x	0	x	0
0	1	0	OSC
0	1	1	OSC/2
1	1	0	OSC/1.5
1	1	1	0

REGISTER DESCRIPTION (continued)

POWER SAVING MODES

Low Power Modes

The SSI 73M2918/2918A supports two power conservation modes, which are controlled by the PCON.1 and PCON.0 control bits of the PCON Register.

If PCON.0 is set, the SSI 73M2918/2918A will go into a power saving mode where the oscillator is running, clocks are supplied to the UART, timers, HDLC, and interrupt blocks, but no clocks are supplied to the CPU. Instruction processing and activity on the address and data ports is halted. Normal operation is resumed when an unmasked interrupt is requested or when a reset occurs.

If PCON.1 is set, the SSI 73M2918/2918A goes into its lowest power mode where the oscillator is halted. The total current consumption in this state should be less than 10 µa. The SSI 73M2918/2918A will start its oscillator and begin to return to normal operation when either a reset occurs, when a falling (rising if corresponding direction bit is set) edge of an unmasked external interrupt from pins INT(2:0) is detected, or when the USR5(1:0) pins change to a state without the oscillator running. Edges used in wakeup modes are not filtered in the SSI 73M2918/2918A so the user must be cautious of noise or small glitches inadvertently waking up the chip. The time interval between the wake up event and execution of the first instruction depends upon the oscillator start-up time. Three good oscillator pulses must be detected before the main internal clocks are generated.

During power-down mode, both the ALE and PSEN pins are pulled high since these signals often provide the output enable and chip enable for the ROM (active low). This ensures that the external components are in their lowest power state.

USR PROGRAMMABLE I/O

Port Control USR1, USR2, USR3, USR4, COMSEL

The core chip provides 32 user I/O pins. Each pin is programmed separately as either an input or as an output by a bit in a direction register. If the bit in the direction register is set to a logic 1, the I/O control will treat the corresponding pin as an input. If it is a logic 0, the pin will be treated as an output whose value is determined by the port data register. The USR1 and USR2 port registers are accessed through the internal SFR bus. The USR3 and USR4 ports are accessed through the external memory bus by a MOVX instruction. The USR4 port provides the user with an automatic chip select function if selected by the user. If the user does not require some (or any) of the chip select pin options, he may program the USR4 port pins to operate in the same way as USR3 port pins.

The USRX data register contents are asserted at the USR port pins if the port is configured as an output. When reading from the data register's SFR address, the pin logic values are returned as data except when the port address is the destination address for a read-modify-write instruction. In this case, the latched register values are returned as data. When reading data from a data register that is mapped in the external memory space, the pin values are always returned as data. The COMSEL register allows for 2 additional input pins. In normal operation these pins can be used as general purpose inputs. The user can program the register so that either rising or falling transitions or logical combinations of the COMSEL pins will wake up the chip in power-down mode.

USR1 PORT

USR1 DATA SFR ADDRESS 90
Bit Addressable
Reset State 00h

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
USR1.7	USR1.6	USR1.5	USR1.4	USR1.3	USR1.2	USR1.1	USR1.0

Bits in this register will be asserted on the USR1(7:0) pins if the corresponding direction register bit is a 0. Reading this SFR's address will return data reflecting the values of pins USR1(7:0) except when address 90h is the destination address for a read-modify-write instruction. In this case, the latched register values are returned as data. USR1 port signals are also used as timer controls. In applications where the external signals are required for timer count modes, the corresponding port pin should be configured as an input.

USR1 bit 0 = TIMER0 T0 PIN

USR1 bit 1 = TIMER1 T1 PIN

USR1 bit 2 = TIMER2 T2 EX PIN

USR1 bit 3 = TIMER2 T2 PIN

USR1 PORT DIRECTION (DIR1) SFR ADDRESS 91
Byte Addressable
Reset State FFh

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
DIR1.7	DIR1.6	DIR1.5	DIR1.4	DIR1.3	DIR1.2	DIR1.1	DIR1.0

This register is used to designate the USR1 pins as either inputs or outputs. If the register bit is reset to a 0, the corresponding USR1 pin is programmed as an output that will be driven by the corresponding USR1 data register bit. If the register bit is a 1, the corresponding pin will be treated as an input.

After a reset, the USR1 pins will present a high impedance output state and the input values will not be driven from the pin, but will be driven to a 0 internally. The pins will assume normal I/O operation once the processor has written the Port Direction Register. This feature will ensure the chip is in a low current state at reset (the situations where the chip drives out against external inputs, or where floating inputs are applied to internal circuitry are thus prevented).

USR2 PORT

USR2 PORT DATA SFR ADDRESS D8
Bit Addressable
Reset State 00h

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
USR2.7	USR2.6	USR2.5	USR2.4	USR2.3	USR2.2	USR2.1	USR2.0

Bits in this register will be asserted on the USR2(7:0) pins if the corresponding direction register bit is a 0. Reading this SFR's address will return data reflecting the values of pins USR2(7:0) except when address D8h is the destination address for a read-modify-write instruction. In this case, the latched register values are returned as data.

USR2 PORT (continued)

USR2 PORT DIRECTION (DIR2) SFR ADDRESS D9
Byte Addressable
Reset State FFh

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
DIR2.7	DIR2.6	DIR2.5	DIR2.4	DIR2.3	DIR2.2	DIR2.1	DIR2.0

This register is used to designate the USR2 pins as either inputs or outputs. If the register bit is reset ito a 0, the corresponding USR2 pin is programmed as an output that will be driven by the corresponding USR2 I/O data register bit. If the register bit is a 1, the corresponding pin will treated as an input.

After a reset, the USR2 pins will present a high impedance output state and the input values will not be driven from the pin, but will be driven to a 0 internally. The pins will assume normal I/O operation once the processor has written the Port Direction Register. This feature will ensure the core chip is in a low current state at reset (the situations where the chip drives out against external inputs, or where floating inputs are applied to internal circuitry are thus prevented).

USR3 PORT

USR3 PORT DATA EXTERNAL ADDRESS 0000
Byte Addressable
Reset State 00h

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
USR3.7	USR3.6	USR3.5	USR3.4	USR3.3	USR3.2	USR3.1	USR3.0

Bits in this register will be asserted on the USR3(7:0) pins if the corresponding direction register bit is a 0. Reading this SFR's address will return data reflecting the values of pins USR3(7:0). if the bank select feature is chosen, USR3.7 acts as address bit 17 and USR3 data bit 7 is ignored.

USR3 I/O PORT DIRECTION (DIR3) EXTERNAL ADDRESS 0001
Byte Addressable
Reset State FFh

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
DIR3.7	DIR3.6	DIR3.5	DIR3.4	DIR3.3	DIR3.2	DIR3.1	DIR3.0

This register is used to designate the USR3 pins as either inputs or outputs. If the register bit is reset to a 0, the corresponding USR3 pin is programmed as an output that will be driven by the corresponding USR3 data register bit. If the register bit is a 1, the corresponding pin will be treated as an input.

After a reset, the USR3 pins will be inputs to support the ISA bus address for the 550 register set. If the bank select feature is chosen, USR3 pin 7 is forced to be an output.

The USR3(6:0) are used for AD550(9:3) for the 550 interface.

BANK SELECT (BNKSEL) EXTERNAL ADDRESS 0002
Byte Addressable
Reset State 00h

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
B7	B6	B5	B4	B3	B2	B1	B0

This resister is used to accommodate systems where more than 64 kBytes (up to 128 kBytes) of program memory are required. USR3 pin 7 acts as an address pin, A16, if BSEN is set to a 1 and if the processor is fetching an instruction and not data memory. If BSEN is set to a 1, A15 is also modified during instruction fetches as shown. If BSEN is a 0, no alterations to address bit A15 are made, and USR3 pin 7 is a function of USR3 bit 7 and DIR3 bit 7.

Bits (7-3) are general purpose read/write register bits.

A15 is the value of the 16th address bit as it appears at pin A15.

A15' is the address from port 2 internal logic, the value that will appear as the most significant address bit if no bank select feature is chosen.

A16 is the value of the 17th and MSB of the instruction address seen at the USR3.7 port pin, if the bank select feature is selected. If the bank select feature is not selected, USR3.7 acts as a normal USR3 I/O port pin.

BSEN	BS1	BS0	A15	A15	A16	ADDRESS
0	*	*	0	0	USR3.7	0K - 32K
0	*	*	1	1	USR3.7	32K - 64K
1	0	0	0	0	0	0K - 32K
1	0	0	1	1	0	32K - 64K
1	0	1	0	0	0	0K - 32K
1	0	1	1	0	1	64K - 96K
1	1	0	0	0	0	0K - 32K
1	1	0	1	1	1	96K - 128K
1	1	1	0	0	0	0K - 32K
1	1	1	1	0	1	64K - 96K

* = Don’t care.

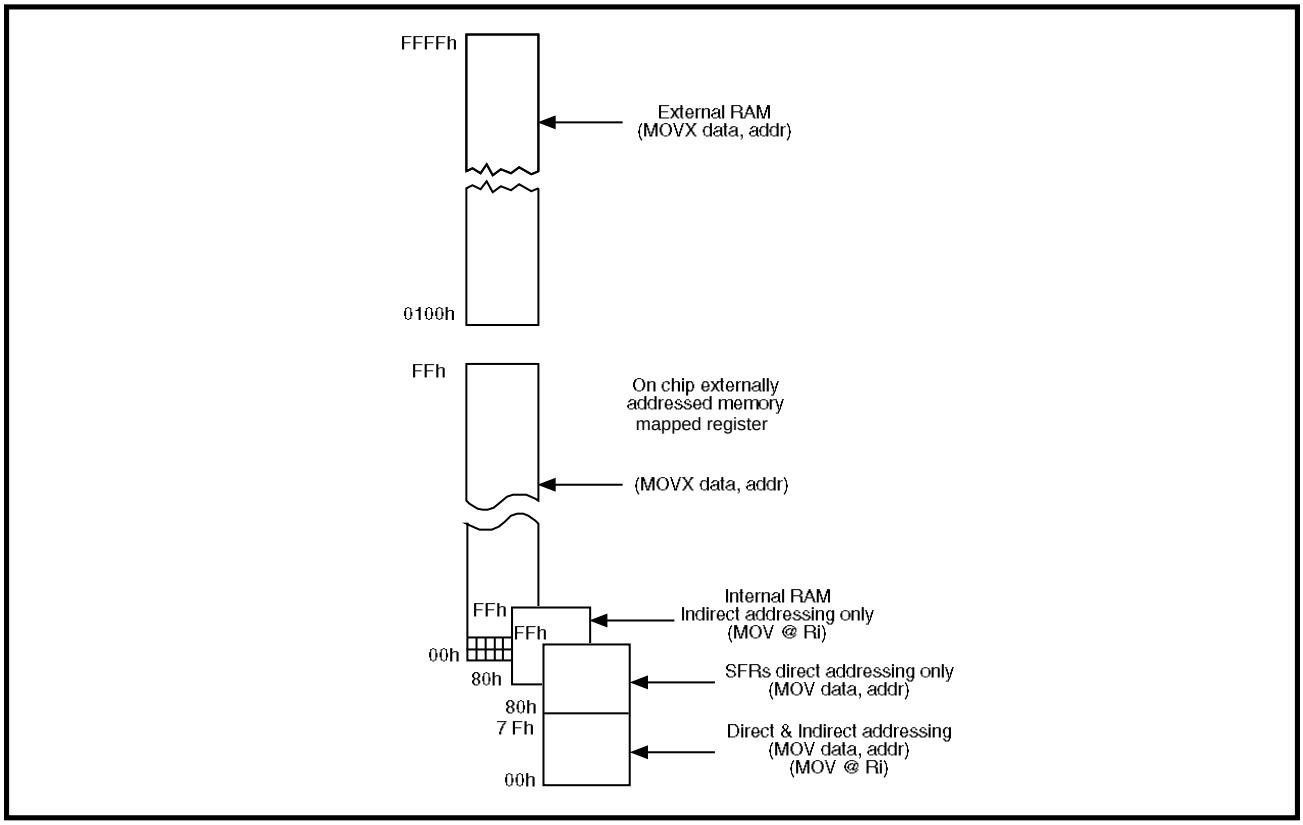


FIGURE 5: Memory Map

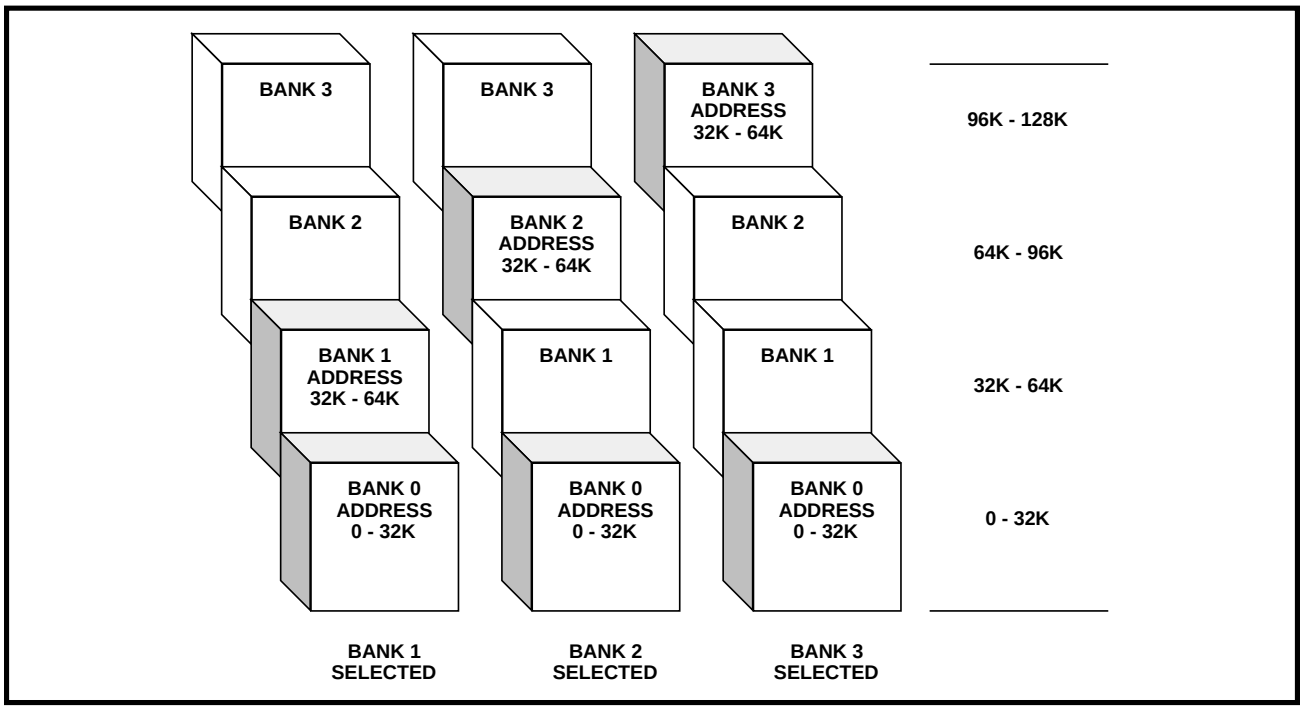


FIGURE 6: 128K of Bank-Selected Program Memory

USR PROGRAMMABLE I/O (continued)

USR4 PORT

USR4 PORT DATA EXTERNAL ADDRESS 0003
Byte Addressable
Reset State 00h

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
USR4.7	USR4.6	USR4.5	USR4.4	USR4.3	USR4.2	USR4.1	USR4.0

Bits in this register will be asserted on the USR4(7:0) pins if the corresponding direction register bit is a 0 and if the corresponding bit in the Chip Select Enable Register, 0005, is set to a 0. Reading this register will return data reflecting the values of pins USR4(7:0).

USR4 I/O PORT DIRECTION (DIR4) EXTERNAL ADDRESS 0004
Byte Addressable
Reset State FFh

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
DIR4.7	DIR4.6	DIR4.5	DIR4.4	DIR4.3	DIR4.2	DIR4.1	DIR4.0

This register is used to designate the USR4 pins as either inputs or outputs. If the register bit is reset to a 0, the corresponding USR4 pin is programmed as an output that will be driven by the corresponding USR4 I/O data register bit if the corresponding bit in the chip select enable register, 005, is set to a 0. If the register bit is a 1, the corresponding pin will treated as an input only if the corresponding bit in register 005 is set to a 0.

After a reset, the USR4 pins will act as chip select outputs.

USR4 PORT CHIP SELECT/INTERRUPT ENABLE (CSEN) EXTERNAL ADDRESS 0005
Byte Addressable
Reset State FFh

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
CSEN6	CSEN5	CSEN4	CSEN3	CSEN2	CSEN1	IRQDEN	IRQCEN

This register is used to designate the USR4 pins as either user programmable I/Os, as chip select ($\overline{CS1}$ - $\overline{CS6}$) pins, or as available interrupts (IRQC and IRQD) in PnP modes, on a pin by pin basis. This feature is designed to help reduce external glue logic for peripheral memory mapped devices. The chip select function is programmed by setting the appropriate bits in the CSEN Register. When a alternative function select pin is enabled by setting the corresponding EN bit to a 1, all data and direction information from registers 0003 and 0004 for this bit are ignored and the selected port becomes an output. If the bit is reset to a 0, the pin will be treated as a normal programmable user I/O pin as defined by registers 0003 and 0004.

The chip select pins have a defined memory map. The intent is that the outputs can be wire OR'ed together for a flexible selection of peripheral chip selects. All chip selects will be disabled (forced to a logic 1. It is assumed that all chip selects are active low) after the read or write is completed, and the appropriate chip select will be enabled as the next new external addresses is asserted. After a reset, the CSB pull-up devices are all enabled, that is, all chip select outputs are high. Users must account for this if these pins are intended to be general purpose I/Os.

The IRQC and IRQD outputs are either driven logic levels or high impedance as determined by the PnP logic if the corressponding IRQEN bit is set.

USR4 PORT CHIP SELECT/INTERRUPT ENABLE (CSEN) EXTERNAL ADDRESS 0005 (continued)

The chip selects partition a 64K memory space as follows:

CHIP SELECT PIN	ADDRESS	# BYTES
Reserved	0000H - 00FFH	256
CS1(USR4.2)	0100H - 07FFH	2K-256
CS2(USR4.3)	0800H - 0FFFH	2K
CS3(USR4.4)	1000H - 1FFFH	4K
CS4(USR4.5)	2000H - 3FFFH	8K
CS5(USR4.6)	4000H - 7FFFH	16K
CS6(USR4.7)	8000H - FFFFH	32K

NOTE: You can't read from external addresses 0000H - 00FFH. These are reserved for SSI 73M2918/2918A internally defined registers.

COMSEL PORT

COMSEL PORT REGISTER EXTERNAL ADDRESS 0006
Byte Addressable
Reset State 0XX0 0000b

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
USR	COMSEL1	COMSEL2	POL1	POL2	ACTE0	ACTE1	AND01

This register allows the firmware to read the COMSEL bits to determine base I/O addresses and interrupt level assignments for the 550 register set in non PnP modes. If the COMSEL pins are not required for a given application, these pins can be used as general purpose input pins with wakeup capability.

Bits 0-4 of the COMSEL Register can be programmed such that a transition at the COMSEL1 pin, a transition at the COMSEL2 pin, or the logical combination of COMSEL1 and COMSEL2 can wakeup the processor from its power-down mode.

Bit 7 USR

Bit 7 is used as a general purpose register bit.

Bit 6 COMSEL1

Bit 6 reflects the value of chip pin COMSEL1.

Bit 5 COMSEL1

Bit 5 reflects the value of chip pin COMSEL2.

Bit 4 Comsel1 Polarity

Bit 4 determines which edge or level is used in the wakeup detection circuit. A low level selects a rising transition and the true pin value of COMSEL1 to the wakeup combinatorial circuit. When this bit is set to a 1, a falling transition and complemented COMSEL1 value is presented to the wakeup combinatorial circuit.

Bit 3 Comsel2 Polarity

Bit 3 determines which edge or level is used in the wakeup detection circuit. A low level selects a rising transition and the true pin value of COMSEL2 to the wakeup combinatorial circuit. When this bit is set to a 1, a falling transition and complemented COMSEL2 value is presented to the wakeup combinatorial circuit.

Bit 2 Comsel1 Edge Activity Enabled

When bit 2 is set to a 1, a transition of COMSEL1 of the appropriate level as dictated by bit 4, will wake up the processor. If this bit is reset to a 0, edge activity on this pin is ignored.

Bit 1 Comsel2 Edge Activity Enabled

When bit 1 is set to a 1, a transition of COMSEL1 of the appropriate level as dictated by bit 3, will wake up the processor. If this bit is reset to a 0, edge activity on this pin is ignored.

Bit 0 Combinatorial and of Comsel1 and Comsel2 Level Enabled

When bit 0 is set to a 1, the value COMSEL1 or its complimented value as dictated by bit 3, AND'ed with the value COMSEL2 or its complimented value as dictated by bit 2, will wake up the processor. If this bit is reset to a 0, the levels of COMSEL1 and COMSEL2 are ignored.

COMSEL1	COMSEL2	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0	WAKEUP
*	*	*	*	0	0	0	no
0-1	*	0	*	1	*	*	yes
1-0	*	1	*	1	*	*	yes
*	0-1	*	0	*	1	*	yes
*	1-0	*	1	*	1	*	yes
0	0	1	1	*	*	1	yes
1	0	0	1	*	*	1	yes
0	1	1	0	*	*	1	yes
1	1	0	0	*	*	1	yes

* = Don't Care

REGISTER DESCRIPTION (continued)

HDLC REGISTERS

HDLC CONTROL REGISTER 0 (HDLC0) SFR ADDRESS C0
Bit Addressable Reset State 00XX 0000 b
Bits 5 and 4 are read only bits

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
WRXD	WPTXD	TXD	PRXD	RXD CTRL1	RXD CTRL0	PTX CTRL1	PTX CTRL0

This register controls the basic set-up of the DTE and modem pins RXD, TXD, PRXD, and PTXD.

Bit 7 WRXD

Bit 7 allows the processor to write directly to the SSI 73M2918/2918A RXD output pin. The value of bit 7 will appear at the RXD pin only if bit 3 is a 1 and bit 2 is a 1.

Bit 6 WPTXD

Bit 6 allows the processor to write directly to the SSI 73M2918/2918A PTXD output pin. The value of bit 6 will appear at the PTXD pin only if bit 1 is a 1 and bit 0 is a 0.

Bit 5 TXD

Bit 5 is a read only bit that reflects the value at the SSI 73M2918/2918A TXD input pin.

Bit 4 PRXD

Bit 4 is a read only bit that reflects the value at the SSI 73M2918/2918A PRXD input pin.

Bits 3:2 RXD Control

Bit 3 and bit 2 control the source of the RXD output pin. This output goes to the DTE's RS232 interface. The source of this signal can be the core's UART TXD output, the PRXD output from a modem peripheral (clear channel), the DTE's TXD(echo), or the value written into bit 7 of this register.

BIT 3	BIT 2	RXD OUTPUT
0	0	UART TXD output
0	1	PRXD buffered (clear channel)
1	0	TXD buffered (echo)
1	1	WRXD (bit 7)

Bit 1:0 PTXD Control

Bit 1 and bit 0 control the source of the PTXD output pin. This output goes to the modem's TX data input. The source of this signal can be the core's HDLC TX output, the DTE's TXD output (clear channel), the value written into bit 6 of this register, or the UART's output. Also, when bit[1:0] is 11, the UART's input is the value at the PRXD pin. This 11 state allows the UART to share the same I/O as the HDLC Packetizer.

BIT 1	BIT 0	PTXD OUTPUT
0	0	HDLC TXD output
0	1	TXD buffered (clear channel)
1	0	WPTXD (bit 6)
1	1	UART TX output UART RX input = PRXD

HDLC CONTROL REGISTER 1 (HDLC1) SFR ADDRESS C1
Byte Addressable
Reset State 00h

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
HDLC RST	CCITT	CRC PRE	RXCRC 32	RXCRC 16	TXCRC CTRL	ZERO ID	HDLC EN

This register controls the basic set-up of the HDLC block This register will be written during intialization and not during normal message processing.

Bit 7 HDLC Software Set

When bit 7 is a 1, the HDLC circuit is reset and held in a low power state and no interrupts from the HDLC circuitry will be generated. When a 0 is written to this bit, the HDLC circuit will behave according to its control bits. Bit 7 and the power-on-reset signal are OR'ed together to form a reset signal for the HDLC block.

Bit 7 is cleared to a 0 upon a power-up-reset.

Bit 6 CRC Type Control

Bit 6 selects the CRC algorithm used in the 16 bit CRC calculation. There are two types of 16-bit CRCs commonly used, CRC 16 and the CCITT 16-bit CRC. If this bit is set to a 1, the CCITT type is selected.

Bit 6 is cleared to a 0 upon a reset.

Bit 5 CRC Preset Value

Bit 5 selects the reset value for the CRC generator and receiver. If this bit is set to a 1, the CRC generator and receiver are initialized to 1s and if this bit is reset to a 0, they are initialized to 0s. This bit should be set to a 1 for most CCITT polynomials.

Bit 5 is cleared to a 0 upon a reset.

Bits 4:3 RX CRC Control

Bit 4 and bit 3 determine the type of CRC remainder that will be checked at the end of a received frame. The HDLC block can support both 16-bit CRC and 32-bit CRC. If both bit 4 and bit 3 are reset, bits 7 and 6 of the HDLC Status Register will be held to a logic 0. If both bit 4 and bit 3 are logic 1s, a special CRC search mode is enabled where both bits 7 and 6 of the HDLC Status Register are enabled. This mode is used during a connection to determine which CRC is used by the initiating modem. If the 16-bit CRC remainder is not matched at the end of the received frame, then bit 6 of the HDLC Status Register is set. If the 32-bit CRC remainder is not matched at the end of the received frame, then bit 7 of the HDLC Status Register is set. Once the correct CRC type is established during a connection, either bit 4 or bit 3 should be set to a 1 enabling the appropriate invalid CRC status bit.

HDLC CONTROL REGISTER 1 (HDLC1) SFR ADDRESS C1 (continued)

BIT 4	BIT 3	CRC TYPE
0	0	No CRC Check
0	1	Enable CRDC 16 Status
1	0	Enable CRC 32 Status
1	1	Enable CRC 16 Status and CRC 32 Status

Bit 2 TX CRC Control

Bit 2 controls the type of CRC to be transmitted. If bit 2 is reset to a logic 0, a 16-bit CRC will be transmitted with the send CRC command. If bit 2 is set to a logic 1, a 32-bit CRC will be transmitted.

Bit 1 Zero Insert/Delete Control

When bit 1 is set to a 1, a 0 will be transmitted if either the SEND DATA or SEND CRC bits of the HDLC TX control are set after five consecutive 1s have been transmitted. Also, when this bit is set, a 0 will be removed from the received data stream if it immediately follows a pattern of a 0 followed by five consecutive 1s. If bit 1 is reset to a 0, no 0s will be inserted during transmission, and no 0s will be deleted during reception.

Bit 1 is cleared to a 0 upon a reset.

Bit 0 HDLC Interrupt Enable

When bit 0 is reset to a 0, the HDLC will be prevented from generating an interrupt. The status bits that indicate the source of the interrupt can still be set allowing the HDLC block to be serviced in a polled mode.

Bit 0 is cleared to a 0 upon reset.

HDLC TX CONTROL REGISTER (HTXC) SFR ADDRESS C2
Byte Addressable
Reset State 00h

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
0	0	0	DIV16 CLK	SEND ABORT	SEND CRC	SEND DATA	SEND FLAG

This register is used to control the source of data that appears on the PTXD pin. A bit is shifted out on each rising edge of the PTXCLK pin input. If no control bits are set, or more than 1 TX control bit is set, the PTXD pin will go to a logic 1.

Bit 7:5 Always 0

Bit 4 16X Clock Select

Under normal synchronous operation, the PTXCLK and PRXCLK are used to receive and transmit data PRXD and PTXD. The clock rate is equal to the data rate. In asynchronous modes, a clock 16 times the bit rate is provided at PTXCLK and PRXCLK.

When bit 4 is set to a 1 for asynchronous operation, the clocks at the PTXCLK and PRXCLK pins are divided by 16 to provide transmit and receive shift clocks. An internal clock for sampling incoming PRXD data is synchronized by detecting any falling edge on the PRXD data pin. The rising edge of this internal clock, which used to sample incoming data, is delayed from the falling data edge by 8 PRXCLK periods and will continue at this phase and at a PRXCLK/16 frequency until another falling PRXD edge is detected.

If bit 4 is reset to a 0, the rising edge of PTXCLK is used to sample the data at PRXD, and the falling edge of PTXCLK is used to shift new data onto PTXD.

Bit 3 is cleared to a 1 upon a reset.

Bit 3 Abort

When bit 3 is set to a 1, a series of consecutive 1s will immediately be transmitted through the PTXD pin on every falling edge of PTXCLK. The message will have been aborted after 2 TX ready interrupts are received. No 0s will be inserted during the abort transmission.

Bit 3 is cleared to a 1 upon a reset.

Bit 2 Send CRC

When bit 2 is set, the bytes in the TX CRC generator will be inverted and serially transmitted to the PTXD output on the falling edge on PTXCLK as soon as the present data byte transmission is completed. If bit 1 of the HDLC Control Register is a 0, a 0 will be inserted into the CRC data stream after five consecutive 1s are transmitted. As soon as the last bit of the CRC is sent, a series of flags will be automatically sent until another TX control bit is set. No TX ready interrupts will be generated during the transmission of the CRC bytes. A TX ready interrupt will be generated as the first bit of each flag byte is transmitted indicating that the CRC transmission has been completed. This should be cleared by a dummy write to the TX Data Register.

Bit 2 will be cleared to a 0 upon a reset.

Bit 1 Send Data

When bit 1 is set, the data in the TX Data Register will be serially transmitted through the PTXD pin on each falling edge of PTXCLK, LSB first. If bit 1 of the HDLC Control Register is a 0, a 0 will be inserted into the data stream after five consecutive 1s are transmitted. After all eight data register bits have been sent, the HDLC will continue to send data by loading the parallel serial transmit register with new transmit register data, unless either a TX underrun is detected or one of the other TX control bits has been set. This bit will be cleared by the HDLC circuitry as soon as a TX underrun is detected. A TXRDY interrupt will be generated at as the first data of each data byte is transmitted.

Bit 1 will be cleared to a 0 upon a reset.

Bit 0 Send Flag

When bit 0 is set, a pattern of 7E will be transmitted to the PTXD output as soon as either the next data byte or CRC has completed transmission. No 0s will be inserted during the flag transmission. When bit 0 is reset back to a 0, the HDLC circuitry will complete the flag byte in progress and then transmit according to bits in the TX Control Register. TX ready interrupts will be generated as each byte of flag transmission is initiated.

Bit 0 will be cleared to a 0 upon a reset.

HDLC REGISTERS (continued)

HDLC STATUS REGISTER (HSTAT) SFR ADDRESS C3
Byte Addressable
Reset State 00h
Read Only Register

If any of the HDLC status bits are set, bit 1 of the HDLC Interrupt Register (NEW STATUS) will be set if the corresponding bit in the HDLC Interrupt Enable Register is set.

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
CRC32	CRC16	TX UNDRN	RX OVRN	INVAL FLAG	ABORT DET	IDLE DET	FLAG DET

Bit 7 Invalid CRC 32

Bit 7 will be set if the CRC search mode or the 32-bit CRC is enabled by the HDLC Control Register and an incorrect remainder for the 32-bit CRC is detected at the last received byte prior to receiving a flag.

Bit 7 will by cleared upon a reset and is cleared by a read of the HDLC Stat Register.

Bit 6 Invalid CRC 16

Bit 6 will be set if the CRC search mode or the 16-bit CRC is enabled by the HDLC Control Register and an incorrect remainder for the 16-bit CRC is detected at the last received byte prior to receiving a flag.

Bit 6 will by cleared upon a reset and is cleared by a read of the HDLC Stat Register.

Bit 5 TX Underrun

When bit 5 is set, a transmit underrun condition has been detected. This condition occurs when the HDLC has finished transmitting a message byte, but no new data has been loaded into the TX Data Register, and no other transmit control bit has been set. This bit will be set only if the send data bit, bit 1 of the TX Control Register is set. The transmit data is double buffered since the TX Data Register is downloaded into a TX Serial Register when the HDLC begins to transmit a new data byte. At the time of loading the TX Serial Register, a TX ready interrupt is generated.This interrupt must be serviced by either loading a new data byte (the next data byte to be transmitted) into the TX Data Register, or by setting another TX control bit, before the current data byte has completed transmission (at which point another TX ready interrupt would be generated). If a TX underrun is detected, the HDLC will abort the current transmission by sending continuous 1s and will reset the send data control bit in the TX Control Register.

Bit 5 will by cleared upon a reset and is cleared by a read of the HDLC Stat Register.

Bit 4 RX Overrun

When bit 4 is set, a receive overrun condition has been detected. This condition occurs when the HDLC has received a new byte, but the last received data byte has not yet been read from the RX Data Register. As soon as a new data byte has been received in an 8-bit serial register, it is loaded into the RX Data Registerand a new RX data interrupt is generated. If this interrupt is not serviced by reading the RX Data Register during the time another new data byte is received, the RX overrun status bit will be set. The new received data will not overwrite the older unread data.

Bit 4 will by cleared upon a reset and is cleared by a read of the HDLC Stat Register.

Bit 3 Invalid Flag

When bit 3 is set, an invalid flag has been detected. This condition occurs when a 7E pattern with no inserted 0s is detected, and this pattern did not originate on a byte boundary. Note, two consecutive flags may share a 0, so that the second (or subsequent) flag may not appear to be on a byte boundary. This condition does not result in an invalid flag indication. Instead, the bit counter is reset to 0.

Bit 3 will by cleared upon a reset and is cleared by a read of the HDLC Stat Register.

Bit 2 Abort Detect

When bit 2 is set, an abort condition has been detected. This condition occurs when seven consecutive 1s, with no inserted 0s, are received after an active state. Bit 2 will be cleared upon a reset and is cleared by a read of the HDLC Stat Register.

Bit 1 Idle Detect

When bit 1 is set, the first indication of an idle state is detected. An idle state is declared when 15 consecutive 1s, with no inserted 0s, are received after an active state.

Bit 1 will be cleared upon a reset and is cleared by a read of the HDLC Stat Register.

Bit 0 Flag Detect

When bit 0 is set, the HDLC has received a 7E pattern with no inserted 0's. Bit 0 will by cleared upon a reset and is cleared by a read of the HDLC Stat Register.

HDLC INTERRUPT ENABLE REGISTER (HIE) SFR ADDRESS C4
Byte Addressable
Reset State 00h

If the bit is set, the corresponding interrupt source is enabled.

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
TX RDY IE	RX RDY IE	TX RDY EN	RX RDY EN	INVAL FLG IE	ABORT IE	IDLE IE	FLAG IE

Bit 7 Transmitter Ready Interrupt Enable

When bit 7 is set, an HDLC interrupt will be generated if bit 0 (TX RDY) of the HDLC Interrupt Register is also set. If bit 7 is reset to a 0, no HDLC interrupt indication will be given as TX RDY is set.This interrupt enable allows the TX RDY to be a polled bit. Note that bit 5 of this register is a pre-mask to the TX RDY bit, that is, it will prevent the TX RDY bit from ever being set.

Bit 7 will be cleared upon a reset.

Bit 6 Receiver Ready Interrupt Enable

When bit 6 is set, an HDLC interrupt will be generated if bit 1 (RXRDY) of the HDLC Interrupt Register is also set. If bit 6 is reset to a 0, no HDLC interrupt indication will be given as RX RDY is set.This interrupt enable allows the RX RDY to be a polled bit. Note that bit 4 of this register is a pre-mask to the RX RDY bit, that is, it will prevent the RX RDY bit from ever being set.

Bit 6 will be cleared upon a reset.

HDLC INTERRUPT ENABLE REGISTER (HIE) SFR ADDRESS C4 (continued)

Bit 5 Transmit Ready Enable

Bit 5 is used to enable the TX RDY and TX underrun interrupt sources. When bit 5 is set, the transmitter ready indication will set bit 0 of the HDLC Interrupt Register. The TX RDY indication will go active as the first bit of a message byte is being transmitted, except during CRC transmission. Also, if this bit is set, the TX underrun condition will result in a new status interrupt. If bit 5 is reset to a 0, bit 0 of the HDLC Interrupt Register will not be set, and no corresponding HDLC interrupt will be generated. Also, a TX underrun condition, as indicated by bit 5 of the HDLC Status Register, will not result in an HDLC interrupt or in setting the new status interrupt bit.

Bit 5 will be cleared upon a reset.

Bit 4 Receiver Ready Enable

Bit 4 is used to enable the RX RDY and RX overrun interrupt sources. When bit 4 is set, the receiver ready indication will set bit 1 of the HDLC Interrupt Register. The RX RDY indication will go active when a data byte (a byte that is not a flag, idle, or an abort pattern) is loaded into the RX Data Register. Also, if this bit is set, the RX overrun condition will result in a new status interrupt. If bit 4 is reset to a 0, bit 1 of the HDLC Interrupt Register will not be set, and no corresponding HDLC interrupt will be generated. Also, a RX overrun condition, as indicated by bit 4 of the HDLC Status Register, will not result in a HDLC interrupt or in setting the new status interrupt bit.

Bit 4 will be cleared upon a reset.

Bit 3 Invalid Flag Interrupt Enable

When bit 3 is set, a HDLC interrupt will be generated if bit 3 (INVALID FLAG) of the HDLC Status Register is also set. If bit 3 is reset to a 0, bit 2 (NEW STATUS) of the HDLC Interrupt Register will not be set as a result of an invalid flag boundary detection and no HDLC interrupt will be generated.

Bit 3 will be cleared upon a reset.

Bit 2 Abort Dectect Interrupt Enable

When bit 2 is set, a HDLC interrupt will be generated if bit 2 (ABORT DETECT) of the HDLC Status Register is also set. If bit 2 is reset to a 0, bit 2 (NEW STATUS) of the HDLC Interrupt Register will not be set as a result of an abort pattern detection and no HDLC interrupt will be generated.

Bit 2 will be cleared upon a reset.

Bit 1 Idle Detect Interrupt Enable

When bit 1 is set, an HDLC interrupt will be generated if bit 1 (IDLE DETECT) of the HDLC Status Register is also set. If bit 1 is reset to a 0, bit 2 (NEW STATUS) of the HDLC Interrupt Register will not be set as a result of an idle pattern detection and no HDLC interrupt will be generated.

Bit 1 will be cleared upon a reset.

Bit 0 Flag Detect Interrupt Enable

When bit 0 is set, a HDLC interrupt will be generated if bit 0 (FLAG DETECT) of the HDLC Status Register is also set. If bit 0 is reset to a 0, bit 2 (NEW STATUS) of the HDLC Interrupt Register will not be set as a result of a flag pattern detection and no HDLC interrupt will be generated.

Bit 0 will be cleared upon a reset.

HDLC INTERRUPT REGISTER (HINT) SFR ADDRESS C5
Byte Addressable
Read Only Register
Reset State 00h

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
0	0	0	0	0	NEW STATUS	DATA RDY	TX RDY

This register is used to determine the source of HDLC interrupts. If one or more of these register bits are set, the HDLC interrupt will go active if bit 0 of the HDLC Control Register is set to a 1.

Bit 2 New Status

When bit 2 is set, an unmasked HDLC status bit from the HDLC Status Register is set.

Bit 2 will by cleared upon a reset and is cleared by a read of the HDLC Status Register.

Bit 1 Data Ready

When bit 1 is set, a new received byte has been loaded into the RX Data Register. Note, received bits that are flag, abort, or idle patterns are not considered data, and will not be loaded into the RX Data Register. All inserted 0s are removed from this byte. The RX Data Register must be read prior to the completed reception of the next data byte.

Bit 1 will by cleared upon a reset and is cleared by a read of the RX Data Register.

Bit 0 TX Ready

Bit 0 is set if any TX control bit is set as the first bit of data, flag or an idle byte is being transmitted. While transmitting the current byte, the HDLC state machines are ready for commands pertaining to the next byte to be transmitted. A new data byte must be loaded into the TX Data Register to clear the TX ready status bit.

Bit 0 will by cleared upon a reset and is cleared by writing to the TX Data Register.

RX DATA REGISTER (RXD) SFR ADDRESS C6
Byte Addressable
Reset State XXh
Read Only Register

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
RX DAT7	RX DAT6	RX DAT5	RX DAT4	RX DAT3	RX DAT2	RX DAT1	RX DAT0

RX DATA REGISTER (RXD) SFR ADDRESS C6 (continued)

Bit 7:0 Received Data Byte

Bit 7 through bit 0 is the received data byte (LSB is received first) with all inserted 0s removed. A data ready interrupt will be generated when a new data byte is received. Reading this register will clear the data ready interrupt.

TX DATA REGISTER (TXD) SFR ADDRESS C7
Byte Addressable
Reset State XXh
Write Only Register

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT	BIT 0
TX DAT7	TX DAT6	TX DAT5	TX DAT4	TX DAT3	TX DAT2	TX DAT1	TX DAT0

Bit 7:0 Transmit Data Byte

Bit 7 through bit 0 will be transmitted at the next byte boundary (LSB first) if the TX control send data bit is set. The HDLC will insert all necessary 0s. A TX ready interrupt will be generated when a new data byte can be loaded into the TX Data register. Writing this register will clear the TX ready interrupt.

CRC GENERATIONS

CCITT Type
The CRC check field is generated by the transmitter. The computation starts with the first transmitted bit after the opening flag and stops at the last data bit prior to the frame check sequence bytes, and excludes inserted 0s. The CRC generating logic is initialized to all ones. The bits are operated upon by the generating polynomial, X16 + X12 + X5 + 1. During CRC transmission, the bytes in the CRC generating logic are inverted and transmitted, high order bit first.

The receiver also initializes its CRC computation logic to all ones after the beginning flag. Its polynomial generator (also X16 + X12 + X5 + 1) should see the same value as the transmitter's polynomial generator as the last data bit is received. Note the receiver's polynomial generator does not process inserted 0s. After the bytes are received in the frame check sequence, a remainder of 1111 0000 1011 1000 (X0 through X15, respectively) should be detected in the receiver's polynomial generator. If this is not the case, it is assumed that the preceding frame was in error and an invalid CRC is declared.

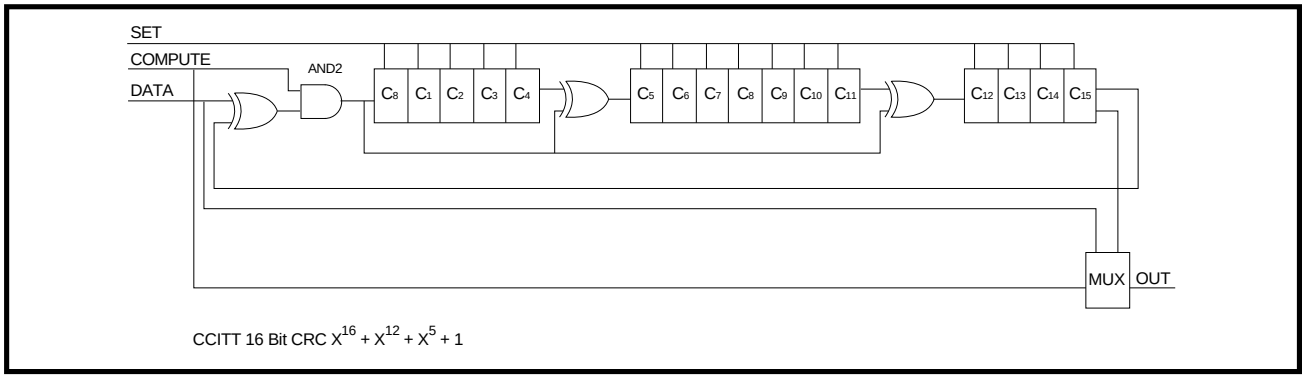


FIGURE 7: CCITT Type

CRC 16

The CRC check field is generated by the transmitter. The computation starts with the first transmitted bit after the opening flag and stops at the last data bit prior to the frame check sequence bytes, and excludes inserted 0s. The CRC generating logic is initialized to all zeros. The bits are operated upon by the generating polynomial, X16 + X15 + X2 + 1. During CRC transmission, the bytes in the CRC generating logic are transmitted, high order bit first.

The receiver also initializes its CRC computation logic to all zeros after the beginning flag. Its polynomial generator (also X16 + X15 + X2 + 1) should see the same value as the transmitter's polynomial generator as the last data bit is received. Note the receiver's polynomial generator does not process inserted 0s. After the bytes are received in the frame check sequence, a remainder of 0000 0000 0000 0000 should be detected in the receiver's polynomial generator. If this is not the case, it is assumed that the preceding frame was in error and an invalid CRC is declared.

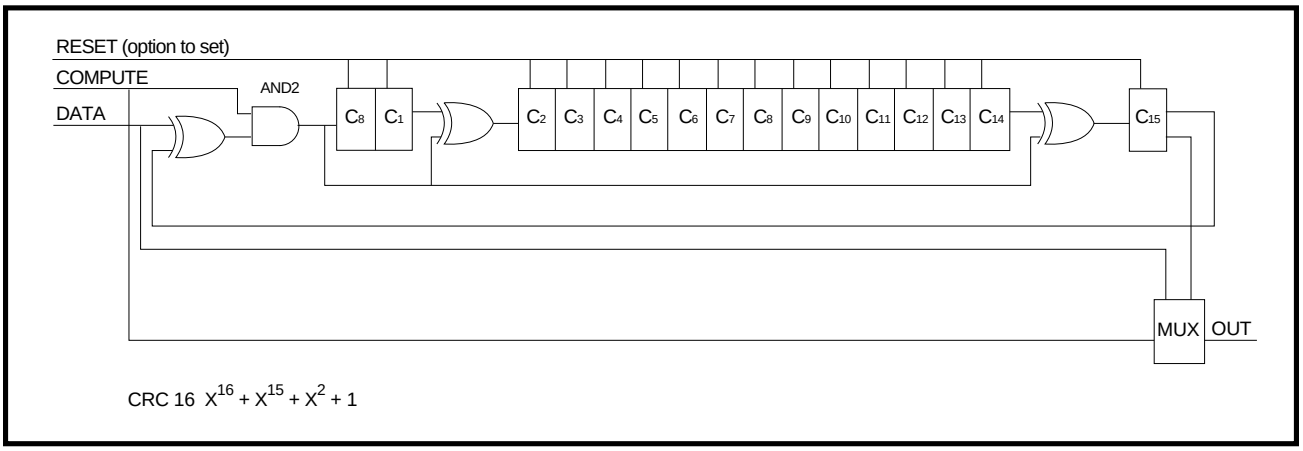


FIGURE 8: CRC 16

CRC GENERATIONS (continued)

CRC 32

The CRC check field is generated by the transmitter. The computation starts with the first transmitted bit after the opening flag and stops at the last data bit prior to the frame check sequence bytes, and excludes inserted 0s. The CRC generating logic is initialized to all ones. The bits are operated upon by the generating polynomial, X32 + X26 + X23 + X22 + X16 + X12 + X11 + X10 + X8 + X7 + X5 + X4 + X2 + X + 1. During CRC transmission, the bytes in the CRC generating logic are inverted and transmitted, high order bit first.

The receiver also initializes its CRC computation logic to all ones after the beginning flag. Its polynomial generator should see the same value as the transmitter's polynomial generator as the last data bit is received. Note the receiver's polynomial generator does not process inserted 0s. After the bytes are received in the frame check sequence, a remainder of 1101 1110 1011 1011 0010 0000 1110 0011 (X0 through X32, respectively) should be detected in the receiver's polynomial generator. If this is not the case, it is assumed that the preceding frame was in error and an invalid CRC is declared.

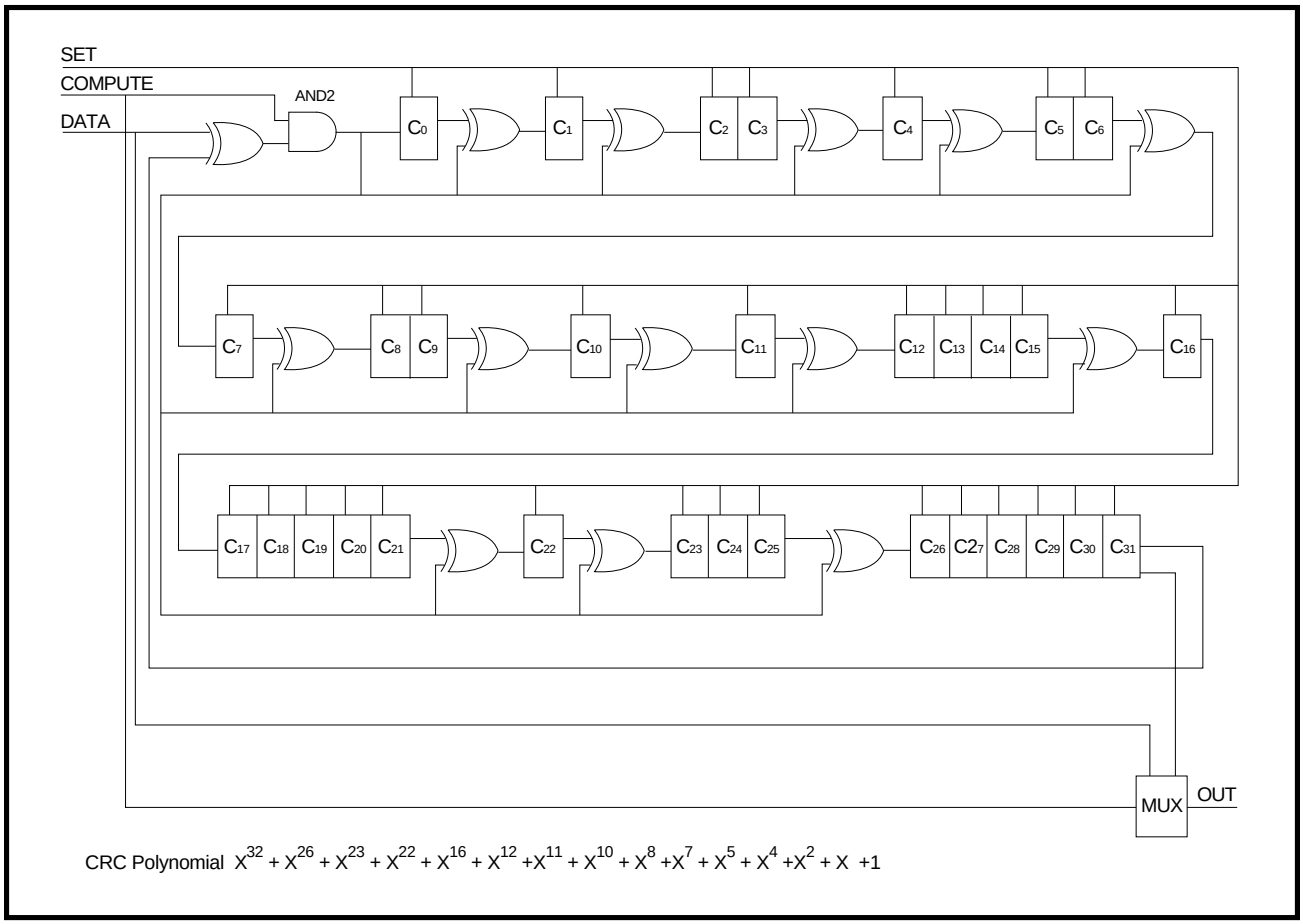


FIGURE 9: 32-Bit CRC

MEMORY MAPPED REGISTERS

	Address locations 0008-00FF are reserved for future use								
08									0F
00	USER3	DIR3	BNKSEL	USER4	DIR4	CSEN	COMSEL		07

SSI 73M2918/2918A SFR MAP

F8									FF
F0	B								F7
E8									EF
E0	ACC								E7
D8	*USR2	*DIR2	*CLKCTRL						DF
D0	PSW								D7
C8	T2CON		RCAP2L	RCAP2H	TL2	TH2			CF
C0	*HDLC0	*HDLC1	*TXC	*HSTAT	*HIE	*HINT	*HRXD	*HTXD	C7
B8	IP	*CPR	*DLL	*DLM	*PNPSTAT	*PNPDR	*PNPILS	*PNPIC	BF
B0	*LSR	*T/R FIFO	*IER	*IIR	*LCR	*MCR	*MSA	*SCR	B7
A8	IE				*PNPIOBA				AF
A0	P2								A7
98	SCON	SBUF							9F
90	*USR1	*DIR1	*IDIR						97
88	TCON	TMOD	TL0	TL1	TH0	TH1			8F
80	P0	SP	DPL	DPH				PCON	87

* Unique to the SSI 73M2918. There may not be an equivalent function on an 8032.

PIN DESCRIPTION

NAME	TYPE	DESCRIPTION
VND	GND	Negative digital voltage. (Digital Ground)
VPD	I	Positive digital voltage (+Digital Supply)
MR	I	Master reset. When this pin is a logic 1 the 550 registers and the microprocessor are reset.
OSCIN	I	Crystal input for internal oscillator, also input for external source.
OSCOUT	O	Crystal oscillator output.
$\overline{\text{PSEN}}$	O	Program store enable. This output goes low occurs during a fetch from external program memory. (Active low)
$\overline{\text{RD}}$	O	Output strobe activated during a bus read. Can be used to enable data onto the bus from an external memory mapped device. (Active low)
$\overline{\text{WR}}$	O	Output strobe during a bus write. Used as a write strobe to external memory mapped devices. (Active low)
ALE	O	Address Latch Enable output pulse for latching the low byte of the address during accesses to external memory.
AD0-AD7	I/O	Multiplexed address/data bus I/O lines for external memory mapped and program memory devices.
A0-A15	O	Latched address bus for devices that require separate data and address bus.
$\overline{\text{INT0}}$-$\overline{\text{INT2}}$	I	External interrupt 0,1 and 2.
CLKOUT1	O	Clock output programmable either OSC/2, OSC/1 or logic 0.
CLKOUT2	O	Clock output 1.8432 MHz clock for an external UART given an oscillator frequency of 11.0592 MHz, 22.1184 MHz, 18.432 MHz, or 13.824 MHz.
TXD	I	Serial input port to SSI 73M2918/2918A microcontroller from DTE. Same as RXD UART input.
RXD	O	Serial output port of SSI 73M2918/2918A microcontroller UART to DTE. Same as TXD UART output.
PTXCLK	I	Input clock used to transmit data PTXD.
PTXD	O	HDLC Packetizer's TX output. This pin can also be programmed to be the DTE's TXD output (clear channel) or the value written into bit 6 of the HDLC Control Register.
PRXCLK	I	Input clock used to receive data PRXD.
PRXD	I	Serial input port (from modem device).
USR1.0 - USR1.7	I/O	USR programmable I/O port.

NAME	TYPE	DESCRIPTION
USR2.0 - USR2.7	I/O	USR programmable I/O port.
USR3.7	I/O	If the bank select feature is chosen, USR3(7) acts as address bit 17 and the USR3 data bit 7 is ignored.
USR4.0 - USR4.1	I/O	USR programmable I/O port. These pins can also be used as programmable interrupt outputs to the host from the 550 register set where USR4.0 is IRQC and USR4.1 is IRQD.
USR4.2 - USR4.7	I/O	USR programmable I/O port. These pins can also be used as programmable chip select outputs for peripheral memory mapped devices.

HOST 550 INTERFACE

COMSEL(2:1)	I	These ports are used as COMSEL(2:1) of the 550 interface. These lines are used when the Plug and Play hardware is disabled. These pins are also general purpose input pins that can be read through the COMSEL memory mapped register.
ALE550	I	An input that gates the address inputs as valid.
AD550(11:10)	I	Address inputs used for addressing Plug and Play Read_Data, Write_Data, and Address Ports.
AD550(9:3)	I	Address inputs for internal generation of chip select for the 550 register set.
AD550(2:0)	I	Address lines from the PC bus. These bits address the individual 550 registers.
DB550(7:0)	I/O	550 Data bus. This bus comprises 8 Input/Output pins for communication between the SSI 73M2918/2918A 550 register set and the host PC.
$\overline{IOR}$	I	If the PC Bus interface chip select is active, $\overline{IOR}$ initiates a read of the 550 Data Bus when low.
$\overline{IOW}$	I	If the PC bus interface chip select is active, $\overline{IOW}$ initiates a write of the 550 Data Bus when low.
IRQA	O	This output is the first of four interrupt lines that can be internally connected to the 550 UART interrupt. This output generates an interrupt to a host PC from an unmasked interrupt source in the 550 register set. This pin can be a driven logic level or high impedance as indicated by a host write to the modem control register's enable interrupt bit. When the Plug and Play hardware is disabled, the 550 UART interrupt is internally connected to this pin. When the Plug and Play hardware is enabled, this pin is enabled from the Interrupt Line Select SFR Register.
$\overline{IRQ}$	O	This output is the second of four interrupt lines that can be internally connected to the 550 UART interrupt. This pin can only be utilized when Plug and Play hardware is enabled and its enable bit is set in the Interrupt Line Select SFR Register. NOTE: IRQC and IRQD are shared functions with USR4.0 and USR4.1.

PIN DESCRIPTION (continued)

PIN ASSIGNMENT TABLE - SSI 73M2918/2918A QFP PACKAGE

PIN	NAME	PIN	NAME	PIN	NAME	PIN	NAME
1	DB550[0]	26	DB550[5]	51	AD550[0]	76	COMSEL2
2	DB550[1]	27	DB550[6]	52	AD550[1]	77	ALE550
3	DB550[2]	28	IRQB	53	AD550[2]	78	$\overline{\text{IOR}}$
4	DB550[3]	29	DB550[7]	54	AD550[10]	79	$\overline{\text{IOW}}$
5	DB550[4]	30	CLK2OUT	55	IRQA	80	COMSEL1
6	A1	31	VPD	56	USR2.7	81	AD550[5]
7	A2	32	CLK1OUT	57	USR2.6	82	AD550[6]
8	A3	33	TXD	58	USR2.5	83	AD550[7]
9	A4	34	RXD	59	USR2.4	84	AD550[8]
10	A5	35	PTXCLK	60	USR2.3	85	AD550[9]
11	A6	36	PTXD	61	USR2.2	86	USR3.7
12	A7	37	PRXCLK	62	USR2.1	87	VND
13	A8	38	PRXD	63	USR2.0	88	$\overline{\text{RD}}$
14	A9	39	$\overline{\text{INT2}}$	64	VPD	89	$\overline{\text{WR}}$
15	A10	40	$\overline{\text{INT1}}$	65	AD550[11]	90	ALE
16	A11	41	$\overline{\text{INT0}}$	66	USR4.7	91	D0
17	A12	42	VND	67	USR4.6	92	D1
18	A13	43	USR1.0	68	USR4.5	93	D2
19	A14	44	USR1.1	69	USR4.4	94	D3
20	A15	45	USR1.2	70	USR4.3	95	D4
21	$\overline{\text{PSEN}}$	46	USR1.3	71	USR4.2	96	D5
22	MR	47	USR1.4	72	USR4.1	97	D6
23	VND	48	USR1.5	73	USR4.0	98	D7
24	OSCOUT	49	USR1.6	74	AD550[3]	99	VPD
25	OSCIN	50	USR1.7	75	AD550[4]	100	A0

PIN ASSIGNMENT TABLE - SSI 73M2918/2918A TQFP PACKAGE

PIN	NAME	PIN	NAME	PIN	NAME	PIN	NAME
1	DB550[2]	26	DB550[7]	51	AD550[10]	76	IRQB
2	DB550[3]	27	CLK2OUT	52	IRQA	77	$\overline{IOW}$
3	DB550[4]	28	VPD	53	USR2.7	78	COMSEL1
4	A1	29	CLK1OUT	54	USR2.6	79	AD550[5]
5	A2	30	TXD	55	USR2.5	80	AD550[6]
6	A3	31	RXD	56	USR2.4	81	AD550[7]
7	A4	32	PTXCLK	57	USR2.3	82	AD550[8]
8	A5	33	PTXD	58	USR2.2	83	AD550[9]
9	A6	34	PRXCLK	59	USR2.1	84	USR3.7
10	A7	35	PRXD	60	USR2.0	85	VND
11	A8	36	$\overline{INT2}$	61	VPD	86	$\overline{RD}$
12	A9	37	$\overline{INT1}$	62	AD550[11]	87	$\overline{WR}$
13	A10	38	$\overline{INT0}$	63	USR4.7	88	$\overline{ALE}$
14	A11	39	VND	64	USR4.6	89	D0
15	A12	40	USR1.0	65	USR4.5	90	D1
16	A13	41	USR1.1	66	USR4.4	91	D2
17	A14	42	USR1.2	67	USR4.3	92	D3
18	A15	43	USR1.3	68	USR4.2	93	D4
19	$\overline{PSEN}$	44	USR1.4	69	USR4.1	94	D5
20	MR	45	USR1.5	70	USR4.0	95	D6
21	VND	46	USR1.6	71	AD550[3]	96	D7
22	OSCOUT	47	USR1.7	72	AD550[4]	97	VPD
23	OSCIN	48	AD550[0]	73	COMSEL2	98	A0
24	DB550[5]	49	AD550[1]	74	ALE550	99	DB550[0]
25	DB550[6]	50	AD550[2]	75	$\overline{IOR}$	100	DB550[1]

PIN DESCRIPTION (continued)

SSI 73M2918/2918A PGA

PIN	NAME	PIN	NAME	PIN	NAME	PIN	NAME
B2	AD550[10]	M2	IRQB	M12	DB550[2]	B12	DB550[7]
B1	IRQA	N2	$\overline{IOW}$	M13	DB550[3]	A12	CLK2OUT
C2	USR2.7	M3	COMSEL1	L12	DB550[4]	B11	VPD
C1	USR2.6	N3	AD550[5]	L13	A1	A11	CLK1OUT
D2	USR2.5	M4	AD550[6]	K12	A2	B10	TXD
D1	USR2.4	N4	AD550[7]	K13	A3	A10	RXD
E2	USR2.3	M5	AD550[8]	J12	A4	B9	PTXCLK
E1	USR2.2	N5	AD550[9]	J13	A5	A9	PTXD
F3	USR2.1	L6	USR3.7	H11	A6	C8	PRXCLK
F2	USR2.0	M6	GND	H12	A7	B8	PRXD
F1	VPD	N6	$\overline{RD}$	H13	A8	A8	$\overline{INT2}$
G2	AD550[11]	M7	$\overline{WR}$	G12	A9	B7	$\overline{INT1}$
G3	USR4.7	L7	ALE	G11	A10	C7	$\overline{INT0}$
G1	USR4.6	N7	D0	G13	A11	A7	GND
H1	USR4.5	N8	D1	F13	A12	A6	USR1.0
H2	USR4.4	M8	D2	F12	A13	B6	USR1.1
H3	USR4.3	L8	D3	F11	A14	C6	USR1.2
J1	USR4.2	N9	D4	E13	A15	A5	USR1.3
J2	USR4.1	M9	D5	E12	PSEN	B5	USR1.4
K1	USR4.0	N10	D6	D13	MR	A4	USR1.5
K2	AD550[3]	M10	D7	D12	GND	B4	USR1.6
L1	AD550[4]	N11	VPD	C13	OSCOUT	A3	USR1.7
M1	COMSEL2	N12	A0	B13	OSCIN	A2	AD550[0]
L2	ALE550	M11	DB550[0]	C12	DB55O[5]	B3	AD550[1]
N1	$\overline{IOR}$	N13	DB550[1]	A13	DB550[6]	A1	AD550[2]

ELECTRICAL SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Operation outside these rating limits may cause permanent damage to this device.

PARAMETER	RATING
Supply Voltage	-0.5V to +7.0V
Pin Input Voltage	-0.5V to Vcc + 0.5V
Storage Temperature	-55°C to 150°C

RECOMMENDED OPERATING CONDITIONS SSI 73M2918

Supply Voltage	4.5V to 5.5V
Oscillator Frequency	DC to 34 MHz
Operating Temperature	-40°C to +85°C

RECOMMENDED OPERATING CONDITIONS SSI 73M2918A

Supply Voltage	4.75V to +5.5V
Oscillator Frequency	DC to 44 MHz
Operating Temperature	-40°C to +50°C

DC CHARACTERISTICS

PARAMETER		CONDITION	MIN	NOM	MAX	UNIT
Input Low (Except OSCIN, RESET, PTXCLK, PRXCLK)	V_{IL}		-0.5		0.2 Vcc-0.1	V
Input Low Voltage OSCIN,RESET, PTXCLK, PRXCLK	V_{IL}		-0.5		0.2 Vcc	V
Input High Voltage (Except OSCIN, RESET, PTXCLK, PRXCLK)	V_{IH}		0.5 VCC		Vcc + 0.5	V
Input High Voltage OSCIN, RESET, PTXCLK, PRXCLK	V_{IH}		0.7 Vcc		Vcc + 0.5	V
Output Low Voltage (Except OSCOUT)	V_{OL}	IOL = 3.2 mA			0.45	V
Output Low Voltage OSCOUT	V_{OLOSC}	IOL = 3.0 mA			0.7	V
Output High Voltage (Except OSCOUT)	V_{OH}	IOH = 3.2 mA	Vcc - 0.45			V
Output High Voltage OSCOUT	V_{OHOSC}	IOH = 3.0 mA	Vcc - 0.7			V

DC CHARACTERISTICS (continued)

PARAMETER		CONDITION	MIN	NOM	MAX	UNIT
Input Leakage Current (Except OSCIN)	I_{IL}	Vss<Vin<Vcc			1	µA
Input Leakage Current OSCIN	I_{IL}	Vss<Vin<Vcc	1		20	µA
Maximum Power Supply Normal Operation	$I_{DD}1$	22 MHz 30 pF/pin			40	mA
Maximum Power Supply Idle Mode	$I_{DD}2$	22 MHz			10	mA
Maximum Power Supply Power-Down Mode	$I_{DD}3$	@ 25°C			10	µA

AC TIMING

Oscillator Frequency	F_{OSC}		0		34 @ 4.5V	MHz
Oscillator Period	T_{OSC}	4.5V	30			ns
ALE Pulse Width	T_{LHLL}		2TOSC-10			ns
Address Valid to ALE Low	T_{AVLL}		TOSC			ns
Address Hold after ALE Low	T_{LLA}		TOSC-10			ns
ALE Low to PSEN Low	T_{LLPL}		TOSC-10			ns
PSEN Pulse Width Low	T_{PLPH}		3TOSC-20			ns
PSEN Low to Valid Inst In	T_{PLIV}				3TOSC-50	ns
Address to Valid Inst In	T_{AVIV}	2918			6TOSC-50	ns
		2918A			6TOSC-32	ns
Input Instr Hold-PSEN High	T_{PXIX}		0			ns
PSEN Instr Float-PSEN High	T_{PXIZ}				20*	ns
RD Pulse Width	T_{RLRH}		6TOSC-20			ns
WR Pulse Width	T_{WLWH}		6TOSC-20			ns
RD Low to Valid Data In	T_{RLDV}				5TOSC - 50	ns
Data Hold After RD	T_{RHDX}		0			ns
Data Float After RD	T_{RHDZ}				20*	ns
ALE Low to Valid Data In	T_{LLDV}				8TOSC - 50	ns
ALE Low to RD or WR Low	T_{LLWL}		3TOSC-20		3TOSC + 20	ns
Data Valid to WR Low	T_{QVWX}		TOSC			ns
Data Hold After WR High	T_{WHQZ}		TOSC-10			ns
RD Low to Address Float	T_{RLAZ}				10	ns
		Ext. program memory read cycle				
		Ext. WR cycle extension memory				
		Ext. RD cycle ext. memory				

* See AC Timing on next page

AC TIMING (continued)

The microcontroller portion of the timing is very similar to the 8032 except in AD(7:0), the multiplexed address data port known as port 0 in the 8032. Its timing has been altered somewhat to allow more address setup time for peripheral program ROM and memory mapped peripherals. This is important at higher operating frequencies. The 8032 has a “dead” cycle of one oscillator period between the time PSEN goes high, indicating that the instruction ROM will release the AD(7:0) bus, to the time the processor will assert address on the AD(7:0) bus. This dead time of one whole oscillator cycle has been shortened to approximately 20 ns after the PSEN (or RD) signal is sensed to be high.

The timing specification for TPXIZ and TRHDZ of a maximum of 20 ns can be violated at the expense of increased operating current. The will begin asserting the AD(7:0) bus approximately 20 ns after PSEN or RD go high. This should be ample time for the control signals in the peripheral device to turn off their pad drivers. If the peripheral device does not release the bus promptly, there will be a short time where there is contention on the AD(7:0) bus between the processor and peripheral. This should not prevent proper operation, but it will increase operating current slightly.

AC TIMING FOR 550 INTERFACE

PARAMETER		CONDITION	MIN	NOM	MAX	UNIT
ALE550 Valid to $\overline{IOR}$ Low	T_{ADVRL}		0			ns
ALE550 Valid to $\overline{IOW}$ Low	T_{ADVWL}		0			ns
AD550(11:0) Valid to $\overline{IOR}$ Low	T_{ADVRL}		0			ns
AD550(11:1) Valid to $\overline{IOW}$ Low	T_{ADVWL}		20			ns
AD550(11:0) Hold after $\overline{IOW}$ High	T_{ADHWH}		0			ns
DB550(7:0) Vlaid after $\overline{RD}$ Low	T_{DBVARL}				50	ns
DB550(7:0) Valid to $\overline{IOW}$ High	T_{DBVWH}		20			ns
DB550(7:0) Float after $\overline{IOR}$ High	T_{DBFRH}				30	ns
DB550(7:0) Hold after $\overline{IOW}$ High	T_{DBWH}		10			ns
$\overline{IOR}$ Pulse Width Low	T_{PWL}		20			ns
$\overline{IOW}$ Pulse Width Low	T_{PWWL}		20			ns

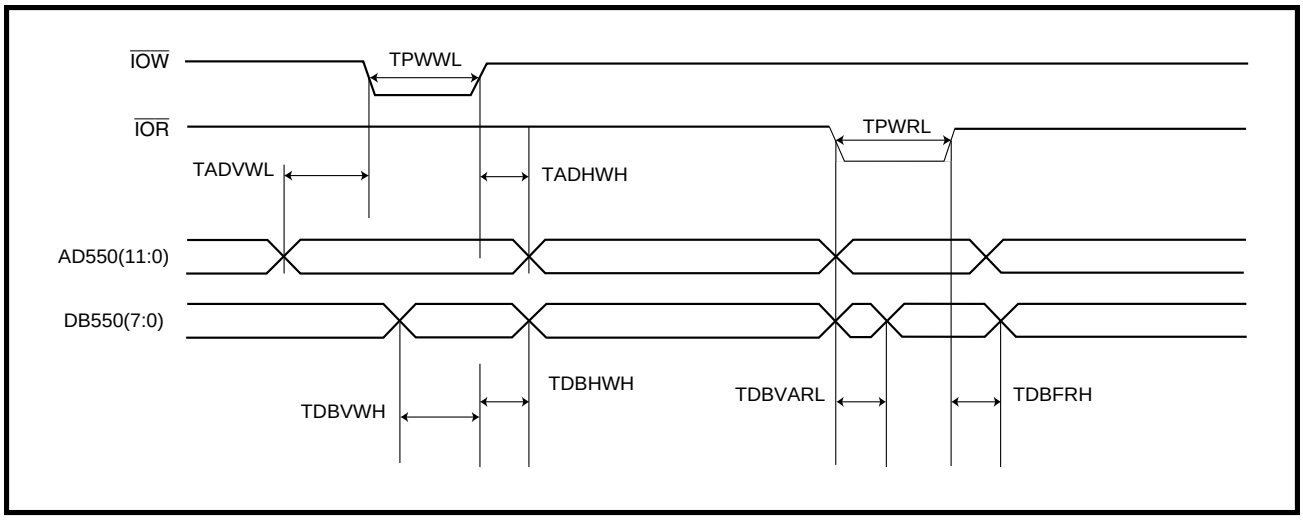


FIGURE 10: AC Timing For 550 Interface

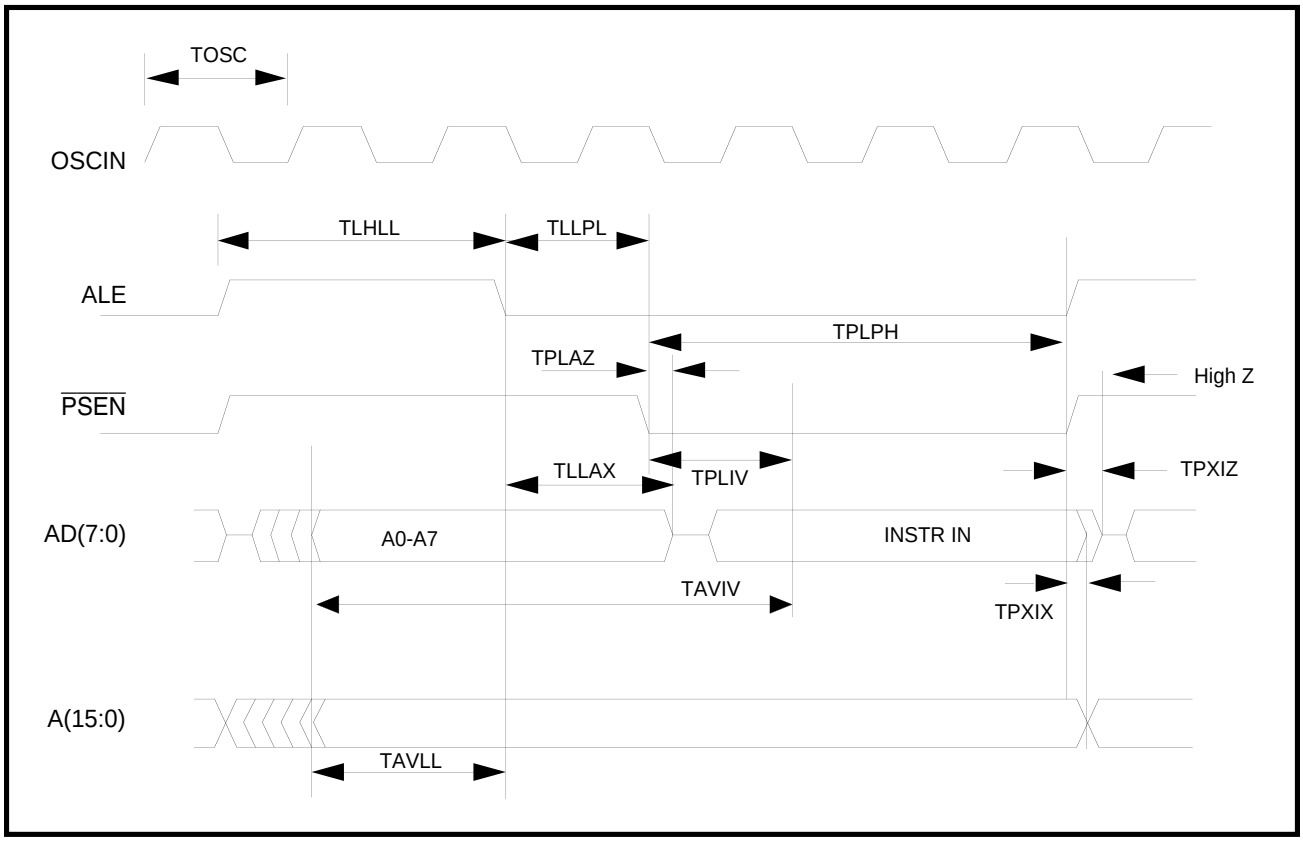


FIGURE 11: External Program Memory Read Cycle

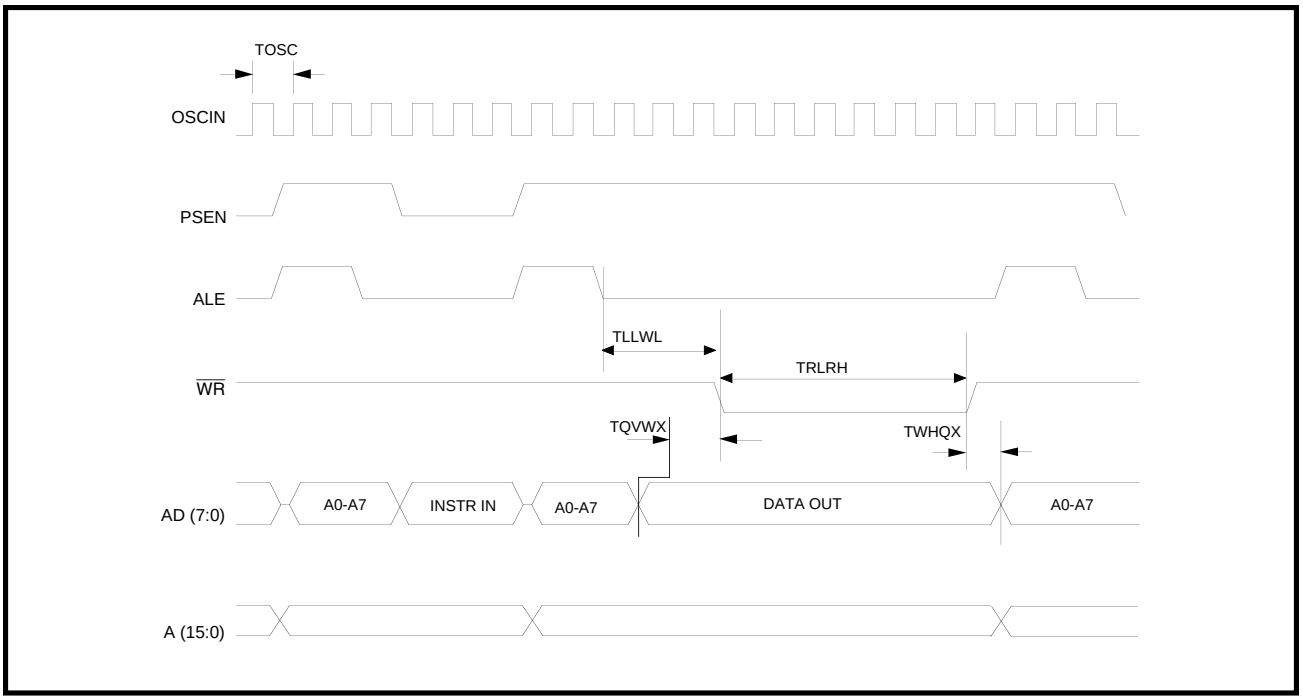


FIGURE 12: External Data Memory Write Cycle

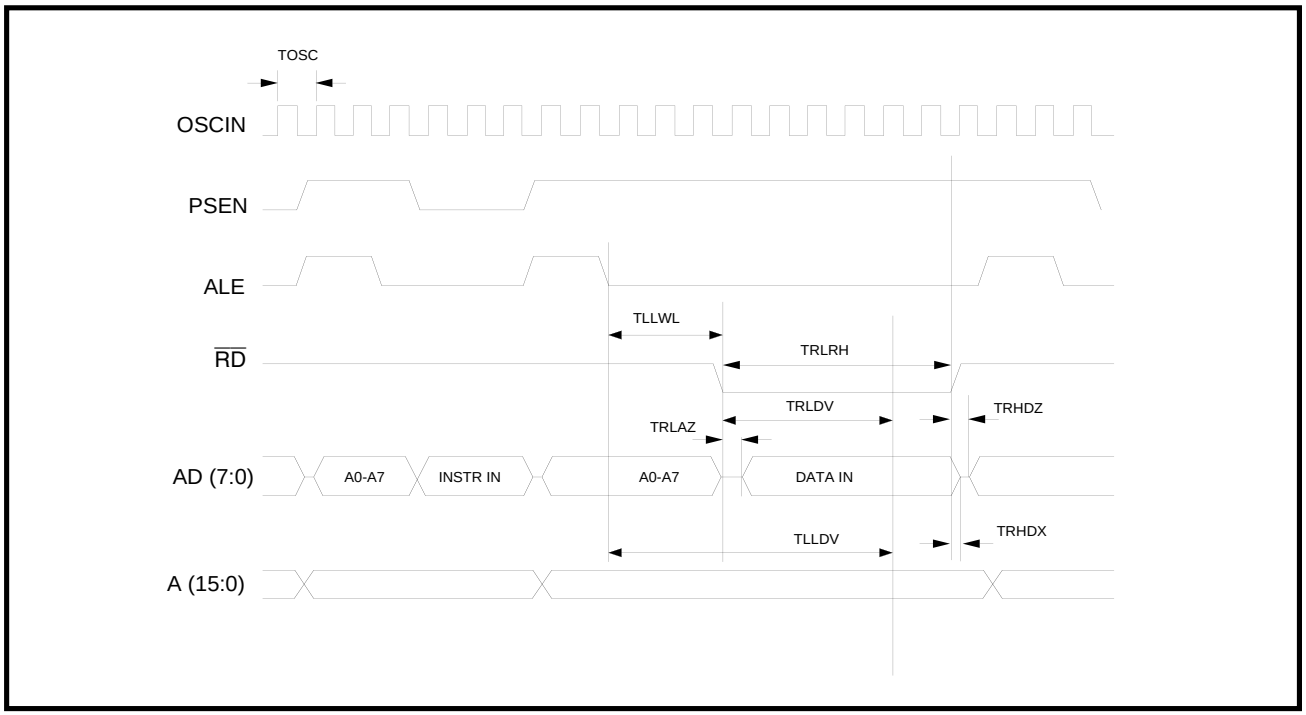
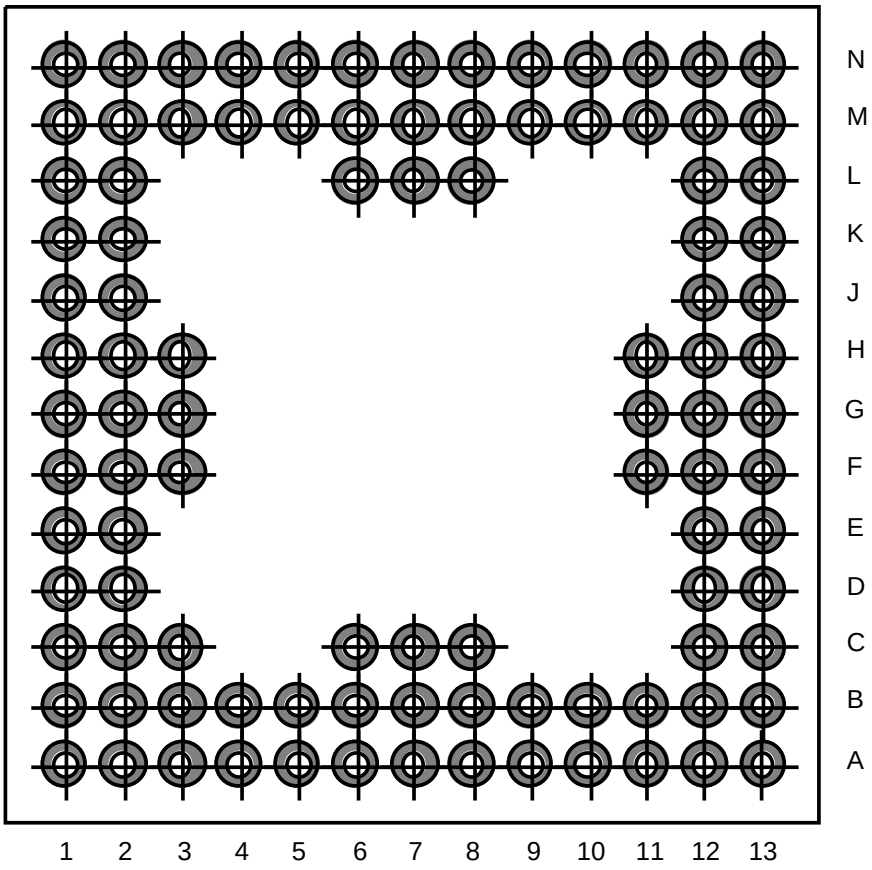


FIGURE 13: External Data Memory Read Cycle

PACKAGE PIN DESIGNATIONS

(Bottom View)

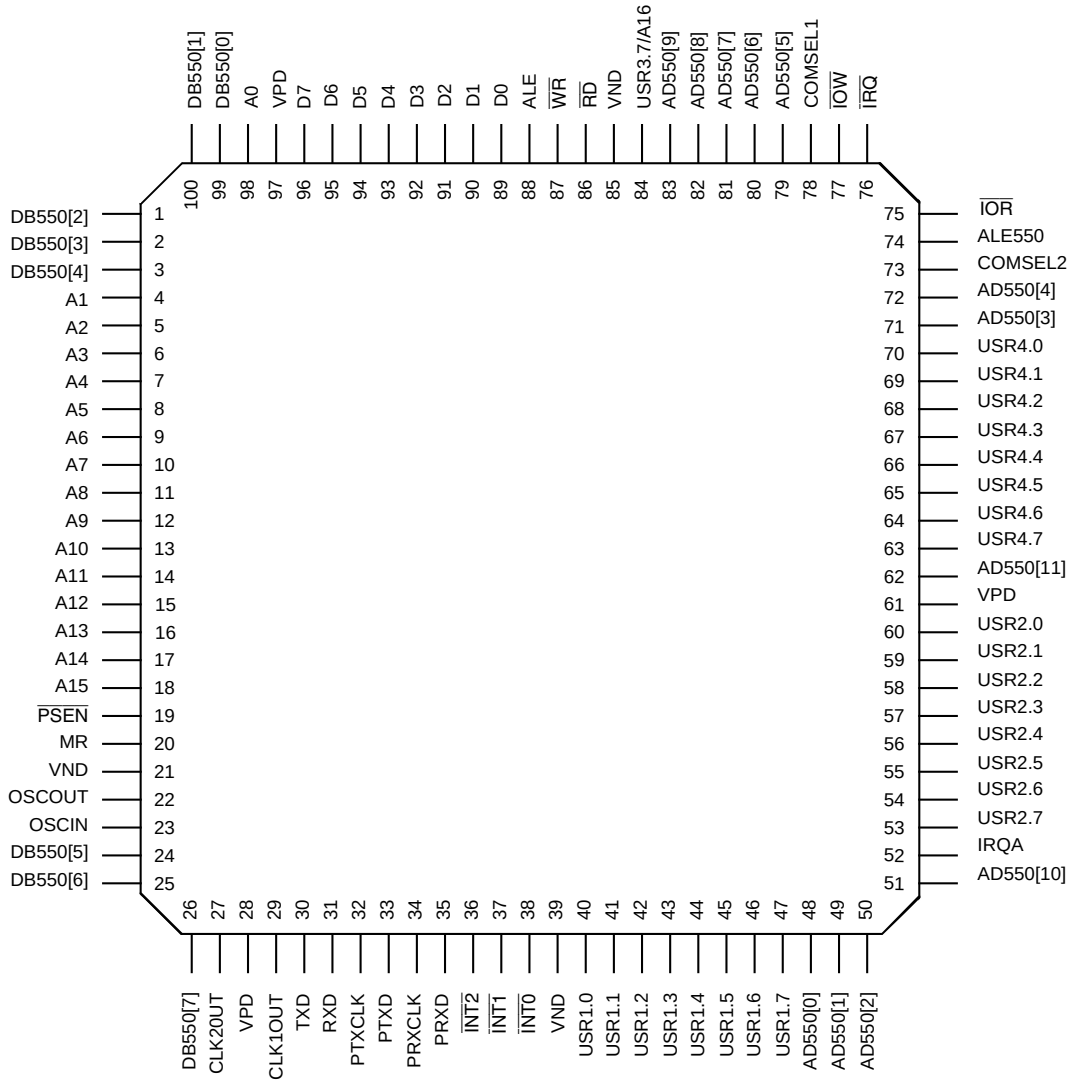


100-Pin PGA (Pin Grid Array)
Bottom View

CAUTION: Use handling procedures necessary for a static sensitive component.

PACKAGE PIN DESIGNATIONS

(Top View)



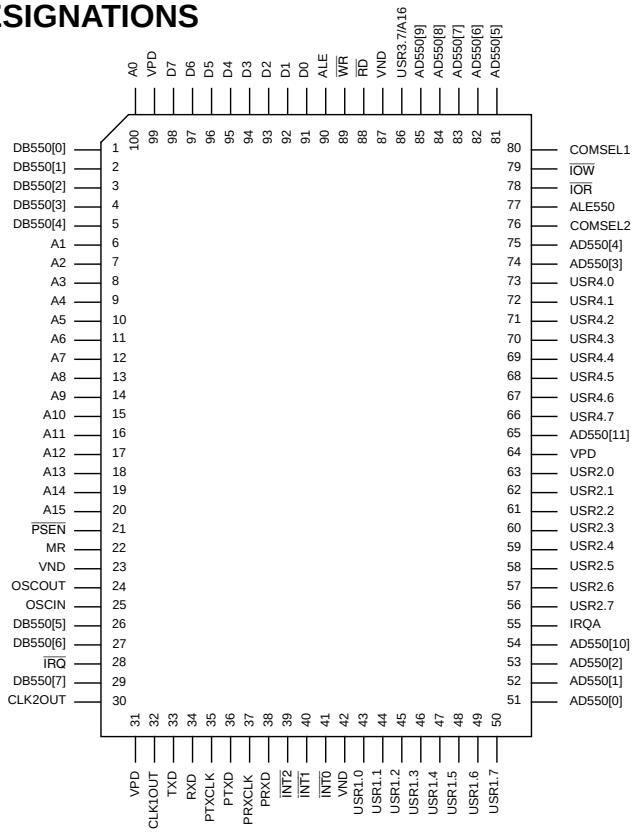
100-Lead TQFP

CAUTION: Use handling procedures necessary for a static sensitive component.

SSI 73M2918/2918A
Plug and Play
Microcontroller and UART

PACKAGE PIN DESIGNATIONS

(Top View)



100-Lead QFP

CAUTION: Use handling procedures necessary for a static sensitive component.

ORDERING INFORMATION

PART DESCRIPTION		ORDER NUMBER	PACKAGE MARK
SSI 73M2918	100-Lead QFP	73M2918-IG	73M2918-IG
	100-Lead TQFP	73M2918-IGT	73M2918-IGT
	100-Pin PGA	73M2918-IA	73M2918-IA
SSI 73M2918A	100-Lead QFP	73M2918A-IG	73M2918-IG
	100-Lead TQFP	73M2918A-IGT	73M2918-IGT
	100-Pin PGA	73M2918A-IA	73M2918-IA

Preliminary Data: Indicates a product not completely released to production. The specifications are based on preliminary evaluations and are not guaranteed. Small quantities are available, and Silicon Systems should be consulted for current information.

Silicon Systems, Inc., 14351 Myford Road, Tustin, CA 92680-7022 (714) 573-6000, FAX (714) 573-6914

silicon systems®
A TDK Group Company

SSI 73M2918B
Plug and Play Microcontroller and UART

Advance Information

March 1996

DESCRIPTION

The SSI 73M2918B is a combination of the SSI 73M2910 modem microcontroller, a virtual 550 UART, and built in hardware to support the Plug and Play ISA standard, implemented in Silicon Systems' advanced sub micron CMOS process. The 73M2918B is a version of the 73M2918, modified to permit external gating for 16-bit addressing required for Windows 95®. The 8-bit processor has the same attributes as the 8032 including instruction cycle time, UART, timers, interrupts, 256 bytes of on-chip RAM and programmable I/O. The virtual 550 UART utilizes proprietary technology, which results in complete emulation of the industry standard 550 UART, and adds significant features. The 550 UART emulator provides familiar 550 functionality to the PC and replaces the serial link between the PC and the dedicated processor with a parallel data interface. The architecture results in a high-performance system solution that is optimized for low power portable modem applications.

The SSI 73M2918B also includes the user friendly HDLC Packetizer that is available in the SSI 73M2910. It has serial I/O, hardware support for 16-bit and 32-bit CRC, zero insert/delete control, a dedicated interrupt and a clear channel mode for by-passing the packetizer.

Other features include additional user programmable I/O with programmable bank select and chip select logic, designed to eliminate board level glue logic. It also includes two general purpose input pins with programmable wakeup capability.

For devices that require non-multiplexed address and data buses, eight latched outputs for the low byte of the address are available.

The SSI 73M2918B has two extra interrupt sources, an external interrupt and an HDLC interrupt. The HDLC interrupt has two registers associated with it: the HDLC Interrupt Register which is used to determine the source of the interrupt, and the HDLC Interrupt Enable Register that enables the source of the interrupt.

FEATURES

- **Supports 16-bit addressing for Windows 95®**
- **8032 compatible instruction set**
- **Virtual 550 UART**
- **Dedicated Plug and Play ISA Bus Hardware**
- **44 MHz (SSI 73M2918AB)**
- **+ 5V power supply**
- **HDLC support logic (Packetizer, 16 and 32 CRC, zero ID)**
- **24 pins of user programmable I/O ports**
- **8 pins of programmable chip select logic for memory mapped peripherals**
- **3 external interrupt sources (programmable polarity)**
- **16 dedicated latched address pins**
- **Multiplexed data/address bus**
- **Instruction cycle time identical to 8032**
- **Buffered oscillator (OSC/2 or OSC/1.5) output pin**
- **1.8432 MHz UART clock available if crystal frequencies of 11.0592 MHz, 22.1184 MHz, 18.432 MHz, or 13.824 MHz are used**
- **Bank select circuitry to support up to 128k of external program memory**
- **Available in 100-Lead QFP, 100-Lead TQFP and 100-Pin PGA packages**

Advance Information: Indicates a product still in the design cycle, and any specifications are based on design goals only. Do not use for final design.

Silicon Systems, Inc., 14351 Myford Road, Tustin, CA 92680-7022 (714) 573-6000, FAX (714) 573-6914

Section 5

ANALOG SIGNALLING PRODUCTS

We are sorry, the 75T201 data sheet is not available in an electronic format. Please contact your local Sales office for more information or contact Silicon Systems directly to obtain a paper version.

Phone: (714) 573-6000
FAX: (714) 573-6914
E-mail: info@ssi1.com

Also, please visit SSi's World Wide Web home page at:

http://www.ssi1.com

Thank you.

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http://www.ssi1.com

Thank you.

Section 6

HIGH SPEED LINE TRANSCEIVERS

SSI 78P300

T1/E1 Integrated Short Haul Transceiver with Receive Jitter Attenuation

December 1993

DESCRIPTION

The SSI 78P300 is a fully integrated transceiver for both North American 1.544 MHz (T1), and European 2.048 MHz (E1/CEPT) applications. Transmit pulse shapes (DSX-1 or E1/CEPT) are selectable for various line lengths and cable types.

The SSI 78P300 provides receive jitter attenuation starting at 3 Hz, and is microprocessor controllable through a serial interface.

The SSI 78P300 offers a variety of diagnostic features including transmit and receive monitoring. Clock inputs may be derived from an on-chip crystal oscillator or digital inputs. The SSI 78P300 uses an advanced double-poly, double-metal CMOS process and requires only a single 5-volt power supply.

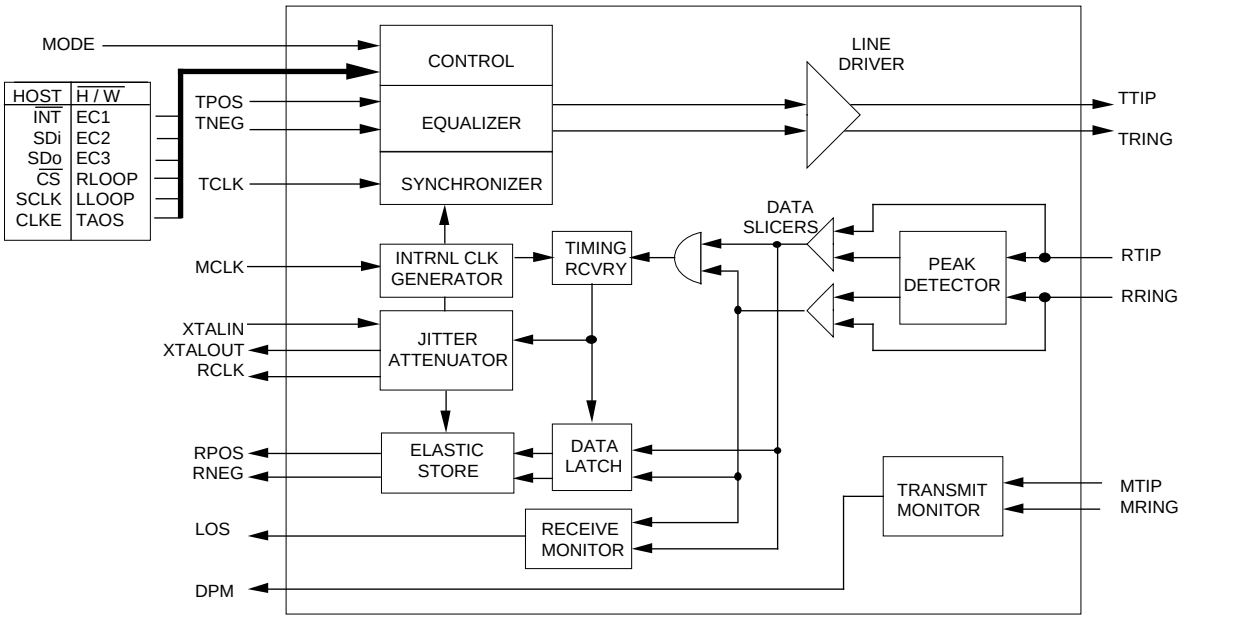
APPLICATIONS

- PCM / Voice Channel Banks
- Data Channel Bank / Concentrator
- T1 / E1 multiplexer
- Digital Access and Cross-connect Systems (DACS)
- Computer to PBX interface (CPI & DMI)
- High speed data transmission lines
- Interfacing Customer Premises Equipment to a CSU
- Digital Loop Carrier (DLC) terminals

FEATURES

- **Compatible with most popular PCM framers including the 2180A and 2181**
- **Line driver, data recovery and clock recovery functions**
- **Pin and functionally compatible with Crystal CS61574**
- **Minimum receive signal of 500 mV**
- **Selectable slicer levels (CEPT/DSX-1) improve SNR**
- **Programmable transmit equalizer shapes pulses to meet DSX-1 pulse template from 0 to 655 ft**
- **Local and remote loopback functions**
- **Transmit Driver Performance Monitor (DPM) output**
- **Receive monitor with Loss of Signal (LOS) output**
- **Receiver jitter tolerance 0.4 UI from 40 kHz to 100 kHz**
- **Microprocessor controllable**
- **Receive jitter attenuation starting at 6 Hz**
- **Available in 28 pin DIP or PLCC**

BLOCK DIAGRAM



CAUTION: Use handling procedures necessary for a static sensitive component.

FUNCTIONAL DESCRIPTION

The SSI 78P300 is a fully integrated PCM transceiver for both 1.544 MHz (DSX-1) and 2.048 MHz (CEPT) applications. This transceiver allows transmission of digital data over existing twisted-pair installations.

The SSI 78P300 transceiver interfaces with two twisted-pair lines (one twisted-pair for transmit, one twisted-pair for receive) through standard pulse transformers and appropriate resistors.

TRANSMITTER

Data received for transmission onto the line is clocked serially into the device at TPOS and TNEG. Input synchronization is supplied by the transmit clock (TCLK). The transmitted pulse shape is determined by Equalizer Control signals EC1 through EC3 as shown in Table 1. Refer to Table 2 and Figure 1 for master and transmit clock timing characteristics. Shaped pulses are applied to the AMI line driver for transmission onto the line at TTIP and TRING. Equalizer Control signals may be hardwired in the Hardware mode, or input as part of the serial data stream (SDI) in the Host mode.

Pulses can be shaped for either 1.544 or 2.048 MHz applications. 1.544 MHz pulses for DSX-1 applications can be programmed to match line lengths from 0 to 655 feet of ABAM cable. The SSI 78P300 also matches FCC and ECSA specifications for CSU applications. 2.048 MHz pulses can drive coaxial or shielded twisted-pair lines using appropriate resistors in line with the output transformer.

DRIVER PERFORMANCE MONITOR

The transceiver incorporates a Driver Performance Monitor (DPM) in parallel with the TTIP and TRING at the output transformer. The DPM output level goes high upon detection of 63 consecutive zeros. It is reset when a one is detected on the transmit line, or when a reset command is received.

LINE CODE

The SSI 78P300 transmits data as a 50% AMI line code as shown in Figure 2. Power consumption is reduced by activating the AMI line driver only to transmit a mark. The output driver is disabled during transmission of a space.

RECEIVER

The SSI 78P300 receives AMI signals from one twisted-pair line on each side of a center-grounded transformer. Positive pulses are received at RTIP and negative pulses are received at RRING. Recovered data is output at RPOS and RNEG, and the recovered clock is output at RCLK. Refer to Table 3 and Figure 3 for SSI 78P300 receiver timing.

The signal received at RPOS and RNEG is processed through the peak detector and data slicers. The peak detector samples the inputs and determines the maximum value of the received signal. A percentage of the peak value is provided to the data slicers as a threshold level to ensure optimum signal-to-noise ratio.

For DSX-1 applications (determined by Equalizer Control inputs EC1 - EC3 $\neq$ 000) the threshold is set to 70% of the peak value. This threshold is maintained above 65% for up to 15 successive zeros over the range of specified operating conditions. For CEPT applications (EC inputs = 000) the threshold is set to 50 %.

The receiver is capable of accurately recovering signals with up to -13.6 dB of cable attenuation (from 2.4 V), corresponding to a received signal level of approximately 500 mV (1500 feet of ABAM cable.) Regardless of received signal level, the peak detectors are held above a minimum level of .3 V to provide immunity from impulsive noise.

After processing through the data slicers, the received signal is routed to the data and clock recovery sections, and to the receive monitor. The receive monitor generates a Loss of Signal (LOS) output upon receipt of 175 consecutive zeros (spaces). The receiver monitor loads a digital counter at the RCLK frequency. The count is incremented each time a zero is received, and reset to zero each time a one (mark) is received. Upon receipt of 175 consecutive zeros the LOS pin goes high, and the RCLK output is replaced with the MCLK. If MCLK is not supplied the RCLK output will be replaced with the centered crystal clock.

The LOS pin will reset as soon as a one (mark) is detected.Recovered clock signals are supplied to the jitter attenuator and the data latch. The recovered data is passed to the elastic store where it is buffered and synchronized with the dejittered recovered clock (RCLK).

JITTER ATTENUATION

Jitter attenuation of the SSI 78P300 clock and data outputs is provided by a Jitter Attenuation Loop (JAL) and an Elastic Store (ES). An external crystal oscillating at 4 times the bit rate provides clock stabilization. Refer to Table 4 for crystal specifications. The ES is a 32 x 2-bit register. Recovered data is clocked into the ES with the recovered clock signal, and clocked out of the ES with the dejittered clock from the JAL. When the bit count in the ES is within two bits of overflowing or underflowing, the ES adjusts the output clock by 1/8 of a bit period. The ES produces an average delay of 16 bits in the receive path.

OPERATING MODES

The SSI 78P300 transceiver can be controlled through hard-wired pins (Hardware mode). This transceiver can also be commanded to operate in one of several diagnostic modes.

The SSI 78P300 can be controlled by a microprocessor through a serial interface (Host mode). The mode of operation is set by the MODE pin logic level.

HOST MODE OPERATION

To allow a host microprocessor to access and control the SSI 78P300 through the serial interface, MODE is set to 1. The serial interface (SDI/SDO) uses a 16-bit word consisting of an 8-bit Command/Address byte and an 8-bit Data byte. Figure 4 shows the serial interface data structure and timing.

The Host mode provides a latched Interrupt output ($\overline{INT}$) which is triggered by a change in the Loss of Signal (LOS) and/or Driver Performance Monitor (DPM) bits. The Interrupt is cleared when the interrupt condition no longer exists, and the host processor enables the respective bit in the serial input data byte. Host mode also allows control of the serial data and receive data output timing. The Clock Edge (CLKE) signal determines when these outputs are valid, relative to the Serial Clock (SCLK) or RCLK as follows:

CLKE	OUTPUT	CLOCK	VALID EDGE
LOW	RPOS	RCLK	RISING
	RNEG	RCLK	RISING
	SDO	SCLK	FALLING
HIGH	RPOS	RCLK	FALLING
	RNEG	RCLK	FALLING
	SDO	SCLK	RISING

The SSI 78P300 serial port is addressed by setting bit A4 in the Address/Command byte, corresponding to address 16. The SSI 78P300 contains only a single output data register so no complex chip addressing scheme is required. The register is accessed by causing the Chip Select (CS) input to make a transition from high to low. Bit 1 of the serial Address/Command byte provides Read/Write control when the chip is accessed. A logic 1 indicates a read operation, and a logic 0 indicates a write operation. Table 5 lists serial data output bit combinations for each status. Serial data I/O timing characteristics are shown in Table 6, and Figures 5 and 6.

HARDWARE MODE OPERATION

In Hardware mode the transceiver is accessed and controlled through individual pins. With the exception of the $\overline{INT}$ and CLKE functions, Hardware mode provides all the functions provided in the Host mode. In the Hardware mode RPOS and RNEG outputs are valid on the rising edge of RCLK. To operate in Hardware mode, MODE must be set to 0. Equalizer Control signals (EC1 through EC3) are input on the Interrupt, Serial Data In and Serial Data Out pins. Diagnostic control for Remote Loopback (RLOOP), Local Loopback (LLOOP), and Transmit All Ones (TAOS) modes is provided through the individual pins used to control serial interface timing in the Host mode.

RESET OPERATION

Upon power up, the transceiver is held static until the power supply reaches approximately 3V. Upon crossing this threshold, the device begins a 32 ms reset cycle to calibrate the transmit and receive delay lines and lock the Phase Lock Loop to the receive line. A reference clock is required to calibrate the delay lines. The transmitter reference is provided by TCLK. The crystal oscillator provides the receiver reference in the SSI 78P300. If the SSI 78P300 crystal oscillator is grounded, MCLK is used as the receiver reference clock.

The transceiver can also be reset from the Host or Hardware mode. In Host mode, reset is commanded by simultaneously writing RLOOP and LLOOP to the register. In Hardware mode, reset is commanded by holding RLOOP and LLOOP high simultaneously for 200 ns. Reset is initiated on the falling edge of the reset request. In either mode, reset clears and sets all registers to 0 and centers the oscillator, then begins calibration.

DIAGNOSTIC MODE OPERATION

In Transmit All Ones (TAOS) mode the TPOS and TNEG inputs to the transceiver are ignored. The transceiver transmits a continuous stream of 1's when the TAOS mode is activated. TAOS can be commanded simultaneously with Local Loopback, but is inhibited during Remote loopback.

In Remote Loopback (RLOOP) mode, the transmit data and clock inputs (TPOS, TNEG and TCLK) are ignored. The RPOS and RNEG outputs are looped back through the transmit circuits and output on TTIP and TRING at the RCLK frequency. Receiver circuits are unaffected by the RLOOP command and continue to output the RPOS, RNEG and RCLK signals received from the twisted-pair line.

In Local Loopback (LLOOP) mode, the receiver circuits are inhibited. The transmit data and clock inputs (TPOS, TNEG and TCLK) are looped back onto the receive data and clock outputs (RPOS, RNEG and RCLK.) The transmitter circuits are unaffected by the LLOOP command. The TPOS and TNEG inputs (or a stream of 1's if the TAOS command is active) will be transmitted normally. When used in this mode with a crystal, the transceiver can be used as a stand-alone jitter attenuator.

POWER REQUIREMENTS

The SSI 78P300 is a low-power CMOS device. It operates from a single +5V power supply which can be connected externally to both the transmitter and receiver. However, the two inputs must be within ±.3V of each other, and decoupled to their respective grounds separately, as shown in Figure 7. Isolation between the transmit and receive circuits is provided internally.

PIN DESCRIPTION

NAME	TYPE	DESCRIPTION
MCLK	I	Master Clock: A 1.544 or 2.048 MHz clock input used to generate internal clocks. Upon Loss of Signal (LOS), RCLK is derived from MCLK. If MCLK not applied, this pin should be grounded.
TCLK	I	Transmit Clock: Transmit clock input. TPOS and TNEG are sampled on the falling edge of TCLK.
TPOS	I	Transmit Positive Data: Input for positive pulse to be transmitted on the twisted-pair or coaxial cable.
TNEG	I	Transmit Negative Data: Input for negative pulse to be transmitted on the twisted-pair or coaxial cable.
MODE	I	Mode Select: Setting MODE to logic 1 puts the SSI 78P300 in the Host mode. In the Host mode, the serial interface is used to control the SSI 78P300 and determined its status. Setting MODE to logic 0 puts the SSI 78P300 in the Hardware (H/W) mode. In the Hardware mode the serial interface is disabled and hard-wired pins are used to control configuration and report status.
RNEG/RPOS	O	Receive Negative Data/Receive Positive Data: Received data outputs. A signal on RNEG corresponds receipt of a negative pulse on RTIP and RRING. A signal on RPOS corresponds to receipt of a positive pulse on RTIP and RRING. RNEG and RPOS outputs are Non-Return-to-Zero (NRZ). In the Host Mode, CLKE determines the clock edge (RCLK) at which these outputs are stable and valid. In the Hardware mode both outputs are stable and valid on the rising edge or RCLK.
RCLK	O	Recovered Clock: This is the clock recovered from the signal received at RTIP and RRING.

PIN DESCRIPTION (continued)

NAME	TYPE	DESCRIPTION
XTALIN/ XTALOUT	I/O	Crystal Input/Crystal Output: An external crystal operating at four times the bit rate (6.176 MHz for DSX-1, 8.192 MHz for CEPT applications with an 18.7 pF load) is required to enable the jitter attenuation function of the SSI 78P300. These pins may also be used to disable the jitter attenuator by connecting the XTALIN pin to the positive supply through a resistor, and tying the XTALOUT pin to ground.
DPM	O	Driver Performance Monitor: DPM goes to a logic 1 when the transmit monitor loop (MTIP and MRING) does not detect a signal for 63 ±2 clock periods. DPM remains at logic 1 until a signal is detected.
LOS	O	Loss Of Signal: LOS goes to a logic 1 when 175 consecutive spaces have been detected. LOS returns to a logic 0 when a mark is detected.
TTIP/TRING	O	Transmit Tip/Transmit Ring: Differential Driver Outputs. These outputs are designed to drive a 25 Ω load. The transmitter will drive 100 Ω shielded twisted-pair cable through a 2:1 step-up transformer without additional components. To drive 75 Ω coaxial cable, two 2.2 Ω resistors are required in series with the transformer.
TGND	-	Transmit Ground: Ground return for the transmit drivers power supply TV+.
TV+	I	Transmit Power Supply: +5 VDC power supply input for the transmit drivers. TV+ must not vary from RV+ by more than ±0.3V.
MTIP/MRING	I	Monitor Tip/Monitor Ring: These pins are used to monitor the tip and ring transmit outputs. The transceiver can be connected to monitor its own output or the output of another SSI 78P300. To prevent false interrupts in the Host mode if the monitor is not used, apply a clock signal to one of the monitor pins and tie the other monitor pin to approximately the clock's mod-level voltage. The monitor clock can range from 100 kHz to the TCLK frequency.
RTIP/RRING	I	Receive Tip/Receive Ring: The AMI signal received from the line is applied at these pins. A center-tapped, center-grounded, 2:1 step-up transformer is required on these pins. Data and clock from the signal applied at these pins are recovered and output on the RPOS/RNEG, and RCLK pins.
RV+	I	Receive Power Supply: +5 VDC power supply for all circuits except the transmit drivers. (Transmit drivers are supplied by TV+.)
RGND	-	Receive Ground: Ground return for power supply RV+.
$\overline{\text{INT}}$	O	Interrupt (Host Mode): This SSI 78P300 Host mode output goes low to flag the host processor when LOS or DPM go active. $\overline{\text{INT}}$ is an open-drain output and should be tied to power supply RV+ through a resistor. $\overline{\text{INT}}$ is reset by clearing the respective register bit (LOS and/or DPM.)
EC1	I	Equalizer Control 1 (H/W Mode): The signal applied at this pin in the SSI 78P300 Hardware mode is used in conjunction with EC2 and EC3 inputs to determine shape and amplitude of AMI output transmit pulses.

PIN DESCRIPTION (continued)

NAME	TYPE	DESCRIPTION
SDI	I	Serial Data In (Host Mode): The serial data input stream is applied to this pin when the SSI 78P300 operates in the Host mode. SDI is sampled on the rising edge of SCLK.
EC2	I	Equalizer Control 2 (H/W Mode): The signal applied at this pin in the SSI 78P300 Hardware mode is used in conjunction with EC1 and EC3 inputs to determine shape and amplitude of AMI output transmit pulses.
SDO	O	Serial Data Out (Host Mode): The serial data from the on-chip register is output on this pin in the SSI 78P300 Host mode. If CLKE is high, SDO is valid on the rising edge of SCLK. If CLKE is low SDO is valid on the falling edge of SCLK. This pin goes to a high-impedance state when the serial port is being written to and when $\overline{CS}$ is high.
EC3	I	Equalizer Control 3 (H/W Mode): The signal applied at this pin in the SSI 78P300 Hardware mode is used in conjunction with EC1 and EC2 inputs to determine shape and amplitude of AMI output transmit pulses.
$\overline{CS}$	I	Chip Select (Host Mode): This input is used to access the serial interface in the SSI 78P300 Host mode. For each read or write operation, $\overline{CS}$ must remain low for duration of operation.
RLOOP	I	Remote Loopback (H/W Mode): This input controls loopback functions in the SSI 78P300 Hardware mode. Setting RLOOP to a logic 1 enables the Remote Loopback mode. Setting both RLOOP and LLOOP causes a Reset.
SCLK	I	Serial Clock (Host Mode): This clock is used in the SSI 78P300 Host mode to write data to or read data from the serial interface registers.
LLOOP	I	Local Loopback (H/W Mode): This input controls loopback functions in the SSI 78P300 Hardware mode. Setting LLOOP to a logic 1 enables the Local Loopback Mode.
CLKE	I	Clock Edge (Host Mode): Setting CLKE to logic 1 causes RPOS and RNEG to be valid on the falling edge of RCLK, and SDO to be valid on the rising edge of SCLK. When CLKE is a logic 0, RPOS and RNEG are valid on the rising edge of RCLK, and SDO is valid on the falling edge of SCLK.
TAOS	I	Transmit All Ones (H/W Mode): When set to a logic 1, TAOS causes the SSI 78P300 (Hardware mode) to transmit a continuous stream of marks at the TCLK frequency. Activating TAOS causes TPOS and TNEG inputs to be ignored. TAOS is inhibited during Remote Loopback.

ELECTRICAL SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Operation above maximum ratings may damage the device.

PARAMETER	RATING
DC Supply (referenced to GND), RV+, TV+	0 to 6.0V
Input Voltage, Any Pin, V_{IN} (see note 1)	RGND -0.03 to RV+ +0.03V
Input Current, Any Pin, I_{In} (see note 2)	-10 to 10mA
Ambient Operating Temperature, T_A	-40 to 85°C
Storage Temperature, T_{STG}	-65 to 150°C

[1] Excluding RTIP and RRING which must stay within -6V to RV+ + 0.3V.

[2] Transient currents of up to 100 mA will not cuase SCR latch-up. TTIP, TRING, TV+ and TGND can withstand a continuous current of 100 mA.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
DC supply , RV+, TV+ (see note 1)		4.75	5.0	5.25	V
Ambient Operating Temp., T_A		-40	25	85	°C
Total Power Dissipation, P_D (see note 2)	100% Ones Density & Maximum Line Length @ 5.25V	-	620	-	mW

[1] TV+ must not exceed RV+ by more than ±0.3V.

[2] Power dissipation while driving 25Ω load over operating temperature range. Includes device and load. Digital input levels are within 10% of the supply rails and digital outputs are driving a 50pF capacitive load.

DIGITAL CHARACTERISTICS

T_A = -40° to 85°C, V+ = 5.0 V± 5%, GND = 0V

V_{IH}	High Level Input Voltage (pins 1-5, 10, 23-28) (see note 1, 2)		2.0	-	-	V
V_{IL}	Low Level Input Voltage (pins 1-5, 10, 23-28) (see note 1, 2)		-	-	0.8	V
V_{OH}	High Level Output Voltage (pins 6-8, 11, 12, 23, 25) (see note 1, 2)	I_{OUT} = -400 µA	2.4	-	-	V
V_{OL}	Low Level Output Voltage (pins 6-8, 11, 12, 23, 25) (see note 1, 2)	I_{OUT} = 1.6 mA	-	-	0.4	V
I_{LL}	Input Leakage Current		0		±10	µA
I_{3L}	Three -State Leakage Current (pin 25) (see note 1)		0	-	±10	µA

[1] Functionality of pins 23 and 25 depends on mode. See Host / Hardware Mode descriptions.

[2] Output drivers will output CMOS logic levels into CMOS loads.

ELECTRICAL SPECIFICATIONS (continued)

ANALOG SPECIFICATIONS

T_A = -40° to 85°C, V+ = 5.0 V± 5%, GND = 0V

PARAMETER		TEST CONDITIONS	MIN	NOM	MAX	UNIT
AMI Output Pulse Amplitudes	DSX-1	Measured at the DSX	2.4	3.0	3.6	V
	CEPT	Measured at Line Side	2.7	3.0	3.3	V
Load Presented to Transmitter Output			-	25	-	Ω
Jitted Added	10 Hz - 8 kHz		-	-	0.01	UI
by the Transmitter	8 kHz - 40 kHz		-	-	0.025	UI
(see note 1)	10 Hz - 40 kHz		-	-	0.025	UI
	Broad Band		-	-	0.05	UI
Sensitivity Below DSX	(0dB = 2.4V)		13.6	-	-	dB
			500	-	-	mV
Loss of Signal Threshold			-	0.3	-	V
Data Decision Threshold	DSX-1		63	70	77	%peak
	CEPT		43	50	57	%peak
Allowable Consecutive Zeros Before LOS			160	175	190	-
Input Jitter Tolerance 10 kHz - 100 kHz			0.4	-	-	UI
Jitter Attenuation Curve Corner Frequency (see note 2)			-	3	-	Hz

[1] Input signal to TCLK is jitter-free.
[2] Circuit attenuates jitter at 20 dB/decade above the corner frequency.

TABLE 1: Equalizer Control Inputs

EC3	EC2	EC1	LINE LENGTH	CABLE LOSS	APPLICATION	FREQUENCY
0	1	1	0 - 133 ft ABAM	0.6 dB		
1	0	0	133 - 266 ft ABAM	1.2 dB		
1	0	1	266 - 399 ft ABAM	1.8 dB	DSX-1	1.544 MHz
1	1	0	399 - 533 ft ABAM	2.4 dB		
1	1	1	533 - 655 ft ABAM	3.0 dB		
0	0	0	CCITT Recommendation G.703		CEPT	2.048 MHz
0	1	0	FCC Part 68, Option A		CSU	1.544 MHz
0	1	1	ECSA T1C1.2			

TABLE 2: 78P300 Master Clock and Transmit Timing Characteristics

PARAMETER			CONDITIONS	MIN	NOM	MAX	UNIT
Master clock frequency	MCLK	DSX-1		-	1.544	-	MHz
	MCLK	CEPT		-	2.048	-	MHz
Master clock tolerance	MCLKt			-	±100	-	ppm
Master clock duty cycle	MCLKd			40	-	60	%
Crystal frequency	fc	DSX-1		-	6.176	-	MHz
	fc	CEPT		-	8.192	-	MHz
Transmit clock frequency	TCLK	DSX-1		-	1.544	-	MHz
	TCLK	CEPT		-	2.048	-	MHz
Transmit clock tolerance	TCLKt			-	-	±50	ppm
Transmit clock duty cycle	TCLKd			10	-	90	%
TPOS/TNEG to TCLK setup time	t_{SUT}			25	-	-	ns
TCLK to TPOS/TNEG Hold time	t_{HT}			25	-	-	ns

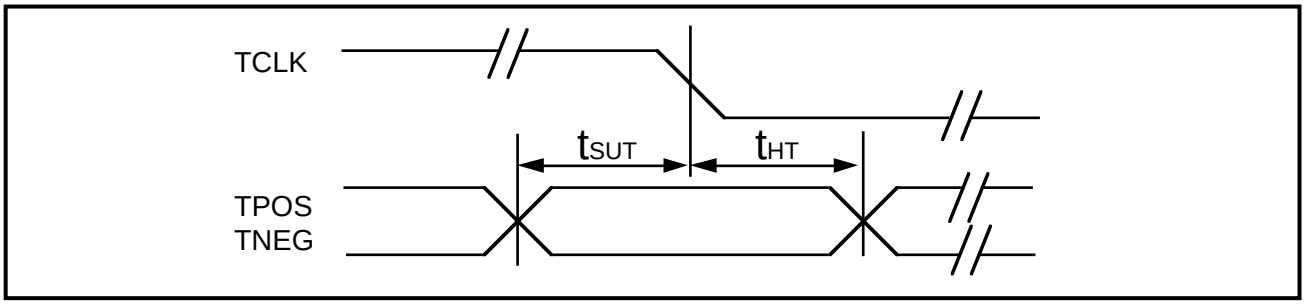


FIGURE 1: 78P300 Transmit Clock Timing Diagram

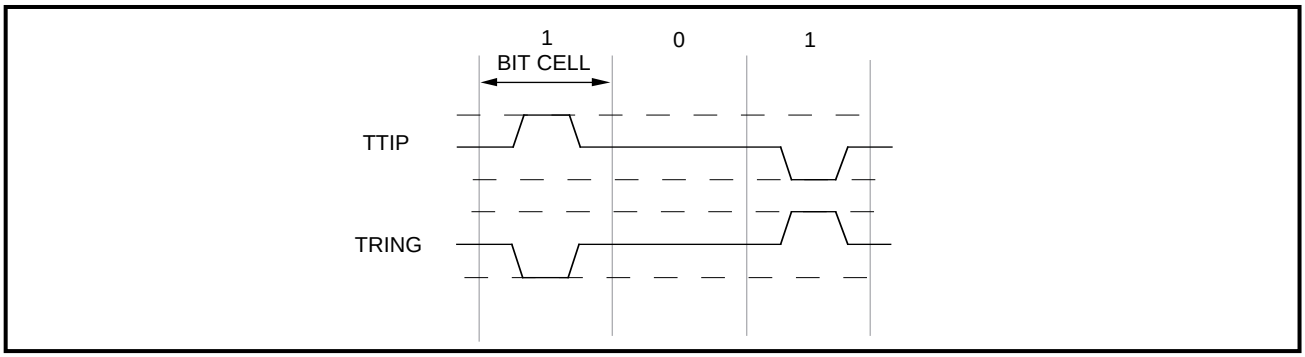


FIGURE 2: 50% AMI Coding Diagram

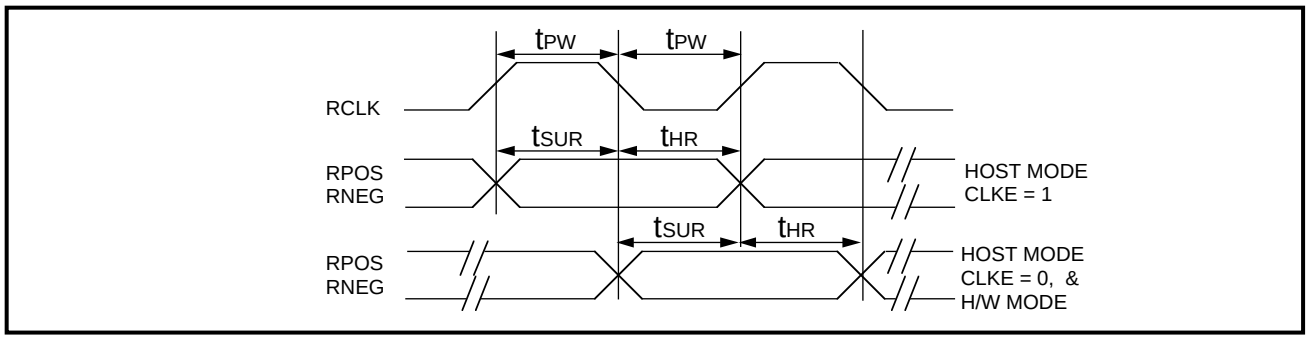


FIGURE 3: 78P300 Receive Clock Timing Diagram

TABLE 3: 78P300 Receive Timing Characteristics

PARAMETER			CONDITIONS	MIN	NOM[1]	MAX	UNIT
Receive clock duty cycle RCLKd				40	-	60	%
Receive clock pulse width	t_{PW}	DSX-1		-	324	-	ns
	t_{PW}	CEPT		-	244	-	ns
RPOS/RNEG to RCLK	t_{SUR}	DSX-1		-	274	-	ns
rising setup time	t_{SUR}	CEPT		-	194	-	ns
RCLK rising to RPOS/	t_{HR}	DSX-1		-	274	-	ns
RNEG hold time	t_{HR}	CEPT		-	194	-	ns

[1] Typical figures are at 25°C and are for design aid only; not guaranteed and not subject to production testing.

TABLE 4: SSI 78P300 Crystal Specifications (External)

PARAMETER	T1	CEPT
Frequency	6.176 MHz	8.192 MHz
Frequency Stability	±20 ppm @ 25°C	±20 ppm @ 25°C
	±25 ppm from -40°C to + 85°C (Ref 25°C reading)	± 25 ppm from -40°C to + 85°C (Ref 25°C reading)
Pullability	CL = 11 pF to 18.7 pF, +ΔF = 175 to 195 ppm	CL = 11 pF to 18.7 pF, +ΔF = 95 to 115 ppm
	CL = 18.7 pF to 34 pF, -ΔF = 175 to 195 ppm	CL = 18.7 pF to 34 pF, -ΔF = 95 to 115 ppm
Effective series resistance	40 Ω Maximum	30 Ω Maximum
Crystal cut	AT	AT
Resonance	Parallel	Parallel
Maximum drive level	2.0 mW	2.0 mW
Mode of operation	Fundamental	Fundamental
Crystal holder	HC49 (R3W), C_O = 7 pF Maximum, C_M = 17 pF typical	HC49 (R3W), C_O = 7 pF Maximum, C_M = 17 pF typical

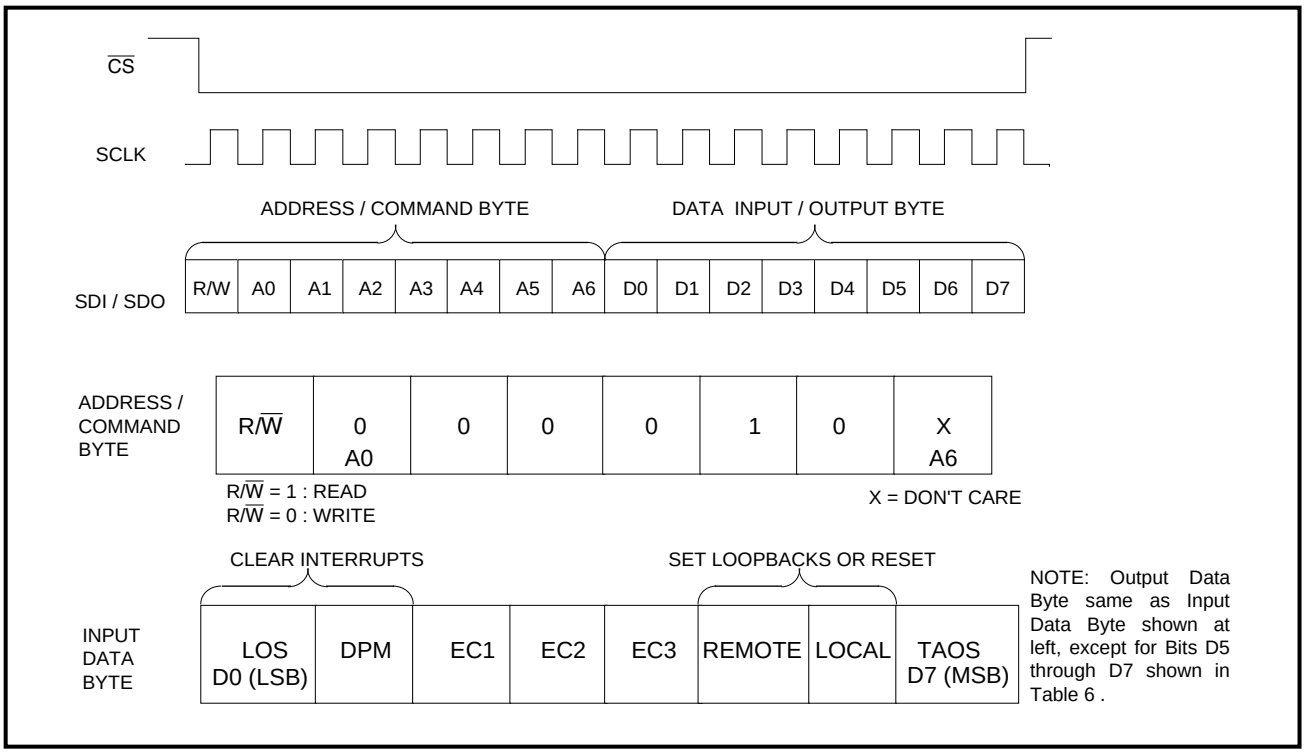


FIGURE 4: SSI 78P300 Serial Interface Data Structure

TABLE 5: SSI 78P300 Serial Data Output Bits (See Figure 4)

BIT D5	BIT D6	BIT D7	STATUS
0	0	0	Reset has occurred, or no program input.
0	0	1	TAOS active
0	1	0	Local Loopback active
0	1	1	TAOS and Local Loopback active
1	0	0	Remote Loopback active
1	0	1	DPM has changed state since last Clear DPM occurred
1	1	0	LOS has changed state since last Clear LOS occurred
1	1	1	LOS and DPM have both changed state since last Clear DPM and Clear LOS occurred

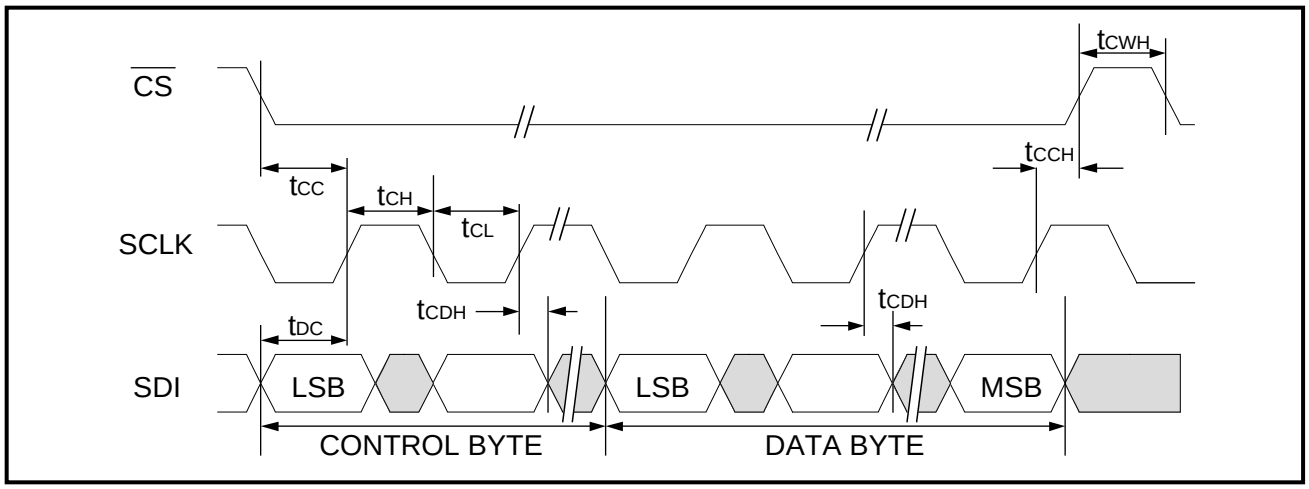


FIGURE 5: SSI 78P300 Serial Data Input Timing Diagram

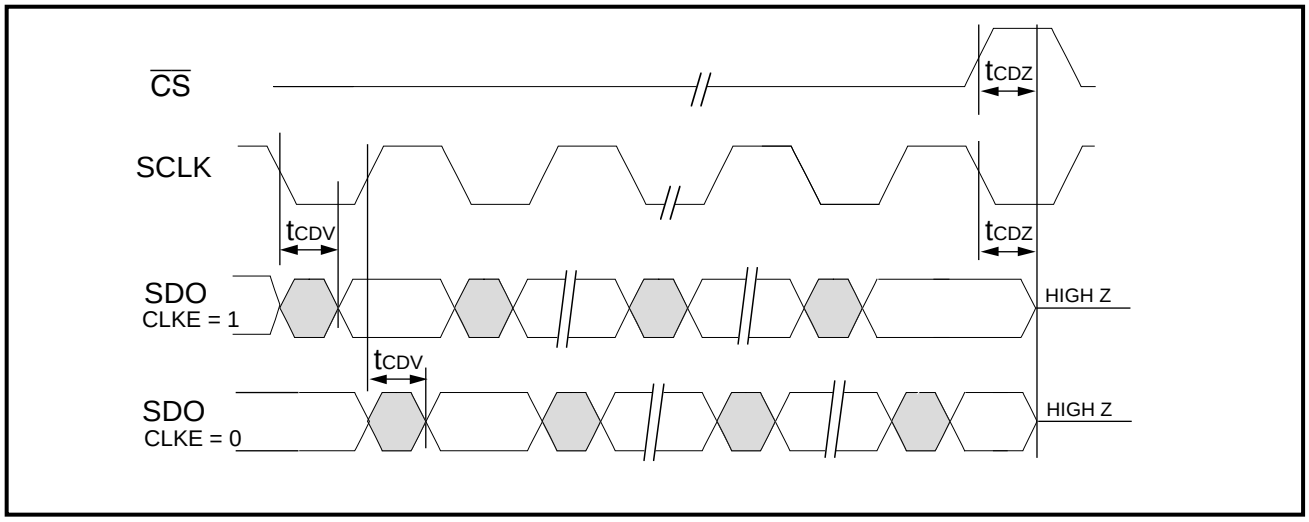


FIGURE 6: SSI 78P300 Serial Data Output Timing Diagram

TABLE 6: SSI 78P300 Serial I/O Timing Characteristics (See Figures 5 and 6)

PARAMETER		CONDITIONS	MIN	NOM[1]	MAX	UNIT
Rise/Fall time - any digital output	t_{RF}	Load 1.6 mA, 50 pF	-	-	100	ns
SDI to SCLK setup time	t_{DC}		50	-	-	ns
SCLK to SDI hold time	t_{CDH}		50	-	-	ns
SCLK low time	t_{CL}		240	-	-	ns
SCLK high time	t_{CH}		240	-	-	ns
SCLK rise and fall time	t_R, t_F		-	-	50	ns
CS to SCLK setup time	t_{CC}		50	-	-	ns
SCLK to CS hold time	t_{CCH}		50	-	-	ns
CS inactive time	t_{CWH}		250	-	-	ns
SCLK to SDO valid	t_{CDV}		-	-	200	ns
SCLK falling edge or CS rising edge to SDO high Z	t_{CDZ}		-	100	-	ns

[1] Typical figures are at 25°C and are for desing aid only; not guaranteed and not subject to production testing.

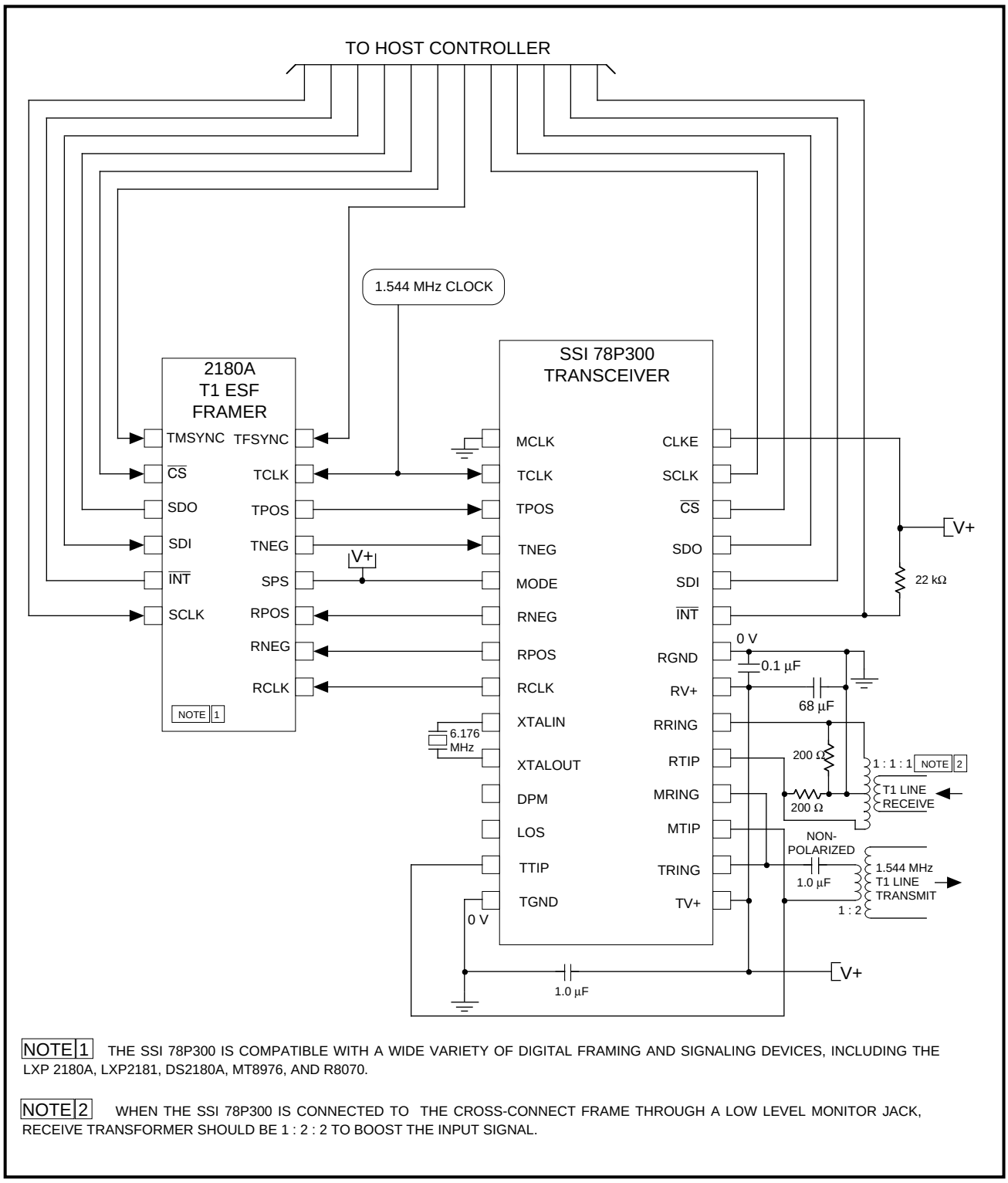
APPLICATION INFORMATION

SSI 78P300 1.544 MHz T1 INTERFACE APPLICATIONS

Figure 7 is a typical 1.544 MHz T1 application. The SSI 78P300 is shown in the Host mode with the 2180A T1/ESF Framer providing the digital interface with the host controller. Both devices are controlled through the serial interface. The power supply inputs are tied to a common bus with appropriate decoupling capacitors installed (1.0 µF on the transmit side, 68 µF and 0.1 µF on the receive side.)

SSI 78P300 2.048 MHz E1/CEPT INTERFACE APPLICATIONS

Figure 8 is a typical 2.048 MHz E1/CEPT application. The SSI 78P300 is shown in Hardware mode with the 2181 E1/CRC4 Framer. Resistors are installed in line with the transmit transformer for loading a 75 Ω coaxial cable. The in-line resistors are not required for transmission on 100 Ω shielded twisted-pair lines. As in the T1 application Figure 7, this configuration is illustrated with a crystal in place to enable the SSI 78P300 Jitter Attenuation Loop, and a single power supply bus. The hard-wired control lines for TAOS, LLOOP and RLOOP are individually controllable, and the LLOOP and RLOOP lines are also tied to a single control for the Reset function.



NOTE 1 THE SSI 78P300 IS COMPATIBLE WITH A WIDE VARIETY OF DIGITAL FRAMING AND SIGNALING DEVICES, INCLUDING THE LXP 2180A, LXP2181, DS2180A, MT8976, AND R8070.

NOTE 2 WHEN THE SSI 78P300 IS CONNECTED TO THE CROSS-CONNECT FRAME THROUGH A LOW LEVEL MONITOR JACK, RECEIVE TRANSFORMER SHOULD BE 1 : 2 : 2 TO BOOST THE INPUT SIGNAL.

FIGURE 7: Typical SSI 78P300 1.544 MHz T1 Application (Host Mode)

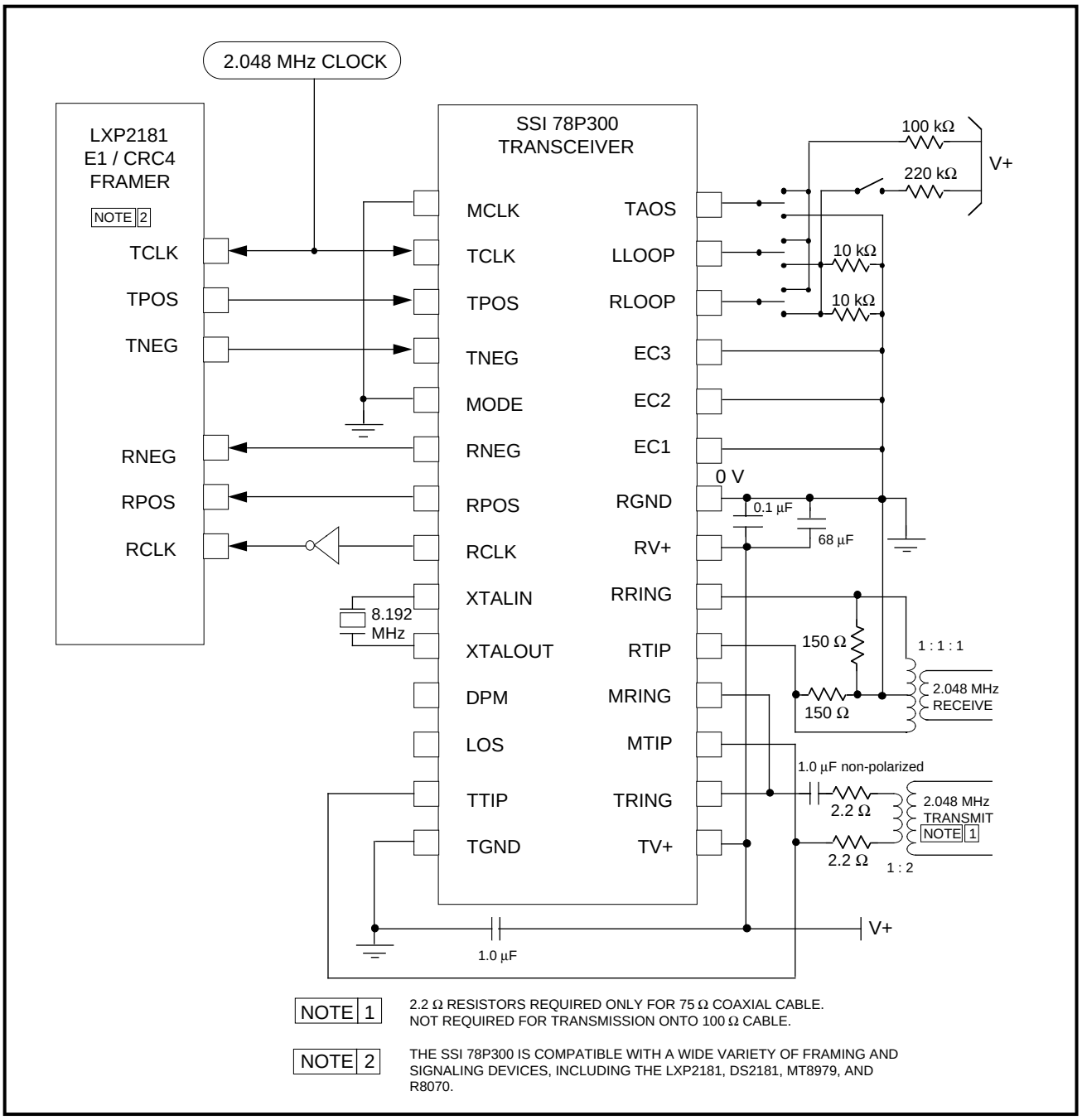
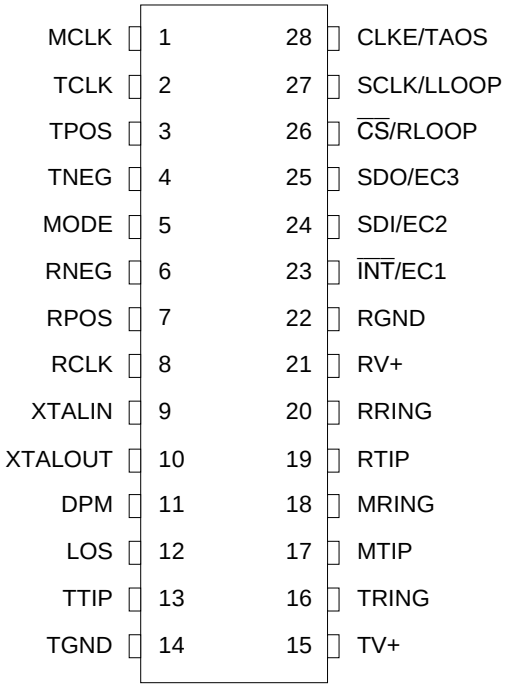


FIGURE 8: Typical SSI 78P300 2.048 MHz E1 Application (Hardware Mode)

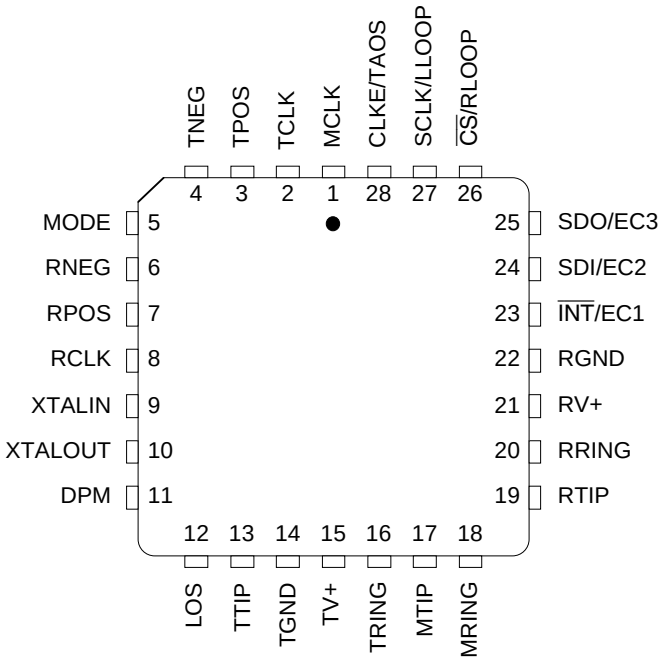
PACKAGE PIN DESIGNATIONS

(Top View)

CAUTION: Use handling procedures necessary for a static sensitive component.



28-Pin DIP



28-Pin PLCC

ORDERING INFORMATION

PART DESCRIPTION	ORDER NO.	PKG. MARK
SSI 78P300 28-Pin PLCC	78P300-IH	78P300-IH
SSI 78P300 28-Pin DIP	78P300-IP	78P300-IP

Silicon Systems, Inc., 14351 Myford Road, Tustin, CA 92680-7022 (714) 573-6000, FAX (714) 573-6914

SSI 78P304A

Low-Power T1/E1 Integrated Short Haul Transceiver with Receive Jitter Attenuation

December 1993

DESCRIPTION

The SSI 78P304A is a fully integrated low-power transceiver for both North American 1.544 MHz (T1), and European 2.048 MHz (E1/CEPT) applications. It features a constant low output impedance transmitter allowing for high transmitter return loss in E1 applications. Transmit pulse shapes (DSX-1 or E1/CEPT) are selectable for various line lengths and cable types.

The SSI 78P304A provides receive jitter attenuation starting at 3 Hz, and is microprocessor controllable through a serial interface.

The SSI 78P304A offers a variety of diagnostic features including transmit and receive monitoring. The device incorporates an on-chip crystal oscillator, and also accepts digital clock inputs. It uses an advanced double-poly, double-metal CMOS process and requires only a single 5-volt power supply.

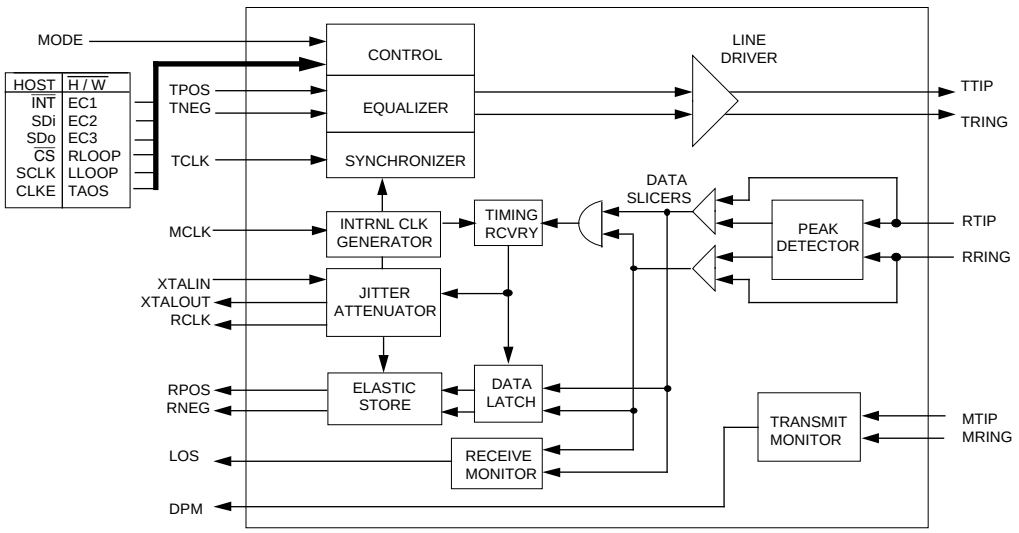
APPLICATIONS

- PCM / Voice Channel Banks
- Data Channel Bank / Concentrator
- T1 / E1 multiplexer
- Digital Access and Cross-connect Systems (DACS)
- Computer to PBX interface (CPI & DMI)
- High speed data transmission lines
- Interfacing Customer Premises Equipment to a CSU
- Digital Loop Carrier (DLC) terminals

FEATURES

- **Low power consumption (400 mW maximum) 40% less than the SSI 78P300**
- **Constant low output impedance transmitter regardless of data pattern**
- **High transmit and receive return loss**
- **Meets or exceeds all industry specifications including CCITT G.703, ANSI T1.403 and ATT Pub 62411**
- **Compatible with most popular PCM framers including the 2180A (T1) and 2181/2181A (E1)**
- **Line driver, data recovery and clock recovery functions**
- **Minimum receive signal of 500 mV**
- **Selectable slicer levels (CEPT/DSX-1) improve SNR**
- **Programmable transmit equalizer shapes pulses to meet DSX-1 pulse template from 0 to 655 ft**
- **Local and remote loopback functions Transmit / Receive performance monitors with DPM and LOS outputs**
- **Receiver jitter tolerance 0.4 UI from 40 kHz to 100 kHz**
- **Receive jitter attenuation starting at 6 Hz**
- **Microprocessor controllable**
- **Available in 28 pin DIP or PLCC**

FIGURE 1: BLOCK DIAGRAM



FUNCTIONAL DESCRIPTION

The SSI 78P304A is a fully integrated PCM transceiver for both 1.544 MHz (DSX-1) and 2.048 MHz (E1) applications. It allows transmission of digital data over existing twisted-pair installations. The SSI 78P304A transceiver interfaces with two twisted-pair lines, one twisted-pair for transmit, one twisted-pair for receive.

TRANSMITTER

Data received for transmission onto the line is clocked serially into the device at TPOS and TNEG. Input synchronization is supplied by the transmit clock (TCLK). The transmitted pulse shape is determined by Equalizer Control signals EC1 through EC3 as shown in Table 1. Refer to Table 2 and Figure 2 for master and transmit clock timing characteristics. Shaped pulses are applied to the AMI line driver for transmission onto the line at TTIP and TRING. Equalizer Control signals may be hardwired in the Hardware mode, or input as part of the serial data stream (SDI) in the Host mode.

Pulses can be shaped for either 1.544 or 2.048 MHz applications. 1.544 MHz pulses for DSX-1 applications can be programmed to match line lengths from 0 to 655 feet of ABAM cable. The SSI 78P304A also matches FCC and ECSA specifications for CSU applications. A 1:1.15 transmit transformer is used for all 1.544 MHz systems.

2.048 MHz pulses can drive coaxial or shielded twisted-pair lines. For E1 systems, a 1:2 transmit transformer and series resistors are recommended. This design meets or exceeds all CCITT and European PTT specifications for transmit and receive return loss. A 1:1 or 1:1.26 transformer may be used without series resistors.

DRIVER PERFORMANCE MONITOR

The transceiver incorporates a Driver Performance Monitor (DPM) in parallel with TTIP and TRING at the output transformer. The DPM output goes high upon detection of 63 consecutive zeros. It is reset when a one is detected on the transmit line, or when a reset command is received.

LINE CODE

The SSI 78P304A transmits data as a 50% AMI line code as shown in Figure 3. The output driver maintains a constant low output impedance regardless of whether it is driving marks or spaces.

RECEIVER

The SSI 78P304A receives the signal input from one twisted-pair line on each side of a center-grounded transformer. Positive pulses are received at RTIP and negative pulses are received at RRING. Recovered data is output at RPOS and RNEG, and the recovered clock is output at RCLK. Refer to Table 3 and Figure 4 for SSI 78P304A receiver timing.

The signal received at RPOS and RNEG is processed through the peak detector and data slicers. The peak detector samples the inputs and determines the maximum value of the received signal. A percentage of the peak value is provided to the data slicers as a threshold level to ensure optimum signal-to-noise ratio. For DSX-1 applications (determined by Equalizer Control inputs EC1 - EC3 $\neq$ 000) the threshold is set to 70% of the peak value. This threshold is maintained above 65% for up to 15 successive zeros over the range of specified operating conditions. For E1 applications (EC inputs = 000 or 001) the threshold is 50%.

The receiver is capable of accurately recovering signals with up to -13.6 dB of attenuation (from 2.4V), corresponding to a received signal level of approximately 500 mV. Maximum line length is 1500 feet of ABAM cable (approximately 6 dB of attenuation). Regardless of received signal level, the peak detectors are held above a minimum level of .3V to provide immunity from impulsive noise.

After processing through the data slicers, the received signal is routed to the data and clock recovery sections, and to the receive monitor. The receive monitor generates a Loss of Signal (LOS) output upon receipt of 175 consecutive zeros (spaces). The receiver monitor loads a digital counter at the RCLK frequency. The count is incremented each time a zero is received, and reset to zero each time a one (mark) is received. Upon receipt of 175 consecutive zeros the LOS pin goes high, and a smooth transition replaces the RCLK output with the MCLK. (If MCLK is not supplied the RCLK output will be replaced with the centered crystal clock.) The LOS pin is reset immediately upon receipt of a one.

Recovered clock signals are supplied to the jitter attenuator and the data latch. The recovered data is passed to the elastic store where it is buffered and synchronized with the dejittered recovered clock (RCLK).

JITTER ATTENUATION

Jitter attenuation of the SSI 78P304A clock and data outputs is provided by a Jitter Attenuation Loop (JAL) and an Elastic Store (ES). An external crystal oscillating at 4 times the bit rate provides clock stabilization. Refer to Table 4 for crystal specifications. The ES is a 32 x 2-bit register. Recovered data is clocked into the ES with the recovered clock signal, and clocked out of the ES with the dejittered clock from the JAL. When the bit count in the ES is within two bits of overflowing or underflowing, the ES adjusts the output clock by 1/8 of a bit period. The ES produces an average delay of 16 bits in the receive path.

OPERATING MODES

The SSI 78P304A transceiver can be controlled through hard-wired pins (Hardware mode) or by a microprocessor through a serial interface (Host mode). The mode of operation is set by the MODE pin logic level. The SSI 78P304A can also be commanded to operate in one of several diagnostic modes.

HOST MODE OPERATION

To allow a host microprocessor to access and control the SSI 78P304A through the serial interface, MODE is set to 1. The serial interface (SDI/SDO) uses a 16-bit word consisting of an 8-bit Command/Address byte and an 8-bit Data byte. Figure 5 shows the serial interface data structure and timing.

The Host mode provides a latched Interrupt output ($\overline{INT}$) which is triggered by a change in the Loss of Signal (LOS) and/or Driver Performance Monitor (DPM) bits. The Interrupt is cleared when the interrupt condition no longer exists, and the host processor enables the respective bit in the serial input data byte. Host mode also allows control of the serial data and receive data output timing. The Clock Edge (CLKE) signal determines when these outputs are valid, relative to the Serial Clock (SCLK) or RCLK as follows:

CLKE	Output	Clock	Valid Edge
LOW	RPOS	RCLK	Rising
	RNEG	RCLK	Rising
	SDO	SCLK	Falling
HIGH	RPOS	RCLK	Falling
	RNEG	RCLK	Falling
	SDO	SCLK	Rising

The SSI 78P304A serial port is addressed by setting bit A4 in the Address/Command byte, corresponding to address 16. The SSI 78P304A contains only a single output data register so no complex chip addressing scheme is required. The register is accessed by causing the Chip Select (CS) input to make a transition from high to low. Bit 1 of the serial Address/Command byte provides Read/Write control when the chip is accessed. A logic 1 indicates a read operation, and a logic 0 indicates a write operation. Table 6 lists serial data output bit combinations for each status. Serial data I/O timing characteristics are shown in Table 6, and Figures 6 and 7.

HARDWARE MODE OPERATION

In Hardware mode the transceiver is accessed and controlled through individual pins. With the exception of the $\overline{INT}$ and CLKE functions, Hardware mode provides all the functions provided in the Host mode. In the Hardware mode RPOS and RNEG outputs are valid on the rising edge of RCLK. To operate in Hardware mode, MODE must be set to 0. Equalizer Control signals (EC1 through EC3) are input on the Interrupt, Serial Data In and Serial Data Out pins. Diagnostic control for Remote Loopback (RLOOP), Local Loopback (LLOOP), and Transmit All Ones (TAOS) modes is provided through the individual pins used to control serial interface timing in the Host mode.

RESET OPERATION

Upon power up, the transceiver is held static until the power supply reaches approximately 3V. Upon crossing this threshold, the device begins a 32 ms reset cycle to calibrate the transmit and receive delay lines and lock the Phase Lock Loop to the receive line. A reference clock is required to calibrate the delay lines. The transmitter reference is provided by TCLK. The crystal oscillator provides the receiver reference. If the 78P304A crystal oscillator is grounded, MCLK is used as the receiver reference clock.

The transceiver can also be reset from the Host or Hardware mode. In Host mode, reset is commanded by simultaneously writing RLOOP and LLOOP to the register. In Hardware mode, reset is commanded by holding RLOOP and LLOOP high simultaneously for 200 ns. Reset is initiated on the falling edge of the reset request. In either mode, reset clears and sets all registers to 0 and centers the oscillator, then calibration begins.

DIAGNOSTIC MODE OPERATION

In Transmit All Ones (TAOS) mode the TPOS and TNEG inputs to the transceiver are ignored. The transceiver transmits a continuous stream of 1's when the TAOS mode is activated. TAOS can be commanded simultaneously with Local Loopback, but is inhibited during Remote Loopback.

In Remote Loopback (RLOOP) mode, the transmit data and clock inputs (TPOS, TNEG and TCLK) are ignored. The RPOS and RNEG outputs are looped back through the transmit circuits and output on TTIP and TRING at the RCLK frequency. Receiver circuits are unaffected by the RLOOP command and continue to output the RPOS, RNEG and RCLK signals received from the twisted-pair line.

In Local Loopback (LLOOP) mode, the receiver circuits are inhibited. The transmit data and clock inputs (TPOS, TNEG and TCLK) are looped back onto the receive data and clock outputs (RPOS, RNEG and RCLK.) The transmitter circuits are unaffected by the LLOOP command. The TPOS and TNEG inputs (or a stream of 1's if the TAOS command is active) will be transmitted normally. When used in this mode with a crystal, the transceiver can be used as a stand-alone jitter attenuator.

POWER REQUIREMENTS

The SSI 78P304A is a low-power CMOS device. It operates from a single +5 V power supply which can be connected externally to both the transmitter and receiver. However, the two inputs must be within ± .3V of each other, and decoupled to their respective grounds separately, as shown in Figure 8. Isolation between the transmit and receive circuits is provided internally.

PIN DESCRIPTION

NAME	TYPE	DESCRIPTION
MCLK	I	Master Clock: A 1.544 or 2.048 MHz clock input used to generate internal clocks. Upon Loss of Signal (LOS), RCLK is derived from MCLK. If MCLK is not applied, this pin should be grounded.
TCLK	I	Transmit Clock: Transmit clock input. TPOS and TNEG are sampled on the falling edge of TCLK.
TPOS	I	Transmit Positive Data: Input for positive pulse to be transmitted on the twisted-pair or coaxial cable.
TNEG	I	Transmit Negative Data: Input for negative pulse to be transmitted on the twisted-pair or coaxial cable.
MODE	I	Mode Select: Setting MODE to logic 1 puts the SSI 78P304A in the Host mode. In the Host mode, the serial interface is used to control the SSI 78Q904A and determine its status. Setting MODE to logic 0 puts the SSI 78P304A in the Hardware (H/W) mode. In the Hardware mode the serial interface is disabled and hard-wired pins are used to control configuration and report status.
RNEG / RPOS	O	Receive Negative/Positive Data: Received data outputs. A signal on RNEG corresponds to receipt of a negative pulse on RTIP and RRING. A signal on RPOS corresponds to receipt of a positive pulse on RTIP and RRING. RNEG and RPOS outputs are Non-Return-to-Zero (NRZ). In the Host mode, CLKE determines the clock edge at which these outputs are stable and valid. In the Hardware mode both outputs are stable and valid on the rising edge of RCLK.
RCLK	O	Recovered Clock: This is the clock recovered from the signal received at RTIP and RRING.

PIN DESCRIPTION (continued)

NAME	TYPE	DESCRIPTION
XTALIN / XTALOUT	I	Crystal Input / Crystal Output: An external crystal operating at four times the bit rate (6.176 MHz for DSX-1, 8.192 MHz for E1 applications with an 18.7 pF load) is required to enable the jitter attenuation function of the SSI 78P304A. These pins may also be used to disable the jitter attenuator by connecting the XTALIN pin to the positive supply through a resistor, and tying the XTALOUT pin to ground.
DPM	O	Driver Performance Monitor: DPM goes to a logic 1 when the transmit monitor loop (MTIP and MRING) does not detect a signal for 63 ±2 clock periods. DPM remains at logic 1 until a signal is detected.
LOS	O	Loss of Signal: LOS goes to a logic 1 when 175 consecutive spaces have been detected. LOS returns to a logic 0 when a mark is received.
TTIP / TTRING	O	Transmit Tip / Transmit Ring: Differential Driver Outputs. These low impedance outputs achieve maximum power savings through a 1:1.15 transformer (T1), or a 1:1 or 1:1.26 transformer (E1) without additional components. To provide higher return loss for E1 systems, resistors may be used in series with a 1:2 transformer (use 15Ω resistors for 120Ω terminations, and 9.3Ω resistors for 75Ω terminations.)
TGND	-	Transmit Ground: Ground return for the transmit drivers power supply TV+.
TV+	I	Transmit Power Supply: +5 VDC power supply input for the transmit drivers. TV+ must not vary from RV+ by more than ±0.3V.
MTIP / MRING	I	Monitor Tip / Monitor RIng: These pins are used to monitor the tip and ring transmit outputs. The transceiver can be connected to monitor its own output or the output of another 78P304A on the board. To prevent false interrupts in the host mode if the monitor is not used, apply a clock signal to one of the monitor pins and tie the other monitor pin to approximately the clock's mid-level voltage. The monitor clock can range from 100kHz to the TCLK frequency.
RTIP / RRING	O	Receive Tip / Receive Ring: The AMI signal received from the line is applied at these pins. A center-tapped, center-grounded, 2:1 step-up transformer is required on these pins. Data and clock from the signal applied at these pins are recovered and output on the RPOS/RNEG, and RCLK pins.
RV+	I	Received Power Supply: +5 VDC power supply for all circuits except the transmit drivers. (Transmit drivers are supplied by TV+.)
RGND	-	Receive Ground: Ground return for power supply RV+.
$\overline{\text{INT}}$	O	Interrupt (Host Mode): This SSI 78P304A Host mode output goes low to flag the host processor when LOS or DPM go active. $\overline{\text{INT}}$ is an open-drain output and should be tied to power supply RV+ through a resistor. $\overline{\text{INT}}$ is reset by clearing the respective register bit (LOS and/or DPM.)
EC1	I	Equalizer Control 1 (H/W Mode): The signal applied at this pin in the SSI 78P304A Hardware mode is used in conjunction with EC2 and EC3 inputs to determine shape and amplitude of AMI output transmit pulses.

PIN DESCRIPTION (continued)

NAME	TYPE	DESCRIPTION
SDI	I	Serial Data In (Host Mode): The serial data input stream is applied to this pin when the SSI 78P304A operates in the Host mode. SDI is sampled on the rising edge of SCLK.
EC2	I	Equalizer Control 2 (H/W Mode): The signal applied at this pin in the SSI 78P304A Hardware mode is used in conjunction with EC1 and EC3 inputs to determine shape and amplitude of AMI output transmit pulses.
SDO	O	Serial Data Out (Host Mode): The serial data from the on-chip register is output on this pin in the SSI 78P304A Host mode. If CLKE is high, SDO is valid on the rising edge of SCLK. If CLKE is low SDO is valid on the falling edge of SCLK. This pin goes to a high-impedance state when the serial port is being written to and when $\overline{CS}$ is high.
EC3	I	Equalizer Control 3 (H/W Mode): The signal applied at this pin in the SSI 78P304A Hardware mode is used in conjunction with EC1 and EC2 inputs to determine shape and amplitude of AMI output transmit pulses.
$\overline{CS}$	I	Chip Select (Host Mode): This input is used to access the serial interface in the SSI 78P304A Host mode. For each read or write operation, $\overline{CS}$ must remain low for the duration of operation.
RLOOP	I	Remote Loopback (H/W Mode): This input controls loopback functions in the SSI 78P304A Hardware mode. Setting RLOOP to a logic 1 enables the Remote Loopback mode. Setting both RLOOP and LLOOP causes a Reset.
SCLK	I	Serial Clock (Host Mode): This clock is used in the SSI 78P304A Host mode to write data to or read data from the serial interface registers.
LLOOP	I	Local Loopback (H/W Mode): This input controls loopback functions in the SSI 78P304A Hardware mode. Setting LLOOP to a logic 1 enables the Local Loopback Mode.
CLKE	I	Clock Edge (Host Mode): Setting CLKE to logic 1 causes RPOS and RNEG to be valid on the falling edge of RCLK, and SDO to be valid on the rising edge of SCLK. When CLKE is a logic 0, RPOS and RNEG are valid on the rising edge of RCLK, and SDO is valid on the falling edge of SCLK.
TAOS	I	Transmit All Ones (H/W Mode): When set to a logic 1, TAOS causes the SSI 78P304A (Hardware mode) to transmit a continuous stream of marks at the TCLK frequency. Activating TAOS causes TPOS and TNEG inputs to be ignored. TAOS is inhibited during Remote Loopback.

ELECTRICAL SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Operation above maximum ratings may damage the device. Normal operation not guaranteed at these extremes.

PARAMETER		RATING	UNIT
DC supply (referenced to GND)	RV+, TV+	-0 to 6.0	V
Input voltage, any pin (see note 1)	V_{IN}	RGND -0.3 to RV+ + 0.3	V
Input current, any pin (see note 2)	I_{IN}	-10 to +10	mA
Ambient operating temperature	T_A	-40 to 85	°C
Storage temperature	T_{STG}	-65 to 150	°C

[1] Excluding RTIP and RRING which must stay within -6V to RV+ + 0.3V.
[2] Transient currents of up to 100 mA will not cause SCR latch-up. TTIP, TRING, TV+ and TGND can withstand a continuous current of 100 mA.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	MIN	NOM	MAX	UNIT
DC supply (see note 1)	RV+, TV+	4.75	5.0	5.25	V
Ambient Operating Temperature	T_A	-40	25	85	°C
Total power dissipation P_D (see note 2)	100% ones density & max line length @ 5.25V	-	-	400	mW

[1] TV+ must not exceed RV+ by more than ±0.3 V.
[2] Power dissipation while driving 25Ω load over operating temperature range. Includes device and load. Digital input levels are within 10% of the supply rails and digital outputs are driving a 50 pF capacitive load.

DIGITAL CHARACTERISTICS (T_A = -40° to 85 °C, V+ = 5.0V ±5%, GND = 0V)

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
High level input voltage V_{IH} (see notes 1 & 2)		2.0	-	-	V
Low level input voltage V_{IL} (see notes 1 & 2)		-	-	0.8	V
High level output voltage V_{OH} (see notes 1 & 2)	I_{OUT} = -400 µA	2.4	-	-	V
Low level output voltage V_{OL} (see notes 1 & 2)	I_{OUT} = 1.6 mA	-	-	0.4	V
Input leakage current I_{LL} (see note 3)		0	-	±10	µA
Three-state leakage current (see note 2) I_{3L}		0	-	±10	µA

[1] Functionality of pins 23 and 25 depends on mode. See Host / Hardware Mode descriptions.
[2] Output drivers will output CMOS logic levels into CMOS loads.
[3] Except MTIP and MRING I_{LL} = ± 50 µA.

ELECTRICAL SPECIFICATIONS (continued)

ANALOG SPECIFICATIONS (T_A = -40 to 85 °C, V+ = 5.0V ±5%, GND = 0V)

PARAMETER		TEST CONDITIONS	MIN	NOM	MAX	UNIT
AMI Output	DSX-1	measured at the DSX	2.4	3.0	3.6	V
Pulse Amplitudes	CEPT	measured at line side	2.7	3.0	3.3	V
Load presented to transmitter output			-	75	-	Ω
Jitter added by	10 Hz - 8 kHz		-	-	0.01	UI
the transmitter	8 kHz - 40 kHz		-	-	0.025	UI
(see note 1)	10 Hz - 40 kHz		-	-	0.025	UI
	Broad Band		-	-	0.05	UI
Sensitivity below DSX (0 dB = 2.4V)			13.6	-	-	dB
			500	-	-	mV
Loss of Signal threshold			-	0.3	-	V
Data decision	DSX-1		63	70	77	%peak
threshold	CEPT		43	50	57	%peak
Allowable consecutive zeros before LOS			160	175	190	-
Input jitter tolerance	10 kHz - 100 kHz		0.4	-	-	UI
Jitter attenuation curve corner frequency (see note 2)			-	6	-	Hz
Minimum Return Loss (see notes 3 & 4)			Transmit Min	Transmit Typ	Receive Min	Receive Typ	
51 kHz - 102 kHz			20	28	20	30	dB
102 kHz - 2.048 MHz			20	28	20	30	dB
2.048 MHz - 3.072 MHz			20	24	20	25	dB

[1] Input signal to TCLK is jitter-free.
[2] Circuit attenuates jitter at 20 dB/decade above the corner frequency.
[3] In accordance with CCITT G.703/RC6367A return loss specifications (CEPT), when wired as shown in Figure 9.
[4] Guaranteed by design.

TABLE 1: Equalizer Control Inputs for Transmitter

EC3	EC2	EC1	Line Length[1]	Cable Loss[2]	Application	Frequency
0	1	1	0 - 133 ft ABAM	0.6 dB	DSX-1	1.544 MHz
1	0	0	133 - 266 ft ABAM	1.2 dB		
1	0	1	266 - 399 ft ABAM	1.8 dB		
1	1	0	399 - 533 ft ABAM	2.4 dB		
1	1	1	533 - 655 ft ABAM	3.0 dB		
0	0	0	CCITT Recommendation G.703		E1 - Coax (75 Ω) E1 - Twisted-pair (120 Ω)	2.048 MHz
0	0	1				
0	1	0	FCC Part 68, Option A		CSU	1.544 MHz
0	1	1	ECSA T1C1.2			

[1] Line length from transceiver to DSX-1 cross-connect point.
[2] Maximum cable loss at 772 kHz.

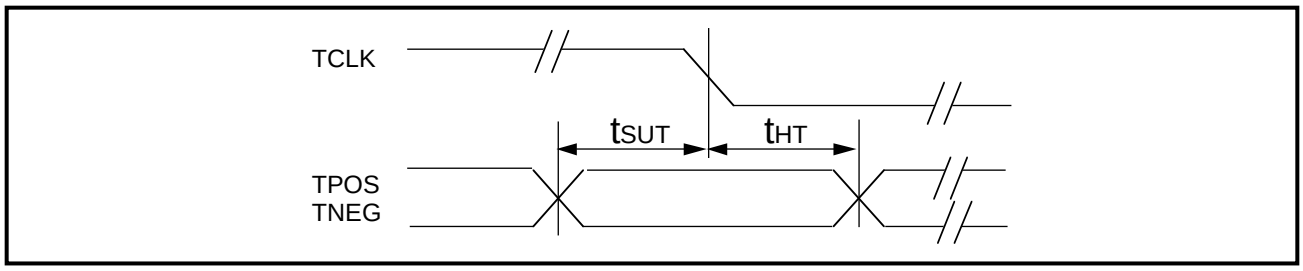


Figure 2: SSI 78P304A Transmit Clock Timing

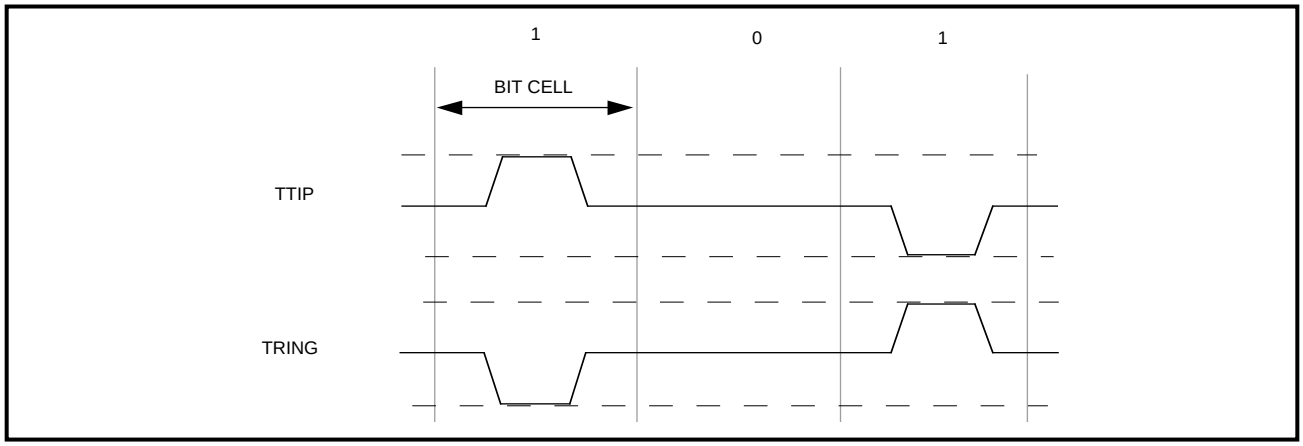


Figure 3: 50% AMI Coding

TABLE 2: SSI 78P304A Master Clock and Transmit Timing Characteristics (See Figure 2)

Parameter		Sym	Min	Typ[1]	Max	Units
Master clock frequency	DSX-1	MCLK	-	1.544	-	MHz
	E1	MCLK	-	2.048	-	MHz
Master clock tolerance		MCLKt	-	±100	-	ppm
Master clock duty cycle		MCLKd	40	-	60	%
Crystal frequency	DSX-1	fc	-	6.176	-	MHz
	E1	fc	-	8.192	-	MHz
Transmit clock frequency	DSX-1	TCLK	-	1.544	-	MHz
	E1	TCLK	-	2.048	-	MHz
Transmit clock tolerance		TCLKt	-	-	±50	ppm
Transmit clock duty cycle		TCLKd	40	-	60	%
TPOS/TNEG to TCLK setup time		t_{SUT}	25	-	-	ns
TCLK to TPOS/TNEG Hold time		t_{HT}	25	-	-	ns

[1] Typical figures are at 25°C and are for design aid only; not guaranteed and not subject to production testing.

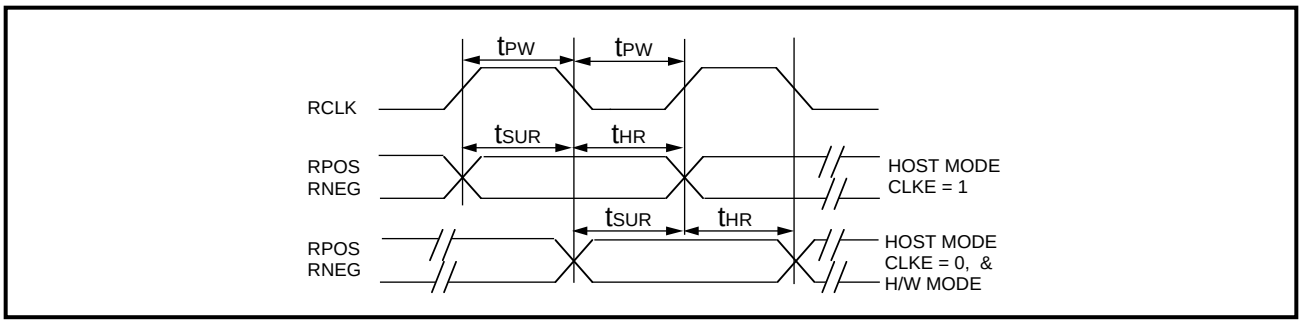


FIGURE 4: SSI 78P304A Receive Clock Timing

TABLE 3: SSI 78P304A Receive Timing Characteristics (See Figure 4)

Parameter		Sym	Min	Typ[1]	Max	Units
Receive clock duty cycle		RCLKd	40	-	60	%
Receive clock pulse width	DSX-1	t_{PW}	-	324	-	ns
	CEPT	t_{PW}	-	244	-	ns
RPOS / RNEG to RCLK	DSX-1	t_{SUR}	-	274	-	ns
rising setup time	CEPT	t_{SUR}	-	194	-	ns
RCLK rising to RPOS /	DSX-1	t_{HR}	-	274	-	ns
RNEG hold time	CEPT	tHR	-	194	-	ns

[1] Typical figures are at 25°C and are for design aid only; not guaranteed and not subject to production testing.

TABLE 4: SSI 78P304A Crystal Specifications (External)

Parameter	T1	E1
Frequency	6.176 MHz	8.192 MHz
Frequency Stability	±20 ppm @ 25° C ±25 ppm from -40° C to + 85° C (Ref 25° C reading)	±20 ppm @ 25° C ±25 ppm from -40° C to + 85° C (Ref 25° C reading)
Pullability	CL = 11 pF to 18.7 pF, +ΔF = 175 to 195 ppm CL = 18.7 pF to 34 pF, -ΔF = 175 to 195 ppm	CL = 11 pF to 18.7 pF, +ΔF = 95 to 115 ppm CL = 18.7 pF to 34 pF, -ΔF = 95 to 115 ppm
Effective series resistance	40Ω Maximum	30Ω Maximum
Crystal cut	AT	AT
Resonance	Parallel	Parallel
Maximum drive level	2.0 mW	2.0 mW
Mode of operation	Fundamental	Fundamental
Crystal holder	HC49 (R3W), C_O = 7 pF maximum C_M = 17 pF typical	HC49 (R3W), C_O = 7 pF maximum C_M = 17 pF typical

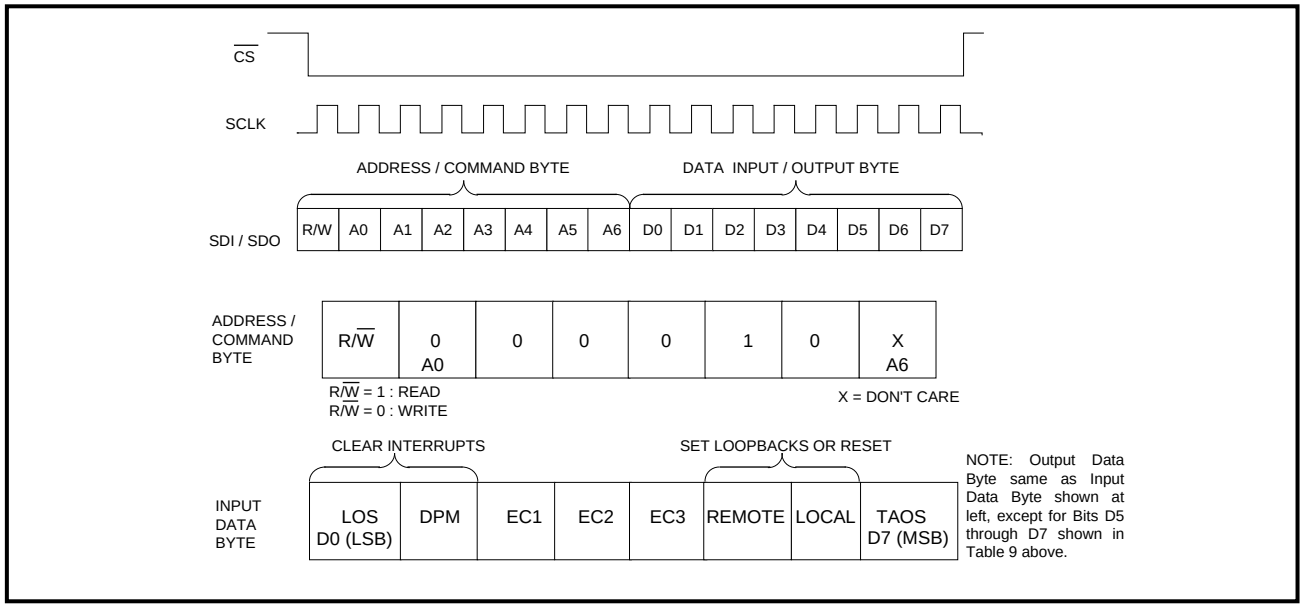


FIGURE 5: SSI 78P304A Serial Interface Data Structure

TABLE 5: SSI 78P304A Serial Data Output Bits (See Figure 5)

Bit D5	Bit D6	Bit D7	Status
0	0	0	Reset has occurred, or no program input.
0	0	1	TAOS active
0	1	0	Local Loopback active
0	1	1	TAOS and Local Loopback active
1	0	0	Remote Loopback active
1	0	1	DPM has changed state since last Clear DPM occurred
1	1	0	LOS has changed state since last Clear LOS occurred
1	1	1	LOS and DPM have both changed state since last Clear DPM and Clear LOS occurred

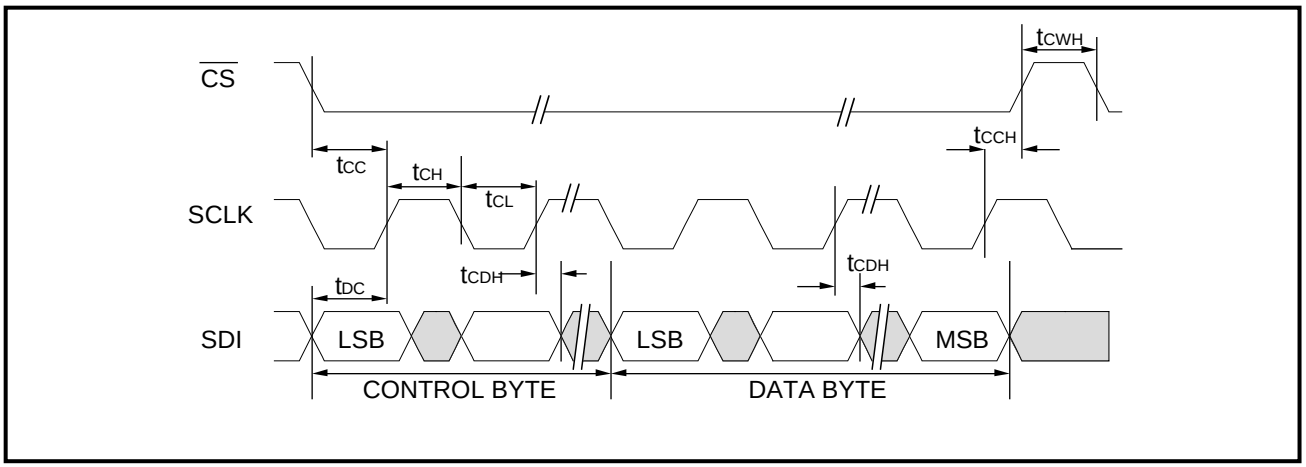


FIGURE 6: SSI 78P304A Serial Data Input Timing Diagram

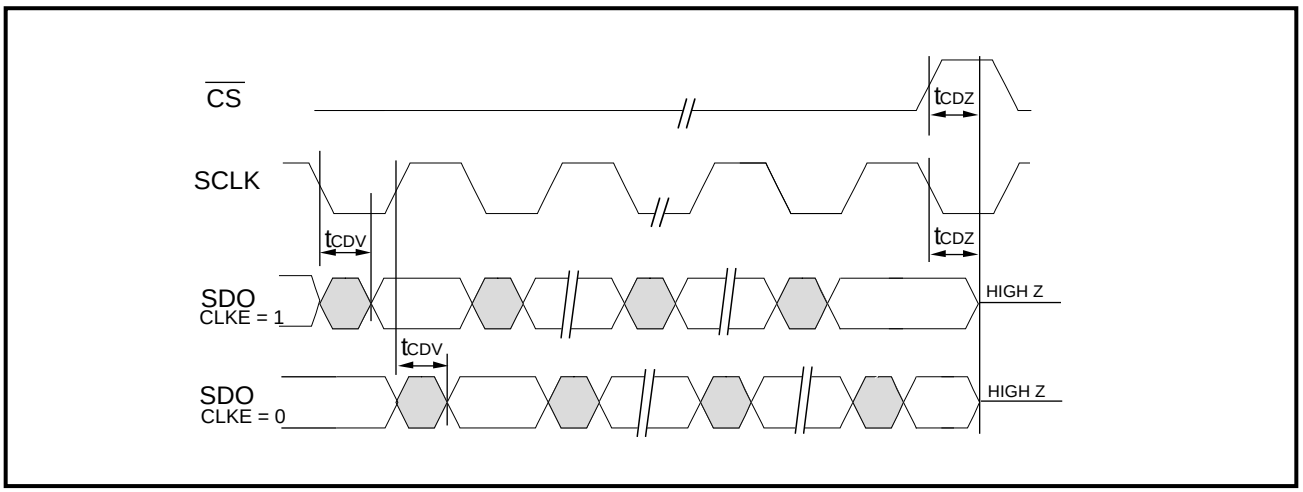


Figure 7: SSI 78P304A Serial Data Output Timing Diagram

TABLE 6: SSI 78P304A Serial I/O Timing Characteristics (See Figures 6 and 7)

Parameter	Sym	Min	Typ[1]	Max	Units	Test Conditions
Rise/Fall time - any digital output	t_{RF}	-	-	100	ns	Load 1.6 mA, 50pF
SDI to SCLK setup time	t_{DC}	50	-	-	ns	
SCLK to SDI hold time	t_{CDH}	50	-	-	ns	
SCLK low time	t_{CL}	240	-	-	ns	
SCLK high time	t_{CH}	240	-	-	ns	
SCLK rise and fall time	t_R , t_F	-	-	50	ns	
$\overline{CS}$ to SCLK setup time	t_{CC}	50	-	-	ns	
SCLK to $\overline{CS}$ hold time	t_{CCH}	50	-	-	ns	
$\overline{CS}$ inactive time	t_{CWH}	250	-	-	ns	
SCLK to SDO valid	t_{CDV}	-	-	200	ns	
SCLK falling edge or $\overline{CS}$ rising edge to SDO high Z	t_{CDZ}	-	100	-	ns	

[1] Typical figures are at 25°C and are for design aid only; not guaranteed and not subject to production testing.

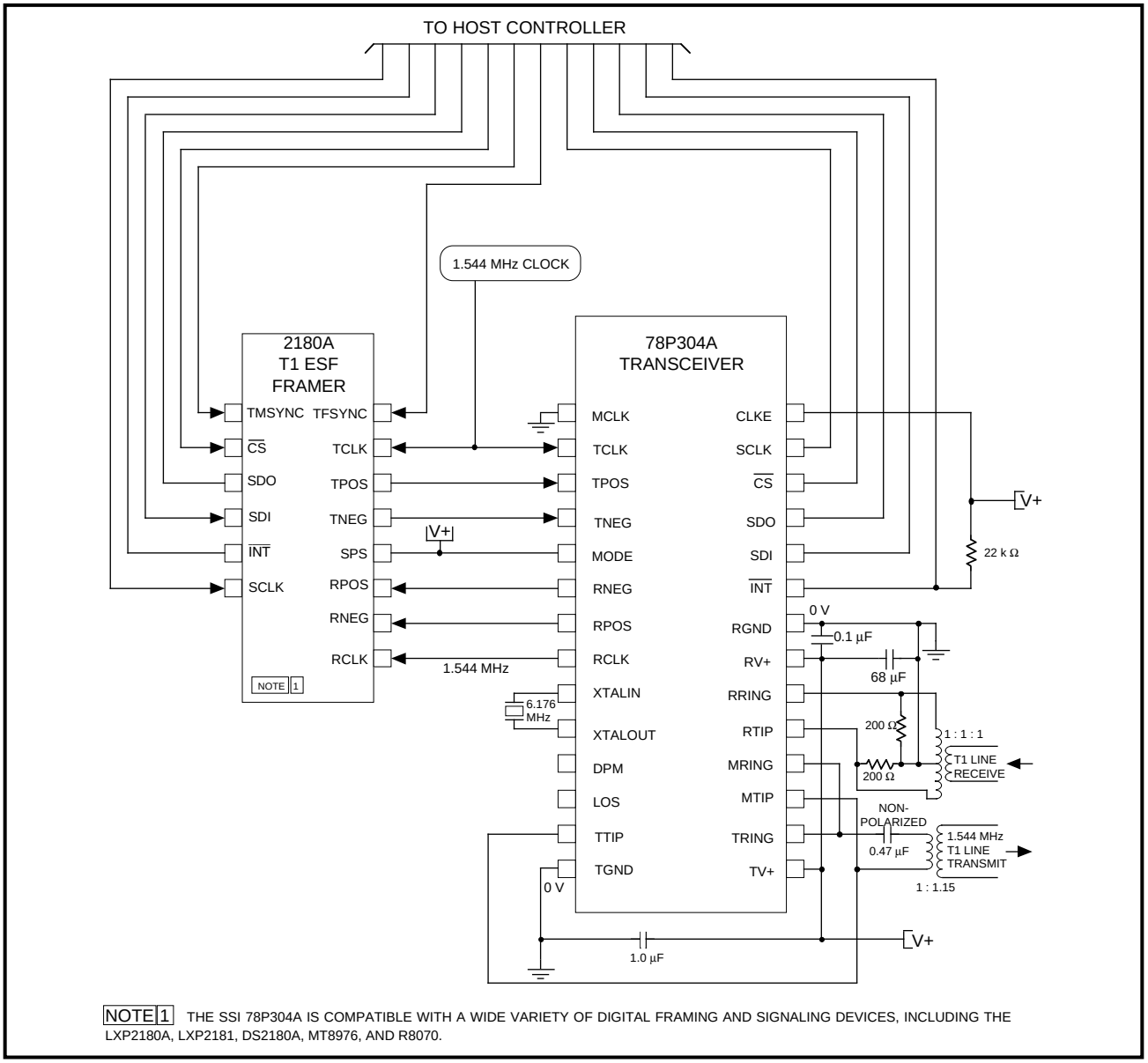
APPLICATION INFORMATION

1.544 MHz T1 INTERFACE APPLICATIONS

Figure 8 is a typical 1.544 MHz T1 application. The SSI 78P304A is shown in the Host mode with the 2180A T1/ESF Framer providing the digital interface with the host controller. Both devices are controlled through the serial interface. The power supply inputs are tied to a common bus with appropriate decoupling capacitors installed (1.0 µF on the transmit side, 68 µF and 0.1 µF on the receive side.)

TABLE 7: E1/CEPT Output Combinations

EC	75Ω Coax	120Ω TWP
0 0 1	1:1, Rt = 10Ω	1:1, Rt = 0Ω
0 0 1	1:2, Rt = 14.3Ω	1:2, Rt = 15Ω
0 0 0	1:1, Rt = 0Ω	1:1.26, Rt = 0Ω
0 0 0	1:2, Rt = 9.37Ω	1:2, Rt = 8.7Ω



NOTE 1 THE SSI 78P304A IS COMPATIBLE WITH A WIDE VARIETY OF DIGITAL FRAMING AND SIGNALING DEVICES, INCLUDING THE LXP2180A, LXP2181, DS2180A, MT8976, AND R8070.

FIGURE 8: Typical SSI 78P304A 1.544 MHz T1 Application (Host Mode)

2.048 MHZ E1/CEPT INTERFACE APPLICATIONS

Figure 9 is a 2.048 MHz E1/CEPT coax application using EC code 000 and 15Ω Rt resistors in line with the transmit transformer to provide high return loss. When high return loss is not a critical factor, a 1:1 or 1:1.26 transformer without in-line resistors provides maximum power savings. Table 7 lists transformer ratios and Rt values with associated 2.048 MHz EC codes for both 75Ω coax and 120Ω TWP. The SSI 78P304A is shown in Hardware mode with the 2181A E1/CRC4 Framer. The hard-wired control lines for TAOS, LLOOP and RLOOP are individually controllable, and the LLOOP and RLOOP lines are also tied to a single control for the Reset function. As in the T1 application Figure 8, this configuration is illustrated with a crystal in place to enable the SSI 78P304A Jitter Attenuation Loop, and a single power supply bus.

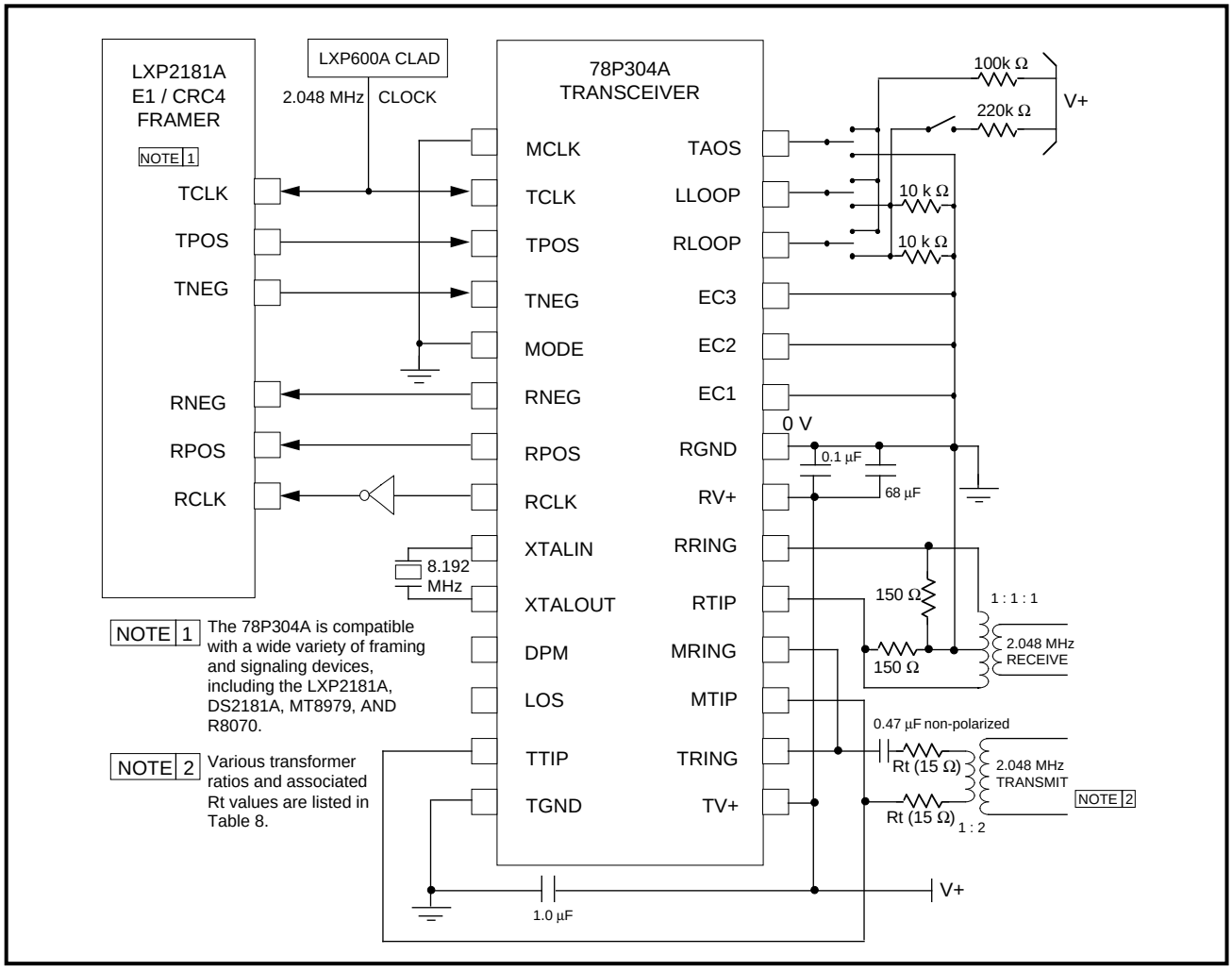
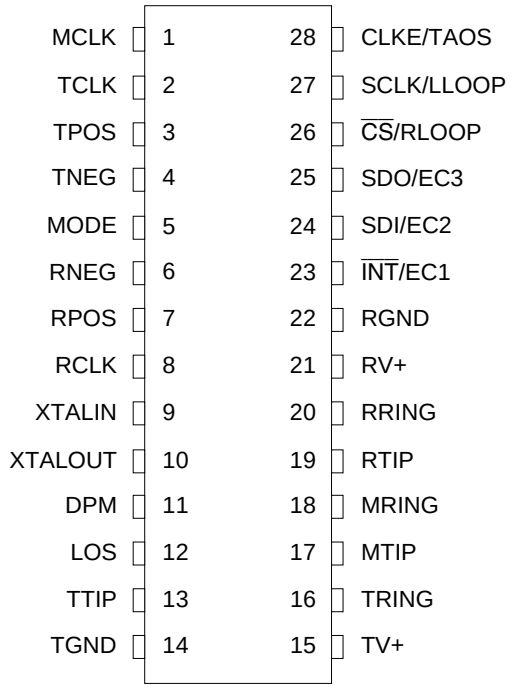


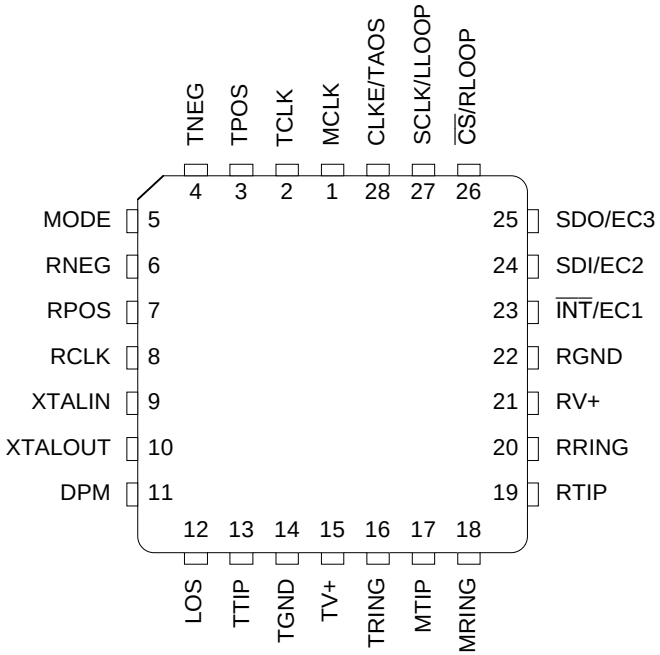
FIGURE 9: SSI 78P304A 2.048 MHz E1 Application (Hardware Mode)

PACKAGE PIN DESIGNATIONS
(Top View)

CAUTION: Use handling procedures necessary for a static sensitive component.



28-Pin DIP



28-Pin PLCC

ORDERING INFORMATION

PART DESCRIPTION	ORDER NO.	PKG. MARK
SSI 78P304A 28-Pin DIP	78P304A-IP	78P304A-IP
SSI 78P304A 28-Pin PLCC	78P304A-IH	78P304A-IH

Silicon Systems, Inc. 14351 Myford Road, Tustin, CA 92680-7022, (714) 573-6000, FAX (714) 573-6914

SSI 78P7200
DS-3/E3/STS-1 Line Interface with Receive Equalizer

January 1996

DESCRIPTION

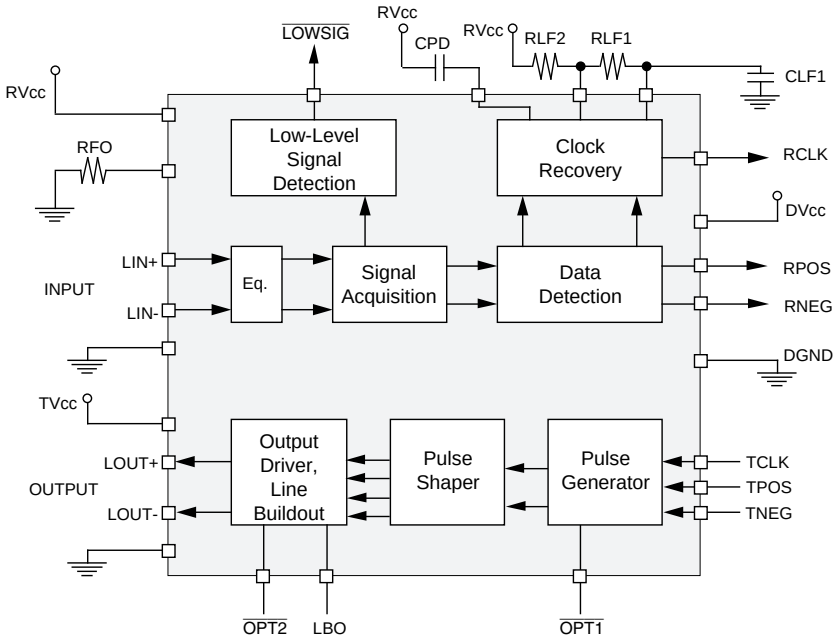
The SSI 78P7200 is a line interface transceiver IC intended for STS-1 (51.84 Mbit/s), DS-3 (44.736 Mbit/s) and E3 (34.368 Mbit/s) applications. The receiver has a very wide dynamic range and is designed to accept HDB3 or B3ZS-encoded Alternate-Mark Inversion (AMI) inputs; it provides CMOS logic level clock, positive data, negative data and low-level signal detector outputs. An on-chip equalizer improves the intersymbol interference tolerance on the receive path. The transmitter converts CMOS logic level clock, positive data and negative data input signals into AMI pulses of the appropriate shape for transmission. A line buildout (LBO) equalizer may be selected to shape the outgoing pulses for shorter line lengths. The SSI 78P7200 requires a single 5 volt supply and is available in a surface mount package.

The 78P7200 works in either rate of STS-1, DS-3 or E3 by simple external components modification.

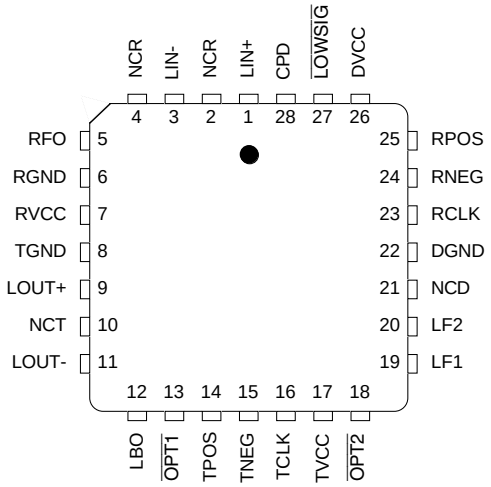
FEATURES

- **Single chip transmit and receive interface for STS-1 (51.84 Mbit/s), E3 (34.368 Mbit/s) or DS-3 (44.736 Mbit/s) applications**
- **On-chip Receive Equalizer**
- **Unique clock recovery circuit, requires no crystals, tuned components or external clock**
- **Selectable transmit line buildout (LBO) to accommodate shorter line lengths**
- **Compliant with ANSI T1.102-1993, Bellcore TR-NWT-000499 and GR-253-CORE, ITU-T G.703 and G.823_1991**
- **Low-level input signal indication**
- **Available in a 28 PLCC surface mount package**
- **-40°C to +85°C operating range**
- **Pin-compatible replacement for SSI 78P236, 78P2361 and 78P2362**

BLOCK DIAGRAM



PIN DIAGRAM



28-Pin PLCC

CAUTION: Use handling procedures necessary for a static sensitive component.

FUNCTIONAL DESCRIPTION

The SSI 78P7200 is a single chip line interface IC designed to work with a 51.84 Mbit/s STS-1, 44.736 Mbit/s DS-3 or 34.368 Mbit/s E3 signal. The receiver recovers clock, positive data and negative data from an Alternate Mark Inversion (AMI) signal. The input signal should be B3ZS or HDB3 coded.

The transmitter accepts CMOS level logical clock, positive data and negative data and converts them to the AMI signal to drive a 75Ω coaxial cable. Programmable internal Line Buildout (LBO) circuitry eliminates the need for external LBO networks. When the option pins are properly selected, the shape of the transmitted signal through any cable length of 0 to 450 feet complies with the published templates of ANSI T1.102, ITU-T G.703, Bellcore TR-NWT-000499 and GR-253-CORE. The SSI 78P7200 is designed to work with a B3ZS or HDB3 coded signal. The B3ZS or HDB3 encoding and decoding functions are normally included in the framer ICs or can easily be implemented in a PAL.

RECEIVER

The receiver input is normally transformer-coupled to the AMI signal. The inputs to the IC are internally referenced to RVCC. Since the input impedance of the SSI 78P7200 is high, the AMI line must be terminated in 75Ω. The input signal to the SSI 78P7200 must be limited to a maximum of three consecutive zeros using a coding scheme such as B3ZS or HDB3.

The AMI signal first enters a fixed equalizer which is designed to overcome the intersymbol interference caused by long cable lengths and crosstalk. This fixed equalizer is optimized for DS-3 application and its effect should be compensated by an external filter circuit similar to Fig. 1, for all square shaped signals such as DS3-high or 34 Mbit/s E3. The signal is then input to a variable gain differential amplifier whose output is maintained at a constant voltage level regardless of the input voltage level. The gain of this amplifier is adjusted by detecting the peak of the signal and comparing it to a fixed reference.

The output of the variable gain amplifier is compared to a threshold value which is a fixed percentage of the signal peak. In this way, even though the input signal amplitude may fall below the minimum value that can be regulated by the variable gain circuit, the proper detection threshold is maintained.

Outputs of the data comparators are connected to the clock recovery circuits. The clock recovery system employs a unique phase locked loop which has an auxiliary frequency-sensitive acquisition loop which is active only when cycle-slipping occurs between the received signal rate and the internal oscillator.

This system permits the loop to independently lock to the frequency and phase of the incoming data stream without the need for high precision and/or adjustable oscillator or tuned circuits.

The response characteristic for the phase locked loop is established by external filter components, RLF1, RLF2 and CLF1. The values of these components are specified such that the bandwidth of the phase locked loop is greater than 200 kHz.

The jitter tolerance of the SSI 78P7200 exceeds the requirements of TR-NWT-000499 for Category II equipment for DS-3 rate and exceeds the requirements of ITU-T G.823 for E3 rate. The jitter transfer function is maximally flat so the IC doesn't add any significant jitter to the system.

Figure 2 shows the recovered clock (RCLK), positive data (RPOS) and negative data (RNEG) signals timing. The data is valid on the rising edge of the clock. The minimum setup and hold times allow easy interface to framer circuits. These signals are CMOS-level outputs.

Should the input signal fall below a minimum value, the $\overline{\text{LOWSIG}}$ pin goes active low. A time delay is provided before this output is active so that transient interruptions do not cause false indications. This signal should be used as one of many indications to the cable disconnect; the framer device should count the number of zeros to declare the loss of signal. The RPOS and RNEG signals generate random data following a silence period. The framer device should ignore RPOS and RNEG data if the $\overline{\text{LOWSIG}}$ pin is active low.

TRANSMITTER

The transmitter accepts unipolar CMOS level logical clock (TCLK), positive data (TPOS) and negative data (TNEG) signals and generates high current drive pulses on the LOUT+ and LOUT- pins. When properly connected to a center tapped transformer, an AMI pulse is generated which can drive a 75Ω coaxial cable.

Figure 3 shows the timing for the transmitter logic signals. The output pulse width is internally set and is not sensitive to input clock (TCLK) pulse width.

When a recommended transformer is used and option pins are properly set, the transmitted pulse shape at the end of a 75Ω terminated cable of 0 to 450 feet will fit the template for DSX3 pulse published in ANSI T1.102-1993, Bellcore TR-NWT-000499 documents.

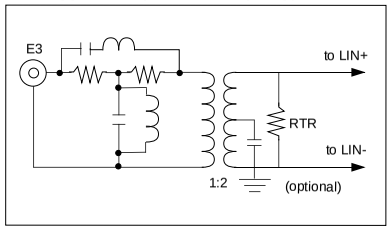
For 51.84 Mbit/s STS-1 application the transmitted pulse for a short cable meets the requirements of Bellcore GR-253-CORE. For 34 Mbit/s E3 application, the transmitted pulse for a short cable meets the requirements of ITU-T G.703 when both LBO and $\overline{\text{OPT1}}$ pins are set LOW.

The SSI 78P7200 incorporates a selectable Line Buildout (LBO) pulse shaper in the transmitter path. For STS-1 and DS-3 applications, the LBO pin should be set HIGH if the cable is shorter than 225 feet and set LOW for longer cable lengths. For E3 application, LBO pin should be set LOW regardless of cable length.

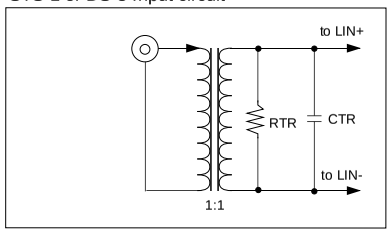
The $\overline{\text{OPT1}}$ pin is set HIGH for normal DS-3 and STS-1 operation. Setting the $\overline{\text{OPT1}}$ pin to LOW increases the transmitter power. The $\overline{\text{OPT1}}$ pin should be set LOW for E3 applications.

The $\overline{\text{OPT2}}$ pin should be set HIGH for normal operation. Setting the $\overline{\text{OPT2}}$ pin to LOW disables the transmitter drivers and reduces the power consumption of the circuit by approximately 125 mW.

E3 Suggested Input circuit Topology

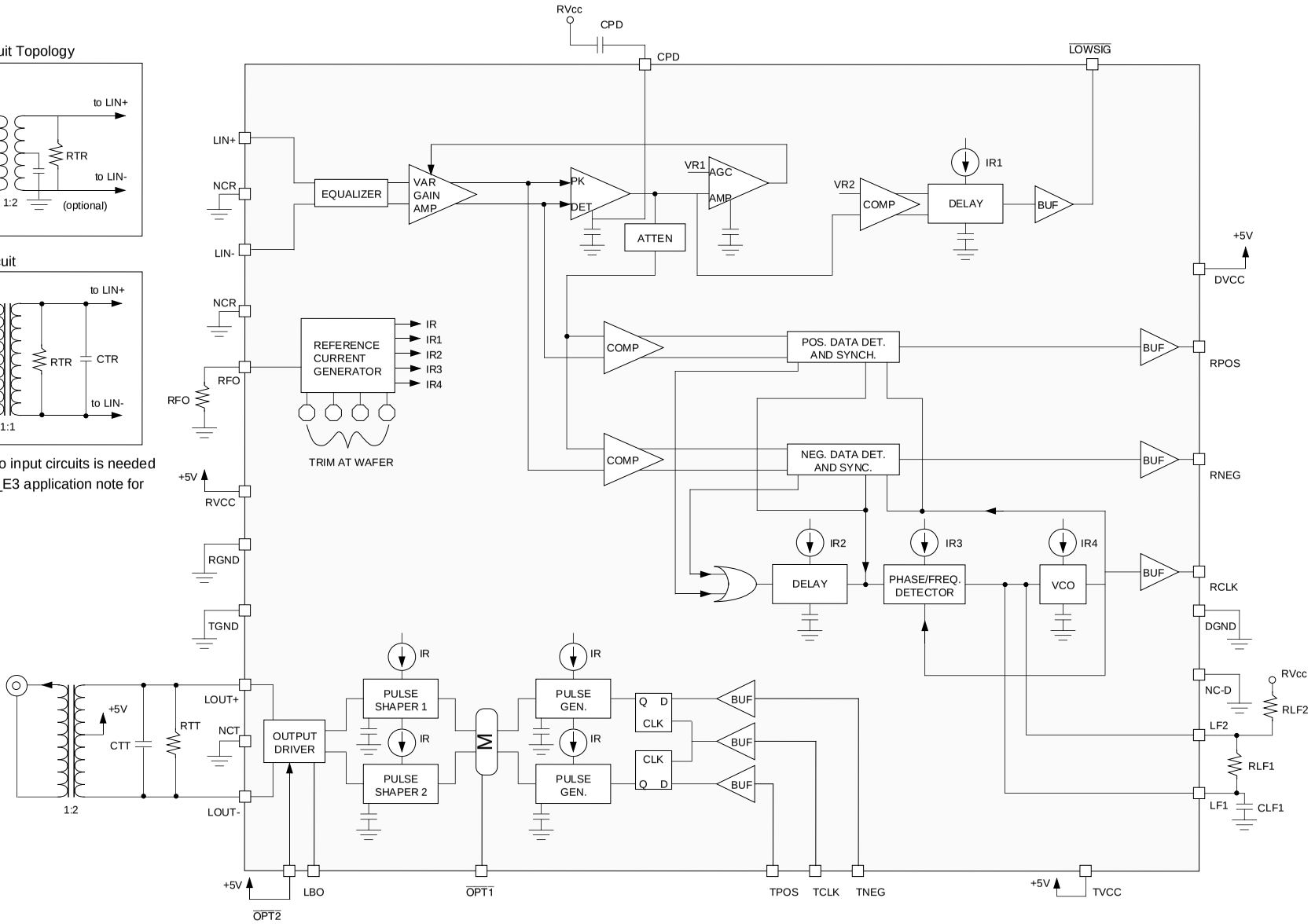


STS-1 or DS-3 Input circuit



Note: Only one of the two input circuits is needed

Note: Refer to 78P7200_E3 application note for details of E3 input circuit



Note: NC pins should be tied to the ground pin indicated by the trailing letter.

FIGURE 1: Functional Diagram

PIN DESCRIPTION

RECEIVER

NAME	TYPE	DESCRIPTION
LIN+, LIN-	I	Differential inputs, transformer-coupled from line.
RPOS	O	Unipolar receiver output, active as result of positive pulse at inputs.
RNEG	O	Unipolar receiver output, active as result of negative pulse at inputs.
RCLK	O	Clock pulses recovered from line data.
$\overline{\text{LOWSIG}}$	O	Low signal logic output indicating that input signal is less than threshold value.

TRANSMITTER

TPOS	I	Unipolar transmitter data input, active high.
TNEG	I	Unipolar transmitter data input, active high.
TCLK	I	Transmitter clock input, active high.
LOUT+	O	Output to transformer for positive data pulses.
LOUT-	O	Output to transformer for negative data pulses.
LBO	I	Transmitter line buildout control. Set low for all E3 or for DS-3/STS-1 cable of 225' or longer. Set high for short DS-3/ STS-1 cable.
$\overline{\text{OPT1}}$	I	Transmit option 1. Selects faster output pulse transition time and higher amplitude when low. Set high for normal DS-3/STS-1 and set low for E3.
$\overline{\text{OPT2}}$	I	Transmit option 2. Disables output driver and reduces output bias current when low. Set high for normal transmit operation.

EXTERNAL COMPONENT CONNECTION

RFO	I	Resistor connected to RGND to provide basic center frequency of receiver phase locked loop oscillator.
LF1, LF2	-	Resistor-capacitor loop filter network to establish bandwidth of phase locked loop.
CPD	-	Capacitor to RVcc that is connected to peak detector node to reduce signal-dependent ripple on that node.

POWER

TVcc	-	5V power supply for transmit circuits.
RVcc	-	5V power supply for receive circuits.
DVcc	-	5V power supply for receive logic circuits.
TGND	-	Ground return for transmit circuits.
RGND	-	Ground return for receive circuits.
DGND	-	Ground return for receive logic circuits.
NCR	-	No connect, Tie to Receiver Ground (RGND).
NCT	-	No connect, Tie to Transmitter Ground (TGND).
NCD	-	No connect, Tie to Digital Ground.

ELECTRICAL SPECIFICATIONS

(TA = -40°C to 85°C, Vcc = 5V ±5%, unless otherwise noted.) Currents flowing into the chip are positive. Current maximums are currents with the largest absolute value. Operation above absolute maximum ratings may permanently damage the device.

ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING
Positive 5V supply: TVcc, RVcc, DVcc	6V
Storage Temperature	-65 to 150°C
Soldering Temperature (10 sec.)	260 °C
Ambient Operating Temperature, TA	-40 to +85°C
Pin Ratings: LOUT+, LOUT-	Vcc -2 to Vcc +2V
LIN+, LIN-, TPOS, TNEG, TCLK, $\overline{\text{LBO}}$, RFO, LF2, LF1, $\overline{\text{OPT1}}$, $\overline{\text{OPT2}}$ Pins	-0.3 to Vcc +0.3V
RPOS, RNEG, RCLK, $\overline{\text{LOWSIG}}$ Pins	-0.3 to Vcc +0.3V or +12 mA

SUPPLY CURRENTS AND POWER

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNIT
Supply Current	ICC	Outputs unloaded, normal operation, transmit and receive all 1's pattern		155	190	mA
Power Dissipation	P	Outputs unloaded, TA = 85°C			0.93	W

EXTERNAL COMPONENTS (Common to STS-1/DS3/E3, nominal value)

Loop filter resistor	RLF1	1% tolerance		6.04		kΩ
Loop filter resistor	RLF2	1%		100		kΩ
Loop filter capacitor	CLF1	5%		0.22		µF
Peak detector capacitor	CPD	10%		0.022		µF

EXTERNAL COMPONENTS (Dependent on speed, nominal Value)			**STS-1**	**DS-3**	**E3**	
Loop center frequency resistor	RFO	1% tolerance	4.53	5.23	6.81	kΩ
Transmit termination capacitor	CTT	5% (Note 1)	10	10	3	pF
Transmit termination resistor	RTT	1%	301	301	604	Ω
Receive termination resistor	RTR	1%	75	75	Note 2	Ω
Receive termination capacitor	CTR	5%	5	5		pF
Receive Transformer Turns Ratio	T1	3%	1:1	1:1	Note 2	

Note 1: C_{TT} value depends on the PC board design. Nominal values are selected for SSI 78P7200 Demo Board.

Note 2: Refer to 78P7200_E3 application note for details.

DIGITAL INPUTS AND OUTPUTS

(CMOS-compatible pins: $\overline{\text{LOWSIG}}$, RPOS, RNEG, RCLK, TPOS, TNEG, TCLK, LBO, $\overline{\text{OPT1}}$.) Currents flowing into the chip are positive. Current maximums are currents with the largest absolute value.

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNIT
Input low voltage	VIL		-0.3		1.5	V
Input high voltage	VIH		3.5		Vcc +0.3	V
Input low current	IIL	VIL = 1.5V	-5		5	µA
Input high current	IIH	VIH = 3.5V	-5		5	µA
Output low voltage	VOL	IOL = 0.1 mA			0.4	V
Output high voltage	VOH	IOH = -0.1 mA	4			V

$\overline{\text{OPT2}}$ CHARACTERISTICS

Input low voltage	VIL	IIL = 0.4 mA			0.5	V
Input high voltage	VIH		2			V

RECEIVER

All of the measurements for the receiver are made with the following conditions unless otherwise stated:

1. The input signal is transformer coupled as shown in Figure 1.
2. RFO = 5.23 kΩ for DS-3, 6.81 kΩ for E3 and 4.53 kΩ for STS-1.

Input signal voltage	VIN	Input AC-Coupled CPD = 0.022 µF	±0.045		±1.2	V
		CPD not used	±0.090		±1.2	V
Input Resistance	RIN	Input at device's common mode voltage	15	20	30	kΩ
Receive data detection threshold	VDTH	Relative to peak amplitude for 22.37/17.18/25.92 MHz sinusoidal input		50		%
Receive data low signal threshold	VLOW		±20		±50	mV
Receive data low signal delay	TLOW	CPD = 0.022 µF		500		µs
		CPD not used VIN(max) = ±250 mV	0.5		3	µs
Receive clock period	TRCF	DS-3		22.35		ns
		STS-1		19.29		ns
		E3		29.1		ns

RECEIVER (continued)

PARAMETER	CONDITIONS		MIN	NOM	MAX	UNIT
Receive clock pulse width TRC		DS-3		12.24		ns
		STS-1		9.65		ns
		E3		14.55		ns
Receive clock positive transition time TRCPT	C_L = 15 pF			4.5	6	ns
Receive clock negative transition time TRCNT	C_L = 15 pF			4.5	6	ns
Positive or negative receive data pulse width TRDP/ TRDN		DS-3		22.35		ns
		STS-1		19.29		ns
		E3		29.1		ns
Receive data set-up time TRDPS/ TRDNS		DS-3	5	11.18	13.7	ns
		STS-1		9.65		ns
		E3	5	14.55		ns
Receive data hold time TRDPH/ TRDNH		DS-3	5	11.18	13.7	ns
		STS-1		9.65		ns
		E3	5	14.55		ns
Receive input jitter tolerance high frequency (Note 1)	60 - 300 kHz VIN (min) = ±45 mV	DS-3 STS-1	0.3			UIPP
	10 - 800 kHz VIN (min) = ±45 mV	E3	0.15			UIPP
	10 - 800 kHz VIN (min) = ±90 mV	E3	0.20			UIPP
Receive input jitter tolerance low frequency (Note 1)	10 Hz to 2.3 kHz	STS-1, DS-3	10			UIPP
	100 Hz to 10 kHz	E3	10			UIPP
Clock Recovery Phase Detector Gain KD	All 1's data pattern, KD = 0.418/RFO	DS-3	72	80	88	µA/Rad
		STS-1		92		µA/Rad
		E3		62		µA/Rad
Clock Recovery Phase Locked Oscillator Gain KO			12	14.5	17	Mrad/ sec. -Volt

Note 1: UI (Unit Interval) defined as 22.35 ns for DS-3, 29.1 ns for E3 and 19.29 ns for STS-1.

TRANSMITTER

All of the measurements for the transmitter are made with the following conditions unless otherwise stated:

1. Transmit pulse characteristics are obtained using a line transformer which has the characteristics, similar to Pulse Engineering PE-65969, Mini circuit T4-1, Valor PT5045.
2. The circuit is connected as in Figure 1.

PARAMETER		CONDITIONS		MIN	NOM	MAX	UNIT
Transmit clock repetition	TTCF		DS-3		22.35		ns
			STS-1		19.29		ns
			E3		29.1		ns
Transmit clock pulse width	TTC		DS-3		11.18		ns
			STS-1		9.65		ns
			E3		14.55		ns
Transmit clock negative transition time	TTCNT				4.5	6	ns
Transmit clock positive transition time	TTCPT				4.5	6	ns
Transmit data set-up time	TTPDS		DS-3	3.5	11.18		ns
			STS-1	3.5	9.65		ns
	TTNDS		E3	3.5	14.55		ns
Transmit data hold time	TTPDH		DS-3	3.5	11.18		ns
			STS-1	3.5	9.65		ns
	TTNDH		E3	3.5	14.55		ns
Transmit positive line pulse width	TTPL	Measured at transformer, LBO = High	DS-3	10.62	11.18	12	ns
		LBO = High	STS-1		9.65		ns
		LBO = Low	E3		14.5		ns
Transmit negative line pulse width	TTNL	Measured at transformer, LBO = High	DS-3	10.62	11.18	12	ns
		LBO = High	STS-1		9.65		ns
		LBO = Low	E3		14.5		ns
Transmit line pulse waveshape		See Note 1 for DS-3 See Note 2 for E3 See Note 3 for STS-1					

Note 1: Characteristics are in accordance with ANSI T1.102 - 1993 Table 4 and Figure 4.
Note 2: Characteristics are in accordance with ITU-T G.703 - 1991 Figure 17.
Note 3: Characteristics are in accordance with ANSI T1.102 - 1993 Figure A.1.

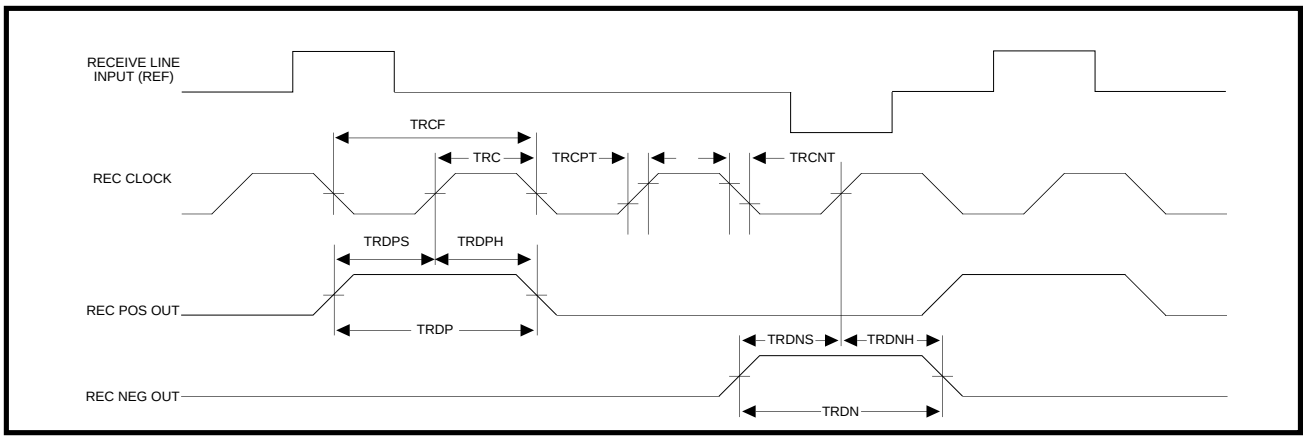


FIGURE 2: Receive Waveforms

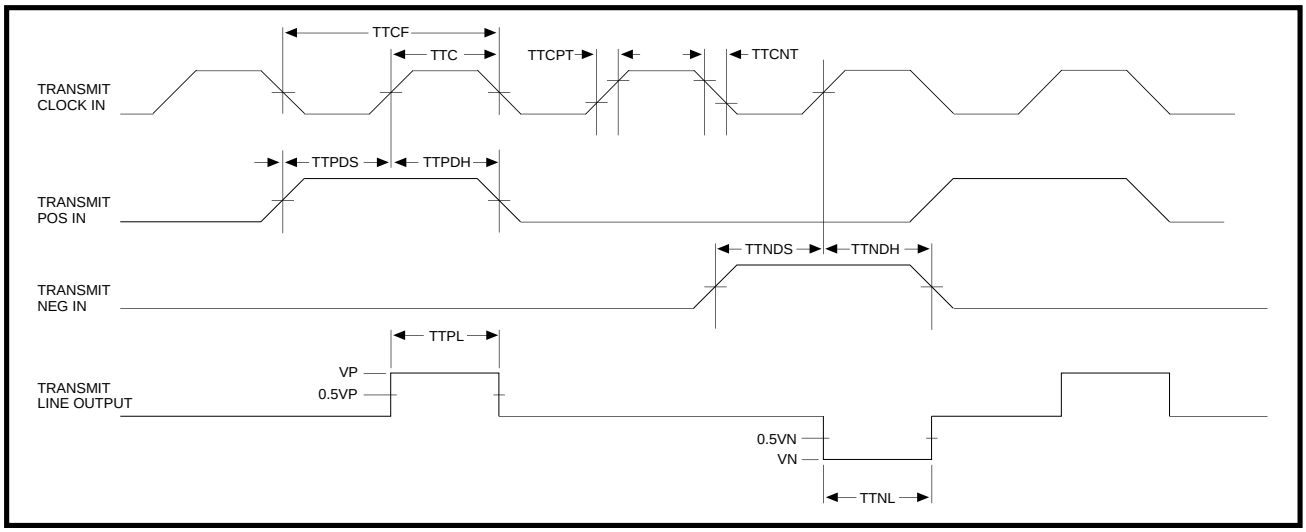
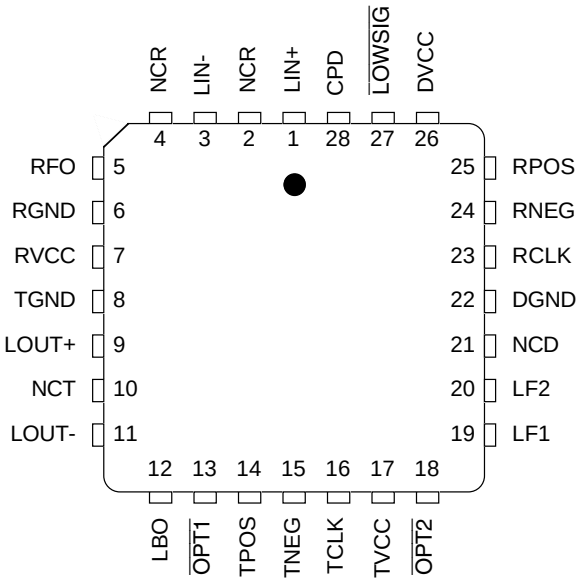


FIGURE 3: Transmit Waveforms

PACKAGE PIN DESIGNATIONS

(Top View)

CAUTION: Use handling procedures necessary for a static sensitive component.



28-Pin PLCC

ORDERING INFORMATION

PART DESCRIPTION	ORDER NUMBER	PACKAGE MARK
SSI 78P7200, DS-3/E3/STS-1 Line Interface 28-pin Surface Mount 28-pin PLCC	78P7200-IH	78P7200-IH

Silicon Systems, Inc. 14351 Myford Road, Tustin, CA 92680-7022, (714) 573-6000, FAX (714) 573-6914

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SSI 78Q2250
155 Mbit/s ATM Line Transceiver

Preliminary Data

March 1996

DESCRIPTION

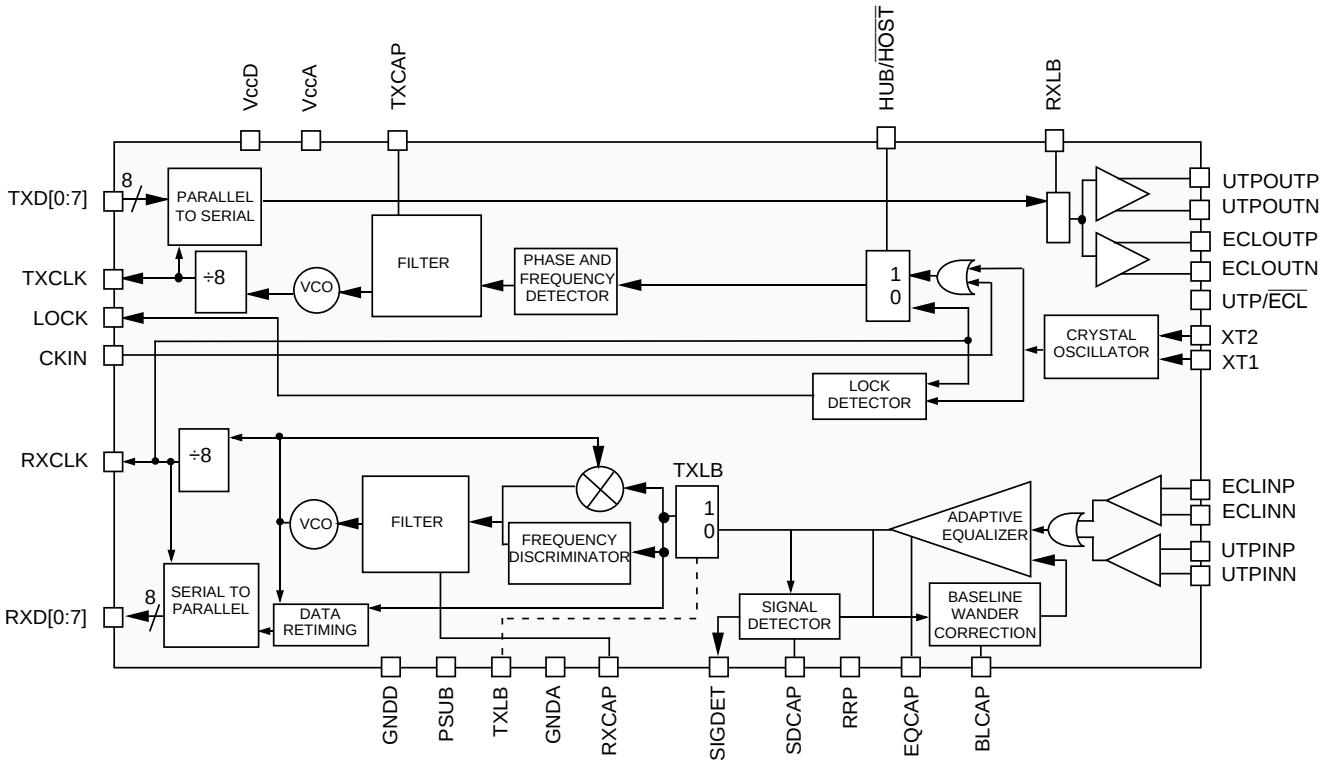
The SSI 78Q2250 is a high-speed line transceiver integrated circuit intended for use in Asynchronous Transfer Mode (ATM) applications. It is used at the interface to Category 5 Unshielded Twisted-Pair (UTP) cabling and is connected to the line via isolation transformers. Optionally, a PECL interface is provided for use with an optical interface device. Interface to digital framer circuits is accomplished via 8-bit parallel CMOS I/O running at 19.44 Mbit/s.

The IC provides full transmit and receive line interface functions with minimum external components required. The receiver provides adaptive equalization for accurate clock and data recovery. The 78Q2250 is built in a BiCMOS technology for highest performance and low power operation, and is housed in a 48-Pin TQFP package.

FEATURES

- **155.52 Mbit/s interface for Category 5 Unshielded Twisted Pair (UTP) cable**
- **Compliant with ATM PMD interface specification for 155.52 Mbit/s over Twisted Pair Cable**
- **Parallel CMOS logic interface at 19.44 Mbit/s**
- **PECL interfaces for connection to fiber optic receive and transmit modules**
- **Automatic gain adaptive equalization**
- **Baseline wander correction**
- **Receive clock and data recovery**
- **Advanced BiCMOS processing**

BLOCK DIAGRAM



FUNCTIONAL DESCRIPTION

The SSI 78Q2250 is an ATM line transceiver IC that contains all the necessary transmit and receive circuitry for connection between 155 Mbit/s line signals and digital Framer/Deframer ICs. The device provides connection to up to 100 meters of category 5 UTP via isolating transformers. The receiver includes adaptive equalization, baseline wander correction, clock and data recovery and serial-to-parallel conversion. The transmitter includes parallel-to-serial conversion, signal clocking from either a crystal or recovered clock and line driver.

TRANSMITTER OPERATION

The transmitter section accepts 8-bit parallel data at 19.44 MHz, serializes it into a 155.52 Mbit/s data signal, and generates an analog signal for transmission through a transformer onto the UTP cable. Clocks for the parallel and serial data signals are generated from a crystal oscillator using a PLL which phase locks a high frequency VCO to the crystal reference frequency via an 8x frequency divider.

Transmitter operation is affected by various mode signals. The HUB/$\overline{\text{HOST}}$ input changes the reference signal for the clock generator. In the hub mode, the transmit clock reference is derived from either the crystal oscillator or CKIN, as described below. In host mode, the transmit clock reference is derived from the receiver recovered clock.

The UTP/$\overline{\text{ECL}}$ input selects the output interface to be used. In UTP mode, the pins UTPOUTP/N are active and connect the chip to the UTP cable through a transformer and a matching resistor as shown in Figure 2. In UTP mode, ECLOUTP/N are inoperative and should be left open. In ECL mode, the UTP pins are inoperative and should be left open and the output data signal comes from pins ECLOUTP/N as differential ECL as illustrated in Figure 3. This allows the chip to drive an optical transceiver.

An external clock signal (CMOS) at CKIN may be substituted for a crystal as the reference frequency for the chip. In this mode, XT1 and XT2 must be configured as shown in Figure 3. Note that the chip can be in either ECL or UTP mode when using either an external clock or a crystal for the reference. CKIN should be tied to Vcc when using a crystal as shown in Figure 2.

RECEIVER OPERATION

The receiver section accepts serial NRZ data at 155.52 Mbit/s either from the UTP or the ECL inputs, equalizes it for cable dispersion, corrects it for baseline wander, recovers a 155.52 MHz clock signal, and converts the data to an 8-bit parallel signal with a corresponding 19.44 MHz clock. When operating the receiver in ECL mode, the UTPINP/N should be left open and, when operating in UTP mode, the ECLINP/N pins should be left open.

In UTP mode, the inputs UTPINP/N receive the 155.52 MHz input signal from Category 5 UTP cable (100 meters maximum length) which is transformer-coupled to the chip as shown in Figure 2. The output SIGDET goes high when the signal detect circuitry determines that a signal is present.

The signal is equalized for the dispersive effects of the cable by the adaptive equalizer section, which searches for a particular signal level and adds a filtered version of the input signal until it detects the right level.

The signal is also corrected for the baseline wander. This is a condition where the effects of the data pattern and the droop of the transformers cause the input data signal to have a non-zero DC component or “baseline.” The baseline wander correction circuit analyzes the positive and negative pulse levels as they emerge from the adaptive equalizer and adjusts the DC component of the equalizer’s input signal. The detection scheme of the baseline wander circuit and the difference in the time constants between it and the adaptive equalizer prevent the two control loops from contending.

The receive PLL recovers a 155.52 MHz clock signal from the equalized data signal. The NRZ data signal is rectified and filtered to generate a 155.52 MHz tone and then it goes into a multiplier-type phase detector.

The loop uses a VCO similar to the one in the transmitter. Frequency acquisition is performed by a quadricorrelator circuit which forces the VCO to a frequency close enough for the loop to self-acquire. A lock detector compares the frequency of the output of the receive PLL to that of the crystal (or the external clock reference). When the frequencies are close enough, its output, LOCK, is asserted indicating that the receive PLL is frequency-locked.

Once the equalized data signal is re-timed with the recovered clock, it is converted to 8 parallel bits and sent off-chip with a 19.44 MHz clock.

LOOPBACK OPERATION

The 78Q2250 is capable of performing signal loopback in two directions. The RXLB pin selects the receive loopback mode. In this mode, the received signal is “looped back” and sent out of transmitter in place of the transmit input signal. The TXLB pin selects the transmit loopback mode, and causes the receiver to use the transmitter output signal as its input. In this case both sets of receive input signals (UTP and ECL) are ignored. Note, the chip should not be in TXLB and HOST mode at the same time.

PIN DESCRIPTION

NAME	TYPE	DESCRIPTION
TXD [7-0]	I,C	Transmit Data Input. The parallel transmit data is converted to serial, bit 7 first.
TXCLK	O,C	Transmit clock output. 19.44 MHz.
CKIN	I,C	Optional 19.44 MHz input for the reference clock. The crystal oscillator external components should be configured as in Figure 3.
ECLOUTP, ECLOUTN	O,E	Active transmit outputs when the chip is in ECL mode. See Figure 3. These outputs are Pseudo ECL, referenced to Vcc.
UTPOUTP, UTPOUTN	O	Active transmit output in UTP mode. See Figure 2.
TXCAP	-	Auxiliary transmit PLL loop filter capacitor.
RXLB	I, C	Loopback receiver input to transmitter output.
UPTINP UTPINN	I	Active receiver inputs in UTP mode. See Figure 2.
ECLINP, ECLINN	I,E	Active receiver inputs in ECL mode. See Figure 3. These inputs are Pseudo ECL, referenced to Vcc.
RXCLK	O,C	Recovered receive clock. 19.44 MHz.
RXD[7-0]	O,C	Receive data. The first bit in the serial stream appears on bit 7.
RXCAP	-	Auxiliary loop filter capacitor for clock recovery PLL.
TXLB	I,C	Loopback transmitter input to receiver output.
SIGDET	O,C	High when an active receive input is detected.
LOCK	O,C	High when the receive PLL is locked.
HUB/$\overline{\text{HOST}}$	I,C	Configures the circuit in Hub (input high) or Host mode (input low).
UTP/$\overline{\text{ECL}}$	I,C	Selects UPT (input high) or ECL (input low) modes.
RRP	-	External reference resistor 10 kΩ ± 1%.
XT1, XT2	-	Crystal Oscillator Inputs. 19.44 MHz crystal.
VccA, VccD	S	Supply Voltage.
GNDD, PSUB, GNDA	S	Ground.
SDCAP	-	Auxiliary signal detector capacitor.
EQCAP	-	Auxiliary equalizer capacitor.
BLCAP	-	Auxiliary baseline wander capacitor.
EQOUT	-	Test pin used by factory, leave open.

NOTES: Pin Type: I - Input; O - Output; S - Supply; C - CMOS digital; E - Differential ECL

ELECTRICAL SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Operation of the IC beyond these limits may result in damage.

PARAMETER		RATING
Ambient Temperature		-40 to 85°C
Junction Temperature	θja = 70°C/W	-40 to 100°C
Lead Temperature	Soldering, 10 sec.	235°C (IR)
Supply Voltage		6V
Power Dissipation	Ta = 85°C, Tj = 125°C	350 mW
Pin Voltage		-0.3 to V_{CC} + 0.3V
Pin Current		100 mA

POWER SUPPLY

The following specifications are met for the conditions: 0°C < Ta < 70°C and 3.0 < V_{CC} < 5.5

PARAMETER		CONDITION	MIN	NOM	MAX	UNIT
Supply Current	(UTP Mode)			65	85	mA
Supply Voltage	(ECL Mode)			65	85	mA

DIGITAL INTERFACE

The following specifications refer to the CMOS interface pins: RXD[7-0], RXCLK, TXD[7-0], TXCLK, CKIN, LOCK, TXLB, RXLB, SIGDET, HUB/$\overline{\text{HOST}}$, UTP/$\overline{\text{ECL}}$.

V_{IL}	3.0 ≤ Vcc ≤ 5.5			Vcc • 0.2	V
V_{IH}	3.0 ≤ Vcc ≤ 5.5	Vcc • 0.8			V
I_{IL}		-100		100	µA
I_{IH}		-100		100	µA
Input Capacitance			10		pF
V_{OL}	I = 100 µA			200	mV
V_{OH}	I = -100 µA	Vcc - 0.2			V

ELECTRICAL SPECIFICATIONS (continued)

EXTERNAL COMPONENTS

PARAMETER	CONDITION	MIN	NOM	MAX	UNIT
External Reference Resistor R_{RP}	1% Tolerance		10		kΩ
Crystal			19.44		MHz
Crystal Capacitor C_{XT}			27		pF
TX Loop Filter Capacitor C_{TX}			TBD		
RX Loop Filter Capacitor C_{RX}			TBD		
Line Transformer Turns Ratio T_L			1:1		
TX Termination Resistor R_{TT}			50		Ω
RX Termination Resistor R_{TR}			100		Ω
Signal Detector Capacitor C_{SD}			TBD		
Equalizer Capacitor C_{EQ}			TBD		
Baseline Wander Capacitor C_{BL}			TBD		

TRANSMITTER

The following are the specifications for the Transmitter section. They assume use of the external components as listed in this data sheet and up to 100 meters of Category 5 Unshielded Twisted Pair (UTP) Cable.

TXD Setup Time T_{SU}	Refer to figure 1	20			ns
TXD Hold Time T_H	Refer to figure 1	20			ns
TXCLK Period T_{PER}	Refer to figure 1		52.6		ns
TXCLK Duty Cycle T_{DC}	Refer to figure 1	40		60	%
Output Voltage	Peak-to-peak differential	0.94	1	1.06	V
Output Voltage Overshoot	Beyond final output voltage value			10	%
Output Voltage Setting	To final output voltage			3.2	ns
Output Jitter	Peak-to-peak			2	ns
NRZ Pulse Duty Cycle	0101 Pattern best fit to a 6.43 ns grid	-0.25		0.25	ns
Rise/ Fall Time	10-90%	1.5		3.5	ns
Rise/ Fall Imbalance				0.5	ns
Baseline Wander	100 Consecutive bits of logical ones		10		%

ECL TRANSMITTER OUTPUTS

Voh	Relative to Vcc		-0.8	-0.7	V
Vol	Relative to Vcc	-1.9	-1.8		V
Rise Time			1		ns
Fall Time			2.5		ns

RECEIVER

The following are the specifications for the Receiver section. They assume use of the external components as listed in this data sheet and up to 100 meters of Category 5 Unshielded Twisted Pair (UTP) Cable.

PARAMETER	CONDITION	MIN	NOM	MAX	UNIT
RXCLK Period RPER	Refer to figure 1		52.6		ns
RXCLK Duty Cycle RDC	Refer to figure 1	40		60	%
RXCLK to Data Propagation Delay, R_{prop}	Refer to figure 1		2		ns
Baseline Wander Tolerance			10		%
Maximum Cable Length	Category 5 UTP		100		m
Bit Error-rate	100m Cat. 5 UTP		10^{-10}		
Input Voltage at UPT Inputs				1.06	V
Maximum Output Jitter	Random data, 100m cable			2	ns

ECL RECEIVER INPUTS

Vil	Relative to Vcc	-1.8			V
Vih	Relative to Vcc			-1	V
Duty Cycle		40		60	%

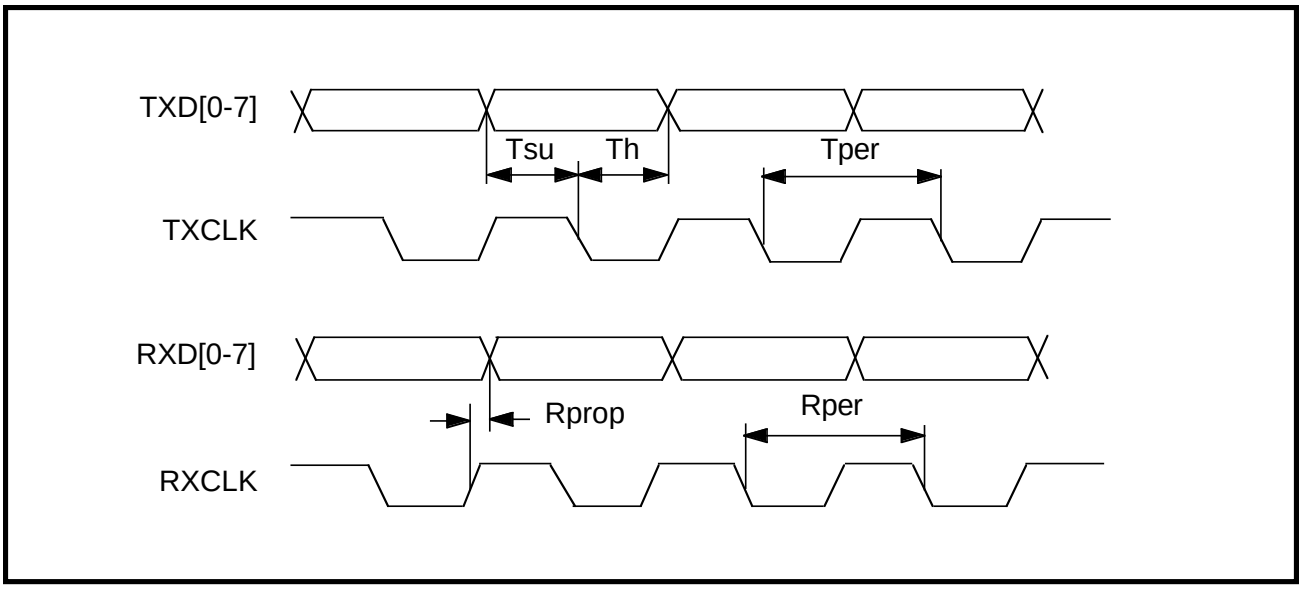
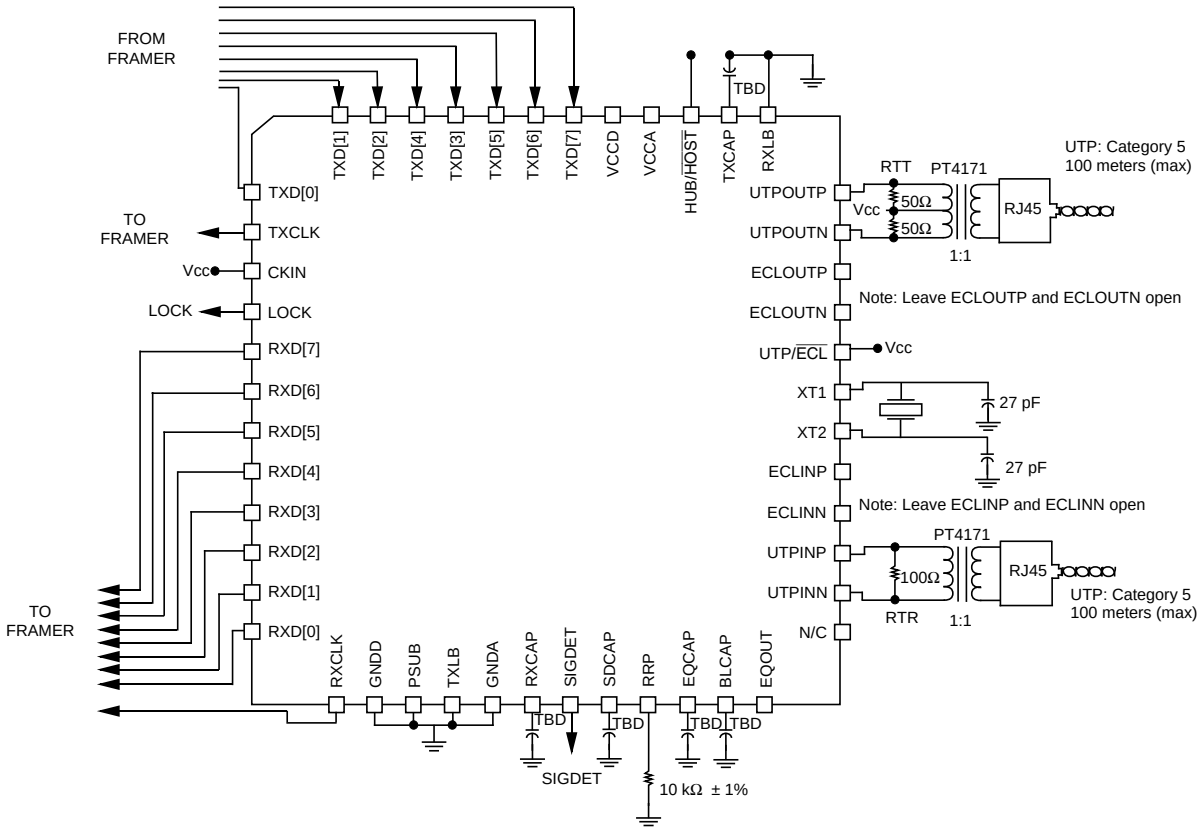
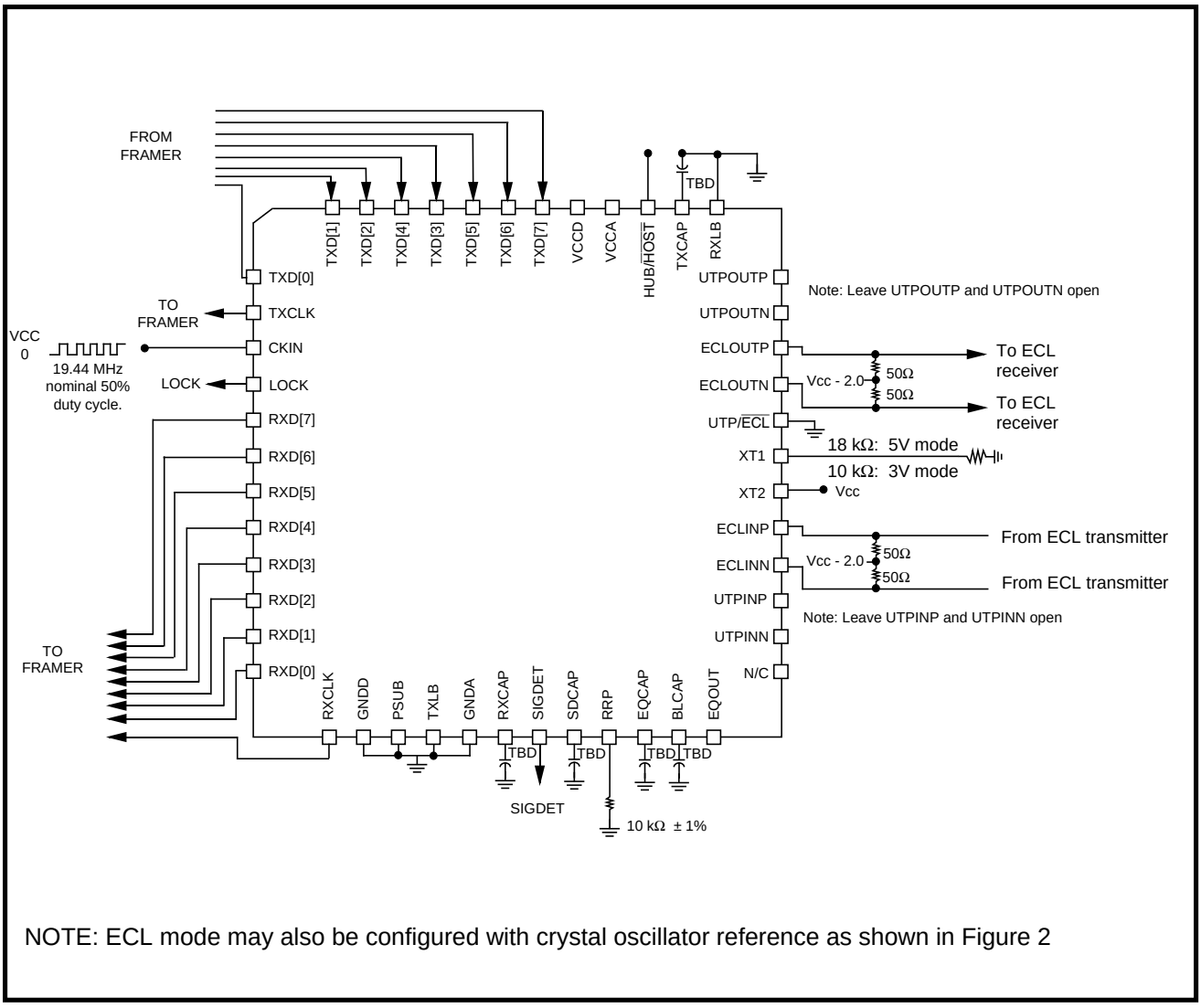


FIGURE: 1 Timing for CMOS I/O



NOTE: UTP mode may also be configured with external clock reference as shown in Figure 3

FIGURE: 2 Circuit Configuration for UTP Mode with Crystal Oscillator Reference



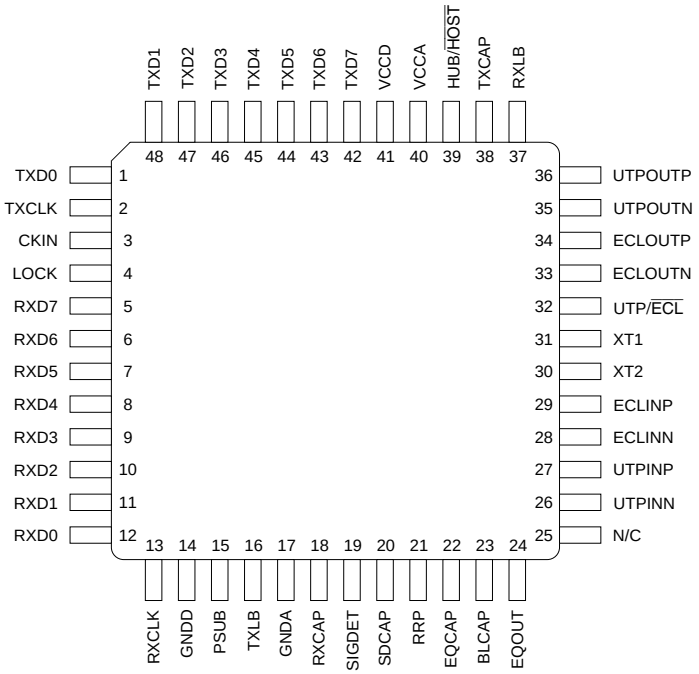
NOTE: ECL mode may also be configured with crystal oscillator reference as shown in Figure 2

FIGURE: 3 Circuit Configuration for ECL Mode with External Clock Reference

SSI 78Q2250
155 Mbit/s ATM
Line Transceiver

PACKAGE PIN DESIGNATIONS

(Top View)



48-Lead TQFP

ORDERING INFORMATION

PART DESCRIPTION	ORDER NUMBER	PACKAGE MARK
SSI 78Q2250 155 Mbit/s ATM Transceiver 48-Pin TQFP	78Q2250-CGT	78Q2250-CGT

Preliminary Data: Indicates a product not completely released to production. The specifications are based on preliminary evaluations and are not guaranteed. Small quantities are available, and Silicon Systems should be consulted for current information.

Silicon Systems, Inc., 14351 Myford Road, Tustin, CA 92680-7022 (714) 573-6000, FAX (714) 573-6914

SSI 78Q2251
100M/155M High Speed Line Transceiver
Target Specification

March 1996

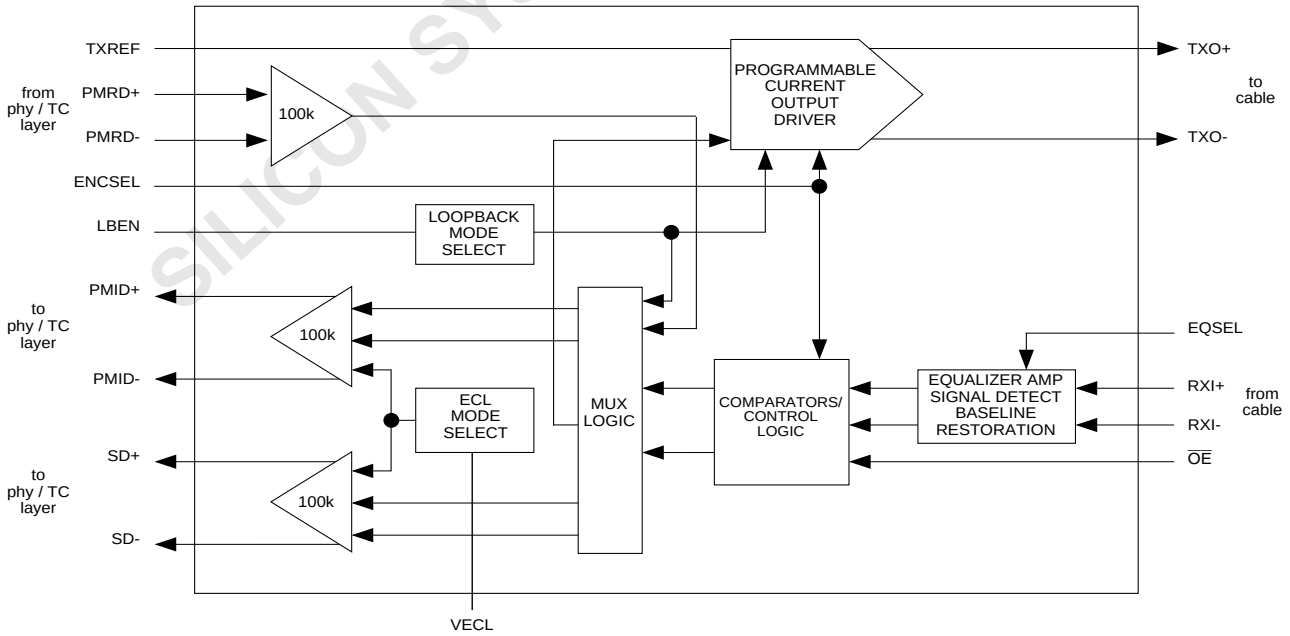
DESCRIPTION

The SSI 78Q2251 is a high speed networking transceiver capable of transmitting and receiving datastreams at 100 Mbit/s and 155 Mbit/s. It is pin compatible with National Semiconductor's DP83223A. It is capable of driving both binary and MTL-3 datastreams. The SSI 78Q2251 allows links over Category 5, datagrade, Unshielded Twisted Pair (UTP) for up to 100 meters. The SSI 78Q2251 is compliant to FDDI ANSI X3T9.5 TP-PMD standard, the IEEE 802.3 100Base-TX Fast Ethernet Specification and the ATM Forum155 Mbit/s twisted Pair PMD Interface Specification. The SSI 78Q2251 incorporates a complete line interface function. This includes a new proprietary adaptive equalizer design with automatic gain control and full baseline wander correction on the receive side, and a sophicated pulse shaper on the transmit side.

FEATURES

- **Compliant with FDDI ANSI X3T9.5 TP-PMD, IEEE 802.3 100Base-TX Ethernet, ATM Forum 155 Mbit/s Twisted Pair Specification**
- **Baseline wander correction**
- **Integrated transmitter and receiver with adaptive equalization**
- **Programmable binary or MLT-3 operation**
- **Extensive loopback feature for board diagnostics**
- **Pin compatible with industry standard 100 Mbit/s and 155 Mbit/s front end**
- **Operation at 3.3V and 5.0V**
- **Available in a 28-Lead PLCC package**

BLOCK DIAGRAM



The target specification is intended as an initial disclosure of specification goals for the product. The specifications are based on design goals, subject to change and are not guaranteed. Silicon Systems assumes no obligation regarding future manufacture unless agreed to in writing.

FUNCTIONAL DESCRIPTION

The SSI 78Q2251 consists of six functional blocks.

Programmable Current Output Driver

Adaptive Equalizer and Baseline Wander Correction

Control Logic

Mux Logic

Loopback Mode Select

ECL Mode Select

The transmit section accepts PECL NRZ or NRZI data at its PMRD± input pins. When the ENCSEL pin is high, the NRZ data is passed directly to the TXO± output pins via the programmable current output driver. When ENCSEL is low, NRZI data from the PMRD± input pins is encoded to an MLT-3 format at the TXO± output pins.

The receive path includes an adaptive equalizer, a baseline wander corrector, and a signal detect block. The multi-mode adaptive equalizer will restore the losses incurred in up to 100 meters of UTP5 cable. The baseline wander corrector adjusts the biasing of the input stage when the time averaged DC component of an incoming data stream changes. The corrected biasing ensures consistent interpretation of the incoming data resulting in improved bit error rates. The signal detect block determines incoming data presence in a manner consistent with the specifications set forth in the ANSI FDDI TP-PMD standard.

Two modes of loopback operation are available. When LBEN is high, the PMID± pins follow the PMRD± pins, the SD+ and SD- pins are forced high and low respectively, and the TXO± pins maintain a balanced output level. When LBEN is floated or is in the range between 1/3 and 2/3 Vcc, the second loopback mode is entered. In this mode the TXO± pins will follow the RXI± pins. The PMID± and SD± pins maintain their normal operational function in that they will reflect the data present on the RXI± pins.

The PMID± and SD± PECL output pins feature a variable operational mode. These VECL (Variable ECL) differential output pins have two operational modes. When the VECL pin is set high, the device will operate in a conventional 50Ω 100k compatible PECL mode. When the VECL pin is pulled low, a second low current mode is entered. This mode consumes 1/3 of the current used by convetional 100k drivers and is capable of driving 100k PECL levels referenced to the 5V rail.

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Section 7

LAN PRODUCTS

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SSI 78Q2120
10/100Base-TX Ethernet Transceiver
Advance Information

March 1996

DESCRIPTION

The SSI 78Q2120 is an auto-sensing, auto-switching 10Base-T/100Base-X fast ethernet transceiver with integrated MII, 10Base-T/100Base-X ENDEC, scrambler/descrambler, clock recovery, and full-featured auto-negotiation function. The transmitter includes on-chip pulse-shaper and a low power line driver, while the receiver has a sophisticated combination AGC, real-time adaptive equalizer, and an adaptive D.C. offset adjustment circuit to provide the best combination of ISI cancellation and baseline wander correction required for accurate clock and data recovery. The 100Base-X transceiver is used at the interface to Cat-5 UTP cabling, and is connected to the line media via simple 1:1 isolation transformers. No external filter is required. Interface to the MAC is accomplished through MII, as specified by IEEE-802.3u. The chip is built in a BiCMOS technology for high performance and low power operation and can operate from a single 3.3V or 5V supply.

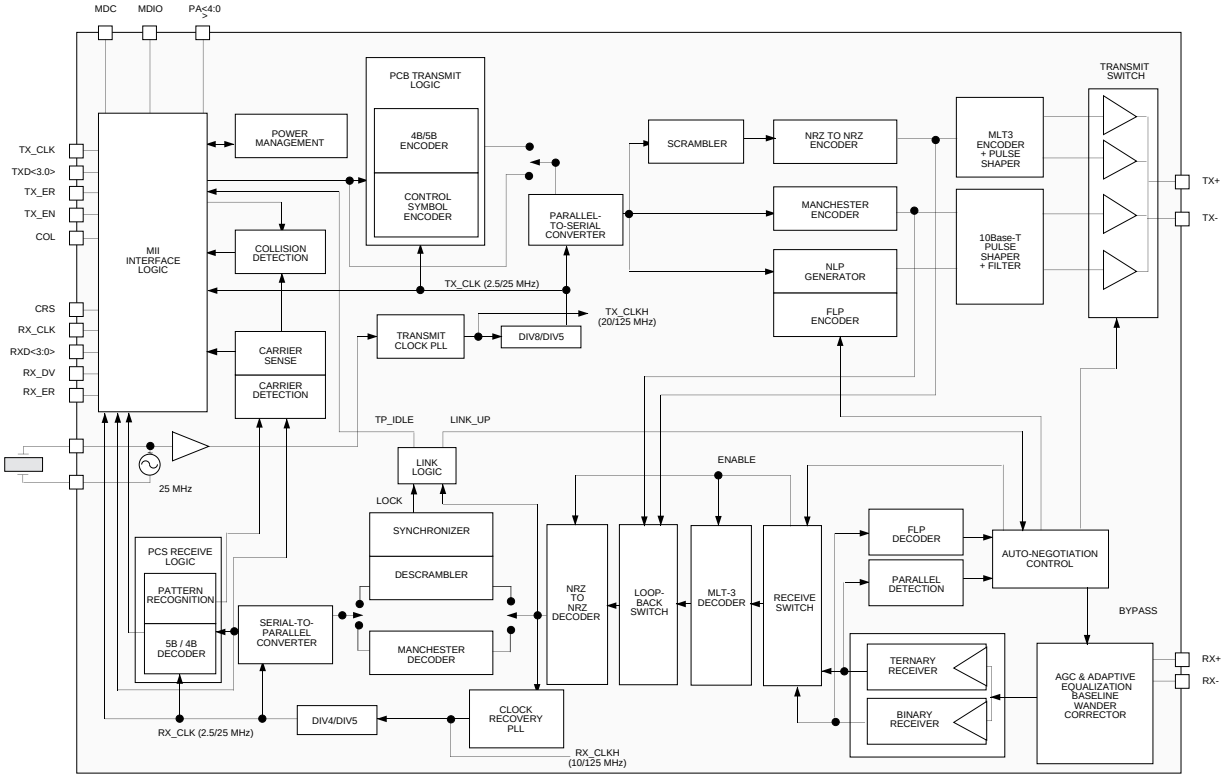
FEATURES

GENERAL

- **10Base-T/100Base-X IEEE-802.3u compliant transceiver**
- **Integrated MII, 10Base-T/100Base-X ENDEC with dual speed clock-recovery, 100Base-X scrambler/descrambler, 10Base-T/100Base-X line driver and receiver, and full-featured auto-negotiation function**
- **Full Duplex operation capable**
- **Extensive LED indicators: LINK, TX, RX, COL/FDX, SPEED**
- **Auto-polarity correction during 10Base-T signal reception and auto-negotiation**
- **Low power design with intelligent power management that shuts off all dormant circuitry. Also supports power-down mode.**

(continued)

BLOCK DIAGRAM



GENERAL (continued)

- Advanced BiCMOS technology
- 64-lead TQFP package
- Operation at a single 5V or 3.3V supply

MII

- Full-featured MII management functions with extended register set
- Same MII interface for 10 and 100 Mbit operation
- RX_CLK may be turned off during no reception through Vendor defined register
- Full 5-bit pin-configurable PHY Address for multiple PHY environment
- Pin selectable power-up high impedance or active
- Power-On-Reset circuitry resets the chip into a known state during power-up
- Operational on power-up without management intervention

AUTO-NEGOTIATION

- Auto-sensing and auto-switching between 10Base-T and 100Base-TX signals
- Parallel Detect function allows interoperability with existing 10Base-T devices and 100Base-TX devices with no auto-negotiation ability

LINE DRIVER/RECEIVER

- Built-in transmit wave shaper for both 10Base-T and 100Base-TX operation. No external filter is required.
- Integrated AGC, adaptive equalization and base-line wander correction for 100Base-TX receiver
- Internal switching between 10Base-T and 100Base-TX signals
- Requires only one set of simple 1:1 isolation transformer for connection to both 10Base-T and 100Base-TX networks
- Smart squelch circuitry to improve receive noise rejection

FUNCTIONAL DESCRIPTION

ANALOG OPERATION

The transmit section of this chip contains all necessary circuitry to convert the MII signals from the MAC, to an IEEE-802.3u compliant data-stream driving a pair of Cat-5 UTP cable. It generates the 20 MHz (10Base-T) or 125 MHz (100Base-X) internal clocks using a programmable PLL synthesizer locked to a local 25 MHz crystal oscillator. 10Base-T signals are predistorted and pulse-shaped to retain backward compatibility with existing 10Base-T transceivers.

On the receive side, data signals from up to 100m of Cat-5 UTP cable enter the chip through a transformer. This signal goes through a combination of adaptive offset adjustment (baseline wander correction), automatic gain, and adaptive equalization. The effect of these circuits is to look for the amount of dispersion and attenuation caused by the cable and the offset (baseline wander) caused by the transformer, and restore the received pulses to logic levels. The amount of gain and equalization applied to the pulses varies with the detected attenuation and dispersion and, therefore, with the length of the cable. The equalized data signal is then decoded through analog receivers, and the clock signal is extracted using a low-jitter PLL. The recovered clock is used to re-time the data signal. The integrated signal qualifier has squelched and unsquelched thresholds, and includes built-in timer to ensure accurate receive signal detection and receive noise rejection.

The SSI 78Q2120 uses the local crystal oscillator to generate accurate bias voltages for setting the various precision circuitry on chip. This technique allows rise and fall times of transmit pulses to be controlled accurately, and also allows center frequencies of the two on-chip VCO's to be set precisely. All of this is achieved without trimming and without precision external components, which are typical in other IC's requiring precision timing. The ability to set accurate center frequencies allow the use of narrow-band PLL circuits without the requirement of frequency discrimination circuits to aid clock acquisition.

DIGITAL OPERATION

All aspects of digital operation are compliant with IEEE-802.3 Clause 14 and IEEE-802.3u Clauses 22, 24, 25 and 28. For the 100Base-TX transmit operation, the SSI 78Q2120 takes 4-bit data from the MAC through MII; encodes it into 5-bit code-group; serializes it into a 125 Mbit/s NRZ bit stream; performs scrambling; converts into MLT-3 signals and drives it on the line. The receive path converts a 125 Mbit/s MLT-3 signal to a 125 Mbit/s NRZ bit stream. It performs a serial to parallel conversion on the data and descrambles it into 5-bit code groups. It then performs a 5B/4B decoding and finally presents the 4-bit receive data to the MAC through MII.

The SSI 78Q2120 also implements the full 10Base-T specification which includes Link Integrity, Collision Detection, Jabber and Loopback. Additionally, Smart Squelch Logic and Auto-Polarity Correction are supported.

REGISTER DESCRIPTION

The MII Management 16-bit Register set implemented in the 2120 is as follows:

ADDRESS	SYMBOL	NAME	DEFAULT (HEX)
0	MR0	Control	(3000)
1	MR1	Status	(7809)
2	MR2	PHY Identifier 1	0300
3	MR3	PHY Identifier 2	E541
4	MR4	Auto-Negotiation Advertisement	(01E1)
5	MR5	Auto-Negotiation Link Partner Ability	0000
6	MR6	Auto-Negotiation Expansion	0000
7	MR7	(Not Implemented, read as zero)	0000
8-15	MR8-15	(Reserved, read as zero)	0000
16	MR16	Vendor Specific	0000

LEGEND

TYPE	DESCRIPTION	TYPE	DESCRIPTION
R	Readable by management	W	Writable by management
SC	Self Clearing	RC	Cleared on a read operation
0/1	Default value upon power-up or reset	(0/1)	Default value dependent on pin setting. The value in brackets indicates typical case.

MR0 - CONTROL REGISTER

BIT	SYMBOL	TYPE	DESCRIPTION
0.15	RESET	R, W, 0, SC	RESET: Setting this bit to logic one resets the 2120 and sets all registers to their default states. This bit is self clearing.
0.14	LOOPBK	R, W, 0	LOOPBACK: When this bit is set to logic one, no transmission of data on the network medium occurs and any receive data on the network medium is ignored. By default, the loopback signal path will encompass as much of the 2120 circuitry as possible. The loop back signal path may be changed through MR16, Vendor Specific Register. This bit allows for a diagnostic test.
0.13	SPEEDSL	R, W, 1	SPEED SELECTION: Upon reading, this bit always reflects the selected speed of operation (1 = 100 Mbit/s; 0 = 10 Mbit/s). This bit can only be written when the Auto-Negotiation Enable bit (0.12, ANEGEN) is disabled (logic low) and TECH <2:0> are zero; in which case it manually selects the speed of operation.
0.12	ANEGEN	R, W, 1	AUTO-NEGOTIATION ENABLE: The auto-negotiation process shall be enabled by setting this bit to logic one. This bit can only be set to logic one if ANEGA bit is a logic one. If this bit is cleared to zero, manual speed selection through bit 0.13 and manual duplex mode selection through bit 0.8 take place.

MR0 - CONTROL REGISTER (continued)

BIT	SYMBOL	TYPE	DESCRIPTION
0.11	PWRDN	R, W, 0	POWER-DOWN: The 2120 may be placed in a low power consumption state by setting this bit to logic one. While in power-down state, the 2120 still responds to management transactions. The power-down state can also be achieved by setting PWRDN pin high.
0.10	ISO	R, W, (0)	ISOLATE: When set to logic one, the 2120 will present a high impedance on its MII output pins. This allows for multiple PHY to be attached to the same MII interface. When the 2120 is iolated, it stills responds to management transactions. The default value of this bit depends on the ISODEF pin. When ISODEF pin is tied high (low), the ISO bit defaults to high (low). The same high impedance state can also be achieved through the ISO pin.
0.9	RANEG	R, W, 0, SC	RESTART AUTO-NEGOTIATION: Normally, the auto-negotiation process is started at power-up. The process can be restarted by setting this bit to logic one. This bit is self clearing.
0.8	DUPLEX	R, W, 0	DUPLEX MODE: Upon reading, this bit always reflects the duplex mode of operation (1 = Full Duplex; 0 = Half Duplex). This bit can only be written when the auto-negotiation enable bit (0.12, ANEGEN) is disabled (logic low) and TECH<2:0> are zero; in which case it manually selects the duplex mode of operation. The loopback diagnostic test through bit 0.14 is not affected by this bit.
0.7	COLT	R, W, 0	COLLISION TEST: When this bit is set to one, 2120 will assert the COL signal in response to the assertion of TX_EN signal.
0.6:0	RSVD	R, 0	RESERVED

MR1 - STATUS REGISTER

Bits 1.15 through 1.11 reflect the ability of the SSI 78Q2120 as configured by the TECH[2:0] and the T4 pins. They do not reflect any ability changes made via the MII management ifterface to bits 0.13 (SPEEDSL), 0.12 (ANEGEN) and 0.8 (DUPLEX).

1.15	100T4	R, (0)	100Base-T4 ability. (0 = Not able, 1 = Able)
1.14	100X_F	R, (1)	100Base-X Full Duplex ability. (0 = Not able, 1 = Able)
1.13	100X_H	R, (1)	100Base-X Half Duplex ability. (0 = Not able, 1 = Able)
1.12	10T_F	R, (1)	10Base-T Full Duplex ability. (0 = Not able, 1 = Able)
1.11	10T_H	R, (1)	10Base-T Half Duplex ability. (0 = Not able, 1 = Able)
1.10:6	RSVD	R, 0	RESERVED
1.5	ANEGC	R, 0	AUTO-NEGOTIATION COMPLETE: A logic one indicates that the auto-negotiation process has been completed, and that the contents of registers MR4, 5, 6 are valid.
1.4	RFAULT	R, 0, RC	REMOTE FAULT: A logic one indicates that a remote fault condition has been detected and when so it remains set until it is cleared. This bit can only be cleared by reading this register (MR1) via the management interface.

MR1 - STATUS REGISTER (continued)

BIT	SYMBOL	TYPE	DESCRIPTION
1.3	ANGEA	R, (1)	AUTO-NEGOTIATION ABILITY: This bit, when one, indicates the ability to perform auto-negotiation. The value of this bit is determined by the ANEGA pin.
1.2	LINK	R, 0	LINK STATUS: A logic one indicates that a valid link has been established.
1.1	JAB	R, 0	JABBER DETECT
1.0	EXTD	R, 1	EXTENDED CAPABILITY: This bit is permanently tied to logic one to indicate that the 2120 provides an extended register set (MR2 and beyond).

MR2, 3 - PHY IDENTIFIER REGISTER

2.15:0	OUI	R, 0300h	ORGANIZATIONALLY UNIQUE IDENTIFIER: Silicon Systems, Inc. OUI is 00-C0-39. This translates to a value of 300h for this register.
3.15:10	OUI	R, 111001	ORGANIZATIONALLY UNIQUE IDENTIFIER: Remaining 6 bits of the OUI.
3.9:4	MN	R, 010100	MODEL NUMBER: The last 2 digits of the model number 2120 is encoded into the 6 bits. (20d = 14h)
3.3:0	RN	R, 0001	REVISION NUMBER: The value of “0001” corresponds to the first revision of the silicon.

MR4 - AUTO-NEGOTIATION ADVERTISEMENT REGISTER

4.15	NP	R,0	NEXT PAGE: Not supported; permanently tied to logic zero.
4.14	ACK	R,0	ACKNOWLEDGE: Write is ignored. This bit will be set internally after receiving 3 consecutive and consistent FLP (Fast Link Pulse) bursts.
4.13	RF	R, W, 0	REMOTE FAULT: When internally set to logic one, the MII Management Interface indicates to the link partner a remote fault condition.
4.12:5	A7:0	R, W, (0Fh)	TECHNOLOGY ABILITY FIELD: The default value of this field is dependent upon MR1.15:11 bits. This field can be overwritten by management to auto-negotiation to an alternate common technology. Only the bits with the corresponding ability bits set may be written by the management.
4.12:10	A7:5	R, 0	Reserved for future technology.
4.9	A4	R, W, (0)	100BASE-T4: The 2120 does not include the function of 100Base-T4 transceiver, but it does provide support for external 100Base-T4 transceiver hook-up. The default value of this bit follows MR1.15 bit. When the default is zero, this bit cannot be written by the management.
4.8	A3	R, W, (1)	100BASE-TX FULL DUPLEX: The default value of this bit follows MR1.14 bit. When the default is zero, this bit cannot be written to a one by the management.

MR4 - AUTO-NEGOTIATION ADVERTISEMENT REGISTER (continued)

BIT	SYMBOL	TYPE	DESCRIPTION
4.7	A2	R, W, (1)	100BASE-TX: The default value of this bit follows MR 1.13 bit. When the default is zero, this bit cannot be written a one by the management.
4.6	A1	R, W, (1)	10BASE-T FULL DUPLEX: The default value of this bit follows MR1.12 bit. When the default is zero, this bit cannot be written a one by the management.
4.5	A0	R, W, (1)	10BASE-T: The default value of this bit follows MR1.11 bit. When the default is zero, this bit cannot be written a one by the management.
4.4:0	S4:0	R, 00001	SELECTOR FIELD: Hard coded with the value of 00001 for IEEE-802.3.

MR5 - AUTO-NEGOTIATION LINK PARTNER ABILITY REGISTER

5.15	NP	R, 0	NEXT PAGE: When set to logic one, it indicates that the link partner wishes to engage in next page exchange.
5.14	Ack	R, 0	ACKNOWLEDGE: When set to logic one, it indicates that the link partner has successfully received at least 3 consecutive and consistent FLP bursts.
5.13	RF	R, 0	REMOTE FAULT: When set to logic one, it indicates that the link partner has a fault.
5.12:5	A7:0	R, 0	TECHNOLOGY ABILITY FIELD: This field contains the technology ability of the link partner. The bit definition is the same as MR4.
5.4:0	S4:0	R, 00000	SELECTOR FIELD: This field contains the type of message sent by the link partner. For IEEE-802.3 compliant link partner transceiver, this field should be 00001.

MR6 - AUTO-NEGOTIATION EXPANSION REGISTER

6.15:5	RSVD	R, 0	RESERVED
6.4	PDF	R, 0, RC	PARALLEL DETECTION FAULT: When set to logic one, it indicates that a fault has been detected in the parallel detection function. This fault is due to more than one technology detecting concurrent link up conditions. This bit can only be cleared by reading this register (MR6) via the management interface.
6.3	LPNPA	R, 0	LINK PARTNER NEXT PAGE ABLE: When set to logic one, it indicates that the link partner supports the next page function.
6.2	NPA	R, 0	NEXT PAGE ABLE: Permanently tied to logic zero since the 2120 does not support next page function.
6.1	PRX	R, 0	PAGE RECEIVED: Permanently tied to logic zero since the 2120 does not support the next page function.
6.0	LPANEGA	R, 0	LINK PARTNER AUTO-NEGOTIATION ABLE: When set to logic one, it indicates that the link partner is able to participate in the auto-negotiation function.

REGISTER DESCRIPTION (continued)

MR16 - VENDOR SPECIFIC REGISTER

BIT	SYMBOL	TYPE	DESCRIPTION
16.15:7	RSVD	R, 0	RESERVED
16.6	CB	R, W, 0	CONTROL BIT: This bit controls the CP pin and is available for general purpose use. A logic zero in this bit will drive CP low and a logic one will drive CP high.
16.5	APOL_	R, W, 0	AUTO POLARITY: During auto-negotiation and 10Base-T mode, the 2120 is able to automatically invert the received signal due to a wrong polarity connection. It does so by detecting the polarity of the link pulses. Setting this bit to logic one disables this feature.
16.4	RVSPOL	R, 0	REVERSE POLARITY: The reverse polarity is detected either through 8 inverted 10Base-T link pulses (NLP) or through one burst of inverted clock pulses in the auto-negotiation link pulses (FLP). When the reverse polarity is detected, 2120 will invert the receive data path and set this bit to logic one if the feature is not disabled.
16.3:2	LBC	R, W, 0	LOOPBACK CONTROL: These two bits determine the level of loop back signal path activated by MR0.14: LOOPBK. Only the receive PLL loopback mode (LBC = 00) is valid when PCS_BP mode is enabled. When the 10Base-T is the selected technology, (LBC = 10) enables a digital loopback test mode within the 10Base-T block. LBC Loopback Level 00 Receive PLL 01 Scrambler/Descrambler 10 4B5B/ 5B4B 11 MII
16.1	DISPM	R, W, 0	DISABLE POWER MANAGEMENT: When set to logic one, the intelligent power management feature is disabled.
16.0	RXCC	R, W, 0	RECEIVE CLOCK CONTROL: When set to logic one, the RX_CLK signal will be held in logic low when there is no reception process (to save power). The RX_CLK signal will restart 1 clock cycle before the assertion of RX_DV and be shut off 6 clock cycles after RX_DV goes low.

PIN DESCRIPTION

MII (MEDIA INDEPENDENT INTERFACE)

NAME	TYPE	DESCRIPTION
TX_CLK	O4	TRANSMIT CLOCK
TX_EN	I	TRANSMIT ENABLE
TXD<3:0>	I	TRANSMIT DATA NIBBLE
TX_ER/TXD<4>	I	TRANSMIT ERROR: In PCS bypass mode (PCS_BP is high), this pin becomes the higher-order bit of the transmit 5-bit group.
COL	O4	COLLISION
RX_CLK	O4	RECEIVE CLOCK: To reduce power consumption, the 2120 provides a mode in which RX_CLK is held inactive (low) when no receive data is detected.
RX_DV	O4	RECEIVE DATA VALID
RXD<3:0>	O4	RECEIVE DATA NIBBLE
RX_ER/RXD<4>	O4	RECEIVE ERROR: In PCS bypass mode (PCS_BP is high), this pin becomes the higher-order bit of the receive 5-bit code group.
CRS	O4	CARRIER SENSE
MDC	I	MANAGEMENT DATA CLOCK
MDIO	IO4	MANAGEMENT DATA INPUT/OUTPUT

PMA (PHYSICAL MEDIA ATTACHMENT) INTERFACE

PCS_BP	I	PCS BYPASS: When strapped to high, the 100Base-TX PCS is bypassed, as well as the scrambler and descrambler functions. Scrambled five-bit code groups for transmission are applied to the TXD[4:0] pins and received on the RXD[4:0] pins. The RX_DV and TX_EN signals are not valid in this mode. PCS_BP mode is not valid when 100Base-TX is not enabled.
TDX<4>	I	Higher-order of the transmit 5-bit code group. Shared with TX_ER pin.
RXD<4>	O4	Higher-order bit of the receive 5-bit code group. Shared with RX_ER pin.

MII CONTROL AND STATUS

$\overline{\text{RST}}$	I	RESET: The IEEE Std. 802.3u MII spec does not define a reset pin and reset is achieved through a MII register bit (0.15). The 2120 also provides an integrated Power-On-Reset circuit that resets the chip during power-up. This pin is therefore provided for testability purposes to overwrite the internal Power-On-Reset circuit. It may be permanently tied to logic high for normal operation. There are thus 3 ways to reset the chip: i) through the internal Power-On-Reset ii) through the $\overline{\text{RST}}$ pin iii) through the MII register bit (0.15)
PWRDN	I	POWER-DOWN: The 2120 may be placed in a low power consumption state by setting this signal to logic high. While in power-down state, the 2120 still responds to management transactions. The same power-down state can also be achieved through the PWRDN bit in the MII register (MR0.11).

MII CONTROL AND STATUS (continued)

NAME	TYPE	DESCRIPTION
ISO	I	ISOLATE: When set to logic one, the 2120 will present a high impedance on its MII output pins. This allows for multiple PHY to be attached to the same MII interface. When the 2120 is isolated, it still responds to management transactions. The same high impedance state can also be achieved through the ISO bit in the MII register (MR0.10).
ISODEF	I	ISOLATE DEFAULT: This pin determines the power-up/reset default of the ISO bit (MR0.10). If it is connected to VDD (GND), ISO bit will have a default value of '1' ('0'). When this signal is tied to VDD, it allows multiple PHY to be connected to the same MII interface.
ANEGA	I	AUTO-NEGOTIATION ABILITY: Strapped to logic high to allow auto-negotiation function. When strapped to logic low, auto-negotiation logic is disabled and manual technology selection is done through TECH<2:0>. This pin is reflected as ANEGA bit (MR1.3).
TECH<2:0>	I	TECHNOLOGY ABILITY/SELECT: When ANEGA is a logic high, TECH<2:0> sets the technology ability of the chip which is reflected in MR4.12:5. When ANEGA is a logic low, TECH<2:0> sets the manual technology selection. The full decoding of TECH<2:0> is as follows: (TECH<0> = 10Base-T, TECH<1> = 100Base-TX, TECH<2> = Full Duplex) ANEGA TECH<2:0> Technology selected 0 000 Selection through MII register 0 001 10Base-T Half Duplex (10T_H) 0 01X 100Base-TX Half Duplex (100X_H) 0 100 Illegal combination 0 101 100Base-T Full Duplex(10T_F) 0 11X 100Base-TX Full Duplex (100X_F) 1 000 None 1 001 10T_H 1 010 100X_H 1 011 10T_H, 100X_H 1 100 Illegal combination 1 101 10T_H, 10T_F 1 110 100X_H, 100X_F 1 111 10T_H, 10T_F, 100X_H, 100X_F

100BASE-T4 LINK INTERFACE

NAME	TYPE	DESCRIPTION
T4	I	EXTERNAL 100BASE-T4 TRANSCEIVER SUPPORT: When strapped to logic high, the 2120 includes 100Base-T4 (provided externally) support in the auto-negotiation logic. This pin is reflected in MR1.15 bit. The link status and control for the external 100Base-T4 transceiver are done through LSTAT_T4<1:0> ans LCTRL_T4<1:0>.
LSTAT_T4<1:0>	I	LINK STATUS 100BASE-T4: Link Status inputs from an external 100Base-T4 transceiver. This allows external 100Base-T4 transceiver to be incorporated into the 2120 auto-negotiation logic. FAIL = 00, READY = 01, OK = 11
LCTRL_T4<1:0>	O4	LINK CONTROL 100BASE-T4: Link control outputs to an external 100Base-T4 transceiver. This allows external 100Base-T4 transceiver to be incorporated into the 2120 auto-negotiation logic. DISABLE = 00, SCAN FOR CARRIER = 01, ENABLE = 11

PHY ADDRESS

PHYAD<4:0>	I	PHY ADDRESS: Allows 32 configurable PHY addresses. The 2120 always responds to data transactions via the MII interface when the PHYAD bits are all zero independent of the logic levels of the PHYAD pins. The one exception is the vendor defined register, which responds only to MII data transactions when the PHYAD bits match the logic levels of the PHYAD pins.

MDI (MEDIA DEPENDENT INTERFACE)

TPOP, TPON	OA	TWISTED PAIR OUTPUT POSITIVE, NEGATIVE: Transmitter outputs for both 10Base-T and 100Base-TX. These are current drivers and need to be terminated by 100Ω resistor in parallel.
TPIP, TPIN	IA	TWISTED PAIR INPUT POSITIVE, NEGATIVE: Receiver outputs for both 10Base-T and 100Base-TX.
RIBB		BIAS CURRENT SETTING RESISTOR: To be tied to an external 10 kΩ (1%) resistor which is connected to analog ground at the other end.
RITX		UTP OUTPUT DRIVE CURRENT SETTING RESISTOR: To be connected to an external 10 kΩ resistor (1%). This can be adjusted so as to compensate for insertion loss of the TX transformer.

LED INDICATORS

$\overline{\text{LEDL}}$	OD8	LED LINK: ON for link up.
$\overline{\text{LEDTX}}$	OD8	LED TRANSMIT: Blinks-ON when there is a transmission (normally OFF).
$\overline{\text{LEDRX}}$	OD8	LED RECEIVE: Blinks-ON when there is a reception (normally OFF).
$\overline{\text{LEDCF}}$	OD9	LED COLLISION/FULL DUPLEX: In half duplex mode, this is a collision LED indicator and it blinks-ON (normally OFF) when a collision occurs. In full duplex mode, the LED is ON all the time.
$\overline{\text{LED}}100\overline{\text{X}}$	OD8	LED 100BASE-X: ON for 100Base-TX connection and OFF for other connections.

PIN DESCRIPTION (continued)

OSCILLATOR/CLOCK

NAME	TYPE	DESCRIPTION
XTAL1, XTAL2		CRYSTAL 1.2: Connect 25 MHz crystal oscillator to XTAL1 and XTAL2, or drive XTAL1 from a 25 MHz oscillator module.

POWER SUPPLY

VPA; VPB;	S	VOLTAGE POSITIVE: A: Analog; B: Transmit Driver; C: Digital Core; VPC; VPD D: Digital I/O. Dual voltages are supported: 5V ± 5%, or 3.3V ± 0.3V.
VNA; VNB;	S	VOLTAGE NEGATIVE: A: Analog; B: Transmit Driver; C: Digital Core; D: Digital VNC; VND; VNQ I/O: Q: Quiet (for substrate tie).

MISCELLANEOUS PINS

CP	O4	CONTROL PIN: This pin is a general purpose output control pin which is controlled by bit MR16.6, CB. CB low will drive CP low and CB high will drive CP high.

TEST PINS

TVCO	OA	TRANSMIT VCO CONTROL VOLTAGE
RVCO	OA	RECEIVE VCO CONTROL VOLTAGE
BLW	OA	BASELINE WANDER CONTROL VOLTAGE
EQR	OA	EQUALIZER CONTROL VOLTAGE
TEST	I	TEST: Strapped to logic low for normal operation.
Other		

LEGEND

TYPE	DESCRIPTION
IA	Analog Input
I	Input (TTL level)
S	Supply
OA	Analog Output
O4	Output with I_{OL} = 4 mA @ 3V
OD8	Output Open Drain with I_{OL} = 8 mA @ 3V

ELECTRICAL SPECIFICATIONS

The following electrical specifications assume proper termination of input and output ports, and nominal connection to transmit and receive isolation transformers.

TRANSMITTER (100BASE-TX)

PARAMETER	CONDITION	MIN	NOM	MAX	UNIT
Differential Output Signal (0 Vp-p)		950		1050	mV
Signal Amplitude Symmetry		98		102	%
Rise and Fall Time		3.0		5.0	ns
Rise and Fall Time Imbalance				0.5	ns
Duty Cycle Distortion (Vp-p)				0.5	ns
Output Jitter (Vp-p)				1.4	ns
Signal Amplitude Overshoot				5	%

RECEIVER (100BASE-TX)

Input Common-Mode Signal (Vp-p)	0 - 125 MHz			2.5	V
Input Squelched Threshold (Vp-p)		600	800	1000	mV
Input Unsquelched Threshold (Vp-p)		200	300	400	mV
PLL Locking Time				800	µs
Diff Input Amplitude Range (0 Vp-p)		0.1		1.5	V
Bit Error Ratio			10^{-10}		

10BASE-T

Output Current		44	48	56	mA
Input Squelched Threshold (0 Vp-p		300	400	585	mV
Input Unsquelched Threshold (0 Vp-p)			150		mV
Diff Input Resistance					kΩ
Open Circuit Input Voltage (Bias)					V
Diff Input Amplitude Range (0 Vp-p)					mV

Advance Information: Indicates a product still in the design cycle, and any specifications are based on design goals only. Do not use for final design.

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SSI 78Q2121
100Base-TX
Fast Ethernet Transceiver
Preliminary Data

March 1996

DESCRIPTION

The SSI 78Q2121 is a 100Base-TX Fast Ethernet transceiver with integrated transmit and clock recovery PLLs. The device interfaces directly to the DEC 21140 controller chip and alike, which has integrated 100Base-TX PCS functions, through a 15-bit 5B symbol interface. The transmitter includes on-chip pulse-shaper and a low power line driver, while the receiver has a sophisticated combination of AGC, real-time adaptive equalizer, and adaptive DC offset adjustment circuit to provide the best combination of ISI cancellation and baseline wander correction required for accurate clock and data recovery. The transceiver is used at the interface to Cat 5 UTP cabling, and is connected to the line media via simple 1:1 isolation transformers. No external filter is required.

The 78Q2121 is built in BiCMOS technology for high performance and low power operation, and can operate from a single 3.3V or 5V supply.

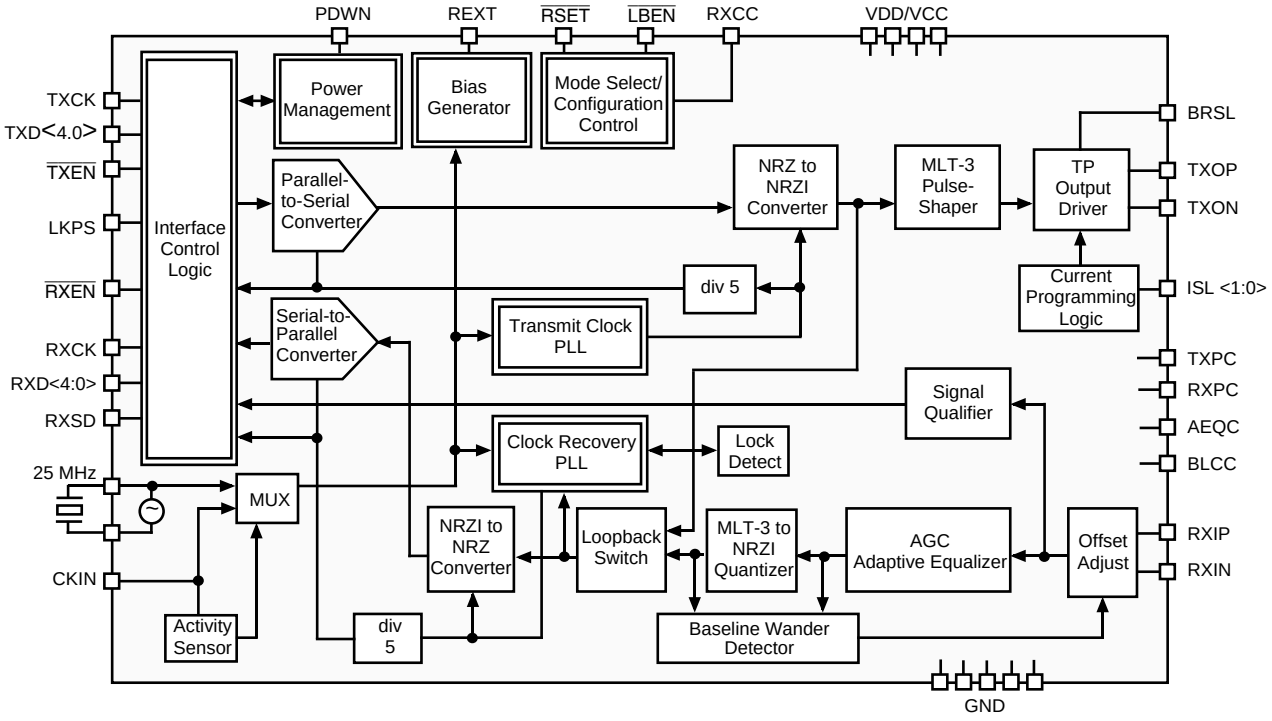
FEATURES

GENERAL

- **IEEE-802.3u compliant 100Base-TX TP-PMD transceiver for Cat 5 UTP cable**
- **Integrated transmit and clock-recovery PLLs**
- **Integrated power-on reset**
- **Supports full-duplex operation**
- **Internal loopback mode**
- **Chip power-down mode**
- **Automatic sensing of supply voltages**
- **Low power design with advanced power management**
- **Advanced BiCMOS technology in a 48-Lead TQFP package**

(continued)

BLOCK DIAGRAM



FUNCTIONAL DESCRIPTION

GENERAL

Supply Voltage

The 78Q2121 can operate from a single 3.3V (± 0.3V) or 5V (± 5%) power supply. Detection of supply voltage is automatic. In the case when both 3.3V and 5V supplies are available, the 5V supply can be used to power the transmit line driver, with 3.3V supplying to the rest of the on-chip circuitry. This combination allows the use of a non center-tapped transmit transformer, thereby allowing line output drive current to be halved without sacrificing performance. This mode allows the most power efficient operation, and is selected when BRSL pin is tied high. Note that this feature is disabled when only 3.3V supply is used.

Clock Selection

The 78Q2121 will default to use the internal crystal oscillator upon power-on. If this is the desired mode of operation, the CKIN pin should be tied low. If the chip is required to use an external 25 MHz clock, connect the external clock to the CKIN pin. The chip will sense the activity on the CKIN pin, and will automatically configure itself to use the external clock instead. In this mode of operation, a crystal is not required. When no crystal is present, the XTLP and XTLN pins should be left unconnected.

Power Management

The 78Q2121 has two power saving modes:

• Chip Power-Down

• Receive Power Management

Chip power-down is activated by enabling the PWDN pin. When the chip is in power-down mode, all on-chip circuitry are shut off, and the device consumes minimum power. When power-down is deactivated, a reset pulse should be applied to restore the chip to its initial power-on state. Note that power-on-reset is activated only upon initial start-up, and is unaffected by chip power-down.

Receive power management is activated by asserting the RXCC pin. In this mode of operation, the clock recovery PLL, and other respective receive circuitry, will be powered down whenever no valid signal is present at all the receive line interface pins.

FEATURES (continued)

- 3.3V or 5V operation with optional dual-supply mode for minimum power consumption

SYM INTERFACE

- 5B NRZ symbol interface connects directly to controller chips with integrated 100Base-TX PCS functions
- Signal detect pin asserted as soon as recovered clock is locked onto receive data
- Receive data automatically blanked out when signal detect is inactive
- Receive clock configurable to be either active or inactive when signal detect is disasserted
- TTL compatible input
- Transmit and receive output pins can be tristated independently

CLOCK GENERATION/RECOVERY

- Generates 125 MHz transmit clock from either external 25 MHz clock source or internal crystal oscillator
- Automatic detection of external clock input
- Advanced lock detection circuit minimizes acquisition time and provides fast lock indication
- Receive clock automatically references to transmit clock when no receive signal is present

LINE DRIVER/RECEIVER

- Built-in transmit pulse-shaper, no external filter required
- Programmable output drive current
- Automatic receive gain and real-time adaptive equalization
- Adaptive baseline wander correction
- Built-in signal qualifier (detector) with ‘smart’ squelch feature
- Line input and/or output pin become high-Z when receive and/or transmit function is disabled respectively, allowing parallel connection of similar PMD devices

As soon as a valid signal is detected, all circuits will automatically be powered up to resume normal operation. Note that RXCK will be inactive when the clock recovery PLL is in power-down state.

Loopback Mode

Digital loopback mode can be enabled through the $\overline{\text{LBEN}}$ pin. This mode allows transmit NRZI bit stream to be looped back to the receive side prior to entering the pulse-shaper and line driver. The loopback data is subsequently re-timed by the clock recovery PLL and re-presented to the receive SYM interface. During loopback, the line transmit pins are tristated, and any data presented to the receive port is ignored.

SYM INTERFACE

The SYM interface is a 15-bit TTL compatible interface composed of two parts:

- Transmit: transmit data (TXD<4:0>)
  transmit clock (TXCK)
  transmit enable ($\overline{\text{TXEN}}$)
- Receive: receive data (RXD<4:0>)
  receive clock (RXCK)
  receive signal detect (RXSD)
  receive enable ($\overline{\text{RXEN}}$)

Transmit

The 5-bit transmit data symbols are clocked in on every rising edge of TXCK. TXCK is a continuous 25 MHz clock referenced to either the internal crystal oscillator or the externally applied clock depending on the mode of operation. However, if the latter mode is used, absolute phase relation between TXCK and CKIN is not guaranteed.

The 5-bit data symbols are concatenated and presented to the analog transmitter as a 125 MHz bit stream, with TXD4 being the first bit to be transmitted, and TXD0 being the last. When $\overline{\text{TXEN}}$ is high, the transmit clock is disabled and TXCK pin becomes high impedence.

Receive

Data recovered from the line media is concatenated to groups of 5-bit symbols, with RXD4 being the first received bit, and RXD0 being the last. These symbols are clocked out to the PCS on the falling edge of the recovered 25 MHz clock (RXCK). RXCK can be pin configured to be either active or inactive when the signal detect pin (RXSD) is not asserted. If the former is selected, RXCK is continuously active. It is phase-locked to the receive data when RXSD is asserted, and is derived from the transmit clock when RXSD is disasserted. If the latter mode is selected, RXCK remains low whenever RXSD is not asserted.

RXSD is asserted as soon as the receive data is locked in and the recovered clock frequency is within 1% of the actual data-rate frequency. RXSD is disasserted when more than 150 consecutive bits of zeros are received. When RXSD is not asserted, all-zero data will appear on the RXD data bus. Note that data on the RXD bus is not aligned to symbol boundaries. When $\overline{\text{RXEN}}$ is high, all receive interface pins are tristated, allowing other chips to drive the MII/SYM signal lines.

TRANSMITTER

The transmit section of the chip contains all necessary circuitry to convert pre-scrambled, 5-bit NRZ symbol data from the PCS to an IEEE-802.3u compliant data-stream driving a pair of Cat-5 UTP cable.

The transmit section consist of three major blocks:

- Transmit PLL
- Pulse-Shaper
- Line Driver

Transmit PLL

The transmitter uses an on-chip low-jitter PLL synthesizer to generate the 125 MHz transmit clock. This PLL locks either to the local 25 MHz crystal oscillator, or the externally applied clock, depending on the mode of operation.

Pulse-Shaper

The pulse-shaper uses a sophisticated current modulation scheme to produce the desired output waveform. Controlled rise/fall time is achieved using accurately controlled C/I filter, and MLT-3 waveforms are generated through current modulation, allowing average drive current to be effectively halved compared to conventional approach.

FUNCTIONAL DESCRIPTION (continued)

Line Driver

The line driver is closely mingled with the pulse-shaper, combined to ensure the output waveform is sufficiently pulse-shaped to exceed FCC requirements. The 78Q2121 allows for programmable output drive current to compensate for insertion losses of various external magnetic modules. Output drive current can be set from 100% to 140% by pin selection through ISL<1:0> pins.

The line driver requires an external 1:1 isolation transformer to interface with the line media. For 3.3V operation, the transformer should be center-tapped to Vcc. In this mode, the transformer efficiency is 50%, and a nominal peak drive current of 40 mA is required. If a 5V supply is available to power the line driver (VPB pin), the advanced on-chip bridge driver can be activated to minimize power consumption.

In this mode, a non center-tapped transformer is used, and the required peak drive current is reduced to 20 mA. This power-saving mode is selected when BRSL pin is tied high. When $\overline{\text{TXEN}}$ is high, the line driver is disabled and the line transmit pins become high-impedence.

RECEIVER

The receive section contains three major blocks:

- Adaptive Equalizer/Baseline Wander Corrector
- Signal Qualifier
- Clock Recovery PLL

Adaptive Equalizer/Baseline Wander Corrector

On the receive side, a data signal from up to 100m of Cat-5 UTP cable enters the chip through a transformer. This signal goes through a combination of adaptive offset adjustment (baseline wander correction), automatic gain, and adaptive equalization. The effect of these circuits is to sense the amount of dispersion, distortion and attenuation caused by the cable and transformer, and restore the received pulses to logic levels. The amount of gain and equalization applied to the pulses varies with the detected attenuation and dispersion and, therefore, with the length of the cable. The equalized MLT-3 data signal is decoded and quantized through analog receivers. The recovered bit-stream is then presented the Clock Recovery PLL for clock acquisition.

Signal Qualifier

The integrated signal qualifier has separate squelched and unsquelched thresholds, and includes a built-in timer to ensure fast and accurate receive signal detection. Upon detection of two or more valid pulses on the line receive port, the pass indication, indicating the presence of valid receive signals, will be asserted. When pass is asserted, the signal detect threshold is lowered by about 60%, and all adaptive circuits are released from their quiescent operating conditions, allowing them to lock onto the incoming data. When no signal is presented for a period of about 1.2 μs, the pass indication will be disasserted, and the signal detect threshold will return to the squelched level. RXSD on the SYM interface is asserted if and only if pass is active and the recovered clock frequency is within 0.1% of the actual data-rate frequency.

Clock Recovery PLL

The 125 MHz receive clock is extracted using a low-jitter PLL. The AC coupled phase detector ensures that clock skew is minimized during periods when data transition density is low. When no receive signal is present, the PLL is directed to lock onto the transmit 125 MHz clock. When pass is asserted, the PLL will use the received NRZI signal as the clock reference. The recovered clock is used to re-time the data signal and, subsequently, converting the data to NRZ format.

BIASING

The 78Q2121 uses the reference clock to generate accurate bias voltages for setting the various precision circuitry on chip. This technique allows rise and fall times of transmit pulses to be controlled accurately, and also allows center frequencies of the two on-chip VCOs to be set precisely. All these are achieved without trimming or precision external components which are typical in other ICs requiring precision timing. The ability to set accurate center frequencies allow the use of narrow-band PLL circuits without the requirement of complex frequency discrimination circuits to aid clock acquisition. Only one external resistor is required for generating various precision bias currents for the bipolar circuits.

PIN DESCRIPTION

Note Abbreviations: S = Supply; IT = TTL Input; O4 = Output with I_{OL} = 4 mA @ Vcc = 3.3V or I_{OL} = 8 mA @ Vcc = 5.0V; A = Analog; IA = Analog Input; OA = Analog Output

NAME	TYPE	DESCRIPTION
VPA	S	Analog Supply
VNA	S	Analog Ground
VPB	S	Transmit Analog Supply
VNB	S	Transmit Analog Ground
VPC	S	CMOS Logic Supply
VNC	S	CMOS Logic Ground
VPD	S	Digital I/O Supply
VND	S	Digital I/O Ground
VNS	S	Substrate Ground
TXCK	O4	Transmit Clock
TXD[4:0]	IT	Transmit Data
$\overline{\text{TXEN}}$	IT	Transmit Enable
RXCK	O4	Receive Clock
RXD[4:0]	O4	Receive Data
RXSD	O4	Receive Signal Detection
$\overline{\text{RXEN}}$	IT	Receive Enable
LKPS	O4	Lock/Pass Indication
TXOP	OA	Transmit UTP Output +
TXON	OA	Transmit UTP Output -
RXIP	IA	Receive UTP Input +
RXIN	IA	Receive UTP Input -
CKIN	IT	External 25 MHz Clock
XTLP	A	25 MHz Crystal Pin +
XTLN	A	25 MHz Crystal Pin -
REXT	A	Bias Current Reference Resistor Pin
$\overline{\text{RSET}}$	IT	Chip Reset
$\overline{\text{LBEN}}$	IT	Loopback Enable
TSA0	IT	Test pin used by factory, leave open
TSA1	IT	Test pin used by factory, leave open
TSA2	IT	Test pin used by factory, leave open

PIN DESCRIPTION (continued)

Note Abbreviations: S = Supply; IT = TTL Input; O4 = Output with I_{OL} = 4 mA @ Vcc = 3.3V or I_{OL} = 8 mA @ Vcc = 5.0V; A = Analog; IA = Analog Input; OA = Analog Output

NAME	TYPE	DESCRIPTION
PDWN	IT	Chip Power-Down
ISL[1:0]	IT	Transmit Line Drive Current Selection
BRSL	IT	Bridge Driver Selection
RXCC	IT	Receive Power Management Enable
AEQC	A	Adaptive Equalizer Filter Voltage
BLCC	A	Baseline Corrector Filter Voltage
TXPC	A	Transmit PLL Filter Voltage
RXPC	A	Clock Recovery PLL Filter Voltage

CONFIGURATION CONTROL

The following section assumes the following:

Pin connection: H = Vcc; L = Gnd; Power Supply: 3.3V => 3.3 ± 0.3V; 5V => 5V ± 5%

SUPPLY VOLTAGE SELECTION

VNA = VNB = VNC = VND = VNS = Gnd

a) 5V only: VPA = VPB = VPC = VPD = 5V

b) 3.3V only: VPA = VPB = VPC = VPD = 3.3V

c) Dual Voltage mode: VPA = VPC = VPD = 3.3V; VPB = 5V

RECEIVE POWER MANAGEMENT MODE SELECTION

RXCC = H: Receive Power Management active (LKPS = pass)

= L: Receive Power Management inactive (LKPS = lock)

NOTE: pass = Signal Qualifier pass indication; lock = Clock Recovery PLL lock indication

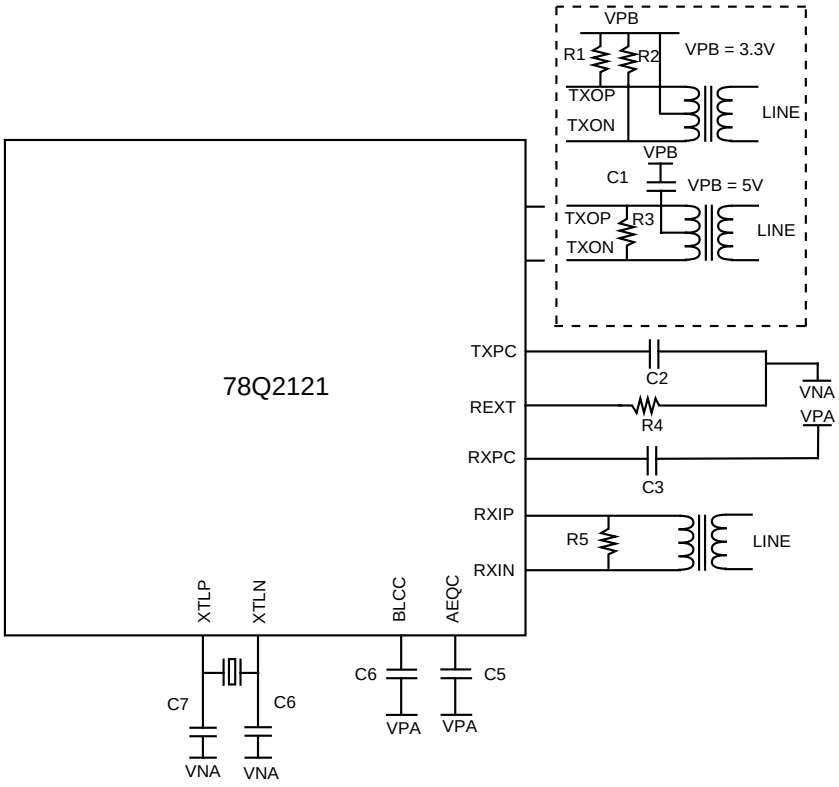
TRANSMIT LINE DRIVE CURRENT SELECTION

Select drive current based on insertion loss specification on line transformer.

ISL<1:0>	DRIVE CURRENT	INSERTION LOSS
00	100%	0.0 - 0.5 dB
01	110%	0.5 - 1.3 dB
10	120%	1.3 - 2.0 dB
11	140%	2.5 - 3.4 dB

EXTERNAL COMPONENTS

The chip requires a few external passive components to function properly. These components, with their recommended values, are shown below:



NAME	FUNCTION	VALUE	TOLERANCE	NOTE
R1	Back termination	50Ω	5%	For BRSL = L only
R2	Back termination	50Ω	5%	For BRSL = L only
R3	Back termination	100Ω	5%	For BRSL = H only
R4	Current setting	9.8 kΩ	1%	
R5	Line termination	100Ω	5%	
C1	Common-mode suppression	0.1 µF	20%	optional
C2	Transmit PLL filter	25 pF	20%	optional
C3	Receive PLL filter	25 pF	20%	optional
C4	Adaptive equalizer filter	10 pF	20%	optional
C5	Baseline corrector filter	5 pF	20%	optional
C6,C7	Crystal load capacitors	20 pF	10%	

EXTERNAL COMPONENTS (continued)

ISOLATION TRANSFORMERS

Two simple 1:1 isolation transformers are all that is required at the line interface, but transformers with integrated common-mode choke are recommended for exceeding FCC requirements. The line transformers should have the following characteristics:

NAME	VALUE	CONDITION
Turns Ratio	1 CT : 1 CT ± 5%	
Open-Circuit Inductance	350 µH (min)	@ 10 mV, 10 kHz
Leakage Inductance	0.40 µH (max)	@ 1 MHz (min)
Inter-Winding Capacitance	12 pF (max)	
DC Resistance	0.9Ω (max)	
Insertion Loss	1.1 dB (typ)	0 - 100 MHz
HIPOT	1500 Vrms	

NOTE: For the line transmit transformer, insertion loss up to 3.4 dB can be tolerated due to the programmability of the output drive current.

For the line receive transformer, OCL can be as low as 100 µH since the baseline wander correction circuit will be able to track the transformer droop.

REFERENCE CRYSTAL

If internal crystal oscillator is to be used, a crystal with the following characteristics should be chosen:

NAME	VALUE	UNITS
Frequency	25.00000	MHz
Load Capacitance	15	pF
Frequency Tolerance	±20	PPM
Aging	±2	PPM/yr
Temperature Stability (0 - 70°C)	±5	PPM
Oscillation Mode	Fundamental	
Parameters at 25°C ± 2°C; Drive Level = 0.5 mW		
Shunt Capacitance (max)	8	pF
Motional Capacitance (min)	10	ƒF
Series Resistance (max)	25	Ω
Spurious Response (max)	> 5 dB below main within 500 kHz	

ELECTRICAL SPECIFICATIONS

Operating Temperature Range: 0 - 70°C

DC ELECTRICAL CHARACTERISTICS

The following ratings assumes the nominal ISL setting of <00>

CHARACTERISTICS		CONDITION	MIN	NOM	MAX	UNIT
Supply Voltage	V_{CC}	V_{CC} = 3.3V V_{CC} = 5.0V	3.0 4.75		3.6 5.25	V V
TTL Input Voltage Low	V_{IL}	V_{CC} = 5.0V			0.8	V
TTL Input Voltage High	V_{IH}	V_{CC} = 5.0V	2.0			V
TTL Output Voltage High	V_{OH}	I_{OH} = 4.0 mA, Vcc = 3.0V	2.4			V
TTL Output Voltage Low	V_{OL}	I_{OL} = 4.0 mA, Vcc = 3.0V			0.4	V
Power-Down current	I_{PDN}				500	µA
Core Supply Current	I_{DDC}			35	50	mA
Line Driver Supply Current (average)	I_{DDB}	BRSL = L BRSL = H		20 10	25 12	mA mA
Total Supply Current (average)	$I_{DDT(AV)}$	BRSL = L BRSL = H		55 45		mA mA

ANALOG ELECTRICAL CHARACTERISTICS

The following electrical specifications assume proper termination of input and output ports and nominal connection to transmit and receive isolation transformers.

Unless otherwise stated, ISL setting is assumed to be <00> {default}.

TRANSMITTER

PARAMETER	CONDITION	MIN	NOM	MAX	UNIT
PLL Locking Time			3		µs
Output Jitter (Vp-p)				1.4	ns
Duty Cycle Distortion (Vp-p)				0.5	ns
UTP Pulse Rise/Fall Time			4		ns
UTP Rise/Fall Time Imbalance			±0.5		ns
Differential Output Signal (0-pk)	R_{load} = 50 Ω	950		1050	mV
Signal Amplitude Symmetry			± 2		%
Signal Amplitude Overshoot			3		%
Peak Output Drive Current	BRSL = L BRSL = H	38 19		42 21	mA mA
Peak Output Current Range	Nominal	100		140	%

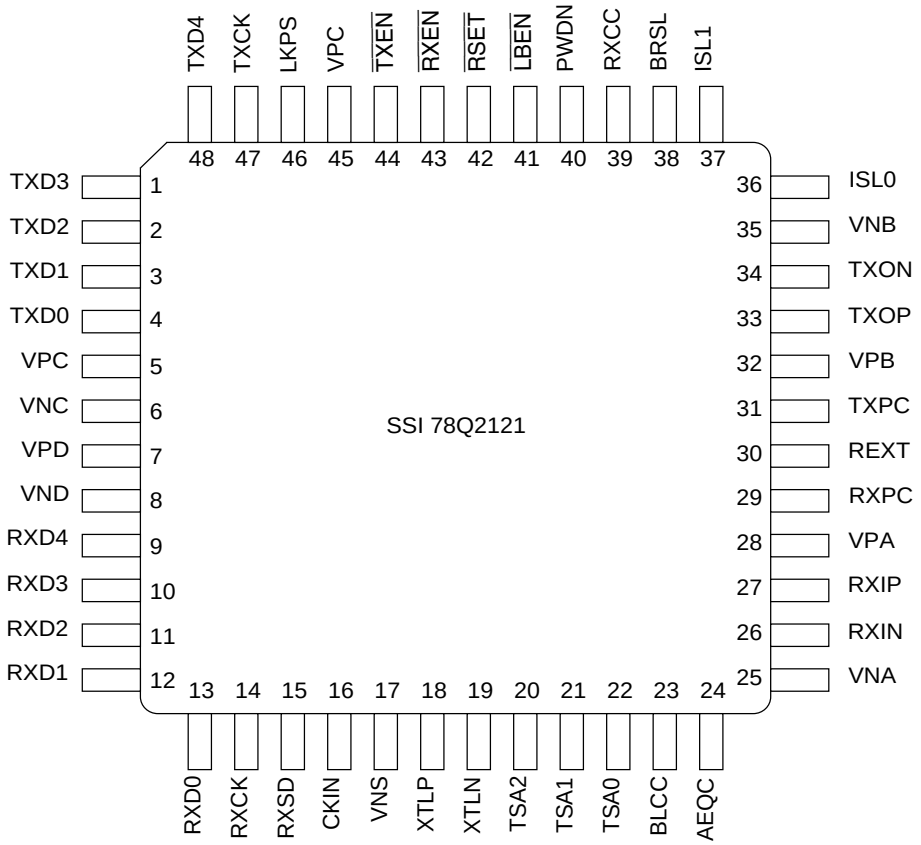
ELECTRICAL SPECIFICATIONS (continued)

RECEIVER

PARAMETER	CONDITION	MIN	NOM	MAX	UNIT
PLL Locking Time			2		µs
Jitter Tolerance			4.0		ns
Bit Error Ratio			10^{-10}		
Input Amplitude Range (0-pk)				1.2	V
Baseline Wander Tracking		-75		+75	%
Input Bias Level		Vcc - 0.5		Vcc	V
Input Squelched Threshold (Vp-p)		600	800	1000	mV
Input Unsquelched Threshold (Vp-p)		200	300	400	mV
Signal Detect Assertion Time				200	µs
Signal Detect De-assertion Time				1.4	µs

PACKAGE PIN DESIGNATIONS

(Top View)



48-Lead TQFP

CAUTION: Use handling procedures necessary for a static sensitive component.

ORDERING INFORMATION

PART DESCRIPTION	ORDER NUMBER	PACKAGE MARK
SSI 78Q2121 48-lead TQFP	78Q2121-CGT	78Q2121-CGT

Preliminary Data: Indicates a product not completely released to production. The specifications are based on preliminary evaluations and are not guaranteed. Small quantities are available, and Silicon Systems should be consulted for current information.

Silicon Systems, Inc., 14351 Myford Road, Tustin, CA 92680-7022 (714) 573-6000, FAX (714) 573-6914

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A TDK Group Company

SSI 78Q8392L
Low Power Ethernet Coaxial Transceiver

January 1996

DESCRIPTION

The SSI 78Q8392L Ethernet Transceiver is a low power BiCMOS coax line transmitter/receiver. The device includes analog transmit and receive buffers, a 10 MHz on-board oscillator, timing logic for jabber and heartbeat functions, output drivers and bandgap reference, in addition to a current reference and collision detector.

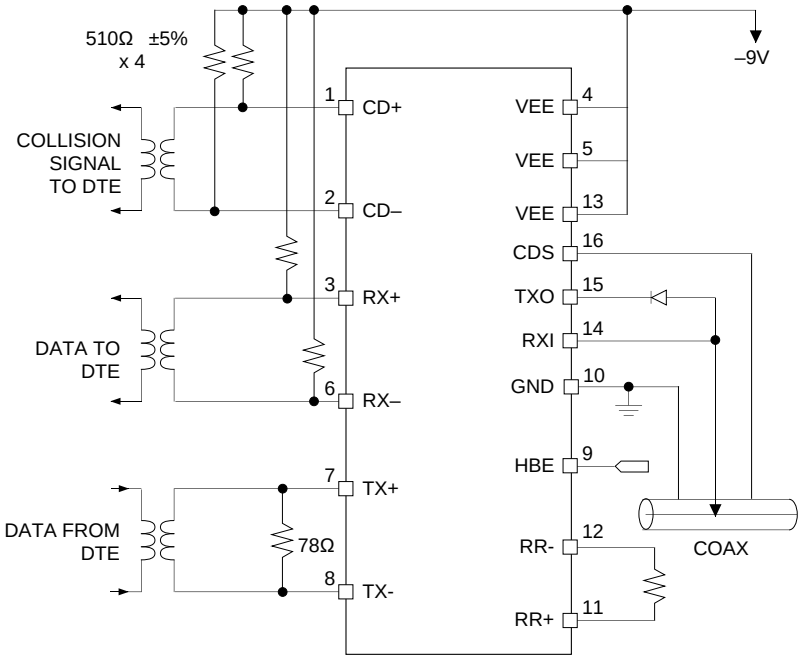
This transceiver provides the interface between the single-ended coaxial cable signals and the Manchester-encoded differential logic signals. Primary functional blocks include the receiver, transmitter, collision detection and jabber timer. This IC may be used in either internal or external MAU environments.

The SSI 78Q8392L is available in 16-pin plastic and 28-pin PLCC packages.

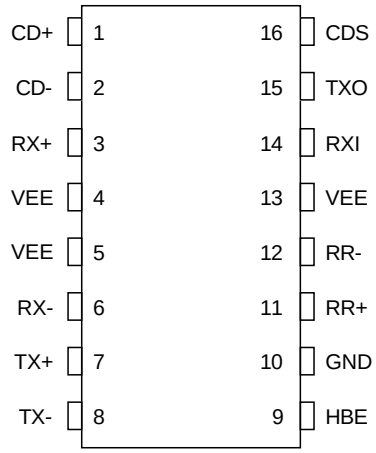
FEATURES

- **Very low power consumption**
- **Compliant with Ethernet II, IEEE 802.3 10Base5 and 10Base2**
- **Integrates all transceiver functions except signal and power isolation**
- **Innovative design minimizes external components count and power consumption**
- **Jabber timer function integrated on chip**
- **Externally selectable CED heartbeat allows operation with IEEE 802.3 compatible repeaters**
- **Squelch circuitry at all inputs rejects noise**
- **Power-on reset and test modes**
- **Advanced BiCMOS process.**

SSI 78Q8392L CONNECTION DIAGRAM



PIN DIAGRAM



16-Pin DIP

CAUTION: Use handling procedures necessary for a static sensitive component.

FUNCTIONAL DESCRIPTION

The SSI 78Q8392L incorporates six basic functions of the Ethernet Transceiver, including receiving, transmitting, collision signaling, collision detection, jabber timing, and the heartbeat function. Refer to Figure 1 for a general system block diagram.

RECEIVER FUNCTIONS

The receiver senses signals through the RXI input, which minimizes reflections on the transmission media using a low capacitance, high resistance input buffer amplifier. The CDS ground input attaches directly to the input buffer from the coaxial shield to eliminate ground loop noise.

In addition to the input buffer, the receiver data path consists of an equalizer, data slicer, receiver squelch circuitry, and an output line driver.

The equalizer improves the cable-induced jitter; the data slicer restores equalized received signals to fast transition signals with binary levels to drive the receiver line driver; and the receiver line driver drives the AUI cable through an isolation transformer that connects to the AUI interface.

Noise on the transmission media is rejected by the receiver squelch circuitry, which determines valid data via three criteria: Average DC level, pulse width and transition period. The DC voltage level is detected and compared to a set level in the receiver comparator circuit. The pulse width must be greater than 20 ns to pass the narrow pulse filter; the transition timer outputs a true level on the RX Data Valid line provided the time between transitions is less than about 200 ns. As long as a valid RXI signal is detected, the output line driver remains enabled. The transition timer disables the line driver when there are no further transitions on the data medium, and the RX+, RX- pins go to a zero differential voltage state (Figure 3).

TRANSMITTER FUNCTIONS

The transmitter data path consists of a transmit input buffer, pulse-shaping filter, transmit squelch circuitry and transmit output line driver.

The self-biasing transmit input buffer receives data through an isolation transformer and translates the AUI differential analog signal to square pulse suitable for driving the pulse shaping filter. The filter outputs a correctly shaped and bandlimited signal to the transmit output driver, which drives the transmission medium through a high impedance current source. When the transmitter is off, the capacitance of the transmit driver is isolated from the transmission media by an external diode with a low capacitance node. The shield of the transmission media serves as the ground return for the transmitter function.

A transmit squelch circuit, which consists of a pulse threshold detector, a pulse width detector, and a pulse duration timer, is used to suppress noise, as well as crosstalk on the AUI cable. The squelch circuitry disables the transmit driver if the signal at TX+ or TX- is smaller than the pulse threshold. Pulse noise is rejected by a pulse width detector that passes only pulses with durations greater than 20 ns. The pulse duration timer disables the transmit driver if no pulses are received for two-bit periods following valid pulses. At the end of a transmission, the pulse duration timer disables the transmitter and triggers the blanking timer, used to block “dribble” bits.

COLLISION DETECTION

A collision occurs when two or more transmitters simultaneously transmit on the transmission media. A collision is detected by comparing the average DC level of the transmission media to a collision threshold. The received signal at RXI is buffered and sent through a low pass filter, then compared in the collision threshold circuit. If the average DC level exceeds a collision threshold, a 10 MHz signal is output on the CD± pins.

COLLISION SIGNALING

When collision signaling is enabled, a 10 MHz signal is sent from the CD± pins through an isolation transformer to the DTE. When the function is disabled, this output goes to a zero differential state. The 10 MHz output from the CD pins indicates a collision on the transmission media, a heartbeat function, or that the transmitter is in jabber mode.

JABBER FUNCTION

When valid data on the TX± pins detected, the jabber timer is started. If there is valid data for more than 20 ns, a latch is set which disables the transmitter output and enables the 10 MHz output on the CD± pins. The latch is reset within 0.5 seconds after the valid data is removed from the transmitter input (TX±). This action resets the jabber timer and disables the 10 MHz CD output. The TX± inputs must remain inactive during the 0.5 second reset period.

HEARTBEAT FUNCTION

The 10 MHz CD outputs are enabled for about 1 µs at approximately 1.1 µs after the end of each transmission. The heartbeat signal tells the DTE that the circuit is functioning. This is implemented by starting the heartbeat timer when the valid data signal indicates the end of a transmission. This function is disabled when HBE pin is tied to VEE.

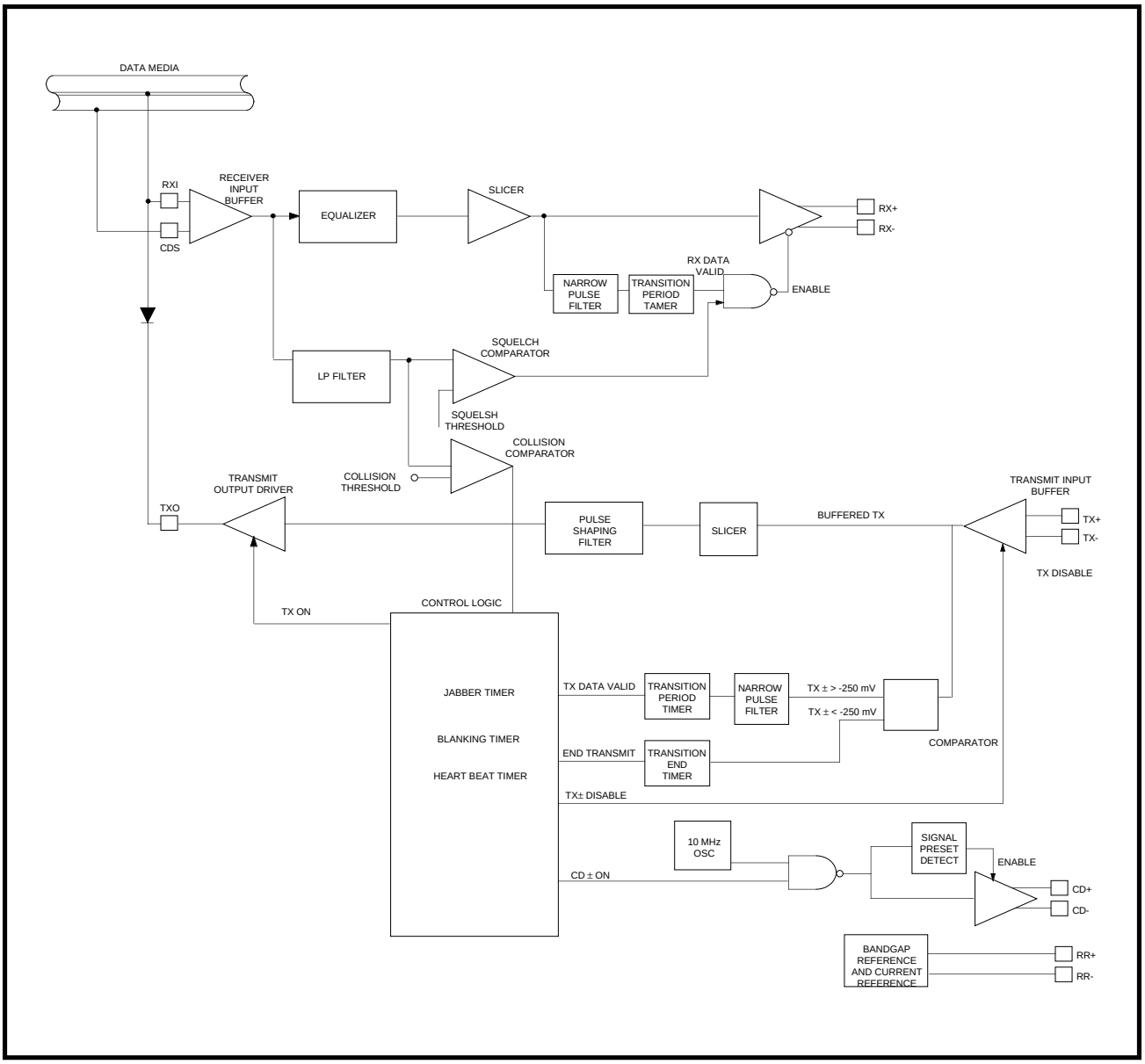


FIGURE 1: SSI 78Q8392L General System Block Diagram

PIN DESCRIPTION

NAME	TYPE	DESCRIPTION
CD+*/CD-	O	Collision Output. Balanced differential line driver outputs from the collision detect circuitry. The 10 MHz signal from the internal oscillator is transferred to these outputs in the event of collision, excessive transmission (jabber), or during CD Heartbeat condition. These outputs are open emitters; pulldown resistors to VEE are required. When operating into a 78Ω transmission line, these resistors should be 510Ω. In Cheapernet applications, where the 78Ω drop cable is not used, higher resistor values (up to 1.5k) may be used to save power.
RX+*/RX-	O	Receive Output. Balanced differential line driver outputs from the Receiver. These outputs also require 510Ω pulldown resistors.
TX+*/TX-	I	Transmit Input. Balanced differential line receiver inputs to the Transmitter. The common mode voltage for these inputs is determined internally and must not be externally established. Signals meeting Transmitter squelch requirements are waveshaped and output at TXO.
HBE	I	Heartbeat Enable. This input enables CD Heartbeat when grounded or left opened, disables it when connected to VEE.
RR+/RR-	I	External Resistor. A fixed 1 kΩ 1% resistor connected between these pins establishes internal operating currents.
RXI	I	Receive Input. Connects directly to the coaxial cable. Signals meeting Receiver squelch requirements are equalized for inter-symbol distortion, amplified, and output at RX+ and RX- pin.
TXO	O	Transmit Output. Connects via an isolation diode to the coaxial cable.
CDS	I	Collision Detect Sense. Ground sense connection for the collision detect circuit. This pin should be connected separately to the shield to avoid ground drops from altering the receive mode collision threshold.
GND	S	Positive Supply Pin.
VEE	S	Negative Supply Pins. These pins should be connected to a large metal frame area on the PC board to handle heat dissipation, and bypassed to the GND pin with a 0.1 μF capacitor as close to the package as possible.

*IEEE names for CD± = CI±, RX± = DI±, TX± = DO±

Notes: Pin type: I-input; O-output; S-power supply

ELECTRICAL SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Absolute maximum ratings indicate limits beyond which permanent damage may occur. Continuous operation at these limits is not recommended; operations should be limited to those conditions specified under recommended operating characteristics.

PARAMETER	RATING
Supply Voltage	-10V
Input Voltage	0 to V_{EE}
Storage Temperature	-65 to 150°C
Soldering (Reflow or Dip)	235°C for 10 sec
Package power dissipation	1.0 watts @ 25°C

DC OPERATING CHARACTERISTICS

0°C ≤ T (ambient) ≤ +70°C, VEE = -9V ± 5%

PARAMETER		CONDITION	MIN	NOM	MAX	UNIT
I_{EE1}	Supply current out of V_{EE} pin - non-transmitting			6	8	mA
I_{EE2}	Supply current out of V_{EE} pin - transmitting			50	65	mA
I_{RXI}	Receive input bias current (RXI)	See Note 3	-2		+25	µA
I_{TDC}	Transmit output dc current level (TXO)	See Note 4	37	41	45	mA
I_{TAC}	Transmit output ac current level (TXO)	See Notes 4 & 5	±28		I_{TDC}	mA
V_{CD}	Collision threshold (Receive mode)	See Note 9	-1.58	-1.52	-1.404	V
V_{OD}	Differential output voltage (RX±, CD±)	See Notes 3 & 7	±550		±1200	mV
V_{OC}	Common mode output voltage (RX±, CD±)	See Note 3, 6 & 7	-3.0	-2.5	-2.0	V
V_{OB}	Differential output voltage imbalance (RX±, CD±)	See Notes 3, 7 & 8			±40	mV
V_{TS}	Transmitter squelch threshold (TX±)		-200	-260	-340	mV
C_X	Input capacitance (RXI)			1.2		pF
R_{RXI}	Shunt resistance - non-transmitting (RXI)	See Note 3	100	150		kΩ
R_{TXO}	Shunt resistance - transmitting (TXO)	See Note 4	200			kΩ

DC OPERATING CHARACTERISTICS (continued)

NOTES

1. Currents into device pins are positive, currents out of device pins are negative. If not specified, voltages are referenced to ground.
2. All typicals are for VEE = -9V, Ta = 25°C.
3. -8.55V > VEE > -9.45V.
4. The voltage on TXO is -4V < V(TXO) < 0.0V.
5. The AC current measurement is referenced to the DC current level.
6. Operating or idle state.
7. Test load as shown in Figure 2.
8. Device measurement taken in idle state.
9. This threshold can be determined by monitoring the CD± output with a DC level in RXI.

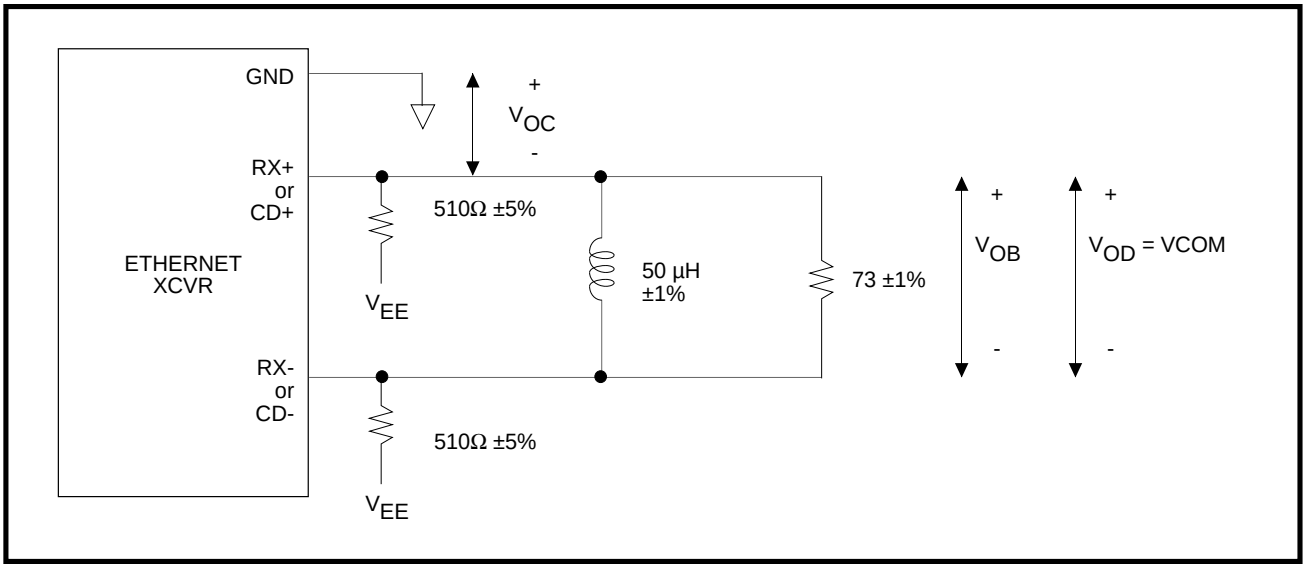


FIGURE 2: Test Load for CD± or RX±

AC OPERATING CHARACTERISTICS

0°C < T(ambient) < +70°C, VEE = 9V ± 5%

PARAMETER	CONDITION	MIN	NOM	MAX	UNIT
t_{RON} Receiver startup delay (RXI to RX±)			400	500	ns
t_{Rd} Receiver propagation delay (RXI to RX±)			10	50	ns
t_{Rr} Differential outputs rise time (RX± , CD±)			4	5	ns
t_{Rf} Differential outputs fall time (RX± , CD±)			4	5	ns
t_{RJ} Receiver & cable total jitter			2	4	ns
t_{TST} Transmitter startup delay (TX± to TXO)			100	200	ns
t_{Td} Transmitter propagation delay (TX± to TXO)			35	50	ns
t_{Tr} Transmitter rise time - 10% to 90% (TXO)		20	25	30	ns
t_{Tf} Transmitter fall time - 90% to 10% (TXO)		20	25	30	ns
t_{TM} t_{Tr} and t_{Tf} mismatch			0.5	2	ns
t_{TON} Transmit turn-on pulse width at V_{TS} (TX±)		8	20	30	ns
t_{TOFF} Transmit turn-off pulse width at V_{TS} (TX±)		140	160	180	ns
t_{CON} Collision turn-on delay			700	900	ns
t_{COFF} Collision turn-off delay				2000	ns
f_{CD} Collision frequency (CD±)		8.5	10	11.5	MHz
t_{CP} Collision pulse width (CD±)		40		60	ns
t_{HON} CD Heartbeat delay (TX± to CD±)		0.6	1	1.6	µs
t_{HW} CD Heartbeat duration (CD±)		0.6	1.0	1.5	µs
t_{JA} Jabber activation delay (TX± to TXO off and CD±)		20		60	ms
t_{JR} Jabber reset unjab time (TX± to TXO and CD±)		250	500	650	ms
t_{RO} Receive Off Pulse Width (RX+ to RX-)		200			ns

ELECTRICAL SPECIFICATIONS (continued)

TRANSMIT SPECIFICATIONS

The first bit transmitted from TXO may have data and phase violations. The second through last bit reproduce the TX± signal with less than or equal to the specified jitter.

There is no logical signal inversion between Tx± and TXO output. A low level from TX+ to TX- results in more current flowing from the coaxial cable into the TXO pin.

At the end of transmission, when the transmitter changes from the enabled state to the idle state, no spurious pulses are generated, i.e., the transition on TXO proceeds monotonically to zero current.

RECEIVE SPECIFICATIONS

The first bit sent from RX± may have data and phase violations. The second through last bit reproduce the received signal with less than or equal to the specified jitter.

There is no logical signal inversion between the RXI input and the RX± output. A high level at RXI produces a positive differential voltage from RX+ to RX-.

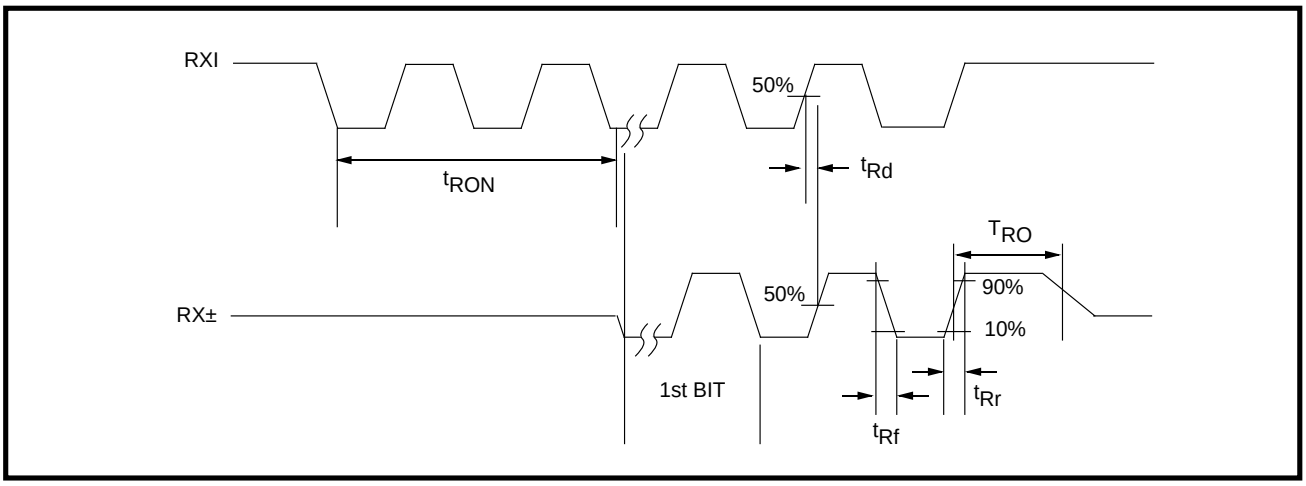


FIGURE 3: Receiver Timing

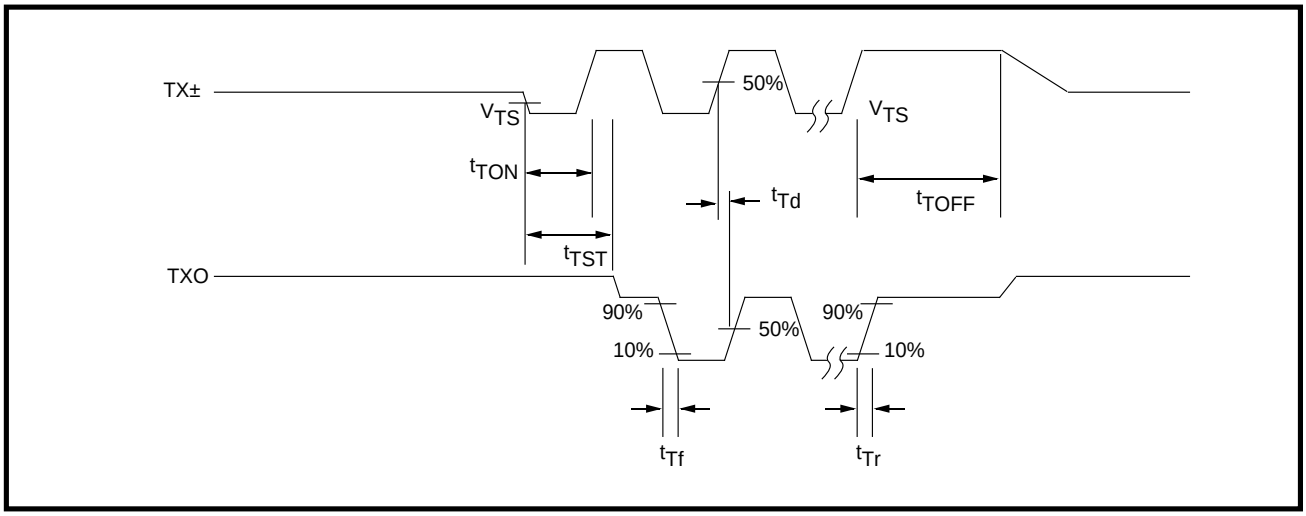


FIGURE 4: Transmitter Timing

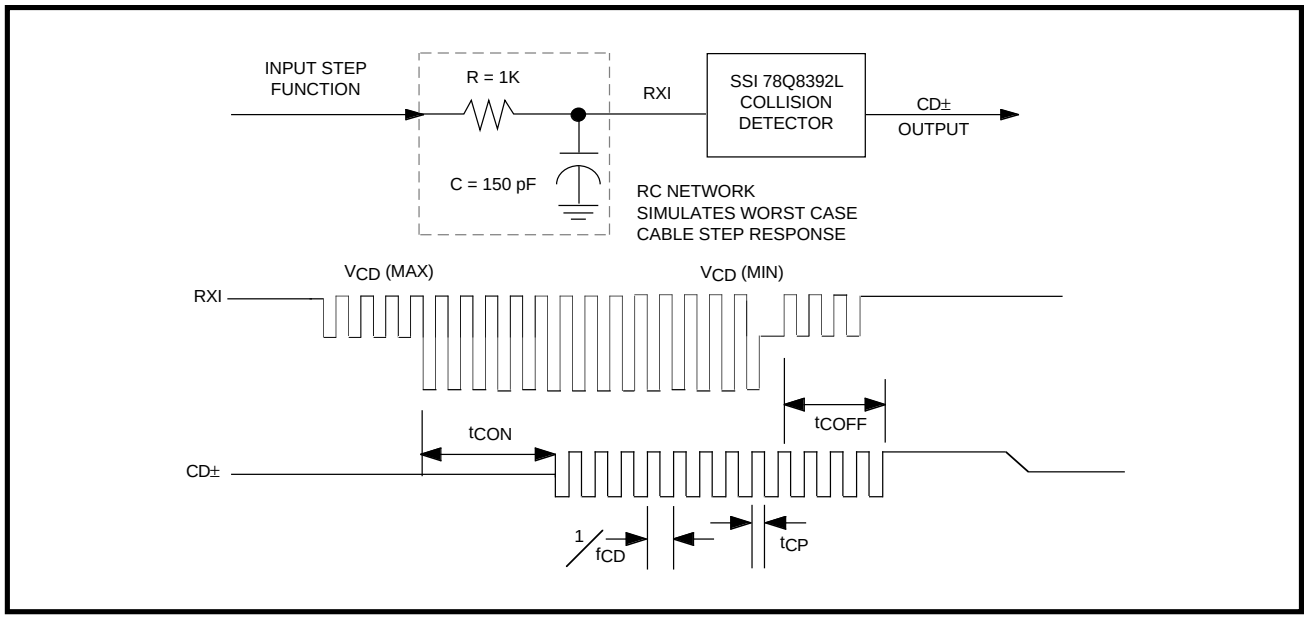


FIGURE 5: Collision Timing

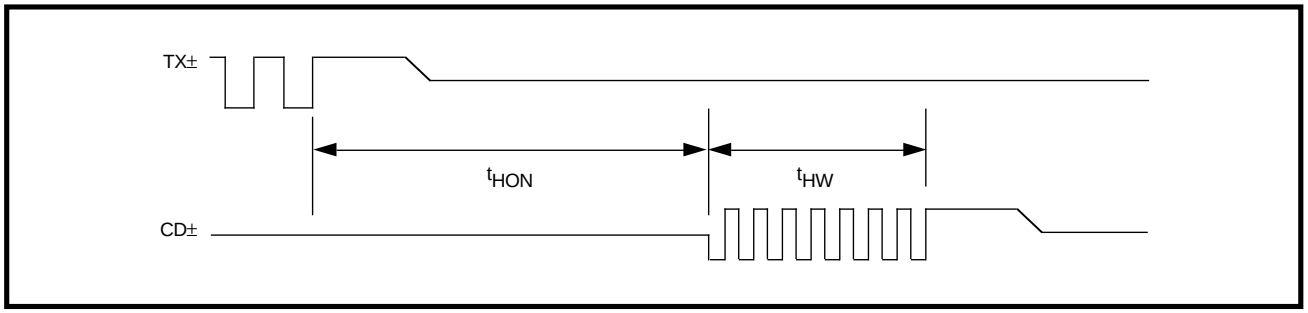


FIGURE 6: Heartbeat Timing

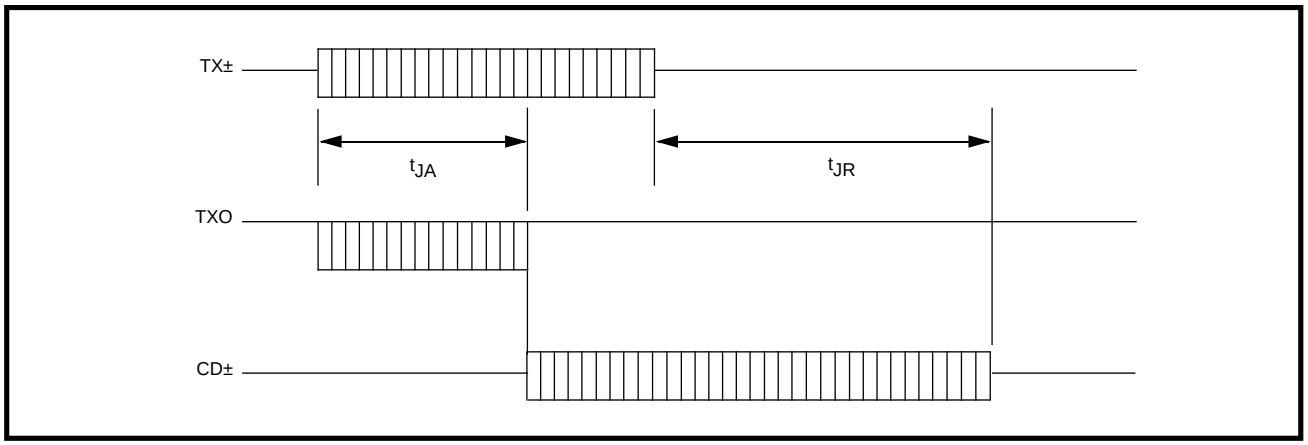


FIGURE 7: Jabber Timing

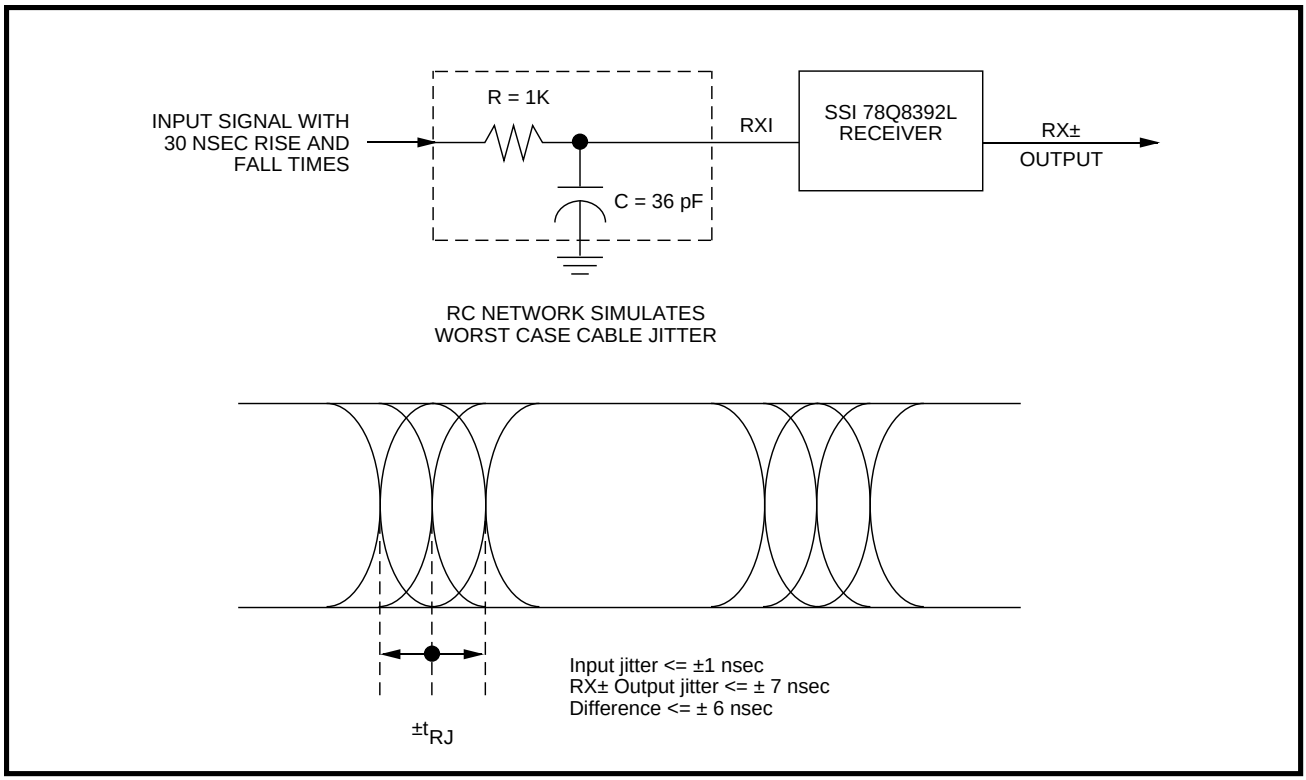


FIGURE 8: Receive Jitter Timing

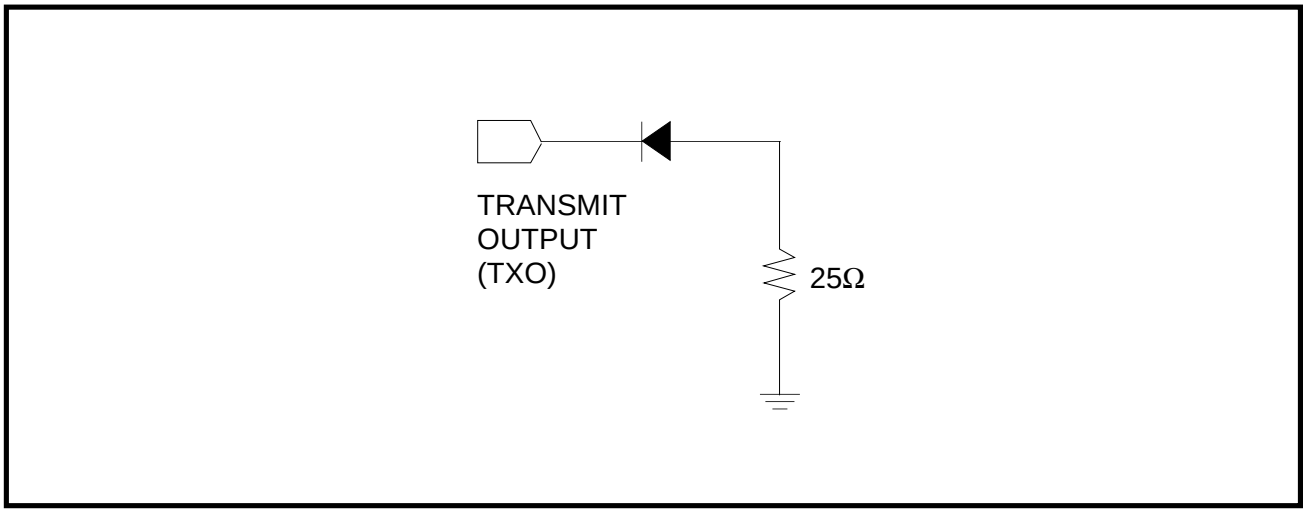


FIGURE 9: Test Loads TXO

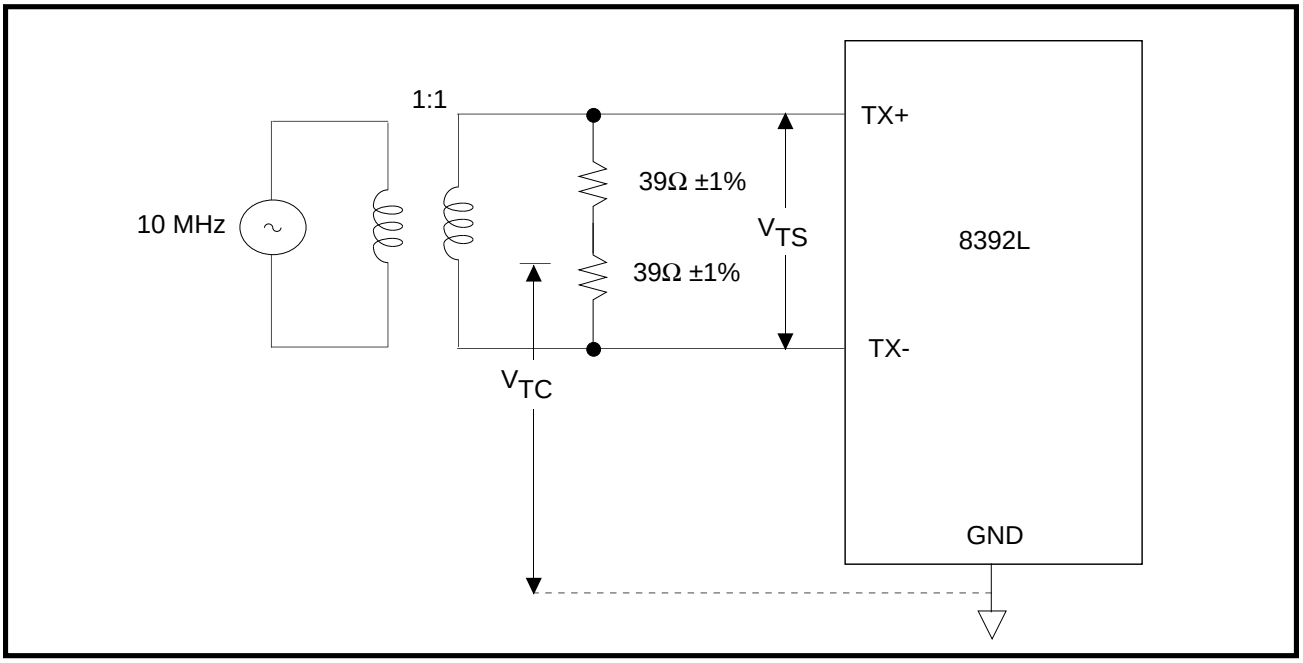
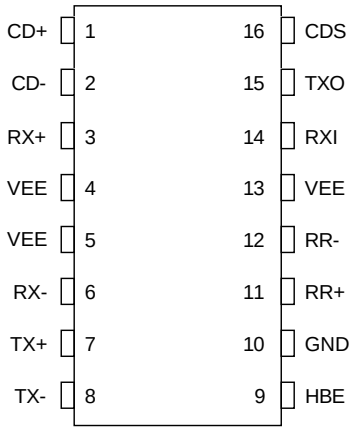


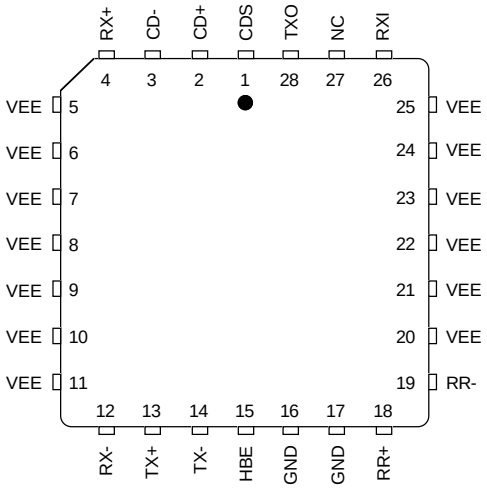
FIGURE 10: Test Circuit for TX± Input

PACKAGE PIN DESIGNATIONS

(Top View)



16-Pin DIP



28-Pin PLCC

CAUTION: Use handling procedures necessary for a static sensitive component.

ORDERING INFORMATION

PART DESCRIPTION	ORDER NUMBER	PACKAGE MARK
SSI 78Q8392L 16-Pin Plastic DIP	78Q8392L-CP	78Q8392L-CP
SSI 78Q8392L 28-Pin Plastic PLCC	78Q8392L-28CH	78Q8392L-28CH

Preliminary Data: Indicates a product not completely released to production. The specifications are based on preliminary evaluations and are not guaranteed. Small quantities are available, and Silicon Systems should be consulted for current information.

Silicon Systems, Inc., 14351 Myford Road, Tustin, CA 92680-7022 (714) 573-6000, FAX (714) 573-6914

SSI 78Q2130
10/100 BaseX Ethernet Controller for PCI and CardBus
Target Specification

February 1996

DESCRIPTION

The 78Q2130 is a 10/100 Mbit/s Ethernet LAN controller IC with bus interface logic for both Peripheral Component Interconnect (PCI) and PCMCIA Card Bus specifications. The controller can act as a bus master on the processor interface, allowing the 2130 to move receive and transmit data to and from computer memory without intervention by the processor. There are separate internal FIFOs for the transmit and receive functions which are large enough to permit full-duplex operation. Connection to the physical layer is made via standard Media Independent Interface (MII),

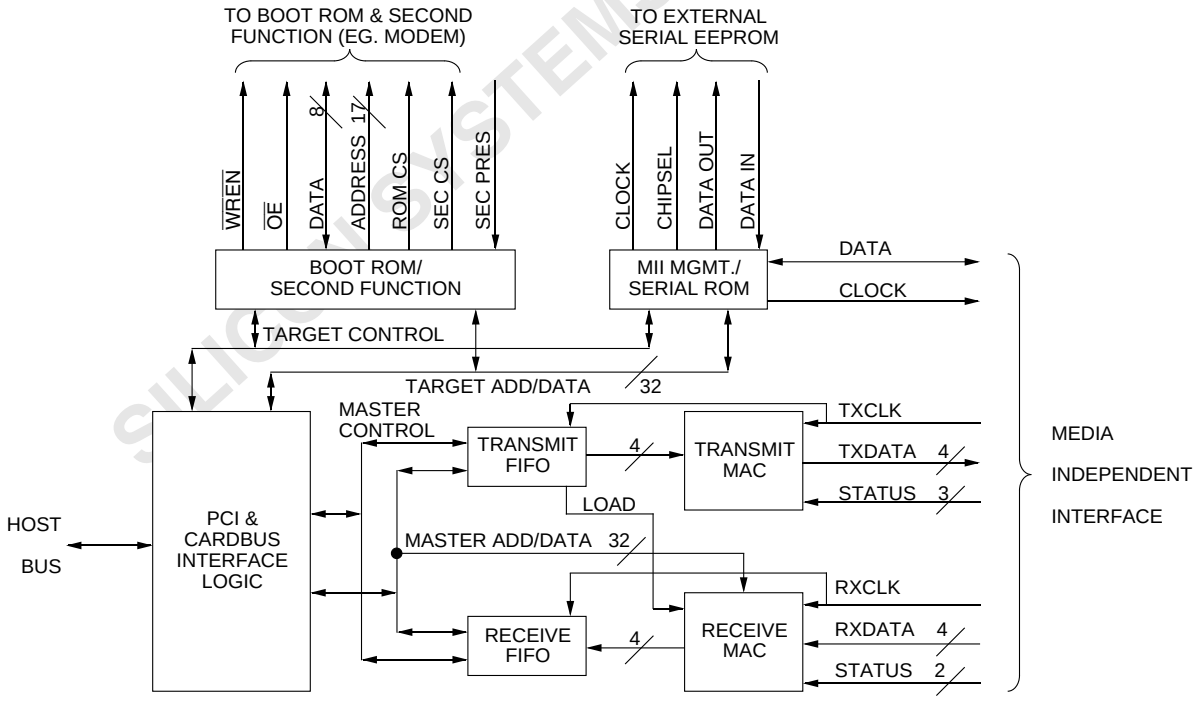
(continued)

FEATURES

- **Ethernet controller for 100 Mbit/s and 10 Mbit/s operation**
- **Integrated bus interface logic for both PCI and PCMCIA CardBus specifications with automatic selection of bus drive**
- **Fully compliant IEEE 802.3u spec for 100BaseX**
- **Connection to PHY layer via Media Independent Interface port**
- **Full-duplex operation at 10 Mbit/s and 100 Mbit/s**

(continued)

BLOCK DIAGRAM



The target specification is intended as an initial disclosure of specification goals for the product. The specifications are based on design goals, subject to change and are not guaranteed. Silicon Systems assumes no obligation regarding future manufacture unless agreed to in writing.

DESCRIPTION (continued)

allowing the use of any physical layer (PHY) devices with an MII port. An internal loopback mode allows on board testing of the chip without the need to plug into a network or network emulator.

The 2130 has an 8-bit general purpose I/O port, a serial EEPROM port and a parallel boot ROM port. The serial EEPROM port is used to support the CIS memory requirement of the CardBus specification. An external peripheral (modem, etc.) can be connected to the boot ROM port and supported by the multi-function feature of the PCI and CardBus specifications. Pin ordering on the host side of the IC is selectable for optimized interconnect with either PCI or CardBus connector. MII pins are located on the other side of the IC and allow for easy connection to that interface. The 78Q2130 is packaged in a 160-lead TQFP and can operate from either a 5V or 3.3V power supply.

FEATURES (continued)

- Enhanced Media Access Controller with optional Binary Logarithmic Arbitration Method (BLAM)
- Adjustable host interface pin order for optimal signal routing to PCI or CardBus connector
- Separate receive and transmit FIFO buffers eliminate the need for external buffer memory
- Connection to serial EEPROM for CIS memory required by CardBus
- Support for external boot ROM
- Multi-function support allows connection of an external peripheral (eg. modem)
- High-level (“intelligent”) access mode from host/driver to serial EEPROM, boot ROM and MII serial management
- Internal loopback testing mode
- Operates from either 5V or 3.3V supply
- Packaged in 160-lead TQFP

Silicon Systems, Inc., 14351 Myford Road, Tustin, CA 92680-7022 (714) 573-6000, FAX (714) 573-6914

silicon systems®
A TDK Group Company

SSI 78Q8373
3V, 5V PCMCIA Ethernet Combo

January 1996

DESCRIPTION

The SSI 78Q8373 is a highly integrated Ethernet IC for use in PCMCIA (Personal Computer Memory Card International Association) applications and can operate with a power supply of 3.3V or 5V. It contains a Media Access Controller (MAC), a 10 Mbit/s Manchester encoder/decoder (ENDEC), a 10Base-T transceiver, a memory-card bus interface (PCMCIA), and an Attachment Unit Interface (AUI). This level of integration allows the user to implement a PCMCIA card for 10Base-T using only the SSI 78Q8373, external memory, and some passive components. The internal bus interface circuit allows connection to a PCMCIA 2.1 bus without other external components. The PCMCIA bus-decoding logic can be bypassed for connection to other bus types. The SSI 78Q8373 connects to twisted-pair media via line transformers through the on-chip transceiver circuit. Connection to other media such as coaxial cable is made through the AUI port to an external transceiver, such as the SSI 78Q8392L Ethernet Coax Transceiver.

The SSI 78Q8373 has a sophisticated power management capability with three different operating modes allowing the user to maximize power savings, making it ideal for use in PCMCIA applications. During normal operation, the IC monitors its own actions and shuts down the circuits that are not being used, resulting in the lowest possible operating power. It also has a standby mode which leaves only the oscillator running, and a full shutdown mode which also turns off the oscillator.

An intelligent Buffer Manager is controlled by the host read, host write, receive and transmit pointers, and the SSI 78Q8373 manages the pointers internally without any host intervention. The device interleaves access to the buffer memory so that accesses from the host and from the network media seem to operate concurrently. Big and little endian byte orderings make for simple bus interface to all standard microprocessors.

The SSI 78Q8373 is available in a 100-lead thin QFP (TQFP) package, and can operate with a power supply of 3.3 volts or 5 volts.

FEATURES

- **Single-chip solution for 10Base-T/PCMCIA designs**
- **Operation at 3.3V or 5V**
- **Pin-compatible with SSI 78Q8370**
- **Integrated 10Base-T transceiver:**
  - **Programmable/automatic selection of twisted pair (RJ45) or AUI port**
  - **Receive polarity detection/correction on twisted-pair inputs**
- **Manchester Encoder/Decoder circuit**
- **AUI port for connection to 10Base2/5 transceiver or AUI cable**
- **Integrated bus interface compliant with PCMCIA release 2.1 specification**
- **Bus interface can be bypassed for non-PCMCIA applications**
- **Protocol Controller compliant with IEEE 802.3 and Ethernet 2.0**
- **Advanced Buffer Manager architecture:**
  - **Automatic management of all pointers**
  - **Allows "simultaneous" access to data in buffer memory by both the network and host**
  - **High-speed received packet skip**
- **Configurable Buffer Memory for design flexibility:**
  - **Two-bank transmit buffer in 2, 4, 8, or 16 Kbyte sizes**
  - **Ring-structure receive buffer from 4 to 62 Kbytes**
- **Software-configurable system bus structure:**
  - **Compatible with major microprocessors**
  - **8- or 16-bit wide data path communications with hosts**
- **Power management options:**
  - **Intelligent power mode automatically shuts off unused circuitry**
  - **Standby mode reduces power while not in operation**
  - **Full shutdown mode offers maximum power savings**
- **Available in a 100-lead TQFP package**

FUNCTIONAL DESCRIPTION

The 78Q8373 consists of six major blocks as shown in Figure 1.

- Buffer Manager (and SRAM Interface)
- Data Link Controller
- Host/PCMCIA Interface
- Manchester ENDEC
- Twisted Pair Transceiver
- Power Management

BUFFER MANAGER

The Buffer Manager manages all accesses to the buffer memory through the SRAM interface. The buffer memory is connected directly to the Data Link Controller (DLC), thus eliminating the need for a local microprocessor. The Buffer Manager also keeps track of all buffer memory pointers automatically, simplifying the software driver task. Together with intelligent arbitration, this makes the 8373 a high performance LAN controller.

The buffer memory is divided into two portions: transmit memory portion and receive memory portion. The transmit memory portion can be partitioned into 2K, 4K, 8K or 16 Kbyte buffer sizes. There is only one transmit bank if a 2 KB transmit buffer size is selected. If the transmit buffer size is greater than 2 KB, then the transmit buffer is configured into two banks of equal size. With the two bank configuration, one transmit bank may be tied up during transmission but the host can still continue to load data packets into the second transmit bank to be transmitted later. The receive buffer has a ring architecture which can be configured from 4K to 62 KB depending on the buffer memory configuration which has a range of 8K to 64 KB.

A central arbitrator inside the Buffer Manager prioritizes and services requests for access to the buffer memory from 4 sources: the Transmitter, the Receiver, Host Read and Host Write. If necessary, the 8373 will assert a 'not ready' handshake to the host while servicing the Transmitter and/or Receiver. The 8373 arbitration mechanism provides packet management by interleaving packet data accesses to the buffer memory such that the operations appear to be simultaneous.

For instance, in the situation where 2 transmit banks are configured, the host can load the first transmit bank and initiate a transmission. While the first transmit bank is being transmitted, the host can continue to load packets in the second transmit bank. At this stage, the 8373 can potentially be receiving data from the medium and loading it into the receive buffer (if the 8373 is in a loop back mode or if self-reception occurs).

DATA LINK CONTROLLER

The Data Link Controller (DLC) implements the ISO/ANSI/IEEE 802-3 CSMA/CD protocol. It consists of a Transmitter, a Receiver and CRC logic (which is shared by both transmit and receive operations). Automatic generation and stripping of the 64-bit preamble and the 32-bit CRC code are provided on-chip.

HOST/PCMCIA INTERFACE

The Host Interface (HIF) provides connection to the host system. It consists of the various registers, DMA circuits and ready logic. Both word and byte interfaces are supported as well as big endian and little endian data ordering. Host access to the buffer memory is through BMR8 (and BMR9). Reading from BMR8 will read a byte or word from the receive buffer and writing to BMR8 will write a byte or word to the transmit buffer. The ready logic is capable of delaying host access to the buffer memory with a time-out mechanism. Both single and burst DMA transfer modes are supported.

The PCMCIA interface circuitry builds on top of the 8373 generic host interface and is only active if the MODE pin is left unconnected (internally pulled-up). The 8373 can thus connect directly to a PCMCIA release 2.1 compliant bus. It also supports decoding for the external CIS memory (both ROM and Flash types). The 8373 pinout has been defined to minimize criss-crossing connections to the PCMCIA connector. This allows for a cost effective 2-layer PCB design.

MANCHESTER ENDEC

This block implements Manchester encoding and decoding. Serial NRZ data from the DLC is converted to Manchester encoded data and sent to either the twisted-pair transceiver block or to the Attachment Unit Interface (AUI) driver, depending on which block is active. The decoder section performs three functions: clock recovery, carrier detection and Manchester decoding. The recovered receive clock will be low at the end of reception and during idle to save power. Jitter of up to ±18 ns can be tolerated by the decoder. This block also translates a 10 MHz collision signal to a logic-level signal before sending it to the DLC block if the AUI port is selected.

TWISTED PAIR TRANSCEIVER

The on-chip Twisted Pair module consists of a number of functions. It has a smart squelch circuitry to determine valid data present on the differential receive inputs TPIP/TPIN. Its transmit and pre-distortion drivers connect to the twisted pair network via the summing resistors and transformer/filter. The link detector/ generator circuitry checks the integrity of the cable connecting the two twisted pair MAUs. Collision, jabber and SQE are also incorporated.

POWER MANAGEMENT

One very useful and important feature that the 8373 offers is intelligent power management. It supports three different power saving modes: Intelligent, Standby, and Full Shutdown. All modes are configurable through registers. In the Intelligent mode, clocks are active only when they are needed. For example, when not transmitting, the clock supplied to the transmitter circuit in the DLC block is not active while host read from buffer memory may be active. In Standby mode, the oscillator clock is disconnected from the rest of the circuits, so that only the oscillator circuits draw power. Full Shutdown turns off the oscillator, resulting in maximum power savings. Note that this mode is not available when using an external clock source.

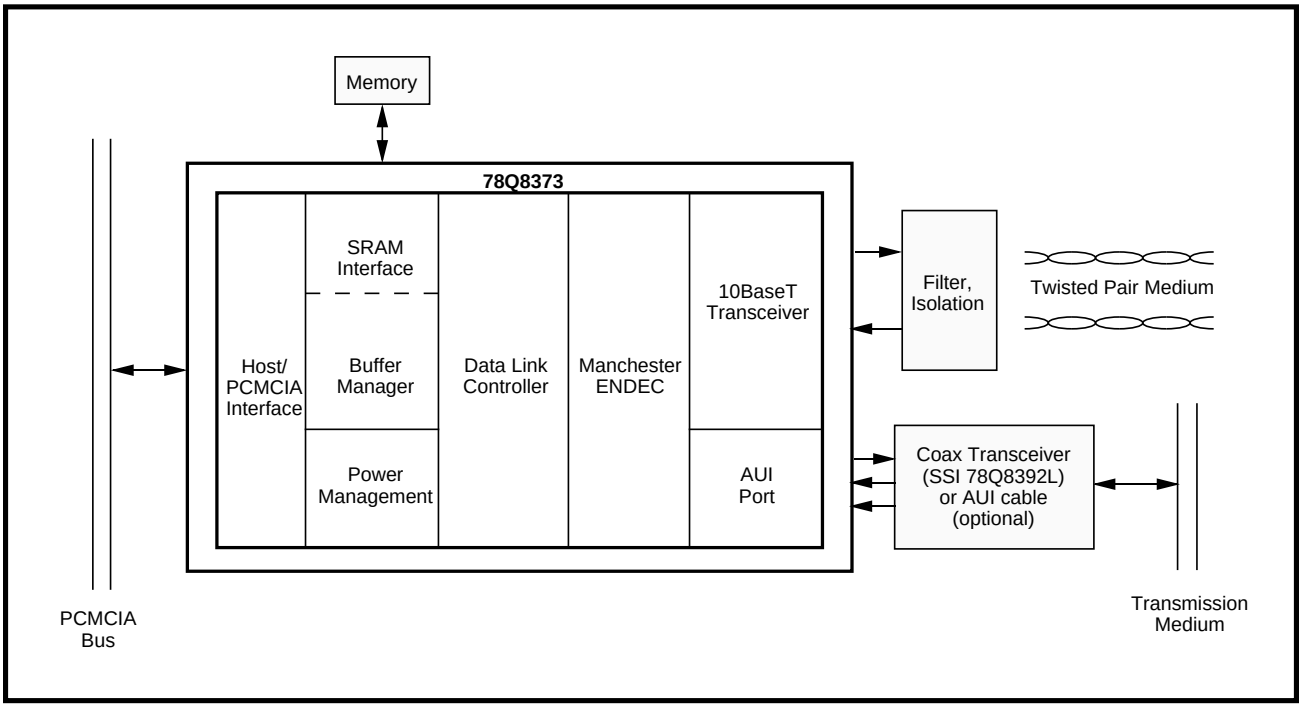


FIGURE 1: System Diagram

Pin Assignment Table - PCMCIA Bus Mode - 100-Pin TQFP

PIN#	PIN NAME	TYPE	PIN#	PIN NAME	TYPE	PIN#	PIN NAME	TYPE	PIN#	PIN NAME	TYPE
1	D1	IO4	26	$\overline{OE}$	I	51	RA4	O4	76	DON	AO
2	D8	IO4U	27	$\overline{WE}$	I	52	RA5	O4	77	DOP	AO
3	D0	IO4	28	$\overline{INPACK}$	O4	53	RA6	O4	78	AGND	P
4	A0	I	29	$\overline{REG}$	I	54	GND	P	79	REXT	R
5	A1	I	30	$\overline{ROMG}$	O4	55	VDD	P	80	AVDD	P
6	A2	I	31	$\overline{FCE}$	O4	56	RA7	O4	81	TPIN	AI
7	A3	I	32	$\overline{XPD}$	O4	57	RA12	O4	82	TPIP	AI
8	RESET	SI	33	XRST	O4	58	RA14	O4	83	MODE	TI
9	VDD	P	34	GND	P	59	$\overline{RWE}$	O4	84	DIN	AI
10	GND	P	35	RD0	IO4U	60	RA13	O4	85	DIP	AI
11	$\overline{IOWR}$	I	36	RD1	IO4U	61	RA8	O4	86	CIN	AI
12	$\overline{IORD}$	I	37	RD2	IO4U	62	RA9	O4	87	CIP	AI
13	$\overline{CE2}$	I	38	RD3	IO4U	63	RA11	O4	88	GND	P
14	D15	IO4U	39	RD4	IO4U	64	$\overline{ROE}$	O4	89	SPKRIN	SI
15	$\overline{CE1}$	I	40	RD5	IO4U	65	RA15	O4	90	$\overline{SPKR}$	O8
16	D14	IO4U	41	RD6	IO4U	66	OSCI	CI	91	CCRA	I
17	D7	IO4	42	RD7	IO4U	67	OSCO	O	92	RRST	O4
18	GND	P	43	GND	P	68	VDD	P	93	LEDLT	OD16
19	D13	IO4U	44	$\overline{RCS0}$	O4	69	GND	P	94	CB	O4
20	D6	IO4	45	$\overline{RCS1}$	O4	70	GND	P	95	$\overline{IOIS16}$	O4
21	D12	IO4U	46	RA10	O4	71	TPDN	AO	96	$\overline{IREQ}$	O8
22	D5	IO4	47	RA0	O4	72	TPDP	AO	97	$\overline{WAIT}$	O4
23	D11	IO4U	48	RA1	O4	73	TPON	AO	98	D10	IO4U
24	D4	IO4	49	RA2	O4	74	TPOP	AO	99	D2	IO4
25	D3	IO4	50	RA3	O4	75	VDD	P	100	D9	IO4U

Legend:

I:	Input (TTL level)
O4, O8:	Output with IOL = 4 or 8 mA
OD16:	Output Open Drain with IOL = 16 mA
IO4, IO4U:	Input (TTL level) and Output with IOL = 4 mA; IO4U refers to IO4 with an internal pull-up resistor
CI:	CMOS level input
SI:	Schmitt trigger input
TI:	Three-state input. May be connected to low, high, or left open.
AI:	Analog input
AO:	Analog output
P:	Power
R:	Resistor to ground
O:	Output

Pin Assignment Table - Generic Bus Mode - 100-Pin TQFP

PIN#	PIN NAME	TYPE	PIN#	PIN NAME	TYPE	PIN#	PIN NAME	TYPE	PIN#	PIN NAME	TYPE
1	HD1	IO4	26	RD8	IO4U	51	RA4	O4	76	DON	AO
2	HD8	IO4U	27	RD9	IO4U	52	RA5	O4	77	DOP	AO
3	HD0	IO4	28	RD10	IO4U	53	RA6	O4	78	AGND	P
4	HA0	I	29	RD11	IO4U	54	GND	P	79	REXT	R
5	HA1	I	30	RD12	IO4U	55	VDD	P	80	AVDD	P
6	HA2	I	31	RD13	IO4U	56	RA7	O4	81	TPIN	AI
7	HA3	I	32	RD14	IO4U	57	RA12	O4	82	TPIP	AI
8	RESET	SI	33	RD15	IO4U	58	RA14	O4	83	MODE	TI
9	VDD	P	34	GND	P	59	$\overline{\text{RWE}}$	O4	84	DIN	AI
10	GND	P	35	RD0	IO4U	60	RA13	O4	85	DIP	AI
11	$\overline{\text{WR}}$	I	36	RD1	IO4U	61	RA8	O4	86	CIN	AI
12	$\overline{\text{RD}}$	I	37	RD2	IO4U	62	RA9	O4	87	CIP	AI
13	$\overline{\text{BHE}}$	I	38	RD3	IO4U	63	RA11	O4	88	GND	P
14	HD15	IO4U	39	RD4	IO4U	64	$\overline{\text{ROE}}$	O4	89	$\overline{\text{DMACK}}$	SI
15	$\overline{\text{CS}}$	I	40	RD5	IO4U	65	RA15	O4	90	DMREQ	O8
16	HD14	IO4U	41	RD6	IO4U	66	OSCI	CI	91	EOP	I
17	HD7	IO4	42	RD7	IO4U	67	OSCO	O	92	RRST	O4
18	GND	P	43	GND	IO4U	68	VDD	P	93	LEDLT	OD16
19	HD13	IO4U	44	$\overline{\text{RCS0}}$	P	69	GND	P	94	CB	O4
20	HD6	IO4	45	$\overline{\text{RCS1}}$	O4	70	GND	P	95	HWORD	O4
21	HD12	IO4U	46	RA10	O4	71	TPDN	AO	96	$\overline{\text{INT}}$	O8
22	HD5	IO4	47	RA0	O4	72	TPDP	AO	97	READY	O4
23	HD11	IO4U	48	RA1	O4	73	TPON	AO	98	HD10	IO4U
24	HD4	IO4	49	RA2	O4	74	TPOP	AO	99	HD2	IO4
25	HD3	IO4	50	RA3	O4	75	VDD	P	100	HD9	IO4U

Legend:

I:	Input (TTL level)
O4, O8:	Output with IOL = 4 or 8 mA
OD16:	Output Open Drain with IOL = 16 mA
IO4, IO4U:	Input (TTL level) and Output with IOL = 4 mA; IO4U refers to IO4 with an internal pull-up resistor
CI:	CMOS level input
SI:	Schmitt trigger input
TI:	Three-state input. May be connected to low, high, or left open.
AI:	Analog input
AO:	Analog output
P:	Power
R:	Resistor to ground
O:	Output

PIN DESCRIPTION

HOST BUS INTERFACE - PCMCIA BUS MODE

<table>
<tr><th>NAME</th><th>TYPE</th><th>DESCRIPTION</th></tr>
<tr><td>RESET</td><td>I</td><td>HARDWARE RESET. Active high. A minimum pulse length of 800 ns is required. This pin resets the 8373's internal pointers and registers to their appropriate states. It also clears the CI (Configuration Index) in the CCR (Card Configuration Register), thus placing the 8373 in an unconfigured (Memory-only Interface) state. The 8373 remains in the unconfigured state until the CI has been written with a non-zero value.</td></tr>
<tr><td>$\overline{\text{IOWR}}$</td><td>I</td><td>I/O WRITE. The $\overline{\text{IOWR}}$ pin is an active low input that enables a write operation by the host to the 8373 internal registers as selected by the host address inputs A[0:3]. The $\overline{\text{REG}}$ and at least one of $\overline{\text{CE1}}$ or $\overline{\text{CE2}}$ must be also active for the I/O write to take place. The 8373 will not respond to the $\overline{\text{IOWR}}$ signal until it has been configured for I/O operation by the host.</td></tr>
<tr><td>$\overline{\text{IORD}}$</td><td>I</td><td>I/O READ. The $\overline{\text{IORD}}$ pin is an active low input that enables a read operation by the host from the 8373 internal registers as selected by the host address inputs A[0:3]. The $\overline{\text{REG}}$ and at least one of $\overline{\text{CE1}}$ or $\overline{\text{CE2}}$ must be also active for the I/O read to take place. The 8373 will not respond to the $\overline{\text{IORD}}$ signal until it has been configured for I/O operation by the host.</td></tr>
<tr><td>$\overline{\text{CE1}}$, $\overline{\text{CE2}}$</td><td>I</td><td>CHIP ENABLE. Active low input signals acting as chip select for the 8373. $\overline{\text{CE1}}$ enables even-numbered address bytes and $\overline{\text{CE2}}$ enables odd-numbered address bytes. When the 8373 is programmed to be in byte mode (DLCR6<5> HBYTE bit is a "1"), $\overline{\text{CE2}}$ is a don't care and only lower databus D[0:7] is used for data transfer. Combinations of $\overline{\text{CE1}}$, $\overline{\text{CE2}}$, A0 and HBYTE bit (DLCR6<5>) are used to select the different modes of I/O space word/byte transfer according to the following table (the table assumes $\overline{\text{REG}}$ is activated):
<table>
<tr><th>HBYTE</th><th>$\overline{\text{CE2}}$</th><th>$\overline{\text{CE1}}$</th><th>A0</th><th>D[15:8]</th><th>D[7:0]</th></tr>
<tr><td>0</td><td>1</td><td>0</td><td>0</td><td>X</td><td>even-byte</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>1</td><td>X</td><td>odd-byte</td></tr>
<tr><td>0</td><td>0</td><td>0</td><td>0</td><td>odd-byte</td><td>even-byte</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>X</td><td>odd-byte</td><td>X</td></tr>
<tr><td>1</td><td>X</td><td>0</td><td>0</td><td>X</td><td>even-byte</td></tr>
<tr><td>1</td><td>X</td><td>0</td><td>1</td><td>X</td><td>odd-byte</td></tr>
</table>
For Attribute Memory access, data transfer occurs only on D[7:0] with the following valid combinations only:
<table>
<tr><th>HBYTE</th><th>$\overline{\text{CE2}}$</th><th>$\overline{\text{CE1}}$</th><th>A0</th><th>D[15:8]</th><th>D[7:0]</th></tr>
<tr><td>X</td><td>X</td><td>0</td><td>0</td><td>X</td><td>even-byte</td></tr>
</table></td></tr>
<tr><td>CCRA</td><td>I</td><td>CARD CONFIGURATION REGISTER ADDRESS. This pin connects to PCMCIA higher address bit. A high (together with $\overline{\text{REG}}$ activation) on this bit selects the internal CCR registers and a low selects the external CIS (Card Information Structure) ROM/Flash memory.</td></tr>
<tr><td>$\overline{\text{OE}}$</td><td>I</td><td>OUTPUT ENABLE. An active low input signal used to read data from the internal CCR (Card Configuration Registers) and from the external Attribute Memory (through the activation of $\overline{\text{FCE}}$ and $\overline{\text{ROMG}}$). This $\overline{\text{OE}}$ should also connect to the output enable of the external Flash Memory or the ROM.</td></tr>
</table>

HOST BUS INTERFACE - PCMCIA BUS MODE (continued)

NAME	TYPE	DESCRIPTION
$\overline{WE}$	I	WRITE ENABLE. An active low input signal used to write data to the internal CCR (Card Configuration Registers) and to the external Attribute (Flash) Memory (through the activation of $\overline{FCE}$). This $\overline{WE}$ should also connect to the write enable of the external Flash Memory.
$\overline{REG}$	I	ATTRIBUTE MEMORY SELECT. When this signal is active (low), it signifies access from or to the Attribute Memory ($\overline{OE}$ or $\overline{WE}$ active) or the I/O space ($\overline{IORD}$ or $\overline{IOWR}$ active). Attribute Memory is generally used to record card capacity and other configuration and attribute information. This includes the standardized CCRs (Card Configuration Registers) which are located internally in the 8373. When Attribute Memory is accessed, only data signals D[0:7] are valid and signals D[8:15] are ignored.
A[0:3]	I	ADDRESS BUS. Selects the set of 8373 internal registers including the CCR (Card Configuration Registers) for read or write operations.
D[0:15]	I/O	DATA BUS. A bi-directional, tri-state bus. The combinations of $\overline{CE1}$, $\overline{CE2}$ and A0 control the portion of the bus that is being utilized. A[0:3] and RBNK1,0 (DLCR7<3:2>) select the set of internal registers for access.

HOST BUS INTERFACE - PCMCIA BUS MODE

The following output signals are inactive (high) until the 8373 is configured for I/O mode.

$\overline{WAIT}$	O	$\overline{WAIT}$. An active low output that is asserted to delay completion of the current I/O read or write operation. It will also be used if the device is unable to respond to read or write requests within 2.4 µs. In these situations, the 8373 will also assert $\overline{IREQ}$ and the host read error status bit (DLCR1<6>) or host write error status bit (DLCR0<0>).
$\overline{INPACK}$	O	INPUT ACKNOWLEDGE. This active low output signal is asserted when the 8373 is selected and it can respond to an I/O read cycle requested by the host. This signal is used by the host to control the enable of any input data buffer between the card and the CPU. This signal will only be active after the 8373 is configured for I/O mode.
$\overline{IOIS16}$	O	I/O IS 16 BIT PORT. This active low output signal is asserted when the 8373 is configured for word transfer to indicate to the host that it is capable of 16-bit access. Therefore, this pin follows the register bit HBYTE (DLCR6<5>) once the 8373 is configured for I/O mode.
$\overline{IREQ}$	O	INTERRUPT REQUEST. This signal is available only after the 8373 is configured for I/O mode. It is asserted when the 8373 requires the intervention of the Host in situations as depicted in DLCR0,1 and BMR15. The IREQ signal is masked by writing a "0" to the respective interrupt enable register. To comply to with PCMCIA 2.0 spec, the 8373 supports both Pulsed- and Level- Mode interrupts as selected by the LevlREQ (CCR0<6>) register bit.
$\overline{SPKR}$	O	SPEAKER. This signal is held inactive (i.e. high) until the 8373 is configured for I/O mode. It provides a single-amplitude, on-off, binary audio waveform intended to drive the host's loudspeaker. The source for the signal is SPKRIN.

PIN DESCRIPTION (continued)

PCMCIA APPLICATION PINS

NAME	TYPE	DESCRIPTION
$\overline{\text{ROMG}}$	O	ROM ENABLE. Active low. This signal will be activated when an attribute memory read is performed on the external CIS memory.
$\overline{\text{FCE}}$	O	FLASH MEMORY CHIP ENABLE. Active low. The flash memory $\overline{\text{WE}}$ (Write Enable) and $\overline{\text{OE}}$ (Output Enable) come from PCMCIA pins $\overline{\text{WE}}$ and $\overline{\text{OE}}$.
$\overline{\text{XPD}}$	O	EXTERNAL POWER DOWN. Active low. When the 8373 enters power down mode, this pin will be low. It can be used to control power down of external devices residing on the same card.
XRST	O	EXTERNAL RESET. Active high. This pin is a reflection of CCR0<7> register bit. This allows a software controlled hardware reset of the 8373 and the rest of the devices residing on the same card.
SPKRIN	I	SPEAKER IN. This pin is qualified with the AUDIO bit, CCR1<3> to produce the inverted $\overline{\text{SPKR}}$ output.

HOST BUS INTERFACE - GENERIC BUS MODE

NAME	TYPE	DESCRIPTION
RESET	I	HARDWARE RESET. Active high. A minimum pulse length of 800 ns is required. This pin resets the 8373's internal pointers and registers to their appropriate states. Note: the 8373 must be reset after power on before usage.
READY	O	READY. This output is asserted to indicate to the host that the 8373 is ready to complete the requested read or write operation. It will also be used if the device is unable to respond to read or write requests within 2.4 µs. In these situations, the 8373 will also assert $\overline{INT}$ and the host read error status bit (DLCR1 <6>) or host write error status bit (DLCR0 <0>). The polarity of the READY pin is determined by the MODE pin.
$\overline{WR}$	I	WRITE. The $\overline{WR}$ pin is an active low input that enables a write operation from the host to the 8373's internal registers as selected by the host address inputs HA[0:3].
$\overline{RD}$	I	READ. The $\overline{RD}$ pin is an active low input that enables a read operation by the host from the 8373's internal registers as selected by the host address inputs HA[0:3].
$\overline{CS}$	I	CHIP SELECT. An active low input signal as the chip select for the 8373.
$\overline{BHE}$	I	BYTE HIGH ENABLE. This is an active low byte/word control pin used only when the 8373 is configured for word transfer by HBYTE bit (DLCR6 <5>). Combinations of $\overline{BHE}$ and HA0 are used to select word, upper byte only or lower byte only transfers.

HBYTE	$\overline{BHE}$	HA0	FUNCTION
0	0	0	Word transfer
0	0	1	Byte transfer on high bus HD[8:15].
0	1	0	Byte transfer on low bus HD[0:7].
0	1	1	Reserved
1	X	X	Byte transfer (HD[0:7])

$\overline{INT}$	O	INTERRUPT. This active low signal is asserted when the 8373 requires the intervention of the Host in situations as depicted in DLCR0,1 and BMR15. The $\overline{INT}$ signal is masked by writing a '0' to the respective interrupt enable register.
EOP	I	END OF PROCESS. Asserted at the end of a DMA transfer by the Host DMA controller. Further DMA requests (DMREQ) will be discontinued after EOP is asserted. Polarity can be selected via the register bit (DLCR7 <1>).
DMREQ	O	DMA REQUEST. The 8373 issues a DMREQ to the Host DMA controller to initiate a write to its transmit buffer or a read from its receive buffer.

PIN DESCRIPTION (continued)

HOST BUS INTERFACE - GENERIC BUS MODE

NAME	TYPE	DESCRIPTION
$\overline{\text{DMACK}}$	I	DMA ACKNOWLEDGE. An active low signal issued by the Host DMA controller when it is ready to perform data transfers between the Host and the 8373's buffer memory via BMR8.
HA[0:3]	I	HOST ADDRESS. Selects the set of internal registers to be accessible by the 8373 for read or write operations.
HD[0:15]	I/O	HOST DATA BUS. A bi-directional, tri-state bus for data, command and status transfers between the Host and the 8373 with the direction being controlled by $\overline{\text{RD}}$ and $\overline{\text{WR}}$. The combinations of HBYTE, $\overline{\text{BHE}}$ and HA0 control the portion of the bus that is being utilized. HA[0:3] and RBNK <0:1> (DLCR7 <2:3>) select the set of internal registers for access.
HWORD	O	HOST WORD CONFIGURATION. This pin is the complement of the register bit HBYTE (DLCR6 <5>). If HBYTE is a '0', the Host interface is configured for word transfers. If HBYTE is a '1', the Host interface is configured for byte transfers on the lower bus, HD[0:7].

BUFFER MEMORY INTERFACE

$\overline{\text{RCS0}}$, $\overline{\text{RCS1}}$	O	RAM CHIP SELECT. $\overline{\text{RCS0}}$ and $\overline{\text{RCS1}}$ are active low chip select lines for the SRAM with $\overline{\text{RCS0}}$ as the least significant byte.
$\overline{\text{ROE}}$	O	RAM OUTPUT ENABLE. Active low. This is the output enable asserted by the 8373 during buffer memory read cycles for the SRAM.
$\overline{\text{RWE}}$	O	RAM WRITE ENABLE. Active low. This is the write enable asserted by the 8373 during buffer memory write cycles for the SRAM.
RD[0:15]	I/O	RAM DATA BUS. This is the data bus between the 8373 and the buffer memory. It can be configured for byte or word transfer depending on register bit RBYTE (DLCR6 <4>) RAM BYTE. For word transfers, the ordering of the most and least significant byte is defined by the register bit, INTLMOT (DLCR7 <0>). In PCMCIA bus mode, this data bus is only 8 bits wide (RD[0:7]).
RA[0:15]	O	RAM ADDRESS BUS. Addresses up to 64 KByte of SRAM buffer memory.

NETWORK ATTACHMENT UNIT INTERFACE

DON, DOP	O	TRANSMIT DATA NEGATIVE and POSITIVE. Differential outputs to external transceiver for transmission.
DIN, DIP	I	RECEIVE DATA NEGATIVE and POSITIVE. Manchester differential inputs from external transceiver for reception.
CIN, CIP	I	COLLISION DETECT NEGATIVE and POSITIVE. When an externally connected transceiver detects a collision on the medium, these differential inputs are driven by a 10 MHz signal.
REXT	-	EXTERNAL RESISTOR. External biasing resistor. Connect to 20 kΩ ±1% to AGND.

NETWORK TWISTED-PAIR MEDIUM INTERFACE

NAME	TYPE	DESCRIPTION
TPON, TPOP	O	TWISTED-PAIR OUTPUT NEGATIVE and POSITIVE. Driver outputs to twisted-pair medium. Must be summed together with TPDN and TPDP by external resistors in a pre-equalization network to produce twisted-pair transmit signal.
TPDN, TPDP	O	TWISTED-PAIR DELAYED NEGATIVE and POSITIVE. Delayed (50 ns) driver outputs to twisted-pair medium. Must be summed together with TPON and TPOP by external resistors in a pre-equalization network to produce twisted-pair transmit signal.
TPIN, TPIP	I	TWISTED-PAIR INPUT NEGATIVE and POSITIVE. Inputs from twisted-pair medium.

DEVICE POWER

VDD	P	POWER SUPPLY. A +5V DC (±5%) or +3.3 VDC (±0.3V) supply is required.
GND	P	SYSTEM GROUND.
AVDD	P	ANALOG VDD. The analog VDD pin required by the internal AUI and twisted-pair circuits is to be connected to a different VDD path from the digital VDD. A +5V DC (±5%) or +3.3 VDC (±0.3V) supply is required.
AGND	P	ANALOG GROUND. The analog ground required by the internal encoder/decoder is to be connected to a separate GND path from the digital GND.

CRYSTAL OSCILLATOR

OSCI	I	OSCILLATOR IN. Connection for one side of the 20 MHz crystal or an input for an external 20 MHz clock source.
OSCO	O	OSCILLATOR OUT. Connection for other side of the 20 MHz crystal. Left unconnected if an external clock is used.

MISCELLANEOUS

CB	O	CONTROL BIT. A complement of the internal register bit, DLCR4 <2>, which is used to activate any external hardware.
RRST	O	REMOTE RESET. This pin follows the RMTRST register bit (DLCR1 <4>). The RMTRST bit is '1' only if a packet with the pattern 0900H in the Type Field is detected and ENA_RMTRST (DLCR5 <2>) is activated. This feature can be used by the nodes on the network to remotely-control external hardware.
MODE	I	MODE SELECT. Tied high to select Generic bus mode with active high READY timing. Tied low to select Generic bus mode with active low READY timing. Left open to select PCMCIA bus mode (it will be internally pulled up).
LEDLT	O	LED LINK, TRANSMIT. Connect to LED with current limiting resistor to VDD. LED is on during link up and off during link down. During link up (when LED is on), a transmission will blink off the LED temporarily to indicate activity. This feature is available for both twisted pair and AUI interfaces.

ELECTRICAL SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Operation beyond the maximum ratings may damage the device.

PARAMETER	RATING
Supply voltage, Vdd	-0.5 to 6.0V
Input voltage, Vin	-0.5 to Vdd + 0.5V
Output voltage, Vout	-0.5 to Vdd + 0.5V
Storage temperature, Tstg	-55 to 150°C
Lead temperature (max 10 sec soldering), Tl	235°C (IR)

DC CHARACTERISTICS (Ta = 0 to 70°C, Vdd = 5V ±5%, 5V Values)

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNIT
Low level input voltage	Vil	TTL inputs			0.8	V
		OSCI pin			1.6	V
		Schmitt inputs			1.1	V
High level input voltage	Vih	TTL inputs	2.2			V
		OSCI pin	3.8			V
		Schmitt inputs	3.5			V
Pull down current (RESET pin)	Ipd		13		50	µA
Low level output voltage	Vol	Rated Iol	0		0.4	V
High level output voltage	Voh	Rated Ioh	2.4		Vdd	V
Low level output current	Iol	Pin types O4, IO4, IO4U Vdd = 5V	4			mA
(with Vol = 0.4V)		Pin type O8 Vdd = 5V	8			mA
		Pin type OD16 Vdd = 5V	16			mA
High level output current	Ioh	Pin types O4, IO4, IO4U Vdd = 5V	-4			mA
(with Voh = 2.4V)		Pin type O8 Vdd = 5V	-8			mA
Leakage current (input/output)	Il		-10		10	µA
Supply current	Idd	Fully active(1)			40	mA
		Idle			30	mA
Power down supply current	Ipwrdn	Osc. on			10	mA
		Osc. off			100	µA

Note: (1) Fully active means 3 “simultaneous” operations: transmitting, receiving (through twisted-pair port) and either host write or read.

DC CHARACTERISTICS (Ta = 0 to 70°C, Vdd = 3.3V ±0.3V, 3V Values)

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNIT
Low level input voltage	Vil	TTL inputs			0.8	V
		OSCI pin			0.7	V
		Schmitt inputs			0.4	V
High level input voltage	Vih	TTL inputs	2			V
		OSCI pin	2.1			V
		Schmitt inputs	2.4			V
Pull down current (RESET pin)	Ipd		5		28	µA
Low level output voltage	Vol	Rated Iol	0		0.4	V
High level output voltage	Voh	Rated Ioh	2.4		Vdd	V
Low level output current	Iol	Pin types O4, IO4, IO4U Vdd = 3.3V	2.4			mA
(with Vol = 0.4V)		Pin type O8 Vdd = 3.3V	4.9			mA
		Pin type OD16 Vdd = 3.3V	9.8			mA
High level output current	Ioh	Pin types O4, IO4, IO4U Vdd = 3.3V	-1.5			mA
(with Voh = 2.4V)		Pin type O8 Vdd = 3.3V	-3			mA
Leakage current (input/output)	Il		-10		10	µA
Supply current	Idd	Fully active(1)			28	mA
		Idle			20	mA
Power down supply current	Ipwrdn	Osc. on			6	mA
		Osc. off			100	µA

Note: (1) Fully active means 3 “simultaneous” operations: transmitting, receiving (through twisted-pair port) and either host write or read.

ELECTRICAL SPECIFICATIONS (continued)

AUI CHARACTERISTICS

(VDD = 5V ± 5%, 3.3 ± 0.3V, Vss = 0V, Ta = 0°C to +70°C)

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
Low Output Voltage for DOP, DON Vaol	Rext = 20 kΩ Rl = 78Ω	Vdd-1.5		Vdd-0.75	V
High Output Voltage for DOP, DON Vaoh	Rext = 20 kΩ Rl = 78Ω	Vdd-0.55		Vdd	V
DOP, DON Output Current Iao	Rext = 20 kΩ	8		14	mA
DIP, DIN, CIP, CIN Open Circuit Input Voltage (bias) Valb	Vdd = 5V ± 5% Vdd = 3.3 ± 0.3V	2.45 2.13		3.33 2.88	V
DIP, DIN, CIP, CIN Diff Squelch Threshold Vasq		-300		-120	mV
DOP, DON Diff Idle Output Vadi	Rl = 78Ω	-40		40	mV
DOP, DON Diff Peak Output Vadv	Rext = 20 kΩ Rl = 78Ω	620		1100	mV
DOP, DON Output Resistance Rao				75	Ω

TWISTED PAIR
(VDD = 5V ± 5%, Ta = 0°C to +70°C)

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
TPIP, TPIN Diff Input Resistance Rti		3			kΩ
TPIP, TPIN Open Circuit Input Voltage (bias) Vtib		2.45		3.33	V
TPIP, TPIN Diff Input Voltage Range Vtiv	VDD = 5V	-3.1		3.1	V
TPIP, TPIN Positive Squelched Threshold Vtps	Note 1	300		585	mV
TPIP, TPIN Negative Squelched Threshold Vtns	Note 1	-585		-300	mV
TPIP, TPIN Positive Unsquelched Threshold Vtpu	Note 2		180		mV
TPIP, TPIN Negative Unsquelched Threshold Vtnu	Note 2		-180		mV
TPIP, TPIN Positive Squelched Threshold Long Distance Mode Vltps	Note 1	120		300	mV
TPIP, TPIN Negative Squelched Threshold Long Distance Mode Vltns	Note 1	-300		-120	mV
TPIP, TPIN Positive Unsquelched Threshold Long Distance Mode Vltpu	Note 2		100		mV
TPIP, TPIN Negative Unsquelched Threshold Long Distance Mode Vltnu	Note 2		-100		mV
TPOP, TPON High Output Voltage Vtoh	I = 32 mA	Vddtp -0.44		Vddtp	V
TPOP, TPON Low Output Voltage Vtol	I = 32 mA	Vsstp		Vsstp +0.44	V
TPDP, TPDN High Voltage Vtdh	I = 16 mA	Vddtp -0.44		Vddtp	V
TPDP, TPDN Low Voltage Vtdl	I = 16 mA	Vsstp		Vsstp +0.44	V
TPDP, TPDN Output Resistance Rtd				27	Ω
TPOP, TPON Output ResistanceRto				13.5	Ω

Note 1: Sine wave at 2 MHz, 5 MHz and 7 MHz
Note 2: Sine wave : 5 MHz ≤ f ≤ 10 MHz

ELECTRICAL SPECIFICATIONS (continued)

TWISTED PAIR
(VDD = 3.3 ± 0.3V, Ta = 0°C to +70°C)

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
TPIP, TPIN Diff Input Resistance Rti		3			kΩ
TPIP, TPIN Open Circuit Input Voltage (bias) Vtib		2.13		2.88	V
TPIP, TPIN Diff Input Voltage Range Vtiv	VDD = 3.3V	-2.2		2.2	V
TPIP, TPIN Positive Squelched Threshold Vtps	Note 1	210		410	mV
TPIP, TPIN Negative Squelched Threshold Vtns	Note 1	-410		-210	mV
TPIP, TPIN Positive Unsquelched Threshold Vtpu	Note 2		130		mV
TPIP, TPIN Negative Unsquelched Threshold Vtnu	Note 2		-130		mV
TPIP, TPIN Positive Squelched Threshold Long Distance Mode Vltps	Note 1	90		210	mV
TPIP, TPIN Negative Squelched Threshold Long Distance Mode Vltns	Note 1	-210		-90	mV
TPIP, TPIN Positive Unsquelched Threshold Long Distance Mode Vltpu	Note 2		70		mV
TPIP, TPIN Negative Unsquelched Threshold Long Distance Mode Vltnu	Note 2		-70		mV
TPOP, TPON High Output Voltage Vtoh	I = 50 mA	Vdd_{TP} -0.3		Vdd_{TP}	V
TPOP, TPON Low Output Voltage Vtol	I = 50 mA	Vss_{TP}		Vss_{TP} +0.3	V
TPDP, TPDN High Voltage Vtdh	I = 25 mA	Vdd_{TP} -0.3		Vdd_{TP}	V
TPDP, TPDN Low Voltage Vtdl	I = 25 mA	Vss_{TP}		Vss_{TP} +0.3	V
TPDP, TPDN Output Resistance Rtd				12	Ω
TPOP, TPON Output Resistance Rto				6	Ω

Note 1: Sine wave at 2 MHz, 5 MHz and 7 MHz
Note 2: Sine wave: 5 MHz ≤ *f* ≤ 10 MHz

TRANSFORMER RATIO:

5V OPERATION		3.3V OPERATION	
RX	TX	RX	TX
1:1	1:1	1:1.4 (step down)	1:1.4 (step down)

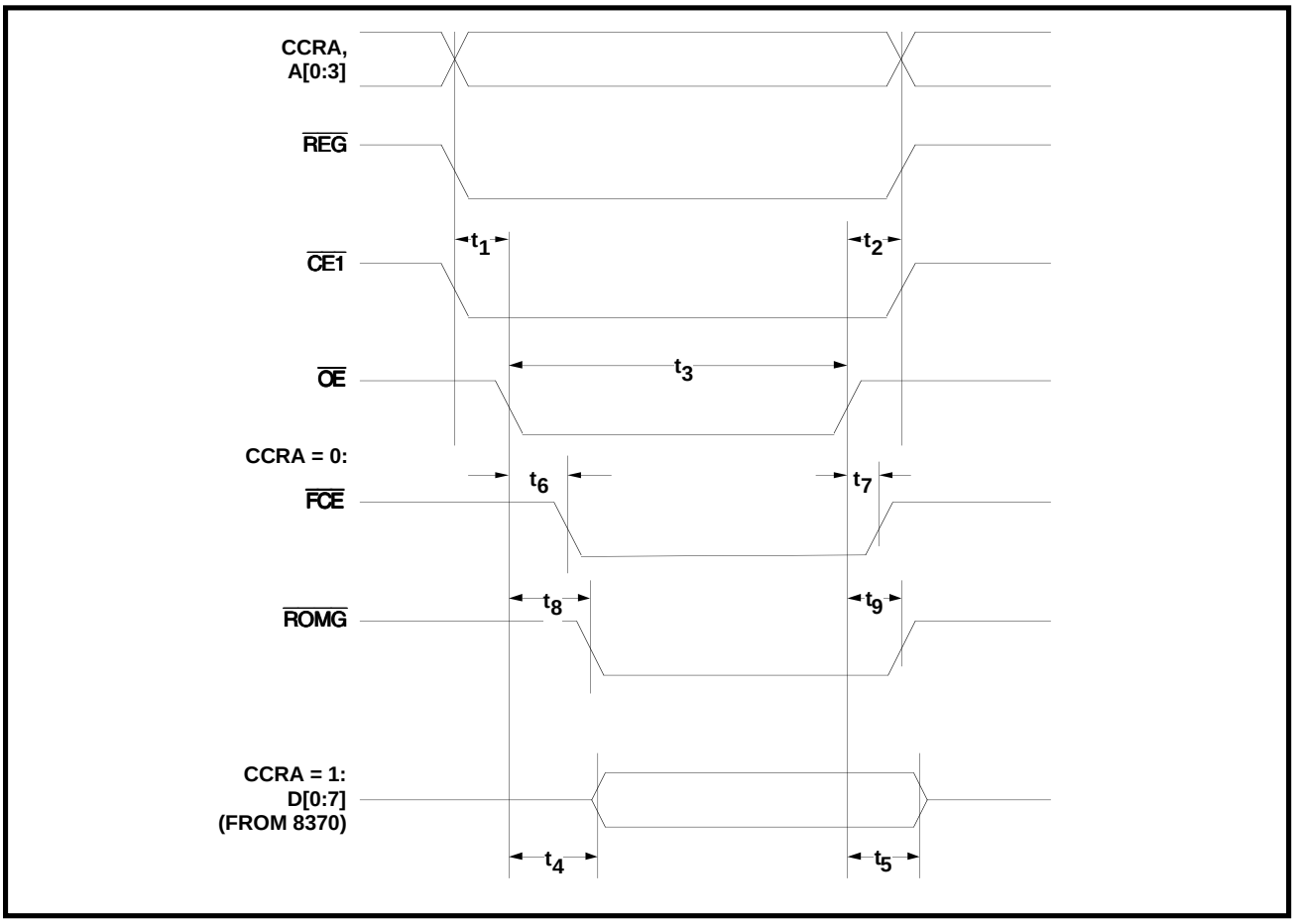


FIGURE 2: Attribute Memory Read Cycle (PCMCIA mode)

Unless otherwise stated, the following conditions apply to the remaining timing tables:
Ta = 0°C to +70°C, Vdd = 5 ± 5%, Vdd = 3.3V ± 0.3V

TABLE 1: Attribute Memory Read Cycle (PCMCIA mode) (Refer to Figure 2)

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNIT
CCRA, A[0:3] Valid to $\overline{OE}$ low; $\overline{REG}$, $\overline{CE1}$ low to $\overline{OE}$ low	t_1		0			ns
$\overline{OE}$ high to CCRA, A[0:3] invalid; $\overline{OE}$ high to $\overline{REG}$, $\overline{CE1}$ high	t_2		0			ns
$\overline{OE}$ low pulse width	t_3	Vdd = 5V	30			ns
		Vdd = 3.3V	35			ns
$\overline{OE}$ low to D[0:7] valid	t_4				45	ns
$\overline{OE}$ high to D[0:7] invalid (data hold)	t_5		10			ns
$\overline{OE}$ low to $\overline{FCE}$ low	t_6	Vdd = 5V			25	ns
		Vdd = 3.3V			35	ns
$\overline{OE}$ high to $\overline{FCE}$ high	t_7	Vdd = 5V			25	ns
		Vdd = 3.3V			35	ns
$\overline{OE}$ low to $\overline{ROMG}$ low	t_8	Vdd = 5V			25	ns
		Vdd = 3.3V			35	ns
OE high to ROMG high	t_9	Vdd = 5V			25	ns
		Vdd = 3.3V			35	ns

TABLE 2: Attribute Memory Write Cycle (PCMCIA MODE) (Refer to Figure 3)

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNIT
CCRA, A[0:3] Valid to $\overline{WE}$ low; $\overline{REG}$, $\overline{CE1}$ low to $\overline{WE}$ low	t_1		0			ns
$\overline{WE}$ high to CCRA, A[0:3] invalid; $\overline{WE}$ high to $\overline{REG}$, $\overline{CE1}$ high	t_2		0			ns
$\overline{WE}$ low pulse width	t_3	Vdd = 5V	30			ns
		Vdd = 3.3V	35			ns
D[0:7] valid to $\overline{WE}$ high (data setup)	t_4		15			ns
$\overline{WE}$ high to D[0:7] invalid (data hold)	t_5		10			ns
$\overline{WE}$ low to $\overline{FCE}$ low	t_6	Vdd = 5V			25	ns
		Vdd = 3.3V			35	ns
WE high to FCE high	t_7	Vdd = 5V			25	ns
		Vdd = 3.3V			35	ns

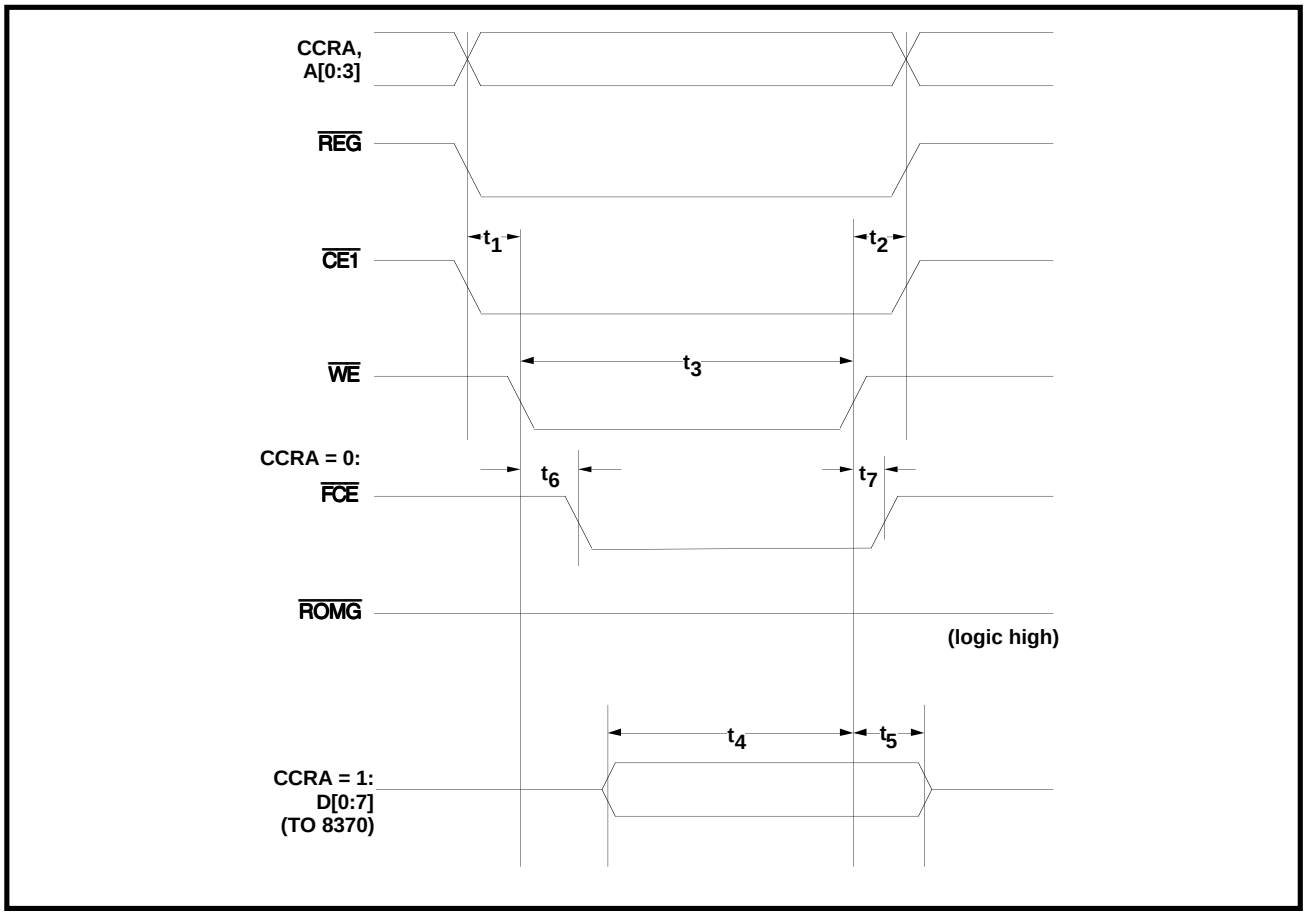


FIGURE 3: Attribute Memory Write Cycle (PCMCIA mode)

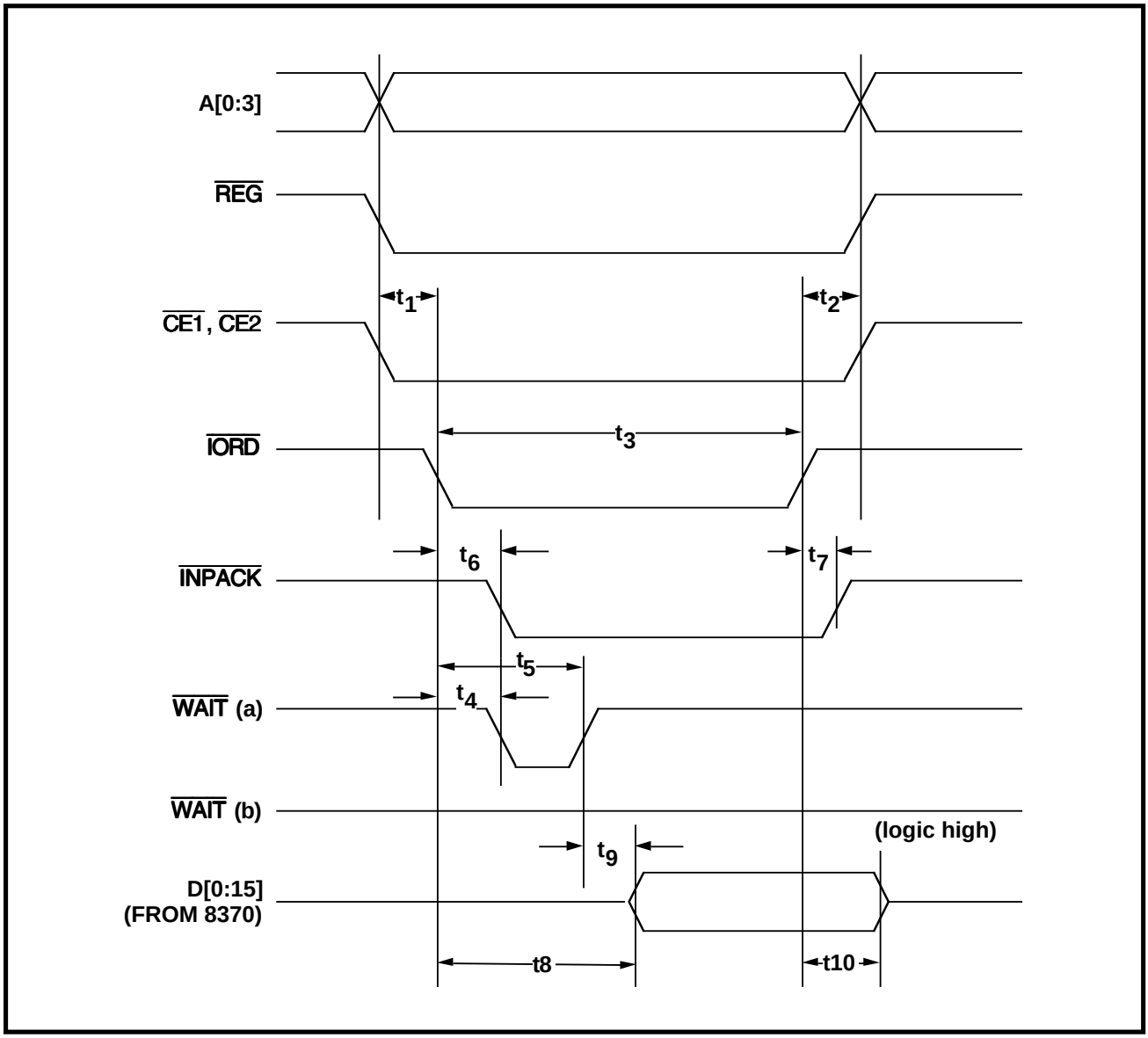


FIGURE 4: I/O Read Cycle (PCMCIA mode)

TABLE 3: I/O Read Cycle (PCMCIA mode) (Refer to Figure 4)

PARAMETER		CONDITIONS		MIN	NOM	MAX	UNIT
A[0:3] valid to $\overline{IORD}$ LOW; $\overline{REG}$, $\overline{CE1}$, $\overline{CE2}$ low to $\overline{IORD}$ low	t_1			0			ns
$\overline{IORD}$ high to A[0:3] invalid; $\overline{IORD}$ high to $\overline{REG}$, $\overline{CE1}$, $\overline{CE2}$ high	t_2			0			ns
$\overline{IORD}$ low pulse width	t_3		Vdd = 5V	30			ns
			Vdd = 3.3V	35			ns
$\overline{IORD}$ low to $\overline{WAIT}$ low	t_4	Port busy (a)	Vdd = 5V	0		35	ns
			Vdd = 3.3V			50	ns
$\overline{IORD}$ low to $\overline{WAIT}$ high(1)	t_5	Port busy (a)				350	ns
$\overline{IORD}$ low to $\overline{INPACK}$ low	t_6		Vdd = 5V			25	ns
			Vdd = 3.3V			35	ns
$\overline{IORD}$ high to $\overline{INPACK}$ high	t_7		Vdd = 5V			25	ns
			Vdd = 3.3V			35	ns
$\overline{IORD}$ low to D[0:15] valid	t_8	Register access (b)	Vdd = 5V			50	ns
			Vdd = 3.3V			70	ns
$\overline{WAIT}$ high to D[0:15] valid	t_9	Port busy (a)				5	ns
$\overline{IORD}$ high to D[0:15] invalid (data hold)	t_{10}			10			ns

TABLE 4: I/O Write Cycle (PCMCIA mode) (Refer to Figure 5)

A[0:3] valid to $\overline{IOWR}$ LOW; $\overline{REG}$, $\overline{CE1}$, $\overline{CE2}$ low to $\overline{IOWR}$ low	t_1			0			ns
$\overline{IOWR}$ high to A[0:3] invalid; $\overline{IOWR}$ high to $\overline{REG}$, $\overline{CE1}$, $\overline{CE2}$ high	t_2			0			ns
$\overline{IOWR}$ low pulse width	t_3		Vdd = 5V	30			ns
			Vdd = 3.3V	35			ns
$\overline{IOWR}$ low to $\overline{WAIT}$ low	t_4	Port busy (a)	Vdd = 5V			35	ns
			Vdd = 3.3V			50	ns
$\overline{IOWR}$ low to $\overline{WAIT}$ high(1)	t_5	Port busy (a)				350	ns
D[0:15] valid to $\overline{IOWR}$ high (data setup)	t_6			15			ns
$\overline{IOWR}$ high to D[0:15] invalid (data hold)	t_7			10			ns

Note: (1) Maximum of 350 ns may occur if system makes contiguous system read cycles at less than 100 ns intervals, and both the transmitter and receiver are active in "loopback" reception (if the transmitter and receiver are idle, the max value becomes 250 ns). 2.4 µs max for host read error.

(a) For Buffer Memory Port when port is busy.

(b) For register or port is not busy.

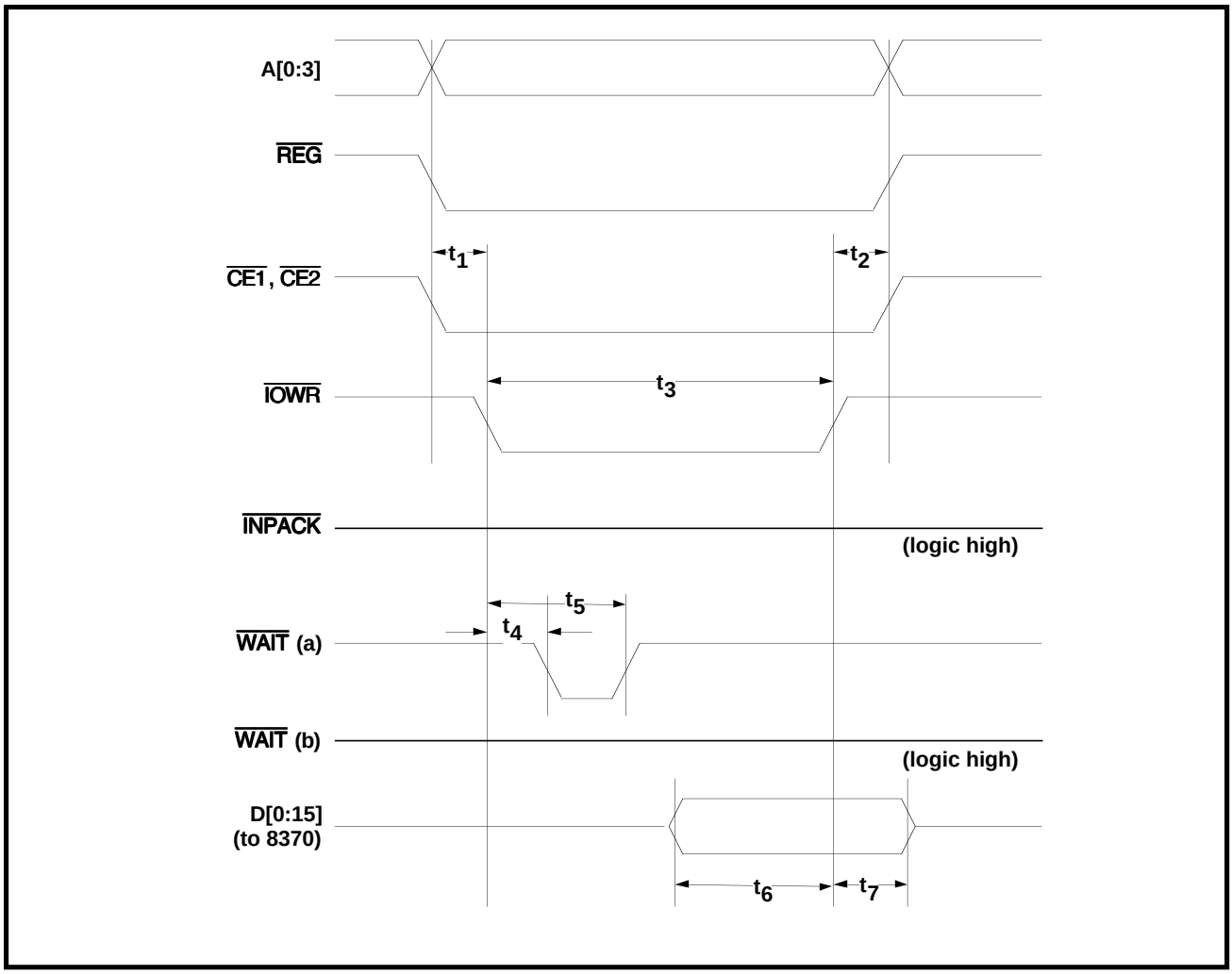


FIGURE 5: I/O Write Cycle (PCMCIA mode)

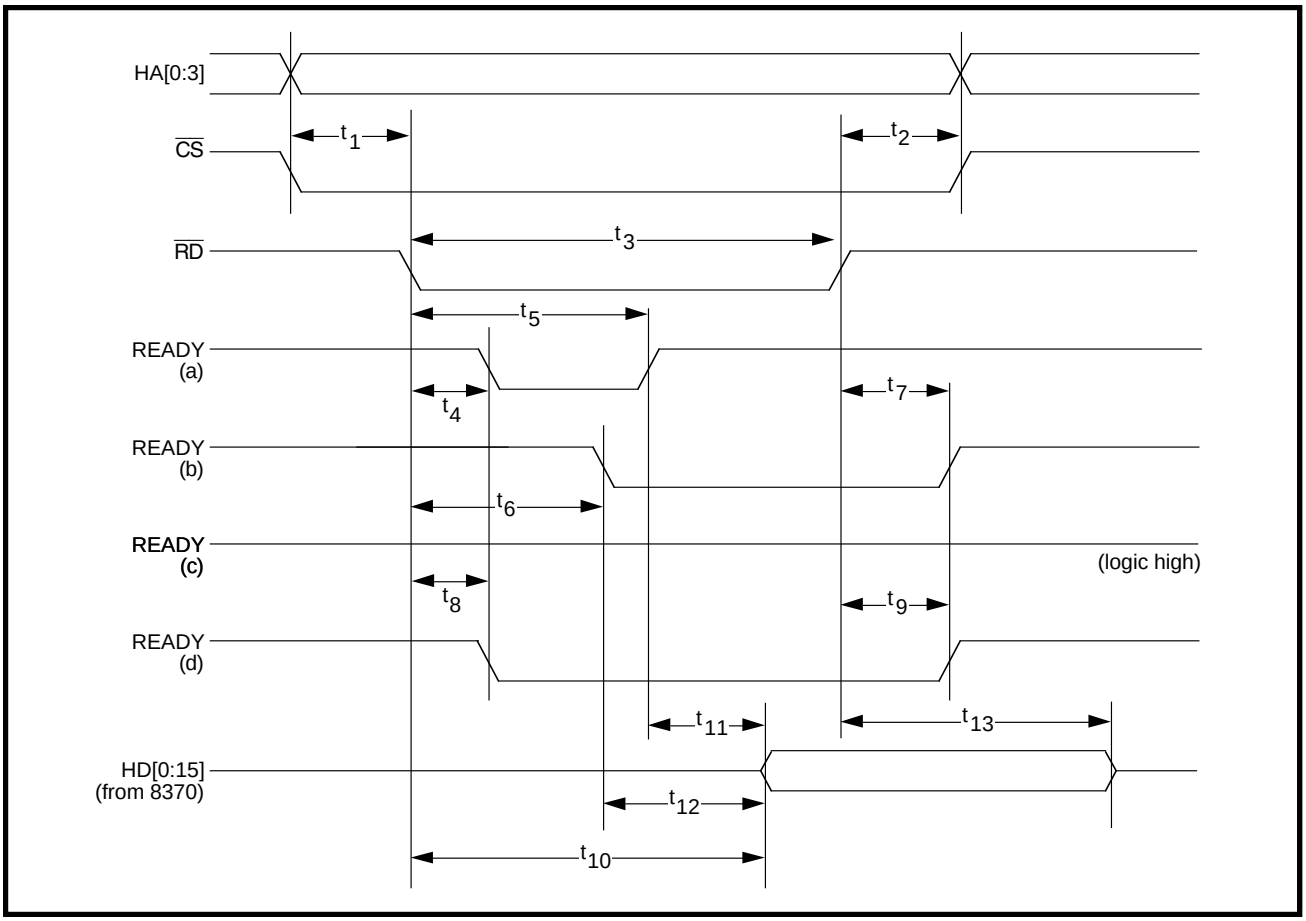


FIGURE 6: Read Cycle, Generic Bus Mode (Refer to Table 5)

TABLE 5: Read Cycle, Generic Bus Mode (Refer to Figure 6)

PARAMETER		CONDITIONS		MIN	NOM	MAX	UNIT
$\overline{CS}$ low to $\overline{RD}$ low; HA[0:3] valid to $\overline{RD}$ low	t_1			0			ns
$\overline{RD}$ high to $\overline{CS}$ high; $\overline{RD}$ high to HA[0:3] invalid	t_2			0			ns
$\overline{RD}$ low pulse width	t_3		Vdd = 5V	30			ns
			Vdd = 3.3V	35			ns
$\overline{RD}$ low to READY low	t_4	(a)	Vdd = 5V	0		35	ns
			Vdd = 3.3V			45	ns
$\overline{RD}$ low to READY high (1)	t_5	(a)				350	ns
$\overline{RD}$ low to READY low (1)	t_6	(b)		0		350	ns
$\overline{RD}$ high to READY high	t_7	(b)		0		25	ns
$\overline{RD}$ low to READY low	t_8	(d)	Vdd = 5V	0		30	ns
			Vdd = 3.3V			40	ns
$\overline{RD}$ high to READY high	t_9	(d)		0		28	ns
$\overline{RD}$ low to HD[0:15] valid	t_{10}	Register access	Vdd = 5V			45	ns
			Vdd = 3.3V			60	ns
READY high to HD[0:15] valid	t_{11}	Port access				5	ns
READY low to HD[0:15] valid	t_{12}	Port access				5	ns
$\overline{RD}$ high to HD[0:15] invalid (data hold)	t_{13}			10			ns

Note: (1) Maximum of 350 ns may occur if system makes contiguous system read cycles at less than 100 ns intervals, and both the transmitter and receiver are active in “loopback” reception (if the transmitter and receiver are idle, the max value becomes 250 ns). 2.4 µs max for host read error.
(a) For Buffer Memory Port when port is busy and RDYSEL = 1.
(b) For Buffer Memory Port when port is busy and RDYSEL = 0.
(c) For register or port is not busy and RDYSEL = 1.
(d) For register or port is not busy and RDYSEL = 0.

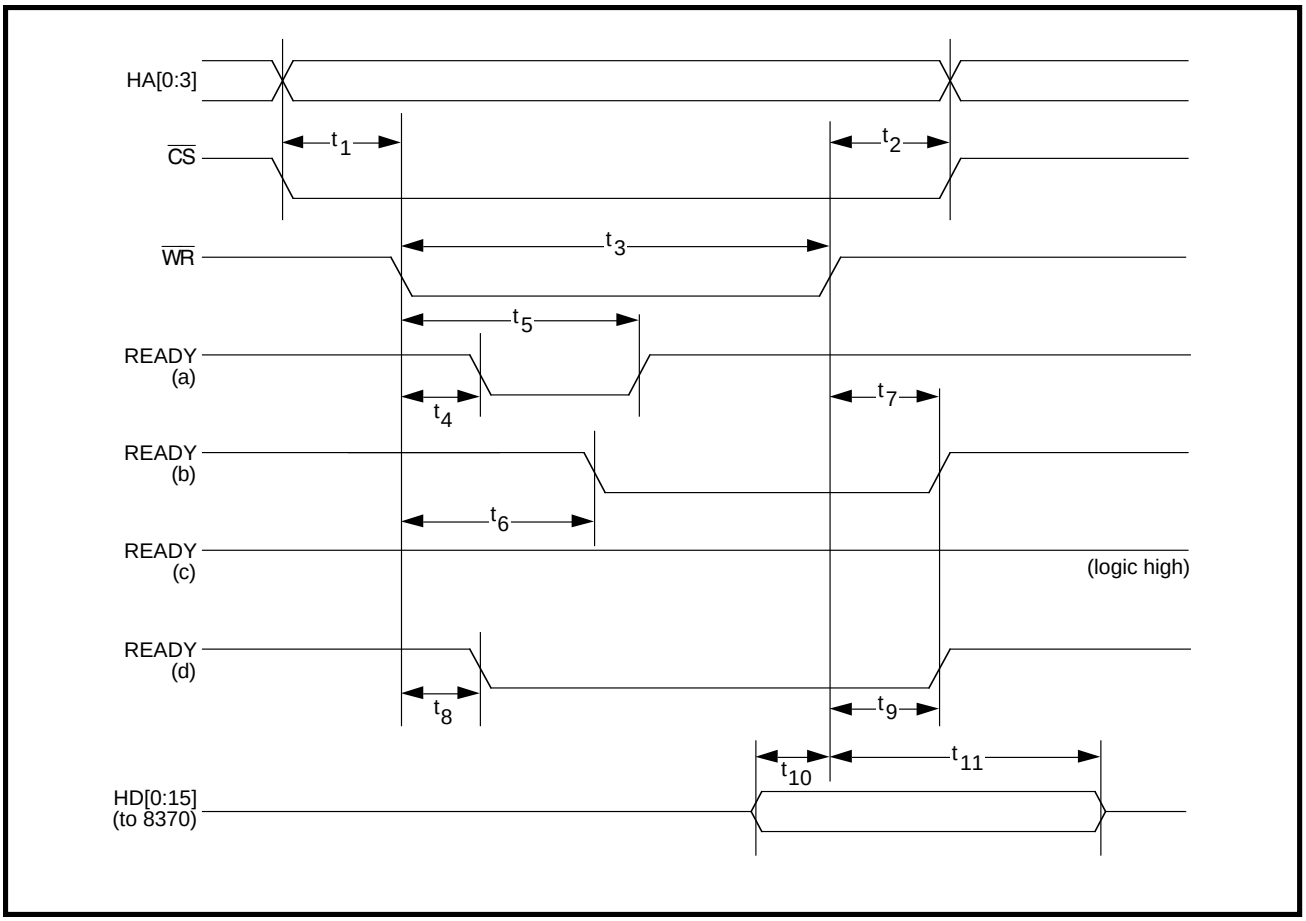


FIGURE 7: Write Cycle, Generic Bus Mode (Refer to Table 6)

TABLE 6: Write Cycle, Generic Bus Mode (Refer to Figure 7)

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNIT
$\overline{CS}$ low to $\overline{WR}$ low; HA[0:3] valid to WR low	t_1		0			ns
$\overline{WR}$ high to $\overline{CS}$ high; $\overline{WR}$ high to HA[0:3] invalid	t_2		0			ns
$\overline{WR}$ low pulse width	t_3	Vdd = 5V	30			ns
		Vdd = 3.3V	35			ns
$\overline{WR}$ low to READY low	t_4	(a) Vdd = 5V	0		35	ns
		Vdd = 3.3V			45	ns
$\overline{WR}$ low to READY high (1)	t_5	(a)			350	ns
$\overline{WR}$ low to READY low (1)	t_6	(b)	0		350	ns
$\overline{WR}$ high to READY high	t_7	(b)			28	ns
$\overline{WR}$ low to READY low	t_8	(d) Vdd = 5V	0		30	ns
		Vdd = 3.3V			40	ns
$\overline{WR}$ high to READY high	t_9	(d)	0		25	ns
HD[0:15] valid to WR high (data setup)	t_{10}		15			ns
$\overline{WR}$ high to HD[0:15] invalid (data hold)	t_{11}		10			ns

Note: (1) Maximum of 350 ns may occur if system makes contiguous system read cycles at less than 100 ns intervals, and both the transmitter and receiver are active on “loopback” reception (if the transmitter and receiver are idle, the max value becomes 250 ns). 2.4 µs max for host write error.
(a) For Buffer Memory Port when port is busy and RDYSEL = 1.
(b) For Buffer Memory Port when port is busy and RDYSEL = 0.
(c) For register or port is not busy and RDYSEL = 1.
(d) For register or port is not busy and RDYSEL = 0.

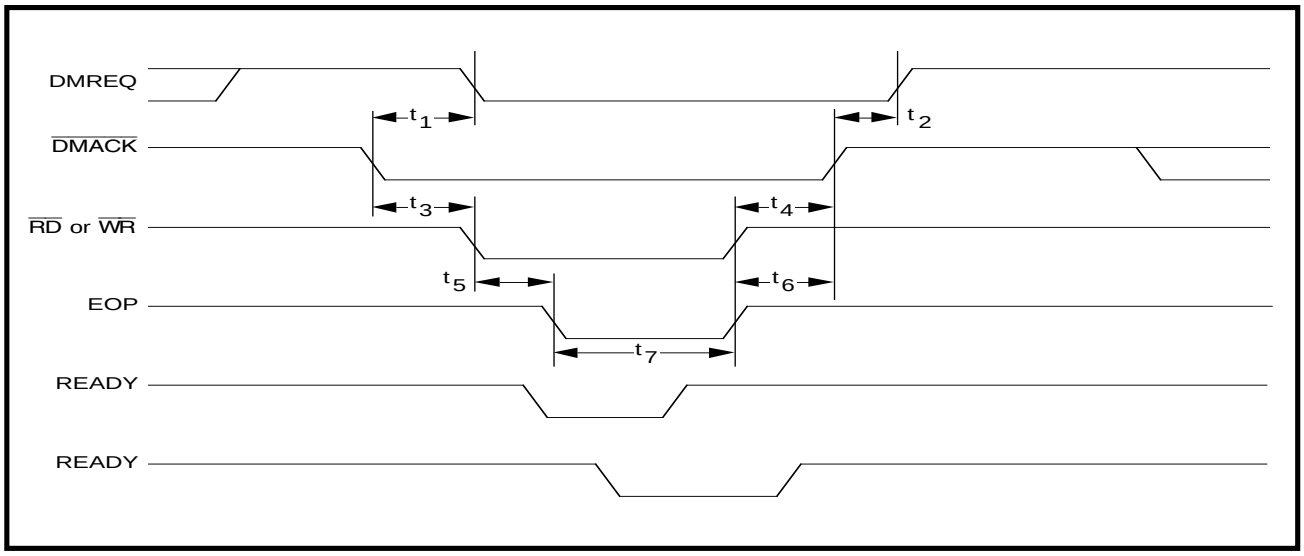


FIGURE 8: Single-Cycle DMA Timing

TABLE 7: Single-Cycle DMA Timing (Refer to Figure 8)

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNIT
$\overline{DMACK}$ low to DMREQ low	t_1	Vdd = 5V	0		25	ns
		Vdd = 3.3V			30	ns
$\overline{DMACK}$ high to DMREQ high	t_2	Vdd = 5V	0		25	ns
		Vdd = 3.3V			30	ns
$\overline{DMACK}$ low to $\overline{RD}$ or $\overline{WR}$ low	t_3		0			ns
$\overline{RD}$ or $\overline{WR}$ high to $\overline{DMACK}$ high	t_4		0			ns
$\overline{RD}$ or $\overline{WR}$ low to EOP low	t_5		0			ns
EOP high to $\overline{DMACK}$ high	t_6		0			ns
EOP low pulse width	t_7		10			ns

Note: (1) An asserted EOP terminates any further DMREQ after $\overline{DMACK}$ returns high.
(2) The DMA cycle uses $\overline{DMACK}$ as the chip select. $\overline{DMACK}$ overrides $\overline{CS}$ and HA[0:3] if they are both asserted at the same time, forcing selection of the Buffer Memory Port as in a DMA cycle.
(3) For READY timing and HD[0:15] timing, see Figure 6, t_4-t_{13}, and Figure 7, t_4-t_{11}.

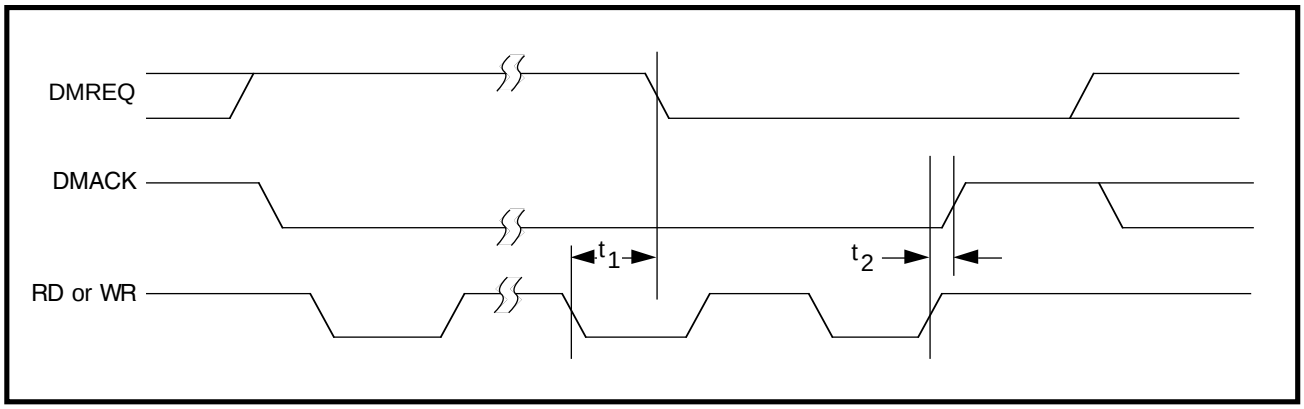


FIGURE 9: Burst DMA Timing

TABLE 8: Burst DMA Timing

PARAMETER	CONDITIONS		MIN	NOM	MAX	UNIT
$\overline{RD}$ or $\overline{WR}$ low to DMREQ low	5V	t_1			30	ns
	3.3V	t_1			40	ns
$\overline{RD}$ or $\overline{WR}$ high to DMACK high		t_2	0			ns

Note: (1) DMREQ goes low during the next-to-last transfer of the burst. $\overline{DMACK}$ should not go high until after the $\overline{RD}$ or $\overline{WR}$ pulse of the last transfer cycle goes high
(2) The DMA cycle uses $\overline{DMACK}$ as the chip select. $\overline{DMACK}$ overrides $\overline{CS}$ and HA[0:3] if they are both asserted at the same time, forcing selection of the Buffer Memory Port as in a DMA cycle.
(3) For READY timing and HD[0:15] timing, see Figure 6, t_4-t_{13}, and Figure 7, t_4-t_{11}.

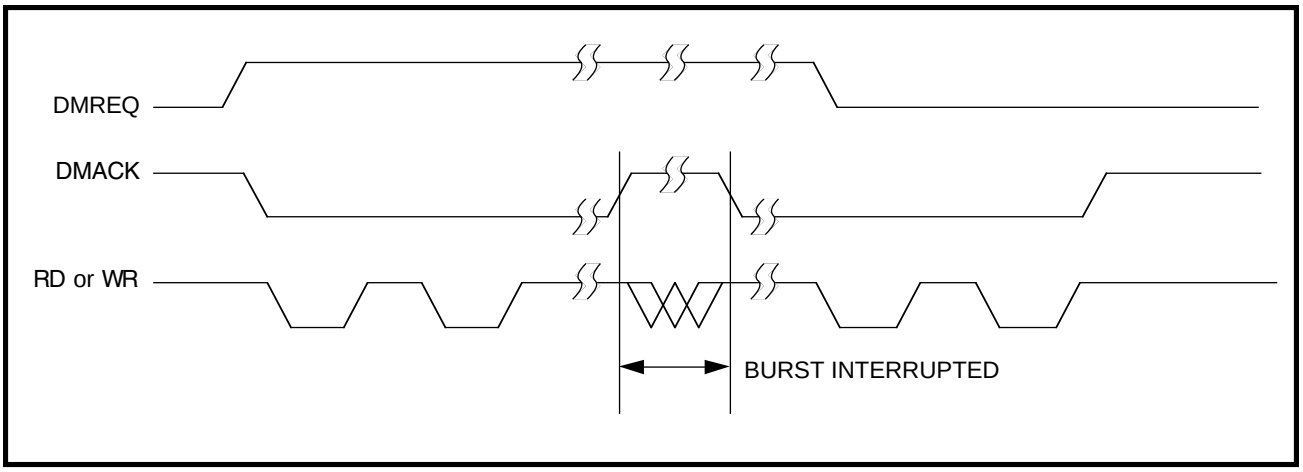


FIGURE 10: Burst DMA Interrupted by $\overline{\text{DMACK}}$

Note: Burst can be interrupted by $\overline{\text{DMACK}}$ high-going pulse during the burst. Burst will resume when $\overline{\text{DMACK}}$ returns low.

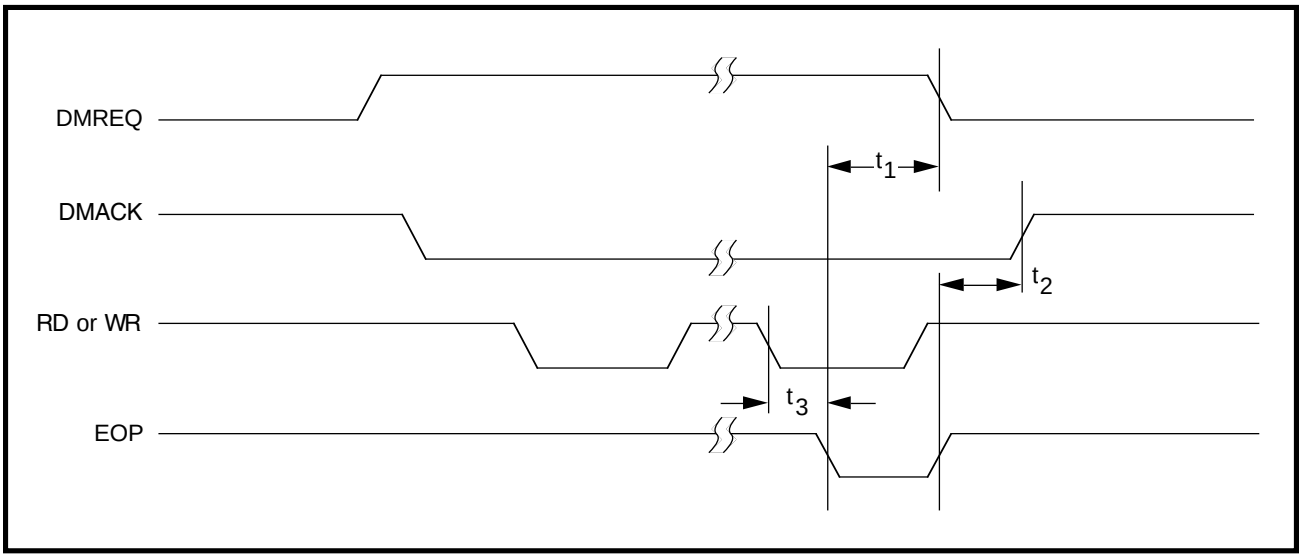


FIGURE 11: Burst DMA Terminated by EOP

TABLE 9: Burst DMA Terminated by EOP

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNIT
EOP low to DMREQ low	t_1	Vdd = 5V	4		28	ns
		Vdd = 3.3V			35	ns
EOP high to DMACK high	t_2		3			ns
RD or WR low to EOP low	t_3		0			ns

Note: EOP can be asserted during any transfer of the burst to terminate the process following that transfer.

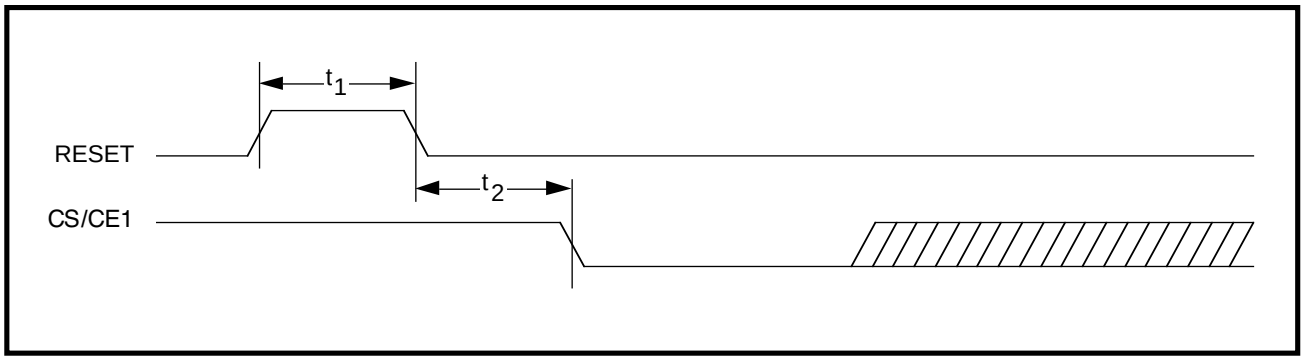


FIGURE 12: RESET Timing

TABLE 10: RESET Timing

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
RESET pulse width t_1		500			ns
RESET low to first $\overline{CS}/\overline{CE1}$ low t_2		800			ns

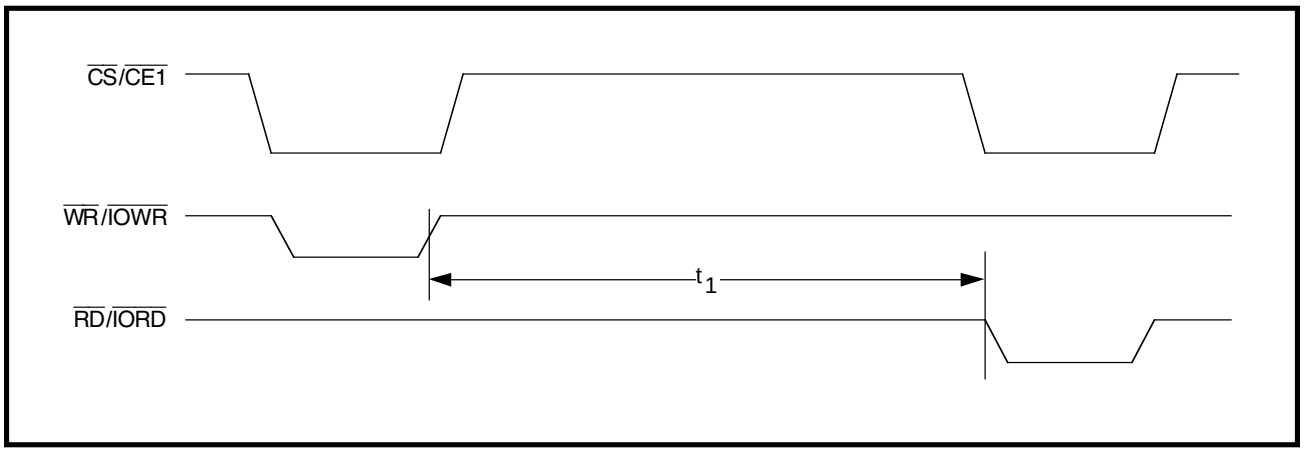


FIGURE 13: Skip Packet Timing

TABLE 11: Skip Packet Timing

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
Writing Skip Packet high to next Buffer Memory Port read t_1		200			ns

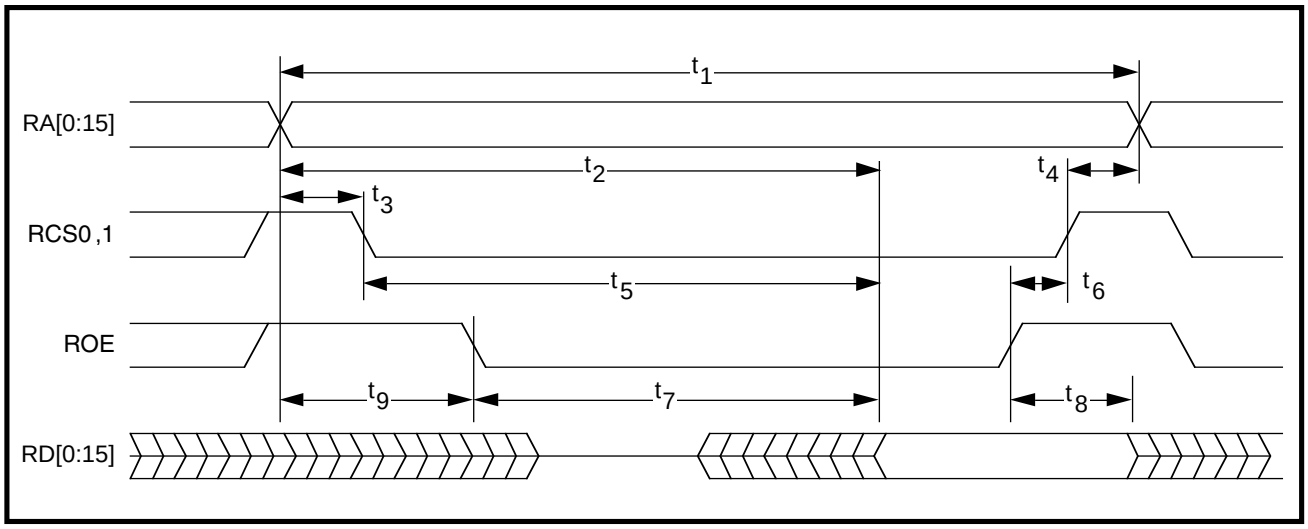


FIGURE 14: SRAM Read Timing

TABLE 12: SRAM Read Timing

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNIT
Read cycle	t_1	RAMSP = 1	95			ns
		RAMSP = 0	145			ns
Address access time	t_2	RAMSP = 1			75	ns
		RAMSP = 0			125	ns
Address valid to $\overline{RCS0}$,$\overline{1}$ low	t_3				8	ns
$\overline{RCS0}$,$\overline{1}$ high to address invalid	t_4		0			ns
Chip select access time	t_5	RAMSP = 1			75	ns
		RAMSP = 0			125	ns
$\overline{ROE}$ high to $\overline{RCS0}$,$\overline{1}$ high	t_6		0		8	ns
Output enable access time	t_7	RAMSP = 1			50	ns
		RAMSP = 0			100	ns
Data hold time	t_8		0			ns
Address valid to $\overline{ROE}$ low	t_9				30	ns

Note: Use SRAM with address access time of 75 ns or less for RAMSP = 1 and 125 ns or less for RAMSP = 0. RAMSP is DLCR6 <6>.

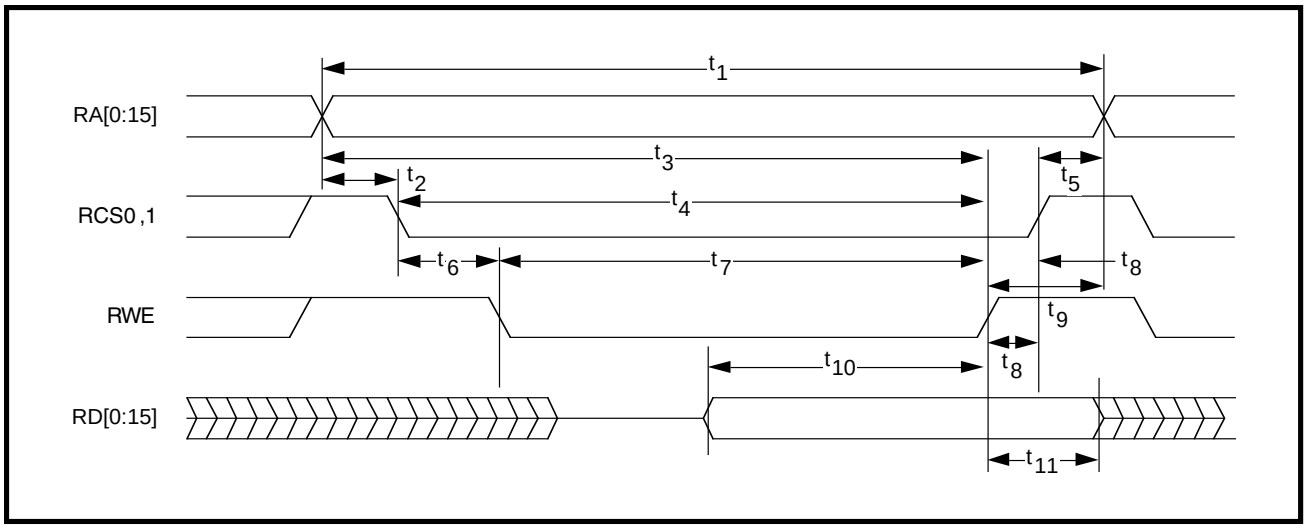


FIGURE 15: SRAM Write Timing

TABLE 13: SRAM Write Timing

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNIT
Write Cycle	t_1	RAMSP = 1	95			ns
		RAMSP= 0	145			ns
Address Valid to $\overline{RCS0,1}$ low	t_2				8	ns
Address Valid to $\overline{RWE}$ high	t_3	RAMSP = 1	70			ns
		RAMSP = 0	120			ns
$\overline{RCS0,1}$ low to $\overline{RWE}$ high	t_4	RAMSP = 1	70			ns
		RAMSP = 0	120			ns
$\overline{RCS0,1}$ high to Address Invalid	t_5		0			ns
$\overline{RCS0,1}$ low to $\overline{RWE}$ low	t_6		0			ns
$\overline{RWE}$ Pulse Width	t_7	RAMSP = 1	70			ns
		RAMSP = 0	120			ns
$\overline{RWE}$ high to $\overline{RCS0,1}$ high	t_8		0			ns
$\overline{RWE}$ high to Address Invalid	t_9		10			ns
Data Setup Time	t_{10}	RAMSP = 1	40			ns
		RAMSP = 0	90			ns
Data Hold Time	t_{11}		20			ns

Note: Use SRAM with address access time of 75 ns or less for RAMSP = 1 and 125 ns or less for RAMSP = 0. RAMSP is DLCR6 <6>.

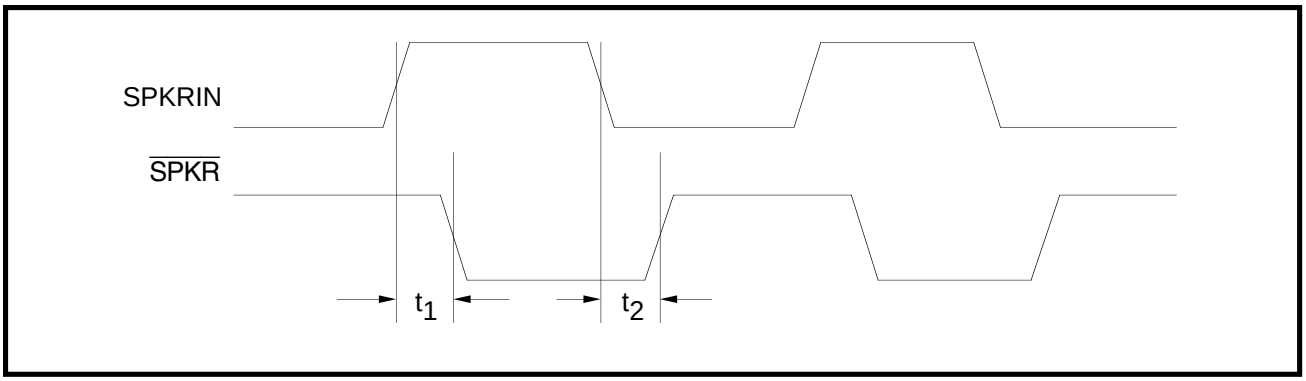


FIGURE 16: Speaker Timing

TABLE 14: Speaker Timing (Refer to Figure 16)

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
$\overline{SPKR}$	Vdd = 5V			25	ns
high to low propagation delay t_1	Vdd = 3.3V			30	ns
$\overline{SPKR}$	Vdd = 5V			25	ns
low to high propagation delay t_2	Vdd = 3.3V			30	ns

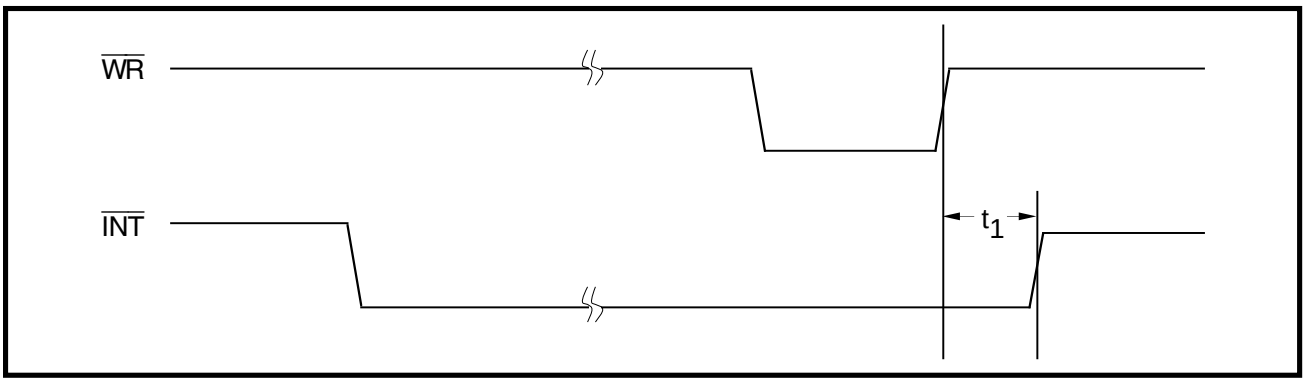


FIGURE 17: Interrupt Timing (Generic Bus Mode)

TABLE 15: Interrupt Timing (Generic Bus Mode)

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
$\overline{INT}$ t_1	Vdd = 5V	7		40	ns
signal cleaning delay	Vdd = 3.3V			50	ns

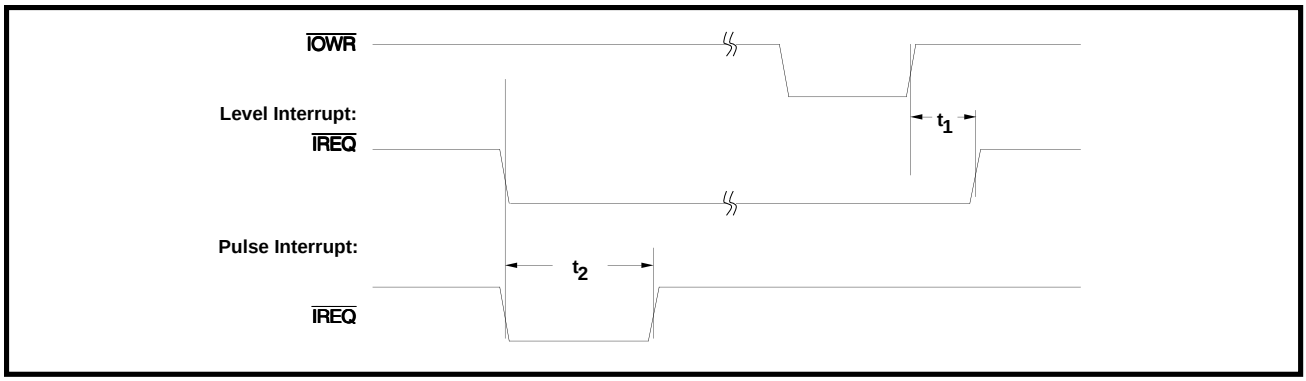


FIGURE 18: Interrupt Timing (PCMCIA Mode)

TABLE 16: Interrupt Timing (PCMCIA Mode)

PARAMETER		CONDITIONS		MIN	NOM	MAX	UNIT
$\overline{IREQ}$		level interrupt	Vdd = 5V	7		40	ns
signal clearing delay	t_1		Vdd = 3.3V			50	ns
$\overline{IREQ}$ low pulse width	t_2	pulse interrupt		750		800	ns

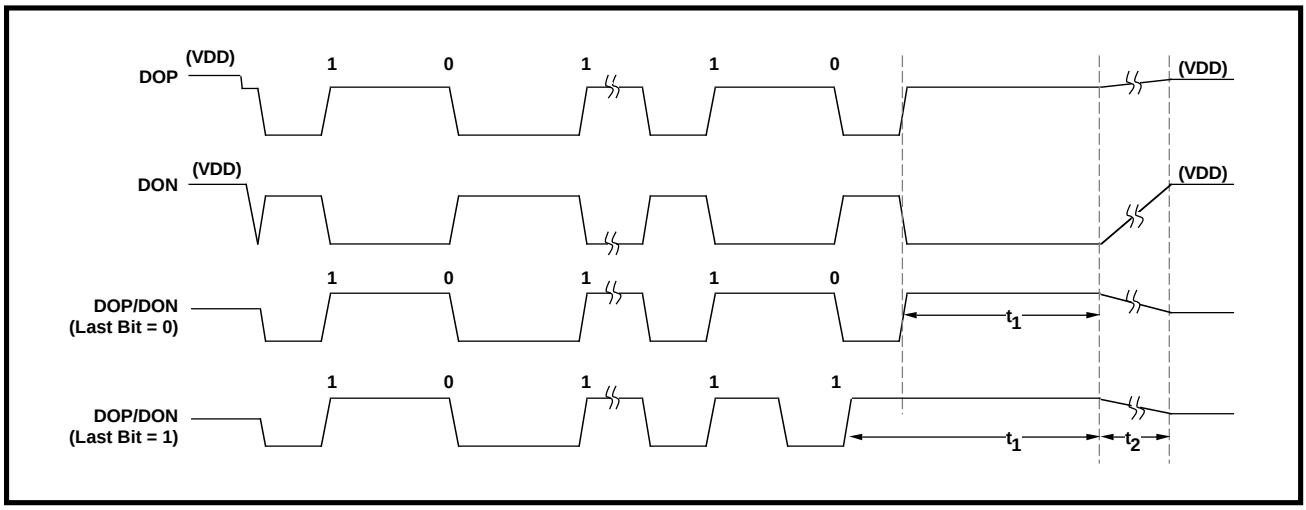


FIGURE 19: Transmit Timing (AUI)

TABLE 17: Transmit Timing (AUI)

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNIT
DOP/DON end-of-packet delimiter	t_1		200			ns
DOP/DON line voltage transition	t_2				8	µs

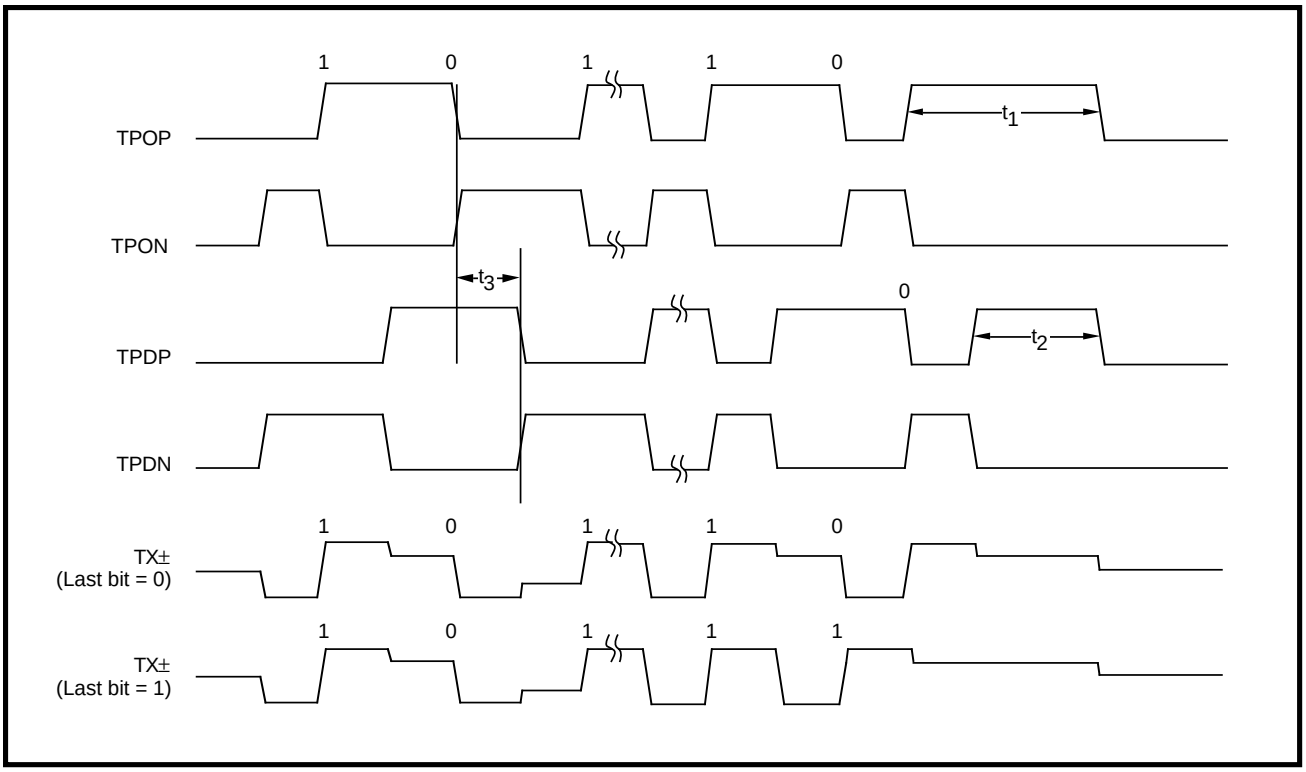


FIGURE 20: Transmit Timing (TP)

TABLE 18: Transmit Timing (TP)

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
TPOP/TPON end-of-packet delimiter t_1		250			ns
TPDP/TPDN end-of-packet delimiter t_2		200			ns
TPOP to TPDP and TPON to TPDN delay t_3			50		ns

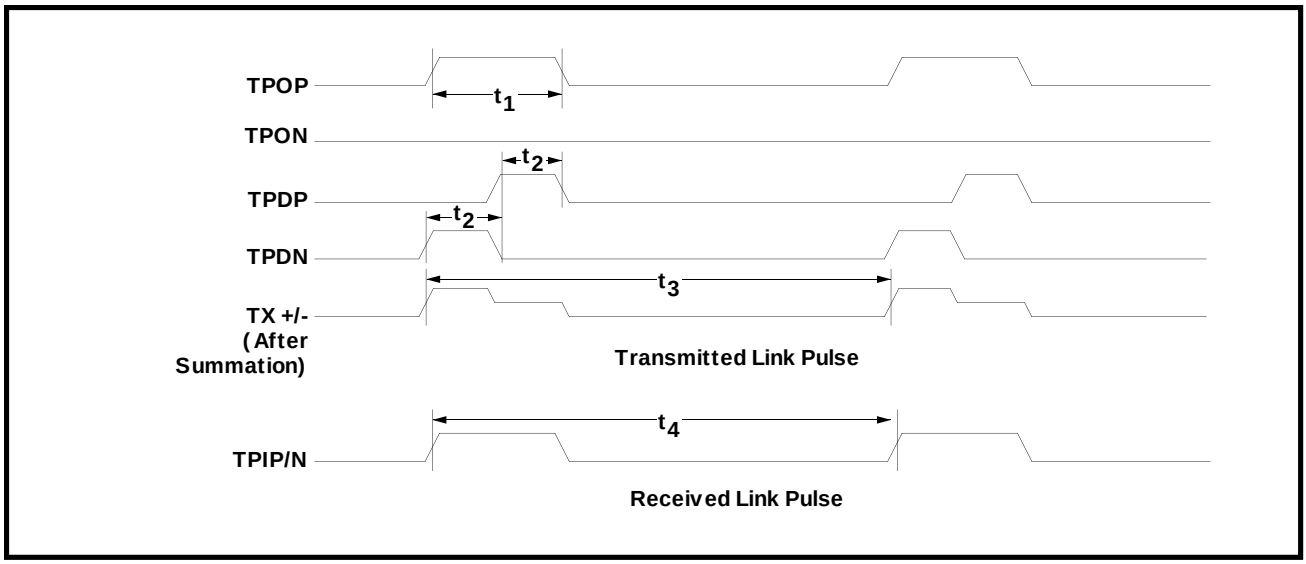


FIGURE 21: Link Test Timing

TABLE 19: Link Test Timing

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNIT
TPOP link pulse width	t_1			150		ns
TPDP/TPDN link pulse width	t_2			100		ns
Duration between transmitted link pulses	t_3		9		11	ms
Duration between received link pulses	t_4		4.1		65	ms

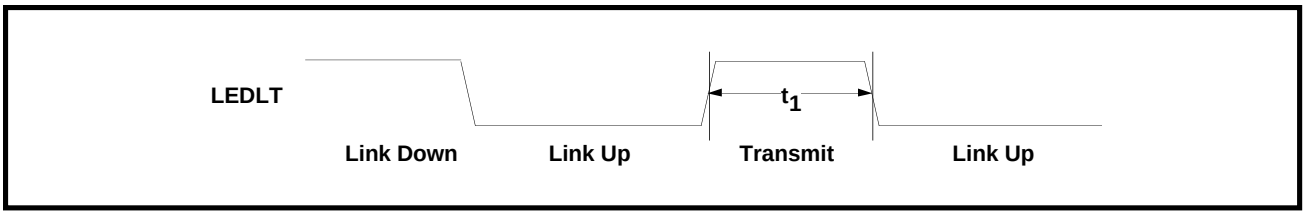


FIGURE 22: LED Timing (TP)

TABLE 20: LED Timing

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNIT
Transmit blink-off timing	t_1	TP selected		100		ms

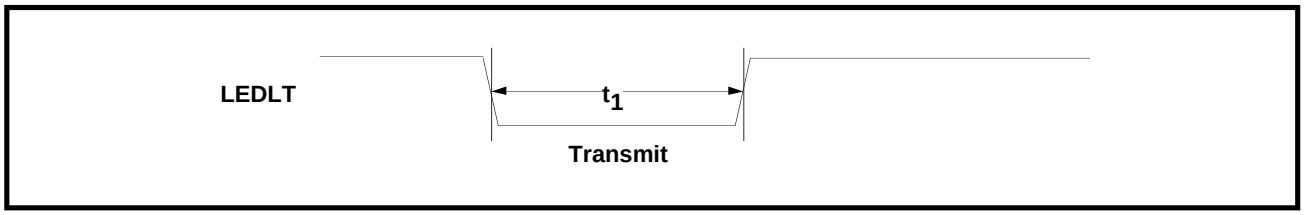


FIGURE 23: LED Timing (AUI)

TABLE 21: LED Timing

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNIT
Transmit blink-on timing	t_1	AUI selected		100		ms

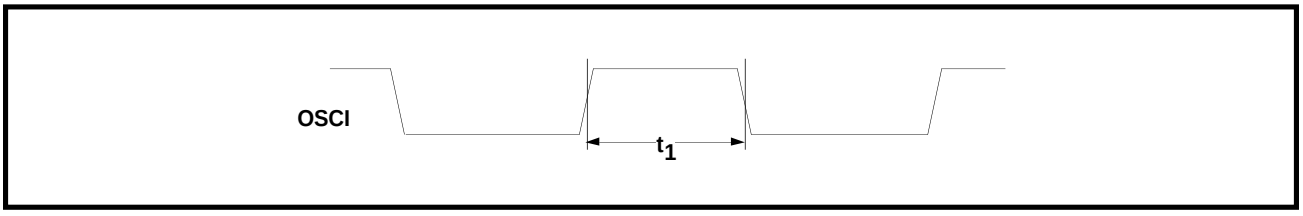


FIGURE 24: Oscillator Duty Cycle

TABLE 22: OSCI Duty Cycle

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNIT
Oscillator duty cycle	t_1		40	50	60	%

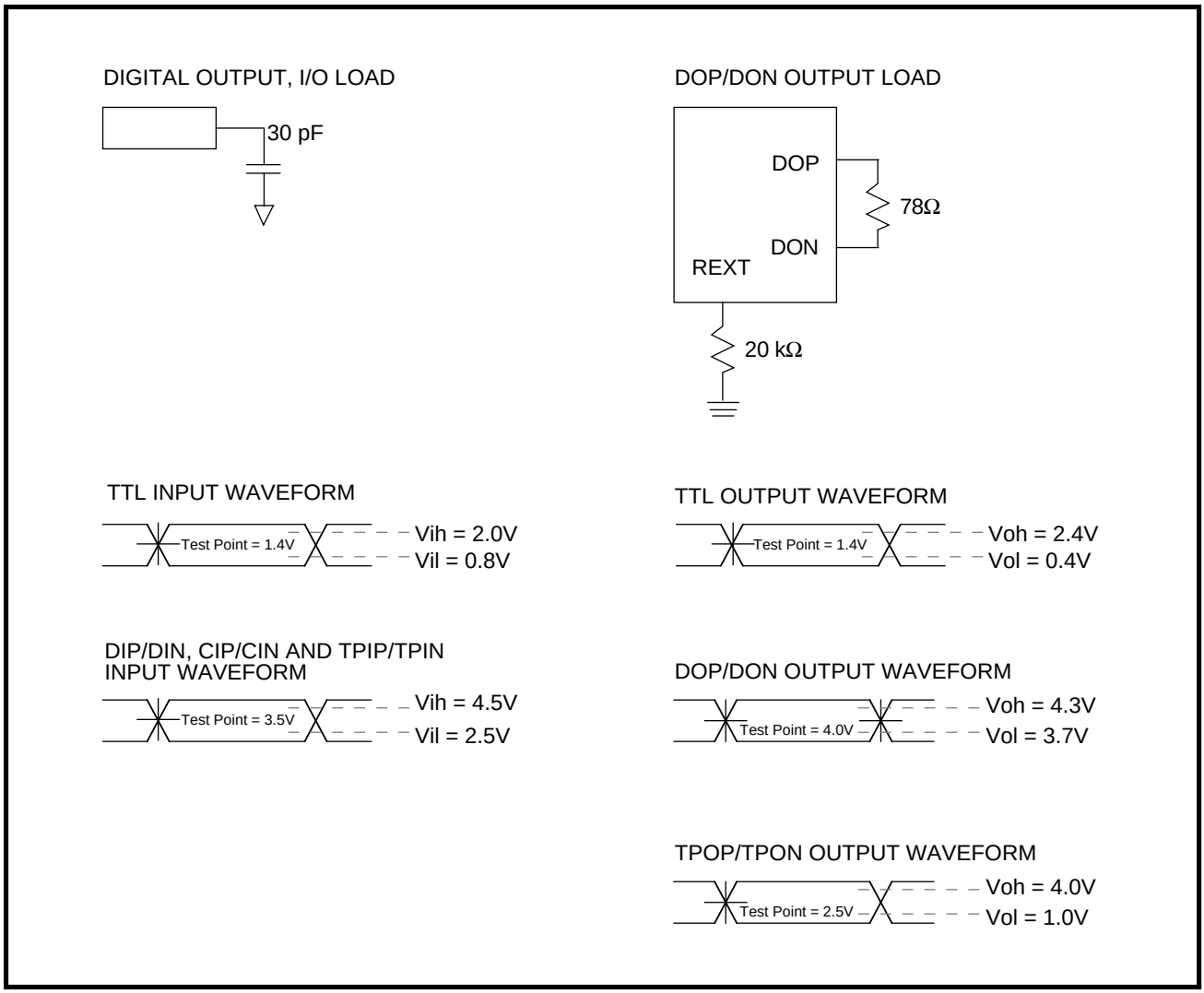
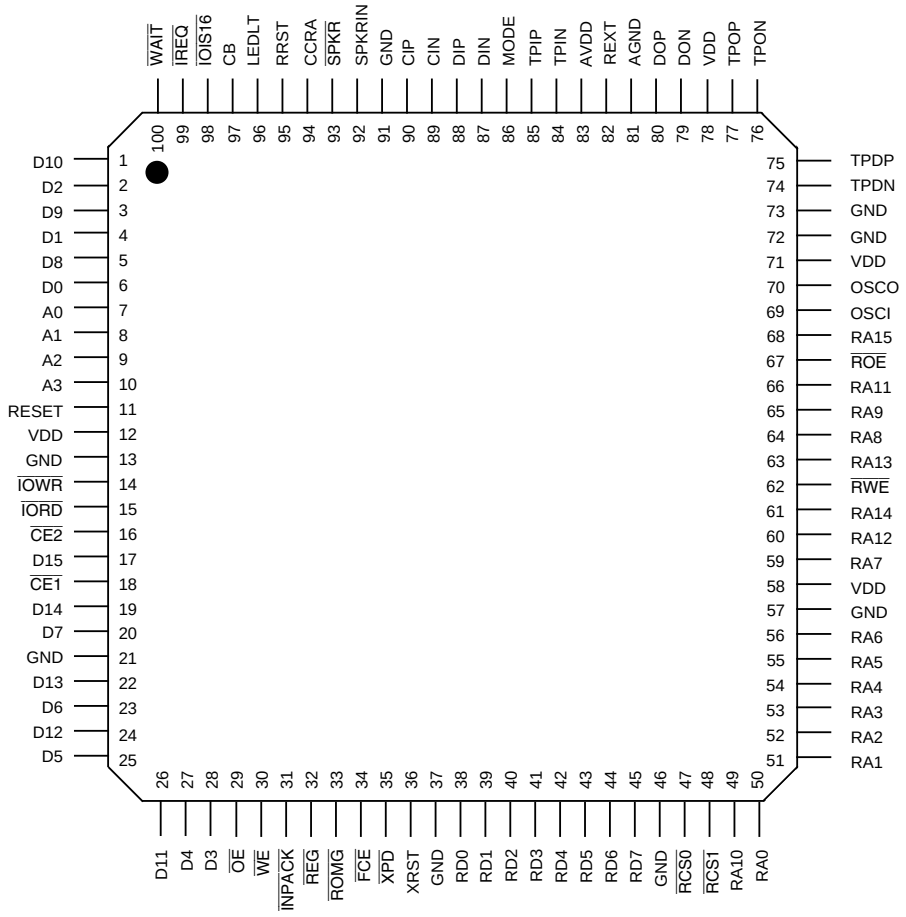


FIGURE 25: Test Conditions

PACKAGE PIN DESIGNATIONS

(Top View)

CAUTION: Use handling procedures necessary for a static sensitive component.



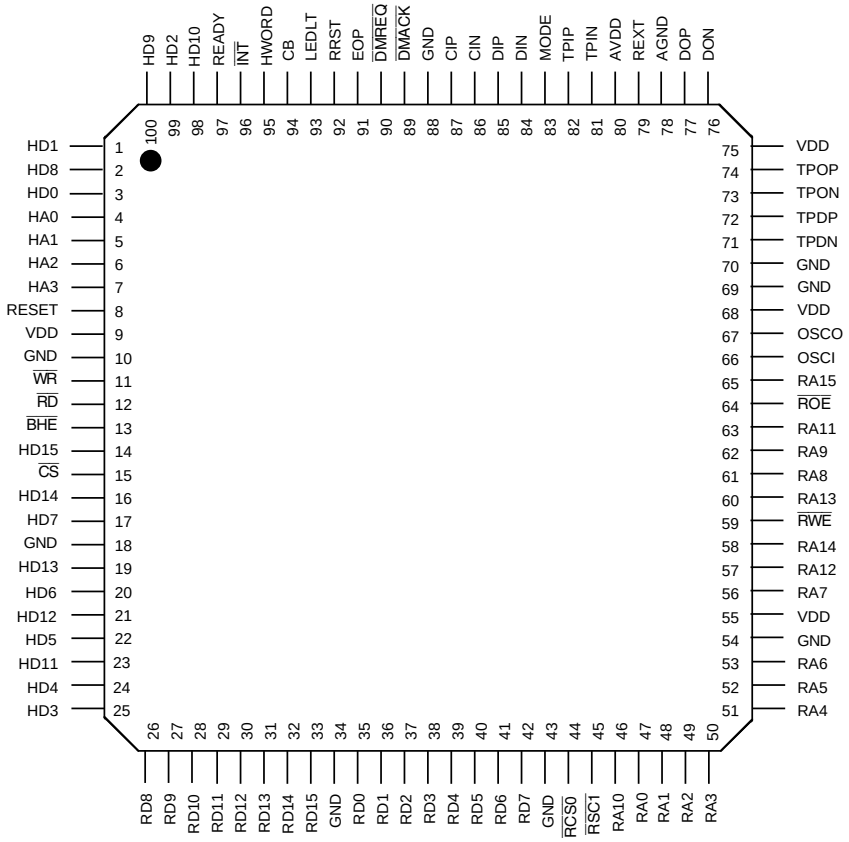
100-Lead TQFP
PCMCIA Bus Mode

SSI 78Q8373
3V, 5V PCMCIA
Ethernet Combo

PACKAGE PIN DESIGNATIONS

(Top View)

CAUTION: Use handling procedures necessary for a static sensitive component.



100-Lead TQFP
Generic Bus Mode

ORDERING INFORMATION

PART DESCRIPTION	ORDER NUMBER	PACKAGE MARK
SSI 78Q8373 - PCMCIA Ethernet Combo 100-lead QFP	78Q8373-CG	78Q8373-CG
100-lead78Q8373TQFP	78Q8373-CGT	78Q8373-CGT

Preliminary Data: Indicates a product not completely released to production. The specifications are based on preliminary evaluations and are not guaranteed. Small quantities are available, and Silicon Systems should be consulted for current information.

Silicon Systems, Inc., 14351 Myford Road, Tustin, CA 92680-7022 (714) 573-6000, FAX (714) 573-6914

silicon systems®
A TDK Group Company

SSI 78Q8377A
10BaseT Ethernet Combo for Plug and Play

Preliminary Data

November 1995

DESCRIPTION

The SSI 78Q8377A is a highly integrated Ethernet IC for use in Ethernet Network Interface Cards (NICs) in the ISA/NEC PC-98 Plug and Play (PnP) environment. It contains a full-duplex Media Access Controller (MAC), a 10 Mbit/s Manchester encoder/decoder (ENDEC), a 10BaseT transceiver, ISA/NEC PC-98 bus interface and an Attachment Unit Interface (AUI). The only external components required to build an Ethernet adapter card with the 78Q8377A are buffer memory, a serial EEPROM and a few passive components. In full duplex operation, transmission line throughput doubles to the theoretical 20 Mbit/s. In this mode, the collision detection, SQE generation and carrier deference are disabled.

The 78Q8377A has an integrated ISA and NEC PC-98 bus interface that physically connects to the bus without any additional glue logic. The 78Q8377A is defined with "jumperless" configuration in mind. The configuration information is stored in serial EEPROM.

The 78Q8377A fully supports the PnP ISA specification. The PnP logic can also be bypassed through a bit in the EEPROM. When the PnP logic is bypassed, the 78Q8377A will power up active after loading the necessary configuration information from the serial EEPROM.

The popular microwire (4-wire) interface is supported by the 78Q8377A to connect to serial EEPROM, which contains configuration information such as I/O Base address, Boot Device address, IRQ selection, MAC address, etc. Reading of essential configuration information like the I/O Base address and Boot Device address is done automatically by the 78Q8377A. The driver software is then responsible to read the rest of the information and program the 78Q8377A registers with the appropriate values read.

The 78Q8377A allows for a diskless station to boot from the installed boot device. The boot feature can also be disabled through a bit in the serial EEPROM. Both read-only and read-write (e.g., flash) memory are supported by the 78Q8377A. Furthermore, accidental write to the flash can be prevented through a write protect register bit.

FEATURES

- **Highly integrated Ethernet combo for Plug and Play (PnP) applications**
- **Integrated ISA and NEC PC-98 bus interface with PnP registers, compliant with PnP spec version 1.0a**
- **Compliant with Windows 95 and PC95 requirements**
- **"Glueless" and "jumperless" connection to ISA and NEC PC-98 bus**
- **Integrated 10Base-T transceiver:**
  - **Programmable/automatic selection of twisted pair (RJ45) or AUI port**
  - **Receive polarity detection/correction on twisted-pair inputs**
- **Manchester Encoder/Decoder circuit**
- **AUI port for connection to 10Base2/5 transceiver or AUI cable**
- **Programmable Full Duplex operation**
- **Serial EEPROM support with MICROWIRE (four wire) interface**
- **Supports both PnP and non-PnP environment through an EEPROM bit**
- **Integrated 24 mA data bus buffer**
- **Boot Device (either read-only or read-write memory) support through an external data buffer ('245) in ISA mode**
- **Numerous I/O base address selection in 16 bytes increment**
- **8 interrupt lines selection**
  Supports edge and level-sensitive interrupts
  Tri-state implementation allows sharing of interrupts for both modes
- **Register compatible to the SSI 78Q8373**
- **Power management options:**
  - **Intelligent power mode automaticallyshuts off unused circuitry**
  - **Standby mode reduces power while not in operation**
  - **Extensive LED indicator**
  - **Full shutdown mode offers maximum power savings**
  - **16-bit address decoding**
- **128-lead QFP package and single 5V supply**

FUNCTIONAL DESCRIPTION

The 78Q8377A consists of six major blocks as shown in Figure 1.

- Buffer Manager (and SRAM Interface)
- Data Link Controller
- ISA Bus Interface
- Manchester ENDEC
- Twisted Pair Transceiver
- Power Management

BUFFER MANAGER

The Buffer Manager manages all accesses to the buffer memory through the SRAM interface. The buffer memory is connected directly to the Data Link Controller (DLC), thus eliminating the need for a local microprocessor. The Buffer Manager also keeps track of all buffer memory pointers automatically, simplifying the software driver task. Together with intelligent arbitration, this makes the 78Q8377A a high performance LAN controller.

The buffer memory is divided into two portions: transmit memory portion and receive memory portion. The transmit memory portion can be partitioned into 2K, 4K, 8K or 16 Kbyte buffer sizes. There is only one transmit bank if a 2 KB transmit buffer size is selected. If the transmit buffer size is greater than 2 KB, then the transmit buffer is configured into two banks of equal size. With the two bank configuration, one transmit bank may be tied up during transmission but the host can still continue to load data packets into the second transmit bank to be transmitted later. The receive buffer has a ring architecture which can be configured from 4K to 62 KB depending on the buffer memory configuration which has a range of 8K to 64 KB.

A central arbitrator inside the Buffer Manager prioritizes and services requests for access to the buffer memory from 4 sources: the Transmitter, the Receiver, Host Read and Host Write. If necessary, the 78Q8377A will assert a 'not ready' handshake to the host while servicing the Transmitter and/or Receiver. The 78Q8377A arbitration mechanism provides packet management by interleaving packet data accesses to the buffer memory such that the operations appear to be simultaneous.

For instance, in the situation where 2 transmit banks are configured, the host can load the first transmit bank and initiate a transmission. While the first transmit bank is being transmitted, the host can continue to load packets in the second transmit bank. At this stage, the 78Q8377A can potentially be receiving data from the medium and loading it into the receive buffer (full duplex 10BaseT operation, or if the 78Q8377A is in a loop back mode or if self-reception occurs).

DATA LINK CONTROLLER

The Data Link Controller (DLC) implements the ISO/ ANSI/IEEE 8802-3 CSMA/CD protocol. It consists of a Transmitter, a Receiver and CRC logic. Automatic generation and stripping of the 64-bit preamble and the 32-bit CRC code are provided on-chip.

The 78Q8377A now includes support for Full Duplex operation making the line throughput to 20 Mbit/s. In this mode, the collision detection and carrier deference are disabled. In addition to that, the Twisted Pair transceiver SQE generation and "natural" loopback are also turned off.

ISA AND NEC PC-98 INTERFACE

The 78Q8377A has an integrated ISA and NEC PC-98 interface that physically connects to both bus without any additional glue logic. The ISA pin is used to select between the two bus interfaces. The data bus buffers (24 mA) have also been integrated on chip. The 78Q8377A is defined with "jumperless" configuration in mind. The configuration information is stored in the serial EEPROM.

PnP Logic

The 78Q8377A fully supports the Plug and Play (PnP) Specification for the ISA system. The PnP logic can also be by-passed through the PnP_ACT bit in the EEPROM. This allows the 78Q8377A to work in both non-PnP as well as PnP environment. When the PnP logic is by-passed, the 78Q8377A will power up active after loading the necessary configuration information from the serial EEPROM.

Serial EEPROM Interface

The popular MICROWIRE (four wire) interface is supported by the 78Q8377A to connect to serial EEPROM. The compatible EEPROM includes 93C56 and 93C66. The serial EEPROM is used to store a number of information: I/O base address, Boot Device address, IRQ selection, MAC address, 78Q8377A register specific setting and PnP related data and control. The reading of the essential configuration information in the serial EEPROM like the I/O base address, Boot Device address and IRQ selection are done automatically by the 78Q8377A. The software driver is then responsible to read the rest of the information and program the 78Q8377A registers with the appropriate values read. Three register bits are provided as the interface points to the serial EEPROM; one for the chip select, one for the clock and the other for the data.

Optional Boot Device Support

In ISA mode 78Q8377A allows for diskless station to boot from the installed Boot Device. It supports 8 memory base addresses for the Boot Device with 16 Kbytes memory size or 4 memory base addresses with 32 Kbytes size or 2 memory base addresses with 64 Kbytes size. The boot feature can also be disabled through a bit in the serial EEPROM. Both read-only and read-write (eg. Flash) memory are supported by the 78Q8377A. Furthermore, accidental write to the Flash can be prevented through a write protect register bit. Due to the low current drive capability of the boot device (normally 2 mA and ISA specifies 24mA), a data buffer (‘245) is needed to isolate the boot device from the bus. The 78Q8377A provides the necessary control pins to the data buffer and the boot device.

MANCHESTER ENDEC

This block implements Manchester encoding and decoding. Serial NRZ data from the DLC is converted to Manchester encoded data and sent to either the twisted-pair transceiver block or to the Attachment Unit Interface (AUI) driver, depending on which block is active. The decoder section performs three functions: clock recovery, carrier detection and Manchester decoding. The recovered receive clock will be low at the end of reception and during idle to save power. Jitter of up to ±18 ns can be tolerated by the decoder. This block also translates a 10 MHz collision signal to a logic-level signal before sending it to the DLC block if the AUI port is selected.

TWISTED PAIR TRANSCEIVER

The on-chip Twisted Pair module consists of a number of functions. It has a smart squelch circuitry to determine valid data present on the differential receive inputs TPIP/TPIN. Its transmit and pre-distortion drivers connect to the twisted pair network via the summing resistors and transformer/filter. The link detector/ generator circuitry checks the integrity of the cable connecting the two twisted pair MAUs. Collision, jabber and SQE are also incorporated.

The 78Q8377A now includes support for Full Duplex operation making the line throughput to 20 Mbit/s. In this mode, the collision detection and carrier deference are disabled. In addition to that, the Twisted Pair transceiver SQE generation and “natural” loopback are also turned off.

POWER MANAGEMENT

One very useful and important feature that the 78Q8377A offers is intelligent power management. It supports three different power saving modes: Intelligent, Standby, and Full Shutdown. All modes are configurable through registers. In the Intelligent mode, clocks are active only when they are needed. For example, when not transmitting, the clock supplied to the transmitter circuit in the DLC block is not active while host read from buffer memory may be active. In Standby mode, the oscillator clock is disconnected from the rest of the circuits, so that only the oscillator circuits draw power. Full Shutdown turns off the oscillator, resulting in maximum power savings. Note that this mode is not available when using an external clock source.

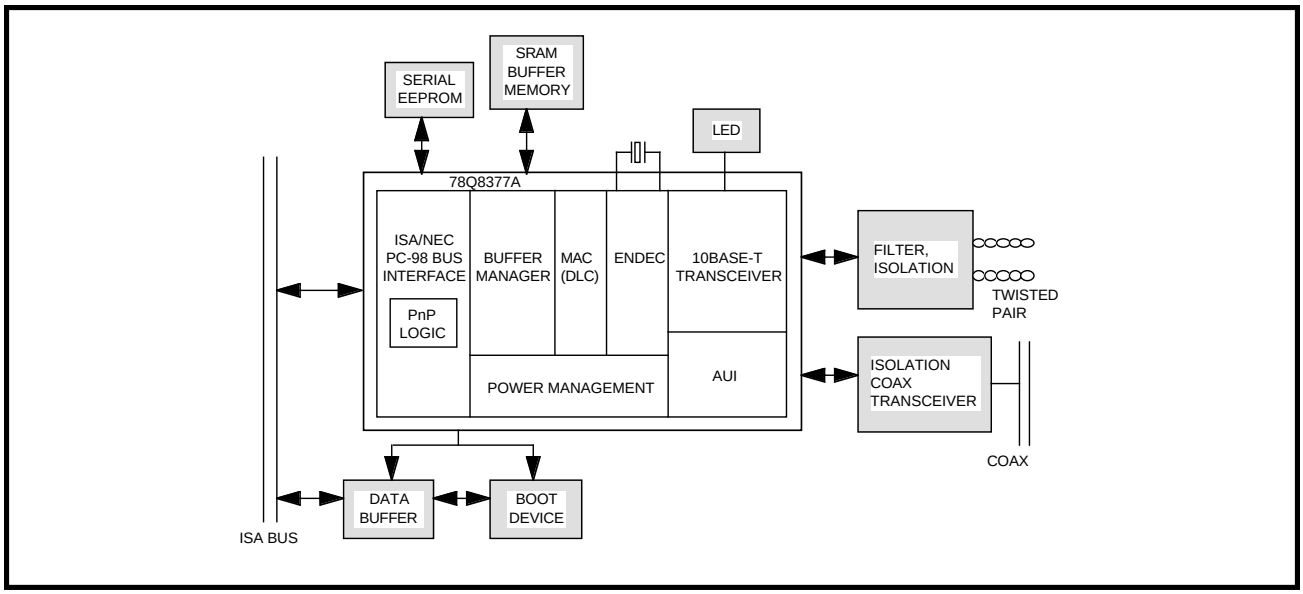


FIGURE 1: System Diagram

Pin Assignment Table (ISA bus)

PIN#	PIN NAME	TYPE	PIN#	PIN NAME	TYPE	PIN#	PIN NAME	TYPE	PIN#	PIN NAME	TYPE
1	RA1	04	33	$\overline{\text{IRQ5}}$	OT24	65	TPON	AO	97	RD14	IO2
2	RA0	04	34	$\overline{\text{IRQ4}}$	OT24	66	TPOP	AO	98	RD13	IO2
3	VSSIO	G	35	$\overline{\text{IRQ3}}$	OT24	67	VDDT	P	99	RD12	IO2
4	VDDIO	P	36	VSSC	G	68	DON	AO	100	RD11	IO2
5	SD15	IO24	37	SA0	I	69	DOP	AO	101	RD10	IO2
6	SD14	IO24	38	SA1	I	70	VSSA	G	102	RD9	IO2
7	SD13	IO24	39	SA2	I	71	RBIAS	R	103	RD8	IO2
8	SD12	IO24	40	SA3	I	72	VDDA	P	104	VSSIO	G
9	VSSIO	G	41	SA4	I	73	TPIN	AI	105	RD7	IO2
10	SD11	IO24	42	SA5	I	74	TPIP	AI	106	RD6	IO2
11	SD10	IO24	43	SA6	I	75	CIN	AI	107	RD5	IO2
12	SD9	IO24	44	SA7	I	76	CIP	AI	108	RD4	IO2
13	SD8	IO24	45	SA8	I	77	DIN	AI	109	RD3	IO2
14	VSSIO	G	46	SA9	I	78	DIP	AI	110	RD2	IO2
15	SD0	IO24	47	VDDC	P	79	VSSC	G	111	RD1	IO2
16	SD1	IO24	48	SA10	I	80	VDDIO	P	112	RD0	IO2
17	SD2	IO24	49	SA11	I	81	RSTDRV	SI	113	VSSIO	G
18	SD3	IO24	50	$\overline{\text{SMEMR}}$	I	82	$\overline{\text{BDCS}}$	O4	114	RA15	O4
19	VSSIO	G	51	$\overline{\text{SMEMW}}$	I	83	$\overline{\text{LEDL}}$	OD16	115	RA14	O4
20	SD4	IO24	52	SA14	I	84	$\overline{\text{LEDT}}$	OD16	116	RA13	O4
21	SD5	IO24	53	SA15	I	85	$\overline{\text{LEDR}}$	OD16	117	RA12	O4
22	SD6	IO24	54	SA16	I	86	$\overline{\text{LEDC}}$	OD16	118	RA11	O4
23	SD7	IO24	55	SA17	I	87	OSCO	O	119	RA10	O4
24	VDDIO	P	56	SA18	I	88	OSCI	CI	120	RA9	O4
25	VSSIO	G	57	SA19	I	89	VDDC	P	121	RA8	O4
26	$\overline{\text{IOCS16}}$	OD24	58	$\overline{\text{IOR}}$	I	90	EECS	O4	122	VSSIO	G
27	IOCHRDY	OD24	59	$\overline{\text{IOW}}$	I	91	$\overline{\text{RWE}}$	O4	123	RA7	O4
28	$\overline{\text{IRQ15}}$	OT24	60	$\overline{\text{SBHE}}$	I	92	$\overline{\text{ROE}}$	IO4	124	RA6	O4
29	$\overline{\text{IRQ12}}$	OT24	61	AEN	I	93	$\overline{\text{RCS1}}$	O4	125	RA5	O4
30	$\overline{\text{IRQ11}}$	OT24	62	VSST	G	94	$\overline{\text{RCS0}}$	O4	126	RA4	O4
31	$\overline{\text{IRQ10}}$	OT24	63	TPDN	AO	95	VDDIO	P	127	RA3	O4
32	$\overline{\text{IRQ9}}$	OT24	64	TPDP	AO	96	RD15	IO2	128	RA2	O4

(See legend for pin description on following page)

LEGEND

TYPE	Description	TYPE	Description	TYPE	Description
I	Input (TTL level)	O4	Output with IOL = 4 mA	P, G	Power, Ground
CI	CMOS level Input	OD16, OD24	Output Open Drain with IOL = 16 or 24 mA	R	Resistor to analog ground (20K ± 1%)
SI	Schmitt trigger Input	OT24	Output Tristate with IOL = 24 mA	IO2, IO24	Input (TTL level) & Output with IOL = 2 or 24 mA
AI	Analog Input	AO	Analog Output		

Pin Assignment Table (NEC PC-98 bus)

PIN#	PIN NAME	TYPE	PIN#	PIN NAME	TYPE	PIN#	PIN NAME	TYPE	PIN#	PIN NAME	TYPE
1	RA1	04	33	IR5	OT24	65	TPON	AO	97	RD14	IO2
2	RA0	04	34	IR6	OT24	66	TPOP	AO	98	RD13	IO2
3	VSSIO	G	35	IR3	OT24	67	VDDT	P	99	RD12	IO2
4	VDDIO	P	36	VSSC	G	68	DON	AO	100	RD11	IO2
5	DB15	IO24	37	AB0	I	69	DOP	AO	101	RD10	IO2
6	DB14	IO24	38	AB1	I	70	VSSA	G	102	RD9	IO2
7	DB13	IO24	39	AB2	I	71	RBIAS	R	103	RD8	IO2
8	DB12	IO24	40	AB3	I	72	VDDA	P	104	VSSIO	G
9	VSSIO	G	41	AB4	I	73	TPIN	AI	105	RD7	IO2
10	DB11	IO24	42	AB5	I	74	TPIP	AI	106	RD6	IO2
11	DB10	IO24	43	AB6	I	75	CIN	AI	107	RD5	IO2
12	DB9	IO24	44	AB7	I	76	CIP	AI	108	RD4	IO2
13	DB8	IO24	45	AB8	I	77	DIN	AI	109	RD3	IO2
14	VSSIO	G	46	AB9	I	78	DIP	AI	110	RD2	IO2
15	DB0	IO24	47	VDDC	P	79	VSSC	G	111	RD1	IO2
16	DB1	IO24	48	AB10	I	80	ISA	I	112	RD0	IO2
17	DB2	IO24	49	AB11	I	81	$\overline{\text{RESET}}$	SI	113	VSSIO	G
18	DB3	IO24	50	AB12	I	82	NC	O4	114	RA15	O4
19	VSSIO	G	51	AB13	I	83	$\overline{\text{LEDL}}$	OD16	115	RA14	O4
20	DB4	IO24	52	AB14	I	84	$\overline{\text{LEDT}}$	OD16	116	RA13	O4
21	DB5	IO24	53	AB15	I	85	$\overline{\text{LEDR}}$	OD16	117	RA12	O4
22	DB6	IO24	54	AB16	I	86	$\overline{\text{LEDC}}$	OD16	118	RA11	O4
23	DB7	IO24	55	AB17	I	87	OSCO	O	119	RA10	O4
24	VDDIO	P	56	AB18	I	88	OSCI	CI	120	RA9	O4
25	VSSIO	G	57	AB19	I	89	VDDC	P	121	RA8	O4
26	NC	OD24	58	$\overline{\text{IOR}}$	I	90	EECS	O4	122	VSSIO	G
27	IORDY	OD24	59	$\overline{\text{IOW}}$	I	91	$\overline{\text{RWE}}$	O4	123	RA7	O4
28	IR13	OT24	60	$\overline{\text{BHE}}$	I	92	$\overline{\text{ROE}}$	IO4	124	RA6	O4
29	IR12	OT24	61	$\overline{\text{CPUENB}}$	I	93	$\overline{\text{RCS1}}$	O4	125	RA5	O4
30	IR11	OT24	62	VSST	G	94	$\overline{\text{RCS0}}$	O4	126	RA4	O4
31	IR10	OT24	63	TPDN	AO	95	VDDIO	P	127	RA3	O4
32	IR9	OT24	64	TPDP	AO	96	RD15	IO2	128	RA2	O4

(See legend for pin description on following page)

LEGEND

TYPE	Description	TYPE	Description	TYPE	Description
I	Input (TTL level)	O4	Output with IOL = 4 mA	P, G	Power, Ground
CI	CMOS level Input	OD16, OD24	Output Open Drain with IOL = 16 or 24 mA	R	Resistor to analog ground (20K ± 1%)
SI	Schmitt trigger Input	OT24	Output Tristate with IOL = 24 mA	IO2, IO24	Input (TTL level) & Output with IOL = 2 or 24 mA
AI	Analog Input	AO	Analog Output		

PIN DESCRIPTION

Note abbreviations: C = Component, AI = Analog Input, DI = Digital Input, AO = Analog Output, DO = Digital Output, DIO = Digital I/O

BUS INTERFACE

<table>
<tr><th>NAME</th><th>TYPE</th><th>DESCRIPTION</th></tr>
<tr><td>ISA</td><td></td><td>ISA/NEC PC-98 bus select. Connect to VDD for ISA bus and connect to VSS for NEC PC-98</td></tr>
<tr><td>SD[15:0]</td><td>DIO</td><td>System Data Bus. A bi-directional, tri-state bus with 24 mA drive capable of connecting directly to the ISA/NEC PC-98 data bus.</td></tr>
<tr><td>SA[19:14];</td><td>DI</td><td>System Address Bus. All I/O access uses 12-bit address decoding. In NEC PC-98 bus mode, all I/O access uses 16-bit address decoding. SA[12] and SA[13] are taken from $\overline{SMEMR}$ and $\overline{SMEMW}$ respectively. SA[3:0] selects the set of 78Q8377A internal registers. SA[19:14] are needed for Boot Device.</td></tr>
<tr><td>AEN</td><td>DI</td><td>Address Enable. When active (high), it indicates a DMA transfer. It is low during I/O and memory cycle and is used to qualify address decoding.</td></tr>
<tr><td>RSTDRV</td><td>DI</td><td>Reset Drive. This pin resets the 78Q8377A internal pointers and registers to their appropriate state. It also puts the 78Q8377A in an unconfigured state. This pin has to remain active for at least 200 ns.</td></tr>
<tr><td>$\overline{SBHE}$</td><td>DI</td><td>System Byte High Enable. When active (low), it indicates a transfer of data on upper byte of the system data bus SD[15:8]. This signal is only applicable when the 78Q8377A is in word mode (when HBYTE bit in DLCR6<5> is set to 0). The complete truth table of the byte/ word and lower/ upper bus transfer is given here.
<table>
<tr><th>HBYTE</th><th>$\overline{SBHE}$</th><th>SA0</th><th>Function</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>Word transfer</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>Byte transfer on SD[15:8]</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>Byte transfer on SD[7:0]</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>Reserved</td></tr>
<tr><td>1</td><td>X</td><td>X</td><td>Byte transfer (SD[7:0])</td></tr>
</table>
The PnP register access is always through the lower data bus independent of HBYTE setting. NEC PC-98 bus mode is defined for 16-bit bus operation only. For those PnP registers located at odd addresses the register access will always utilize the higher data bits.</td></tr>
<tr><td>IOCHRDY</td><td>DO</td><td>I/O Channel Ready. Open-drain signal with 24 mA drive. For normal register access this signal is always inactive (tristate). For accesses to the data port (BMR8), this signal may be pulled low by the chip to delay the completion of the current read or write operation. It will also be used if the device is unable to respond to read or write requests within 2.4 µs. In these situations, the 78Q8377A will also assert interrupt and the host read error status bit (DLCR1<6>) or host write error status bit (DLCR0<0>).</td></tr>
</table>

PIN DESCRIPTION (continued)

Note abbreviations: C = Component, AI = Analog Input, DI = Digital Input, AO = Analog Output, DO = Digital Output, DIO = Digital I/O

BUS INTERFACE

NAME	TYPE	DESCRIPTION
$\overline{\text{IOCS16}}$	DO	I/O Chip Select 16-bit. Active low, open-drain signal with 24 mA drive. When pulled low, it informs the host that 78Q8377A device is capable of 16 bit access. Therefore, this signal can only be activated if HBYTE (DLCR6<5>) is set to zero. The 78Q8377A follows the IEEE P996 specification that recommends this function be implemented as a pure decode of SA[9:0] and AEN, with no dependency on $\overline{\text{IOR}}$ or $\overline{\text{IOW}}$. Since the Plug and Play register is defined for 8-bit access only, the signal $\overline{\text{IOCS16}}$ will not go low for Plug and Play register access independent of the HBYTE setting. This signal is not used in NEC PC-98 bus mode.
$\overline{\text{IOR}}$	DI	I/O Read. Active low read strobe.
$\overline{\text{IOW}}$	DI	I/O Write. Active low write strobe.
$\overline{\text{SMEMR}}$	DI	System Memory Read. Active low memory read cycle strobe. It is active for memory read within the low 1 Mbyte of the memory space. This signal, together with the $\overline{\text{SMEMW}}$, is used to qualify for the Boot Device Chip Select ($\overline{\text{BDCS}}$).
$\overline{\text{SMEMW}}$	DI	System Memory Write. Active low memory write cycle strobe. It is active for memory write within the low 1 Mbyte of the memory space. This signal (when write protect is disabled), together with the $\overline{\text{SMEMR}}$, is used to qualify for the Boot Device Chip Select ($\overline{\text{BDCS}}$).
$\overline{\text{IRQ3}}$, $\overline{4}$, $\overline{5}$, $\overline{9}$, $\overline{10}$, $\overline{11}$, $\overline{12}$, $\overline{15}$	DO	Interrupt Request. Tri-state with 24 mA drive. The 78Q8377A supports both edge and level-sensitive interrupt. When edge mode interrupt is selected, the 78Q8377A generates interrupt by driving a low followed by a high and then tri-stating the interrupt line. When level-sensitive mode is selected, the 78Q8377A generates interrupt by pulling the IRQ line low. It continuously drives it low until the interrupt has been serviced; at which time the IRQ is returned to triisate. This tri-state implementation allows for shareable interrupt line with other cards in the system. In NEC PC-98 bus mode, $\overline{\text{IRQ4}}$ and $\overline{\text{IRQ15}}$ are interrupt lines 6 and 13 respectively. In ISA mode, $\overline{\text{IRQ4}}$ and $\overline{\text{IRQ15}}$ are interrupt lines 4 and 15 respectively.

PIN DESCRIPTION (continued)

Note abbreviations: C = Component, AI = Analog Input, DI = Digital Input, AO = Analog Output, DO = Digital Output, DIO = Digital I/O

BUS INTERFACE

NAME	TYPE	DESCRIPTION
$\overline{BDCS}$	DO	Boot Device Chip Select. Active low signal which indicates that the current memory access cycle is from or to the boot device. The boot device address bus connects directly to the ISA address bus and the data bus connects through a data buffer to the ISA data bus. The boot device $\overline{OE}$ and $\overline{WE}$ pins (eg. for flash memory) connect to the $\overline{SMEMR}$ and $\overline{SMEMW}$ signals respectively. When the WP bit (BMR12<3>) is set, writing to the boot device is prevented. This signal is not used in NEC PC-98 bus mode.

BUFFER MEMORY INTERFACE

$\overline{RCS0}$, $\overline{RCS1}$	DO	RAM Chip Select. $\overline{RCS0}$ and $\overline{RCS1}$ are active low chip select lines for the SRAM with $\overline{RCS0}$ as the least significant byte.
$\overline{ROE}$	DO	RAM Output Enable. Active low. This is the output enable asserted by the 78Q8377A during buffer memory read cycles for the SRAM.
$\overline{RWE}$	DO	RAM Write Enable. Active low. This is the write enable asserted by the 78Q8377A during buffer memory write cycles for the SRAM.
RD[0:15]	DI/O	RAM Data Bus. This is the data bus between the 78Q8377A and the buffer memory. It can be configured for byte or word transfer depending on register bit RBYTE (DLCR6 <4>) RAM BYTE. For word transfers, the ordering of the most and least significant byte is defined by the register bit, INTLMOT (DLCR7 <0>). In PCMCIA bus mode, this data bus is only 8 bits wide (RD[0:7]).
RA[0:15]	DO	RAM Address Bus. Addresses up to 64 KByte of SRAM buffer memory.

NETWORK ATTACHMENT UNIT INTERFACE

DON, DOP	AO	Transmit Data Negative and Positive. Differential outputs to external transceiver for transmission.
DIN, DIP	AI	Receive Data Negative and Positive. Manchester differential inputs from external transceiver for reception.
CIN, CIP	AI	Collision Detect Negative and Positive. When an externally connected transceiver detects a collision on the medium, these differential inputs are driven by a 10 MHz signal.
RBIAS	C	Biasing Resistor. External biasing resistor. Connect to 20 kΩ ±1% to VSSA (Analog ground).

PIN DESCRIPTION (continued)

NETWORK TWISTED-PAIR MEDIUM INTERFACE

NAME	TYPE	DESCRIPTION
TPON, TPOP	AO	Twisted-Pair Output Negative and Positive. Driver outputs to twisted-pair medium. Must be summed together with TPDN and TPDP by external resistors in a pre-equalization network to produce twisted-pair transmit signal.
TPDN, TPDP	AO	Twisted-Pair Delayed Negative and Positive. Delayed (50 ns) driver outputs to twisted-pair medium. Must be summed together with TPON and TPOP by external resistors in a pre-equalization network to produce twisted-pair transmit signal.
TPIN, TPIP	AI	Twisted-Pair Input Negative and Positive. Inputs from twisted-pair medium.

CRYSTAL OSCILLATOR

OSCI	DI	Oscillator In. Connection for one side of the 20 MHz crystal or an input for an external 20 MHz clock source.
OSCO	DO	Oscillator Out. Connection for other side of the 20 MHz crystal. Left unconnected if an external clock is used.

EEPROM PINS

EECS	DO	EEPROM Chip select.
EESK	DO	EEPROM Serial clock. Shared with $\overline{\text{RCS1}}$.
EEDI	DO	EEPROM Data input. Shared with $\overline{\text{RCS0}}$.
EEDO	DI	EEPROM Data output. Shared with $\overline{\text{ROE}}$.

LED PINS

$\overline{\text{LEDL}}$	DO	LED Link. Active low, open drain with 16 mA drive.
$\overline{\text{LEDT}}$	DO	LED Transmit. Active low, open drain with 16 mA drive.
$\overline{\text{LEDR}}$	DO	LED Receive. Active low, open drain with 16 mA drive.
$\overline{\text{LEDC}}$	DO	LED Collision. Active low, open drain with 16 mA drive. When Full Duplex mode is selected, this pin is always low.

POWER SUPPLY PINS

VDD		3 for I/O pads (VDDIO), 2 for digital core (VDDC); 1 for analog (VDDA); 1 for transmit drivers (VDDT).
VSS		8 for I/O pads (VSSIO), 2 for digital core (VSSC); 1 for analog (VSSA); 1 for transmit drivers (VSST).

REGISTER DESCRIPTION

PLUG AND PLAY REGISTERS

Only three 8-bit ports are used by the software to access the Plug and Play registers. The Plug and Play registers are accessed by first writing the address of the desired register to the ADDRESS port, followed by a read of data from the RD_DATA port or a write of data to the WR_DATA port.

PORT NAME	LOCATION	TYPE
ADDRESS	0x0279 (Printer status port)	Write-only
WR_DATA	0x0A79 (0x0279 + 0x0800)	Write-only
RD_DATA	Relocatable in range 0x0203 to 0x03FF	Read-only

PLUG AND PLAY REGISTER MAP

ADDRESS	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
0x00	RD_DATA_ADDR							
0x01	ISOLATION							
0x02	(0)	(0)	(0)	(0)	(0)	RST_CSN	RST_ST	RST_LD
0x03	WAKE[CSN]							
0x04	RESOURCE							
0x05	(0)	(0)	(0)	(0)	(0)	(0)	(0)	R_STAT
0x06	CSN							
0x07	LDN = 0							
0x08 - 0x2F	0							
0x30	0	0	0	0	0	0	0	ACTV
0x31	0	0	0	0	0	0	IORNG_EN	IORNG_V
0x32 - 0x3F	0							
0x40	0	0	0	0	1	1	0	BDA2
0x41	BDA1	BDA0	0	0	0	0	0	0
0x42	(0)	(0)	(0)	(0)	(0)	(0)	M16=0	UL=0
0x43	1	1	1	1	1	1	1	1
0x44	BDSZ1	BDSZ0	0	0	0	0	0	0
0x45 - 0x5F	0							
0x60	IOA15	IOA14	IOA13	IOA12	IOA11	IOA10	IOA9	IOA8
0x61	IOA7	IOA6	IOA5	IOA4	0	0	0	0
0x62 - 0x6F	0							

PLUG AND PLAY REGISTER MAP (continued)

ADDRESS	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
0x70	(0)	(0)	(0)	(0)	IRQ3	IRQ2	IRQ1	IRQ0
0x71	(0)	(0)	(0)	(0)	(0)	(0)	IRQ_LVL	IRQ_TYPE
0x72	(0)	(0)	(0)	(0)	0	0	0	0
0x73	(0)	(0)	(0)	(0)	(0)	(0)	0	0
0x74	(0)	(0)	(0)	(0)	(0)	1	0	0
0x75	(0)	(0)	(0)	(0)	(0)	1	0	0
0x76 - 0xA8	0							
0xA9 - 0xFF	0							

* Please refer to SSI 78Q8377A Technical Reference Guide for a more detailed description of register bits.

LEGEND:

TYPE	DESCRIPTION
R	Readable
W	Writable
0/1	Power up / reset default value

SERIAL EEPROM MAP

ADDRESS	HIGH BYTE	LOW BYTE	DESCRIPTION
0		Bit 0: PnP_ACT	PnP Activate Reg
1	PnP0x41	PnP0x40	Plug and Play
2		PnP0x44	Configuration
3	PnP0x61	PnP0x60	Register
4	PnP0x71	PnP0x70	
5 to 7			Reserved
8 to 1F	Eg: IEEE Address, BMR default setting, etc		Custom Configuration
20	Vendor EISA ID Byte 1	Vendor EISA ID Byte 0	
21	Vendor Assigned ID Byte 1	Vendor Assigned ID Byte 0	PnP
22	Serial Number Byte 1	Serial Number Byte 0	Serial
23	Serial Number Byte 3	Serial Number Byte 2	Identifier
24		Checksum	
25 onwards			PnP Resource Data

PNP ACTIVATE REGISTER

Only bit 0 (PnP_ACT) is defined in this register. This bit is provided to let the 78Q8377A work in a non-PnP environment by powering up active. It also allows the 78Q8377A to participate in the boot process in a non-PnP Bios system.

PNP CONFIGURATION REGISTER

The PnP configuration is also automatically read by the EEPROM logic and the values programmed into the appropriate PnP registers. This becomes the default configuration for the chip in the absence of PnP protocol. The configuration can only be changed through a "PnP protocol" utility.

CUSTOM CONFIGURATION

This space is allocated for custom configuration. The users may fill this space with defaults such as IEEE address, BMR register settings, etc. The software driver is responsible for reading this space and program the appropriate registers (the 78Q8377A EEPROM logic will not read this space).

PNP SERIAL IDENTIFIER

Once the Isolation state is entered, the EEPROM logic will start loading the PnP serial identifier. The PnP serial identifier is loaded one word at a time after the serial isolation protocol has issued 16 pair of reads.

PNP RESOURCE DATA

Entering the Config state initiates the loading of the PnP resource data. After one word has been accumulated from the EEPROM, the R_STAT (resource status) bit is set to one. It will be reset to zero again after two reads from the RESOURCE register and the process repeats. If the Config state is entered from the Sleep state without going through the Isolation state, the first read from the RESOURCE data will return the PnP Serial Identifier data.

REGISTER DESCRIPTION (continued)

APPENDIX

PLUG AND PLAY STATES
There are 4 PnP states defined in the Plug and Play Specification. They are:

- **Wait for Key** (W4K)
- **Sleep** (SLP)
- **Isolation** (ISO)
- **Config** (CFG)

Valid Commands and States

ADDRESS	REGISTER NAME	VALID ACCESS IN STATE		
		SLP	ISO	CFG
0x00	Read Data Address		*	* 1
0x01	Isolation		*	
0x02	Reset	*	*	*
0x03	Wake	*	*	*
0x04, 05	Resource			*
0x06	CSN		*	* 1
0x07	LDN			*
0x30	Activate			*
0x31	I/O Range Check			*
0x40-44, 0x60, 61, 0x70, 71	Memory, I/O, Interrupt		*	

Note 1: The PnP Spec V1.0a does not include the CFG state in this register access.

ELECTRICAL SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Operation beyond the maximum ratings may damage the device.

PARAMETER	RATING
Supply voltage, Vdd	-0.5 to 6.0V
Input voltage, Vin	-0.5 to Vdd + 0.5V
Output voltage, Vout	-0.5 to Vdd + 0.5V
Storage temperature, Tstg	-55 to 150°C
Lead temperature (max 10 sec soldering), Tl	250°C max

DC CHARACTERISTICS (Ta = 0 to 70°C, Vdd = 5V ±5%)

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNIT
Low level input voltage	V_{IL}	TTL inputs			0.8	V
		OSCI pin			1.6	V
		Schmitt inputs			1.1	V
High level input voltage	V_{IH}	TTL inputs	2.2			V
		OSCI pin	3.8			V
		Schmitt inputs	3.5			V
Pull down current (RESET pin)	Ipd		13		50	µA
Low level output voltage	V_{OL}	Rated I_{OL}	0		0.4	V
High level output voltage	V_{OH}	Rated I_{OH}	2.4		Vdd	V
Low level output current (with V_{OL} = 0.4V)	I_{OL}	Pin types O4, IO4	4			mA
		Pin type OD16	16			mA
		Pin type IO2	2			mA
		Pin type OD24, OT24, IO24	24			mA
High level output current (with V_{OH} = 2.4V)	I_{OH}	Pin types O4, IO4	-4			mA
		Pin type IO2	-2			mA
		Pin type OT24, IO24	-24			mA
Leakage current (input/output)	I_L		-10		10	µA
Supply current	Idd	Fully active(1)			40	mA
		Idle			30	mA
Power down supply current	Ipwrdn	Osc. on			10	mA
		Osc. off			100	µA

Note: (1) Fully active means 3 “simultaneous” operations: transmitting, receiving (through twisted-pair port) and either host write or read.

ELECTRICAL SPECIFICATIONS (continued)

AUI CHARACTERISTICS

(VDD = 5V ± 5%, Vss = 0V, Ta = 0°C to +70°C)

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
Low Output Voltage for DOP, DON Vaol	Rext = 20 kΩ R_L = 78Ω	Vdd-1.5		Vdd-0.75	V
High Output Voltage for DOP, DON Vaoh	Rext = 20 kΩ R_L = 78Ω	Vdd-0.55		Vdd	V
DOP, DON Output Current Iao	Rext = 20 kΩ	8		14	mA
DIP, DIN, CIP, CIN Open Circuit Input Voltage (bias) Valb		2.45		3.33	V
DIP, DIN, CIP, CIN Diff Squelch Threshold Vasq		-300		-120	mV
DOP, DON Diff Idle Output Vadi	R_L = 78Ω	-40		40	mV
DOP, DON Diff Peak Output Vadv	Rext = 20 kΩ R_L = 78Ω	620		1100	mV
DOP, DON Output Resistance Rao				75	Ω

TWISTED PAIR
(VDD = 5V ± 5%, Ta = 0°C to +70°C)

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
TPIP, TPIN Diff Input Resistance Rti		3			kΩ
TPIP, TPIN Open Circuit Input Voltage (bias) Vtib		2.45		3.33	V
TPIP, TPIN Diff Input Voltage Range Vtiv	VDD = 5V	-3.1		3.1	V
TPIP, TPIN Positive Squelched Threshold Vtps	Note 1	300		585	mV
TPIP, TPIN Negative Squelched Threshold Vtns	Note 1	-585		-300	mV
TPIP, TPIN Positive Unsquelched Threshold Vtpu	Note 2		180		mV
TPIP, TPIN Negative Unsquelched Threshold Vtnu	Note 2		-180		mV
TPIP, TPIN Positive Squelched Threshold Long Distance Mode Vltps	Note 1	120		300	mV
TPIP, TPIN Negative Squelched Threshold Long Distance Mode Vltns	Note 1	-300		-120	mV
TPIP, TPIN Positive Unsquelched Threshold Long Distance Mode Vltpu	Note 2		100		mV
TPIP, TPIN Negative Unsquelched Threshold Long Distance Mode Vltnu	Note 2		-100		mV
TPOP, TPON High Output Voltage Vtoh	I = 32 mA	Vddtp -0.44		Vddtp	V
TPOP, TPON Low Output Voltage Vtol	I = 32 mA	Vsstp		Vsstp +0.44	V
TPDP, TPDN High Voltage Vtdh	I = 16 mA	Vddtp -0.44		Vddtp	V
TPDP, TPDN Low Voltage Vtdl	I = 16 mA	Vsstp		Vsstp +0.44	V
TPDP, TPDN Output Resistance Rtd				27	Ω
TPOP, TPON Output Resistance Rto				13.5	Ω

Note 1: Sine wave at 2 MHz, 5 MHz and 7 MHz

Note 2: Sine wave : 5 MHz ≤ f ≤ 10 MHz

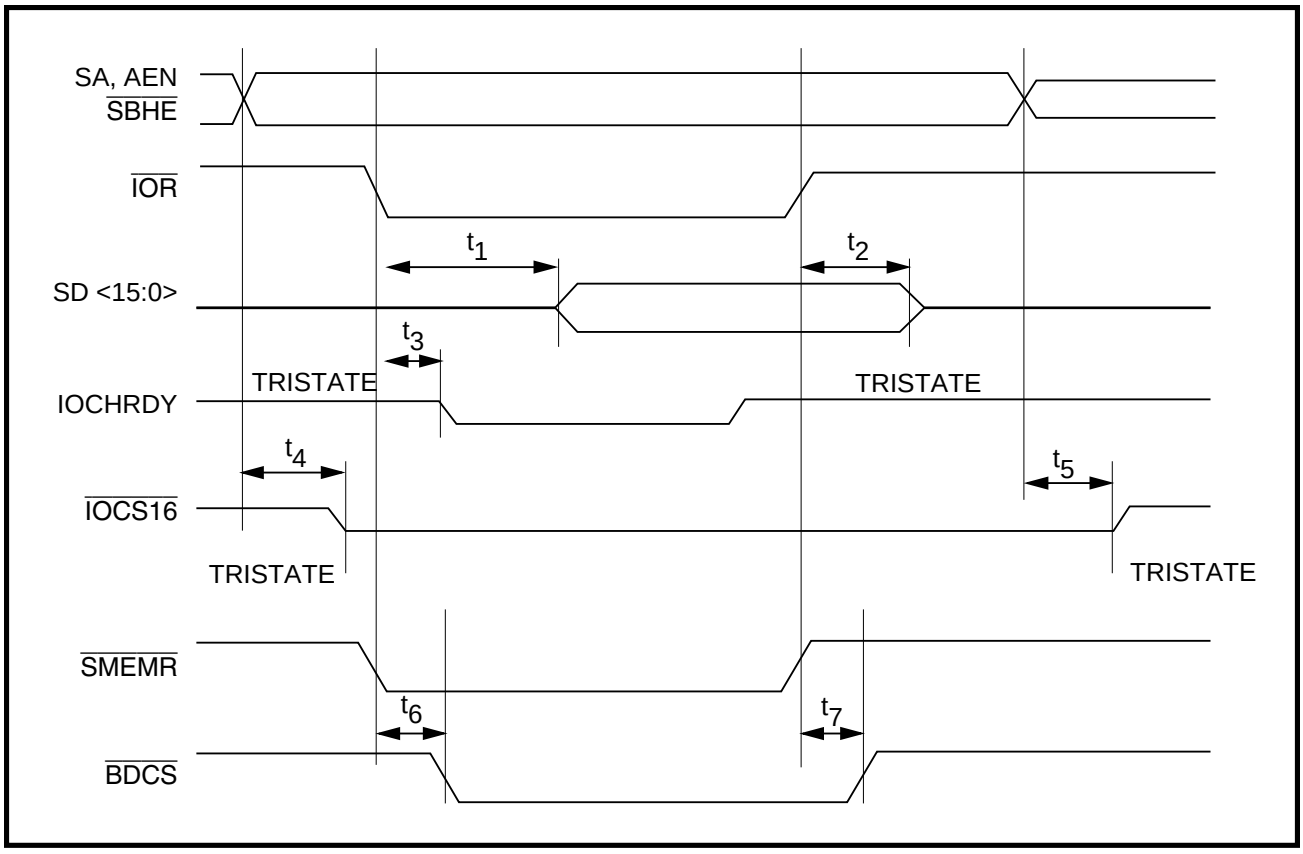


FIGURE 2: Read Cycle

ELECTRICAL SPECIFICATIONS (continued)

TABLE 1: Read Cycle

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNIT
IOR to SD<15:0> valid	t_1				45	ns
IOR to SD<15:0> tristate	t_2		8			ns
IOR to IOCHRDY not ready	t_3				18	ns
SA, AEN to SBHE to IOCS16 Tristate to low	t_4				18	ns
SA, AEN to IOCS16 low to Tristate	t_5				18	ns
SMEMR to BDCS active	t_6				25	ns
SMEMR to BDCS inactive	t_7				25	ns

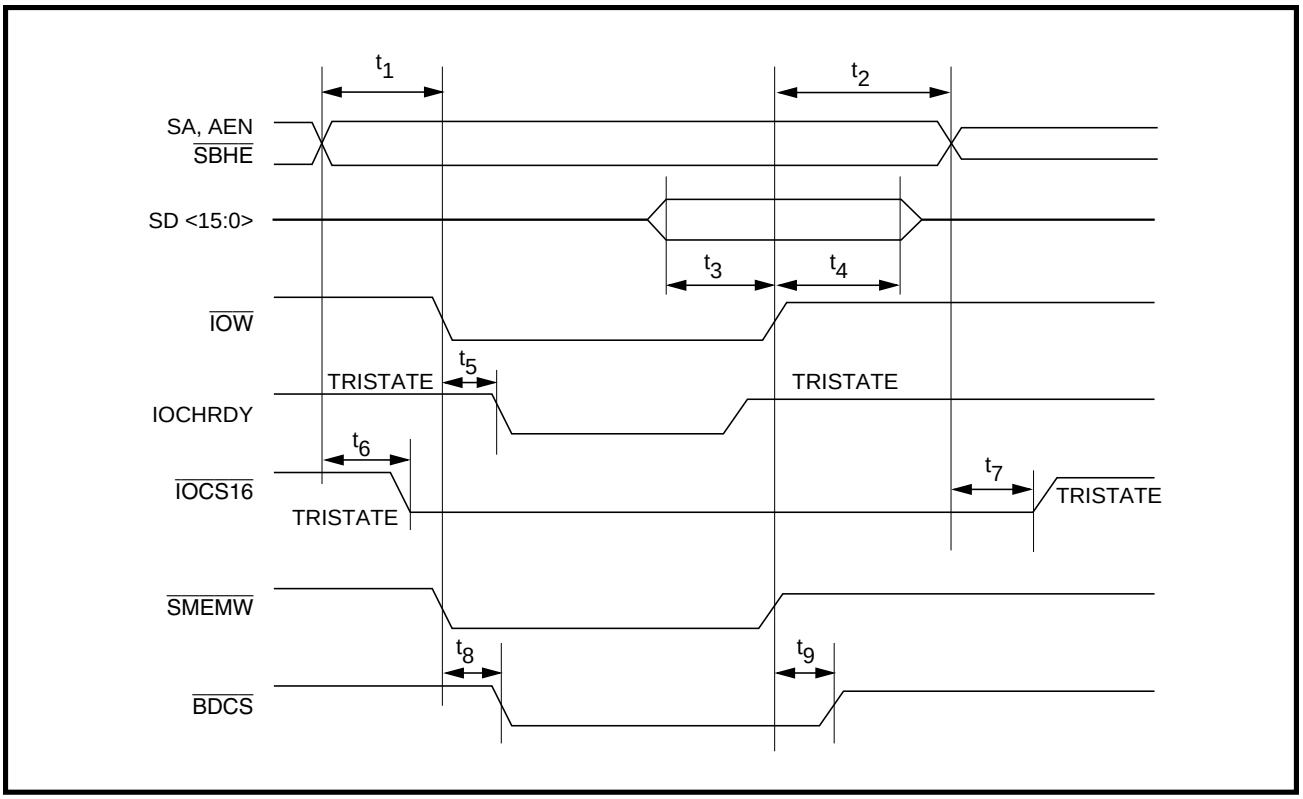


FIGURE 3: Write Cycle

TABLE 2: Write Cycle

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNIT
SA, $\overline{SBHE}$ and AEN setup time to $\overline{IOW}$ low	t_1		15			ns
Hold time of SA, $\overline{SBHE}$ and AEN after $\overline{IOW}$ high	t_2		8			ns
Setup time of SD to $\overline{IOW}$ high	t_3		25			ns
Hold time of SD to after $\overline{IOW}$ low	t_4		8			ns
$\overline{IOW}$ to IOCHRDY not ready	t_5					ns
SA, AEN, $\overline{SBHE}$ to $\overline{IOCS16}$ low to Tristate	t_6				18	ns
SA, AEN to $\overline{IOCS16}$ Tristate to low	t_7				18	ns
$\overline{SMEMW}$ to $\overline{BDCS}$ active	t_8				25	ns
$\overline{SMEMW}$ to $\overline{BDCS}$ inactive	t_9				25	ns

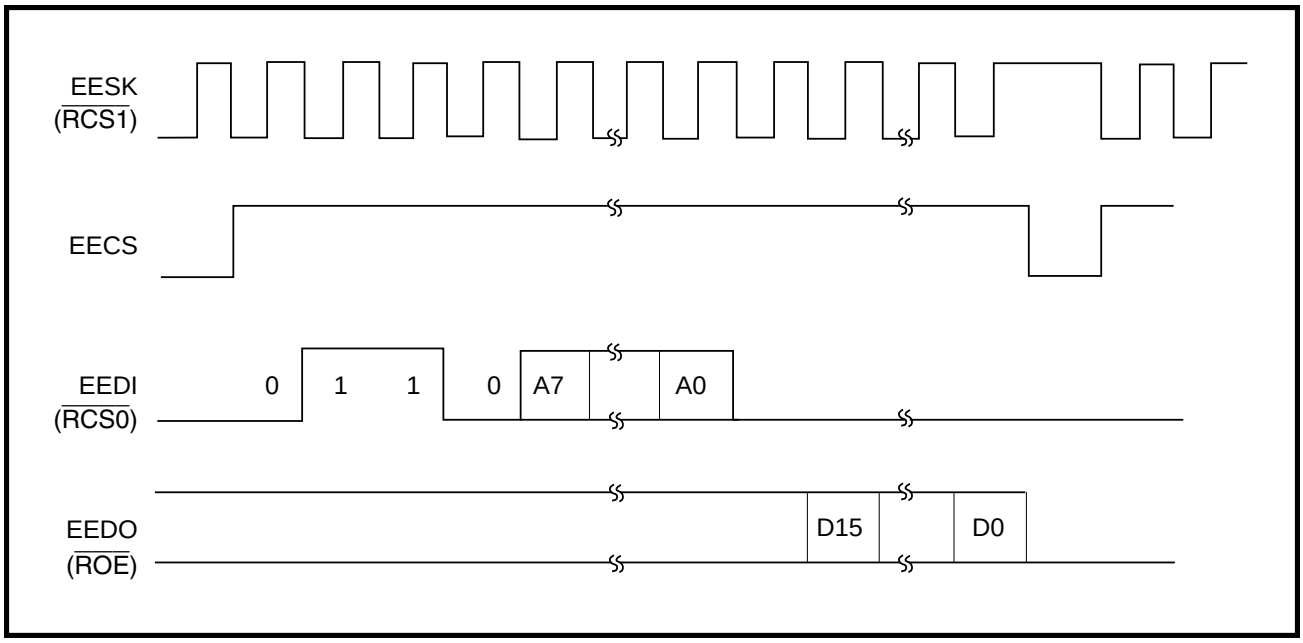


FIGURE 4: Serial Shift EEPROM Interface Read Timing

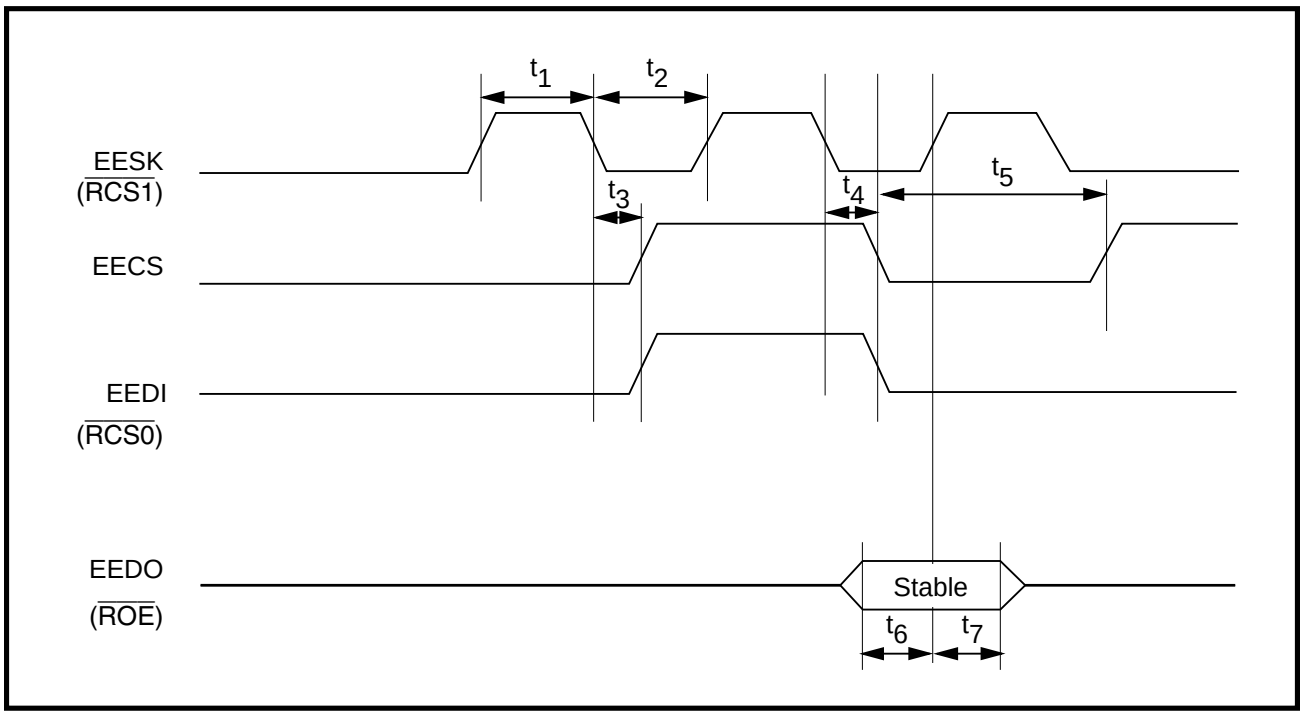


FIGURE 5: Serial EEPROM Control Timing

ELECTRICAL SPECIFICATIONS (continued)

TABLE 3: Serial EEPROM Control Timing

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNIT
EESK High Time	t_1		790	800		ns
EESK Low Time	t_2		790	800		ns
↑EECS, EEDI From ↓EESK	t_3		-15		15	ns
↓EECS, EEDI From ↓EESK	t_4		-15		15	ns
EECS Low Time	t_5		1590	1600		ns
EEDO Setup to ↑EESK	t_6		20			ns
EEDO Hold From ↑EESK	t_7		0			ns

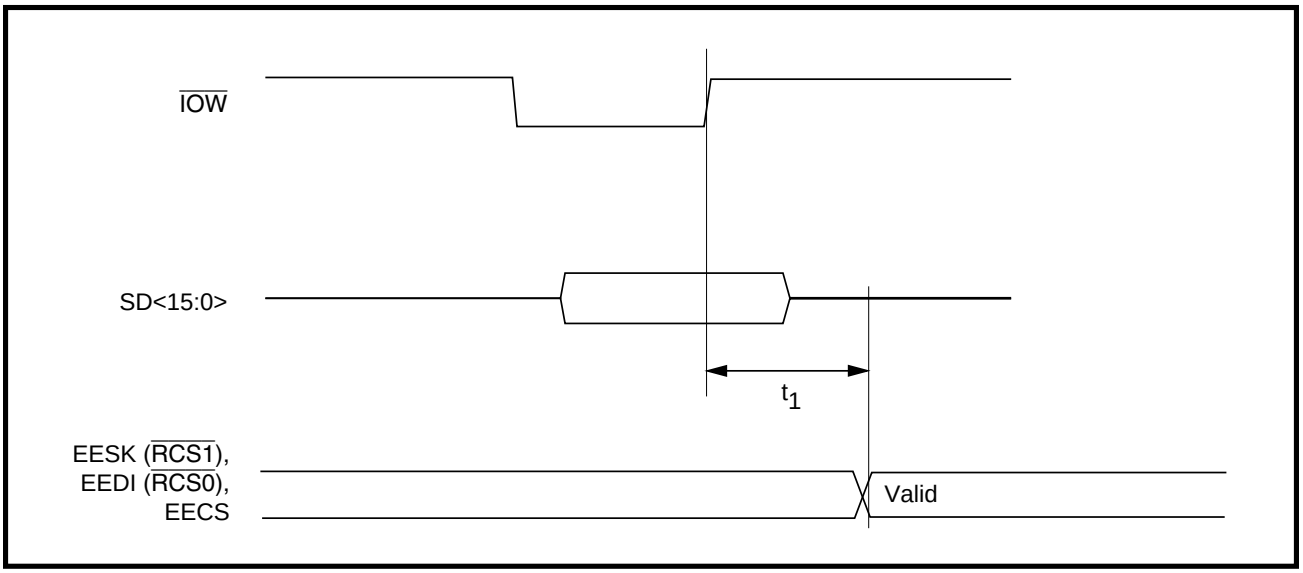


FIGURE 6: EEPROM Write Timing

TABLE 4: EEPROM Write Timing

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNIT
IOW to EESK (RCS1), EEDI (RCS0), EECS valid	t_1				30	ns

Note: The SD signal is for reference only.

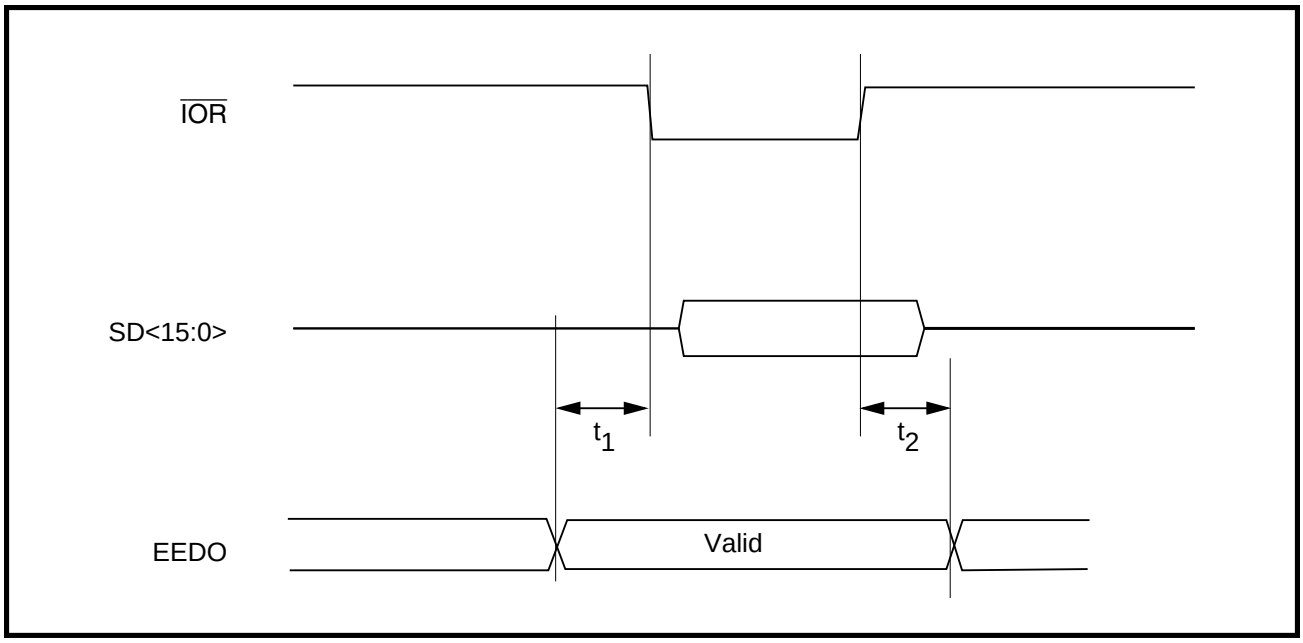


FIGURE 7: EEPROM Read Timing

ELECTRICAL SPECIFICATIONS (continued)

TABLE 5: EEPROM Read Timing

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNIT
EEDO valid to $\overline{IOR}$	t_1		0			ns
$\overline{IOR}$ to EEDO invalid	t_2		0			ns

Note: The SD signal is for reference only.

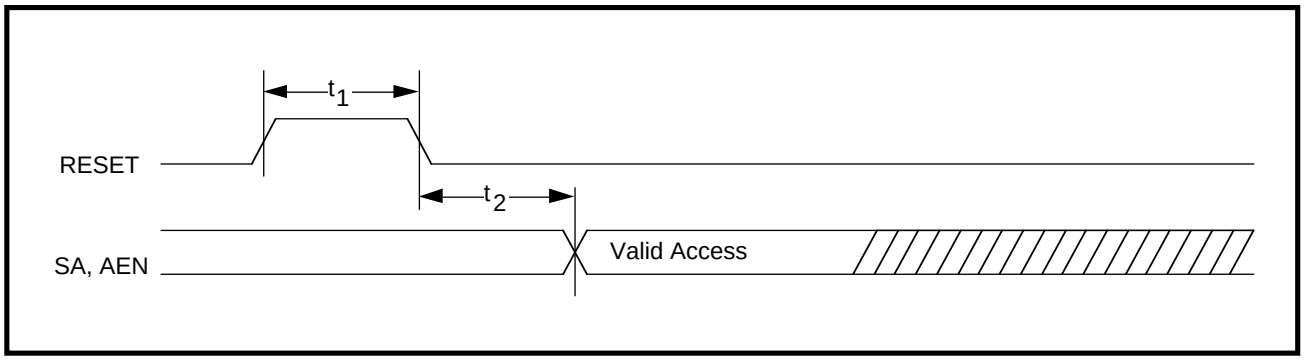


FIGURE 8: RESET Timing

TABLE 6: RESET Timing

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNIT
RESET pulse width	t_1		500			ns
RESET low to first valid access	t_2		800			ns

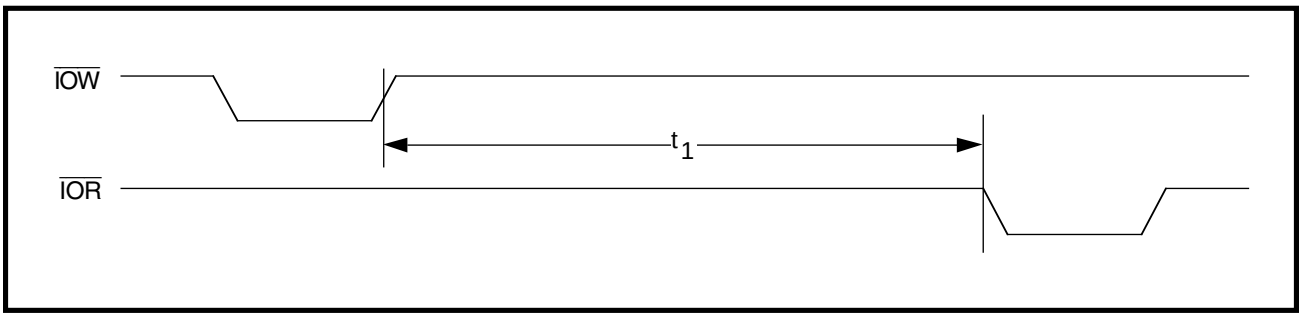


FIGURE 9: Skip Packet Timing

TABLE 7: Skip Packet Timing

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNIT
Writing Skip Packet high to next Buffer Memory Port read	t_1		200			ns

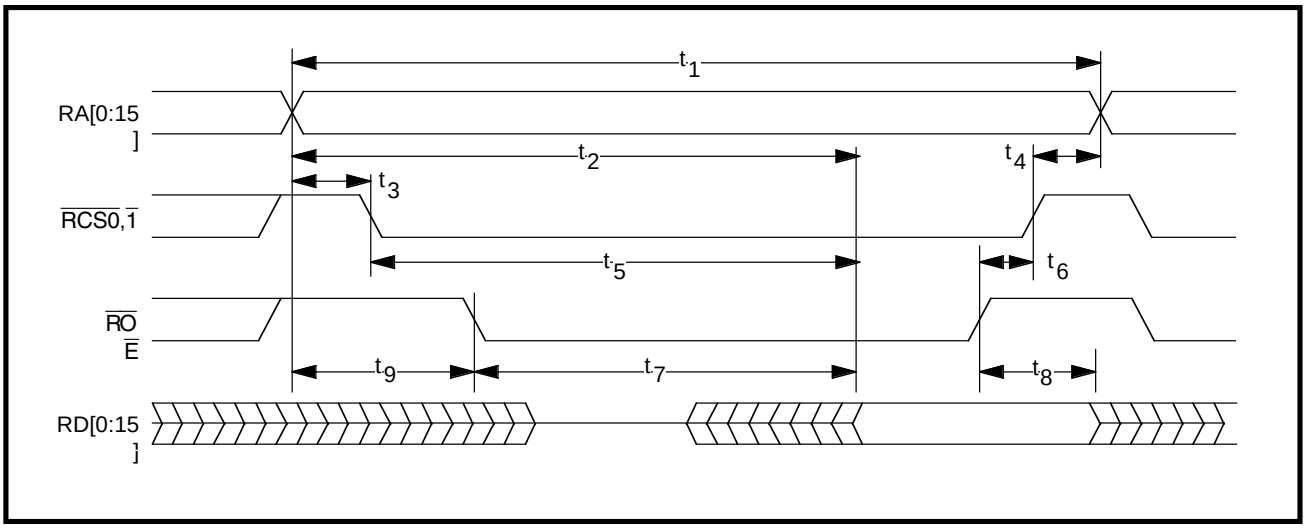


FIGURE 10: SRAM Read Timing

ELECTRICAL SPECIFICATIONS (continued)

TABLE 8: SRAM Read Timing

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNIT
Read cycle	t_1	RAMSP = 1	95			ns
		RAMSP = 0	145			ns
Address access time	t_2	RAMSP = 1			75	ns
		RAMSP = 0			125	ns
Address valid to $\overline{RCS0,1}$ low	t_3				8	ns
$\overline{RCS0,1}$ high to address invalid	t_4		0			ns
Chip select access time	t_5	RAMSP = 1			75	ns
		RAMSP = 0			125	ns
$\overline{ROE}$ high to $\overline{RCS0,1}$ high	t_6		0		8	ns
Output enable access time	t_7	RAMSP = 1			50	ns
		RAMSP = 0			100	ns
Data hold time	t_8		0			ns
Address valid to $\overline{ROE}$ low	t_9				30	ns

Note: Use SRAM with address access time of 75 ns or less for RAMSP = 1 and 125 ns or less for RAMSP = 0. RAMSP is DLCR6 <6>.

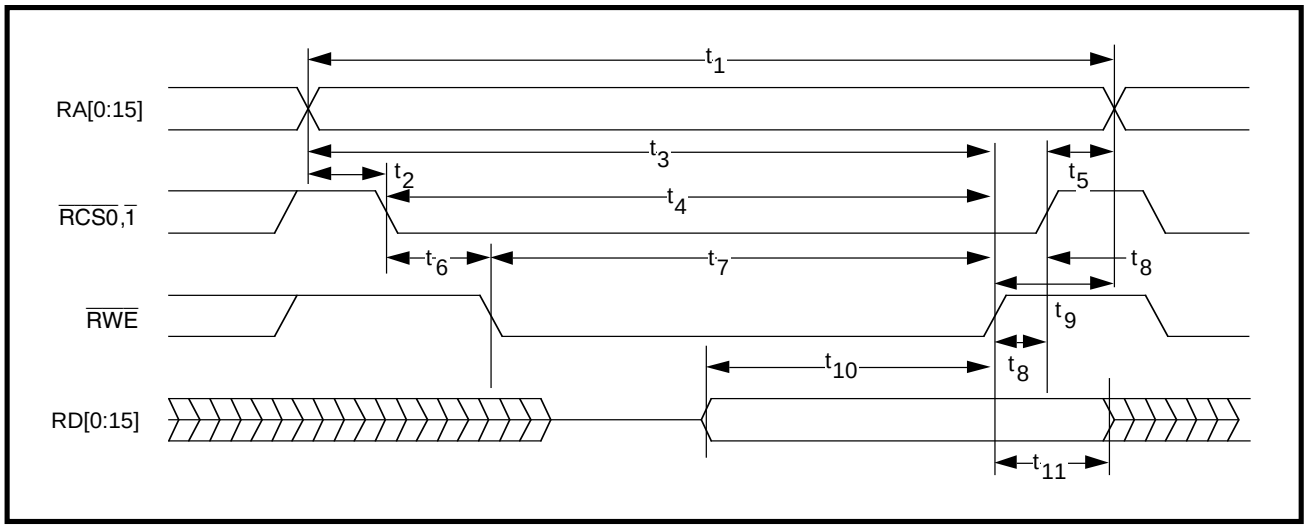


FIGURE 11: SRAM Write Timing

TABLE 9: SRAM Write Timing

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNIT
Write Cycle	t_1	RAMSP = 1	95			ns
		RAMSP= 0	145			ns
Address Valid to $\overline{RCS0,1}$ low	t_2				8	ns
Address Valid to $\overline{RWE}$ high	t_3	RAMSP = 1	70			ns
		RAMSP = 0	120			ns
$\overline{RCS0,1}$ low to $\overline{RWE}$ high	t_4	RAMSP = 1	70			ns
		RAMSP = 0	120			ns
$\overline{RCS0,1}$ high to Address Invalid	t_5		0			ns
$\overline{RCS0,1}$ low to $\overline{RWE}$ low	t_6		0			ns
$\overline{RWE}$ Pulse Width	t_7	RAMSP = 1	70			ns
		RAMSP = 0	120			ns
$\overline{RWE}$ high to $\overline{RCS0,1}$ high	t_8		0			ns
$\overline{RWE}$ high to Address Invalid	t_9		10			ns
Data Setup Time	t_{10}	RAMSP = 1	40			ns
		RAMSP = 0	90			ns
Data Hold Time	t_{11}		20			ns

Note: Use SRAM with address access time of 75 ns or less for RAMSP = 1 and 125 ns or less for RAMSP = 0. RAMSP is DLCR6 <6>.

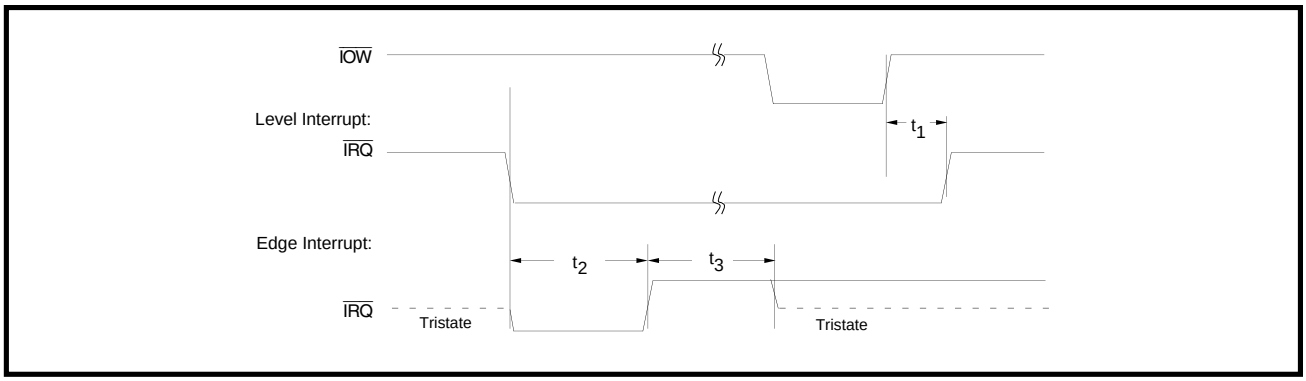


FIGURE 12: Interrupt Timing

ELECTRICAL SPECIFICATIONS (continued)

TABLE 10: Interrupt Timing

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNIT
$\overline{IRQ}$ signal clearing delay	t_1	level interrupt	7		40	ns
$\overline{IRQ}$ low pulse width	t_2	edge interrupt	150		200	ns
$\overline{IRQ}$ high driving time	t_3	edge interrupt	150		200	ns

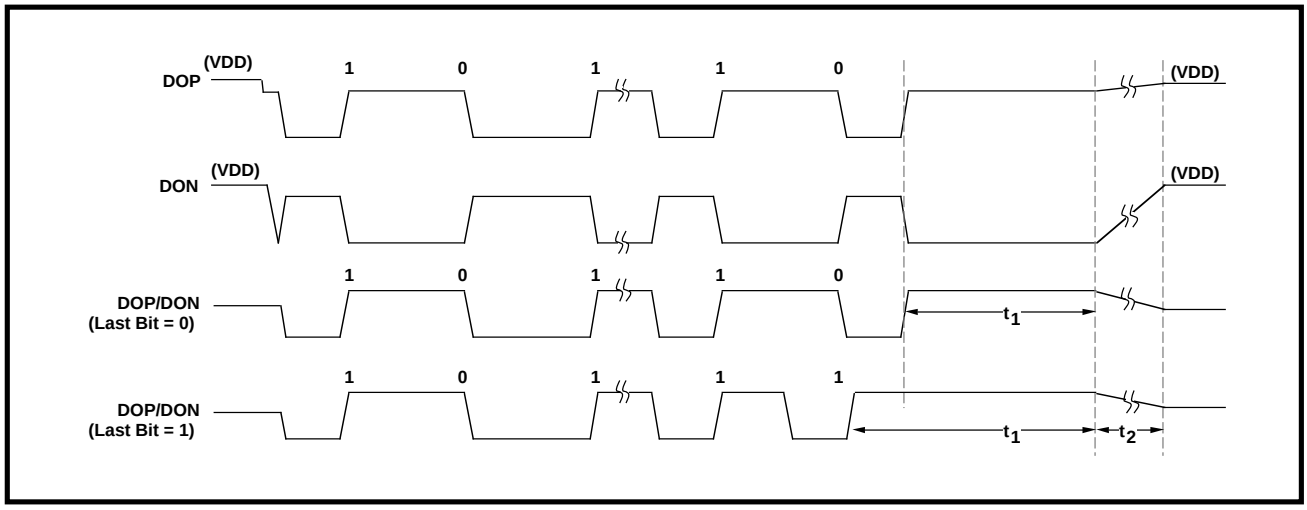


FIGURE 13: Transmit Timing (AUI)

TABLE 11: Transmit Timing (AUI)

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
DOP/DON end-of-packet delimiter t_1		200			ns
DOP/DON line voltage transition t_2				8	µs

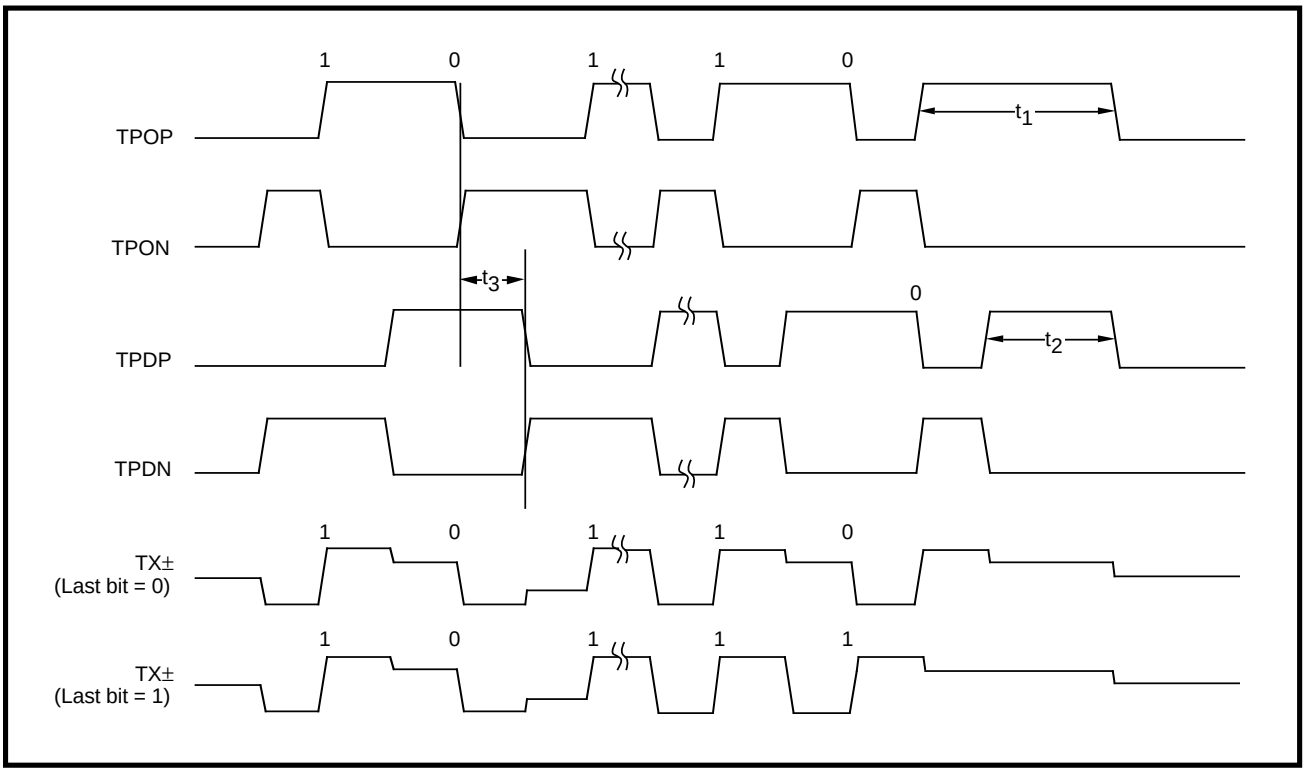


FIGURE 14: Transmit Timing (TP)

TABLE 12: Transmit Timing (TP)

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
TPOP/TPON end-of-packet delimiter t_1		250			ns
TPDP/TPDN end-of-packet delimiter t_2		200			ns
TPOP to TPDP and TPON to TPDN delay t_3			50		ns

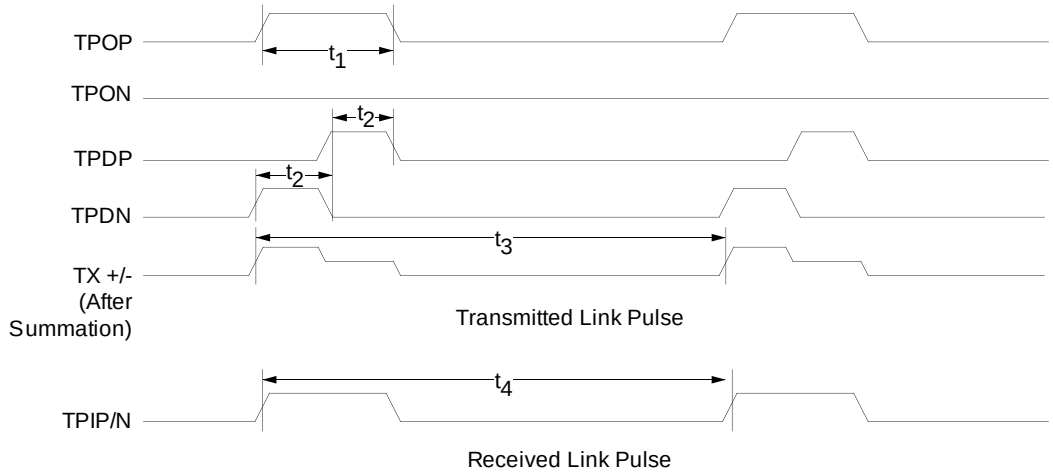


FIGURE 15: Link Test Timing

ELECTRICAL SPECIFICATIONS (continued)

TABLE 13: Link Test Timing

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNIT
TPOP link pulse width	t_1			150		ns
TPDP/TPDN link pulse width	t_2			100		ns
Duration between transmitted link pulses	t_3		9		11	ms
Duration between received link pulses	t_4		4.1		65	ms

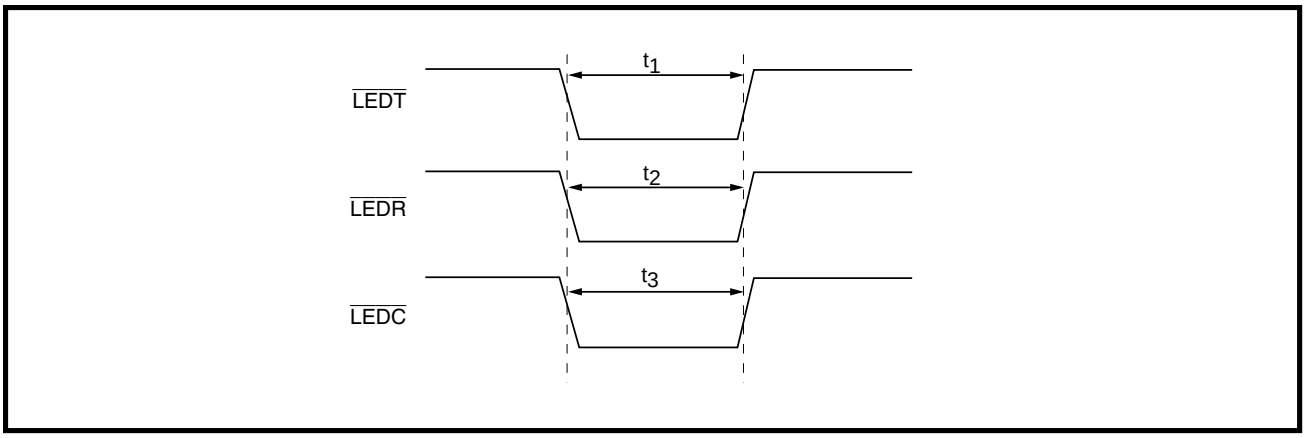


FIGURE 16: LED Timing

TABLE 14: LED Timing

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNIT
Transmit blink-on timing	t_1			100		ms
Receive blink-on timing	t_2			100		ms
Collision blink-on timing	t_3			100		ms

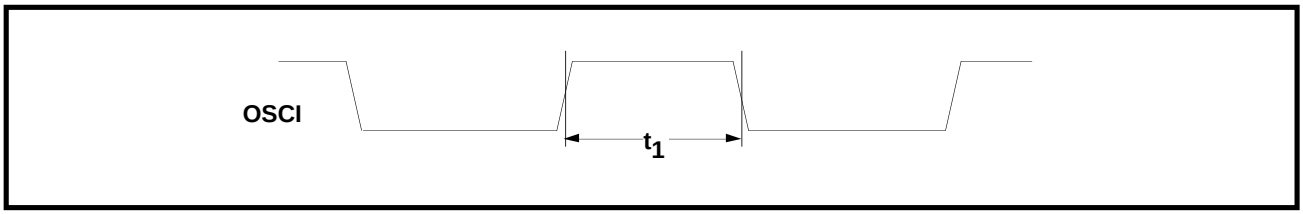


FIGURE 17: Oscillator Duty Cycle

TABLE 15: OSCI Duty Cycle

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNIT
Oscillator duty cycle	t_1		40	50	60	%

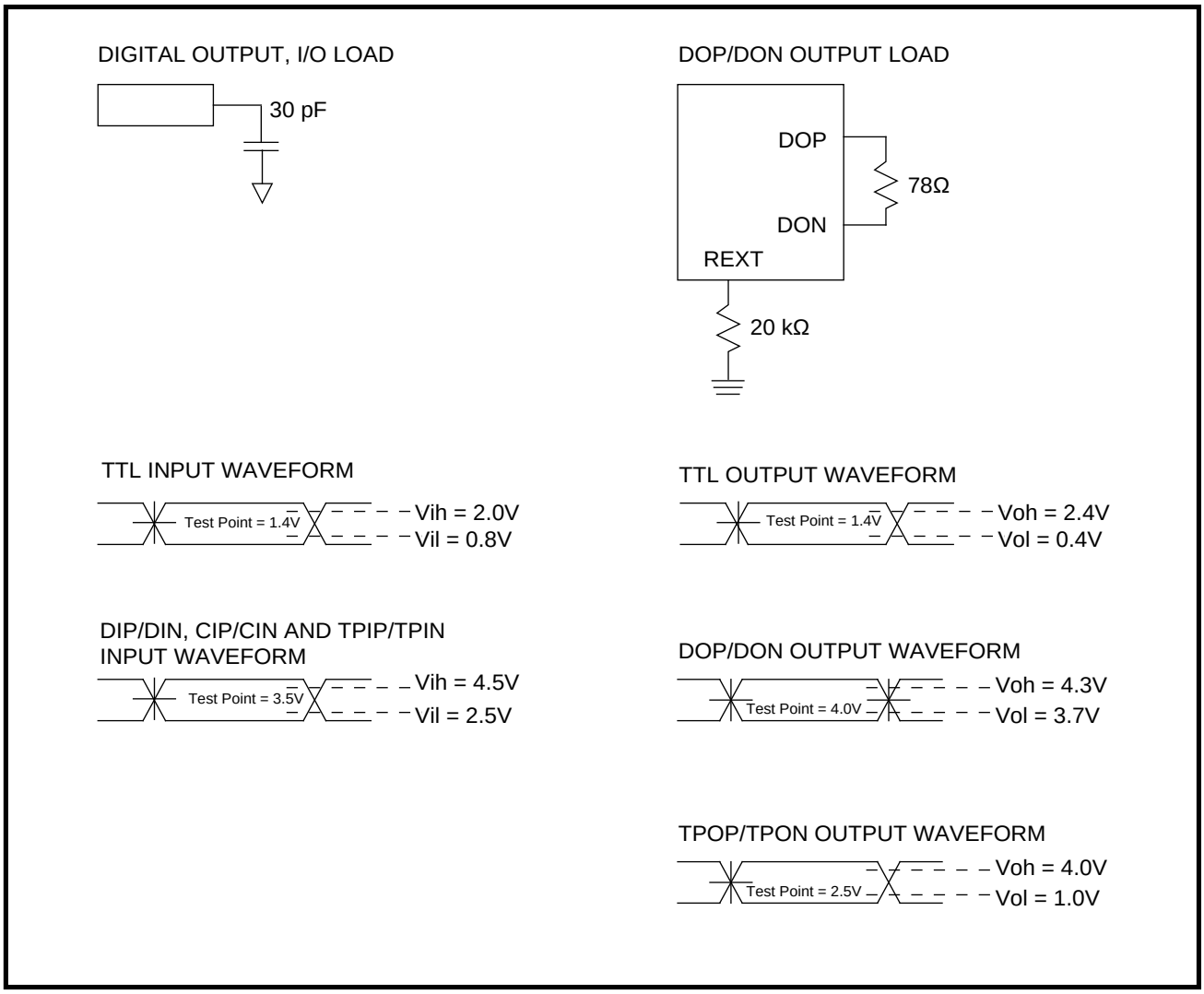
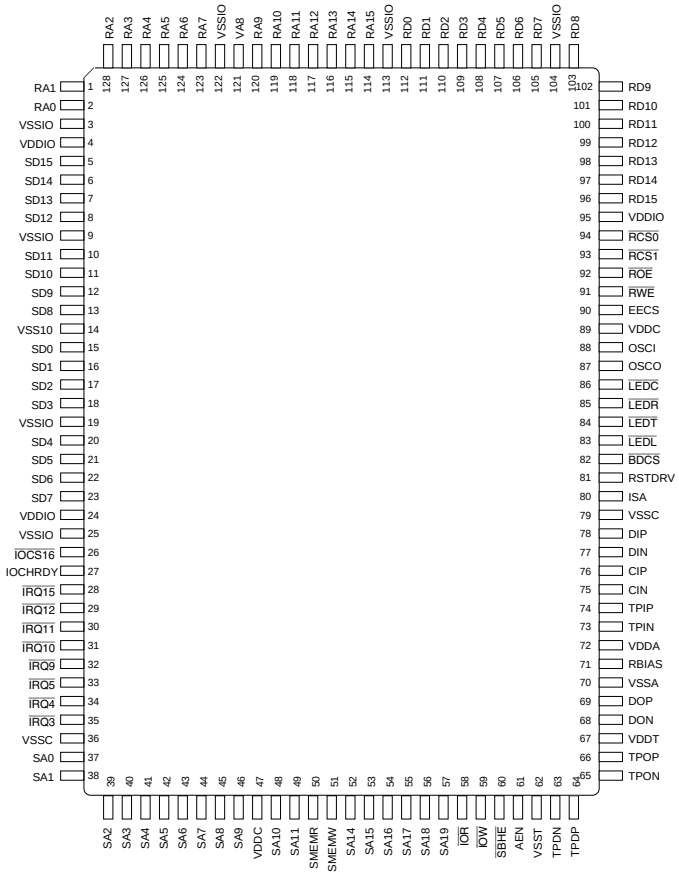


FIGURE 18: Test Conditions

PACKAGE PIN DESIGNATIONS

(Top View)



128-Lead QFP

CAUTION: Use handling procedures necessary for a static sensitive component.

ORDERING INFORMATION

PART DESCRIPTION		ORDER NUMBER	PACKAGE MARK
SSI 78Q8377A	10BaseT Ethernet Control for Plug and Play 128-Lead QFP	SSI 78Q8377A	SSI 78Q8377A

Preliminary Data: Indicates a product not completely released to production. The specifications are based on preliminary evaluations and are not guaranteed. Small quantities are available, and Silicon Systems should be consulted for current information.

Silicon Systems, Inc., 14351 Myford Road, Tustin, CA 92680-7022 (714) 573-6000, FAX (714) 573-6914

silicon systems®
A TDK Group Company

SSI 78Q8378
3V, 5V PC Card Multi-function Ethernet Combo
Preliminary Data

January 1996

DESCRIPTION

The SSi 78Q8378 is a highly integrated Ethernet and peripheral port combo IC for use in Multi-function PC Card applications and can operate with a power supply of 3.3V or 5V. It is compliant with PC Card Standard (Multiple Function) as well as backwards compatible to PCMCIA 2.X specifications. It contains a Media Access Controller (MAC), a 10 Mbit/s Manchester encoder/decoder (ENDEC), a 10BaseT transceiver, a multi-function memory card bus interface (PC Card), a peripheral port interface, and an Attachment Unit Interface (AUI). This level of integration allows the user to implement a multi-function PC Card for 10BaseT and Fax/Modem by using the SSI 78Q8378, a modem chip set, external memory, and some passive components. The internal bus interface circuit allows connection to a Multi-function PC Card V3.0 bus without other external components. The PC Card bus decoding logic can be bypassed for connection to other bus types. The SSI 78Q8378 connects to twisted-pair media via line transformers through the on-chip transceiver circuit. Connections to other media such as coaxial cable is made through the AUI port to an external transceiver, such as the SSi 78Q8392L Ethernet Coax Transceiver.

The SSI 78Q8378 has a sophisticated power management capability with three different operating modes allowing the user to maximize power savings, making it ideal for use in PC Card applications. During normal operation, the IC monitors its own action and shuts down the circuits that are not being used, resulting in the lowest possible operating power. It also has a standby mode which leaves only the oscillator running, and a full shutdown mode which also turns off the oscillator.

An intelligent Buffer Manager is controlled by the host read, host write, receive and transmit pointers, and the SSI 78Q8378 manages the pointers internally without any host intervention. The device interleaves access to the buffer memory so that access from the host and from the network media seem to operate concurrently. Big and little endian byte orderings make for simple bus interface to all standard microprocessors.

The SSI 78Q8378 is available in a 120-lead thin quad flat pack (TQFP) and can operate with a power supply of 3.3 volts or 5 volts.

FEATURES

- **Single-chip solution for 10Base T/PC Card designs with a second peripheral interface**
- **Operation at 3.3V or 5V**
- **Register compatible to the SSI 78Q8373**
- **Programmable full duplex operation**
- **Integrated 10BaseT transceiver:**
  - **Programmable/automatic selection of twisted pair (RJ45) or AUI port**
  - **Receive polarity detection/correction on twisted-pair inputs**
- **Manchester Encoder/Decoder circuit**
- **AUI port for connection to 10Base-2/5 transceiver or AUI cable**
- **PC Card Standard (multiple function spec) V3.0 compliant.**
- **Protocol Controller compliant with IEEE 802.3 and Ethernet 2.0**
  - **Supports packet indication and ring indication functions**
- **Advanced Buffer Manager architecture:**
  - **Automatic management of all pointers**
  - **Allows "simultaneous" access to data in buffer memory by both the network and host**
  - **High-speed received packet skip**
- **Configurable Buffer Memory for design flexibility:**
  - **Two-bank transmit buffer in 2, 4, 8 or 16 Kbyte sizes**
  - **Ring-structure receive buffer from 4 to 62 Kbytes**
- **Software-configurable system bus structure:**
  - **Compatible with major microprecessors**
  - **8 or 16-bit wide data path communications with hosts**
  - **Supports both dual interrupt and shared interrupt schemes.**
  - **Configurable I/O base address for LAN and peripheral port functions with 10-bit address decode**

FEATURES (continued)

- **External CIS memory support: Parallel EEPROM or Flash memory**
- **Power management options:**
  - **Intelligent power mode automatically shuts off unused circuitry**
  - **Standby mode reduces power while not in operation**
  - **Full shutdown mode offers maximum power savings**
- **Available in 120-lead TQFP package**

FUNCTIONAL DESCRIPTION

The 78Q8378 consists of six major blocks as shown in Figure 1.

- Buffer Manager (and SRAM Interface)
- Data Link Controller
- Host/PC Card Interface
- Manchester ENDEC
- Twisted Pair Transceiver
- Power Management

BUFFER MANAGER

The Buffer Manager manages all accesses to the buffer memory through the SRAM interface. The buffer memory is connected directly to the Data Link Controller (DLC), thus eliminating the need for a local microprocessor. The Buffer Manager also keeps track of all buffer memory pointers automatically, simplifying the software driver task. Together with intelligent arbitration, this makes the 78Q8378 a high performance LAN controller.

The buffer memory is divided into two portions: transmit memory portion and receive memory portion. The transmit memory portion can be partitioned into 2K, 4K, 8K or 16 Kbyte buffer sizes. There is only one transmit bank if a 2 KB transmit buffer size is selected. If the transmit buffer size is greater than 2 KB, then the transmit buffer is configured into two banks of equal size. With the two bank configuration, one transmit bank may be tied up during transmission but the host can still continue to load data packets into the second transmit bank to be transmitted later. The receive buffer has a ring architecture which can be configured from 4K to 62 KB depending on the buffer memory configuration which has a range of 8K to 64 KB.

A central arbitrator inside the Buffer Manager prioritizes and services requests for access to the buffer memory from 4 sources: the Transmitter, the Receiver, Host Read and Host Write. If necessary, the 78Q8378 will assert a ‘not ready’ handshake to the host while servicing the Transmitter and/or Receiver. The 78Q8378 arbitration mechanism provides packet management by interleaving packet data accesses to the buffer memory such that the operations appear to be simultaneous.

For instance, in the situation where 2 transmit banks are configured, the host can load the first transmit bank and initiate a transmission. While the first transmit bank is being transmitted, the host can continue to load packets in the second transmit bank. At this stage, the 78Q8378 can potentially be receiving data from the medium and loading it into the receive buffer (if the 78Q8378 is in a loop back mode, if self-reception occurs or if the 8378 is in full duplex mode).

DATA LINK CONTROLLER

The Data Link Controller (DLC) implements the ISO/ANSI/IEEE 802-3 CSMA/CD protocol. It consists of a Transmitter, a Receiver and CRC logic (which is shared by both transmit and receive operations). Automatic generation and stripping of the 64-bit preamble and the 32-bit CRC code are provided on-chip.

HOST/PC CARD INTERFACE

The Host Interface (HIF) provides connection to the host system. It consists of the various registers, DMA circuits and ready logic. Both word and byte interfaces are supported as well as big endian and little endian data ordering. Host access to the buffer memory is through BMR8 (and BMR9). Reading from BMR8 will read a byte or word from the receive buffer and writing to BMR8 will write a byte or word to the transmit buffer. The ready logic is capable of delaying host access to the buffer memory with a time-out mechanism. Both single and burst DMA transfer modes are supported.

PC CARD MULTI-FUNCTION INTERFACE

The PC Card interface has been extended to support multi-function card capability, in particular, LAN and Modem combination. The second peripheral port interface is a general purpose interface. Two additional features have been added to support modem functions. The ring indication function is available in the Status Change Register and a digital speaker signal is controlled through the 78Q8378. Two sets of Function Configuration Registers (FCR) (used to be called Card Configuration Registers - CCR on a single function card) are provided so that each function can be configured independently. The chip includes the function of mapping and decoding the I/O range for the LAN registers and the peripheral port. The 78Q8378 is also capable of handling multiple interrupts from two sources by saving the second interrupt and generating it later according to the PC card Multifunction specification.

It also supports decoding for the external CIS memory (both ROM and Flash types). The 78Q8378 pinout has been defined to minimize criss-crossing connections to the PC Card connector. This allows for a cost effective 2-layer PCB design.

FULL DUPLEX OPERATION

The 78Q8378 now includes support for Full Duplex operation (10 BaseT only), making the line throughput to 20 Mbit/s. In this mode, the collision detection, SQE generation and “natural” loopback of the TP transceiver are disabled.

MANCHESTER ENDEC

This block implements Manchester encoding and decoding. Serial NRZ data from the DLC is converted to Manchester encoded data and sent to either the twisted-pair transceiver block or to the Attachment Unit Interface (AUI) driver, depending on which block is

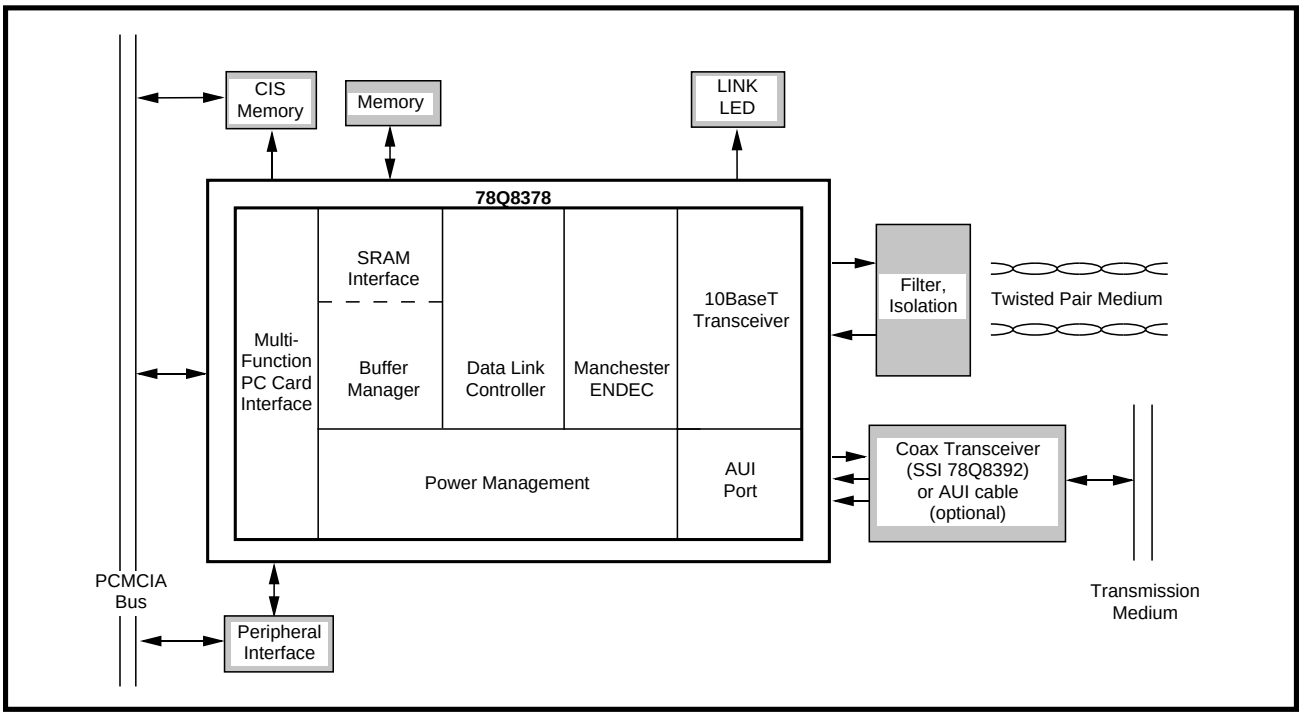


FIGURE 1: System Diagram

MANCHESTER ENDEC (continued)

active. The decoder section performs three functions: clock recovery, carrier detection and Manchester decoding. The recovered receive clock will be low at the end of reception and during idle to save power. Jitter of up to ±18 ns can be tolerated by the decoder. This block also translates a 10 MHz collision signal to a logic-level signal before sending it to the DLC block if the AUI port is selected.

TWISTED PAIR TRANSCEIVER

The on-chip Twisted Pair module consists of a number of functions. It has a smart squelch circuitry to determine valid data present on the differential receive inputs TPIP/TPIN. Its transmit and pre-distortion drivers connect to the twisted pair network via the summing resistors and transformer/filter. The link detector/ generator circuitry checks the integrity of the cable connecting the two twisted pair MAUs. Collision, jabber and SQE are also incorporated.

POWER MANAGEMENT

One very useful and important feature that the 78Q8378 offers is intelligent power management. It supports three different power saving modes: Intelligent, Standby, and Full Shutdown. All modes are configurable through registers. In the Intelligent mode, clocks are active only when they are needed. For example, when not transmitting, the clock supplied to the transmitter circuit in the DLC block is not active while host read from buffer memory may be active. In Standby mode, the oscillator clock is disconnected from the rest of the circuits, so that only the oscillator circuits draw power. Full Shutdown turns off the oscillator, resulting in maximum power savings. Note that this mode is not available when using an external clock source.

Pin Assignment Table - 120-Pin TQFP

PIN #	PIN NAME	TYPE	PIN#	PIN NAME	TYPE	PIN#	PIN NAME	TYPE	PIN#	PIN NAME	TYPE
1	A0	I	31	RD8	IO4	61	RA12	O4	91	DON	AO
2	A1	I	32	RD9	IO4	62	RA14	O4	92	DOP	AO
3	A2	I	33	RD10	IO4	63	$\overline{\text{RWE}}$	O4	93	VSSA	G
4	A3	I	34	RD11	IO4	64	RA13	O4	94	RBIAS	R
5	A4	I	35	RD12	IO4	65	RA8	O4	95	VDDA	P
6	A5	I	36	RD13	IO4	66	RA9	O4	96	TPIN	AI
7	A6	I	37	RD14	IO4	67	RA11	O4	97	TPIP	AI
8	A7	I	38	RD16	IO4	68	$\overline{\text{ROE}}$	O4	98	CIN	AI
9	VDDIO	P	39	VSSIO	G	69	RA15	O4	99	CIP	AI
10	A8	I	40	RD0	IO4	70	VSSIO	G	100	DIN	AI
11	A9	I	41	RD1	IO4	71	OSCI	CI	101	DIP	AI
12	FCRA	I	42	RD2	IO4	72	OSCO	O	102	VSSC	G
13	VSSC	G	43	RD3	IO4	73	VDDC	P	103	VDDC	P
14	$\overline{\text{WE}}$	I	44	RD4	IO4	74	$\overline{\text{MCS}}$	O4	104	LEDLT	OD16
15	$\overline{\text{IOWR}}$	I	46	RD5	IO4	75	$\overline{\text{MPD}}$	O4	105	$\overline{\text{CISCS}}$	O4
16	$\overline{\text{IORD}}$	I	46	RD6	IO4	76	MPD	O4	108	D10	IO4
17	$\overline{\text{OE}}$	I	47	RD7	IO4	77	$\overline{\text{MRST}}$	O4	107	D2	IO4
18	$\overline{\text{CE2}}$	I	48	VSSIO	G	78	MRST	O4	108	D9	IO4
19	$\overline{\text{CE1}}$	I	49	$\overline{\text{RCS0}}$	O4	79	MRI	SI	109	D1	IO4
20	VSSIO	G	50	$\overline{\text{RCS1}}$	O4	80	MSI	SI	110	D8	IO4
21	D15	IO4	51	VDDIO	P	81	MINT	I	111	D0	IO4
22	D14	IO4	52	RA10	O4	82	MRDY	I	112	VSSIO	G
23	D7	IO4	53	RA0	O4	83	CB	O4	113	$\overline{\text{IOIS16}}$	04
24	D13	IO4	54	RA1	O4	84	RRST	O4	114	$\overline{\text{STSCHG}}$	O4
25	D6	IO4	55	RA2	O4	85	VSST	G	115	$\overline{\text{SPKR}}$	O4
26	D12	IO4	56	RA3	O4	86	TPDN	AO	116	$\overline{\text{REG}}$	I
27	D5	IO4	57	RA4	O4	87	TPDP	AO	117	$\overline{\text{INPACK}}$	O4
28	D11	IO4	58	RA5	O4	88	TPON	AO	118	$\overline{\text{WAIT}}$	O4
29	D4	IO4	59	RA6	O4	89	TPOP	AO	119	RESET	SI
30	D3	IO4	60	RA7	O4	90	VDDT	P	120	$\overline{\text{IREQ}}$	O4

Legend:

TYPE	Description	TYPE	Description	TYPE	Description
I	Input (TTL level)	O4	Output with IOL = 4 mA	P, G	Power Ground
CI	CMOS level Input	OD16	Output Open Drain with IOL = 16 mA	R	Resistor to analog ground (20K ± 1%)
SI	Schmitt trigger Input	IO4	Input (TTL level) & Output with IOL = 4 mA		
AI	Analog Input	AO	Analog Output		

PIN DESCRIPTION

HOST BUS INTERFACE - PC CARD BUS

NAME	TYPE	DESCRIPTION
RESET	–	RESET (hardware). Active high. This pin resets the internal LAN function and the modem function by asserting MRST and $\overline{\text{MRST}}$. It also clears the Function Configuration Registers (FCR) including the EnFn bits in the Configuration Option Registers (COR) of both functions thus placing the 78Q8378 in an unconfigured (Memory-Only Interface) state.
$\overline{\text{IOWR}}$	I	I/O WRITE. This pin is an active low input that enables a write operation by the host to the 78Q8378 internal LAN registers or the modem function. The $\overline{\text{REG}}$ signal and at least one of $\overline{\text{CE1}}$ or $\overline{\text{CE2}}$ must also be active for the I/O write to take place. The 78Q8378 will not respond to the $\overline{\text{IOWR}}$ signal until it has been configured for I/O operation by the host.
$\overline{\text{IORD}}$	–	I/O READ. This is an active low input that enables a read operation by the host from the 78Q8378 LAN registers as well as from the modem function. The $\overline{\text{REG}}$ signal and at least one of $\overline{\text{CE1}}$ or $\overline{\text{CE2}}$ must also be active for the I/O read to take place. The 78Q8378 will not respond to the $\overline{\text{IORD}}$ signal until it has been configured for I/O operation by the host.
$\overline{\text{CE1}}$, $\overline{\text{CE2}}$	I	CHIP ENABLE. An active low, input signals as the chip select for the 78Q8378. The $\overline{\text{CE1}}$ enables the even-numbered-address bytes and the $\overline{\text{CE2}}$ enables the odd-numbered-address bytes. The $\overline{\text{CE2}}$ is only used by the LAN function when it is programmed in word mode and not used for attribute memory access.
FCRA	–	FUNCTION CONFIGURATION REGISTER ADDRESS. This pin connects to the PC Card higher address bit. A high (together with $\overline{\text{REG}}$ activation) on this pin selects the internal FCR (Function Configuration Registers) and a low selects the external CIS (Card Information Structure) memory.
$\overline{\text{OE}}$	I	OUTPUT ENABLE. An active low, input signal used to read data from the internal FCR (Function Configuration Registers) and from the external CIS Attribute Memory (through the activation of $\overline{\text{CISCS}}$). This pin needs also to be connected to the output enable of the external memory.
$\overline{\text{WE}}$	I	WRITE ENABLE. An active low, input signal used to write data to the internal FCR (Function Configuration Registers) and to the external CIS Attribute Memory (through the activation of $\overline{\text{CISCS}}$). This pin needs also to be connected to the write enable of the external memory.
$\overline{\text{REG}}$	–	ATTRIBUTE MEMORY SELECT. When this signal is active (low), it signifies access from or to the Attribute Memory (if $\overline{\text{OE}}$ or $\overline{\text{WE}}$ are active) or the I/O space (if $\overline{\text{IORD}}$ or $\overline{\text{IOWR}}$ are active). Attribute Memory is generally used to record card capacity and other configuration and attribute information. This includes the standardized FCR (Function Configuration Registers) which is located internal to the 78Q8378. When Attribute Memory is accessed, only data signals D[0:7] are valid and signals D[8:15] shall be ignored.
A[0:9]	–	ADDRESS BUS. Used for Function Configuration Registers (FCR) selection, CIS memory selection and I/O decoding of both functions.
D[0:15]	I/O	DATA BUS. A bi-directional, tri-state bus. The combinations of $\overline{\text{CE1}}$, $\overline{\text{CE2}}$ and A0 control the portion of the bus that is being utilized. A[0:3] and RBNK1,0 (DLCR7<3:2>) select the set of internal registers for access.

HOST BUS INTERFACE - PC CARD BUS (continued)

The following output signals are inactive (high) until the 78Q8378 is configured for I/O mode.

PIN	TYPE	DESCRIPTION
$\overline{\text{WAIT}}$	O	WAIT. An active low output that is asserted to delay completion of the current I/O read or write operation. It is only used by the LAN function and not by the modem function. This signal will only be active after the 78Q8378 is configured for I/O mode.
$\overline{\text{INPACK}}$	O	INPUT ACKNOWLEDGE. This active low output signal is asserted when the 78Q8378 is selected and it can respond to an I/O read cycle requested by the host. This signal is used by the host to control the enable of any input data buffer between the card and the CPU. This signal will only be active after the 78Q8378 is configured for I/O mode.
$\overline{\text{IOIS16}}$	O	I/O IS 16 BIT. This active low output signal is asserted when the 78Q8378 LAN function is configured for word transfer to indicate to the host that it is capable of 16-bit access. For modem function access, this pin remains high. This signal will only be active after the 78Q8378 is configured for I/O mode.
$\overline{\text{IREQ}}$	O	INTERRUPT REQUEST. This signal is available only after the 78Q8378 is configured for I/O mode. The 78Q8378 supports multiple functions interrupt scheme as outlined by the PC Card Multiple Function Spec and both Pulsed- and Level-Mode Interrupt as selected by the LevIREQ register bit in the COR (Configuration Operation Register).
$\overline{\text{SPKR}}$	O	SPEAKER. This signal is held inactive (i.e., high) until the 78Q8378 is configured for I/O mode. It provides a single-amplitude, on-off, binary audio waveform intended to drive the host's loudspeaker. This signal is used by the modem function only and the source is from the MSI pin.
$\overline{\text{STSCHG}}$	O	STATUS CHANGE. Used to alert the host to changes in the RRdy bit in the PRR (Pin Replacement Register) or the RIEvt or PIEvt bits in the IOER (I/O Event Register).

PIN DESCRIPTION (continued)

MODEM INTERFACE (SECOND PERIPHERAL PORT)

The following signals are active only after the modem EnFn bit in the COR (Configuration Option Register) has been set.

PIN	TYPE	DESCRIPTION
$\overline{\text{MCS}}$	O	MODEM CHIP SELECT. This signal is asserted whenever a modem address range is decoded.
$\overline{\text{MINT}}$	I	MODEM INTERRUPT. This modem interrupt is combined with the internal LAN interrupt according to the PCMCIA Multiple Function Spec and passed to $\overline{\text{IREQ}}$ pin.
MRST, $\overline{\text{MRST}}$	O	MODEM RESET. These signals are asserted (both polarity) when there is a hardware reset or a software reset through the modem SRESET bit in the COR (Configuration Option Register).
MPD, $\overline{\text{MPD}}$	O	MODEM POWER DOWN. Both polarity outputs are provided to reflect the modem PwrDwn bit in the CSR (Configuration and Status Register).
MRDY	I	MODEM READY. A low indicates that the modem is not ready. This signal is not intended to delay the completion of an I/O cycle. In fact, no wait state is provided for modem access. This signal is reflected in the RRdy bit in the modem PRR (Pin Replacement Register).
MSI	I	MODEM SPEAKER INPUT. This pin is qualified with the modem Audio bit in the CSR (Configuration and Status Register) to produce the inverted $\overline{\text{SPKR}}$ output.
MRI	I	MODEM RING INPUT. This pin is used to indicate ringing. This signal is latched into the RIEvt bit in the IOER (I/O Event Register).

CIS MEMORY (1 PIN)

$\overline{\text{CISCS}}$	O	CARD INFORMATION STRUCTURE (CIS) CHIP SELECT. Active low signal which indicates that the current cycle is from or to the external CIS Attribute memory. The CIS memory address and data bus connect directly to the PC Card bus and the output enable and write enable pins connect to the $\overline{\text{OE}}$ and $\overline{\text{WE}}$ pins. When the WP bit (BMR12 < 3 >) is set, writing to the CIS memory is prevented.

BUFFER MEMORY INTERFACE

$\overline{\text{RCS0}}$, $\overline{\text{RCS1}}$	O	RAM CHIP SELECT. $\overline{\text{RCS0}}$ and $\overline{\text{RCS1}}$ are active low chip select lines for the SRAM with $\overline{\text{RCS0}}$ as the least significant byte.
ROE	O	RAM OUTPUT ENABLE. Active low. This is the output enable asserted by the 78Q8378 during buffer memory read cycles for the SRAM.
RWE	O	RAM WRITE ENABLE. Active low. This is the write enable asserted by the 78Q8378 during buffer memory write cycles for the SRAM.
RD[0:15]	I/O	RAM DATA BUS. This is the data bus between the 78Q8378 and the buffer memory. It can be configured for byte or word transfer depending on register bit RBYTE (DLCR6 <4>) RAM BYTE. For word transfers, the ordering of the most and least significant byte is defined by the register bit, INTLMOT (DLCR7 <0>). In PC Card bus mode, this data bus is only 8 bits wide (RD[0:7]).
RA[0:15]	O	RAM ADDRESS BUS. Addresses up to 64 KByte of SRAM buffer memory.

NETWORK ATTACHMENT UNIT INTERFACE

PIN	TYPE	DESCRIPTION
DON, DOP	O	TRANSMIT DATA NEGATIVE and POSITIVE. Differential outputs to external transceiver for transmission.
DIN, DIP	I	RECEIVE DATA NEGATIVE and POSITIVE. Manchester differential inputs from external transceiver for reception.
CIN, CIP	I	COLLISION DETECT NEGATIVE and POSITIVE. When an externally connected transceiver detects a collision on the medium, these differential inputs are driven by a 10 MHz signal.
RBIAS	-	EXTERNAL RESISTOR. External biasing resistor. Connect to 20 kΩ ±1% to AGND.

NETWORK TWISTED-PAIR MEDIUM INTERFACE

TPON, TPOP	O	TWISTED-PAIR OUTPUT NEGATIVE and POSITIVE. Driver outputs to twisted-pair medium. Must be summed together with TPDN and TPDP by external resistors in a pre-equalization network to produce twisted-pair transmit signal.
TPDN, TPDP	O	TWISTED-PAIR DELAYED NEGATIVE and POSITIVE. Delayed (50 ns) driver outputs to twisted-pair medium. Must be summed together with TPON and TPOP by external resistors in a pre-equalization network to produce twisted-pair transmit signal.
TPIN, TPIP	I	TWISTED-PAIR INPUT NEGATIVE and POSITIVE. Inputs from twisted-pair medium.

DEVICE POWER

VDD	P	POWER SUPPLY. A +5V DC (±5%) or +3.3 VDC (±0.3V) supply is required.
GND	P	SYSTEM GROUND.
AVDD	P	ANALOG VDD. The analog VDD pin required by the internal AUI and twisted-pair circuits is to be connected to a different VDD path from the digital VDD. A +5V DC (±5%) or +3.3 VDC (±0.3V) supply is required.
AGND	P	ANALOG GROUND. The analog ground required by the internal encoder/decoder is to be connected to a separate GND path from the digital GND.

CRYSTAL OSCILLATOR

OSCI	I	OSCILLATOR IN. Connection for one side of the 20 MHz crystal or an input for an external 20 MHz clock source.
OSCO	O	OSCILLATOR OUT. Connection for other side of the 20 MHz crystal. Left unconnected if an external clock is used.

PIN DESCRIPTION (continued)

MISCELLANEOUS

NAME	TYPE	DESCRIPTION
CB	O	CONTROL BIT. A complement of the internal register bit, DLCR4 < 2 >, which is used to activate any external hardware.
LEDLT	O	LED LINK, TRANSMIT. Connect to LED with current limiting resistor to VDD. LED is on during link up and off during link down. During link up (when LED is on), a transmission will blink off the LED temporarily to indicate activity. This feature is available only for the twisted pair interface.

ELECTRICAL SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Operation beyond the maximum ratings may damage the device.

PARAMETER	RATING
Supply voltage, Vdd	-0.5 to 6.0V
Input voltage, Vin	-0.5 to Vdd + 0.5V
Output voltage, Vout	-0.5 to Vdd + 0.5V
Storage temperature, Tstg	-55 to 150°C
Lead temperature (max 10 sec soldering), Tl	250°C max

DC CHARACTERISTICS (Ta = 0 to 70°C, Vd-d = 5V ±5%, 5V Values)

PARAMETER		CONDITIONS		MIN	NOM	MAX	UNIT
Low level input voltage	Vil	TTL inputs				0.8	V
		OSCI pin				1.6	V
		Schmitt inputs				1.1	V
High level input voltage	Vih	TTL inputs		2.2			V
		OSCI pin		3.8			V
		Schmitt inputs		3.5			V
Pull down current (RESET pin)	Ipd			13		50	µA
Low level output voltage	Vol	Rated Iol		0		0.4	V
High level output voltage	Voh	Rated Ioh		2.4		Vdd	V
Low level output current	Iol	Pin types O4, IO4, IO4U	Vdd = 5V	4			mA
(with Vol = 0.4V)		Pin type O8,	Vdd = 5V	8			mA
		Pin type OD16	Vdd = 5V	16			mA
High level output current	Ioh	Pin types O4 IO4, IO4U	Vdd = 5V	-4			mA
(with Voh = 2.4V)		Pin type O8	Vdd = 5V	-8			mA
Leakage current (input/output)	Il			-10		10	µA
Supply current	Idd	Fully active(1)				40	mA
		Idle				30	mA
Power down supply current	Ipwrdn	Osc. on				10	mA
		Osc. off				100	µA

Note: (1) Fully active means 3 “simultaneous” operations: transmitting, receiving (through twisted-pair port) and either host write or read.

ELECTRICAL SPECIFICATIONS (continued)

DC CHARACTERISTICS (Ta = 0 to 70°C, Vdd = 3.3V ±0.3V, 3V Values)

PARAMETER		CONDITION		MIN	NOM	MAX	UNIT
Low level input voltage	Vil	TTL inputs				0.8	V
		OSCI pin				0.7	V
		Schmitt inputs				0.4	V
High level input voltage	Vih	TTL inputs		2			V
		OSCI pin		2.1			V
		Schmitt inputs		2.4			V
Pull down current (RESET pin)	Ipd			5		28	µA
Low level output voltage	Vol	Rated Iol		0		0.4	V
High level output voltage	Voh	Rated Ioh		2.4		Vdd	V
Low level output current	Iol	Pin types O4, IO4, IO4U	Vdd = 3.3V	2.4			mA
(with Vol = 0.4V)		Pin type O8	Vdd = 3.3V	4.9			mA
		Pin type OD16	Vdd = 3.3V	9.8			mA
High level output current	Ioh	Pin types O4, IO4, IO4U	Vdd = 3.3V	-1.5			mA
(with Voh = 2.4V)		Pin type O8	Vdd = 3.3V	-3			mA
Leakage current (input/output)	Il			-10		10	µA
Supply current	Idd	Fully active(1)				28	mA
		Idle				20	mA
Power down supply current	Ipwrdn	Osc. on				6	mA
		Osc. off				100	µA

Note: (1) Fully active means 3 “simultaneous” operations: transmitting, receiving (through twisted-pair port) and either host write or read.

AUI CHARACTERISTICS
(VDD = 5V ± 5%, 3.3 ± 0.3V, Vss = 0V, Ta = 0°C to +70°C)

Low Output Voltage for DOP, DON Vaol	Rext = 20 kΩ Rl = 78Ω	Vdd-1.5		Vdd-0.75	V
High Output Voltage for DOP, DON Vaoh	Rext = 20 kΩ Rl = 78Ω	Vdd-0.55		Vdd	V
DOP, DON Output Current Iao	Rext = 20 kΩ	8		14	mA

AUI CHARACTERISTICS (continued)
(VDD = 5V ± 5%, 3.3 ± 0.3V, Vss = 0V, Ta = 0°C to +70°C)

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
DIP, DIN, CIP, CIN Open Circuit Input Voltage (bias) Valb	Vdd = 5V ± 5% Vdd = 3.3 ± 0.3V	2.45 2.13		3.33 2.88	V V
DIP, DIN, CIP, CIN Diff Squelch Threshold Vasq		-300		-120	mV
DOP, DON Diff Idle Output Vadi	Rl = 78Ω	-40		40	mV
DOP, DON Diff Peak Output Vadv	Rext = 20 kΩ Rl = 78Ω	620		1100	mV
DOP, DON Output Resistance Rao				75	Ω

TWISTED PAIR
(VDD = 5V ± 5%, Ta = 0°C to +70°C)

TPIP, TPIN Diff Input Resistance Rti		3			kΩ
TPIP, TPIN Open Circuit Input Voltage (bias) Vtib		2.45		3.33	V
TPIP, TPIN Diff Input Voltage Range Vtiv	VDD = 5V	-3.1		3.1	V
TPIP, TPIN Positive Squelched Threshold Vtps	Note 1	300		585	mV
TPIP, TPIN Negative Squelched Threshold Vtns	Note 1	-585		-300	mV
TPIP, TPIN Positive Unsquelched Threshold Vtpu	Note 2		180		mV
TPIP, TPIN Negative Unsquelched Threshold Vtnu	Note 2		-180		mV
TPIP, TPIN Positive Squelched Threshold Long Distance Mode Vltps	Note 1	120		300	mV
TPIP, TPIN Negative Squelched Threshold Long Distance Mode Vltns	Note 1	-300		-120	mV
TPIP, TPIN Positive Unsquelched Threshold Long Distance Mode Vltpu	Note 2		100		mV
TPIP, TPIN Negative Unsquelched Threshold Long Distance Mode Vltnu	Note 2		-100		mV
TPOP, TPON High Output Voltage Vtoh	I = 32 mA	Vdd_{TP} -0.44		Vdd_{TP}	V

TWISTED PAIR (continued)
(VDD = 5V ± 5%, Ta = 0°C to +70°C)

PARAMETER	CONDITION	MIN	NOM	MAX	UNIT
TPOP, TPON Low Output Voltage Vtol	I = 32 mA	Vsstp		Vsstp +0.44	V
TPDP, TPDN High Voltage Vtdh	I = 16 mA	Vddtp -0.44		Vddtp	V
TPDP, TPDN Low Voltage Vtdl	I = 16 mA	Vsstp		Vsstp +0.44	V
TPDP, TPDN Output Resistance Rtd				27	Ω
TPOP, TPON Output Resistance Rto				13.5	Ω

Note 1: Sine wave at 2 MHz, 5 MHz and 7 MHz
Note 2: Sine wave : 5 MHz ≤ *f* ≤ 10 MHz

TWISTED PAIR
(VDD = 3.3 ± 0.3V, Ta = 0°C to +70°C)

TPIP, TPIN Diff Input Resistance Rti		3			kΩ
TPIP, TPIN Open Circuit Input Voltage (bias) Vtib		2.13		2.88	V
TPIP, TPIN Diff Input Voltage Range Vtiv	VDD = 3.3V	-2.2		2.2	V
TPIP, TPIN Positive Squelched Threshold Vtps	Note 1	210		410	mV
TPIP, TPIN Negative Squelched Threshold Vtns	Note 1	-410		-210	mV
TPIP, TPIN Positive Unsquelched Threshold Vtpu	Note 2		130		mV
TPIP, TPIN Negative Unsquelched Threshold Vtnu	Note 2		-130		mV
TPIP, TPIN Positive Squelched Threshold Long Distance Mode Vltps	Note 1	90		210	mV
TPIP, TPIN Negative Squelched Threshold Long Distance Mode Vltns	Note 1	-210		-90	mV
TPIP, TPIN Positive Unsquelched Threshold Long Distance Mode Vltpu	Note 2		70		mV
TPIP, TPIN Negative Unsquelched Threshold Long Distance Mode Vltnu	Note 2		-70		mV

TWISTED PAIR (continued)
(VDD = 3.3 ± 0.3V, Ta = 0°C to +70°C)

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
TPOP, TPON High Output Voltage Vtoh	I = 50 mA	V_{ddTP} -0.3		V_{ddTP}	V
TPOP, TPON Low Output Voltage Vtol	I = 50 mA	V_{SSTP}		V_{SSTP} +0.3	V
TPDP, TPDN High Voltage Vtdh	I = 25 mA	V_{ddTP} -0.3		V_{ddTP}	V
TPDP, TPDN Low Voltage Vtdl	I = 25 mA	V_{SSTP}		V_{SSTP} +0.3	V
TPDP, TPDN Output Resistance Rtd				12	Ω
TPOP, TPON Output Resistance Rto				6	Ω

Note 1: Sine wave at 2 MHz, 5 MHz and 7 MHz
Note 2: Sine wave: 5 MHz ≤ *f* ≤ 10 MHz

TRANSFORMER RATIO:

5V OPERATION		3.3V OPERATION	
RX	TX	RX	TX
1:1	1:1	1:1.4 (step down)	1:1.4 (step down)

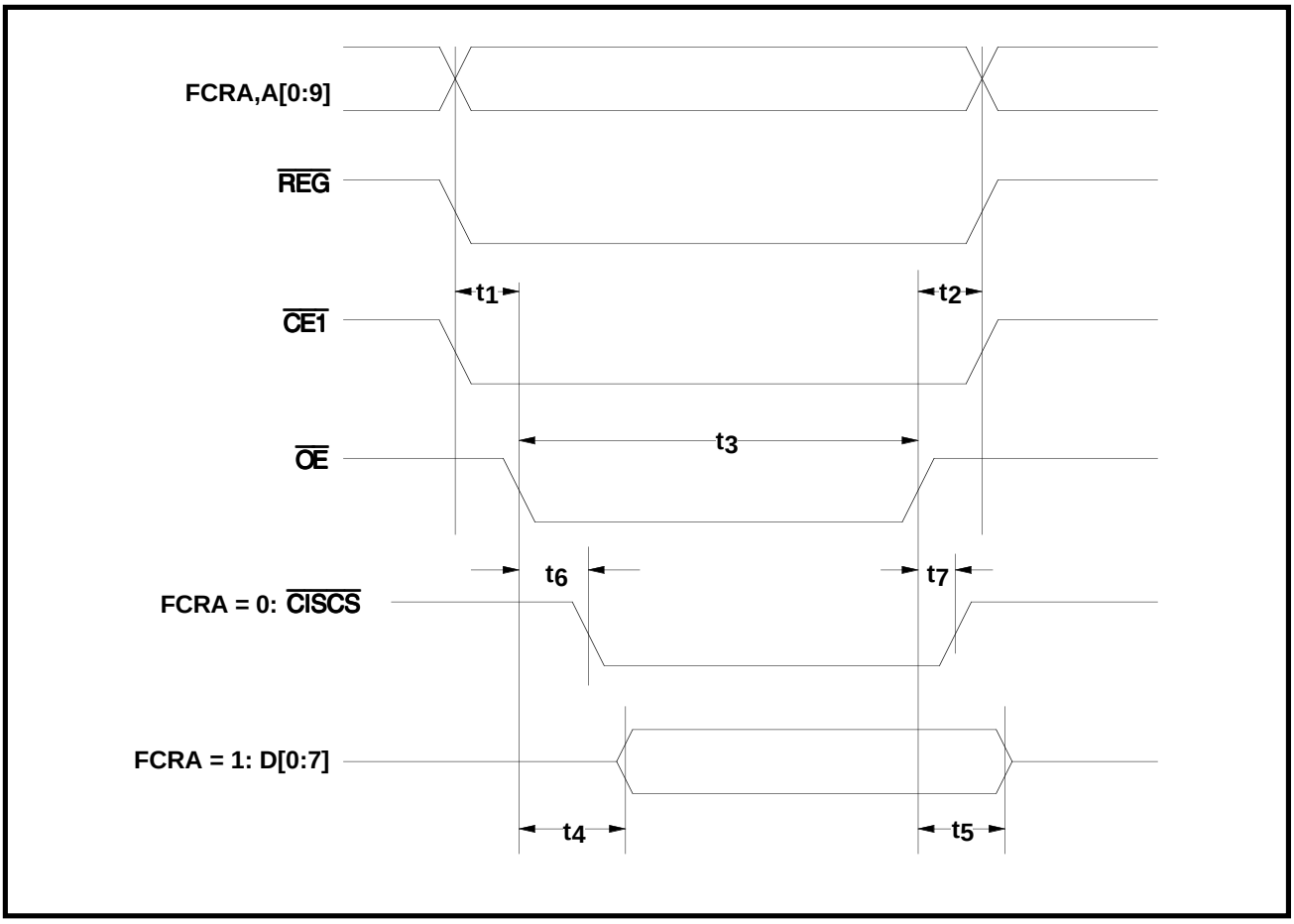


FIGURE 2: Attribute Memory Read Cycle

Unless otherwise stated, the following conditions apply to the remaining timing tables:
Ta = 0°C to + 70°C, Vdd = 5 ± 5%, Vdd = 3.3V ± 0.3V

TABLE 1: Attribute Memory Read Cycle (Refer to Figure 2)

PARAMETER		CONDITION	MIN	NOM	MAX	UNIT
FCRA, A[0:9] Valid to $\overline{OE}$ low; $\overline{REG}$, $\overline{CE1}$ low to $\overline{OE}$ low	t_1		0			ns
$\overline{OE}$ high to A[0:9], FCRA invalid; $\overline{OE}$ high to $\overline{REG}$, $\overline{CE1}$ high	t_2		0			ns
$\overline{OE}$ low pulse width	t_3		45			ns
$\overline{OE}$ low to D[0:7] valid	t_4				50	ns
$\overline{OE}$ high to D[0:7] invalid (data hold)	t_5		5			ns
$\overline{OE}$ low to $\overline{CISCS}$ low	t_6				25	ns
$\overline{OE}$ high to $\overline{CISCS}$ high	t_7				25	ns

TABLE 2: Attribute Memory Write Cycle (Refer to Figure 3)

FCRA, A[0:9] Valid to $\overline{WE}$ low; $\overline{REG}$, $\overline{CE1}$ low to $\overline{WE}$ low	t_1		0			ns
$\overline{WE}$ high to A[0:9], FCRA invalid; $\overline{WE}$ high to $\overline{REG}$, $\overline{CE1}$ high	t_2		0			ns
$\overline{WE}$ low pulse width	t_3		45			ns
D[0:7] valid to $\overline{WE}$ high (data setup)	t_4		15			ns
$\overline{WE}$ high to D[0:7] invalid (data hold)	t_5		10			ns
$\overline{WE}$ low to $\overline{CISCS}$ low	t_6				25	ns
$\overline{WE}$ high to $\overline{CISCS}$ high	t_7				25	ns

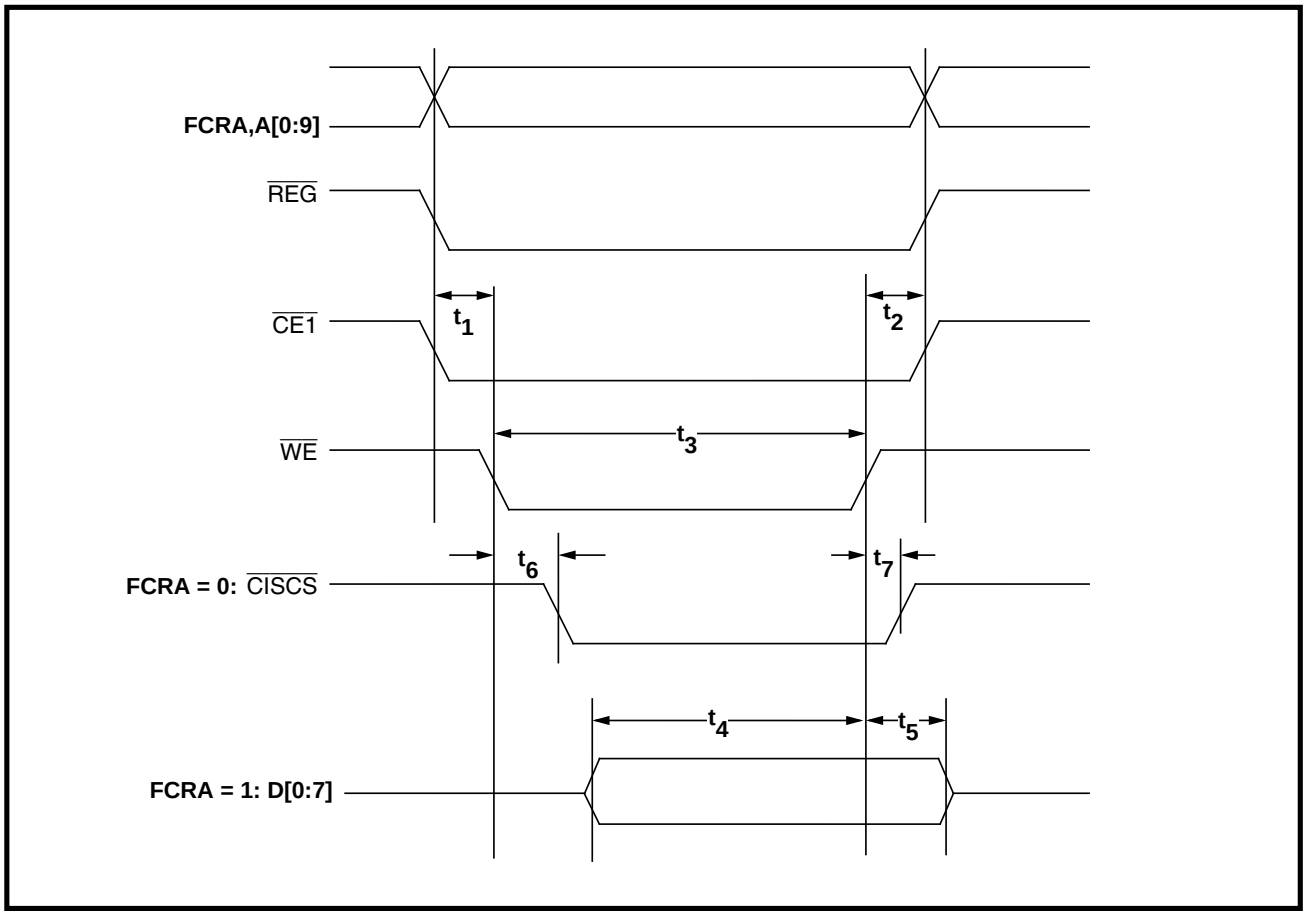


FIGURE 3: Attribute Memory Write Cycle

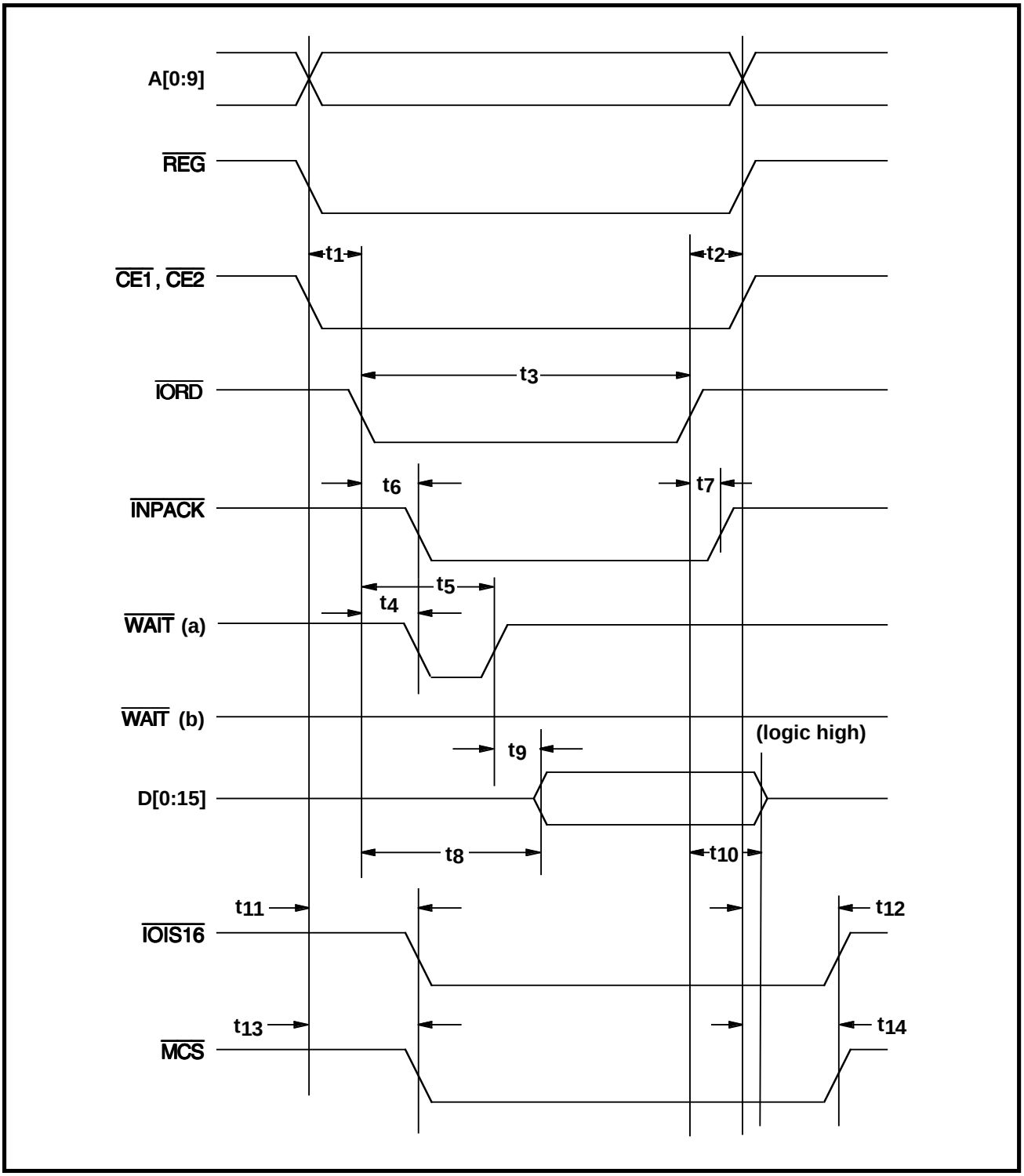


FIGURE 4: I/O Read Cycle

ELECTRICAL SPECIFICATIONS (continued)

TABLE 3: I/O Read Cycle (Refer to Figure 4)

PARAMETER	CONDITION	MIN	NOM	MAX	UNIT
A[0:9] valid to $\overline{IORD}$ LOW; $\overline{REG}$, $\overline{CE1}$, $\overline{CE2}$ low to $\overline{IORD}$ low t_1		0			ns
$\overline{IORD}$ high to A[0:9] invalid; $\overline{IORD}$ high to $\overline{REG}$, $\overline{CE1}$, $\overline{CE2}$ high t_2		0			ns
$\overline{IORD}$ low pulse width t_3		45			ns
$\overline{IORD}$ low to $\overline{WAIT}$ low t_4	Port busy (a)	0		40	ns
$\overline{IORD}$ low to $\overline{WAIT}$ high(1) t_5	Port busy (a)			350	ns
$\overline{IORD}$ low to $\overline{INPACK}$ low t_6				25	ns
$\overline{IORD}$ high to $\overline{INPACK}$ high t_7				25	ns
$\overline{IORD}$ low to D[0:15] valid t_8	Register access (b)			70	ns
$\overline{WAIT}$ high to D[0:15] valid t_9	Port busy (a)			5	ns
$\overline{IORD}$ high to D[0:15] invalid (data hold) t_{10}		5			ns
A[0:9] valid to $\overline{IOIS16}$ low; $\overline{REG}$, $\overline{CE1}$, $\overline{CE2}$ low to $\overline{IOIS16}$ low t_{11}				30	ns
A[0:9] invalid to $\overline{IOIS16}$ high; $\overline{REG}$, $\overline{CE1}$, $\overline{CE2}$ high to $\overline{IOIS16}$ high t_{12}				30	ns
A[0:9] valid to $\overline{MCS}$ low t_{13}				30	ns
A[0:9] invalid to $\overline{MCS}$ high t_{14}				30	ns

Note: (1) Maximum of 350 ns may occur if system makes contiguous system read cycles at less than 100 ns intervals, and both the transmitter and receiver are active in "loopback" reception (if the transmitter and receiver are idle, the max value becomes 250 ns). 2.4 µs max for host read error.

(a) For Buffer Memory Port when port is busy.

(b) For register or port is not busy.

TABLE 4: I/O Write Cycle (Refer to Figure 5)

PARAMETER		CONDITION	MIN	NOM	MAX	UNIT
A[0:9] valid to $\overline{IOWR}$ LOW; $\overline{REG}$, $\overline{CE1}$, $\overline{CE2}$ low to $\overline{IORD}$ low	t_1		0			ns
$\overline{IOWR}$ high to A[0:9] invalid; $\overline{IOWR}$ high to $\overline{REG}$, $\overline{CE1}$, $\overline{CE2}$ high	t_2		0			ns
$\overline{IOWR}$ low pulse width	t_3		45			ns
$\overline{IOWR}$ low to $\overline{WAIT}$ low	t_4	Port busy (a)	0		40	ns
$\overline{IOWR}$ low to $\overline{WAIT}$ high(1)	t_5	Port busy (a)			350	ns
D[0:15] valid to $\overline{IOWR}$ high (data setup)	t_6		15			ns
$\overline{IOWR}$ high to D[0:15] invalid (data hold)	t_7		10			ns
A[0:9] valid to $\overline{IOIS16}$ low	t_8				30	ns
A[0:9] invalid to $\overline{IOIS16}$ high	t_9				30	ns
A[0:9] valid to $\overline{MCS}$ low	t_{10}				30	ns
A[0:9] invalid to $\overline{MCS}$ high	t_{11}				30	ns

Note: (1) Maximum of 350 ns may occur if system makes contiguous system read cycles at less than 100 ns intervals, and both the transmitter and receiver are active in "loopback" reception (if the transmitter and receiver are idle, the max value becomes 250 ns). 2.4 µs max for host write error.

(a) For Buffer Memory Port when port is busy.

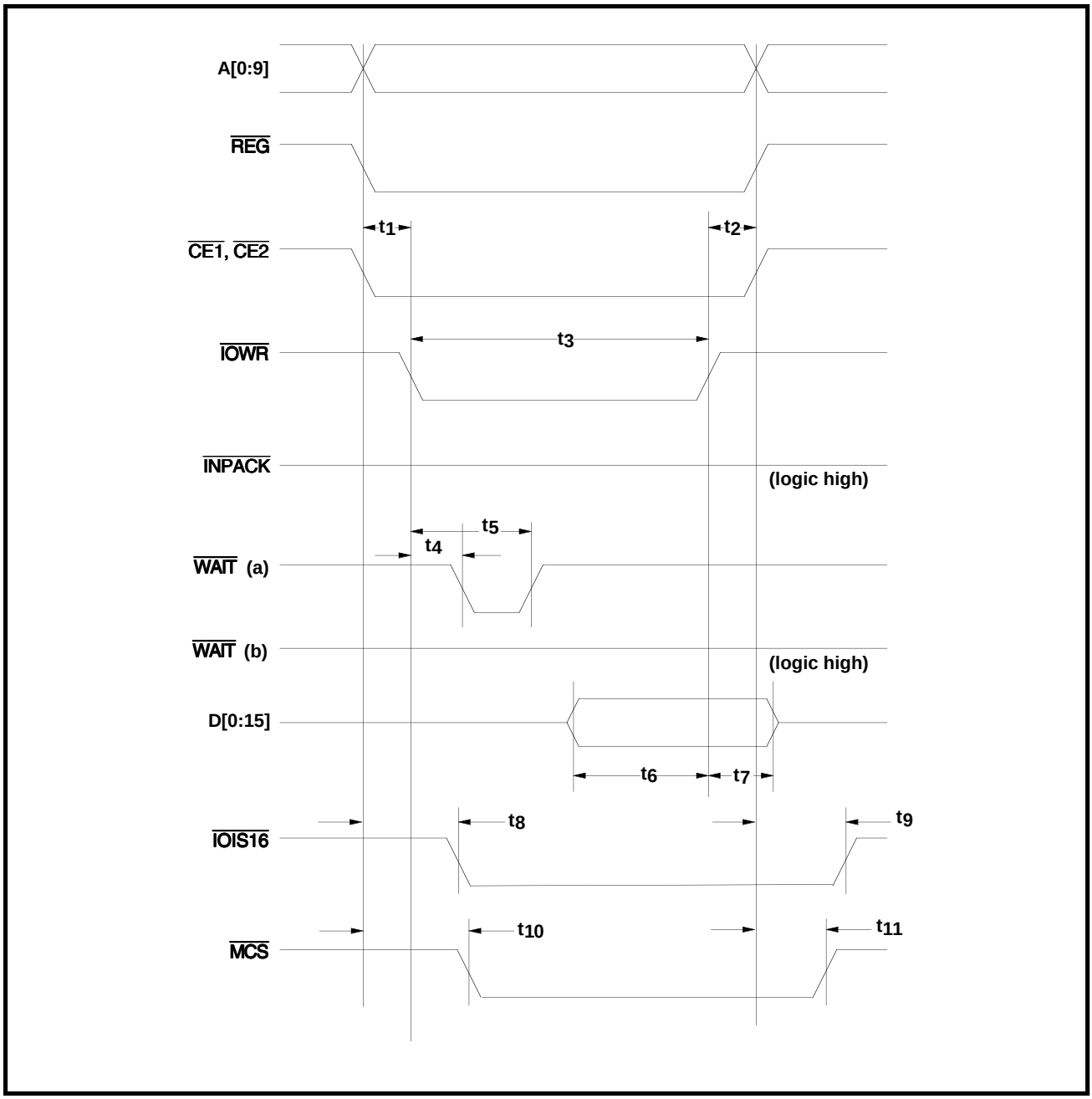


FIGURE 5: I/O Write Cycle

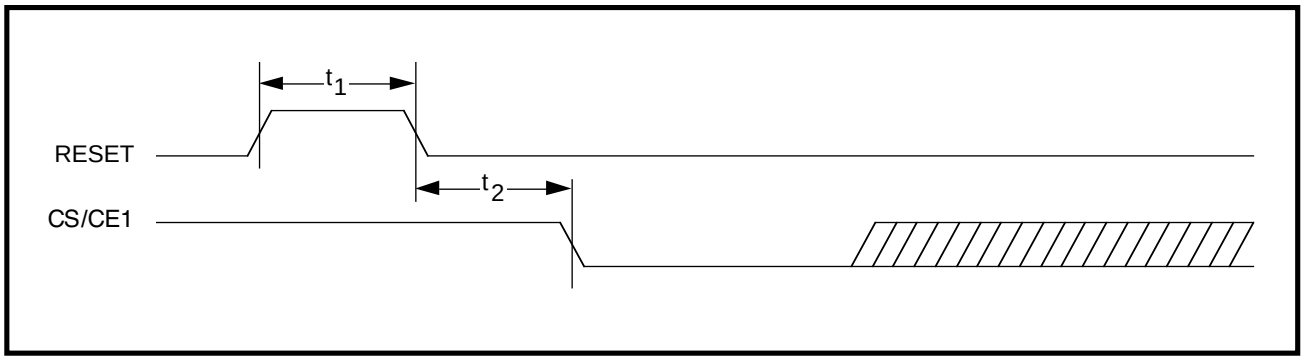


FIGURE 6: RESET Timing

ELECTRICAL SPECIFICATIONS (continued)

TABLE 5: RESET Timing

PARAMETER	CONDITION	MIN	NOM	MAX	UNIT
RESET pulse width t_1		500			ns
RESET low to first $\overline{CS}/\overline{CE1}$ low t_2		800			ns

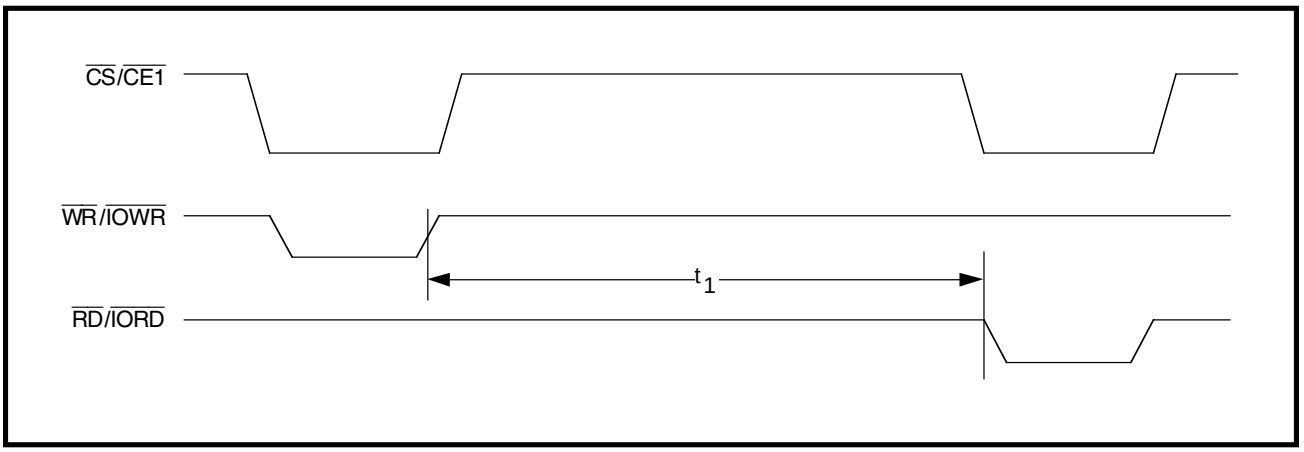


FIGURE 7: Skip Packet Timing

TABLE 6: Skip Packet Timing

Writing Skip Packet high to next Buffer Memory Port read t_1		200			ns

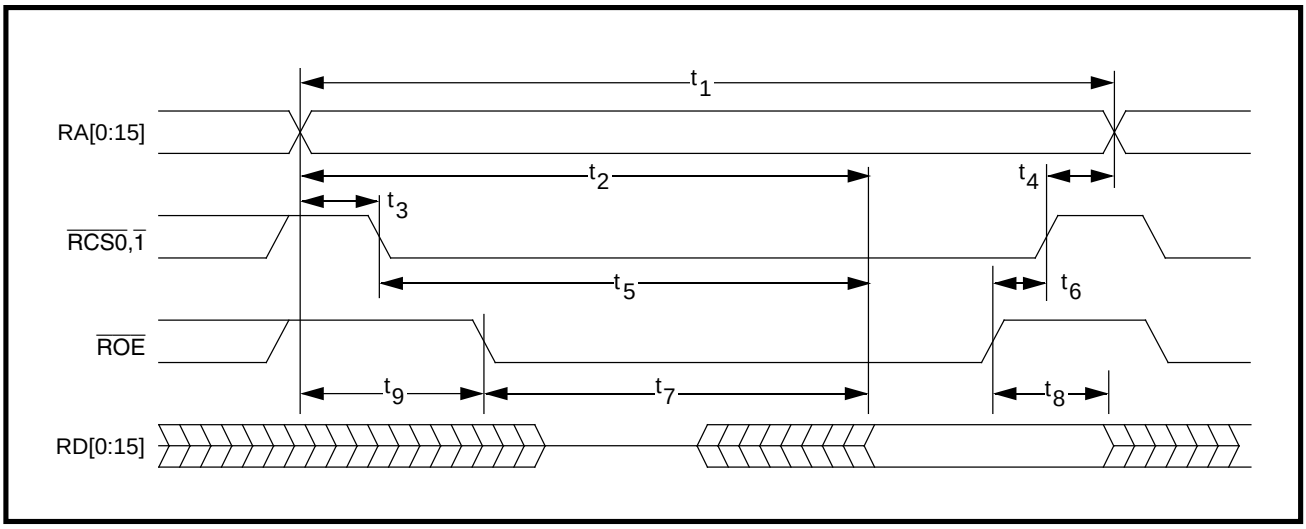


FIGURE 8: SRAM Read Timing

TABLE 7: SRAM Read Timing

PARAMETER		CONDITION	MIN	NOM	MAX	UNIT
Read cycle	t_1	RAMSP = 1	95			ns
		RAMSP = 0	145			ns
Address access time	t_2	RAMSP = 1			75	ns
		RAMSP = 0			125	ns
Address valid to $\overline{RCS0,1}$ low	t_3				8	ns
$\overline{RCS0,1}$ high to address invalid	t_4		0			ns
Chip select access time	t_5	RAMSP = 1			75	ns
		RAMSP = 0			125	ns
$\overline{ROE}$ high to $\overline{RCS0,1}$ high	t_6		0		8	ns
Output enable access time	t_7	RAMSP = 1			50	ns
		RAMSP = 0			100	ns
Data hold time	t_8		0			ns
Address valid to $\overline{ROE}$ low	t_9				30	ns

Note: Use SRAM with address access time of 75 ns or less for RAMSP = 1 and 125 ns or less for RAMSP = 0. RAMSP is DLCR6 <6>.

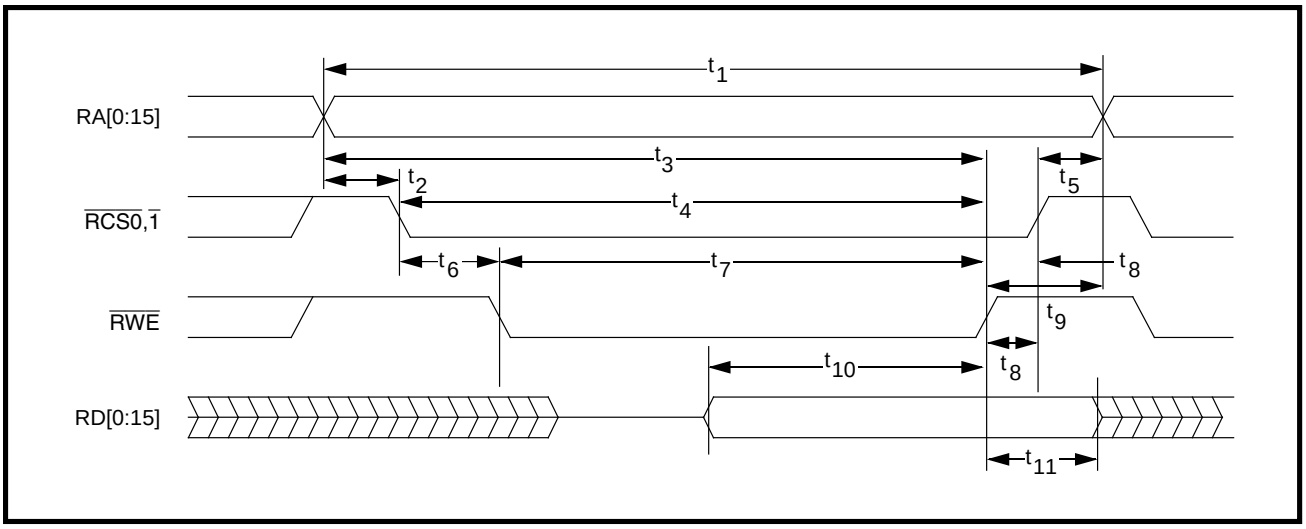


FIGURE 9: SRAM Write Timing

ELECTRICAL SPECIFICATIONS (continued)

TABLE 8: SRAM Write Timing

PARAMETER		CONDITION	MIN	NOM	MAX	UNIT
Write Cycle	t_1	RAMSP = 1	95			ns
		RAMSP= 0	145			ns
Address Valid to $\overline{RCS0,1}$ low	t_2				8	ns
Address Valid to $\overline{RWE}$ high	t_3	RAMSP = 1	70			ns
		RAMSP = 0	120			ns
$\overline{RCS0,1}$ low to $\overline{RWE}$ high	t_4	RAMSP = 1	70			ns
		RAMSP = 0	120			ns
$\overline{RCS0,1}$ high to Address Invalid	t_5		0			ns
$\overline{RCS0,1}$ low to $\overline{RWE}$ low	t_6		0			ns
$\overline{RWE}$ Pulse Width	t_7	RAMSP = 1	70			ns
		RAMSP = 0	120			ns
$\overline{RWE}$ high to $\overline{RCS0,1}$ high	t_8		0			ns
$\overline{RWE}$ high to Address Invalid	t_9		10			ns
Data Setup Time	t_{10}	RAMSP = 1	40			ns
		RAMSP = 0	90			ns
Data Hold Time	t_{11}		20			ns

Note: Use SRAM with address access time of 75 ns or less for RAMSP = 1 and 125 ns or less for RAMSP = 0. RAMSP is DLCR6 <6>.

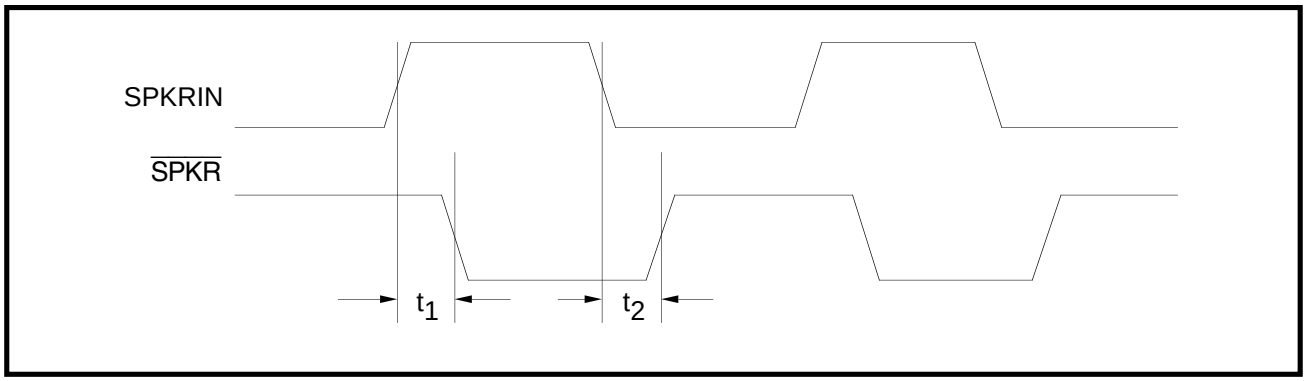


FIGURE 10: Speaker Timing

ELECTRICAL SPECIFICATIONS (continued)

TABLE 9: Speaker Timing (Refer to Figure 10)

PARAMETER	CONDITION	MIN	NOM	MAX	UNIT
$\overline{SPKR}$	Vdd = 5V			25	ns
high to low propagation delay t_1	Vdd = 3.3V			30	ns
$\overline{SPKR}$	Vdd = 5V			25	ns
low to high propagation delay t_2	Vdd = 3.3V			30	ns

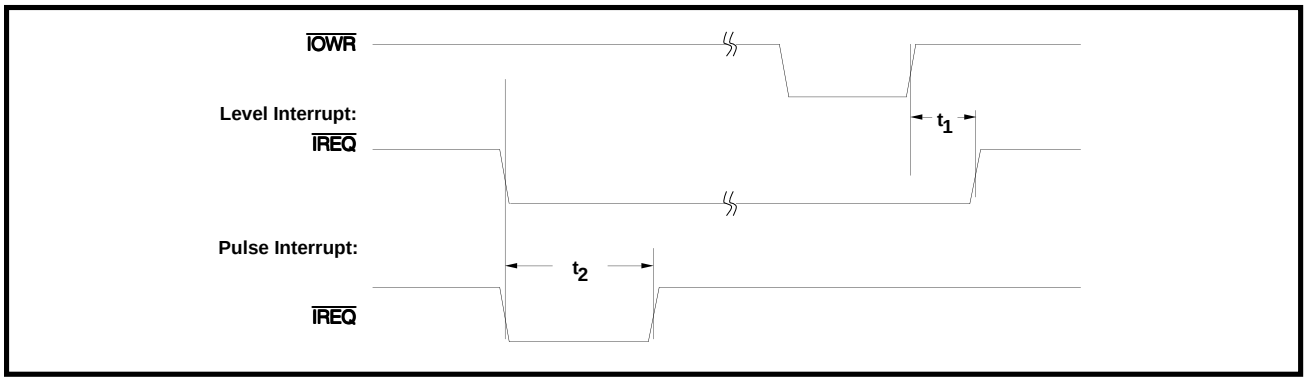


FIGURE 11: Single Interrupt Timing

TABLE 10: Single Interrupt Timing (Refer to Figure 11)

PARAMETER		CONDITION	MIN	NOM	MAX	UNIT
$\overline{IREQ}$ signal clearing delay by $\overline{IOWR}$	t_1	level interrupt			85	ns
$\overline{IREQ}$ low pulse width	t_2	pulse interrupt	750		850	ns

Note: Intrack bit (CSR[0]) must be set to 0 for both functions for single interrupt mode.

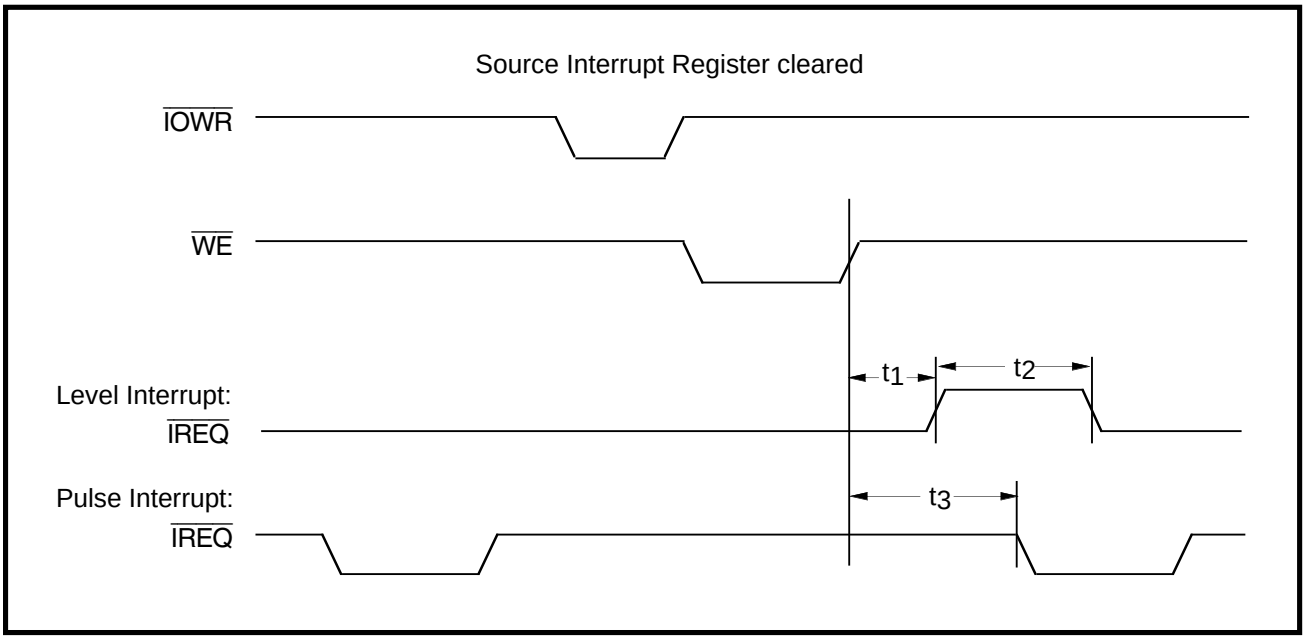


FIGURE 12: Shared Interrupt

TABLE 11: Shared Interrupt (Refer to Figure 12)

PARAMETER		CONDITION	MIN	NOM	MAX	UNIT
$\overline{IREQ}$ signal clearing delay by $\overline{WE}$	t_1	Level interrupt			40	ns
Back to back level interrupt inactive time	t_2	Pending level interrupt	750		850	ns
Pulse interrupt assertion delay	t_3	Pending Pulse interrupt	750		850	ns

Note: 1. Intrack bit (CSR[0]) must be set to 1 & Dintr bit (CORb[3]) to 0 for shared interrupt mode.
2. $\overline{IREQ}$ can only be cleared by host write 0 to intr bit (COR[1]) after clearing the interrupt source registers, DLCR1 or DLCR2.

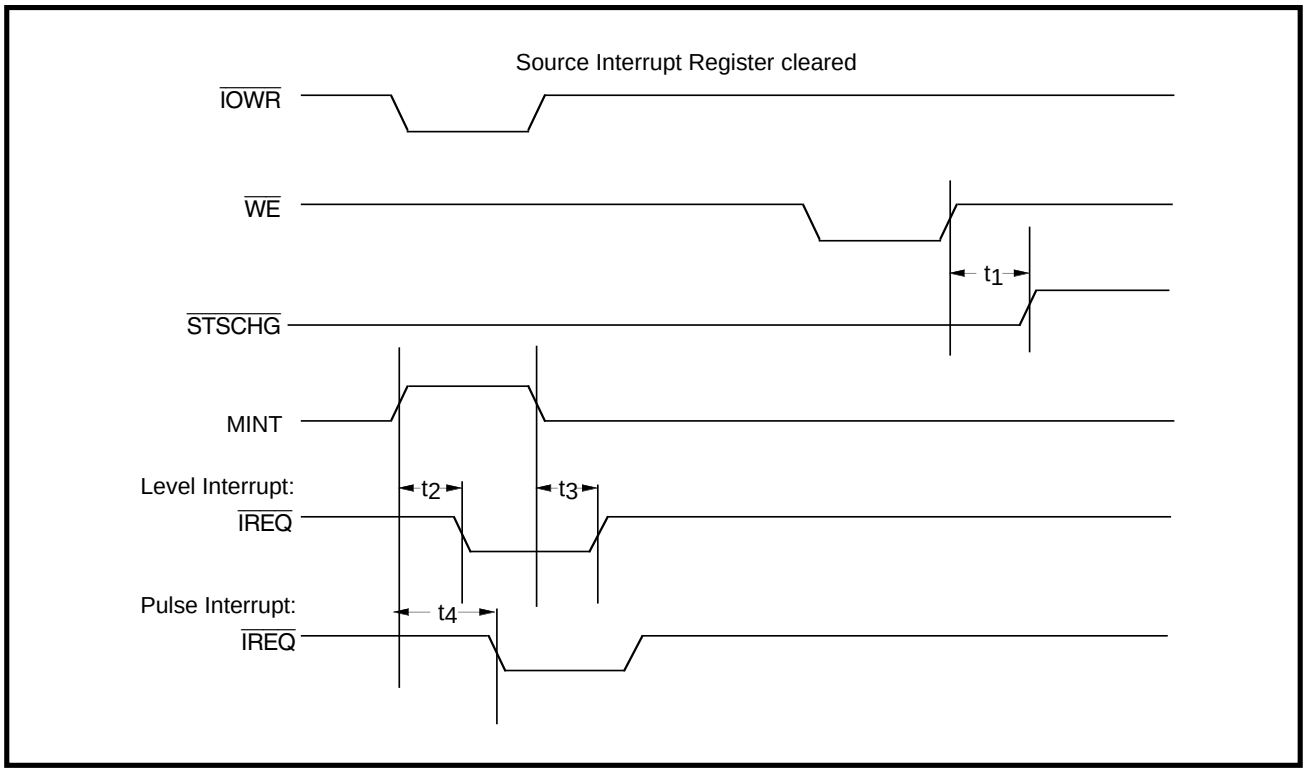


FIGURE 13: Dual Interrupt

ELECTRICAL SPECIFICATIONS (continued)

TABLE 12: Dual Interrupt (Refer to Figure 13)

PARAMETER		CONDITION	MIN	NOM	MAX	UNIT
$\overline{\text{STSCHG}}$ clearing delay for $\overline{\text{WE}}$	t_1				40	ns
Mint high to $\overline{\text{IREQ}}$ low	t_2	Level interrupt			55	ns
Mint low to $\overline{\text{IREQ}}$ high	t_3	Level interrupt			55	ns
Mint high to $\overline{\text{IREQ}}$ low	t_4	Pulse interrupt			55	ns

Note: 1. $\overline{\text{STSCHG}}$ can be cleared by writing 08H into PRRb register after clearing interrupt source registers.
2. Dintr bit (CORb[3]) must be set to high & Intrack bit (CSRb[0]) to low for dual interrupt mode.

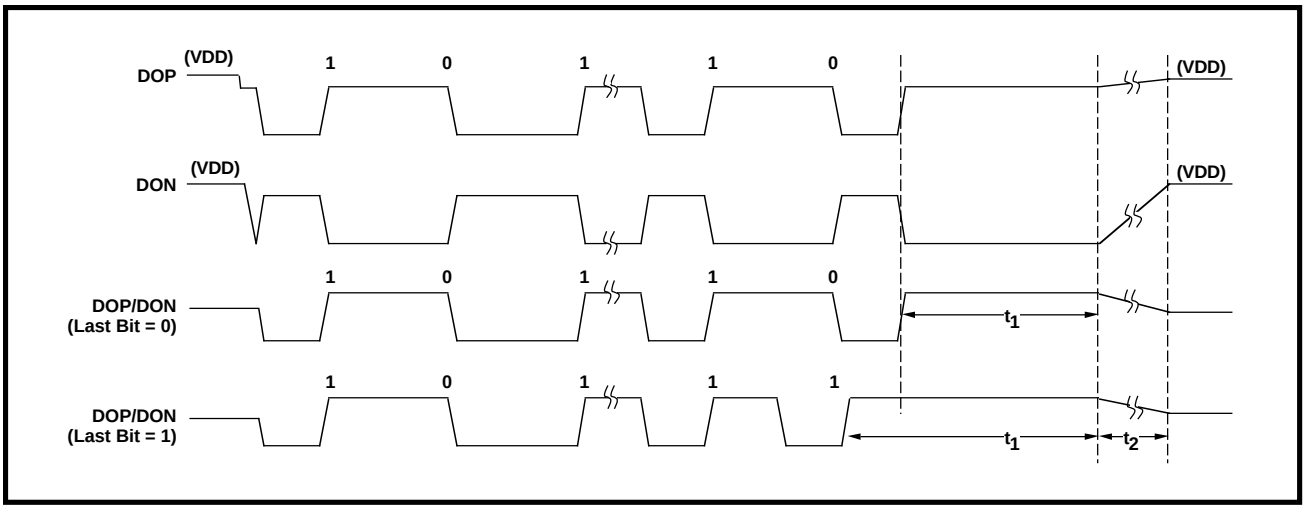


FIGURE 14: Transmit Timing (AUI)

TABLE 13: Transmit Timing (AUI)

DOP/DON end-of-packet delimiter	t_1		200			ns
DOP/DON line voltage transition	t_2				8	µs

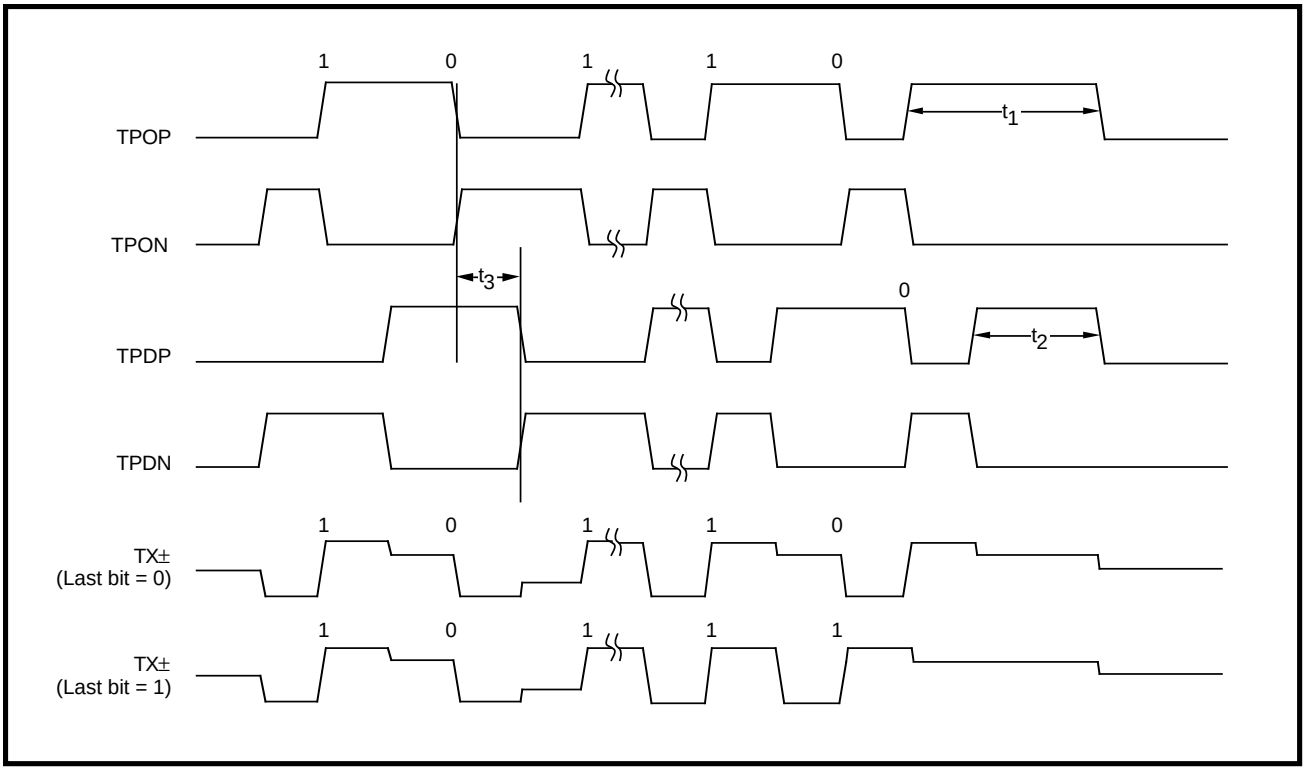


FIGURE 15: Transmit Timing (TP)

ELECTRICAL SPECIFICATIONS (continued)

TABLE 14: Transmit Timing (TP)

PARAMETER	CONDITION	MIN	NOM	MAX	UNIT
TPOP/TPON end-of-packet delimiter t_1		250			ns
TPDP/TPDN end-of-packet delimiter t_2		200			ns
TPOP to TPDP and TPON to TPDN delay t_3			50		ns

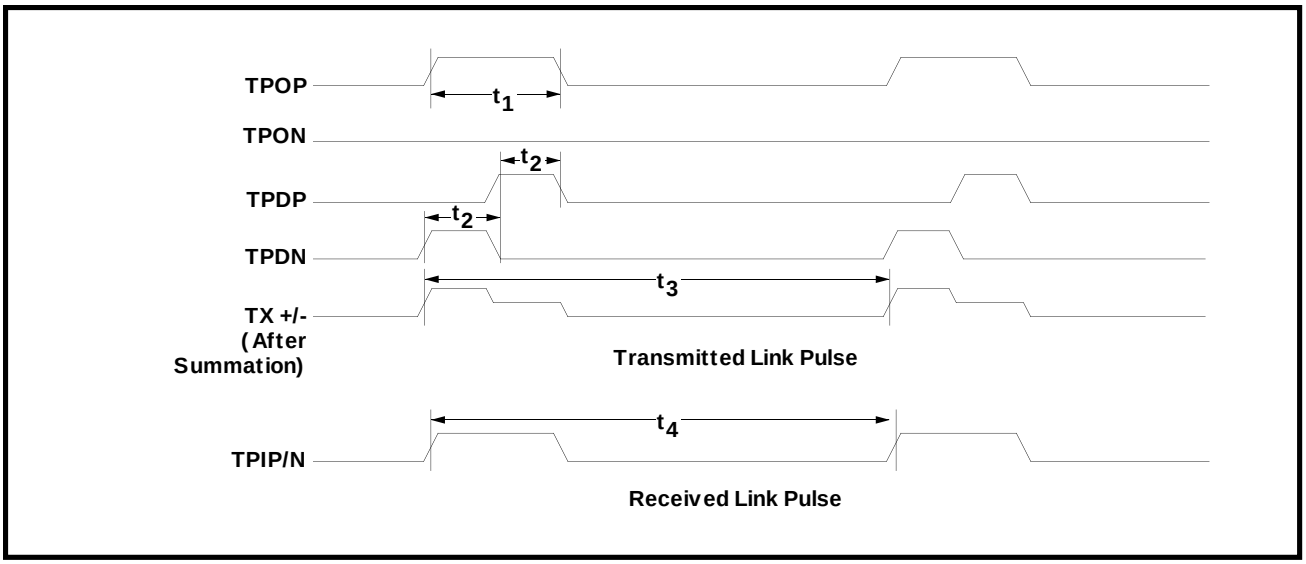


FIGURE 16: Link Test Timing

TABLE 15: Link Test Timing

PARAMETER		CONDITION	MIN	NOM	MAX	UNIT
TPOP link pulse width	t_1			150		ns
TPDP/TPDN link pulse width	t_2			100		ns
Duration between transmitted link pulses	t_3		9		11	ms
Duration between received link pulses	t_4		4.1		65	ms

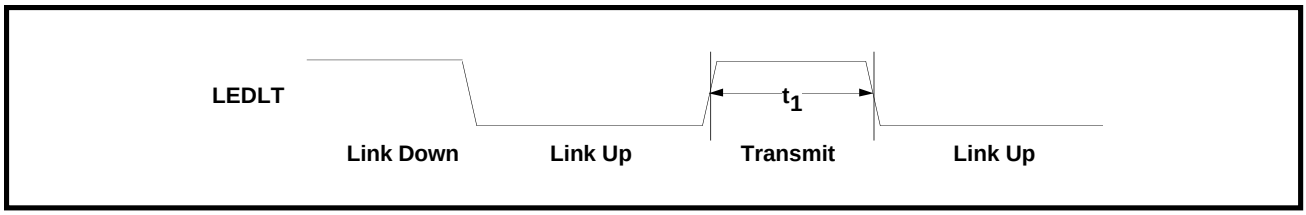


FIGURE 17: LED Timing (TP)

ELECTRICAL SPECIFICATIONS (continued)

TABLE 16: LED Timing

PARAMETER		CONDITION	MIN	NOM	MAX	UNIT
Transmit blink-off timing	t_1	TP selected		100		ms

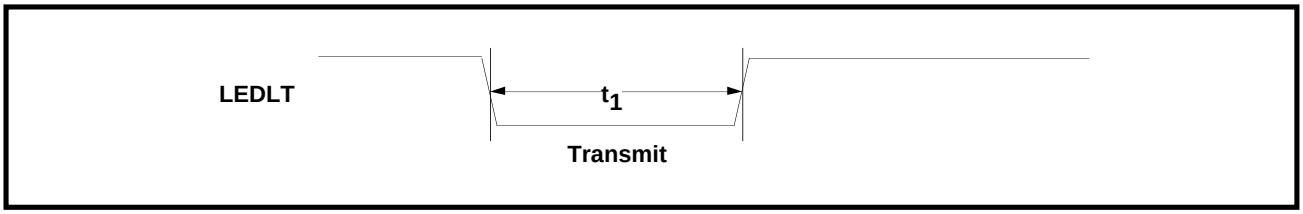


FIGURE 18: LED Timing (AUI)

TABLE 17: LED Timing

Transmit blink-on timing	t_1	AUI selected		100		ms

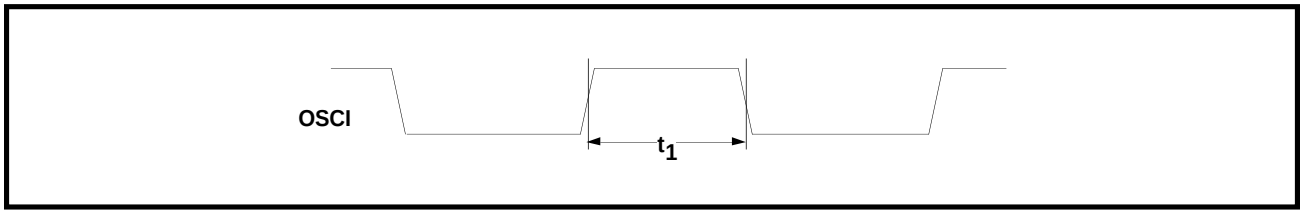


FIGURE 19: Oscillator Duty Cycle

TABLE 18: OSCI Duty Cycle

Oscillator duty cycle	t_1		40	50	60	%

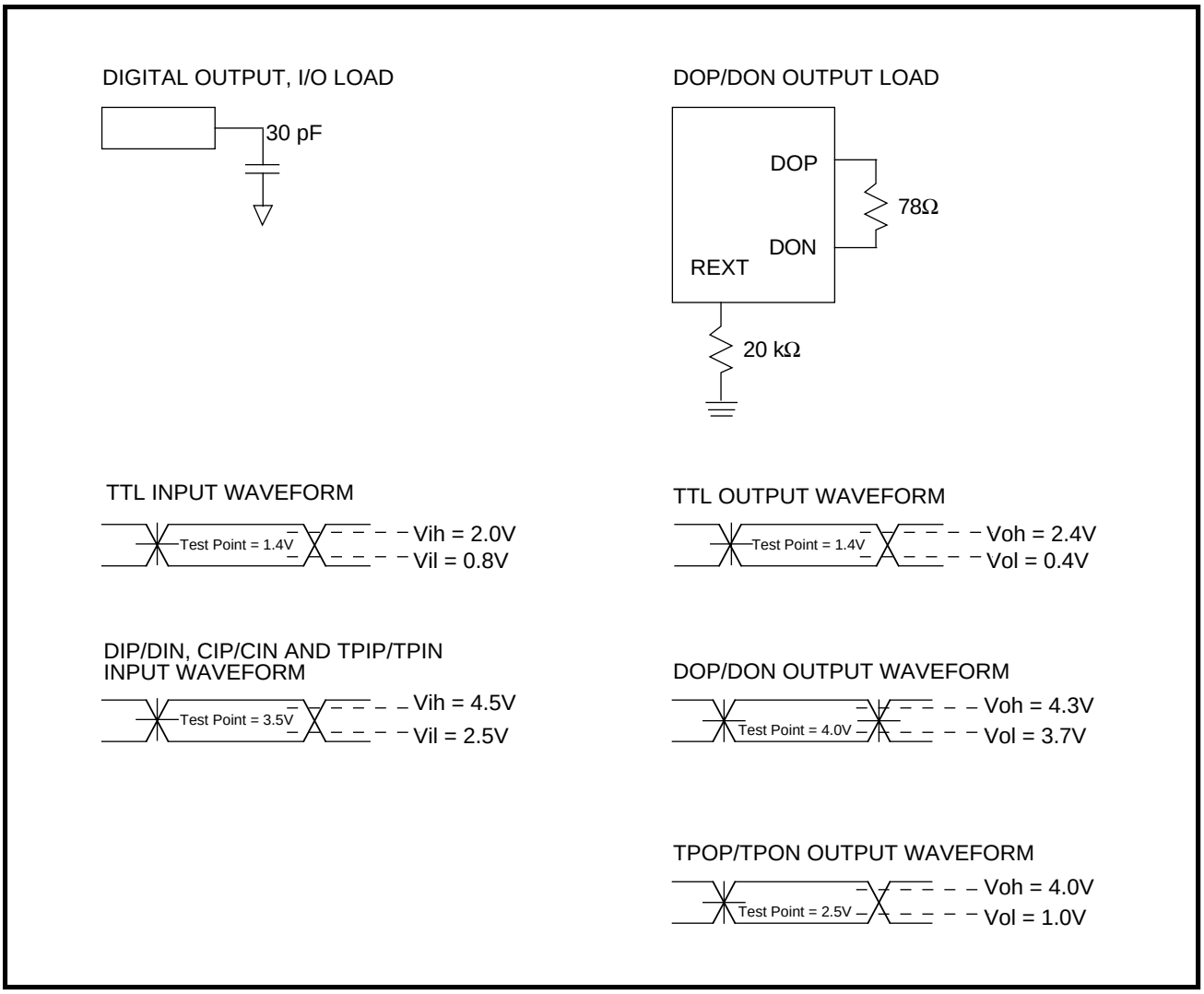
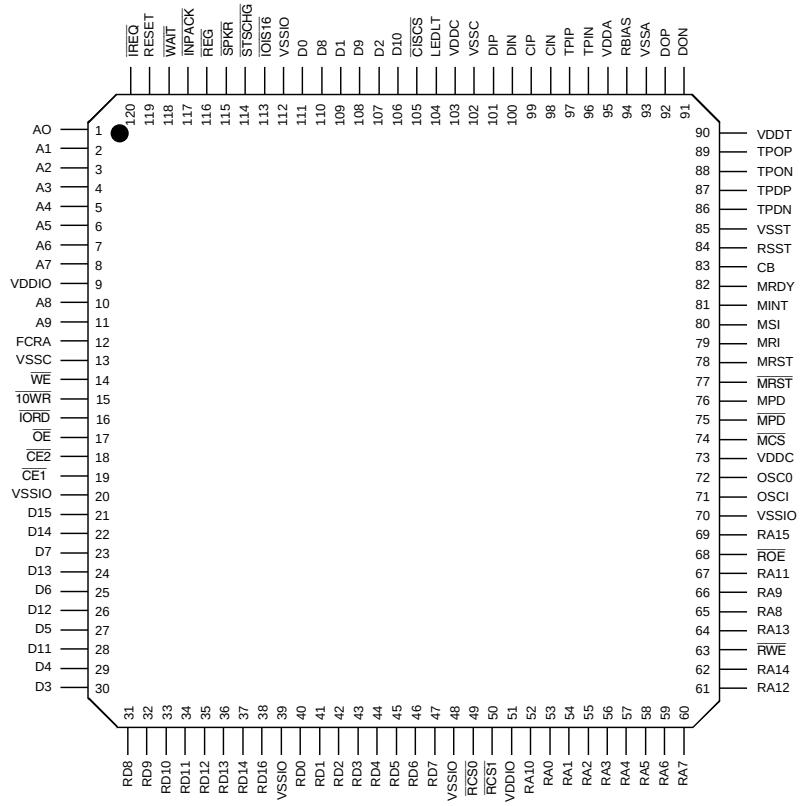


FIGURE 20: Test Conditions

SSI 78Q8378
3V, 5V PC Card
Multi-function Ethernet Combo

PACKAGE PIN DESIGNATIONS

(Top View)



120-Lead TQFP

CAUTION: Use handling procedures necessary for a static sensitive component.

ORDERING INFORMATION

PART DESCRIPTION		ORDER NUMBER	PACKAGE MARK
SSI 78Q8378	120-Lead TQFP	78Q8378GT	78Q8378-CGT

Preliminary Data: Indicates a product not completely released to production. The specifications are based on preliminary evaluations and are not guaranteed. Small quantities are available, and Silicon Systems should be consulted for current information.

Silicon Systems, Inc., 14351 Myford Road, Tustin, CA 92680-7022 (714) 573-6000, FAX (714) 573-6914

Section 8

PROGRAMMABLE ELECTRONICS FILTERS

SSI 32F8001/8002
Low-Power Programmable Electronic Filter

December 1994

DESCRIPTION

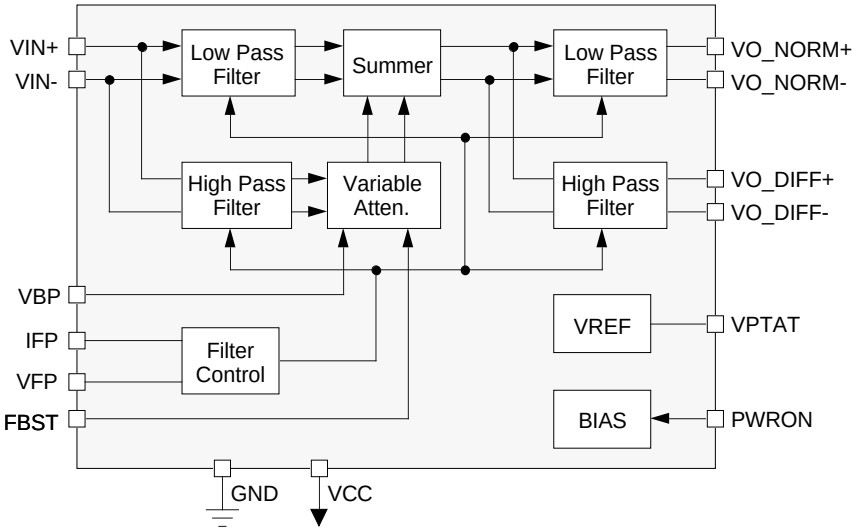
The SSI 32F8001/8002 Programmable Electronic Filter provides an electronically controlled low–pass filter with a separate differentiated low–pass output. A seven–pole, low–pass filter is provided along with a single-pole, single-zero differentiator. Both outputs have matched delays. The delay matching is unaffected by any amount of programmed equalization or bandwidth. This programability combined with low group delay variation make the SSI 32F8001/8002 ideal for use in constant density recording applications. Pulse slimming equalization is accomplished by a two–pole, low–pass with a two–pole, high–pass feed forward section to provide complimentary real axis zeros. A variable attenuator is used to program the zero locations.

The SSI 32F8001/8002 programmable equalization and bandwidth characteristics can be controlled by external DACs. Fixed characteristics are easily accomplished with three external resistors, in addition equalization can be switched in or out by a logic signal. The SSI 32F8001/8002 requires only a +5V supply and are available in 16-lead SON and SOL packages.

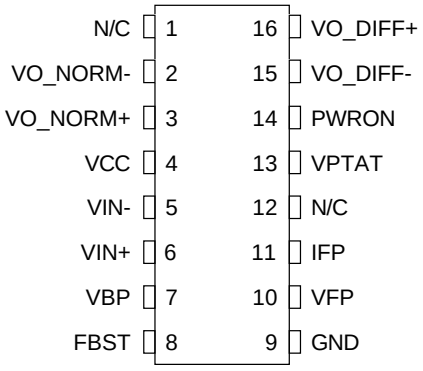
FEATURES

- **Ideal for multi-rate systems applications**
- **Programmable filter cutoff frequency (fc = 9 to 27 MHz, 32F8001; fc = 6 to 18 MHz, 32F8002)**
- **Programmable pulse slimming equalization (0 to 13.5 dB boost at the filter cutoff frequency)**
- **Matched normal and differentiated low-pass outputs**
- **Differential filter inputs and outputs**
- **±12% cutoff frequency accuracy**
- **±2% maximum group delay variation from 0.2 fc to fc**
- **Total harmonic distortion less than 1%**
- **No external filter components required**
- **+5V only operation**
- **16-Lead SON and SOL package**
- **Pin compatible with SSI 32F8011**

BLOCK DIAGRAM



PIN DIAGRAM



16-Lead SOL, SON

CAUTION: Use handling procedures necessary for a static sensitive component.

FUNCTIONAL DESCRIPTION

The SSI 32F8001/8002 is a high performance programmable electronic filter. It features a 7-pole 0.05° equiripple linear phase filter with matched normal and differentiated outputs.

CUTOFF FREQUENCY PROGRAMMING

The SSI 32F8001 programmable electronic filter can be set to a filter cutoff frequency from 9 to 27 MHz with no boost. The SSI 32F8002 can set the cutoff frequency from 6 to 18 MHz with no boost.

Cutoff frequency programming can be established using either a current source fed into pin IFP whose output current is proportional to the SSI 32F8001/8002 output reference voltage VPTAT, or by means of an external resistor tied from the output voltage reference pin VPTAT to pin VFP. The former method is optimized using the SSI 32D4661 Time Base Generator, since the current source into pin IFP is available at the DAC F output of the SSI 32D4661. Furthermore, the voltage reference input is supplied to pin VR3 of the SSI 32D4661 by the reference voltage from the VPTAT pin of the SSI 32F8001/8002. This reference voltage is internally generated by a band-gap circuit in conjunction with a temperature varying reference to create a voltage which is proportional to absolute temperature.

The VPTAT voltage will compensate for internal temperature variation of the fc and boost circuits.

The cutoff frequency, determined by the -3 dB point relative to a very low frequency value (< 10 kHz), is related to the current IVFP injected into pin IFP by the following formulas.

fc (ideal, in MHz)

32F8001 = 45.0 • IFP = 45.0 • IVFP • 1.8/VPTAT

32F8002 = 30.0 • IFP = 30.0 • IVFP • 1.8/VPTAT

where IFP and IVFP are in mA, 0.2 < IFP < 0.6 mA, VPTAT is in volts, and Ta = 25°C.

If a current source is used to inject current into pin IFP, pin VFP should be left open.

If the SSI 32F8001/8002 cutoff frequency is set using voltage VPTAT to bias up a resistor tied to pin VFP, the cutoff frequency is related to the resistor value by the following formulas.

fc (ideal, in MHz)

32F8001 = 45.0 • IFP = 45.0 • 1.8/(3 • Rx)

32F8002 = 30.0 • IFP = 30.0 • 1.8/(3 • Rx)

Rx in kΩ

If pin VFP is used to program cutoff frequency, pin IFP should be left open.

MAGNITUDE EQUALIZATION PROGRAMMING

The magnitude equalization, measured in dB, is the amount of high frequency peaking at the cutoff frequency relative to the original -3 dB point. For example, when 12 dB boost is applied, the magnitude response peaks up 9 dB above the DC gain.

The amplitude of the input signal at frequencies near the cutoff frequency can be increased using this feature. Applying an external voltage to pin VBP which is proportional to reference output voltage VPTAT (provided by the VPTAT pin) will set the amount of boost. A fixed amount of boost can be set by an external resistor divider network connected from pin VBP to pins VPTAT and GND. No boost is applied if pin FBST, frequency boost enable, is at a low logic level.

The amount of boost FB at the cutoff frequency Fc is related to the voltage VBP by the formula

FB (ideal, in dB) = 20 $\log_{10}$[3.73(VBP/VPTAT)+1], where 0 < VBP < VPTAT.

POWER ON / OFF

The SSI 32F8001/8002 supports a power down mode for minimal idle mode power dissipation. When PWRON is pulled up to logic 1, the device is in normal operation mode. When PWRON is pulled down to logic 0, or left open, the device is in the power down mode.

PIN DESCRIPTION

NAME	TYPE	DESCRIPTION
VIN+, VIN-	I	Differential Signal Inputs. The input signals must be AC coupled to these pins.
VO_NORM+, VO_NORM-	O	Differential Normal Outputs. The output signals must be AC coupled.
VO_DIFF+, VO_DIFF-	O	Differential Differentiated Outputs. For minimum time skew, these outputs should be AC coupled.
IFP	I	Frequency Program Input. The filter cutoff frequency f_c, is set by an external current IFP, injected into this pin. IFP must be proportional to voltage VPTAT. This current can be set with an external current generator such as a DAC. VFP should be left open when using this pin.
VFP	I	Frequency Program Input. The filter cutoff frequency can be set by programming a current through a resistor from VPTAT to this pin. IFP should be left open when using this pin.
VBP	I	Frequency Boost Program Input. The high frequency boost is set by an external voltage applied to this pin. VBP must be proportional to voltage VPTAT. A fixed amount of boost can be set by an external resistor divider network connected from VBP to VPTAT and GND. No boost is applied if the FBST pin is grounded, or at logic low.
FBST	I	Frequency Boost. A high logic level or open enables the frequency boost circuitry. A low input disables this function.
PWRON	I	Power On. A high logic level enables the chip. A low level or open pin puts the chip in a low power state.
VPTAT	O	PTAT Reference Voltage. This pin outputs a reference voltage which is proportional to absolute temperature (PTAT). VBP, VFP or IFP must be referenced to this pin for proper operation.
VCC	O	+5 Volt Supply.
GND	I	Ground

ELECTRICAL SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Operation above maximum ratings may damage the device.

PARAMETER	RATINGS
Storage Temperature	-65°C to +150°C
Junction Operating Temperature, Tj	+130°C
Supply Voltage, VCC	-0.5V to 7V
Voltage Applied to Inputs	-0.5V to VCC

ELECTRICAL SPECIFICATIONS (continued)

RECOMMENDED OPERATING CONDITIONS

PARAMETER		RATINGS
Supply voltage	VCC	4.50V < VCC < 5.50V
Ambient Temperature	Ta	0°C < Ta < 70°C

ELECTRICAL CHARACTERISTICS

Unless otherwise specified recommended operating conditions apply.

Power Supply Characteristics

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNIT
Power Supply Current	ICC	PWRON ≤ 0.8V		0.1	0.5	mA
Power Supply Current	ICC	PWRON ≥ 2V		46	60	mA
Power Dissipation	PD	PWRON ≥ 2V, VCC = 5V		230	300	mW
		PWRON ≥ 2V, VCC = 5.5V		275	330	mW
		PWRON ≤ 0.8V		0.5	2.5	mW

DC Characteristics

High Level Input Voltage	VIH	TTL input	2			V
Low Level Input Voltage	VIL				0.8	V
High Level Input Current	IIH	VIH = 2.7V			20	µA
Low Level Input Current	IIL	VIL = 0.4V	-1.5			mA

Filter Characteristics

Filter Cutoff Frequency *(*f* -3 dB)	*fc	32F8001 $fc = \frac{45\ MHz}{mA}(IVFP)$ IVFP = 0.2 to 0.6 mA, Ta = 25 °C	9		27	MHz
		32F8002 $fc = \frac{30\ MHz}{mA}(IVFP)$ IVFP = 0.2 to 0.6 mA, Ta = 25 °C	6		18	MHz
Filter *f*c Accuracy	FCA	*f*c = max.	-12		+12	%
VO_NORM Diff Gain	AO	F = 0.67 *f*c, FB = 0 dB	0.8		1.2	V/V
VO_DIFF Diff Gain	AD	F = 0.67 *f*c, FB = 0 dB	0.8 AO		1.2 AO	V/V
Frequency Boost at *f*c	FB	VBP = VPTAT *f*c = max.	12	13.5	15	dB
		*f*c = min.	11.5	13	14.5	dB
Frequency Boost Accuracy	FBA	VBP/VPTAT = 1.0 *f*c = max.	-1.5		+1.5	dB

FILTER CHARACTERISTICS (continued)

PARAMETER	CONDITIONS		MIN	NOM	MAX	UNIT
Group Delay Variation TGDO Without Boost	f_c = max., $\frac{VBP}{VPTAT}=0$	8001	-500		+500	ps
	F = 0.2 f_c to f_c	8002	-750		+750	ps
	f_c = min., $\frac{VBP}{VPTAT}=0$	8001	-1.5		+1.5	ns
	F = 0.2 f_c to f_c	8002	-2.25		+2.25	ns
Group Delay Variation TGDO Without Boost (continued)	F = 0.2 f_c to f_c $\frac{VBP}{VPTAT}=0$		-2		2	%
	F = f_c to 1.75 f_c $\frac{VBP}{VPTAT}=0$		-4		+4	%
Group Delay Variation TGDB with Boost	f_c = max, VBP = VPTAT		-500		+500	ps
	F = 0.2 f_c to f_c		-750		+750	ps
	f_c = min., VBP = VPTAT		-1.5		+1.5	ns
	F = 0.2 to f_c		-2.25		+2.25	ns
	F = 0.2 f_c TO f_c, VBP = VPTAT		-2.5		+2.5	%
	F = f_c to 1.75 f_c, VBP = VPTAT		-4		+4	%
Filter Input Dynamic Range VIF	THD = 1% max, F = 0.67 f_c, VBP = 0V (1000 pF across Rx)		1			Vp-p
	THD = 1.7% max, F = 0.67 f_c, VBP = 0V, Normal output (1000 pF across Rx)		1.5			Vp-p
Filter Input Dynamic Range VIF	THD = 3.5% max, F = 0.67 f_c, VBP = 0V, Differentiated output (1000 pF across Rx)		1.5			Vp-p
Filter Output Dynamic Range VOF	THD = 1% max, F = 0.67 f_c $R_{LOAD} \geq 1k\Omega$ (1000 pF across Rx)		1			Vp-p
Filter Diff Input Resistance RIN			3	4.3		kΩ
Filter Input Capacitance CIN					3	pF
Output Noise Voltage EOUT	BW = 100 MHz, Rs = 50Ω	8001		3.5	5.4	mVRms
Differentiated Output	f_c = max, VBP = 0V	8002		3.3	5.2	mVRms
Output Noise Voltage EOUT	BW = 100 MHz, Rs = 50Ω	8001		2.3	3.45	mVRms
Normal Output	f_c = max, VBP = 0V	8002		2.1	3.15	mVRms
Output Noise Voltage EOUT	BW = 100 MHz, Rs = 50Ω	8001		7.7	10.75	mVRms
Differentiated Output	f_c = max, VBP = VPTAT	8002		4.8	7	mVRms
Output Noise Voltage EOUT	BW = 100 MHz, Rs = 50Ω	8001		3.8	4.75	mVRms
Normal Output	f_c = max, VBP = VPTAT	8002		2.6	3.3	mVRms

ELECTRICAL SPECIFICATIONS (continued)

FILTER CONTROL CHARACTERISTICS

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNIT
Filter Output Sink Current	IO –		1			mA
Filter Output Source Current	IO +		2			mA
Filter Output Resistance (Single ended)	RO	IO+ = 1.0 mA			60	Ω
Reference Voltage	VPTAT	Tj = 25°C		1.8		V
PTAT Voltage Input	VFP			2/3 VPTAT		V
Programming Current Range	IVFP	Ta = 25°C	0.2		0.6	mA
Programming Voltage Range	V_{VBP}		0		VPTAT	V
Voltage at pin IFP	V_{IFP}	I_{VFP} = 0 mA		2/3 VPTAT		V
Power Up Time		fc = 9 MHz			1.5	µs
		fc = 27 MHz			1	µs
Power Down Time					1	µs

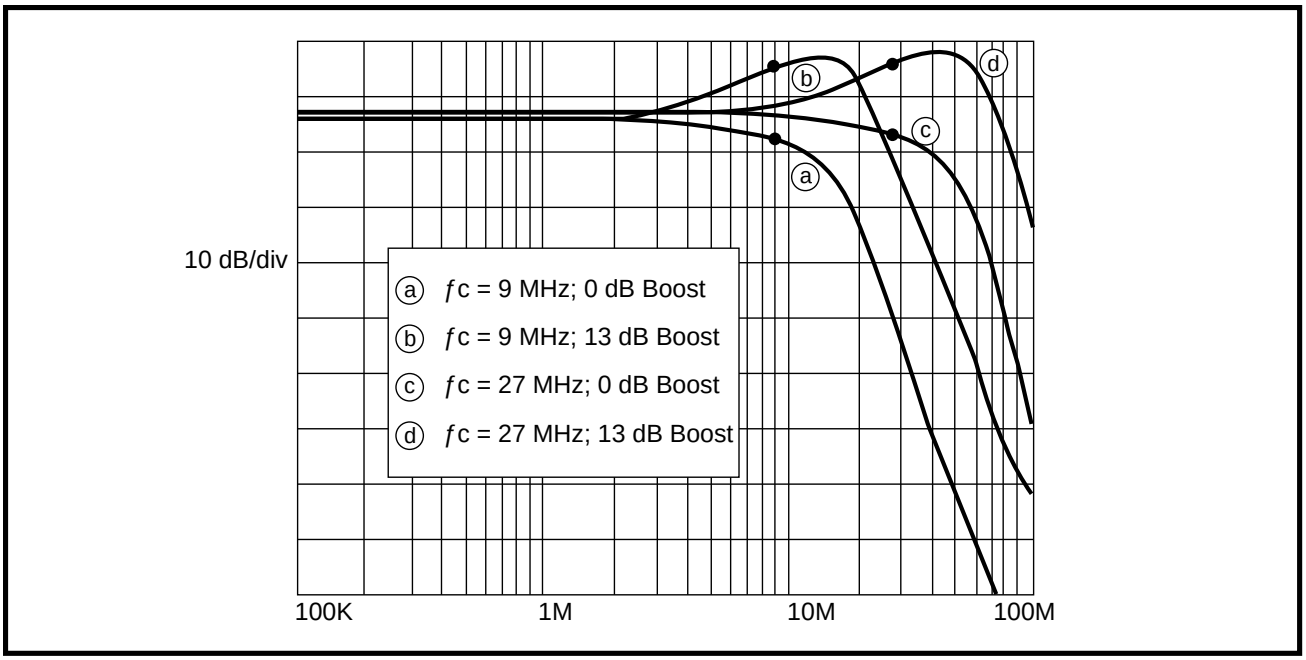


FIGURE 1: 32F8001 Normal Low Pass Response

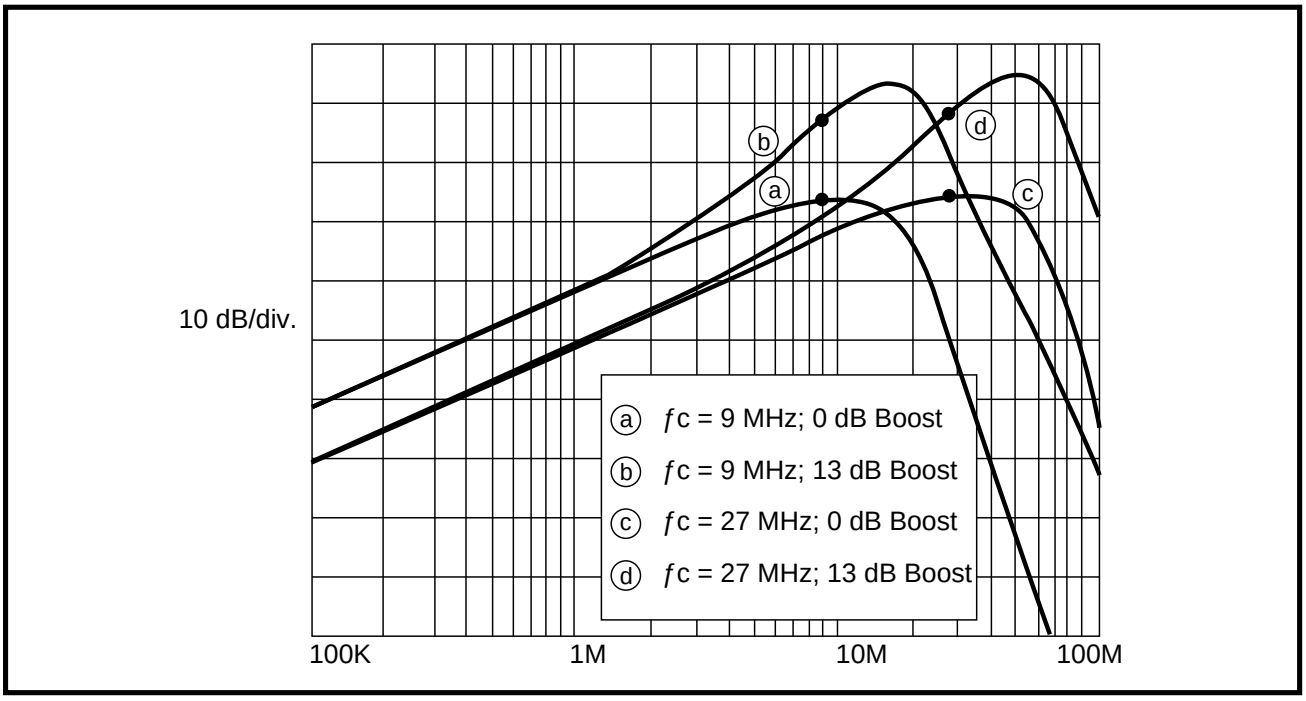


FIGURE 2: 32F8001 Differentiated Low Pass Response

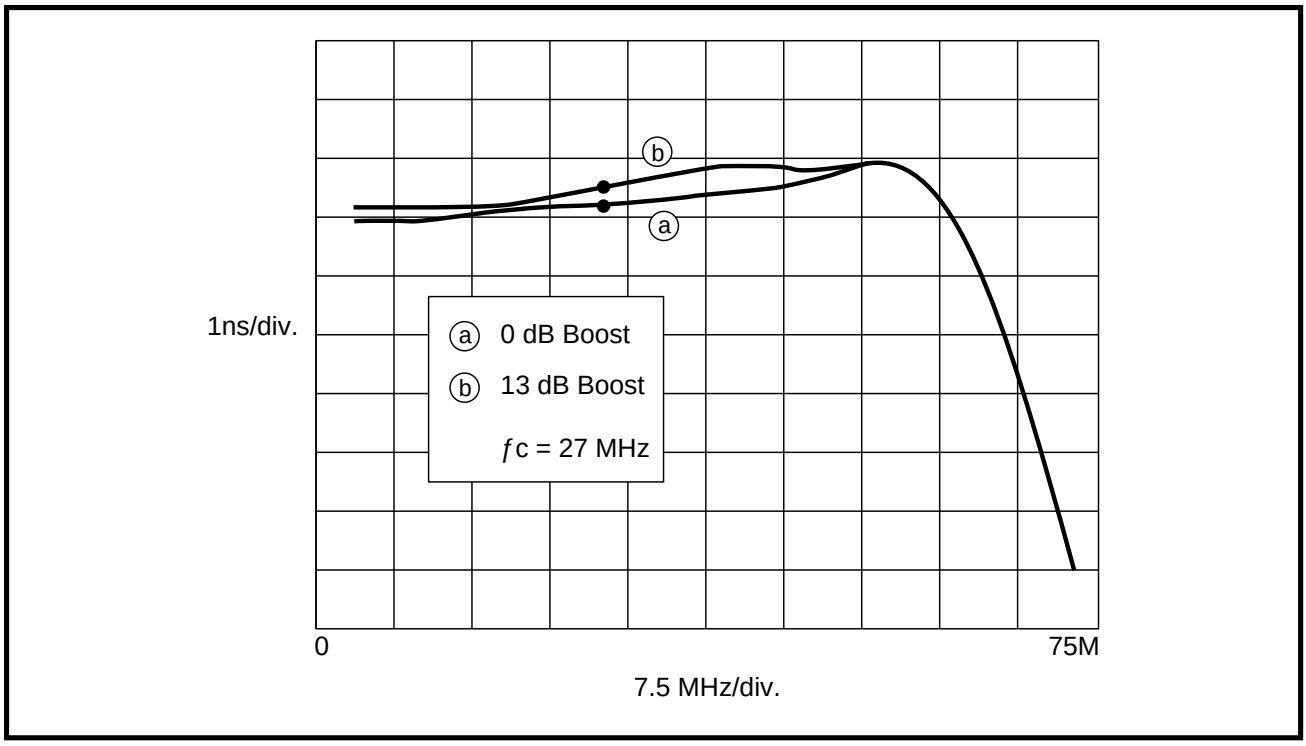
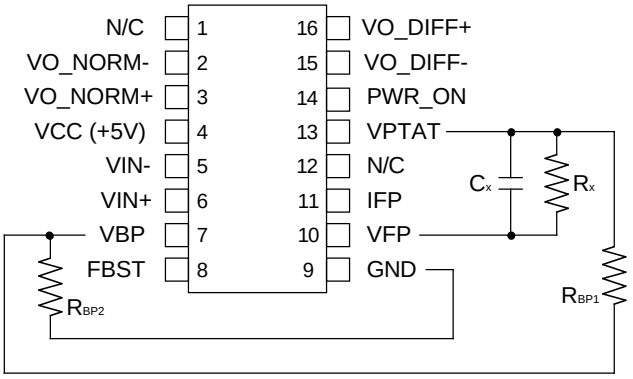


FIGURE 3: 32F8001 Group Delay Response with ƒc = 27 MHz



VPTAT = 1.8V (25°C)

V_{VFP} = 2/3 (VPTAT)

IVFP range: 0.2 mA to 0.6 mA @25°C

(9 to 27 MHz no boost 32F8001)

(6 to 18 MHz no boost 32F8002)

Fixed frequency programming is accomplished as shown in the drawing above.

In this case IVFP (programming current) is equivalent to $\frac{VPTAT}{3} \bullet \frac{1}{R_X}$

i.e., fc = 27 MHz then

IVFP = 0.6 mA @25°C Rx = 1 kΩ

Fixed boost programming is also accomplished as shown above. In this case V_{VBP} is set by a voltage divider, where V_{VBP} is a fraction of VPTAT.

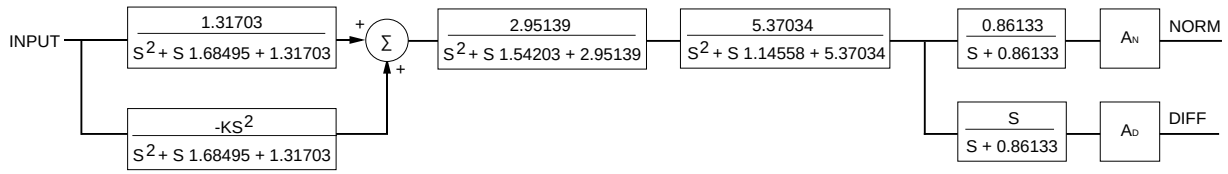
i.e., boost = 9 dB then,

VBP/VPTAT = 0.488 9 dB = 20 log [3.73 (0.488) + 1]

$$\frac{R_{BP2}}{R_{BP1}} = \frac{1}{\left(\frac{VPTAT}{VBP} - 1\right)} = 0.953$$

Cx = 1000 pF - Cx is needed for lower THD at lower fc.

FIGURE 4: 32F8001/8002 Applications Setup



Normalized for $\omega c = (2\pi)\ fc = 1$
AN and AD are adjusted for unity gain (0 dB) at $F = 0.67\ fc$
Denormalize the frequency by substituting $S \rightarrow (S/2\pi fc)$
Eq for fc = 27 MHz, $S = S / [(2\pi)(27 \times 10^6)]$

FIGURE 5: 32F8001/8002 Normalized Block Diagram

TABLE 1: 32F8001/8002 Frequency Boost Calculations, K = 1.31703 (10 BOOST (dB)/20 - 1)

Assuming 13 dB boost for VBP = VPTAT

$$\frac{VBP}{VPTAT} \cong \frac{\left(10^{(FB/20)}\right) - 1}{3.73}$$

Boost	K	VBP / VPTAT	Boost	K	VBP / VPTAT
1 dB	0.16	0.033	6 dB	1.31	0.267
2 dB	0.34	0.069	7 dB	1.63	0.332
3 dB	0.54	0.110	8 dB	1.99	0.405
4 dB	0.77	0.157	9 dB	2.40	0.488
5 dB	1.03	0.209	10 dB	2.85	0.580
			11 dB	3.36	0.683
			12 dB	3.43	0.799
			13 dB	4.57	0.929

or,

$$\text{boost in dB} = 20 \log \left[3.37 \left(\frac{VBP}{VPTAT} \right) + 1 \right]$$

VBP / VPTAT	Boost	VBP / VPTAT	Boost
0.1	2.753 dB	0.6	10.206 dB
0.2	4.841 dB	0.7	11.153 dB
0.3	6.523 dB	0.8	12.006 dB
0.4	7.391 dB	0.9	12.784 dB
0.5	9.142 dB	1.0	13.5 dB

TABLE 2: Calculations

Typical change in f-3 dB point with boost

Boost (dB)	Gain@fc (dB)	Gain@ peak (dB)	$f$peak/fc	f-3dB/fc
0	-3	0.00	no peak	1.00
1	-2	0.00	no peak	1.21
2	-1	0.00	no peak	1.51
3	0	0.15	0.70	1.80
4	1	0.99	1.05	2.04
5	2	2.15	1.23	2.20
6	3	3.41	1.33	2.33
7	4	4.68	1.38	2.43
8	5	5.94	1.43	2.51
9	6	7.18	1.46	2.59
10	7	8.40	1.48	2.66
11	8	9.59	1.51	2.73
12	9	10.77	1.51	2.80
13	10	11.92	1.53	2.87
14	11	13.06	1.53	2.93

Notes:
1. fc is the original programmed cutoff frequency with no boost
2. f-3 dB is the new -3 dB value with boost implemented
3. $f$peak is the frequency where the amplitude reaches its maximum value with boost implemented

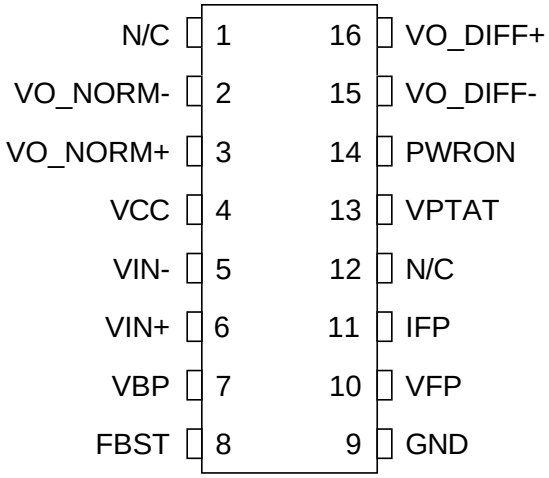
i.e., fc = 9 MHz when boost = 0 dB

if boost is programmed to 5 dB then f-3 dB = 19.8 MHz

$f$peak = 11.07 MHz

SSI 32F8001/8002
Low-Power Programmable Electronic Filter

PACKAGE PIN DESIGNATIONS
(Top View)



16-Lead SON, SOL

THERMAL CHARACTERISTICS: θja

16-Lead SON (150 mil)	105°C/W
16-Lead SOL (300 mil)	100°C/W

CAUTION: Use handling procedures necessary for a static sensitive component.

ORDERING INFORMATION

PART DESCRIPTION	ORDER NO.	PKG. MARK
SSI 32F8001		
16-Lead SOL	32F8001-CL	32F8001-CL
16-Lead SON	32F8001-CN	32F8001-CN
SSI 32F8002		
16-Lead SOL	32F8002-CL	32F8002-CL
16-Lead SON	32F8002-CN	32F8002-CN

Silicon Systems, Inc., 14351 Myford Road, Tustin, CA 92680-7022 (714) 573-6000, FAX (714) 573-6914

silicon systems®
A TDK Group Company

SSI 32F8003
Low-Power Programmable Electronic Filter

Preliminary Data

October 1994

DESCRIPTION

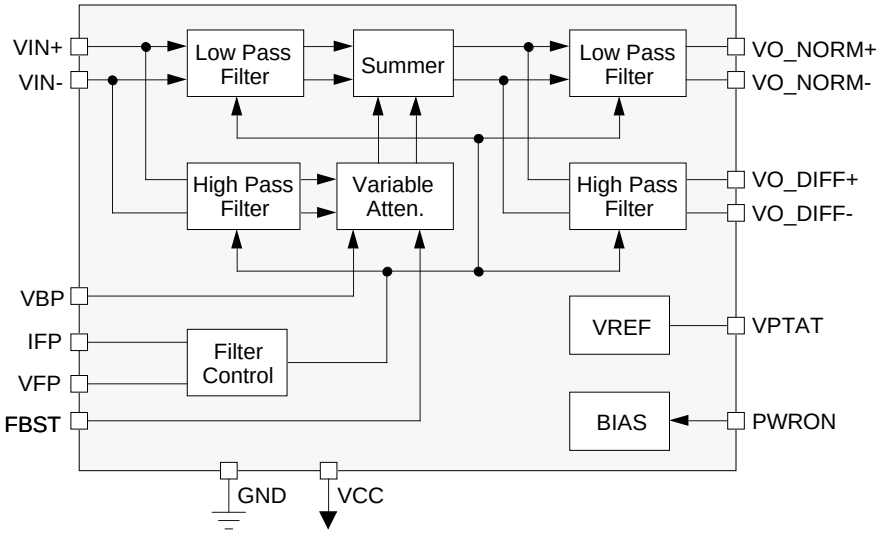
The SSI 32F8003 Programmable Electronic Filter provides an electronically controlled low–pass filter with a separate differentiated low–pass output. A seven–pole, low–pass filter is provided along with a single-pole, single-zero differentiator. Both outputs have matched delays. The delay matching is unaffected by any amount of programmed equalization or bandwidth. This programability combined with low group delay variation makes the SSI 32F8003 ideal for use in constant density recording applications. Pulse slimming equalization is accomplished by a two–pole, low–pass with a two–pole, high–pass feed forward section to provide complimentary real axis zeros. A variable attenuator is used to program the zero locations.

The SSI 32F8003 programmable equalization and bandwidth characteristics can be controlled by external DACs. Fixed characteristics are easily accomplished with three external resistors, in addition equalization can be switched in or out by a logic signal. The SSI 32F8003 requires only a +5V supply and is available in 16-lead SON and SOL packages.

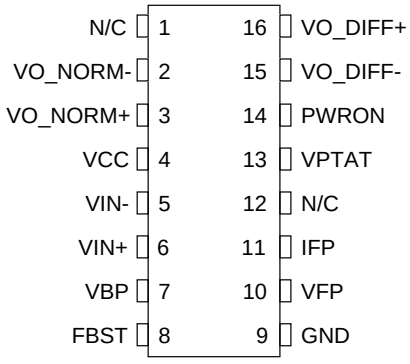
FEATURES

- **Ideal for multi-rate systems applications**
- **Programmable filter cutoff frequency f_c = 4 to 13 MHz**
- **Programmable pulse slimming equalization (0 to 13.5 dB boost at the filter cutoff frequency)**
- **Matched normal and differentiated low-pass outputs**
- **Differential filter inputs and outputs**
- **±13% cutoff frequency accuracy**
- **±2% maximum group delay variation from 0.2 f_c to f_c**
- **Total harmonic distortion less than 1%**
- **No external filter components required**
- **+5V only operation**
- **16-lead SON and SOL package**
- **Pin compatible with SSI 32F8011**

BLOCK DIAGRAM



PIN DIAGRAM



16-Lead SOL, SON

CAUTION: Use handling procedures necessary for a static sensitive component.

FUNCTIONAL DESCRIPTION

The SSI 32F8003 is a high performance programmable electronic filter. It features a 7-pole 0.05° equiripple linear phase filter with matched normal and differentiated outputs.

CUTOFF FREQUENCY PROGRAMMING

The SSI 32F8003 programmable electronic filter can be set to a filter cutoff frequency from 4 to 13 MHz with no boost.

Cutoff frequency programming can be established using either a current source fed into pin IFP whose output current is proportional to the SSI 32F8003 output reference voltage VPTAT, or by means of an external resistor tied from the output voltage reference pin VPTAT to pin VFP. The former method is optimized using the SSI 32D4661 Time Base Generator, since the current source into pin IFP is available at the DAC F output of the SSI 32D4661. Furthermore, the voltage reference input is supplied to pin VR3 of the SSI 32D4661 by the reference voltage from the VPTAT pin of the SSI 32F8003. This reference voltage is internally generated by a band-gap circuit in conjunction with a temperature varying reference to create a voltage which is proportional to absolute temperature.

The VPTAT voltage will compensate for internal temperature variation of the fc and boost circuits.

The cutoff frequency, determined by the -3dB point relative to a very low frequency value (< 10 kHz), is related to the current IVFP injected into pin IFP by the following formulas.

fc (ideal, in MHz) = 21.67 • IFP = 21.67 • IVFP • 1.8/ VPTAT

where IFP and IVFP are in mA, VPTAT is in volts, Ta = 25°C and 0.185 ≤ IFP ≤ 0.6 mA for F8003.

If a current source is used to inject current into pin IFP, pin VFP should be left open.

If the SSI 32F8003 cutoff frequency is set using voltage VPTAT to bias up a resistor tied to pin VFP, the cutoff frequency is related to the resistor value by the following formulas.

fc (ideal, in MHz) = 21.67 • IFP = 21.67 • 1.8/(3 • Rx)

Rx in kΩ

If pin VFP is used to program cutoff frequency, pin IFP should be left open.

MAGNITUDE EQUALIZATION PROGRAMMING

The magnitude equalization, measured in dB, is the amount of high frequency peaking at the cutoff frequency relative to the original -3 dB point. For example, when 12 dB boost is applied, the magnitude response peaks up 9 dB at fc above the DC gain.

The amplitude of the input signal at frequencies near the cutoff frequency can be increased using this feature. Applying an external voltage to pin VBP which is proportional to reference output voltage VPTAT (provided by the VPTAT pin) will set the amount of boost. A fixed amount of boost can be set by an external resistor divider network connected from pin VBP to pins VPTAT and GND. No boost is applied if pin FBST, frequency boost enable, is at a low logic level.

The amount of boost FB at the cutoff frequency fc is related to the voltage VBP by the formula

FB (ideal, in dB) = 20 $\log_{10}$[3.73(VBP/VPTAT)+1], where 0 < VBP < VPTAT.

POWER ON / OFF

The SSI 32F8003 supports a power down mode for minimal idle mode power dissipation. When PWRON is pulled up to TTL logic high, the device is in normal operation mode. When PWRON is pulled down to TTL logic low, or left open, the device is in the power down mode.

PIN DESCRIPTION

NAME	TYPE	DESCRIPTION
VIN+, VIN-	I	Differential Signal Inputs. The input signals must be AC coupled to these pins.
VO_NORM+, VO_NORM-	O	Differential Normal Outputs. The output signals must be AC coupled.
VO_DIFF+, VO_DIFF-	O	Differential Differentiated Outputs. For minimum time skew, these outputs should be AC coupled.
IFP	I	Frequency Program Input. The filter cutoff frequency f_c, is set by an external current IFP, injected into this pin. IFP must be proportional to voltage VPTAT. This current can be set with an external current generator such as a DAC. VFP should be left open when using this pin.
VFP	I	Frequency Program Input. The filter cutoff frequency can be set by programming a current through a resistor from VPTAT to this pin. IFP should be left open when using this pin.
VBP	I	Frequency Boost Program Input. The high frequency boost is set by an external voltage applied to this pin. VBP must be proportional to voltage VPTAT. A fixed amount of boost can be set by an external resistor divider network connected from VBP to VPTAT and GND. No boost is applied if the FBST pin is grounded, or at logic low.
FBST	I	Frequency Boost. A high logic level or open enables the frequency boost circuitry. A low input disables this function.
PWRON	I	Power On. A high logic level enables the chip. A low level or open pin puts the chip in a low power state.
VPTAT	O	PTAT Reference Voltage. This pin outputs a reference voltage which is proportional to absolute temperature (PTAT). VBP, VFP or IFP must be referenced to this pin for proper operation.
VCC	O	+5 Volt Supply.
GND	I	Ground

ELECTRICAL SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Operation above maximum ratings may damage the device.

PARAMETER	RATINGS
Storage Temperature	-65°C to +150°C
Junction Operating Temperature, Tj	+130°C
Supply Voltage, VCC	-0.5V to 7V
Voltage Applied to Inputs	-0.5V to VCC

ELECTRICAL SPECIFICATIONS (continued)

RECOMMENDED OPERATING CONDITIONS

PARAMETER		RATINGS
Supply voltage	VCC	4.50V < VCC < 5.50V
Ambient Temperature	Ta	0°C < Ta < 70°C

ELECTRICAL CHARACTERISTICS

Unless otherwise specified recommended operating conditions apply.

Power Supply Characteristics

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNIT
Power Supply Current	ICC	PWRON ≤ 0.8V		0.1	0.5	mA
Power Supply Current	ICC	PWRON ≥ 2.0V		46	60	mA
Power Dissipation	PD	PWRON ≥ 2.0V, VCC = 5.0V		230	300	mW
		PWRON ≥ 2.0V, VCC = 5.5V		275	330	mW
		PWRON ≤ 0.8V		0.5	2.5	mW

DC Characteristics

High Level Input Voltage	VIH	TTL input	2			V
Low Level Input Voltage	VIL				0.8	V
High Level Input Current	IIH	VIH = 2.7V			20	µA
Low Level Input Current	IIL	VIL = 0.4V	-1.5			mA

Filter Characteristics

Filter Cutoff Frequency *(ƒ -3dB)	*ƒc	$ƒc = \frac{21.67\ MHz}{mA}(IVFP)$	4		13	MHz
Filter ƒc Accuracy	FCA	ƒc = max.	-13		+13	%
VO_NORM Diff Gain	AO	F = 0.67 ƒc, FB = 0 dB	0.8		1.2	V/V
VO_DIFF Diff Gain	AD	F = 0.67 ƒc, FB = 0 dB	0.8AO		1.2AO	V/V
Frequency Boost at ƒc	FB	VBP = VPTAT ƒc = max.	12	13.5	15	dB
		ƒc = min.	11.5	13	14.5	dB
Frequency Boost Accuracy	FBA	VBP/VPTAT = 1.0 ƒc = max.	-1.5		1.5	dB

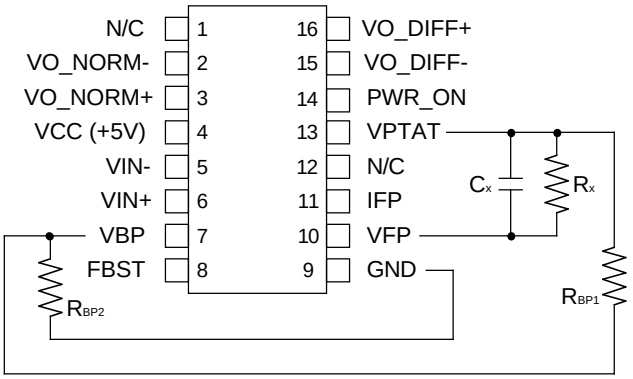
FILTER CHARACTERISTICS (continued)

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
Group Delay Variation TGDO Without Boost (continued)	f_c = max, F = 0.2 f_c to f_c, $\frac{VBP}{VPTAT}=0$	-1		+1	ns
	f_c = min, F = 0.2 f_c to f_c, $\frac{VBP}{VPTAT}=0$	-3		+3	ns
	F = 0.2 f_c to f_c, $\frac{VBP}{VPTAT}=0$	-2		+2	%
	F = f_c to 1.75 f_c $\frac{VBP}{VPTAT}=0$	-3		+3	%
Group Delay Variation TGDB With Boost	f_c = max, VBP = VPTAT, F = 0.2 f_c to f_c	-1		+1	ns
	f_c = min, VBP = VPTAT, F = 0.2 to f_c	-3		+3	ns
	F = 0.2 f_C TO f_C, VBP = VPTAT	-2		+2	%
	F = f_c to 1.75 f_c, VBP = VPTAT	-3		+3	%
Filter Input Dynamic Range VIF	THD = 1% max, F = 0.67 f_c, VBP = 0V (1000 pF across Rx)	1			Vp-p
	THD = 1.5% max, F = 0.67 f_c, VBP = 0V, Normal output (1000 pF across Rx)	1.5			Vp-p
Filter Input Dynamic Range VIF	THD = 2.0% max, F = 0.67 f_c, VBP = 0V, Differentiated output (1000 pF across Rx)	1.5			Vp-p
Filter Diff Input Resistance RIN		3	4.3		kΩ
Filter Input Capacitance CIN				7	pF
Output Noise Voltage EOUT Differentiated Output	BW = 100 MHz, Rs = 50Ω, f_c = max, VBP = 0V		3		mV rms

ELECTRICAL SPECIFICATIONS (continued)

FILTER CONTROL CHARACTERISTICS

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNIT
Output Noise Voltage Normal Output	EOUT	BW = 100 MHz, Rs = 50Ω fc = max, VBP = 0V		1.8		mV rms
Output Noise Voltage Differentiated Output	EOUT	BW = 100 MHz, Rs = 50Ω fc = max, VBP = VPTAT		4.3		mV rms
Output Noise Voltage Normal Output	EOUT	BW = 100 MHz, Rs = 50Ω fc = max, VBP = VPTAT		2.2		mV rms
Filter Output Sink Current	IO –		1			mA
Filter Output Source Current	IO +		2			mA
Filter Output Resistance (Single ended)	RO	IO+ = 1.0 mA			60	Ω
Reference Voltage	VPTAT	Tj = 25°C		1.8		V
PTAT Voltage Input	VFP			2/3 VPTAT		V
Programming Current Range	IVFP	Ta = 25°C	0.185		0.6	mA
Programming Voltage Range	V_{VBP}		0		VPTAT	V
Voltage at pin IFP	V_{IFP}	I_{VFP} = 0 mA		2/3 VPTAT		V
Power Up Time		fc = min			1.5	µs
		fc = max			1	µs
Power Down Time					1	µs



VPTAT = 1.8V (25°C)

V_{VFP} = 2/3 (VPTAT)

IVFP range: 0.185 mA to 0.6 mA @25°C

Fixed frequency programming is accomplished as shown in the drawing above.

In this case IVFP (programming current) is equivalent to $\frac{VPTAT}{3} \cdot \frac{1}{R_X}$

i.e., fc = 13 MHz then

IVFP = 0.6 mA @25°C Rx = 1 kΩ

Fixed boost programming is also accomplished as shown above. In this case V_{VBP} is set by a voltage divider, where V_{VBP} is a fraction of VPTAT.

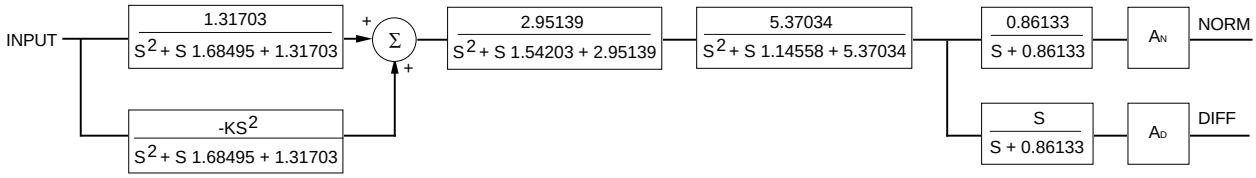
i.e., boost = 9 dB then,

VBP/VPTAT = 0.488 9 dB = 20 log [3.73 (0.488) + 1]

$$\frac{R_{BP2}}{R_{BP1}} = \frac{1}{\left(\frac{VPTAT}{VBP} - 1\right)} = 0.953$$

Cx = 1000 pF - Cx is needed for lower THD at lower fc.

FIGURE 4: 32F8003 Applications Setup



Normalized for $\omega c = (2\pi)\ fc = 1$
AN and AD are adjusted for unity gain (0 dB) at $F = 0.67\ fc$
Denormalize the frequency by substituting $S \rightarrow (S/2\pi fc)$
Eq for fc = 27 MHz, $S = S / [(2\pi)(27 \times 10^6)]$

FIGURE 5: 32F8003 Normalized Block Diagram

TABLE 1: 32F8003 Frequency Boost Calculations, K = 1.31703 ($10^{\text{BOOST (dB)/20}} - 1$)

Assuming 13.5 dB boost for VBP = VPTAT

$$\frac{VBP}{VPTAT} \cong \frac{(10^{(FB/20)}) - 1}{3.73}$$

Boost	K	VBP / VPTAT	Boost	K	VBP / VPTAT
1 dB	0.16	0.033	6 dB	1.31	0.267
2 dB	0.34	0.069	7 dB	1.63	0.332
3 dB	0.54	0.110	8 dB	1.99	0.405
4 dB	0.77	0.157	9 dB	2.40	0.488
5 dB	1.03	0.209	10 dB	2.85	0.580
			11 dB	3.36	0.683
			12 dB	3.43	0.799
			13 dB	4.57	0.929

or,

$$\text{boost in dB} = 20\log\left[3.73\left(\frac{VBP}{VPTAT}\right) + 1\right]$$

VBP / VPTAT	Boost	VBP / VPTAT	Boost
0.1	2.753 dB	0.6	10.206 dB
0.2	4.841 dB	0.7	11.153 dB
0.3	6.523 dB	0.8	12.006 dB
0.4	7.391 dB	0.9	12.784 dB
0.5	9.142 dB	1.0	13.5 dB

TABLE 2: Calculations

Typical change in f-3 dB point with boost

Boost (dB)	Gain@fc (dB)	Gain@ peak (dB)	$f$peak/fc	f-3dB/fc
0	-3	0.00	no peak	1.00
1	-2	0.00	no peak	1.21
2	-1	0.00	no peak	1.51
3	0	0.15	0.70	1.80
4	1	0.99	1.05	2.04
5	2	2.15	1.23	2.20
6	3	3.41	1.33	2.33
7	4	4.68	1.38	2.43
8	5	5.94	1.43	2.51
9	6	7.18	1.46	2.59
10	7	8.40	1.48	2.66
11	8	9.59	1.51	2.73
12	9	10.77	1.51	2.80
13	10	11.92	1.53	2.87
14	11	13.06	1.53	2.93

Notes:
1. fc is the original programmed cutoff frequency with no boost
2. f-3 dB is the new -3 dB value with boost implemented
3. $f$peak is the frequency where the amplitude reaches its maximum value with boost implemented

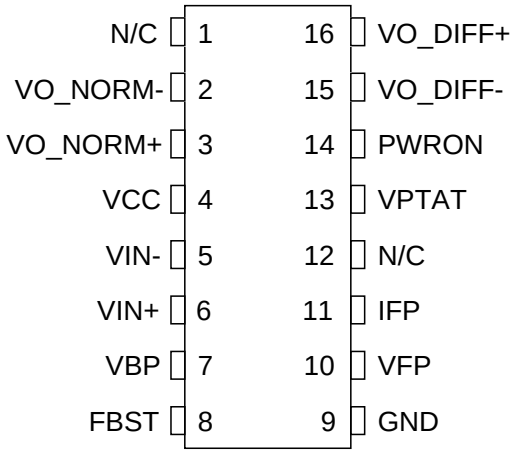
i.e., fc = 9 MHz when boost = 0 dB

if boost is programmed to 5 dB then f-3 dB = 19.8 MHz

$f$peak = 11.07 MHz

SSI 32F8003
Low-Power Programmable Electronic Filter

PACKAGE PIN DESIGNATIONS
(Top View)



16-Lead SON, SOL

CAUTION: Use handling procedures necessary for a static sensitive component.

THERMAL CHARACTERISTICS: θja

16-lead SON (150 mil)	105°C/W
16-lead SOL (300 mil)	100°C/W

ORDERING INFORMATION

PART DESCRIPTION		ORDER NUMBER	PACKAGE MARK
SSI 32F8003	16-Lead SOL	32F8003-CL	32F8003-CL
	16-Lead SON	32F8003-CN	32F8003-CN

Preliminary Data: Indicates a product not completely released to production. The specifications are based on preliminary evaluations and are not guaranteed. Small quantities are available, and Silicon Systems should be consulted for current information.

Silicon Systems, Inc., 14351 Myford Road, Tustin, CA 92680-7022 (714) 573-6000, FAX (714) 573-6914

silicon systems®
A TDK Group Company

SSI 32F8030
Programmable Electronic Filter

December 1993

DESCRIPTION

The SSI 32F8030 Programmable Electronic Filter provides an electronically controlled low–pass filter with a separate differentiated low–pass output. A seven–pole, 0.05° Equiripple-type linear phase, low–pass filter is provided along with a single-pole, single-zero differentiator. Both outputs have matched delays. The delay matching is unaffected by any amount of programmed high frequency peaking (boost) or bandwidth. This programability, combined with low group delay variation makes the SSI 32F8030 ideal for use in many applications. Double differentiation high frequency boost is accomplished by a two–pole, low–pass with a two–pole, high–pass feed forward section to provide complementary real axis zeros. A variable attenuator is used to program the zero locations, which controls the amount of boost.

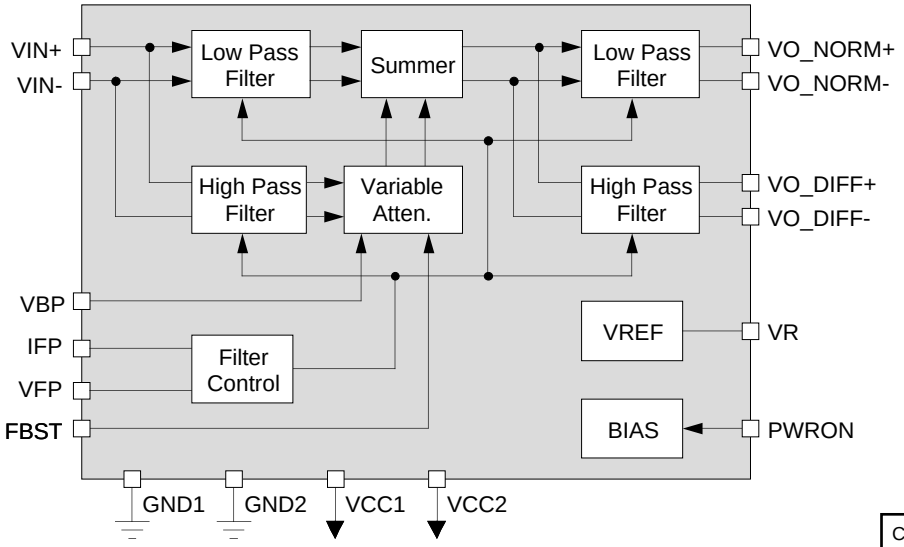
The SSI 32F8030 programmable boost and bandwidth characteristics can be controlled by external DACs or DACs provided in the SSI 32D4661 Time Base Generator. Fixed characteristics are easily accomplished with three external resistors. In addition, boost can be switched in or out by a logic signal.

The SSI 32F8030 requires only a +5V supply and is available in 16-Lead SON, and SOL packages.

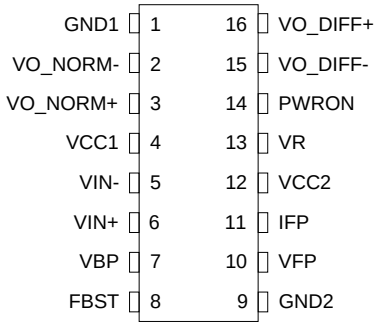
FEATURES

- **Ideal for:**
  - **constant density recording applications**
  - **magnetic tape recording**
- **Programmable filter cutoff frequency (fc = 250 kHz to 2.5 MHz)**
- **Programmable high frequency peaking (0 to 9 dB boost at the filter cutoff frequency)**
- **Matched normal and differentiated low-pass outputs**
- **Differential filter input and outputs**
- **±3.0% group delay variation from 0.2 fc to 1.75 fc, 0.25 MHz ≤ fc ≤ 2.5 MHz**
- **Total harmonic distortion less than 1%**
- **+5V only operation**
- **16-Lead SON, and SOL packages**
- **5 mW idle mode**

BLOCK DIAGRAM



PIN DIAGRAM



CAUTION: Use handling procedures necessary for a static sensitive component.

FUNCTIONAL DESCRIPTION

The SSI 32F8030, a high performance programmable electronic filter, provides a low pass 0.05° Equiripple-type linear phase seven pole filter with matched normal and differentiated outputs. The device has been optimized for usage with several Silicon Systems products, including the SSI 32D4661 Time Base Generator, the SSI 32P54x family of Pulse Detectors, and the SSI 32P4720 Combo device (Data Separator and Pulse Detector).

CUTOFF FREQUENCY PROGRAMMING

The SSI 32F8030 programmable electronic filter can be set to a filter cutoff frequency from 250 kHz to 2.5 MHz (with no boost).

Cutoff frequency programming can be established using either a current source fed into the IFP pin, whose output current is proportional to the SSI 32F8030 output reference voltage VR, or by means of an external resistor tied from the output voltage reference pin VR to pin VFP. The former method is optimized using the SSI 32D4661 Time Base Generator, since the current source into pin IFP is available at the DAC F output of the 32D4661. Furthermore, the voltage reference input is supplied to pin VR3 of the 32D4661 by the reference voltage VR from the VR pin of the 32F8030. This reference voltage is an internally generated bandgap reference, which typically varies less than 1 % over voltage supply and temperature variation. (For the calculations below IVFP = current into IFP or VFP pins).

The cutoff frequency, determined by the -3dB point relative to a very low frequency value (< 10kHz), is related to the current IVFP injected into pin IFP by the formula

Fc (ideal, in MHz) = 3.125•IFP = 3.125•IVFP•2.2/VR, where IFP and IVFP are in mA, 0.08<IFP<0.8 mA, and VR is in volts.

If a current source is used to inject current into pin IFP, pin VFP should be left open.

If the 32F8030 cutoff frequency is set using voltage VR to bias up a resistor tied to pin VFP, the cutoff frequency is related to the resistor value by the formula

Fc (ideal, in MHz) = 3.125•IFP = 3.125•2.2/(3•Rx) where Rx is in kΩ, & 0.917 kΩ <Rx<9.17 kΩ.

If pin VFP is used to program cutoff frequency, pin IFP should be left open.

SLIMMER HIGH FREQUENCY BOOST PROGRAMMING

The amplitude of the output signal at frequencies near the cutoff frequency can be increased using this feature. Applying an external voltage to pin VBP which is proportional to reference output voltage VR (provided by the VR pin) will set the amount of boost. A fixed amount of boost can be set by an external resistor divider network connected from pin VBP to pins VR and GND. No boost is applied if pin FBST, frequency boost enable, is at a low logic level.

The amount of boost FB at the cutoff frequency Fc is related to the voltage VBP by the formula

FB (ideal, in dB) = $20 \log_{10}[1.884(VBP/VR)+1]$, where 0<VBP<VR.

PIN DESCRIPTION

NAME	DESCRIPTION
VIN+, VIN-	DIFFERENTIAL SIGNAL INPUTS. The input signals must be AC coupled to these pins.
VO_NORM+, VO_NORM-	DIFFERENTIAL NORMAL OUTPUTS. The output signals must be AC coupled.
VO_DIFF+, VO_DIFF-	DIFFERENTIAL DIFFERENTIATED OUTPUTS. For minimum time skew, these outputs should be AC coupled to the pulse detector.
IFP	FREQUENCY PROGRAM INPUT. The filter cutoff frequency FC, is set by an external current IFP, injected into this pin. IFP must be proportional to voltage VR. This current can be set with an external current generator such as a DAC. VFP should be left open when using this pin.
VFP	FREQUENCY PROGRAM INPUT. The filter cutoff frequency can be set by programming a current through a resistor from VR to this pin. IFP should be left open when using this pin.
VBP	FREQUENCY BOOST PROGRAM INPUT. The high frequency boost is set by an external voltage applied to this pin. VBP must be proportional to voltage VR. A fixed amount of boost can be set by an external resistor divider network connected from VBP to VR and GND. No boost is applied if the FBST pin is grounded, or at logic low.
FBST	FREQUENCY BOOST. A high logic level or open input enables the frequency boost circuitry.
PWRON	POWER ON. A high logic level enables the chip. A low level puts the chip in a low power state.
VR	REFERENCE VOLTAGE. Internally generated reference voltage.
VCC1, VCC2	+5 VOLT SUPPLY.
GND1, GND2	GROUND

ELECTRICAL SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Operation above maximum ratings may damage the device.

PARAMETER	RATING
Storage Temperature	-65 to +150°C
Junction Operating Temperature, Tj	+130°C
Supply Voltage, VCC1, VCC2	-0.5 to 7V
Voltage Applied to Inputs	-0.5 to VCC + 0.5V
IFP, VFP Inputs Maximum Current	≤1.2 mA

RECOMMENDED OPERATING CONDITIONS

PARAMETER	RATING
Supply voltage, VCC1, VCC2	4.5 < VCC1,2 < 5.50V
Ambient Temperature	0 < Ta < 70°C

ELECTRICAL SPECIFICATIONS

Power Supply Characteristics

Unless otherwise specified, recommended operating conditions apply.

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNIT
ICC	Power Supply Current	PWRON ≤ 0.8V			0.5	mA
ICC	Power Supply Current	PWRON ≥ 2.0V		28	42	mA
PD	Power Dissipation	PWRON ≥ 2.0V		140	231	mW
PD	Power Dissipation	PWRON ≤ 0.8V			3	mW

DC Characteristics

VIH	High Level Input Voltage	TTL input	2.0		VCC+0.3	V
VIL	Low Level Input Voltage		-0.3		0.8	V
IIH	High Level Input Current	VIH = 2.7V			20	μA
IIL	Low Level Input Current	VIL = 0.4V	–1.5			mA

Filter Characteristics

fc = 1.25 MHz unless otherwise stated

FCA	Filter fc Accuracy	using IFP pin: IFP = 0.4 mA or using VFP pin: Rx = 1.84 kΩ	1.125		1.375	MHz
AO	VO_NORM Diff Gain	F = 0.67 fc, FB = 0 dB	0.8		1.20	V/V
AD	VO_DIFF Diff Gain	F = 0.67 fc, FB = 0 dB	0.9AO		1.1AO	V/V
FBA	Frequency Boost Accuracy	VBP = VR	8.0	9.2	10.4	dB
TGD0	Group Delay Variation Without Boost*	0.25 MHz ≤ fc ≤ 2.5 MHz F = 0.2 fc to 1.75 fc	–3		+3	%
TGDB	Group Delay Variation With Boost*	0.25 MHz ≤ fc ≤ 2.5 MHz VBP = VR, F = 0.2 fc to 1.75 fc	–3		+3	%
VIF	Filter Input Dynamic Range	THD = 1% max, F = 0.67 fc (no boost, 1000 pF capacitor across Rx)	1.0			Vpp
VOF	Filter Normal Output Dynamic Range	THD = 1% max, F = 0.67 fc VBP = 0 (1000 pF capacitor across Rx)	1.0			Vpp
VOF	Filter Normal Output Dynamic Range	THD = 1% max, F = 0.67 fc VBP = VR (1000 pF capacitor across Rx)	1.0			Vpp
VOF	Filter Differentiated Output Dynamic Range	THD = 1% max, F = 0.67 fc VBP = 0 (1000 pF capacitor across Rx)	1.0			Vpp
VOF	Filter Differentiated Output Dynamic Range	THD = 1% max, F = 0.67 fc VBP = VR (1000 pF capacitor across Rx)	1.0			Vpp

Filter Characteristics (continued)

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
RIN Filter Diff Input Resistance		3.0	4.0	5.0	kΩ
CIN Filter Diff Input Capacitance*			3.0		pF
EOUT Output Noise Voltage* Differentiated Output	BW = 100 MHz, Rs = 50Ω, Ifp = 0.8 mA, VBP = 0.0V		2.7	3.2	mVRms
EOUT Output Noise Voltage* Normal Output	BW = 100 MHz, Rs = 50Ω Ifp = 0.8 mA, VBP = 0.0V		1.6	2.0	mVRms
EOUT Output Noise Voltage* Differentiated Output	BW = 100 MHz, Rs = 50Ω Ifp = 0.8 mA, VBP = VR		3.1	3.8	mVRms
EOUT Output Noise Voltage* Normal Output	BW = 100 MHz, Rs = 50Ω Ifp = 0.8 mA, VBP = VR		1.8	2.2	mVRms
EOUT Output Noise Voltage* Differentiated Output	BW = 10 MHz, Rs = 50Ω, Ifp = 0.08 mA, VBP = 0.0V		1.8	2.1	mVRms
EOUT Output Noise Voltage* Normal Output	BW = 10 MHz, Rs = 50Ω Ifp = 0.08 mA, VBP = 0.0V		1.0	1.2	mVRms
EOUT Output Noise Voltage* Differentiated Output	BW = 10 MHz, Rs = 50Ω Ifp = 0.08 mA, VBP = VR		2.0	2.5	mVRms
EOUT Output Noise Voltage* Normal Output	BW = 10 MHz, Rs = 50Ω Ifp = 0.08 mA, VBP = VR		1.1	1.5	mVRms
IO- Filter Output Sink Current		1.0			mA
IO+ Filter Output Source Current		2.0			mA
RO Filter Output Resistance**	Sinking 1 mA from pin			70	Ω
* Not directly testable in production, design characteristic. ** Single ended					

Filter Control Characteristics

VR Reference Voltage Output		2.0		2.40	V
I_{VR} Reference Output Source Current				2.0	mA

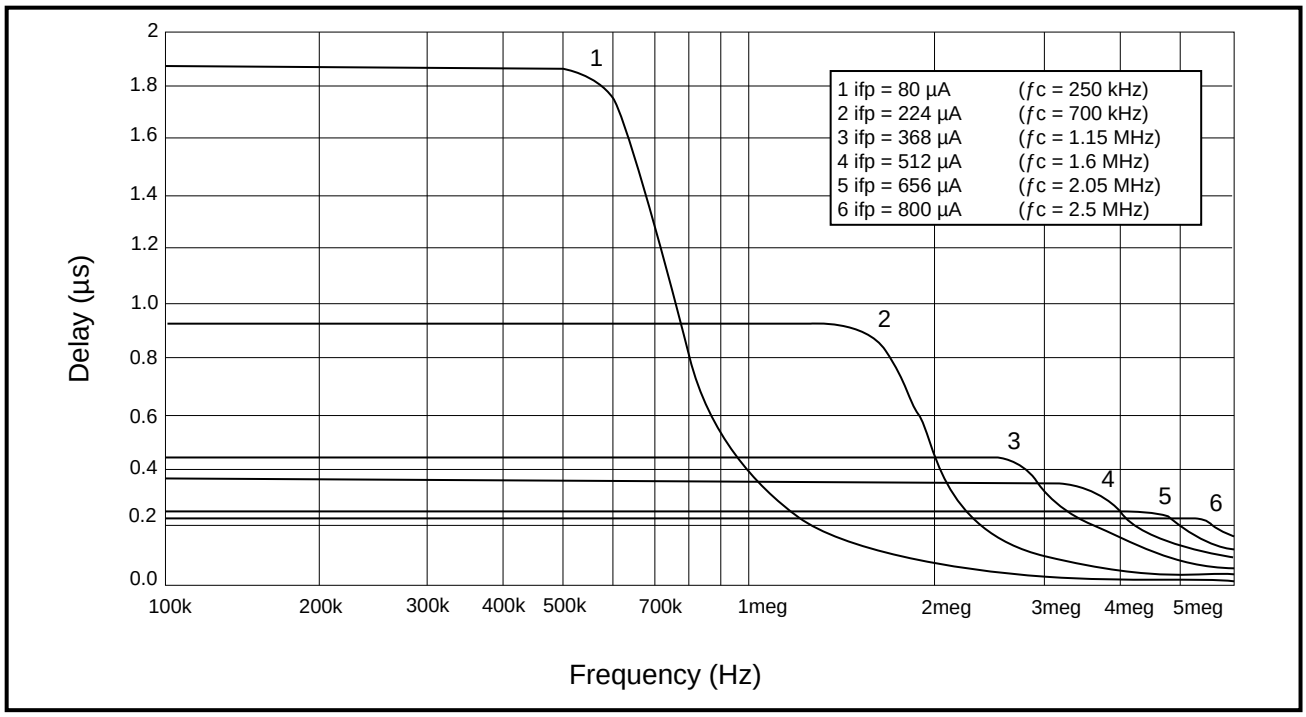


FIGURE 1: Typical Normal/Differentiated Output Group Delay Response

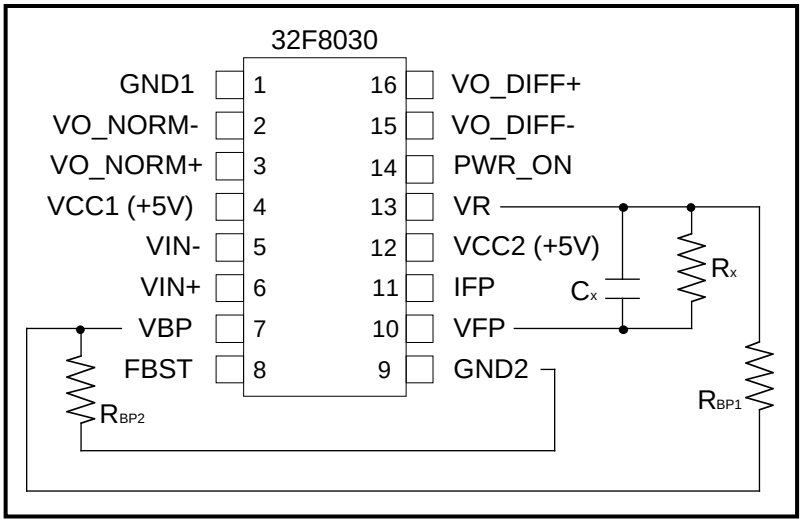


FIGURE 1: 32F8030 Applications Setup 16-Pin SO

VR = 2.2V

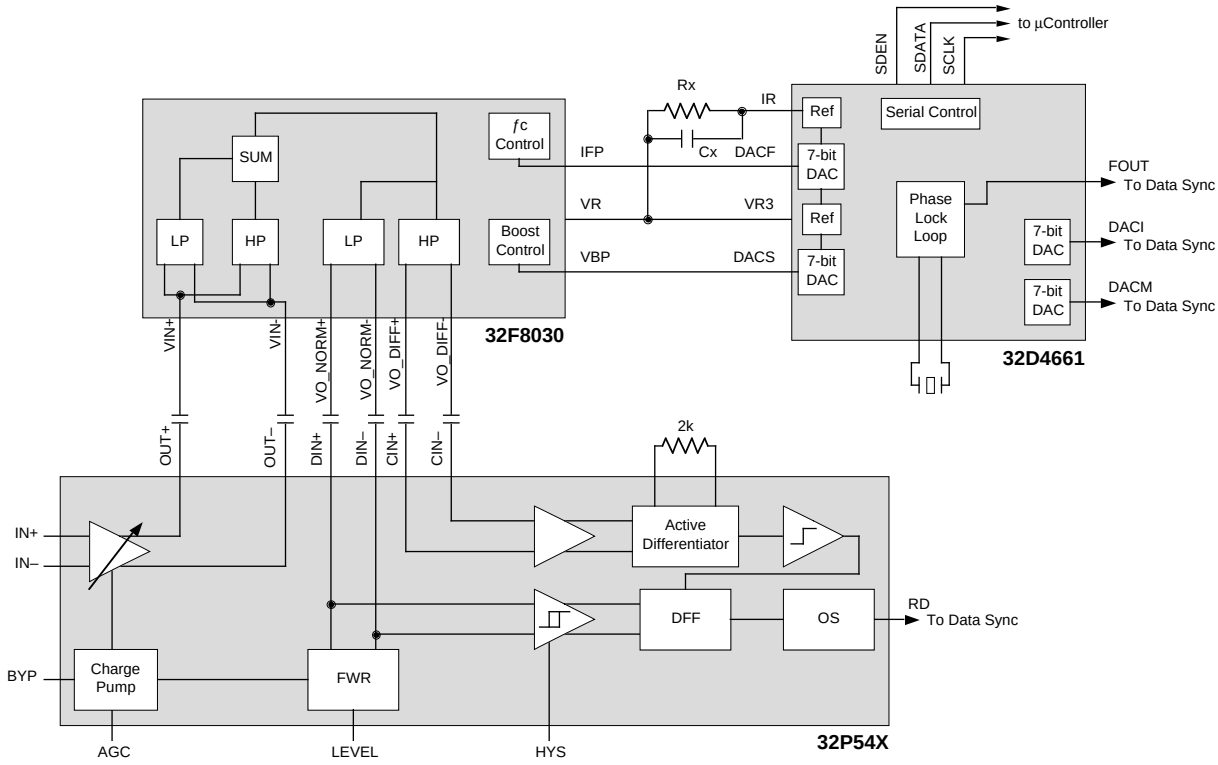
VFP = .667 VR

IVfp = .33VR/Rx

IVfp range: 0.08 mA to 0.8 mA
(0.25 MHz to 2.5 MHz)

Cx = 1000 pF needed for THD at low ƒc

VFP is used when programming current is set with a resistor from VR.
When VFP is used IFP must be left open.



IOF = DACF output current

IOF = (0.98F•VR)/127Rx

Rx = (0.98F•VR)/127IOF

Rx = current reference setting resistor

VR = Voltage Reference = 2.2V

F = DAC setting: 0-127

Full scale, F = 127

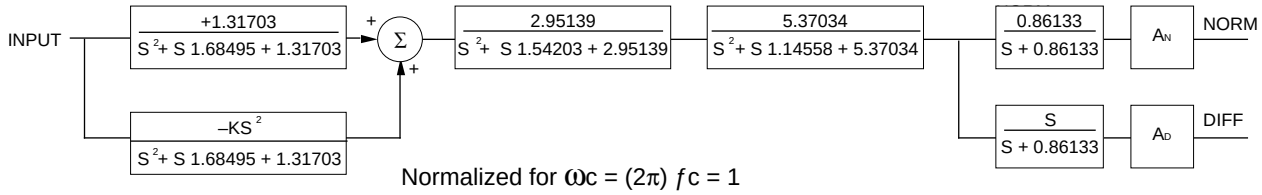
For range of Max fc = 2.5 MHz then IFP = 0.8 mA

Therefore, for Max programming current range to 0.8 mA:

Rx = (0.98)(2.2/0.8) = 2.7 kΩ

Please note that in setups such as this where IFP is used for cutoff frequency programming VFP must be left open.

FIGURE 2: Applications Setup, Constant Density Recording
32F8030, 32P54X, 32D4661



Normalized for ωc = (2π) fc = 1

AN and AD are adjusted for unity gain (0 dB) at F = 0.67 fc

Denormalize the frequency by substituting S → (S/2πfc)

Eq for fc = 2.5 MHz, S = S / [(2π)(2.5•10⁶)] = S / (1.57080 • 10⁷)

FIGURE 3: 32F8030 Normalized Block Diagram

TABLE 1: 32F8030 Frequency Boost Calculations - K = 1.31703 ($10^{BOOST\ (dB)\ /\ 20}$ -1)

Assuming 9.2 dB boost for VBP = VR

$$\frac{VBP}{VR} \cong \frac{\left(10^{(FB/20)}\right)-1}{1.884}$$

Boost	K	VBP/VR	Boost	K	VBP/VR
1 dB	0.16	0.065	6 dB	1.31	0.288
2 dB	0.34	0.137	7 dB	1.63	0.358
3 dB	0.54	0.219	8 dB	1.99	0.437
4 dB	0.77	0.310	9 dB	2.40	0.526
5 dB	1.03	0.413			

or,

$$\text{boost in dB} = 20\log\left[1.884\left(\frac{VBP}{VR}\right)+1\right]$$

VBP/VR	Boost	VBP/VR	Boost
0.1	1.499 dB	0.6	6.569 dB
0.2	2.777 dB	0.7	7.305 dB
0.3	3.891 dB	0.8	7.984 dB
0.4	4.879 dB	0.9	8.613 dB
0.5	5.765 dB	1.0	9.200 dB

TABLE 2: Calculations

Typical change in f-3 dB point with boost

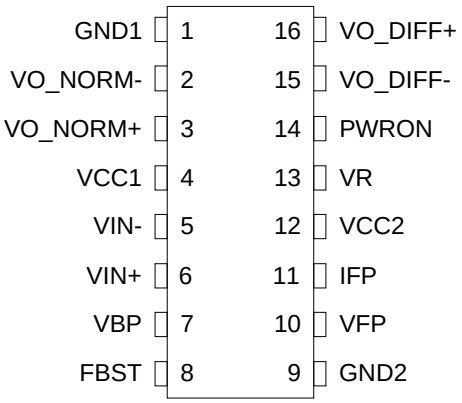
Boost (dB)	Gain @ fc(dB)	Gain @ peak(dB)	$f$peak/fc	f-3 dB/fc
0	-3	0.00	no peak	1.00
1	-2	0.00	no peak	1.21
2	-1	0.00	no peak	1.51
3	0	0.15	0.70	1.80
4	1	0.99	1.05	2.04
5	2	2.15	1.23	2.20
6	3	3.41	1.33	2.33
7	4	4.68	1.38	2.43
8	5	5.94	1.43	2.51
9	6	7.18	1.46	2.59

Notes: 1. fc is the original programmed cutoff frequency with no boost
2. f-3 dB is the new -3 dB value with boost implemented
3. $f$peak is the frequency where the magnitude peaks with boost implemented

i.e., fc = 2.5 MHz when boost = 0 dB
if boost is programmed to 5 dB then f-3 dB = 5.5 MHz
$f$peak = 3.075 MHz

PACKAGE PIN DESIGNATIONS

(Top View)



16-Lead SON, SOL

Thermal Characteristics: θjA

16-lead SON (150 mil)	105° C/W
16-lead SOL (300 mil)	100° C/W

CAUTION: Use handling procedures necessary for a static sensitive component.

ORDERING INFORMATION

PART DESCRIPTION	ORDER NUMBER	PACKAGE MARK
16-lead SON (150 mil)	32F8030-CN	32F8030-CN
16-lead SOL (300 mil)	32F8030-CL	32F8030-CN

Silicon Systems, Inc., 14351 Myford Road, Tustin, CA 92680-7022 (714) 573-6000, FAX (714) 573-6914

SSI 32F8101
Low-Power Programmable Filter

January 1996

DESCRIPTION

The SSI 32F8101 is a high performance, low power, digitally programmable low-pass filter for applications requiring variable-frequency filtering. The device consists of three functional blocks: [1] a 7th-order 0.05° Equiripple Low-Pass filter, [2] two DACs for controlling the filter cutoff frequency and high-frequency peaking (boost), and [3] a Serial Port for programming the f_c and Boost DACs.

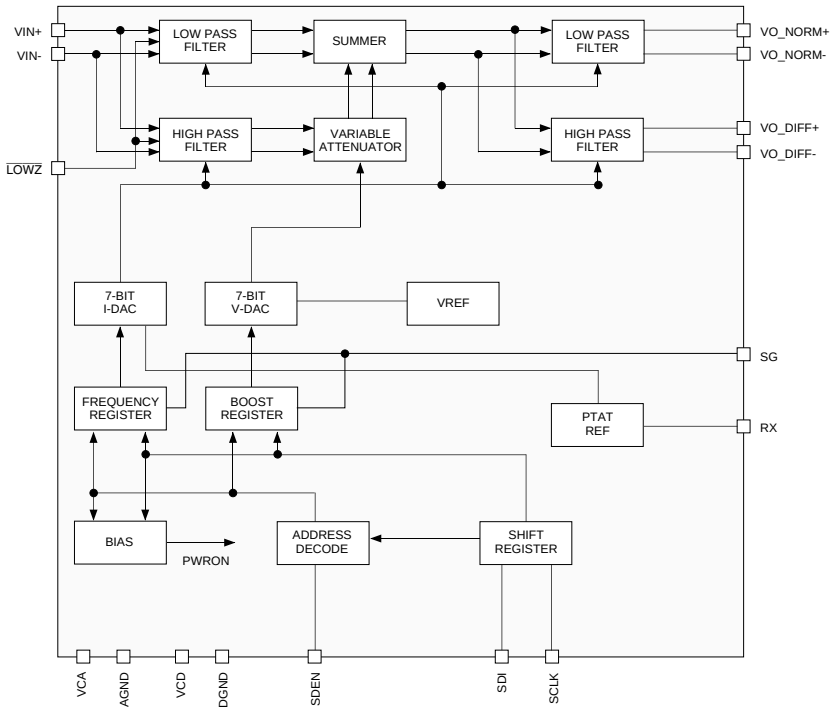
Cutoff frequency and boost are controlled by the two on-chip 7-bit DACs, which are programmed via the 3-line serial interface. Boost is programmable from 0 to 14.6 dB nominally at maximum f_c, and is implemented using two symmetrical, real-axis zeroes. Both boost and f_c control do not affect the flat group delay response.

The SSI 32F8101 device is ideal for variable data rate and variable frequency shaping applications. It requires only a +5V supply and has an idle mode for minimal power dissipation. The SSI 32F8101 is available in a 16-lead SON package.

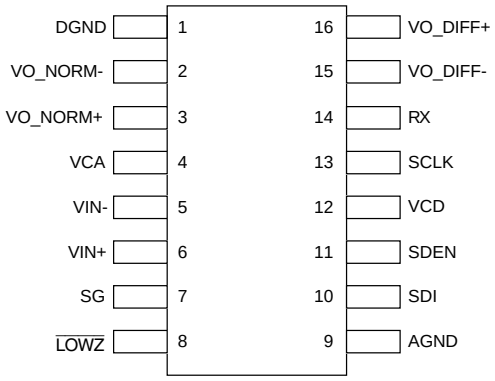
FEATURES

- **Programmable cutoff frequency 8.4 to 30 MHz**
- **Programmable boost/equalization of 0 to 14.6 dB**
- **Matched normal and differentiated outputs**
- **±15% f_c accuracy**
- **±2% maximum group delay variation**
- **Less than 1.5% total harmonic distortion**
- **Low-Z input switch controlled by $\overline{\text{LOWZ}}$ pin**
- **No external filter components required**
- **95 mW nominal power, <5 mW idle**

BLOCK DIAGRAM



PIN DIAGRAM



16-Lead SON

CAUTION: Use handling procedures necessary for a static sensitive component.

SSI 32F8101
Low-Power Programmable Filter

FUNCTIONAL DESCRIPTION

The SSI 32F8101 programmable filter consists of an electronically controlled low-pass filter with a separate differentiated low-pass output. A seven-pole, low-pass filter is provided along with a single-pole, single-zero differentiator. Both outputs have matched delays. The delay matching is unaffected by any amount of programmed equalization or bandwidth. Programmable bandwidth and boost/equalization is provided by internal 7-bit control DACs. High-frequency boost equalization is accomplished by a two-pole, low-pass with a two-pole, high-pass feed forward section to provide complimentary real axis zeros. A variable attenuator is used to program the zero locations.

The filter implements a 0.05 degree equiripple linear phase response. The normalized transfer functions (i.e., $\omega c = 2\pi fc = 1$) are:

$Vnorm/Vi = 13.65983 \bullet [(-Ks^2 + 1.31703)/D(s)] \bullet AN$

and

$Vdiff/Vi = (Vnorm/Vi) \bullet (s/0.86133) \bullet AD$

Where D (s)=

$(S^2 + 1.68495s + 1.31703)(S^2 + 1.54203s + 2.95139)$

$(S^2 + 1.4558s + 5.37034)(s + 0.86133)$,

AN and AD are adjusted for a gain of 1 at fs = (2/3) fc.

FILTER OPERATION

Normally AC coupled differential signals are applied to the VIN± inputs of the filter, although DC coupling can be implemented. To improve settling time of the coupling capacitors, the VIN± inputs are placed into a Low-Z state when the $\overline{LOWZ}$ pin is brought low. The programmable bandwidth and boost/equalization features are controlled by internal DACs and the registers programmed through the serial port. The current reference for both DACs is set using a single 13.3 kΩ external resistor connected from pin RX to ground. The voltage at pin RX is proportional to absolute temperature (PTAT), hence the current for the DACs is a PTAT reference current.

Bandwidth Control

The programmable bandwidth is set by the filter cutoff DAC. This DAC has two separate 7-bit registers that can program the DAC value as follows:

$fc = 0.253 \bullet DACF - 2.218$ (MHz)

where DACF = Cutoff Frequency Control Register value (decimal)

The filter cutoff set by the internal DAC is the unboosted 3 dB frequency. When boost/equalization is added, the actual 3 dB point will move out. Table 1 provides information on boost versus 3 dB frequency.

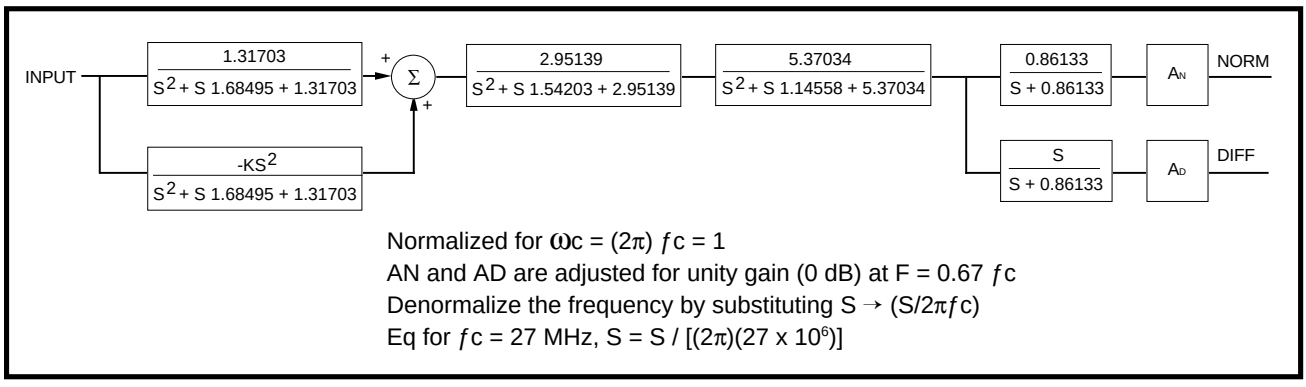


FIGURE 1: SSI 32F8101 Normalized Block Diagram

TABLE 1: Calculations

Typical change in f-3 dB point with boost

Boost (dB)	Gain@fc (dB)	Gain@ peak (dB)	$f$peak/fc	f-3 dB/fc	K
0	-3	no peak	no peak	1.00	0
1	-2	no peak	no peak	1.21	0.16
2	-1	no peak	no peak	1.50	0.34
3	0	0.15	0.70	1.80	0.54
4	1	0.99	1.05	2.04	0.77
5	2	2.15	1.23	2.20	1.03
6	3	3.41	1.33	2.33	1.31
7	4	4.68	1.38	2.43	1.63
8	5	5.94	1.43	2.51	1.97
9	6	7.18	1.46	2.59	2.40
10	7	8.40	1.48	2.66	2.85
11	8	9.59	1.51	2.73	3.36
12	9	10.77	1.51	2.80	3.93
13	10	11.92	1.53	2.87	4.57
14	11	13.06	1.53	2.93	5.28
15	12	14.18	1.56	3.0	6.09

Notes:
1. fc is the original programmed cutoff frequency with no boost
2. f - 3 dB is the new -3 dB value with boost implemented
3. $f$peak is the frequency where the amplitude reaches its maximum value with boost implemented

   i.e., fc = 9 MHz when boost = 0 dB

   if boost is programmed to 5 dB then f - 3 dB = 19.8 MHz

   $f$peak = 11.07 MHz

4. $K = 1.31703 \left(10^{\frac{\text{BOOST (dB)}}{20}} - 1\right)$

FUNCTIONAL DESCRIPTION (continued)

BOOST / EQUALIZATION CONTROL

The programmable equalization is also controlled by an internal DAC. The 7-bit Filter Boost Control Register (FBCR) determines the amount of equalization that will be added to the 3 dB cutoff frequency, as follows:

Boost =

$20 \log [(0.0239 \bullet DACB) + 7.6 \bullet 10^{-5} \bullet DACB \bullet DACF) + 1.132]$

where DACB = value in FBCR register.

For example, with the DAC set for maximum output (FBCR = 7F hex or 127) at the maximum cutoff frequency (DACF = 7F hex or 127) there will be 14.6 dB of boost added at the 3 dB frequency. This will result in +11 dB of signal boost above the 0 dB baseline.

SERIAL INTERFACE OPERATION

The serial interface is a CMOS bi-directional port for reading and writing programming data from/to the internal registers of the SSI 32F8101. For data transfers SDEN is brought high, serial data is presented at the SDATA pin, and a serial clock is applied to the SCLK pin.

After the SDEN goes high, the first 16 pulses applied to the SCLK pin will shift the data presented at the SDATA pin into an internal shift register on the rising edge of each clock. An internal counter prevents more than 16 bits from being shifted into the register. The data in the shift register is latched when SDEN goes low. If less than 16 clock pulses are provided before SDEN goes low, the data transfer is aborted.

All transfers are shifted into the serial port LSB first. The first byte of the transfer is address and instruction information. The LSB of this byte is the R/W bit which determines if the transfer is a read (1) or a write (0). The remaining seven bits determine the internal register to be accessed. The second byte contains the programming data. At initial power-up, the contents of the internal registers will be in an unknown state and they must be programmed prior to operation. During power down modes, the serial port remains active and register programming data is retained.

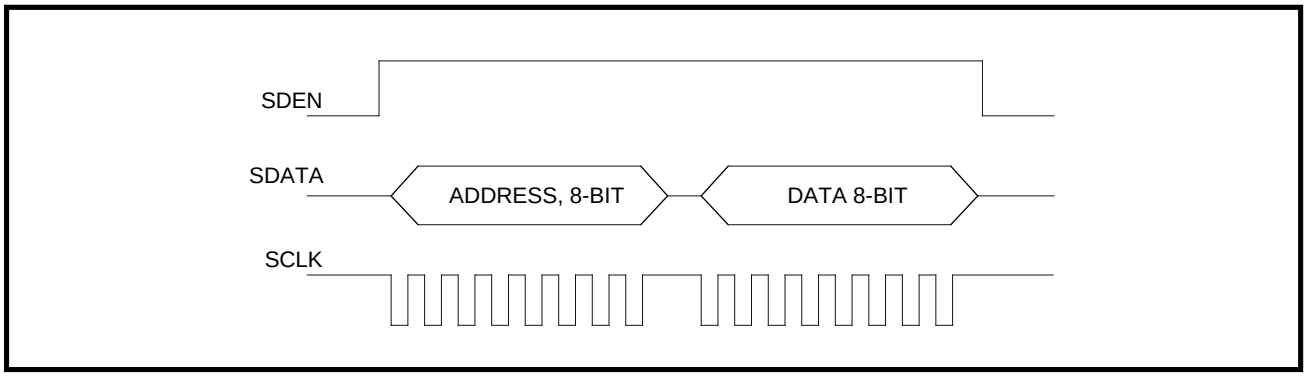


FIGURE 2: Serial Port Data Transfer Format

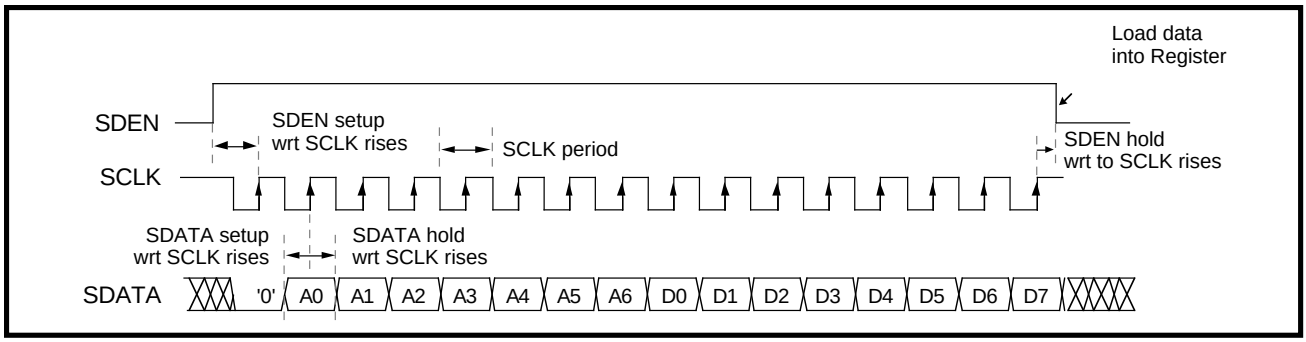


FIGURE 3: Serial Interface Timing Diagram - Writing Control Register

TABLE 2: Serial Port Register Mapping

REGISTER NAME	ADDRESS A6						A0	R/W	DATA BIT MAP D7							D0
POWER DOWN CONTROL	0	0	0	0	0	1	0	0	–	--	–	–	--	FILTER 1=DISABLE 0=ENABLE	--	
DATA MODE CUTOFF	0	0	0	0	0	1	1	0	*	DAC BIT 6	DAC BIT 5	DAC BIT 4	DAC BIT 3	DAC BIT 2	DAC BIT 1	DAC BIT 0
SERVO MODE CUTOFF	0	0	1	0	0	1	1	0	*	DAC BIT 6	DAC BIT 5	DAC BIT 4	DAC BIT 3	DAC BIT 2	DAC BIT 1	DAC BIT 0
FILTER BOOST	0	0	0	1	0	1	1	0	--	DAC BIT 6	DAC BIT 5	DAC BIT 4	DAC BIT 3	DAC BIT 2	DAC BIT 1	DAC BIT 0
FILTER BOOST, SERVO	0	0	1	1	0	1	1	0	--	DAC BIT 6	DAC BIT 5	DAC BIT 4	DAC BIT 3	DAC BIT 2	DAC BIT 1	DAC BIT 0

* These bits are used only for testing. They should be programmed to 0 in actual operation.

PIN DESCRIPTION

POWER SUPPLY PINS

NAME	TYPE	DESCRIPTION
VCA	-	Filter analog power supply pin
VCD	-	Serial port power supply pin
AGND	-	Filter analog ground pin
DGND	-	Serial port digital ground pin

INPUT PINS

VIN+, VIN-	I	FILTER SIGNAL INPUTS: The AGC output signals must be AC coupled into these pins.
SG	I	SERVO GATE: TTL input when high enables servo frequency and boost registers to the control DACs. When low the data frequency and boost registers are enabled.
$\overline{\text{LOWZ}}$	I	LOW_Z CONTROL: TTL input when low reduces the filter input resistance. When high, the input is at high impedance state.

OUTPUT PINS

VO_DIFF+,	O	DIFFERENTIAL DIFFERENTIATED OUTPUTS: Filter differentated VO_DIFF- outputs. These outputs are normally AC coupled.
VO_NORM+,	O	DIFFERENTIAL NORMAL OUTPUTS: Filter normal low pass output signals. VO_NORM- These outputs are normally AC coupled.
RX	-	REFERENCE RESISTOR INPUT: An external 13.3 kΩ, 1% resistor is connected from this pin to ground to establish a precise PTAT (proportional to absolute temperature) reference current for the filter.

SERIAL PORT PINS

SDEN	I/O	SERIAL DATA ENABLE: Serial enable CMOS compatible input. A high level input enables the serial port.
SDI	I/O	SERIAL DATA: Serial data CMOS compatible input. NRZ programming data for the internal registers is applied to this input.
SCLK	I/O	SERIAL CLOCK: Serial clock CMOS compatible input. The clock applied to this pin is synchronized with the data applied to SDATA.

ELECTRICAL SPECIFICATIONS

Unless otherwise specified, the recommended operating conditions are as follows: 4.5V < POSITIVE SUPPLY VOLTAGE < 5.5V, 0°C < T (ambient) < 70°C, and 25°C < T(junction) < 135°C. Currents flowing into the chip are positive. Current maximums are currents with the highest absolute value.
Rx = 13.3 kΩ, Cx = 1000 pF from Rx pin to VCA. Input signals are AC-coupled into VIN±.

ABSOLUTE MAXIMUM RATINGS

Operation beyond the maximum ratings may damage the device.

PARAMETER	RATING
Storage Temperature	-65 to 150°C
Junction Operating Temperature	+135°C
Positive Supply Voltage (Vp)	-0.5 to 7V
Voltage Applied to Logic Inputs	-0.5V to Vp + 0.5V
All other Pins	-0.5V to Vp + 0.5V

POWER SUPPLY CURRENT AND POWER DISSIPATION

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNITS
ICC (VCA,D)	Output pins open DACF = 127 Boost = 0 dB		19	30	mA
PWR Power Dissipation	Output pins open DACF = 127 Boost = 0 dB		95	165	mW
Sleep Mode Power	PWRON = 1			5	mW

TTL COMPATIBLE INPUTS

Input low voltage	VIL		-0.3		0.8	V
Input high voltage	VIH		2		VPD	V
					+0.3	
Input low current	IIL	VIL = 0.4V	-0.4			mA
Input high current	IIH	VIH = 2.4V			100	µA

CMOS COMPATIBLE INPUTS

Input low voltage	Vp = 5V	-0.3		1.5	V
Input high voltage	Vp = 5V	3.5		VCD +0.3	V

ELECTRICAL SPECIFICATIONS (continued)

SERIAL PORT

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNITS
SCLK period		Read from serial port	140			ns
		Write to serial port	100			ns
SCLK low time	TCKL	Read from serial port	60			ns
		Write to serial port	40			ns
SCLK high time	TCKH	Read from serial port	60			ns
		Write to serial port	40			ns
Enable to SCLK	TSENS		35			ns
SCLK to disable	TSENH		100			ns
Data set-up time	TDS		15			ns
Data hold time	TDH		15			ns
SDATA tri-state delay	TSENDL				50	ns
SDATA turnaround time	TTRN		70			ns
SDEN low time	TSL		200			ns

PROGRAMMABLE FILTER CHARACTERISTICS

Filter cutoff range	fc @ -3 dB point fc (MHz) = 0.253 • DACF - 2.218, Boost = 0 dB 42 ≤ DACF ≤ 127		8.4 - 30		MHz
Filter cutoff accuracy	DACF = 42 and 127	-15		15	%
FNP, FNN differential gain AN	f = 0.67xfc, boost = 0 dB	0.7	1.0	1.25	V/V
FDP, FDN differential gain AD	f = 0.67xfc, boost = 0 dB	0.8 AN	1.0 AN	1.2 AN	V/V
Boost accuracy Boost = 20 log [(0.0239 • DACB) + (7.6 • 10^{-5} • DACB • DACF) + 1.132]	6.6 dB, DACF = 42, DACS = 37	-1.0		+1.0	dB
	7.5 dB, DACF = 127, DACS = 37	-1.0		+1.0	dB
	9.4 dB, DACF = 42, DACS = 67	-1.25		+1.25	dB
	10.6 dB, DACF = 127, DACS = 67	-1.25		+1.25	dB
	13.2 dB, DACF = 42, DACS = 127	1.5		+1.5	dB
	14.6 dB, DACF = 127, DACS = 127	-1.5		+1.5	dB
Data mode group delay variation, DACF = 0 to 127	f = 0.2 fc to fc, 42 ≤ DACF ≤ 127	-2		+2	%
	f = fc to 1.75 fc, 42 ≤ DACF ≤ 84	-3		+3	%
	85 ≤ DACF ≤ 127	-6.5		+6.5	%

PROGRAMMABLE FILTER CHARACTERSITICS (continued)

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNITS
Data mode group delay variation, DACS = 0 to 127	DACF = 127 f = 0.2 fc to fc	-0.5		+0.5	ns
	DACF = 42 f = 0.2 fc to fc	-1.25		+1.25	ns
	DACF = 127 f = fc to 1.75fc	-1.5		+1.5	ns
	DACF = 42 f = fc to 1.75fc	-1.9		+1.9	ns
Filter differential output dynamic range	THD = 1.5%, f = 0.67fc boost = 0 dB, normal and differentiated outputs	1			Vp-p
Filter differential input resistance	Normal	4			kΩ
	Low-Z		200	400	Ω
Filter differential input capacitance				7	pF
Output Noise Voltage: BW = 100 MHz, Rs = 50Ω					
differentiated output	fc = 30 MHz, boost = 0 dB		4.4	6.6	mV Rms
differentiated output	fc = 30 MHz, DACS = 127		7.7	11.6	mV Rms
normal output	fc = 30 MHz, boost = 0 dB		2.5	3.8	mV Rms
normal output	fc = 30 MHz, DACS = 127		3.7	5.6	mV Rms
Filter output sink current		0.5			mA
Filter output offset voltage		-200		200	mV
Filter output source current		2.0			mA
Filter output resistance	single ended			200	Ω
Rx pin voltage	Ta = 27°C		600		mV
	Ta = 127°C		800		mV
Rx resistance	1% fixed value		13.3		kΩ

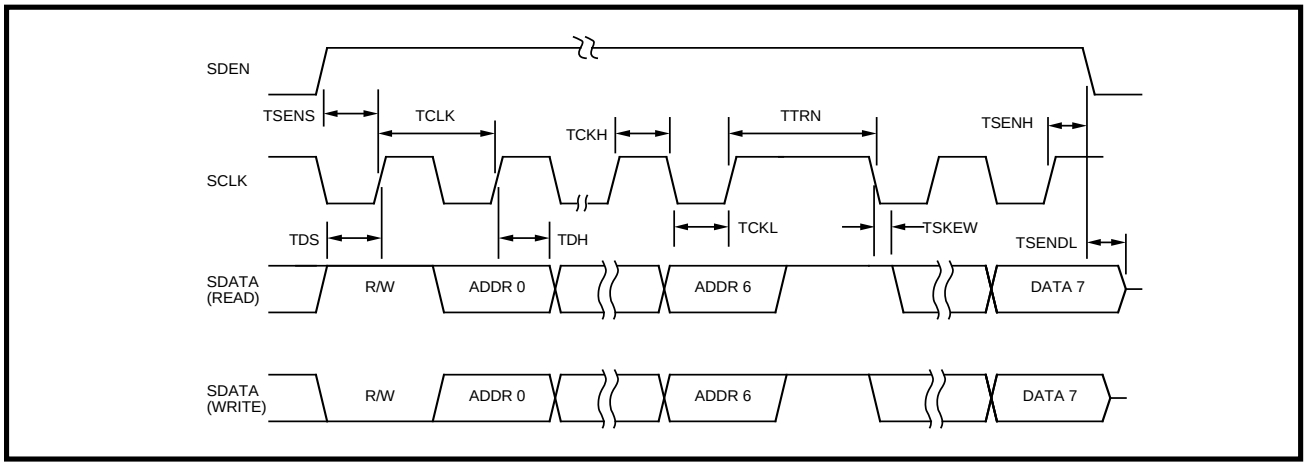
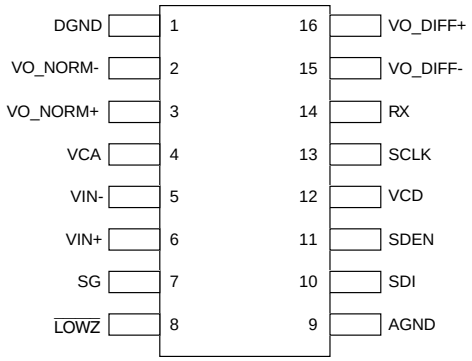


FIGURE 4: Serial Port Timing Information

PACKAGE PIN DESIGNATIONS

(Top View)



16-Lead SON

THERMAL CHARACTERISTICS: θja

16-lead SON	100° C/W

CAUTION: Use handling procedures necessary for a static sensitive component.

ORDERING INFORMATION

PART DESCRIPTION	ORDER NUMBER	PACKAGE MARK
SSI 32F8101 16-Lead SON	32F8101-CN	32F8101-CN

Preliminary Data: Indicates a product not completely released to production. The specifications are based on preliminary evaluations and are not guaranteed. Small quantities are available, and Silicon Systems should be consulted for current information.

Silicon Systems, Inc., 14351 Myford Road, Tustin, CA 92680-7022 (714) 573-6000, FAX (714) 573-6914

SSI 32F8102/8103/8104
Low-Power Programmable Filter

February 1996

DESCRIPTION

The 32F810X is a high performance, low power, digitally programmable low-pass filter for applications requiring variable-frequency filtering. The device consists of three functional blocks: [1] a 7th-order 0.05° Equiripple Low-Pass filter, [2] two DACs for controlling the filter cutoff frequency and high-frequency peaking (boost), and [3] a Serial Port for programming the fc and Boost DACs.

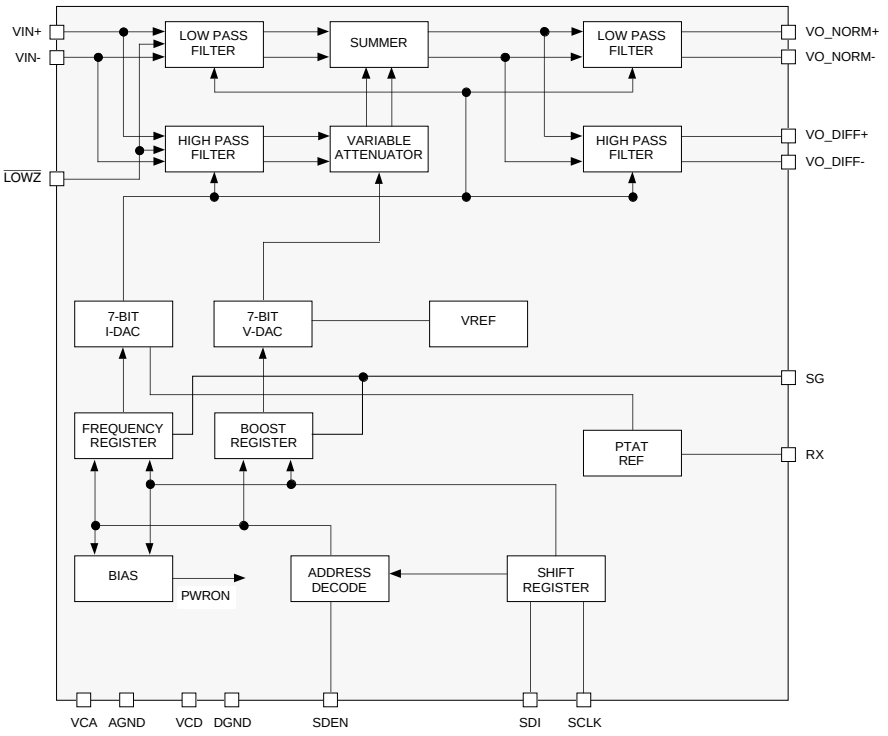
Cutoff frequency and boost are controlled by the two on-chip 7-bit DACs, which are programmed via the 3-line serial interface. Boost is programmable from 0 to 14.3 dB nominally at maximum fc, and is implemented using two symmetrical, real-axis zeroes. Both boost and fc control do not affect the flat group delay response.

The 32F810X device is ideal for variable data rate and variable frequency shaping applications. It requires only a +5V supply and has an idle mode for minimal power dissipation. The SSI 32F810X is available in a 16-lead SON package.

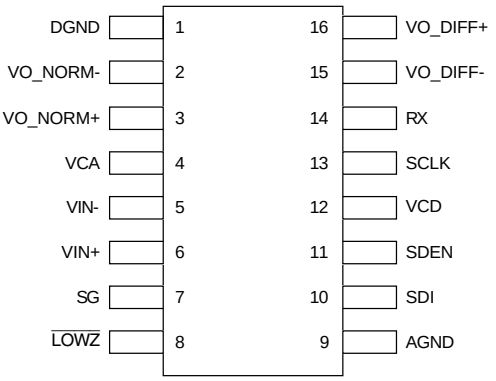
FEATURES

- **Programmable cutoff frequency:**
  - **32F8102 - 5.5 to 18 MHz**
  - **32F8103 - 3.7 to 12 MHz**
  - **32F8104 - 2.9 to 9 MHz**
- **Programmable boost/equalization of 0 to 14.3 dB**
- **Matched normal and differentiated outputs**
- **±15% fc accuracy**
- **±2% maximum group delay variation**
- **Less than 1.5% total harmonic distortion**
- **Low-Z input switch controlled by $\overline{\text{LOWZ}}$ pin**
- **No external filter components required**
- **95 mW nominal power, <5 mW idle**

BLOCK DIAGRAM



PIN DIAGRAM



16-Lead SON

CAUTION: Use handling procedures necessary for a static sensitive component.

SSI 32F8102/8103/8104
Low-Power Programmable Filter

FUNCTIONAL DESCRIPTION

The SSI 32F810X programmable filter consists of an electronically controlled low-pass filter with a separate differentiated low-pass output. A seven-pole, low-pass filter is provided along with a single-pole, single-zero differentiator. Both outputs have matched delays. The delay matching is unaffected by any amount of programmed equalization or bandwidth. Programmable bandwidth and boost/equalization is provided by internal 7-bit control DACs. High-frequency boost equalization is accomplished by a two-pole, low-pass with a two-pole, high-pass feed forward section to provide complimentary real axis zeros. A variable attenuator is used to program the zero locations.

The filter implements a 0.05 degree equiripple linear phase response. The normalized transfer functions (i.e., $\omega c = 2\pi fc = 1$) are:

$Vnorm/Vi = 13.65983 \bullet [(-Ks^2 + 1.31703)/D(s)] \bullet AN$

and

$Vdiff/Vi = (Vnorm/Vi) \bullet (s/0.86133) \bullet AD$

Where D (s)=

$(S^2 + 1.68495s + 1.31703)(S^2 + 1.54203\ s + 2.95139)$

$(S^2 + 1\ .4558s + 5.37034)(s + 0.86133)$,

AN and AD are adjusted for a gain of 1 at $fs = (2/3)fc$.

FILTER OPERATION

Normally AC coupled differential signals are applied to the VIN± inputs of the filter, although DC coupling can be implemented. To improve settling time of the coupling capacitors, the VIN± inputs are placed into a Low-Z state when the $\overline{LOWZ}$ pin is brought low. The programmable bandwidth and boost/equalization features are controlled by internal DACs and the registers programmed through the serial port. The current reference for both DACs is set using a single 13.3 kΩ external resistor connected from pin RX to ground. The voltage at pin RX is proportional to absolute temperature (PTAT), hence the current for the DACs is a PTAT reference current.

Bandwidth Control

The programmable bandwidth is set by the filter cutoff DAC. This DAC has two separate 7-bit registers that can program the DAC value as follows:

$fc = 0.1474 \bullet DACF - 0.726$ (MHz) for the 32F8102
$fc = 0.09745 \bullet DACF - 0.376$ (MHz) for the 32F8103
$fc = 0.07198 \bullet DACF - 0.142$ (MHz) for the 32F8104
where DACF = Cutoff Frequency Control Register value (decimal)

The filter cutoff set by the internal DAC is the unboosted 3 dB frequency. When boost/equalization is added, the actual 3 dB point will move out. Table 1 provides information on boost versus 3 dB frequency.

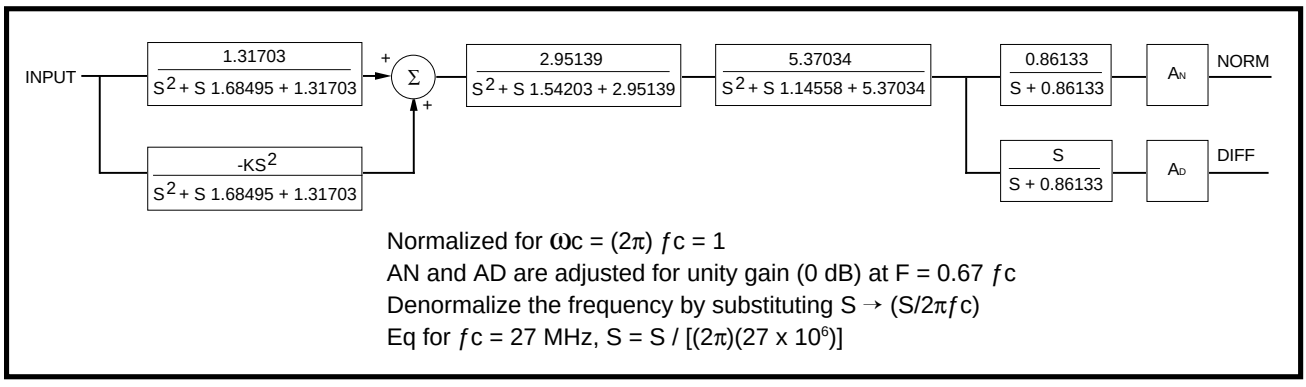


FIGURE 1: 32F8102/8103/8104 Normalized Block Diagram

TABLE 1: Calculations

Typical change in f-3 dB point with boost

Boost (dB)	Gain@fc (dB)	Gain@ peak (dB)	$f$peak/fc	f-3dB/fc	K
0	-3	no peak	no peak	1.00	0
1	-2	no peak	no peak	1.21	0.16
2	-1	no peak	no peak	1.50	0.34
3	0	0.15	0.70	1.80	0.54
4	1	0.99	1.05	2.04	0.77
5	2	2.15	1.23	2.20	1.03
6	3	3.41	1.33	2.33	1.31
7	4	4.68	1.38	2.43	1.63
8	5	5.94	1.43	2.51	1.97
9	6	7.18	1.46	2.59	2.40
10	7	8.40	1.48	2.66	2.85
11	8	9.59	1.51	2.73	3.36
12	9	10.77	1.51	2.80	3.93
13	10	11.92	1.53	2.87	4.57
14	11	13.06	1.53	2.93	5.28

Notes:
1. fc is the original programmed cutoff frequency with no boost
2. f-3 dB is the new -3 dB value with boost implemented
3. $f$peak is the frequency where the amplitude reaches its maximum value with boost implemented

i.e., fc = 9 MHz when boost = 0 dB

if boost is programmed to 5 dB then f-3 dB = 19.8 MHz

$f$peak = 11.07 MHz

4. $K = 1.31703 \left(10^{\frac{\text{BOOST (dB)}}{20}} - 1\right)$

BOOST/EQUALIZATION CONTROL

The programmable equalization is also controlled by an internal DAC. The 7-bit Filter Boost Control Register (FBCR) determines the amount of equalization that will be added to the 3 dB cutoff frequency, as follows:

Boost (dB) = 20 • log [0.0239 • DACB + 7.6 • 10^{-5} • DACB • DACF + 1.132] for 32F8102

Boost (dB) = 20 • log [0.025 • DACB + 4.7 • 10^{-5} • DACB • DACF + 1.1] for 32F8103

Boost (dB) = 20 • log [0.0253 • DACB + 5.27 • 10^{-5} • DACB • DACF + 1.1] for 32F8104

where DACB = value in FBCR register.

For example, with the DAC set for maximum output (FBCR = 7F hex or 127) at the maximum cutoff frequency (DACF = 7F hex or 127) there will be 14 dB of boost added at the 3 dB frequency. This will result in +11 dB of signal boost above the 0 dB baseline.

SERIAL INTERFACE OPERATION

The serial interface is a CMOS bi-directional port for reading and writing programming data from/to the internal registers of the 32F810X. For data transfers SDEN is brought high, serial data is presented at the SDATA pin, and a serial clock is applied to the SCLK pin.

After the SDEN goes high, the first 16 pulses applied to the SCLK pin will shift the data presented at the SDATA pin into an internal shift register on the rising edge of each clock. An internal counter prevents more than 16 bits from being shifted into the register. The data in the shift register is latched when SDEN goes low. If less than 16 clock pulses are provided before SDEN goes low, the data transfer is aborted.

All transfers are shifted into the serial port LSB first. The first byte of the transfer is address and instruction information. The LSB of this byte is the R/W bit which determines if the transfer is a read (1) or a write (0). The remaining seven bits determine the internal register to be accessed. The second byte contains the programming data. At initial power-up, the contents of the internal registers will be in an unknown state and they must be programmed prior to operation. During power down modes, the serial port remains active and register programming data is retained.

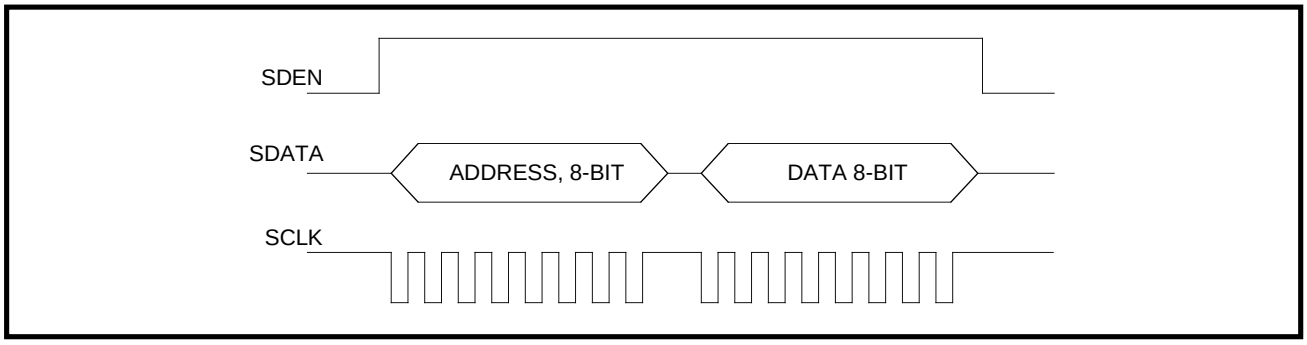


FIGURE 2: Serial Port Data Transfer Format

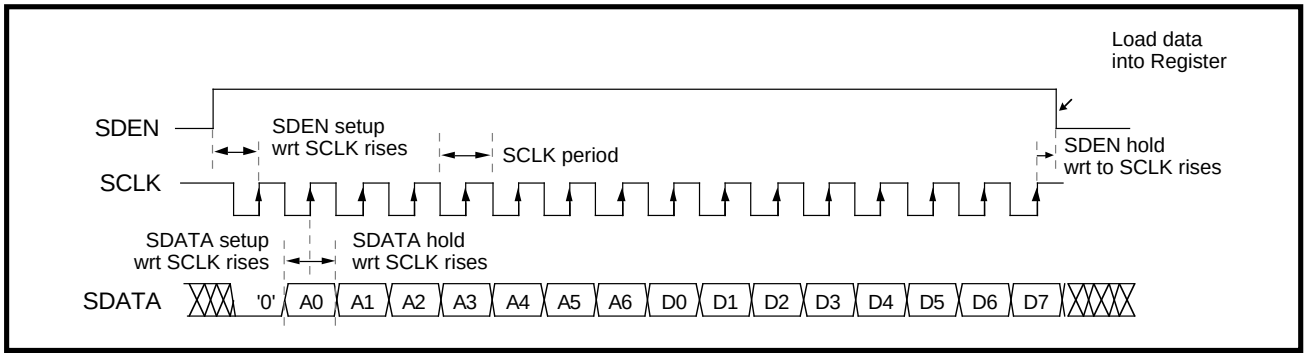


FIGURE 3: Serial Interface Timing Diagram - Writing Control Register

TABLE 2: Serial Port Register Mapping

REGISTER NAME	ADDRESS							R/W	DATA BIT MAP							
	A6					A0			D7							D0
POWER DOWN CONTROL	0	0	0	0	0	1	0	0	--	--	--	--	--	FILTER 1=DISABLE 0=ENABLE	--	
DATA MODE CUTOFF	0	0	0	0	0	1	1	0	*	DAC BIT 6	DAC BIT 5	DAC BIT 4	DAC BIT 3	DAC BIT 2	DAC BIT 1	DAC BIT 0
SERVO MODE CUTOFF	0	0	1	0	0	1	1	0	*	DAC BIT 6	DAC BIT 5	DAC BIT 4	DAC BIT 3	DAC BIT 2	DAC BIT 1	DAC BIT 0
FILTER BOOST	0	0	0	1	0	1	1	0	--	DAC BIT 6	DAC BIT 5	DAC BIT 4	DAC BIT 3	DAC BIT 2	DAC BIT 1	DAC BIT 0
FILTER BOOST, SERVO	0	0	1	1	0	1	1	0	--	DAC BIT 6	DAC BIT 5	DAC BIT 4	DAC BIT 3	DAC BIT 2	DAC BIT 1	DAC BIT 0

* These bits are used only for testing. They should be programmed to 0 in actual operation.

PIN DESCRIPTION

POWER SUPPLY PINS

NAME	TYPE	DESCRIPTION
VCA	-	Filter analog power supply pin
VCD	-	Serial port power supply pin
AGND	-	Filter analog ground pin
DGND	-	Serial port digital ground pin

INPUT PINS

VIN+, VIN-	I	FILTER SIGNAL INPUTS: The AGC output signals must be AC coupled into these pins.
SG	I	SERVO GATE: TTL input when high enables servo frequency and boost registers to the control DACs. When low the data frequency and boost registers are enabled.
$\overline{\text{LOWZ}}$	I	LOW_Z CONTROL: TTL input when low reduces the filter input resistance. When high, the input is at high impedance state.

OUTPUT PINS

VO_DIFF+, VO_DIFF-	O	DIFFERENTIAL DIFFERENTIATED OUTPUTS: Filter differentated outputs. These outputs are normally AC coupled.
VO_NORM+, VO_NORM-	O	DIFFERENTIAL NORMAL OUTPUTS: Filter normal low pass output signals. These outputs are normally AC coupled.
RX	-	REFERENCE RESISTOR INPUT: An external 13.3 kΩ, 1% resistor is connected from this pin to ground to establish a precise PTAT (proportional to absolute temperature) reference current for the filter.

SERIAL PORT PINS

SDEN	I/O	SERIAL DATA ENABLE: Serial enable CMOS compatible input. A high level input enables the serial port.
SDI	I/O	SERIAL DATA: Serial data CMOS compatible input. NRZ programming data for the internal registers is applied to this input.
SCLK	I/O	SERIAL CLOCK: Serial clock CMOS compatible input. The clock applied to this pin is synchronized with the data applied to SDATA.

ELECTRICAL SPECIFICATIONS

Unless otherwise specified, the recommended operating conditions are as follows: 4.5V < POSITIVE SUPPLY VOLTAGE < 5.5V, 0°C < T (ambient) < 70°C, and 25°C < T(junction) < 130°C. Currents flowing into the chip are positive. Current maximums are currents with the highest absolute value.
Rx = 13.3 kΩ, Cx = 1000 pF from Rx pin to VCA. Input signals are AC-coupled into VIN±.

ABSOLUTE MAXIMUM RATINGS
Operation beyond the maximum ratings may damage the device.

PARAMETER	RATING
Storage Temperature	-65 to 150°C
Junction Operating Temperature	+130°C
Positive Supply Voltage (Vp)	-0.5 to 7V
Voltage Applied to Logic Inputs	-0.5V to Vp + 0.5V
All other Pins	-0.5V to Vp + 0.5V

POWER SUPPLY CURRENT AND POWER DISSIPATION

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNITS
ICC (VCA,D)	Output pins open DACF = 127 Boost = 0 dB		19	30	mA
PWR Power Dissipation	Output pins open DACF = 127 Boost = 0 dB		95	165	mW
Sleep Mode Power	PWRON = 1			5	mW

TTL COMPATIBLE INPUTS

Input low voltage	VIL		-0.3		0.8	V
Input high voltage	VIH		2		VPD +0.3	V
Input low current	IIL	VIL = 0.4V	-0.4			mA
Input high current	IIH	VIH = 2.4V			100	µA

CMOS COMPATIBLE INPUTS

Input low voltage	Vp = 5V	-0.3		1.5	V
Input high voltage	Vp = 5V	3.5		VCD +0.3	V

ELECTRICAL SPECIFICATIONS (continued)

SERIAL PORT

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNITS
SCLK period		Read from serial port	140			ns
		Write to serial port	100			ns
SCLK low time	TCKL	Read from serial port	60			ns
		Write to serial port	40			ns
SCLK high time	TCKH	Read from serial port	60			ns
		Write to serial port	40			ns
Enable to SCLK	TSENS		35			ns
SCLK to disable	TSENH		100			ns
Data set-up time	TDS		15			ns
Data hold time	TDH		15			ns
SDATA tri-state delay	TSENDL				50	ns
SDATA turnaround time	TTRN		70			ns
SDEN low time	TSL		200			ns

PROGRAMMABLE FILTER CHARACTERISTICS

Filter cutoff range (32F8102)		fc @ -3 dB point fc (MHz) = 0.1474 • DACF - 0.7258 42 ≤ DACF ≤ 127	5.5		18	MHz
Filter cutoff range (32F8103)		fc @ -3 dB point fc (MHz) = 0.09745 • DACF - 0.3756 42 ≤ DACF ≤ 127	3.7		12	MHz
Filter cutoff range (32F8104)		fc @ -3 dB point fc (MHz) = 0.07198 • DACF - 0.142 42 ≤ DACF ≤ 127	2.9		9	MHz
Filter cutoff accuracy		DACF = 42 and 127	-15		15	%
FNP, FNN differential gain	AN	f = 0.67 • fc, boost = 0 dB	0.8	1.0	1.25	V/V
FDP, FDN differential gain	AD	f = 0.67 • fc, boost = 0 dB	0.8 AN	1.0 AN	1.25 AN	V/V

PROGRAMMABLE FILTER CHARACTERSITICS (continued)

PARAMETER	CONDITIONS		MIN	NOM	MAX	UNITS
Boost accuracy	DACF = 42, DACB = 37		-1.0		+1.0	dB
	DACF = 127, DACB = 37		-1.0		+1.0	dB
	DACF = 42, DACB = 67		-1.25		+1.25	dB
	DACF = 127, DACB = 67		-1.25		+1.25	dB
	DACF = 42, DACB = 127		1.5		+1.5	dB
	DACF = 127, DACB = 127		-1.5		+1.5	dB
Data mode group delay	f = 0.2 fc to fc		-2		+2	%
variation, DACF = 42 to 127, DACB = 0 to 127	f = fc to 1.75 fc		-4		+4	%
Data mode group delay	DACF = 127	32F8102	-0.75		+0.75	ns
variation, DACB = 0 to 127	f = 0.2 fc to fc	32F8103	-1.0		+1.0	ns
		32F8104	-1.25		+1.25	ns
	DACF = 42	32F8102	-2.5		+2.5	ns
	f = 0.2 fc to fc	32F8103	-3		+3	ns
		32F8104	-3.75		+3.75	ns
	DACF = 127	32F8102	-1.4		+1.4	ns
	f = fc to 1.75fc	32F8103	-1.5		+1.5	ns
		32F8104	-1.9		+1.9	ns
	DACF = 42	32F8102	-2.85		+2.85	ns
	f = fc to 1.75fc	32F8103	-3.75		+3.75	ns
		32F8104	-5.65		+5.65	ns
Filter differential output dynamic range	THD = 1.5%, f = 0.67fc boost = 0 dB, normal and differentiated outputs		1			Vp-p
Filter differential input resistance	Normal		4			kΩ
	Low-Z			200	400	Ω
Filter differential input capacitance					7	pF

PROGRAMMABLE FILTER CHARACTERSITICS (continued)

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNITS
Output Noise Voltage: BW = 100 MHz, Rs = 50Ω					
32F8102					
differentiated output	ƒc = 18 MHz, boost = 0 dB		4.1	6.2	mV Rms
differentiated output	ƒc = 18 MHz, DACS = 127		6.9	10.4	mV Rms
normal output	ƒc = 18 MHz, boost = 0 dB		2.2	3.3	mV Rms
normal output	ƒc = 18 MHz, DACS = 127		3.2	4.8	mV Rms
32F8103					
differentiated output	ƒc = 12 MHz, boost = 0 dB		3.8	5.7	mV Rms
differentiated output	ƒc = 12 MHz, DACS = 127		6.5	9.8	mV Rms
normal output	ƒc = 12 MHz, boost = 0 dB		2.2	3.3	mV Rms
normal output	ƒc = 12 MHz, DACS = 127		3.1	4.7	mV Rms
32F8104					
differentiated output	ƒc = 9 MHz, boost = 0 dB		3.6	5.4	mV Rms
differentiated output	ƒc = 9 MHz, DACS = 127		5.6	8.4	mV Rms
normal output	ƒc = 9 MHz, boost = 0 dB		2.0	3.0	mV Rms
normal output	ƒc = 9 MHz, DACS = 127		2.7	4.1	mV Rms
Filter output sink current		0.5			mA
Filter output offset voltage		-200		200	mV
Filter output source current		2.0			mA
Filter output resistance	single ended			200	Ω
Rx pin voltage	Ta = 27°C		600		mV
	Ta = 127°C		800		mV
Rx resistance	1% fixed value		13.3		kΩ

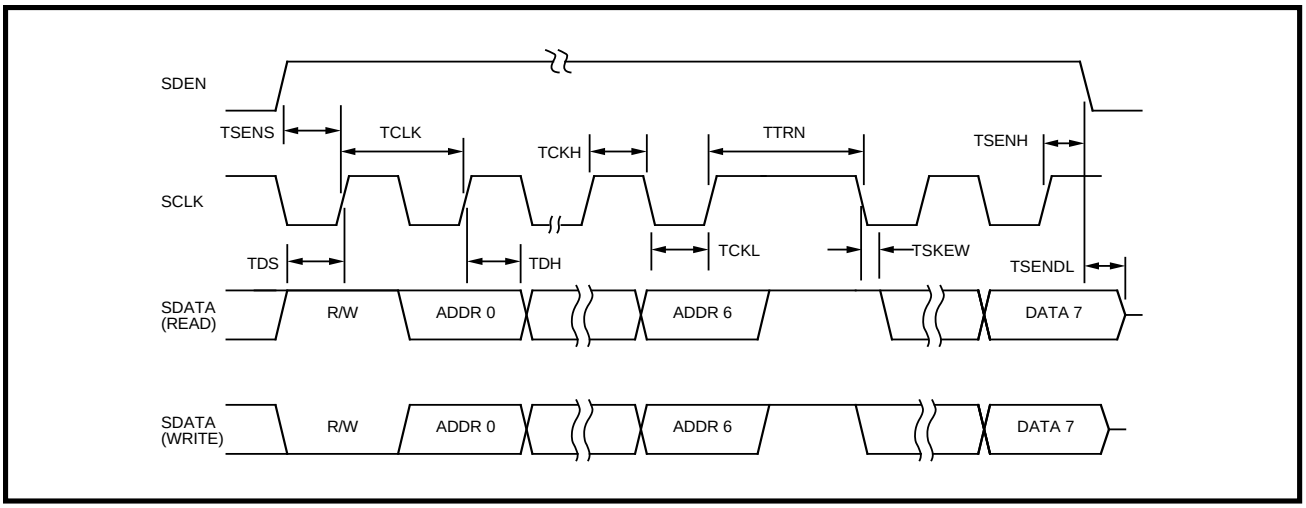


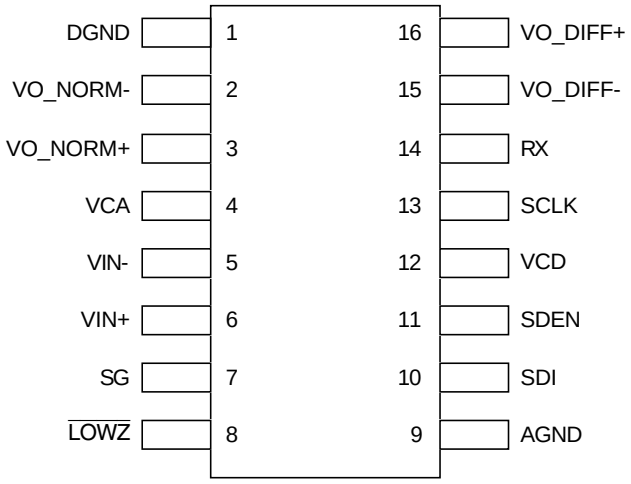
FIGURE 4: Serial Port Timing Information

PACKAGE PIN DESIGNATIONS

(Top View)

THERMAL CHARACTERISTICS: θja

16-lead SON	100° C/W



16-Lead SON

CAUTION: Use handling procedures necessary for a static sensitive component.

ORDERING INFORMATION

PART DESCRIPTION		ORDER NUMBER	PACKAGE MARK
SSI 32F8102	16-Lead SON	32F8102-CN	32F8102-CN
SSI 32F8103	16-Lead SON	32F8103-CN	32F8103-CN
SSI 32F8104	16-Lead SON	32F8104-CN	32F8104-CN

Silicon Systems, Inc., 14351 Myford Road, Tustin, CA 92680-7022 (714) 573-6000, FAX (714) 573-6914

SSI 32F8120
Low-Power Programmable Electronic Filter

January 1994

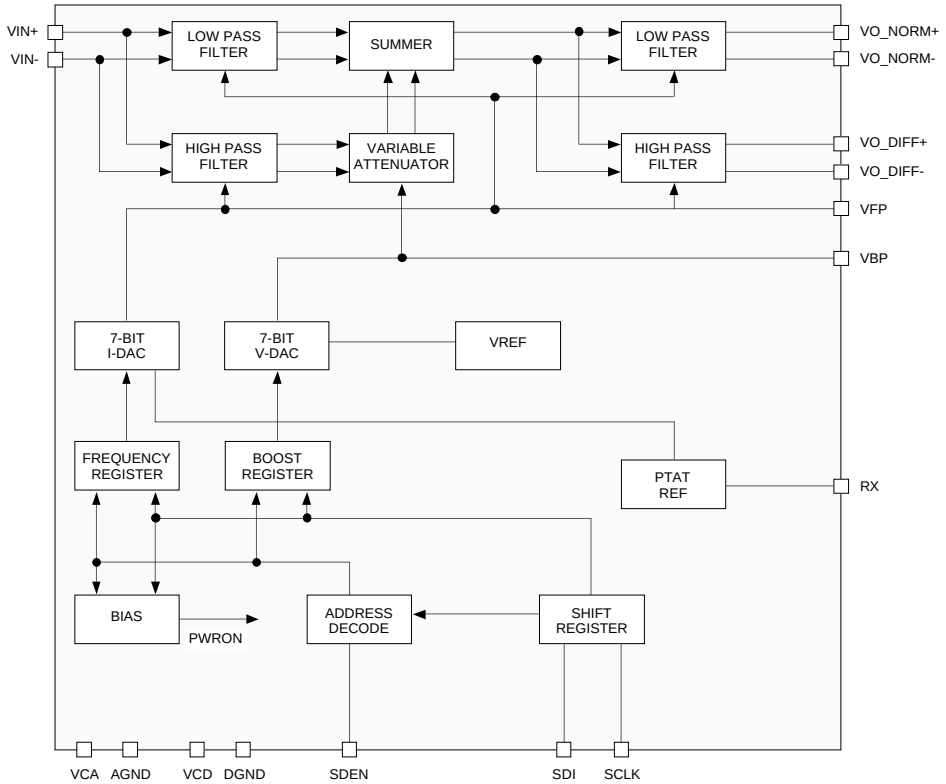
DESCRIPTION

The SSI 32F8120 is a continuous time, low pass filter with programmable bandwidth and high frequency boost. The low pass filter is a 2 zero / 7 pole 0.05° phase equiripple type, featuring excellent group delay characteristics. It features 1.5 - 8 MHz programmable bandwidth and 0-10 dB programmable boost. Both functions are controlled by 7-bit command words, which are input via a 3-line serial interface.

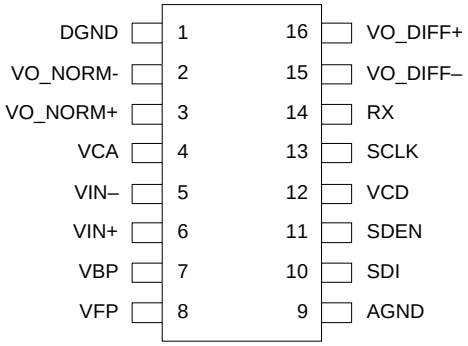
FEATURES

- **Programmable filter cutoff frequency (fc =1.5 to 8 MHz) with no external components**
- **Programmable pulse slimming equalization (0 to 10 dB boost at the filter cutoff frequency)**
- **± 10% cutoff frequency accuracy**
- **Matched normal and differentiated low-pass outputs**
- **Differential filter inputs and outputs**
- **Device Idle mode**
- **+5V only operation**
- **No external filter components required**
- **Supports constant density recording**

BLOCK DIAGRAM



PIN DIAGRAM



CAUTION: Use handling procedures necessary for a static sensitive component.

SSI 32F8120
Low-Power Programmable Electronic Filter

FUNCTIONAL DESCRIPTION

CUTOFF FREQUENCY PROGRAMMING

The SSI 32F8120 programmable electronic filter can be set to a filter cutoff frequency from 1.5 to 8 MHz. The cutoff frequency can be set by using the serial port through pins SDI, SDEN, and SCLK. SDI is the serial data input for an 8-bit control shift register, SDEN is the control register enable, and SCLK is the control register clock. The data packet is transmitted MSB (D7) first. The first four bits are the register address, the last four are the data bits. Registers larger than four bits must be loaded with two 8-bit data packets. See Table 1.

f_c is determined by the equation:

f_c (MHz) = 0.061321 (F_Code) + 0.212264

1.5 MHz ≤ f_c ≤ 8 MHz

21 ≤ F_ Code ≤ 127

SLIMMER HIGH FREQUENCY BOOST PROGRAMMING

The amplitude of the input signal at frequencies near the cutoff frequency can be increased using this feature. By controlling the V-DAC output, the boost can be determined. The amount of boost at the cutoff frequency is related to the V-DAC output by the following formula:

$$[\text{Output of V}-\text{DAC} = \text{VBP} = \text{VREF} \times \frac{\text{S\_Code}}{127}]$$

BOOST (dB) = 20•log [0.01703 (S_Code) +1].

TABLE 1

ADDRESS BITS				USAGE	DATA BITS			
D7	D6	D5	D4		D3	D2	D1	D0
X	0	0	0	S-MSB REGISTER	X	S6	S5	S4
X	0	0	1	S-LSB REGISTER	S3	S2	S1	S0
X	0	1	0	F-MSB REGISTER	X	F6	F5	F4
X	0	1	1	F-LSB REGISTER	F3	F2	F1	F0
X	1	1	1	P REGISTER	X	X	X	P0

X = Don't Care
S = 7-bit Boost (Slimming) Control
F = 7-bit Frequency (Bandwidth) Control
P = Power Down Control; PO = 1 for power up; PO = 0 for power down

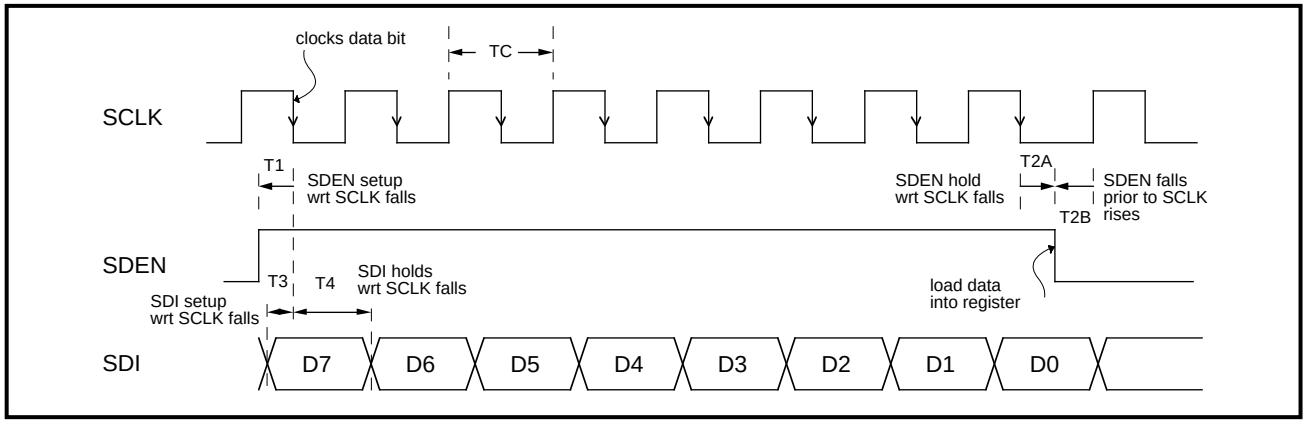


FIGURE 1: Serial Port Timing Diagram

PIN DESCRIPTION

NAME	TYPE	DESCRIPTION
VIN+, VIN–	I	DIFFERENTIAL FILTER INPUTS. The input signals must be AC coupled to these pins.
VO_NORM+, VO_NORM–	O	DIFFERENTIAL NORMAL OUTPUTS. The output signals must be AC coupled to the pulse detector.
VO_DIFF+ VO_DIFF–	O	DIFFERENTIAL DIFFERENTIATED OUTPUTS. For minimum pulse pairing, these outputs should be AC coupled to the pulse detector.
SDEN	I	SERIAL DATA ENABLE. A logic HIGH level allows SERIAL CLOCK to clock data into the control register via the SERIAL DATA input. A logic LOW level latches the register data and issues the information to the appropriate circuitry.
SCLK	I	SERIAL CLOCK. Negative edge triggered clock input for serial register.
SDI	I	SERIAL DATA INPUT.
RX	–	REFERENCE CURRENT SET. With an external resistor (Rx = 5 kΩ ±1%) to ground, this pin gives a voltage proportional to the absolute temperature, setting the range for VFP.
VCA	I	ANALOG +5 VOLT SUPPLY.
VCD	I	DIGITAL +5 VOLT SUPPLY.
AGND	I	ANALOG GROUND.
DGND	I	DIGITAL GROUND.
VBP	O	BOOST PROGRAMMING VOLTAGE. Output of V-DAC which programs the boost.
VFP	O	CUTOFF FREQUENCY PROGRAMMING VOLTAGE. Output of I-DAC which programs the cutoff frequency.*
*A minimum load resistance of 150 kΩ should be used to avoid affecting the total minimum on-chip resistance of 1.35 kΩ.		

ELECTRICAL SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Operation above maximum ratings may damage the device.

PARAMETER	RATING
Storage Temperature	-65 to +150 °C
Junction Operating Temperature, Tj	+130 °C
Supply Voltage, VCC	-0.5 to 7V
Voltage Applied to Inputs*	-0.5 to VCC V
Maximum Power Dissipation, fc = 8 MHz, Vcc = 5.5V	0.5W
T1 Lead Temperature (1/16" from case for 10 seconds)	260 °C
* Analog input signals of this magnitude shall not cause any change or degradation in filter performance after signal has returned to normal operating range.	

RECOMMENDED OPERATING CONDITIONS

Supply voltage, VCC	4.5V < VCC < 5.5V
Ambient Temperature	0 °C < Ta < 70 °C
Tj Junction Temperature	0 °C < Tj < 130 °C

ELECTRICAL CHARACTERISTICS

Unless otherwise specified recommended operating conditions apply.

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
Isupply	VCC = 5.5V, outputs unloaded		55	75	mA
Idle Mode Current			9	13	mA
Idle to Active Mode Recovery Time				50	µs
Serial port program to output response time				50	µs

DC Characteristics

VIH	High Level Input Voltage	TTL input	2.0			V
VIL	Low Level Input Voltage				0.8	V
IIH	High Level Input Current	VIH = 2.7V			20	µA
IIL	Low Level Input Current	VIL = 0.4V	–1.5			mA

Filter Characteristics

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
f_c Filter Cutoff Frequency	21 ≤ F_Code ≤ 127	1.5		8	MHz
FCA Filter f_c Accuracy	F_Code = 127	-10		+10	%
	F_Code = 21	-15		+15	%
Cutoff Resolution	1.5 to 8 MHz	100			kHz
AO VO_NORM Diff Gain	F = 0.67 f_c	0.7		1.1	V/V
AD VO_DIFF Diff Gain	F = 0.67 f_c	0.90 AO		1.2 AO	V/V
FB Frequency Boost at f_c	FB(dB) = 20 log [0.01703 (S_Code) +1]	0		10	dB
FBA Frequency Boost Accuracy	0 to 10 dB, Ta < 22 °C	–1.5		+1.5	dB
FBA Frequency Boost Accuracy	0 to 10 dB, Ta > 22 °C	–1		+1	dB
TGD0 Group Delay Variation Without Boost	0.2 f_c - f_c	–2% gdm		+2% gdm	ns
f_c = 1.5 - 8 MHz gdm = group delay magnitude	f_c - 1.75 f_c	–3% gdm		+3% gdm	ns
TGDB Group Delay Variation With Boost	0.2 f_c - f_c	–2% gdm		+2% gdm	ns
f_c = 1.5 - 8 MHz	f_c - 1.75 f_c	–3% gdm		+3% gdm	ns
Boost Resolution	1.5 to 8 MHz	.25			dB
VOF Filter Output Dynamic Range	THD = 1.5% max, VBP = 0, VO_NORM 1000 pF capacitor across Rx F_Code = 127	1.5			Vppd
VOF Filter Output Dynamic Range	THD = 3.5% max, VBP = 0, VO_DIFF 1000 pF capacitor across Rx F_Code = 127	1.5			Vppd

ELECTRICAL SPECIFICATIONS (continued)

Filter Characteristics (continued)

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
RIN Filter Diff Input Resistance		3.0			kΩ
CIN Filter Input Capacitance				7	pF
EOUT Output Noise Voltage (VO_NORM)	BW = 100 MHz, 0 dB Boost 50Ω input ƒc = 8 MHz 10 dB Boost		1.8 2.35	3 4	mVRms mVRms
EOUT Output Noise Voltage (VO_DIFF)	BW = 100 MHz, 0 dB Boost 50Ω input ƒc = 8 MHz 10 dB Boost		4.2 5.85	6 9	mVRms mVRms
IO- Filter Output Sink Current		1.0			mA
IO+ Filter Output Source Current		3.0			mA
RO Filter Output Resistance (Single ended)	Output source current, IO+ = 1 mA			60	Ω
TC Period, SCLK		100			ns
T1 SDEN Setup to SCLK Falls		10		TC/2-10	ns
T2A SDEN Hold wrt SCLK Falls		10		TC/4	ns
T2B SDEN Falls prior to SCLK Rises		25			ns
T3 SDI Setup to SCLK Falls		25			ns
T4 SDI Hold to SCLK Falls		25			ns
Power Supply Rejection Ratio	100 mVpp @ 5 MHz on VCA, VCD	40	70		dB
Common Mode Rejection Ratio	Vin = 0 VDC + 100 mVpp @5 MHz	30	50		dB
Bias: Vin+, Vin-	VCC = 5V	2.5	2.9	3.3	V
VO_NORM+, VO_NORM–	VCC = 5V	2.8	3.2	3.6	V
VO_DIFF+, VO_DIFF-	VCC = 5V	2.8	3.2	3.6	V
Output offset Normal and Differentiated		 -150		 +150	 mV

TABLE 2: Calculations

Typical change in f-3 dB point with boost

Boost (dB)	Gain@fc (dB)	Gain@ peak (dB)	$f$peak/fc	f-3dB/fc	K
0	-3	0.00	no peak	1.00	0
1	-2	0.00	no peak	1.21	0.16
2	-1	0.00	no peak	1.51	0.34
3	0	0.15	0.70	1.80	0.54
4	1	0.99	1.05	2.04	0.77
5	2	2.15	1.23	2.20	1.03
6	3	3.41	1.33	2.33	1.31
7	4	4.68	1.38	2.43	1.63
8	5	5.94	1.43	2.51	1.97
9	6	7.18	1.46	2.59	2.40
10	7	8.40	1.48	2.66	2.85

Notes: 1. fc is the original programmed cutoff frequency with no boost

2. f-3 dB is the new -3 dB value with boost implemented

3. $f$peak is the frequency where the amplitude reaches its maximum value with boost implemented

i.e., fc = 2 MHz when boost = 0 dB

if boost is programmed to 5 dB then f-3 dB = 4.40 MHz

$f$peak = 2.46 MHz

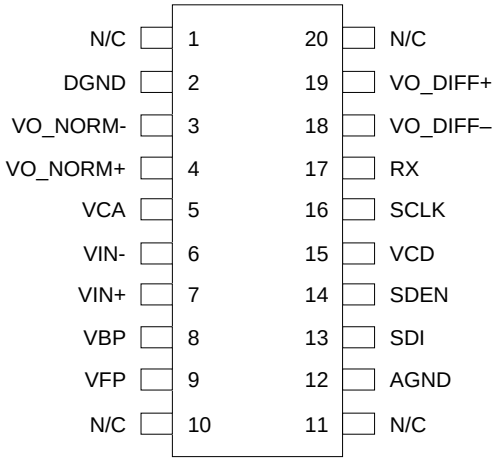
SSI 32F8120
Low-Power Programmable Electronic Filter

PACKAGE PIN DESIGNATIONS

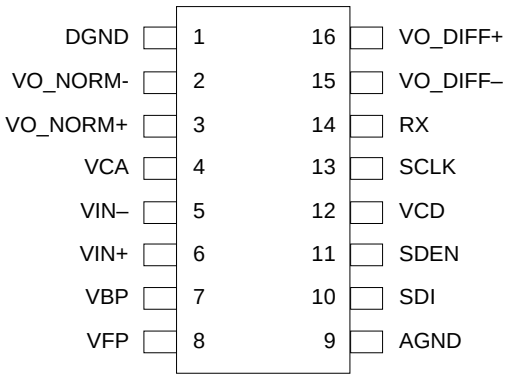
(Top View)

THERMAL CHARACTERISTICS: θja

16-lead SOL	100° C/W
20-lead SOV	125° C/W



20-Lead SOV



16-Lead SOL

CAUTION: Use handling procedures necessary for a static sensitive component.

ORDERING INFORMATION

PART DESCRIPTION		ORDER NUMBER	PACKAGE MARK
SSI 32F8120	16-Lead SOL	32F8120-CL	32F8120-CL
	20-Lead SOV	32F8120-CV	32F8120-CV

Silicon Systems, Inc., 14351 Myford Road, Tustin, CA 92680-7022 (714) 573-6000, FAX 714/573-6914

Patent No. 5,063,309, Patent Pending 823,067

0194 - rev.

SSI 32F8130/8131
Low-Power Programmable Electronic Filter

January 1996

DESCRIPTION

The SSI 32F8130/8131 Programmable Electronic Filters are digitally controlled low pass filters with a normal low pass output and a time differentiated low pass output. The low pass filter is of a 7-pole / 2-zero 0.05° phase equiripple type, with flat group delay response beyond the passband.

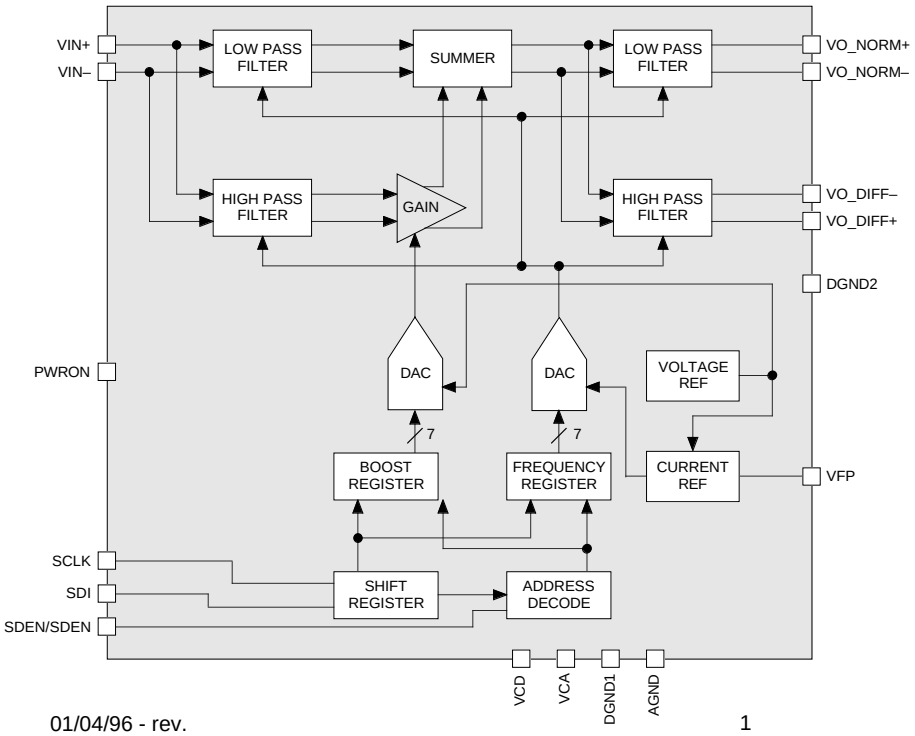
The SSI 32F8130/8131 bandwidth and boost are controlled by two on-chip 7-bit DACs, which are programmed via a 3-line serial interface. The SSI 32F8130 filter bandwidth is programmable from 285 kHz to 2.2 MHz. The SSI 32F8131 is programmable from 150 kHz to 1.4 MHz. The boost is programmable from 0 to 10 dB. Because the boost function is implemented as two zeros on the real axis with opposite sign, the flat group delay characteristic is not affected by the boost programming.

The SSI 32F8130/8131 are ideal for multi-rate, equalization applications. They require only a +5V supply and have a power down mode for minimal idle dissipation. The SSI 32F8130/8131 is available in a 16-lead SOL package.

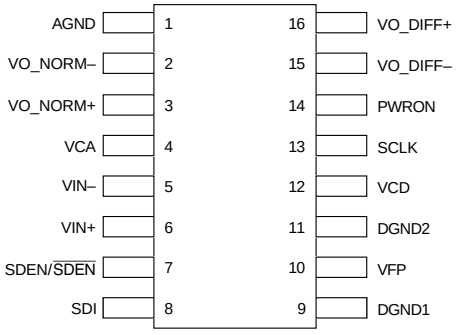
FEATURES

- **Programmable filter cutoff frequency (SSI 32F8130: f_c = 0.285 to 2.2 MHz, SSI 32F8131: f_c = 0.15 to 1.4 MHz) with no external components, serial data connections to minimize pin count**
- **Power down mode (<5 mW)**
- **Programmable pulse slimming equalization (0 to 10 dB boost at the filter cutoff frequency)**
- **Matched normal and differentiated low-pass outputs**
- **Differential filter inputs and outputs**
- **Programming via internal 7-bit DACs**
- **No external filter components required**
- **+5V only operation**
- **Supports constant density recording**

BLOCK DIAGRAM



PIN DIAGRAM



16-Lead SOL

SSI 32F8130: Lead 7 = SDEN
SSI 32F8131: Lead 7 = $\overline{\text{SDEN}}$

CAUTION: Use handling procedures necessary for a static sensitive component.

FUNCTIONAL DESCRIPTION

The SSI 32F8130/8131, a high performance programmable electronic filter, provides a 7-pole / 2-zero 0.05° equiripple linear phase low pass function with matched normal and time differentiated outputs. The device includes multiple biquads and first-order sections to accomplish the filter function, two 7-bit DACs for bandwidth and boost controls, a 3-line serial interface, and complete bias reference circuits. Only one external precision 8.25 kΩ resistor should be connected from the VFP pin to ground for operation. See Figure 1.

SERIAL INTERFACE

The SSI 32F8130/8131 allows easy digital controls of filter bandwidth and magnitude equalization via a 3-line serial interface. The three pins are SDI, SDEN and SCLK. SDI is the serial data input to an internal 8-bit shift register. SDEN is the shift register enable. SCLK is the shift register clock. Besides the 8-bit shift register which accepts data from the SDI input, there are four 4-bit registers which hold the filter bandwidth and boost controls. Two 4-bit registers are assigned to each control function, because a 7-bit binary control is required for each function.

The S-MSB register, whose address code is X000, holds the 3 MSBs of the boost control. The S-LSB register, whose address code is X001, holds the 4 LSBs of the boost control. The F-MSB register, whose address code is X010, holds the 4 MSBs of the cutoff frequency control. The F-LSB register, whose address code is X011, holds the 4 LSBs of the cutoff frequency control.

The serial interface consists of data packets, which are structured as 4-bit address decode followed by 4-bit data. Figure 2 shows the serial interface timing to successfully program the SSI 32F8130/8131.

CUTOFF FREQUENCY PROGRAMMING

The cutoff frequency, f_c, is defined as the -3 dB bandwidth with no magnitude equalization applied, and is programmable from 285 kHz to 2.2 MHz for SSI 32F8130, and 150 kHz to 1.4 MHz for SSI 32F8131. While the f_c is controlled by an on-chip 7-bit DAC, the cutoff frequency resolution is better than 20-kHz step.

Let F_Code be the decimal equivalent of the 7-bit control. The cutoff frequency can be determined by the following equations:

SSI 32F8130 f_c (kHz) = 16.73 • F_Code + 84

SSI 32F8131 f_c (kHz) = 10.81 • F_Code + 37

where $12 \leq F\_Code \leq 127$.

MAGNITUDE EQUALIZATION PROGRAMMING

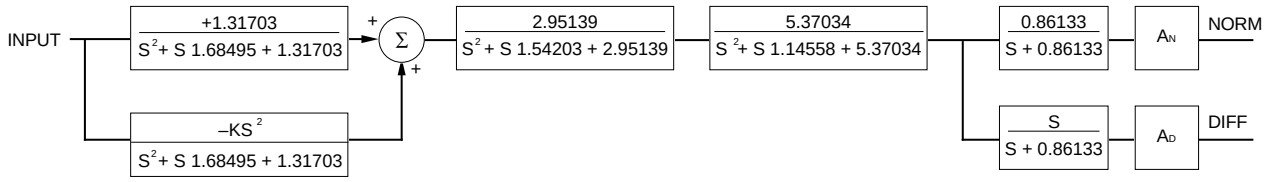
The magnitude equalization, measured in dB, is the amount of high frequency peaking at the cutoff frequency relative to the original -3 dB point. For example, when 10 dB boost is applied, the magnitude response peaks up 7 dB above the DC gain. This equalization function is also controlled by an on-chip 7-bit DAC.

Let S_Code be the decimal equivalent of the 7-bit control. The magnitude equalization can be determined by the equation:

Boost (dB) = $20 \cdot \log_{10} [0.0145 \cdot S\_Code + 1]$ for 32F8130

Boost (dB) = $20 \cdot \log_{10} [0.01703 \cdot S\_Code + 1]$ for 32F8131

where $0 \leq S\_Code \leq 127$.



Normalized for wc = (2π) fc = 1
AN and AD are adjusted for unity gain (0 dB) at F = 0.67 fc
Denormalize the frequency by substituting S → (S/2π fc)
Eq for fc = 2.5 MHz, S = S / [(2π) (2.5 • 10^6)] = S / (1.57080 • 10^7)

$$K = 1.31703(10^{\frac{Boost(dB)}{20}} - 1)$$

FIGURE 1: Normalized Transfer Function of the SSI 32F8130/8131

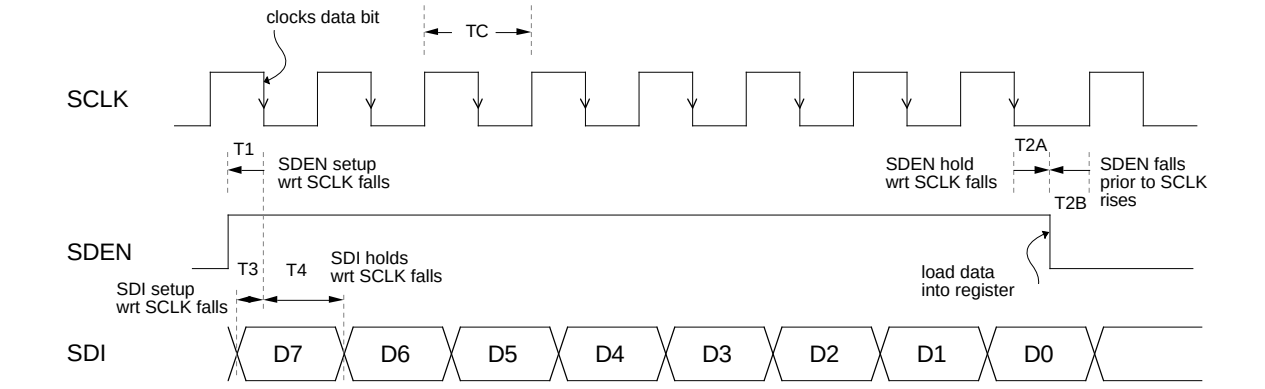


FIGURE 2: Serial Port Timing Relationship

Note:
The serial data enable function of the SSI 32F8130 and that of the SSI 32F8131 are of opposite polarity.

TABLE 1: Data Packet Fields

	ADDRESS BITS				USAGE	DATA BITS			
	D7	**D6**	**D5**	**D4**		**D3**	**D2**	**D1**	**D0**
R0	X	0	0	0	S - MSB REGISTER	X	S6	S5	S4
R1	X	0	0	1	S - LSB REGISTER	S3	S2	S1	S0
R2	X	0	1	0	F - MSB REGISTER	X	F6	F5	F4
R3	X	0	1	1	F - LSB REGISTER	F3	F2	F1	F0

X = Don't care bit.

PIN DESCRIPTION

NAME	DESCRIPTION
VIN+, VIN–	DIFFERENTIAL FILTER INPUTS. The input signals must be AC coupled to these pins.
VO_NORM+, VO_NORM–	DIFFERENTIAL NORMAL OUTPUTS. The output signals must be AC coupled to the load.
VO_DIFF+ VO_DIFF–	DIFFERENTIAL DIFFERENTIATED OUTPUTS. These outputs should be AC coupled to the load.
PWR_ON	POWER ON. A TTL high logic level enables the chip. A low level or open circuit puts the chip into a low power state.
$\overline{\text{SDEN}}$ (8130) $\overline{\text{SDEN}}$ (8131)	SERIAL DATA ENABLE. An active level allows SCLK to clock data into the shift register via the SDI input. An inactive level latches the register data and issues the information to the appropriate circuitry. Active level for SSI 32F8130 is HIGH, for SSI 32F8131 is LOW.
SCLK	SERIAL CLOCK. Negative edge triggered clock input for serial register.
SDI	SERIAL DATA INPUT.
VCA	ANALOG +5 VOLT SUPPLY.
VCD	DIGITAL +5 VOLT SUPPLY.
AGND	ANALOG GROUND.
DGND1 DGND2	DIGITAL GROUND.
VFP	CUTOFF FREQUENCY PROGRAMMING REFERENCE. A resistor of 8.25 kΩ should be connected between this pin and AGND.

ELECTRICAL SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Operation above maximum ratings may permanently damage the device.

PARAMETER	RATING
Storage Temperature	-65 to +150°C
Junction Operating Temperature, Tj	+130°C
Supply Voltage, VCC	-0.5 to 7V
Voltage Applied to Inputs*	-0.5 to VCCV
T1 Lead Temperature (1/16" from case for 10 seconds)	260°C

* Analog input signals of this magnitude shall not cause any change or degradation in filter performance after signal has returned to normal operating range.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	RATING
Supply voltage, VCC	4.50 < VCC < 5.50V
Ambient Temperature	0 < Ta < 70°C
Tj Junction Temperature	0 < Tj < 130°C

ELECTRICAL CHARACTERISTICS

Unless otherwise specified recommended operating conditions apply. F_Code = 64, S_Code = 0.

PARAMETER		CONDITIONS		MIN	NOM	MAX	UNIT
Idle Mode Current						1	mA
Isupply					60	70	mA
Power Dissipation		PWR_ON ≤ 0.8V				6	mW
		PWR_ON ≥ 2.0V			303	385	mW
Idle to Active Mode Recovery Time						50	µs
Serial port program to output response time						50	µs
DC Characteristics							
VIH	High Level Input Voltage	TTL input		2			V
VIL	Low Level Input Voltage					0.8	V
IIH	High Level Input Current	VIH = 2.7V				25	µA
IIL	Low Level Input Current	VIL = 0.4V		-1.5			mA
Filter Characteristics							
fc	Filter Cutoff Frequency	12 < F_Code < 127					
		SSI 32F8130		0.285		2.2	MHz
		SSI 32F8131		0.15		1.4	MHz
FCA	Filter fc Accuracy	over fc range	32F8130	-12		+12	%
			32F8131	-10		+10	%
Cutoff Resolution		$\text{Resolution} = \frac{\text{Max } fc}{127}$	32F8130		17		kHz
			32F8131		11		kHz
AO	VO_NORM Diff Gain	F = 0.67 fc	32F8130	0.7		1.1	V/V
			32F8131	0.8		1.2	V/V
AD	VO_DIFF Diff Gain	F = 0.67fc	32F8130	0.8 AO		1.15 AO	V/V
			32F8131	1.0 AO		1.2 AO	V/V
FB	Frequency Boost at fc (32F8130)	FB(dB) = 20 log [0.0145 • S_Code + 1] 0 ≤ S_Code ≤ 127		0		9	dB
	(32F8131)	FB(dB) = 20 log [0.0173 • S_Code + 1] 0 ≤ S_Code ≤ 127		0		10	dB
FBA	Frequency Boost Accuracy	S_Code = 127		-1.5		+1.5	dB
TGD0	Group Delay Variation Without Boost	0.2 fc to fc	32F8130	-2.5		+2.5	%
			32F8131	-2		+2	%
		fc to 1.75 fc		-3		+3	%
TGDB	Group Delay Variation With Boost	0.2 fc to fc	32F8130	-2.5		+2.5	%
			32F8131	-2		+2	%
		fc to 1.75 fc		-3		+3	%
Boost Resolution				0.25			dB
VOF_N	Filter Output Dynamic Range	THD = 1% max, Normal Output		1			Vp-p

ELECTRICAL CHARACTERISTICS (continued)
Unless otherwise specified recommended operating conditions apply. F_Code = 64, S_Code = 0.

PARAMETER		CONDITIONS		MIN	NOM	MAX	UNIT
Filter Characteristics (continued)							
VOF_D	Filter Output Dynamic Range	THD = 1% max, Differentiated Output		1			Vp-p
RIN	Filter Diff Input Resistance			3.0	4.0	5.0	kΩ
CIN	Filter Input Capacitance				3.0		pF
EOUT	Output Noise Voltage (VO_NORM)	BW = 100 MHz, 50Ω input fc = Max fc	0 dB Boost		1.2	1.9	mVRms
			max Boost		1.4	2.0	mVRms
EOUT	Output Noise Voltage (VO_DIFF)	BW = 100 MHz, 50Ω input fc = Max fc	0 dB Boost		2.1	2.7	mVRms
			max Boost		2.5	3.4	mVRms
IO–	Filter Output Sink Current			1.0			mA
IO+	Filter Output Source Current			3.0			mA
RO	Filter Output Resistance (Single ended)	Output source current, IO+ = 1 mA			50	70	Ω
T1 SDEN Set-up WRT SCLK Falls				10		TC/2-10	ns
T2A SDEN Hold WRT SCLK Falls				10		TC/4	ns
T2B SDEN Falls (rises for 8131) prior to SCLK rises				25			ns
T3 SDI Set-up WRT SCLK Falls				25			ns
T4 SDI Hold WRT SCLK Falls				25			ns
SCLK Period, TC				100			ns
Power Supply Rejection Ratio VO_NORM		100 mVp-p from 10 kHz to 10 MHz on VCA, VCD		30	40		dB
Power Supply Rejection Ratio VO_DIFF				20	30		dB
Common Mode Rejection Ratio VO_NORM		Vin = 0VDC + 10 mVp-p from 10 kHz to 10 MHz		30	40		dB
Common Mode Rejection Ratio VO_DIFF				20	30		dB
Bias:	VO_NORM±	VCC = 5V		2.40	2.75	3.10	V
	Vin±			2.20	2.35	2.80	V
	VO_DIFF±			2.40	2.75	3.10	V
Normal Output Offset Variation		F_Code switched from 12-127		-200		200	mV
Differentiated Output Offset Variation		F_Code switched from 12-127		-200		200	mV

TABLE 1: Calculations (Typical change in f-3 dB point with boost)

Boost (dB)	Gain@fc (dB)	Gain@ peak (dB)	$f$peak/fc	f-3dB/fc	K
0	-3	0.00	no peak	1.00	0
1	-2	0.00	no peak	1.21	0.16
2	-1	0.00	no peak	1.51	0.34
3	0	0.15	0.70	1.80	0.54
4	1	0.99	1.05	2.04	0.77
5	2	2.15	1.23	2.20	1.03
6	3	3.41	1.33	2.33	1.31
7	4	4.68	1.38	2.43	1.63
8	5	5.94	1.43	2.51	1.97
9	6	7.18	1.46	2.59	2.40
10	7	8.40	1.48	2.66	2.85

Notes: 1. fc is the original programmed cutoff frequency with no boost

2. f-3 dB is the new -3 dB value with boost implemented

3. $f$peak is the frequency where the amplitude reaches its maximum value with boost implemented

i.e., fc = 1 MHz when boost = 0 dB

if boost is programmed to 5 dB then f-3 dB = 2.20 MHz

$f$peak = 1.23 MHz

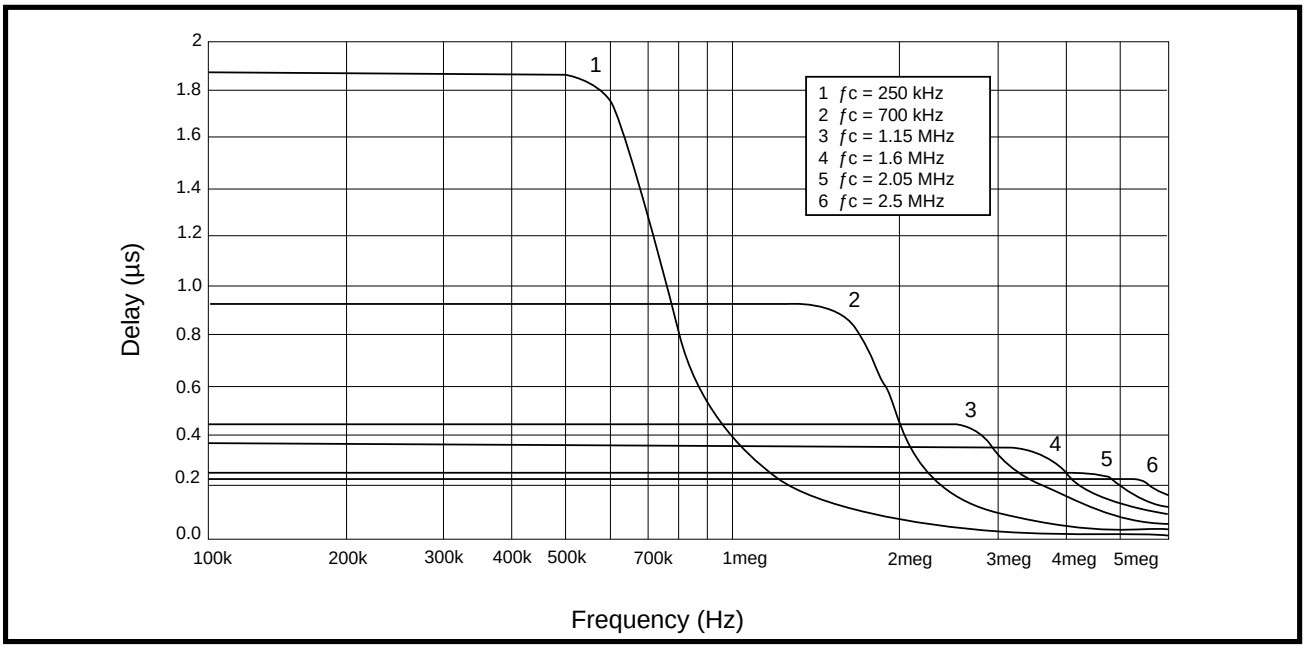


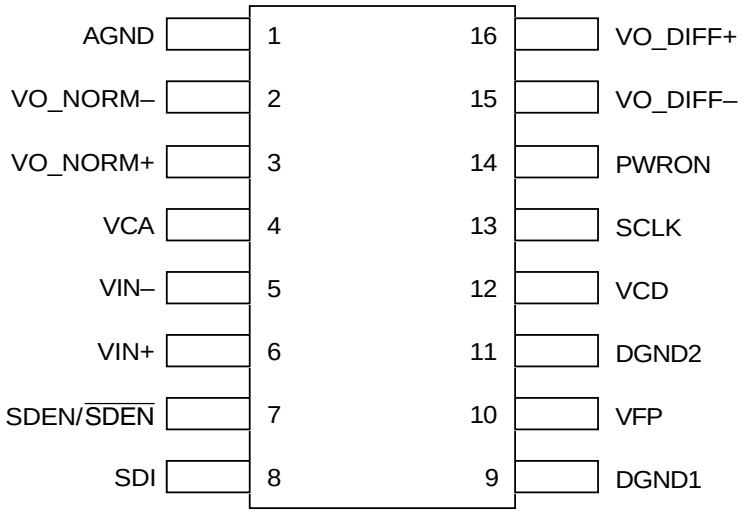
FIGURE 3: Typical Normal/Differentiated Output Group Delay Response

SSI 32F8130/8131
Low-Power Programmable Electronic Filter

PACKAGE PIN DESIGNATIONS
(Top View)

THERMAL CHARACTERISTICS: θjA

16-Lead SOL	100° C/W



16-Lead SOL

SSI 32F8130: Lead 7 = $\overline{\text{SDEN}}$
SSI 32F8131: Lead 7 = $\overline{\text{SDEN}}$

CAUTION: Use handling procedures necessary for a static sensitive component.

ORDERING INFORMATION

PART DESCRIPTION	ORDER NO.	PKG. MARK
SSI 32F8130 16-Lead SOL	32F8130-CL	32F8130-CL
SSI 32F8131 16-Lead SOL	32F8131-CL	32F8131-CL

Silicon Systems, Inc., 14351 Myford Road, Tustin, CA 92680-7022 (714) 573-6000, FAX (714) 573-6914

01/04/96 - rev.

silicon systems®
A TDK Group Company

SSI 32F8144
Programmable Electronic Filter

January 1996

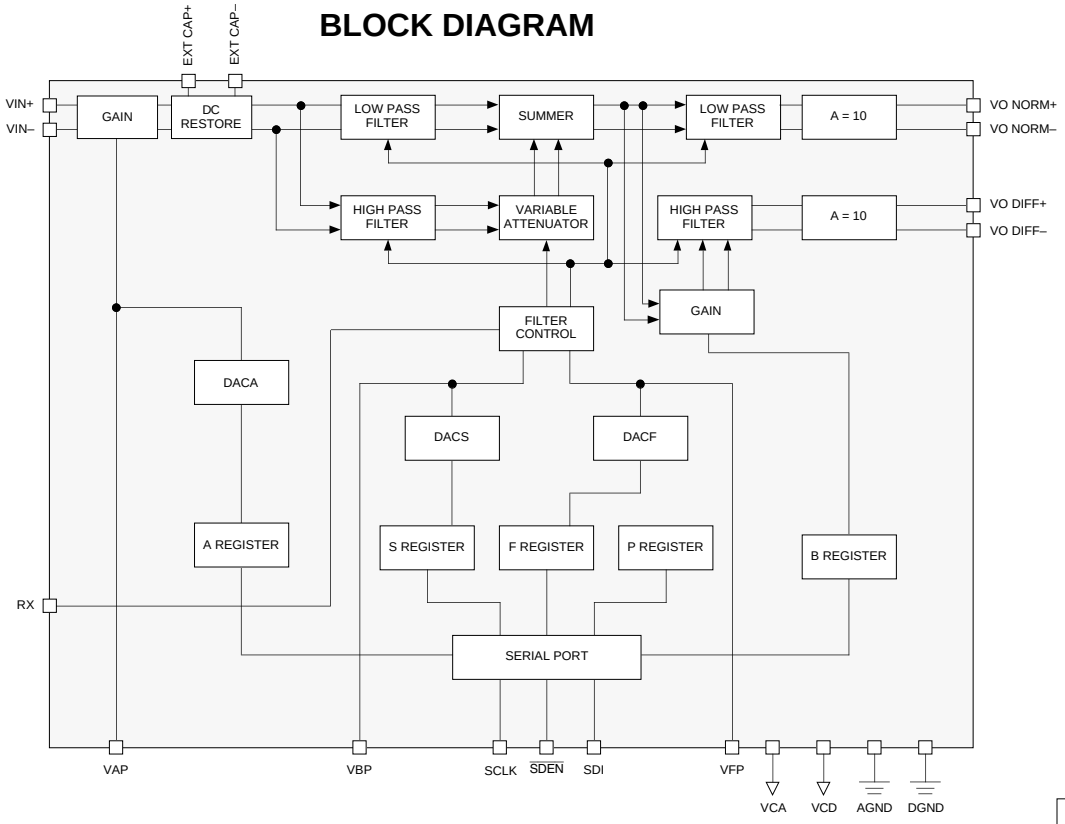
DESCRIPTION

This custom integrated circuit incorporates a pulse equalizer of variable equalization and variable bandwidth with a transfer function of a 2 zero/7 pole linear phase filter, as well as variable gain stages controlled by DACs. Equalization, gain and bandwidth changes are user-programmable via three serial lines to a microprocessor. The equalizer is totally contained and calibrating. It is realized in a high speed fully differential mode. A seven pole linear phase equiripple ± 0.05 degree filter forms the low-pass function. The cutoff frequency of the low-pass section is programmed via a 7-bit serial shift register and can be programmed from 7 to 27 MHz. Pulse slimming equalization uses two programmable magnitude, opposite sign zeroes on the real axis. Pulse slimming boost is from 0 to 9.5 dB at the filter cutoff frequency using a 7 bit serial shift register. Gain can be programmed from 10 V/V to 100 V/V for normal outputs and from 10 V/V to 50 V/V for differentiated outputs.

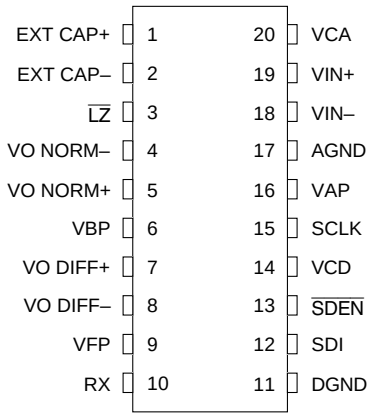
FEATURES

- **Programmable filter cutoff frequency (7 MHz ≤ f_c ≤ 27 MHz) with no external components**
- **± 10% cutoff frequency accuracy**
- **Programmable pulse slimming equalization (0 to 9.5 dB boost at the filter cutoff frequency)**
- **Matched delay normal and differentiated low-pass outputs**
- **Differential filter inputs and outputs**
- **Device idle mode (45 mW nom.)**
- **+5V only operation**
- **Supports constant density recording**
- **Input stage gain control with DAC**
- **Relative gain between normal and differentiated outputs controlled with serial port**

BLOCK DIAGRAM



PIN DIAGRAM



20-lead SOL

CAUTION: Use handling procedures necessary for a static sensitive component.

FUNCTIONAL DESCRIPTION

The SSI 32F8144, a high performance programmable electronic filter, provides a low pass equiripple type seven pole filter with matched normal and differentiated outputs with variable gain using DACs.

The SSI 32F8144 has seven control registers: A, B, S1, S2, F1, F2 and P registers. Register A contains four bits, B is three bits, and P is one bit. S1, S2, F1, and F2 contain seven bits. Register A controls the gain of the input stage and register B controls the gain between the normal and differentiated outputs. Since the F, S registers contain 7 bits, they require two data packets which must be loaded sequentially. S1-2 registers are for high frequency boost. F1-2 registers are for cutoff frequency control. The P register is for power down command. The structure and command of each register are described as follows.

Data is loaded serially with MSB first. Each data packet contains 8 bits. The first four bits (D7 - D4) are designated as address bits with D7 always a "don't care." The last four bits (D3 - D0) are the data bits (see Table 1).

The registers are loaded by using the serial port through the SDI, $\overline{\text{SDEN}}$ and SCLK pins. The SDI pin is the serial bit input. The $\overline{\text{SDEN}}$ pin is the control register enable. The SCLK is the control register clock. The packet is transmitted MSB (D7) first.

GAIN PROGRAMMING

The input gain stage is programmed with register A (Register 4, R4). The A_Code programs this gain as follows:

$$Av(V/V) = 10 \bullet \frac{A\_Code}{15}$$

$$1 \le A\_Code \le 15$$

This input gain stage is DC coupled to the filter core through DC restore circuitry. A large capacitor (1 µF) is placed between pins EXT_CAP+ and EXT_CAP- to null the input offset to the filter. Register B (Register 5, R5) controls the relative gain between the normal and differentiated outputs. There are three discrete options which are listed as follows:

AN/AD = 1.0 B_Code = 3 (B2 = 0, B1 = 1, B0 = 1)

$1 \le A\_Code \le 7$

AN/AD = 1.5 B_Code = 5 (B2 = 1, B1 = 0, B0 = 1)

$1 \le A\_Code \le 11$

AN/AD = 2.0 B_Code = 6 (B2 = 1, B1 = 1, B0 = 0)

$1 \le A\_Code \le 15$ (B3 is a "don't care")

CUTOFF FREQUENCY PROGRAMMING

The filter cutoff frequency can be set from 7 to 27 MHz. The 7-bit F_Code programs the cutoff frequency as follows:

$$fc(MHz) = 27 \bullet \frac{F\_Code}{127} \qquad 33 \le F\_Code \le 127$$

SLIMMER HIGH FREQUENCY BOOST PROGRAMMING

The amplitude of the input signal at frequencies near the cutoff frequency can be increased using this feature. By controlling the DACS output, the boost can be determined. The amount of boost at the cutoff frequency is related to the DACS output by the following formula:

BOOST (dB) = 20 • log [0.01563(S_Code) +1].

The 7-bit S_Code is loaded into S1 and S2 registers (registers 0 and 1 - R0, R1).

POWER-DOWN CONTROL

The D0 bit of the P register (register 7, R7) determies the power up/down state of the SSI 32F8144. Upon initial power up, the D0 bit of the P register should be initialized to "1" for normal operation. D3 - D1 are "don't care."

By programming D0 to "0," the SSI 32F8144 is switched into a power-down state, dissipating minimum idle power. The filter is switched off. The serial port remains active awaiting the next command.

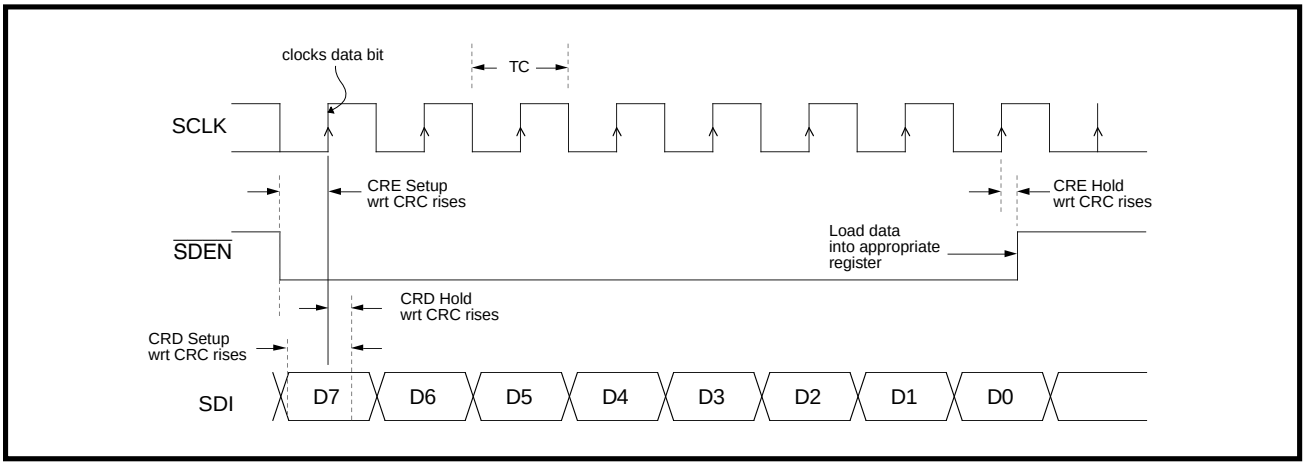


FIGURE 1: Serial Port Timing Relationship

TABLE 1: Control Register Assignment

ADDRESS BITS					USAGE	DATA BITS			
	D7	D6	D5	D4		D3	D2	D1	D0
R0	X	0	0	0	S1 REGISTER	X	S6	S5	S4
R1	X	0	0	1	S2 REGISTER	S3	S2	S1	S0
R2	X	0	1	0	F1 REGISTER	X	F6	F5	F4
R3	X	0	1	1	F2 REGISTER	F3	F2	F1	F0
R4	X	1	0	0	A REGISTER	A3	A2	A1	A0
R5	X	1	0	1	B REGISTER	X	B2	B1	B0
R7	X	1	1	1	P REGISTER	X	X	X	P0

X = Don’t Care
S = Boost (Slimming) Control
F = Frequency (Bandwidth) Control
A = Gain Setting (0-10)
B = Gain of VO_DIFF relative to the gain of VO_NORM
P = Sleep Mode Control (P0 = 1, On Mode; P0 = 0, Sleep Mode)

SDI is the serial data input for an 8-bit control shift register. The data packet is transmitted Most Significant Bit (D7) first. The first four bits are the register address, the last four are the data bits. Registers larger than four bits must be loaded with two 8-bit data packets. These packets should be loaded sequentially.

PIN DESCRIPTION

NAME	DESCRIPTION
VIN+, VIN-	DIFFERENTIAL SIGNAL INPUTS
VO_NORM+, VO_NORM-	DIFFERENTIAL NORMAL OUTPUTS
VO_DIFF+ VO_DIFF-	DIFFERENTIAL DIFFERENTIATED OUTPUTS
$\overline{\text{SDEN}}$	CONTROL REGISTER ENABLE. A logic LOW level allows CONTROL REGISTER CLOCK to clock data into the control register via the CONTROL REGISTER DATA input. A logic HIGH level latches the register data and issues the information to the appropriate circuitry. This is a TTL input.
SCLK	CONTROL REGISTER CLOCK. Positive edge triggered clock input for serial register. This is a TTL input.
SDI	CONTROL REGISTER DATA. This is a TTL input (see Figure 1).
RX	CURRENT SET RESISTOR. This external resistor to ground provides a reference current. (RX = 5 kΩ ±1%) A 1000 pF capacitor must be connected in parallel with Rx.
VCA	ANALOG +5V SUPPLY.
VCD	DIGITAL +5V SUPPLY.
AGND	ANALOG GROUND.
DGND	DIGITAL GROUND.
VAP	ANALOG TO DIGITAL TEST VOLTAGE. This is an analog voltage that is proportional to the setting on the digital output on the A/D convertor. This is a test pin related to the variable gain.
VBP	BOOST PROGRAMMING VOLTAGE. A voltage that is related to the boost. A test pin.
VFP	CUTOFF FREQUENCY PROGRAMMING VOLTAGE. A voltage that is related to the cutoff frequency. A test pin.
EXT CAP+ EXT CAP-	EXTERNAL CAPACITOR. These pins are available for an external capacitor which is used in a feedback network to null the input offset. $C_{EXT} \geq 0.47\ \mu F$, 1.0 μF nominal.
$\overline{\text{LZ}}$	LOW IMPEDANCE. This is a control signal which causes the input impedance of the filter to be low when this pin is low. The impedance is high if the pin is open or in the high state. This is a TTL input.

ELECTRICAL SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Operation above maximum ratings may damage the device.

PARAMETER	RATINGS
Storage Temperature	-65 to +150°C
Junction Operating Temperature, Tj	+130°C
Supply Voltage, VCC	-0.5 to 7V
Voltage Applied to Inputs*	-0.5 to VCCV
Maximum Power Dissipation, fc = 27 MHz, Vcc = 5.5V	.55W
T1 Lead Temperature (1/16" from case for 10 seconds)	260°C

* Analog input signals of this magnitude shall not cause any change or degradation in filter performance after signal has returned to normal operating range.

RECOMMENDED OPERATING CONDITIONS

Supply voltage, VCC	4.50 < VCC < 5.50 V
Ambient Temperature	0 < Ta < 70°C
Tj Junction Temperature	0 < Tj < 130°C

ELECTRICAL CHARACTERISTICS

Unless otherwise specified recommended operating conditions apply.

PARAMETER		CONDITION	MIN	NOM	MAX	UNIT
Idle Mode Current		P0 = “0”		11	15	mA
Supply Current		Vcc = 5.5V		85	100	mA
PD	Power Dissipation	P0 = “0”		45	71.5	mW
		P0 = “1”		400	550	mW
Idle to Active Mode Recovery Time					50	µs
Serial port program to output response time					50	µs
DC Characteristics						
VIH	High Level Input Voltage	TTL input	2.0			V
VIL	Low Level Input Voltage				0.8	V
IIH	High Level Input Current	VIH = 2.7V			20	µA
IIL	Low Level Input Current	VIL = 0.4V			–1.5	mA
Filter Characteristics						
fc	Filter Cutoff Frequency	33 ≤ F_Code ≤ 127	7		27	MHz

ELECTRICAL CHARACTERISTICS (continued)

Unless otherwise specified recommended operating conditions apply.

PARAMETER		CONDITION	MIN	NOM	MAX	UNIT
FCA	Filter f_c Accuracy	Over full f_c range, $33 \le F\_Code \le 127$	-10		10	%
AO	VO_NORM Diff Gain (Note)	F = 0.67 f_c	10		100	V/V
AD	VO_DIFF Diff Gain (Note)	F = 0.67 f_c, set with serial port	10		50	V/V
VO_NORM Gain Tolerance		A_O = 100	-15		15	%
VO_DIFF Gain Tolerance		A_D = 50	-15		15	%
FB	Frequency Boost at f_c	FB(dB) = 20 log [.01563 (S_Code) +1]	0		9.5	dB
FBA	Frequency Boost Accuracy	0 to 9.5 dB	–1.25		+1.25	dB
TGD0	Group Delay Variation Without Boost	0.2 f_c - f_c	–2% gdm		+2% gdm	ns
	gdm = group delay magnitude	f_c - 1.75 f_c	–3% gdm		+3% gdm	ns
TGDB	Group Delay Variation With Boost	0.2 f_c - f_c	–2% gdm		+2% gdm	ns
		f_c - 1.75 f_c	–3% gdm		+3% gdm	ns
VOF	Filter Output Dynamic Range	Vo_NORM, T_{HD} = 1.5%	1			Vp-p
		Vo_DIFF, T_{HD} = 2.0%	1			Vp-p
		Vo_NORM, T_{HD} = 2.0%	1.5			Vp-p
		Vo_DIFF, T_{HD} = 3.0%	1.5			Vp-p
RIN	Filter Diff Input Resistance		3.0	3.5	4.0	kΩ
CIN	Filter Input Capacitance				7	pF
EOUT	Output Noise Voltage (VO_NORM)	BW = 100 MHz, 50Ω input, 0 dB Boost		2.5	4.0	mV rms
		f_c = 27 MHz, 9.5 dB Boost		3.7	10	mV rms
EOUT	Output Noise Voltage (VO_DIFF)	BW = 100 MHz, 50Ω input, 0 dB Boost		4.4	6	mV rms
		f_c = 27 MHz, 9.5 dB Boost		7.8	14	mV rms
IO–	Filter Output Sink Current		1.0			mA
IO+	Filter Output Source Current		3.0			mA
RO	Filter Output Resistance (Single ended)	IO+ = 1 mA		30	50	Ω
$\overline{SCLK}$ Period, TC			100			ns
$\overline{SDEN}$ Set-up WRT $\overline{SCLK}$ Rising Edge			10		25	ns
$\overline{SDEN}$ Hold WRT $\overline{SCLK}$ Rising Edge			5		TC/2-10	ns

Note: The overall gain of VO_DIFF with respect to VIN is 10 to 50 V/V. Additionally, the gain of VO_NORM with respect to VO_DIFF will be adjustable and have gain values of 1.0, 1.5 and 2.0.

ELECTRICAL CHARACTERISTICS (continued)

Unless otherwise specified recommended operating conditions apply.

PARAMETER	CONDITION	MIN	NOM	MAX	UNIT
$\overline{SDEN}$ Rises Prior to $\overline{SCLK}$ Falls		15			ns
SDI Set-up WRT $\overline{SCLK}$ Rising Edge		15			ns
SDI Hold WRT $\overline{SCLK}$ Rising Edge		15			ns
Power Supply Rejection Ratio	100 mVp-p in VCA, VCD from 100 kHz to 10 MHz	45	70		dB
Common Mode Rejection Ratio	VIN = 0 VDC + 100 mVp-p from 100 kHz to 10 MHz	40	65		dB
DC Bias: VO_NORM+, VO_NORM- VO_DIFF+, VO_DIFF-	VCC = 5V, single ended	2.05	2.55	3.05	V
Vin+, Vin-		2.5	3.0	3.5	V
Delay mismatch normal and differentiated outputs				1	ns

TABLE 2: Calculations

Typical change in f-3 dB point with boost

Boost (dB)	Gain@fc (dB)	Gain@ peak (dB)	$f$peak/fc	f-3dB/fc	K
0	-3	0.00	no peak	1.00	0
1	-2	0.00	no peak	1.21	0.16
2	-1	0.00	no peak	1.51	0.34
3	0	0.15	0.70	1.80	0.54
4	1	0.99	1.05	2.04	0.77
5	2	2.15	1.23	2.20	1.03
6	3	3.41	1.33	2.33	1.31
7	4	4.68	1.38	2.43	1.63
8	5	5.94	1.43	2.51	1.97
9	6	7.18	1.46	2.59	2.40
10	7	8.40	1.48	2.66	2.85

Notes: 1. fc is the original programmed cutoff frequency with no boost

2. f-3 dB is the new -3 dB value with boost implemented

3. $f$peak is the frequency where the amplitude reaches its maximum value with boost implemented

e.g., fc = 9 MHz when boost = 0 dB

if boost is programmed to 5 dB then f-3 dB = 19.8 MHz

$f$peak = 11.07 MHz

SSI 32F8144
Programmable
Electronic Filter

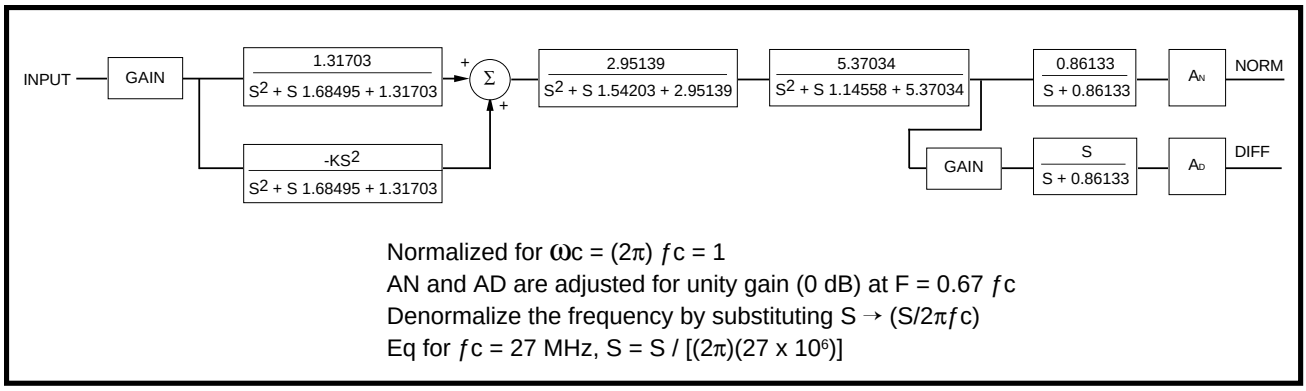


FIGURE 2: 32F8144 Normalized Block Diagram

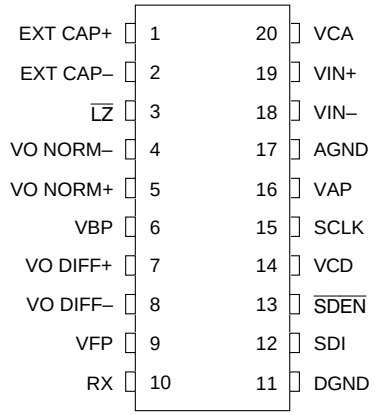
PACKAGE PIN DESIGNATIONS

(Top View)

THERMAL CHARACTERISTICS: θja

20-lead SOL	95°C/W
20-Lead SOV	125°C/W

CAUTION: Use handling procedures necessary for a static sensitive component.



20-lead SOL, SOV

ORDERING INFORMATION

PART DESCRIPTION		ORDERING NUMBER	PACKAGE MARK
SSI 32F8144	20-Lead SOL (300 mil)	32F8144 - CL	32F8144 - CL
SSI 32F8144	20-Lead SOV (220mil)	32F8144 - CV	32F8144 - CV

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01/08/96 - rev.

Section 9

DATA CONVERSION PRODUCTS

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SSI 79W2522
Dual 4-bit ADCs

Advance Information

February 1996

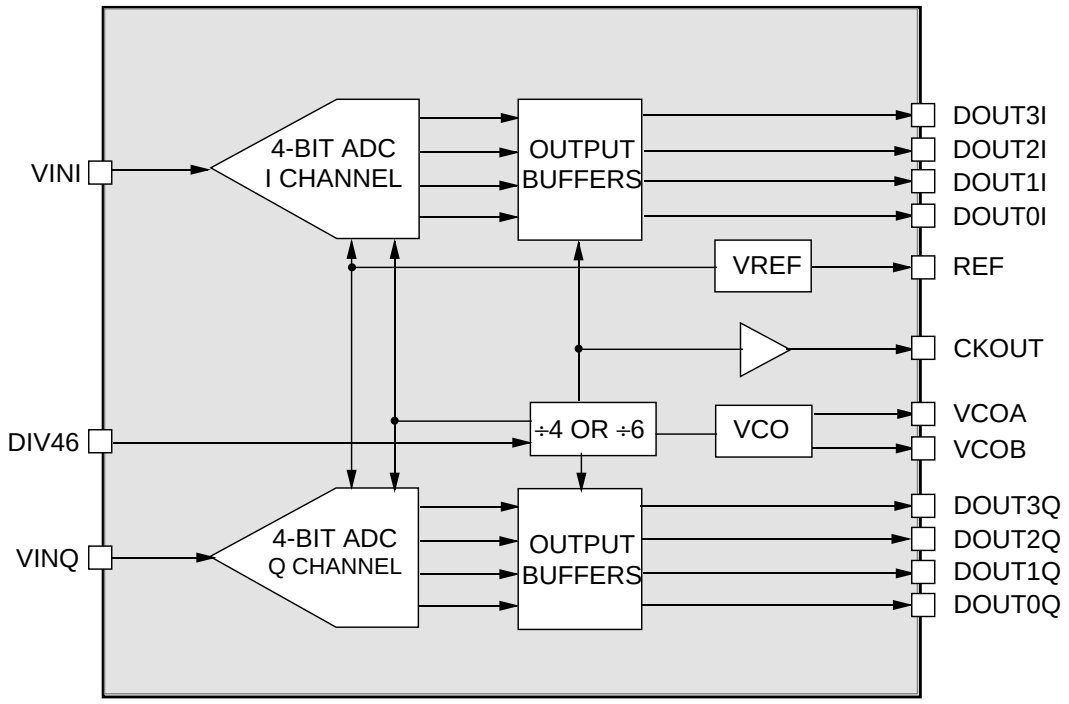
DESCRIPTION

The SSI 79W2522 is a low cost, high performance dual 4-bit (6-bit linearity) analog to digital converter IC with VCO and programmable clock divider. The device supports conversion rates from 20 to 60 M samples per second based on the VCO frequency and the clock divider selection. A typical application for the 79W2522 is analog-to-digital conversion in QPSK demodulation systems that require recovery of multiple baseband frequencies, such as digital satellite receiver boxes.

FEATURES

- **Matched 4-bit flash analog-to-digital converters**
  - **6-bit linearity (0.25 LSB)**
  - **Maximum 1% gain mismatch**
  - **Maximum phase mismatch of 2 degrees**
  - **Internal voltage reference**
- **20 to 60 Msps conversion rates**
- **Internal VCO drive circuitry (requires external LC and phase detector)**
  - **Internal divide-by-4 and divide-by-6 switching**
- **TTL compatible outputs**
- **5 volt operation**
- **28-pin SOL package (optional 28-pin PLCC or 32 pin QFP)**

BLOCK DIAGRAM



FINCTIONAL DESCRIPTION

The 79W2522 contains dual 4-bit flash analog-to-digital converters that are synchronously sampled by an internally generated clock signal. The device accepts two analog input signals within a range of 0 to 1.0 Vp-p that are AC coupled into the VINI and VINQ pins of the device. The device provides two 4-bit parallel outputs that represent the digitized value of the input signals. An internal VCO generates the internal sample clock for the ADCs. The sample clock is also buffered and provided as an external clock signal (CKOUT) for the parrallel data outputs.

ANALOG TO DATA DIGITAL CONVERTERS (ADCs)

The 79W2522 contains two matched 4-bit flash ADCs that support sampling frequencies up to 60 Msps. The input signals to the ADCs are typically AC coupled into pins VINI and VINQ. The input signals are referenced to an internally generated bandgap voltage that is also provided as an output, REF. This output is capable of driving 1 mA into a 1 kΩ load. The ADCs capture samples on the rising edge of the CKOUT signal with the data for that sample being valid on the falling edge of the next clock cycle (reference Figure 2). The 4-bit digitized output data is represented as a Gray code according to the following table:

VCO CLOCK GENERATOR

The internal VCO clock generator consists of a VCO core, output buffering, and a divider circuit that allows the VCO output to te divided either by 4 or 6. The VCO is connected to an external LC tank circuit that controls the ocillation of the VCO over a specified frequency range. The divider circuit allows the VCO to operate over a smaller frequency range while still supporting sample rates from 20 to 60 Msps. Driving the DIVB46 pin high (1) selects a divide-by-4 to support the highest sampling range of 30 to 60 Msps. Driving the DIV46 pin low (0) selects a divide-by-6 to support the lower sampling range of 20 to 40 Msps.

The CKOUT pin is a buffered version of the internal sampling clock. The falling edge of CKOUT is used by external devices to latch the data on the DOUTnl and DOUTnQ pins (reference Figure 2).

ANALOG INPUT	DIGITAL OUTPUT (GRAY CODE)
- (15/2) LSB	0000
- (13/2) LSB	0001
- (11/2) LSB	0011
- (9/2) LSB	0010
- (7/2) LSB	0110
- (5/2) LSB	0111
- (3/2) LSB	0101
- (1/2) LSB	0100
+ (1/2) LSB	1100
+ (3/2) LSB	1101
+ (5/2) LSB	1111
+ (7/2) LSB	1110
+ (9/2) LSB	1010
+ (11/2) LSB	1011
+ (13/2) LSB	1001
+(15/2) LSB	1000

LSB = Input Range/ 16

PIN DESCRIPTION

ANALOG PINS

(Pins marked N/C should be left unconnected during normal use)

NAME	TYPE	DESCRIPTION
VINI	I	I Input. This pin is the analog input to the In-phase ADC (IADC). The input to this pin should be AC coupled.
VINQ	I	Q Input. This pin is the analog input to the Quadrature ADC (QADC). The input to this pin should be AC coupled.
REF	O	Voltage Reference. This pin is an output from the internal voltage reference for the ADCs.
VCOA	I	VCO A. This pin is the input of the VCO. It is connected to an external LC resonator.
VCOB	I	VCO B. This pin is the gain control of the VCO. It is normally left open.
VCOVCC	O	VCO SUPPLY. This pin is the internally generated supply for the VCO. It is connected to an external LC resonator.

DIGITAL PINS

CKOUT	O	Clock Output. This is the output clock for the ADC. Data is clocked out on the rising edge of this output. The falling edge of this output can be used to latch data into an external device.
DIV46	I	Divider Select. This pin selects the divider for the VCO clock output. A low (0) level input selects the divide-by-6 mode. A high (1) level input selects the divide-by-4 mode.
DOUTn1	O	IADC Outputs. These four pins are the digital output of the IADC. They are clocked out on the rising edge of the CKOUT output and should be latched with the falling edge of the CKOUT output.
DOUTnQ	O	QADC Outputs. These four pins are the digital output of the QADC. They are clocked out on the rising edge of the CKOUT output and should be latched with the falling edge of the CKOUToutput.

POWER/GROUND

VPD	-	Digital power. These two pins are the power pins for the digital circuitry.
VND	-	Digital ground. These two pins are the ground pins for the digital circuitry.
VNA	-	Analog ground. These pins are the analog ground for the VCO and ADCs.
VPA	-	Analog power. These pins are the analog power supply for the ADCs.

ELECTRICAL SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Operation beyond the maximum ratings may damage the device

PARAMETER	RATING
Storage temperature	-55 to 150°C
Junction operating temperature	+110°C
Positive supply voltage (Vp)	-0.3 to 6V
Voltage applied to any pin	-0.3V to VPn + 0.3V

TARGET SPECIFICATIONS

Unless otherwise specified: $0^o \leq Ta \leq 70^o$ C; positive power supply (VDn, VAn) = +5.0 V +/-5%.

OPERATING CHARACTERISTICS

PARAMETER	CONDITION	MIN	NOM	MAX	UNIT
Analog supply current				TBD	mA
Digital supply current				TBD	mA
Power supply rejection ratio	TBD	30			dB

DIGITAL I/O CHARACTERISTICS

High level input voltage		2.0		VPD+0.6	V
Low level input voltage		-0.3		0.8	V
High level input current				50	µA
Low level input current				50	µA
High level output voltage	CL = 25 pF	2.4		VPD	V
Low level output voltage	CL = 25 pF	0		0.4	
Output rise time	CKOUT, DOUTnI, DOUTnQ: 0.4V to 2.4V			5	nS
Output fall time	CKOUT, DOUTnI, DOUTnQ: 2.4V to 0.4V			5	nS
Output set up time (Tsu)	DOUTnI, DOUTnQ stable to CKOUT↓	4			nS
Output hold time (Th)	CKOUT ↓ to DOUTnQ, DOUTnI inactive	3			nS
CLK duty cycle		40		60	%

ADC CHARACTERISTICS

PARAMETER	CONDITION	MIN	NOM	MAX	UNIT
Input voltage range	AC coupled input	0.0		1.0	Vp-p
Input overvoltage	AC coupled input			2.5	Vp-p
Input resistance	VINI and VINQ	250			Ω
Input capacitance	VINI and VINQ			10	pF
Sampling frequency	VCO clock 150 to 240 MHz	20		60	Msps
Effective number of bits		3.8			bits
ADC Offset error				0.25	LSB
Linearity	Differential			0.25	LSB
	Integral			0.25	LSB
Gain mismatch	VINI=VINQ			1	%
Gain error				5	%
Phase mismatch	VINI=VINQ			2	°
ADC crosstalk	VINI=1.0 Vp-p, 29 MHz;			-40	dB
	VINQ=1.0 Vp-p, 23 MHz				
	VINQ=1.0 Vp-p, 25 MHz;			-40	dB
	VINI=1.0 Vp-p, 29 MHz				
REF output voltage	VREF loaded with 1 kΩ; I_{VREF} = 1 mA	1.14	1.20	1.26	V

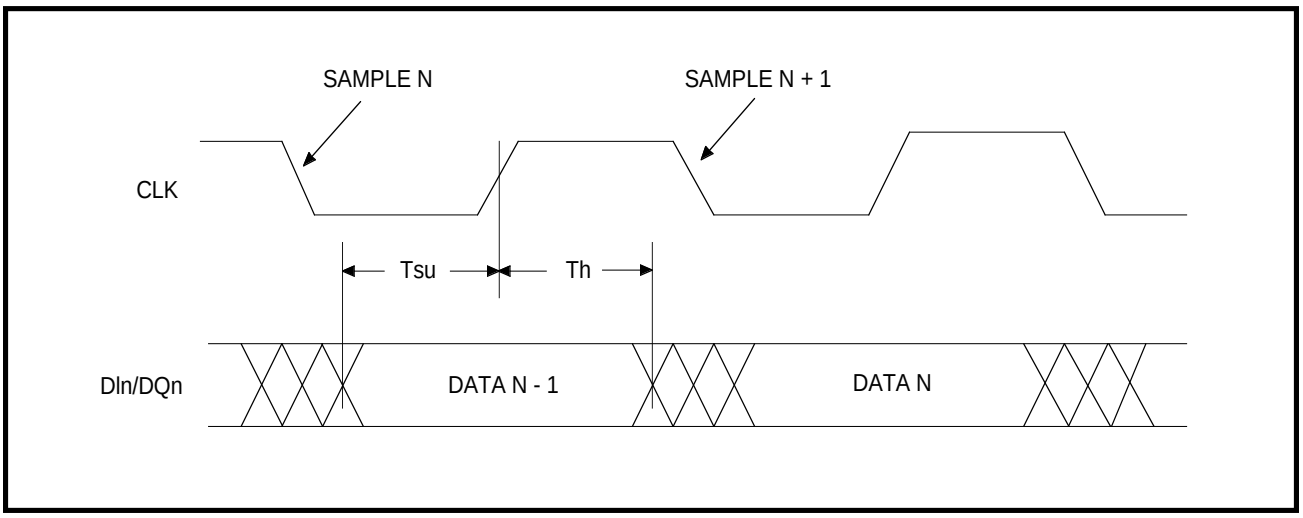
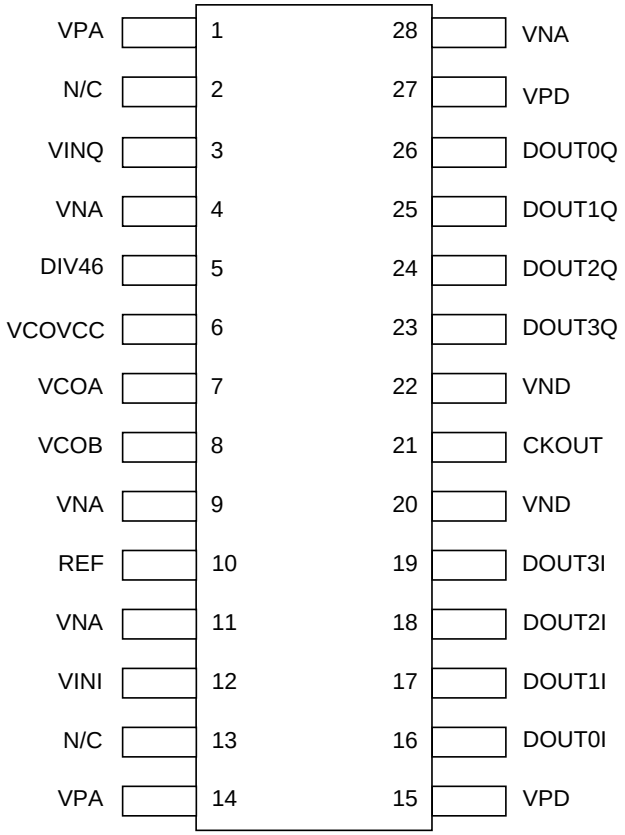


Figure 2: ADC Data Sampling and Output Timing

PACKAGE PIN DESIGNATIONS

(Top View)



79W2522
CL 28-Pin

CAUTION: Use handling procedures necessary for a static sensitive component.

Advance Information: Indicates a product still in the design cycle, and any specifications are based on design goals only. Do not use for final design.

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SSI 79W2530
Combined Demodulator/Filter

Target Specification

January 1996

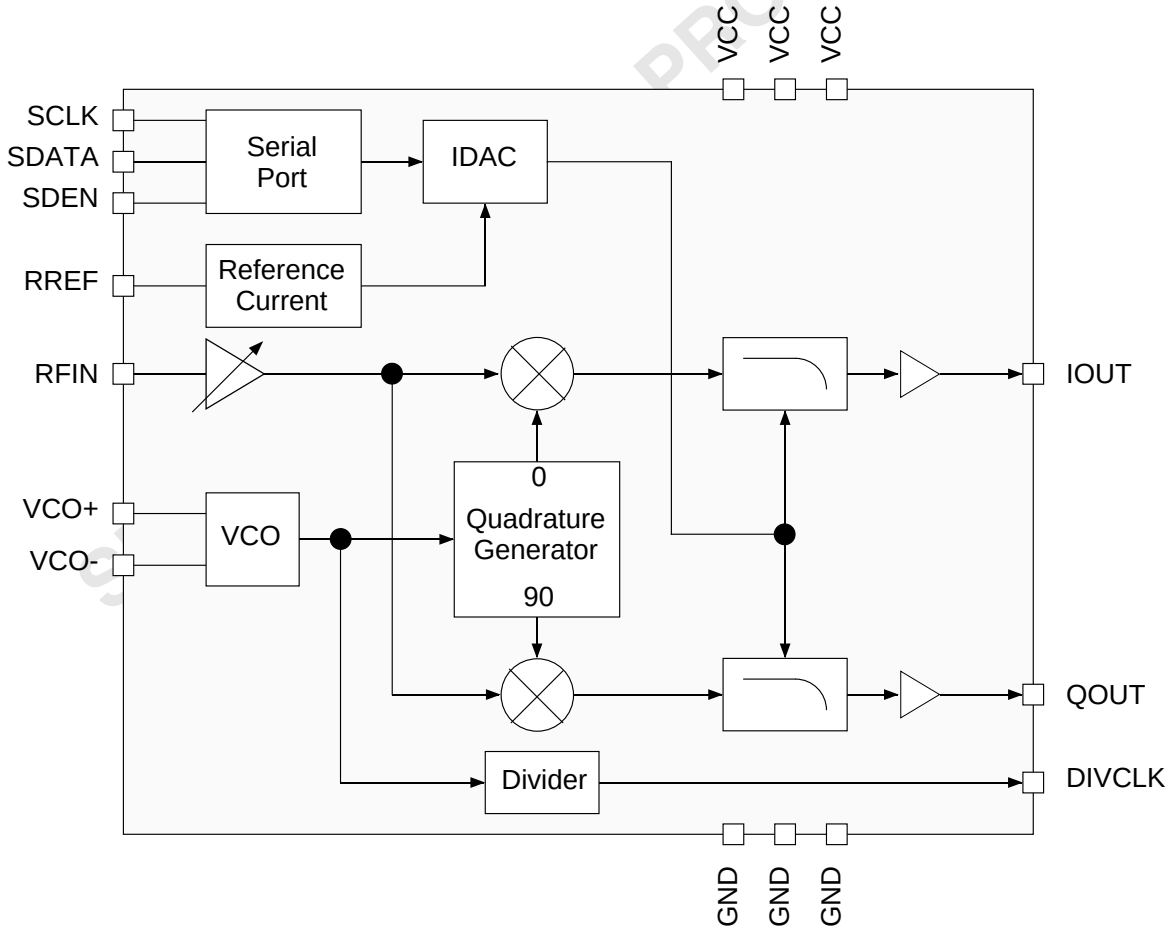
GENERAL DESCRIPTION

The SSI 79W2530 is a low cost, high performance device that accepts RF inputs from 400 MHz to 500 MHz and provides filtered, demodulated in-phase and quadrature outputs. The device includes integrated low pass filters with a programmable 3 dB cut-off frequency from 6.75 to 33.0 MHz. The 3 dB frequency is programmed through a serial port interface.

FEATURES

- **400 MHz to 500 MHz input range**
- **Internal VCO to generate the mix frequency**
- **Integrated 4th order Butterworth filters**
  - **Programmable f_C from 6.75 to 33.0 MHz**
  - **Integrated current DAC for filter control**
- **5 volt operation**
- **20-lead SO packaging**

BLOCK DIAGRAM



The target specification is intended as an initial disclosure of specification goals for the product. The specifications are based on design goals, subject to change and are not guaranteed. Silicon Systems assumes no obligation regarding future manufacture unless agreed to in writing.

DESCRIPTION

The SSI 79W2530 combines a down converter and quadrature demodulator with dual low pass filters on a single integrated circuit. A typical application for the SSI 79W2530 device is in the tuner block of a satellite receivers/decoder.

DEMODULATOR

The device accepts an input signal between 400 MHz and 500 MHz from a 50Ω system impedance and internally amplifies and splits the signal. The splitter is designed so that the two output signals are matched in output phase and amplitude. These signals are input to a pair of mixers that are driven by a quadrature oscillator whose frequency of oscillation is controlled by external components. The oscillator clock is also divided by 16 and provided as a buffered output signal. The mixers downconvert the input signal to a baseband frequency and provide in-phase and quadrature. The output of the mixers are provided to the input of the filter section.

LOW PASS FILTERS

The outputs of the demodulator are filtered by a pair of matched 4th order Butterworth filters that can be programmed over a range of 6.75 to 33.0 MHz. The cutoff frequency of the filters is determined by an internal current DAC whose magnitude is set by a 9-bit digital word. The 9-bit word allows the filter cutoff to be varied across the range of 6.75 MHz to 33.0 MHz in 51 kHz steps. The outputs of the filters are buffered and provided to the IOUT and QOUT pins on the device.

SERIAL PORT PROGRAMMING

Internal registers of the SSI 79W2530 are accessed via a serial port inerface that supports data transfer rates up to 20 MHz.

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SSI 88M8828
Integrated Audio Device

Advance Information

June 1995

DESCRIPTION

The SSI 88M8828 is a high integration CMOS device that contains all the functions necessary to implement a complete 16-bit stereo audio playback and record channel. When combined with an external FM synthesizer, the 88M8828 is a complete 16-bit sound system that supports the major sound standards including Sound Blaster/Sound Blaster Pro™, Windows Sound System™ (WSS), and MPU401 MIDI.

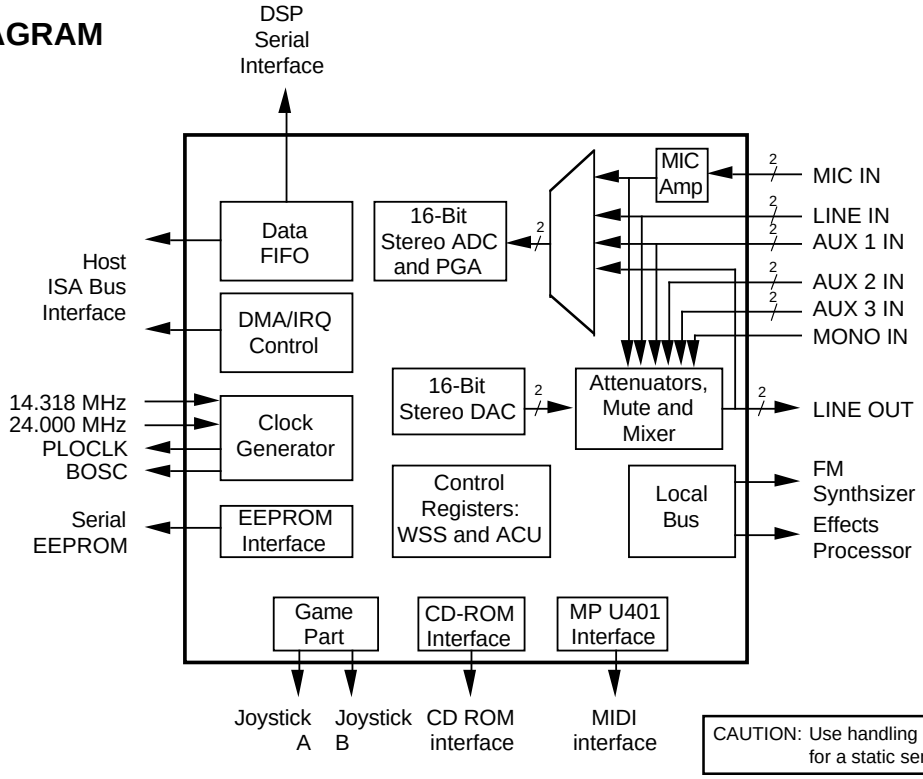
The 88M8828 includes stereo digital to analog and analog to digital converters with associated digital filtering, along with transmit and receive DSP serial ports to allow direct connection to external general purpose DSPs. The device also includes a five input stereo mixer, a game port timer, simultaneous capture and playback DMA channels, local I/O port, FM synthesizer port, DSP serial ports, and a CD ROM port that supports IDE and several custom interfaces. The 88M8828 provides for system design flexibility by supporting power-up auto configuration from an external serial EEPROM and several power down modes.

FEATURES

- **Supports major sound standards:**
  - **Sound Blaster™ and Sound Blaster Pro™**
  - **Microsoft Windows Sound System™ (WSS)**
  - **MPU401 MIDI**
  - **Adlib™**
- **16-bit stereo codec with programmable sampling rates to 48 kHz**
  - **Internal PLL for wide range of sample frequencies**
  - **Interface to miscellaneous digital audio sources**
- **Simultaneous playback and record (dual DMA channels)**
- **MPC2 compatible mixer with 5 stereo and 1 mono inputs plus DAC feedback**

(continued)

BLOCK DIAGRAM



CAUTION: Use handling procedures necessary for a static sensitive component.

FEATURES (continued)

- Full ISA bus interface supporting relocatable base addresses, interrupts and DMA
  - 4 base addresses, 5 interrupts and 3 DMA port assignments
- Local I/O port for reduced bus transceivers
- Game port interface with internal 558 type timers
- FM synthesizer control port
- 16-bit signed/8-bit unsigned linear PCM
- Programmable power management
- Dynamic range of 88 dB
- THD of <0.03%
- CD ROM interfaces
  - Mitsumi, Panasonic, Goldstar, Sony and IDE
- DSP serial ports for record and playback
  - Simplified interface to DSPs, effects processors, wavetable synthesizers and MPEG decoders

FUNCTIONAL DESCRIPTION

The SSI 88M8828 is a high integration audio device that forms a complete PC audio sound system when combined with an external FM synthesis device (such as the Yamaha OPL3). The device is designed to interface directly to the system ISA bus, allowing the host processor to program the internal registers that control the device functions. The internal registers of the 88M8828 are partitioned into functional blocks related to the Audio Control Unit (ACU), CD ROM, Windows Sound System™ (WSS), FM synthesis, Effects Processor (EP), MPU401, Game Port (GP), and the Master Configuration register (MC). Table 1 provides the address mapping for these base functional blocks.

MASTER CONTROL REGISTER

The basic functions of the 88M8828 are controlled by programming the Master Control registers (MC). These registers determine the assignment of the DMA channels, the interrupt channels, and the base addresses for the various internal blocks of the device. At power-up, the device looks for an external serial EEPROM from which it uses to initialize the contents of the MC registers. If an EEPROM is not detected, the default base address values are retained. After the power-up sequence, the contents of the MC registers can be programmed via the ISA bus to reconfigure the device.

HOST INTERFACE

The host processor communicates with the 88M8828 over the ISA bus interface. When the ISA bus address enable line (SAEN) is driven low by the host processor, the internal decode logic of the 88M8828 compares the present address bits on the ISA bus with the base address information contained in the MC registers. While SAEN is low if a valid address is detected, the 88M8828 uses the address and the ISA control lines

TABLE 1: 88M8828 Register Mapping

Functional Block	Symbol	Available Addresses	Default	MC6 Enable Bit	Address Range
Master Control	MC	F80, F20, E80, E20	F80h	n/a	0h - Fh
Game Port	GP	200	200h	1xxx xxxx	0h - 1h
MPU401	MPU	330, 332, 334, 336	330h	x1xx xxxx	0h - 1h
Effects Processor	EP	000h - 7F8h	398h	xx1x xxxx	0h - 7h
Audio Control Unit	ACU	220, 240, 260, 280	220h	xxx1 xxxx	0h - Fh
CD ROM	CD	000h - 7F8h	320h	xxxx 1xxx	0h - 4h
Windows Sound System	WSS	530, 604, E80, F40	530h	xxxx x1xx	0h - 7h
FM Synthesizer	FM	388, See Note 1.	388h	xxxx xx1x	0h - 7h

Note 1: The FM Synthesizer Interface can be accessed either via the ISA Bus Base address location or from the ACU register set.

TABLE 2: Master Control Status Register Mapping (MCBase + 0, Read Only)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Version ID	Version ID	WSS-IRQ	CD-IRQ	MPU-IRQ	FM-IRQ	ACU-IRQ	Reserved
1	0	1 = Active	1 = Active	1 = Active	1 = Active	1 = Active	
		0 = Inactive	0 = Inactive	0 = Inactive	0 = Inactive	0 = Inactive	

TABLE 3: Master Control Index Register (MCBase + 0, Write Only)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
R/W Enable	0	0	Master Control Data Index D4 - 0				

TABLE 4: Master Control Index Register Mapping

ID	Register Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	Base Address	WSS		SB		MPU		MC	
1	EP Address	A3	A10	A9 - A4					
2	CD Address	A3	A10	A9 - A4					
3	Control Register 0	OSC	MPU-IRQ		CD-IRQ			CD-DMA	
4	Control Register 1	WSS-IRQ	FM-IRQ			ACU-IRQ		ACU-DMA	
5	Enable Register	Game	MPU	EP	ACU	CD	WSS	FM	OPL
6	Serial Port Clock Polarity	RX2 PULM	RX1 PULM	LRI2P	BCI2P	LRI1P	BCI1P	LROP	BCOP
7	Serial Port Clock Format	SPLM1 - 0		RX2 EN	RX1 EN	TX EN	LRI2M	LRI1M	LROM
8	Serial Port Clock Directions	TXPU LM	TXLR	LRI2 IO	BCI2 IO	LRI1 IO	BCI1 IO	LRO IO	BCO IO
9	Serial Port Sync Delays	RX2 LR	RX1 LR	RX2 DLY1 - 0		RX1 DLY1 - 0		TX DLY1 - 0	
10	Bit-Clock Divider Select	N/U	N/U	RX2 DIV1 - 0		RX1 DIV1 - 0		TX DIV1 - 0	
11	RX1 Bit-Clock Divider Select	N/U	N/U	RX2DV5 - 0					
12	Codec-Serial Port Control	PD1 - 0		PW DNP	DCAL	RX2 DAC	RX1 DAC	FIFO DAC	TX SRC
13	PLL Counter M	PTM	DSB DMA	N/U	M4 - 0				
14	PLL Counter N	CAP SR1	CAP SR0	N5 - 0					
15	PLL Counter J & H	J3 - 0				H3 - 0			
24	Bus Interface	PDT3 - 0				EEDO	EEDI	EESK	EECS

HOST INTERFACE (continued)

($\overline{SIOR}$, $\overline{SIOW}$) to determine the type of data access and the appropriate register to address.

The 88M8828 can initiate a DMA cycle over the ISA bus by driving the desired DMA request line (DRQ0, 1, or 3) and waiting for the acknowledgment from the host processor's DMA controller. Upon receipt of an acknowledge signal ($\overline{DACK0}$, $\overline{1}$, or $\overline{3}$), the device will arbitrate with the DMA controller to transfer the designated number of sample bytes. The 88M8828 supports dual DMA channels so that playback and record can be performed simultaneously. If two DMA channels are not available in the system, the device can be configured to share a single DMA channel for non-simultaneous playback and record.

PROGRAMMABLE PLL CLOCK SYNTHESIZER

An on-chip clock synthesizer/multiplier generates the oversampling clocks used by the delta-sigma codec. It synthesizes all the Windows Sound System and ACU sampling frequencies from the 24 MHz crystal. Alternatively, the PLL can be programmed to utilize the serial interface shift clock.

The output of the PLL is available for use on the PLOCLK pin. Most DSPs, effects processors, wavetable synthesizers and MPEG decoders can utilize this clock output in place of local oscillators.

Master Control Index Registers ID=13-15 control the PLL counters.

The Master Bit Clock source is selected in the Master Control Index Register ID=7 bits SPLM1-0. Different clock sources will be utilized for ACU, Windows Sound System or DSP serial port applications.

Refer to the 88M8828 Programmer's Reference for additional information on selecting the master clock source and configuring the phase lock loop.

POWER MANAGEMENT

The 88M8828 contains a Power Down Timer for reducing system power consumption. After a period of inactivity the device will automatically enter its power down mode. Device power consumption falls to T.B.D. µA. Upon the next device access (ISA bus control register read/write operation) the 88M8828 will resume normal operation and the timer restarts.

Alternatively, various modes of reduced power consumption can be initiated from Master Control Index Register ID=12.

Master Control Index Register ID=24 contains four bits for initializing the power down timer. The default power down timer value of 8h provides a 5 minute timeout period. For longer periods of timeout increase the timer value (maximum timeout of 9.3 minutes for timer value = Fh).

CONFIGURATION SERIAL EEPROM

The 88M8828 contains a 3 wire serial interface for access to an external serial EEPROM. Device configuration and miscellaneous data may be stored in a 93C66 type EEPROM. The 88M8828 looks for the EEPROM after power-on reset and if present initializes itself to the configuration stored therein. If no EEPROM is found the 88M8828 initializes itself with the default definitions. The host system may then reconfigure the 88M8828 as required.

If an EEPROM is present the host must write the 88M8828's configuration to the EEPROM after configuring. Master Control Index register ID=24 contains four bits for controlling the EEPROM's chip select, clock, data in and data out. These signals are under direct program control. The software program must guarantee proper timing and control of the EEPROM.

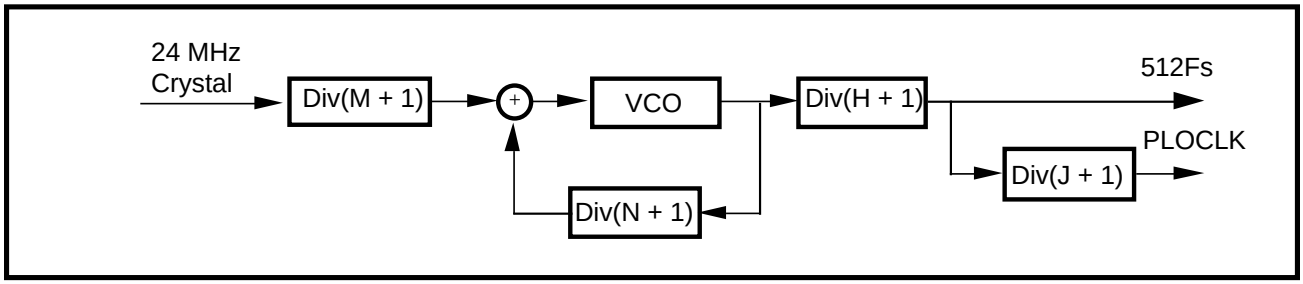


FIGURE 1: Phase Lock Loop (PLL) Control Logic

Refer to the 88M8828 Programmer's Reference for information on the EEPROM's 88M8828 configuration data structure.

WINDOWS SOUND SYSTEM (WSS)

The 88M8828 supports the full WSS standard for audio playback and recording. At power-up, the default address for the WSS function is 530h. This address can be modified by either direct programming from the ISA bus or by loading a value from the external configuration EEPROM. The user can access the EEPROM control bits by indirect addressing from the MC Index Register ID=24.

In the WSS operating mode, the device is configured according to the contents of the WSS register set. There are four base address registers: the first two registers provide indirect access to an additional 32 registers; the third register provides status information; and the fourth register contains 8-bit playback or record data.

Because the WSS and ACU interfaces share a common audio codec, when operating in the WSS mode the ACU Interface is automatically disabled. The ACU's control logic is powered down for minimum system noise.

Master Control Index Registers ID=0 and 4 set up the WSS base address and interrupt enable bit. The WSS Enable bit (DB2) in Master Control Index Register ID=5 must be set to enable the WSS Interface.

Table 5 provides the mapping information for the WSS base address functions.

The 88M8828 supports both MODE1 and MODE2 operation. In MODE1 operation (MODE2 bit of I12 = 0) the device is configured to look like the industry standard 1848 codec, utilizing only the first 16 indirect registers. In MODE2 operation (MODE2 bit of I12 = 1) the device has expanded capabilities that utilize all 32 indirect registers.

Refer to the 88M8828 Programmer's Reference for a complete description of the WSS Indexed Register set. Table 6 identifies the Indexed WSS Registers supported in the 88M8828.

AUDIO CONTROL UNIT (ACU)

The Audio Control Unit (ACU) includes an 8051 µ-controller core for controlling its audio resources. The default base address for the ACU is 220h. This address can be modified to one of four base addresses by setting bits four and five of MC register MC1. When an external EEPROM is detected, these bits are automatically set at power-up according to the data in the EEPROM. The user can also access these bits through the ISA bus by indirect addressing from the MC Index Register ID=24.

The mixer registers are addressed indirectly through the ACU Index Address register (I4) and the Mixer Data Register (I5).

Master Control Index Registers ID=0 and 4 set up the ACU base address, interrupt configuration and DMA configuration.

Refer to the 88M8828 Programmer's Reference for a complete description of the ACU Indexed Register set.

Table 7 identifies the ACU base registers supported in the 88M8828.

Game Port (GP)

The 88M8828 includes a game port interface that supports two external joysticks. The interface can monitor the X and Y coordinate inputs and two button inputs from each joystick. The base address of the GP register is 200h. Writing to this address triggers the internal timers whose time constants are set by the position of the external joysticks. Reading back this register provides the user with status of the buttons and the X and Y coordinates. The X and Y coordinate bits are held at "1" until the internal timers have timed out. The bit mapping for the GP register is provided in Table 8.

FM SYNTHESIZER

The 88M8828 supports external FM synthesizers, such as the Yamaha OPL2/3/4. The 88M8828 decodes ISA bus addresses to identify data that is intended for the FM synthesizer device. The 8828 generates the FM chip select signal ($\overline{\text{FMCS}}$) at ISA Bus address 388h and drives the external I/O port with the appropriate address, strobe, and data. The device also receives the interrupt ($\overline{\text{FMINT}}$) from the FM synthesizer and maps it to the appropriate ISA bus interrupt line.

The local bus is shared with the Effects Processor.

Master Control Index Register ID = 4 sets up the FM interrupt configuration.

TABLE 5: WSS Base Address Register Mapping

Base +	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	Configuration, WO	DSS	ISS	WSS-IRQ2	WSS-IRQ1	WSS-IRQ0	WSS-DMA2	WSS-DMA1	WSS-DMA0
0	Version, RO	CHN1		IRQ-SEN1	IRQ-SEN0	DMA-SEN1	DMA-SEN0	VER1	
4	Index Address, R/W	INIT	MCE	TRD	IA4 - 0				
5	Index Data, R/W	ID7 - 0							
6	Status, RO	CU/L	CL/R	CRDY	SER	PU/L	PL/R	PRDY	INT
7	Capture Data, RO	CD7 - 0							
7	Playback Data, WO	PD7 - 0							

TABLE 6: WSS Indexed Registers Mapping

0	Left ADC Input Control	LSS1 - 0		LMGE	n/u	LAG3 - 0			
1	Right ADC Input Control	RSS1 - 0		RMGE	n/u	RAG3 - 0			
2	Left AUX #1 Input Control	LX1M	n/u	n/u	LX1G4 - 0				
3	Right AUX #1 Input Control	RX1M	n/u	n/u	RX1G4 - 0				
4	Left AUX #2 and AUX #3 Input Control	LX2M	n/u	n/u	LX2G4 - 0				
5	Right AUX #2 and AUX #3 Input Control	RX2M	n/u	n/u	RX2G4 - 0				
6	Left DAC Output Control	LDM	n/u	LDA5 - 0					
7	Right DAC Output Control	RDM	n/u	RDA5 - 0					
8	Fs & Playback Data Format	n/u	FMT	n/u	S/M	CSF2 - 0			C2SL
9	Interface Configuration	CPIO	PPIO	n/u	n/u	ACAL	SDC	CEN	PEN
10	Pin Control	n/u	n/u	n/u	n/u	n/u	n/u	IEN	n/u
11	Errror Status and Initialization	COR	PUR	ACI	DRS	0	0	0	0
12	MODE and ID	n/u	MODE2	n/u	n/u	ID3 - 0			
13	Loopback Control	n/u	n/u	n/u	n/u	n/u	n/u	n/u	LBE
14	Playback Upper Base Control	PUB7 - 0							
15	Playback Lower Base Control	PLB7 - 0							
16	Alternate Feature Enable	n/u	n/u	n/u	n/u	n/u	n/u	n/u	DACZ

TABLE 6: WSS Indexed Registers Mapping (continued)

Base +	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
17	Reserved	n/u	n/u	n/u	n/u	n/u	n/u	n/u	n/u
18	Left Line Input Control	LLM	n/u	n/u	LLG4 - 0				
19	Right Line Input Control	RLM	n/u	n/u	RLG4 - 0				
20	Reserved	n/u	n/u	n/u	n/u	n/u	n/u	n/u	n/u
21	Reserved	n/u	n/u	n/u	n/u	n/u	n/u	n/u	n/u
22	Left MIC Input Control	LMM	n/u	n/u	LMG4 - 0				
23	Right MIC Input Control	RMM	n/u	n/u	RMG4 - 0				
24	Alternate Feature Status	n/u	n/u	CI	PI	CU	CO	PO	PU
25	Version/Chip ID	V2 - 0			n/u	n/u	CID2 - 0		
26	Mono Input Control	MIM	n/u	n/u	n/u	MIA3 - 0			
27	Reserved	n/u	n/u	n/u	n/u	n/u	n/u	n/u	n/u
28	Capture Data Format	n/u	FMT	n/u	S/M	n/u	n/u	n/u	n/u
29	Reserved	n/u	n/u	n/u	n/u	n/u	n/u	n/u	n/u
30	Capture Upper Base Count	CUB7 - 0							
31	Playback Lower Base Control	CLB7 - 0							

TABLE 7: ACU Base Address Registers Mapping

Base +	Name	Dir.	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
4	Mixer Index Address	WO	MA7 - 0							
5	Mixer Data	R/W	MD7 - 0							
6	ACU Control	WO	X	X	X	X	X	X	X	RST
A	ACU Output Data	RO	DO7 - 0							
C	ACU Output Status	RO	FULL	X	X	X	X	X	X	X
C	ACU Input Data	WO	DI7 - 0							
E	ACU Input Status	FULL	X	X	X	X	X	X	X	X

TABLE 8: ACU Base Indexed Registers Mapping

Base +	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	Mixer Reset	X	X	X	X	X	X	X	X
2	Mixer Master Volume Mono	MML3 - 0				MMR3 - 0			
22	Mixer Master Volume Stereo	MSL3 - 0				MSR3 - 0			
6	Mixer FM Volume Mono	0	FMM1 - 0		1	FMR3 - 0			
26	Mixer FM Volume Stereo	FSL3 - 0				FSR3 - 0			
8	Mixer CD Volume Mono	CML3 - 0				CMR3 - 0			
28	Mixer CD Volume Stereo	CSL3 - 0				CSR3 - 0			
A	Mixer MIC Volume	X	X	X	X	0	MI2 - 0		
C	Mixer ADC Source & Filter	0	0	LPF-SEL1	1	LPF-SEL2	SRC1 - 0		1
1E	Mixer DAC Control	X	X	DAC-LPF	X	X	X	DAC-EN	X
2E	Mixer Line-In Volume	LL3 - 0				LR3 - 0			
20	Mixer Playback Source	0	0	0	1	LINE	CD	MIC	1

TABLE 9: Game Port Register Mapping

Base +	Name	Dir.	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
200h	Game port	R/W	BB2	BB1	AB2	AB1	BY	BX	AY	AX

TABLE 10: MPU401 (MPU) Port Register Mapping

0	I/O Buffer	R/W	D7 - 0							
1	Command port	W	MC7 - 0							
1	Status port	R	IN	OUT	x	x	x	x	x	x

FUNCTIONAL DESCRIPTION (continued)

SERIAL INTERFACE PORTS

The 88M8828 includes one serial transmit port and two serial receive ports providing a serial digital audio interface to external wavetable synthesizers, DSP effects processors and MPEG decoders. These ports can be configured to support many different protocols that are compatible with most wave table synthesizers and general purpose DSPs.

The serial interface port registers are mapped into the Master Control Index Registers ID=6 - 12. These ports are disabled at reset (ID=8).

Refer to the 88M8828 Programmer's Reference for a complete description of the Serial Port Registers.

MPU401 MIDI PORT (MPU)

The 88M8828 includes a UART that supports the MPU401 standard for MIDI. The register mapping for the MPU401 (MPU) port is provided in Table 10. The default base address for the MPU registers is 330h.

Master Control Index Registers ID=0 and 3 set up the MPU base address and interrupt configuration. The MPU Enable bit (DB6) in Master Control Index Register ID=5 must be set to enable the MPU Interface.

CD ROM INTERFACE

The 88M8828 provides an interface that can be configured to support CD-ROM drives that use IDE, Sony, Mitsumi, Panasonic or Goldstar interface formats. While the 88M8828 supports the electrical interface for the above stated devices each interface will require a separate connector due to different pinout definitions.

Master Control Index Registers ID=2 and 3 set up the CD base address, interrupt configuration and DMA configuration.

EFFECTS PROCESSOR INTERFACE

The 88M8828 supports an external effects processor by providing a chip select ($\overline{\text{EPCS}}$) output. The address and data information is provided on the external I/O port.

The local bus is shared with the FM Synthesizer.

Master Control Index Register ID=1 sets up the EP base address. The EP Enable bit (DB5) in Master Control Index Register ID=5 must be set to enable the EP Interface.

CRYSTAL

The 88M8828 contains two crystal oscillators for system utilization. Connect a 14.318 MHz crystal to the XTAL1 pins and a 24.000 MHz crystal to the XTAL2 pins. Both crystals must be parallel resonant mode types with 20 pF load capacitors.

The 14.318 MHz crystal provides the clock reference for OPL2/3 FM synthesizers. The 24.000 MHz crystal provides the clock reference for all device resources. Utilizing the PLL the 88M8828 is able to provide a wide range of sampling frequencies.

External CMOS oscillators may be used in place of the crystals. Connect the appropriate external clock sources to the XTAL1I and XTAL2I pins. The unused XTAL1O and XTAL2O pins are to be left unconnected.

ANALOG INTERFACES

The external analog input interface consists of a stereo microphone input, stereo line-in and 3 auxiliary inputs and a mono input. The analog output consists of one stereo line-out. This interface is MPC Level-2 compatible requiring 1 Vrms maximum signals.

The microphone input channels include an optional 20 dB gain amp. The ADC is serviced by a four channel input multiplexer. Inputs to the multiplexer are the microphone input, line-in, auxiliary 1 and the line-out output. Only one of these inputs may be selected at any given time. Unused analog inputs are to be capacitively coupled to analog ground.

Refer to the 88M8828 Demo Board schematic for examples of microphone and analog interfacing circuits.

The DAC output plus the microphone input, line-in, auxiliaries 1, 2 and 3 and mono-in are inputs to the line-out multiplexer. Each line-out multiplexer source has its own attenuator and mute control. 16 levels of gain plus mute are provided in the 88M8828. The line-out signal is a line-level output for driving an external amplifier or powered speakers. Even high impedance headphones must be driven by an amplifier.

PIN DESCRIPTION

ISA BUS

NAME	TYPE	DESCRIPTION
SA0-11	I	ISA BUS ADDRESS BITS 0 THROUGH 11: These bits are decoded during an I/O cycle (SAEN = 0) to access the internal registers.
SAEN	I	ISA BUS ADDRESS ENABLE INPUT: Driving this pin high enables a DMA cycle. Driving this pin low enables an I/O cycle.
$\overline{\text{SIOR}}$	I	ISA BUS READ SIGNAL: Driving this pin low allows data to be read from the register location identified by the address on SA0-11.
$\overline{\text{SIOW}}$	I	ISA BUS WRITE SIGNAL: Driving this pin low allows data to be written to the register location identified by the address on SA0-11.
SD0-7	I/O	ISA BUS DATA BITS 0 THROUGH 7: These pins are bi-directional pins that serve as the 8-bit ISA data bus.
IRQn	O	INTERRUPT REQUEST LINES: These five pins (IRQ5, IRQ7, IRQ9, IRQ10, IRQ11) are driven by the 8828 to notify the host that servicing is required. These pins are assigned to the internal functional blocks by programming internal registers (see register maps).
DRQn	O	DMA REQUEST LINES: These three pins (DRQ0, DRQ1, DRQ3) are driven high by the 8828 to request a DMA transfer and will remain active until the DMA cycle is complete. The pins are connected to the associated DRQ lines on the ISA bus. Control over each pin is assigned by programming the internal registers (see register maps).
$\overline{\text{DACK}}$n	I	DMA ACKNOWLEDGE: These three pins ($\overline{\text{DACK0}}$, $\overline{\text{DACK1}}$, $\overline{\text{DACK3}}$) are driven low by the host to acknowledge that the requested DMA activity has been acknowledged. The pins are connected to the associated $\overline{\text{DACK}}$n lines on the ISA bus. The signals from each pin are routed internally according to the assignments of the DRQn pins.
SRESDRV	I	MASTER RESET. This input resets the 8828.

LOCAL BUS

$\overline{\text{RES}}$	O	RESET: This output is driven low when the SRESDRV pin is driven high by the host.
BD0-7	I/O	LOCAL DATA BUS BITS 0 THROUGH 7: These pins are bi-directional pins that serve as the 8-bit local data bus.
BA0-2	O	LOCAL BUS ADDRESS: These pins are the address bits for the local bus.
$\overline{\text{BRD}}$	O	LOCAL BUS READ: This pin is driven low by the 8828 to indicate a local bus read cycle.
$\overline{\text{BWD}}$	O	LOCAL BUS WRITE: This pin is driven low by the 8828 to indicate a local bus write cycle.

GAME PORT

NAME	TYPE	DESCRIPTION
GD0-3	I	GAME PORT XY INPUTS: These four pins (GD0, GD1, GD2, GD3) are the RC inputs for the internal game port timers that determine X and Y coordinate information.
$\overline{GD4}$-$\overline{7}$	I	GAME PORT BUTTON INPUTS: These four pins (GD4, GD5, GD6, GD7) are the button inputs from the external joystick. A low level indicates a button is pushed.

FM INTERFACE

$\overline{FMCS}$	O	FM CHIP SELECT: The 8828 drives this pin low to select the external FM synthesizer chip.
$\overline{FMINT}$	I	FM INTERRUPT: This pin is driven low by the external FM synthesizer to interrupt the 8828.
$\overline{EPCS}$	O	EFFECTS PROCESSOR CHIP SELECT: The 8828 drives this pin low to select the external effects processor chip.

CD-ROM

SP/PWD	I	CD-ROM POWER DOWN.
GS	I	CD-ROM TYPE SELECT: Future option. Currently not used.
$\overline{NINT}$	I	CD-ROM INTERRUPT: This pin is driven low by the CD-ROM to interrupt the 8828.
CD_DRQ	I	CD-ROM DMA REQUEST: This pin is driven high by the CD-ROM to request a DMA.
CD_DACK	O	CD-ROM DMA ACKNOWLEDGE: This pin is driven high by the 8828 to acknowledge the DMA request from the CD-ROM drive.
$\overline{CMD}$	O	CD-ROM COMMAND/DATA SELECT: This pin selects either a data or command transfer.
$\overline{CDEN}$	O	CD-ROM BUS ENABLE: The 8828 drives this pin low to indicate that the CD-ROM bus is active.
$\overline{ST0}$-$\overline{3}$	O	CD-ROM STATUS PORT: These pins are driven by the CD-ROM to indicate status.
$\overline{IOCS16}$	I	CD-ROM 16-BIT SELECT: This pin is driven low by the IDE device to indicate to the 8828 that it is capable of 16-bit data transfers.
CD16EN	O	16-BIT OR 8-BIT DATA TRANSFER SELECT: This pin is driven low for 16-bit data transfers in PIO mode. Conversely, the pin is high for 8-bit data transfers. When transferring in DMA mode the data transfers are always 16-bit and CD16EN will not be asserted.

MIDI PORT

MIDIRX	I	MIDI RECEIVE INPUT: This is the receive data from the MIDI port.
MIDITX	O	MIDI TRANSMIT OUTPUT: This is the transmit data from the MIDI port.

PIN DESCRIPTION (continued)

DSP SERIAL PORT

NAME	TYPE	DESCRIPTION
BCO	I/O	TRANSMIT BIT CLOCK: Clock for transmit data from the serial port.
LRO	I/O	TRANSMIT SYNC: Multi-configurable sync to denote start of data transfer.
TXD	O	TRANSMIT DATA: Serial port transmit data.
BCI1/2	I/O	RECEIVE BIT CLOCK: Clock for the two receive channels (BCI1, BCI2).
RXD1/2	I	RECEIVE DATA: Input data signals (RXD1, RXD2) from the external DSP. RXD1 is clocked by BCI1, RXD2 is clocked by BCI2.
LRI1/2	I/O	RECEIVE SYNC: Multi-configurable sync to denote start of data transfer. (LRI1, LRI2).

OSCILLATORS

BOSC	O	BUFFERED OSCILLATOR OUTPUT: This pin is a X1 or X1/4 output of the XTAL1 oscillator.
PLOCLK	O	PLL OUTPUT.
XTAL1I/O	I	EXTERNAL CRYSTAL CONNECTION: 14.318 MHz OPL crystal (Parallel Resonant Mode).
XTAL2I/O	I	EXTERNAL CRYSTAL CONNECTION: 24.000 MHz 8051 crystal (Parallel Resonant Mode).

ANALOG I/O

MICR/L	I	MICROPHONE INPUTS: Stereo (MICR, MICL) input for an external microphone.
LINR/L	I	LINE INPUTS: Stereo (LINR, LINL) inputs for an external line source.
AUXnR/L	I	AUXILIARY INPUTS: Stereo inputs (AUX1R, AUX1L; AUX2R, AUX2L; AUX3R, AUX3L) for three external auxiliary audio devices.
MONO	I	MONO INPUT: Mono input from external source such as PC speaker drive.
LOR/L	O	LINE OUTPUTS: Stereo (LINER, LINEL) outputs for driving an external amplifier.
FILTR/L	-	AD FILTER: Connect a 1000 pF NPO capacitor between each of these pins and analog ground.
VREF	I	INTERNAL REFERENCE VOLTAGE: Connect a 47 µF tantalum and 0.1 µF ceramic capacitor from this pin to analog ground.
REFGND	I	GROUND REFERENCE.
COM	O	COMMON MODE REFERENCE OUTPUT: Connect a 47 µF, 10V tantalum capacitor in parallel with a 0.1 µF ceramic capacitor from this pin to analog ground.

TEST PINS

TEST	I	TEST PIN: Tie this pin to GND.

POWER/GROUND

VD1-7	-	DIGITAL POWER: These seven pins are connected to the digital power supply.
GNDD1-8	-	DIGITAL GROUND: These eight pins are connected to the digital ground plane.
VA1/2	-	ANALOG POWER: These two pins are connected to the analog power supply.
GNDA1-2	-	ANALOG GROUND: These two pins are connected to the analog ground plane.

ELECTRICAL SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Operation beyond the maximum ratings may damage the device

PARAMETER	RATING
Storage temperature	-65 to 150°C
Junction operating temperature	+130°C
Positive supply voltage (Vp)	-0.3 to 6V
Voltage applied to any pin	-0.3V to Vp + 0.3V

ELECTRICAL CHARACTERISTICS

Unless otherwise specified: Ta = 25°C; positive power supply (VD, VA) = +5V; logic levels 0 = 0V, 1 = VD. Conversion rate (Fs) = 48 kHz; external PLOCLK = 24.576 MHz. Full scale input sine wave 1 kHz, measurement bandwidth 20 Hz to 20 kHz.

Analog Input Characteristics

PARAMETER	CONDITION	MIN	NOM	MAX	UNIT
ADC Resolution			16		bits
Dynamic range	Line-in, AUX inputs	80	88		dB
	MIC Inputs	72	80		dB
Total harmonic distortion	All inputs			0.03	%
Frequency response	0 to 0.40 Fs	-0.5		0.2	dB
Full scale input voltage	Line-in, AUX inputs	2.6	2.8	3.0	Vp-p
	MIC Inputs (Gain = 0 dB)	2.6	2.8	3.0	Vp-p
	MIC Inputs (Gain = 20 dB)	0.26	0.28	0.30	Vp-p
Input DC bias		2.00	2.25	2.50	V
Input resistance		10		100	kΩ
Input capacitance				15	pF
Programmable gain	Line-in, AUX inputs	-0.2		22.7	dB
	MIC Inputs	-0.2		42.7	dB
Gain step		1.3	1.5	1.7	dB

Analog Output Characteristics

DAC Resolution			16		bits
Dynamic range	Line out (LOL, LOR)	80	88		dB
Total harmonic distortion	10 kΩ, 100 pF load			0.03	%
Full scale output voltage		1.8	2.0	2.2	Vp-p
Output DC bias		2.00	2.25	2.50	V
Load resistance (RL)		2			kΩ
Load capacitance (CL)				100	pF
VREF output voltage		2.00	2.25	2.50	V
CMO Current Drive			100		µA

ELECTRICAL CHARACTERISTICS (continued)

Digital Filter Characteristics

PARAMETER	CONDITION	MIN	NOM	MAX	UNIT
Passband		0		0.40 Fs	Hz
Frequency response		-0.5		0.4	dB
Passband ripple		-0.5		0.5	dB
Transition band		0.40 Fs		0.60 Fs	Hz
Stop band		0.60 Fs			Hz
Stop band rejection		68			dB

Mixer Input Gain Control Programming

PARAMETER (DAC VALUE)	**CONDITION** (SIGNAL)	MIN	NOM	MAX	UNIT
00H	Line-in, AUXn, Mic, MONO		0		dB
01H			-1.5		dB
02H			-3.0		dB
03H			-4.5		dB
04H			-6.0		dB
05H			-8.0		dB
06H			-10.0		dB
07H			-13.0		dB
08H			-16.0		dB
09H			-20.0		dB
0AH			-24.0		dB
0BH			-28.0		dB
0CH			-32.0		dB
0DH			-36.0		dB
0EH			-42.0		dB
0FH			-68.0		dB

Power Consumption Characteristics (Ta = 25°C, VD = VD1-7 = +5.0V, GNDD = 0.0V)

PARAMETER	CONDITION	MIN	TYP	MAX	UNIT
Normal Operating Mode					mA
Power Down Mode					µA

Digital Characteristics (Ta = 25°C, VD = VD1-7 = +5.0V, GNDD = 0.0V)

PARAMETER	CONDITION	MIN	NOM	MAX	UNIT
High-Level Input Voltage V_{IH}	Digital Inputs XTAL1I, XTAL2I	2.0 VD-1.0		VD+0.3 VD+0.3	V V
Low-Level Input Voltage V_{IL}		-0.3		0.8	V
High-Level Output Voltage V_{OH}	ISA Bus SD Pins IO = -16 ma All others IO = -4 ma	2.4 2.4		VD VD	V V
Low-Level Output Voltage V_{OL}	ISA Bus SD Pins IO = 16 ma All others IO = 4 ma			0.4 0.4	V V
Input Leakage Current	Digital Inputs	-10		10	uA
Output Leakage Current	Digital Outputs, High Impedance	-10		10	uA

Timing Characteristics (Ta = 25°C, VD1-7 = +5.0V, GNDD = 0.0V)

IOW or IOR strobe width T_{STW}					ns
Data valid to IOW rising edge (write cycle) T_{WDSU}					ns
IOR falling edge to data valid (read cycle) T_{RDDV}					ns
SA setup to IOR or IOW falling edge T_{ADSU}					ns
SA hold from IOW or IOR rising edge T_{ADHD}					ns
DACK inactive to IOW or IOR falling edge $T_{SUD}1$					ns
DACK active from IOW or IOR rising edge $T_{SUD}2$					ns
DACK setup to IOR dalling edge $T_{DKSU}1$					ns
DACK setup to IOW falling edge $T_{DKSU}2$					ns
Data hold from IOW rising edge $T_{DHD}2$					ns
DRQ hold from IOW or IOR falling edge T_{DRHD}					ns
Time between rising edge of IOW or IOR to next falling of IOW or IOR T_{BWDN}					ns
Data hold from IOR rising edge $T_{DHD}1$					ns

Timing Characteristics (Ta = 25°C, VD1-7 = +5.0V, GNDD = 0.0V) (continued)

PARAMETER		CONDITION	MIN	TYP	MAX	UNIT
DACK hold from IOW rising edge	$T_{DKHD}1$					ns
DACK hold from IOR rising edge	$T_{DKHD}2$					ns
SRESDRV pulse width high	T_{RES}					ns

DSP Serial Port Characteristics (Ta = 25°C, VD1-7 = +5.0V, GNDD = 0.0V)

BCO and BCI1/2 frequency						MHz
BCI1/2 rising to LRI1/2 valid	$T_{LRI}1$					ns
BCI1/2 falling to LRI1/2 valid	$T_{LRI}2$					ns
BCI1/2 rising to RXD1/2 valid	$T_{RX}1$					ns
BCI1/2 falling to RXD1/2 valid	$T_{RX}2$					ns
BCO rising to LRO valid	$T_{LRO}1$					ns
BCO falling to LRO valid	$T_{LRO}2$					ns
BCO rising to TXD valid	$T_{TX}1$					ns
BCO falling to TXD valid	$T_{TX}2$					ns

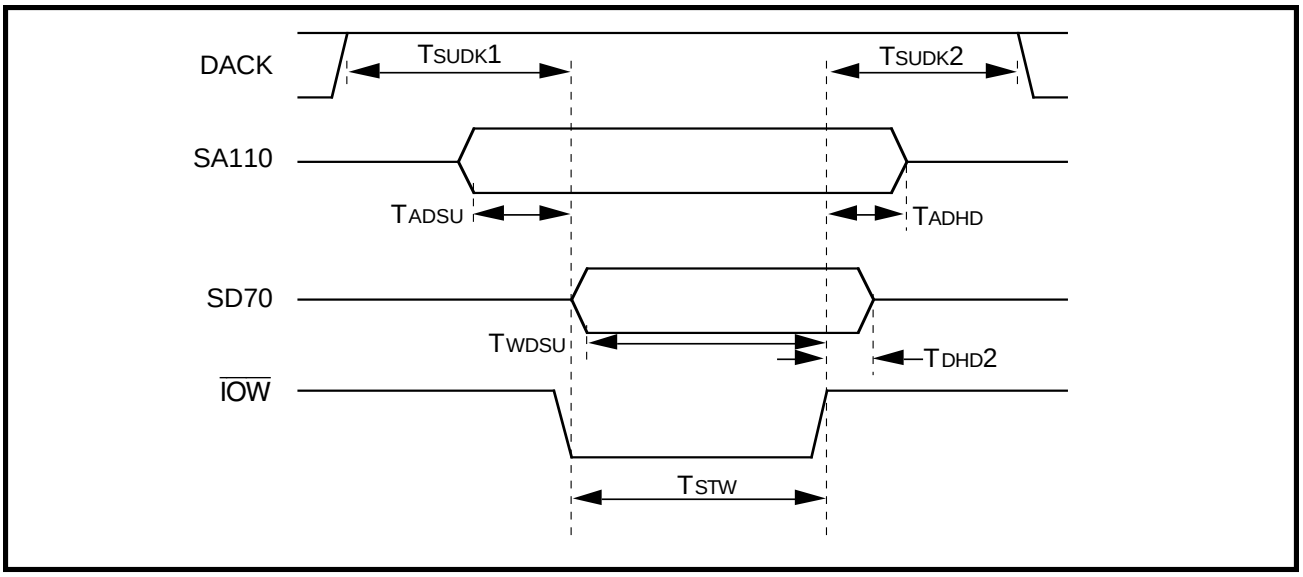


FIGURE 2: Control Register Write

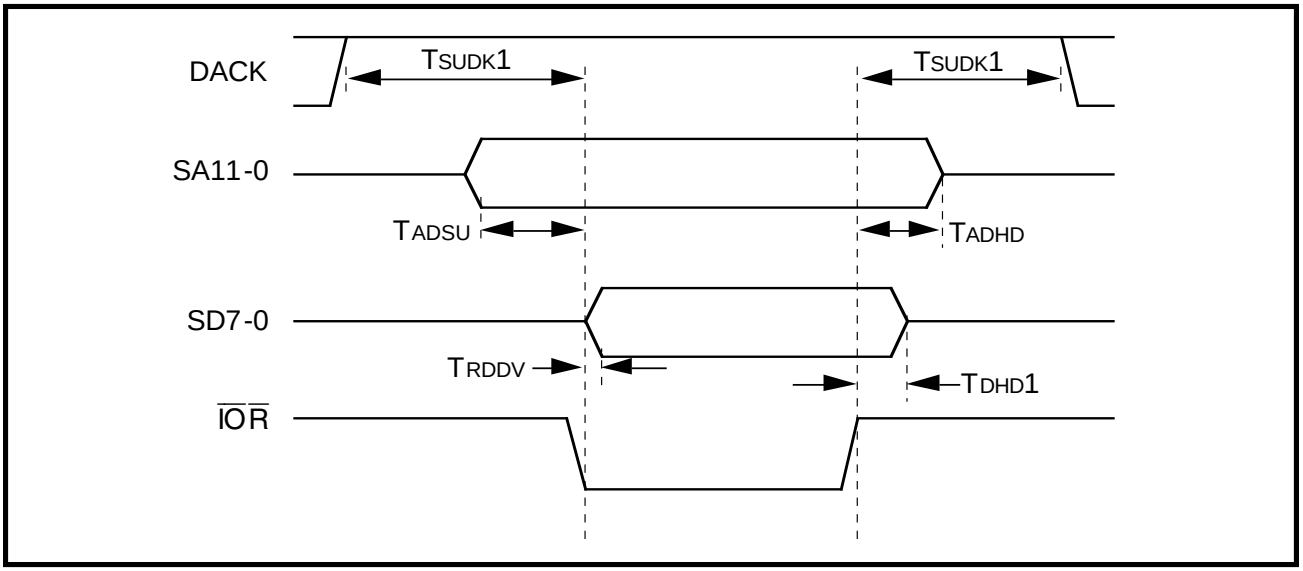


FIGURE 3: Control Register Read

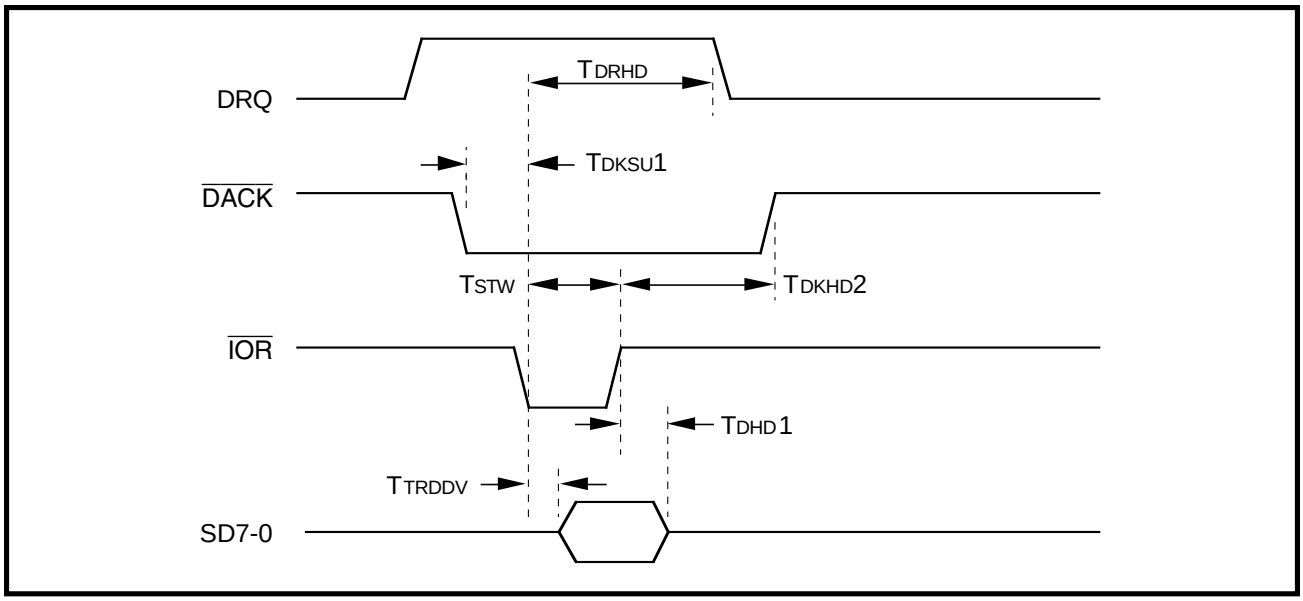


FIGURE 4: 8-bit Mono DMA Read

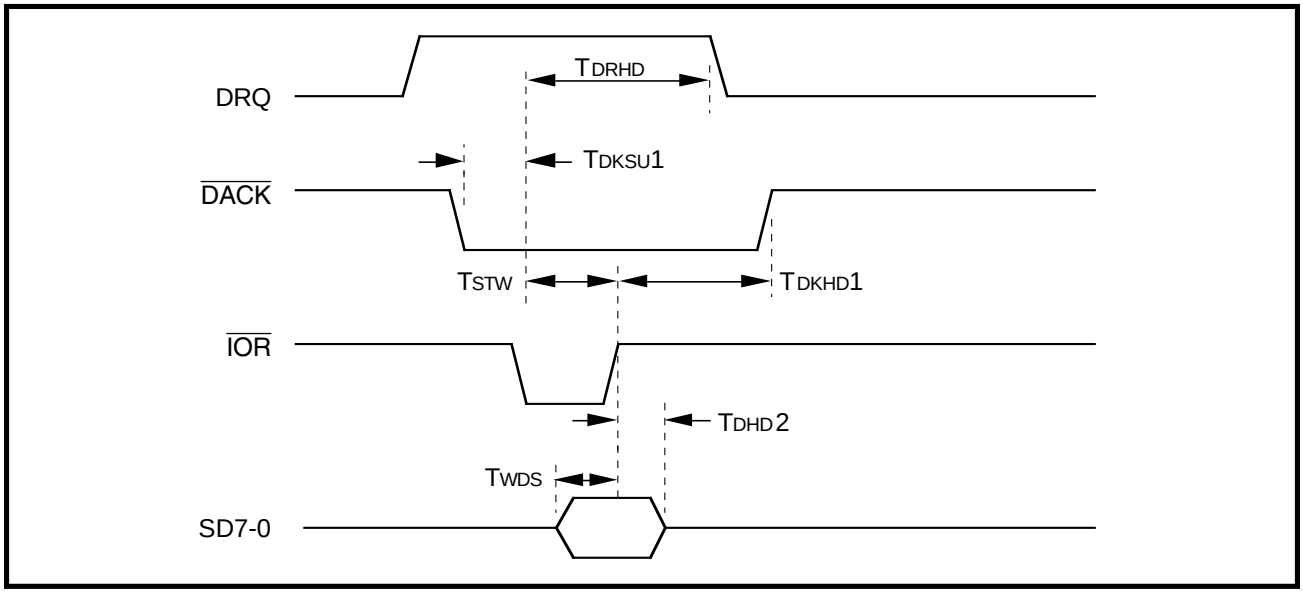


FIGURE 5: 8-bit Mono DMA Write

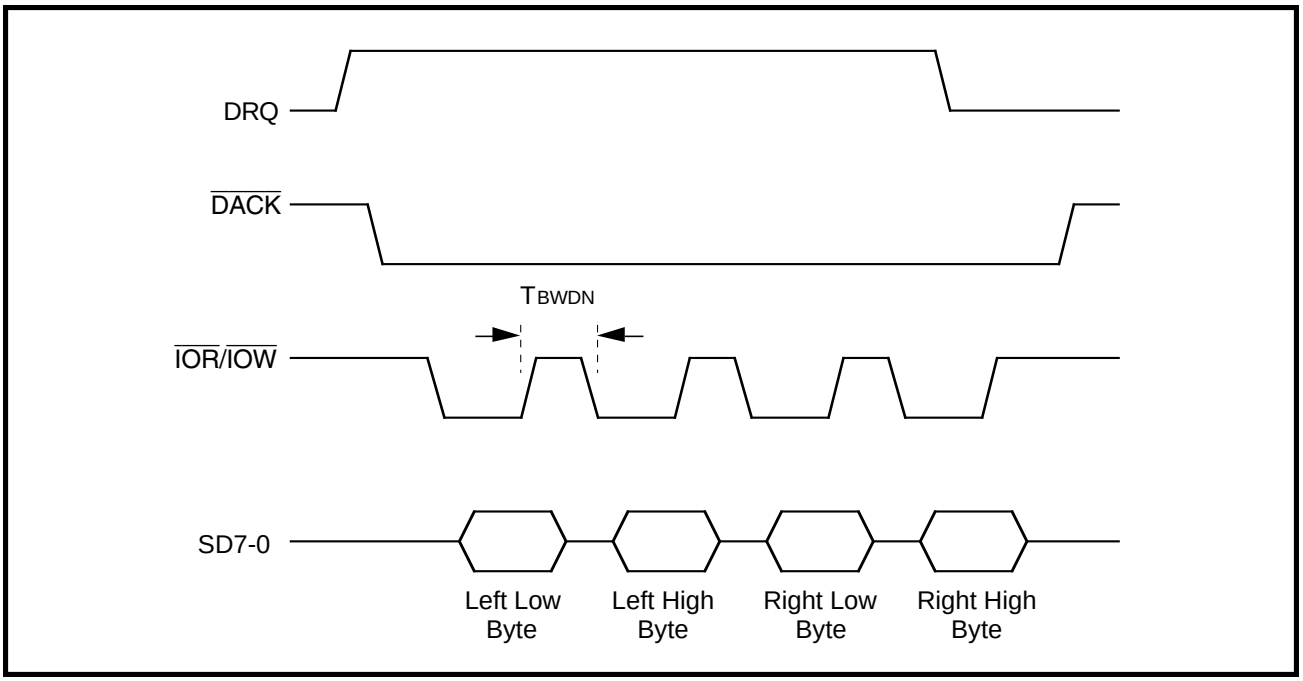


FIGURE 6: 16-bit Stereo DMA Read/Write

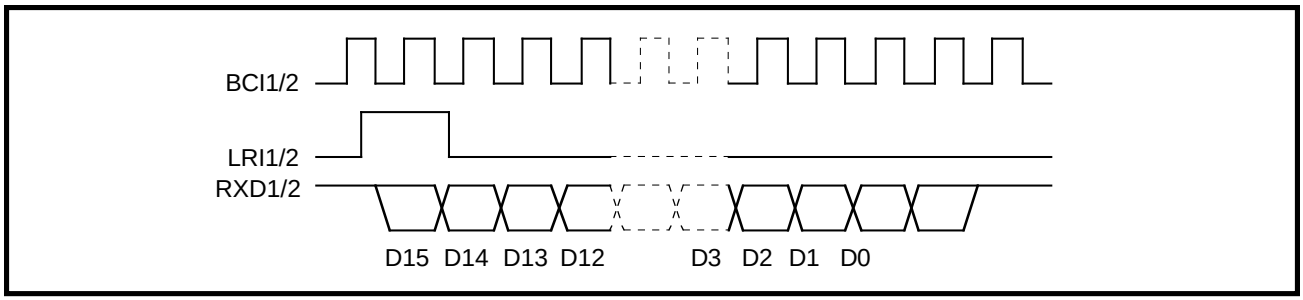


FIGURE 6: Receive Serial Port (16-bit Word, Pulse Sync Mode)

Refer to Master Control Index Registers

ID = 6:	BCI1/2P = 0	LRI1/2P = 0	RX1/2PULM = 0
ID = 7:	LRI1/2M = 1	RX1/2EN = 1	
ID = 8:	BCI1/2IO = 1	LRI1/2IO = 1	
ID = 9:	RX1/2DLY1-0 = 00	RX1/2LR = 1	
ID = 10:	RX1/2DIV1-0 = 10		

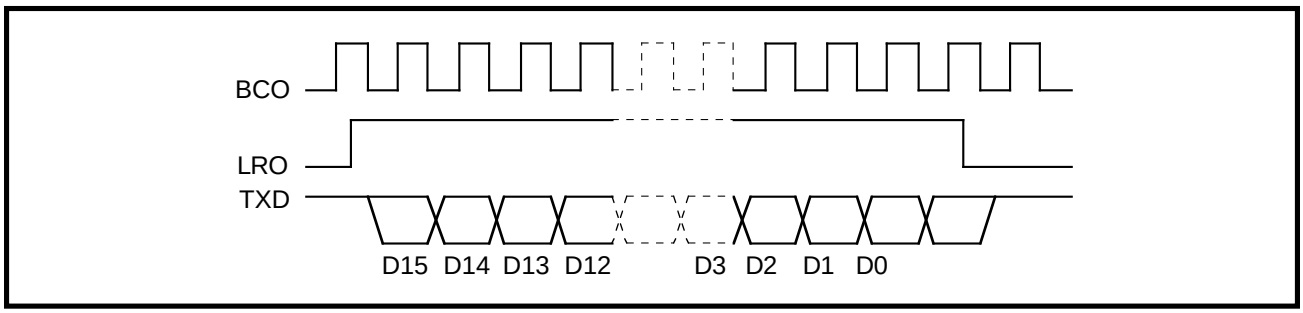


FIGURE 7: Transmit Serial Port (16-bit Word, Pulse Sync Mode)

Refer to Master Control Index Registers

ID = 6:	BCO = 0	LROP = 0		
ID = 7:	LROM = 1	TXEN = 1		
ID = 8:	BCOIO = 0	LROIO = 0	TXLR = 1	TXPULM = 1
ID = 9:	TXDLY1-0 = 00			
ID = 10:	TXDIV1-0 = 10			

TABLE 11: Pin Assignment 128-Lead QFP

PIN#	PIN NAME	TYPE	PIN#	PIN NAME	TYPE	PIN#	PIN NAME	TYPE	PIN#	PIN NAME	TYPE
1	$\overline{\text{IOCS16}}$	I	33	BD6	I/O4	65	MIDIRX	I	97	TEST	I
2	SA0	I	34	BD5	I/O4	66	MIDITX	O4	98	VA1	AP
3	SA1	I	35	BD4	I/O4	67	$\overline{\text{EPCS}}$	O4	99	GNDA1	AG
4	SA2	I	36	GND5	G	68	$\overline{\text{FMINT}}$	I	100	REFGND	A
5	SA3	I	37	BD3	I/O4	69	$\overline{\text{FMCS}}$	O4	101	VREF	A
6	SA4	I	38	BD2	I/O4	70	DRQ3	O4	102	FILTL	A
7	SA5	I	39	BD1	I/O4	71	DRQ1	O4	103	FILTR	A
8	SA6	I	40	BD0	I/O4	72	DRQ0	O4	104	GNDA2	AG
9	SA7	I	41	$\overline{\text{RES}}$	O4	73	$\overline{\text{DACK3}}$	I	105	VA2	AP
10	SA8	I	42	$\overline{\text{BRD}}$	O4	74	$\overline{\text{DACK1}}$	I	106	COM	A
11	SA9	I	43	$\overline{\text{BWR}}$	O4	75	$\overline{\text{DACK0}}$	I	107	$\overline{\text{GD4}}$	I
12	SA10	I	44	BA0	O4	76	VD1	P	108	$\overline{\text{GD5}}$	I
13	SA11	I	45	BA1	O4	77	GND1	G	109	$\overline{\text{GD6}}$	I
14	SAEN	I	46	BA2	O4	78	SRESDRV	I	110	$\overline{\text{GD7}}$	I
15	$\overline{\text{SIOR}}$	I	47	VD5	P	79	IRQ11	O4	111	$\overline{\text{GD0}}$	I
16	$\overline{\text{SIOW}}$	I	48	GND6	G	80	IRQ10	O4	112	$\overline{\text{GD1}}$	I
17	SD0	I/O16	49	GND7	G	81	IRQ9	O4	113	$\overline{\text{GD2}}$	I
18	SD1	I/O16	50	VD6	P	82	IRQ7	O4	114	$\overline{\text{GD3}}$	I
19	BOCS	O4	51	PLOCLK	O4	83	IRQ5	O4	115	SP/PWD	I
20	XTAL1O	I	52	GND8	G	84	LOR	A	116	GS	I
21	XTAL1I	I	53	VD7	P	85	LOL	A	117	CDDRQ	I
22	GND3	G	54	XTAL2I	I	86	AUX3R	A	118	CDDACK	O4
23	VD3	P	55	XTAL2O	I	87	AUX2R	A	119	$\overline{\text{CDEN}}$	O4
24	SD2	I/O16	56	BCO	O4	88	AUX1R	A	120	$\overline{\text{CMD}}$	O4
25	SD3	I/O16	57	LRO	O4	89	LINR	A	121	CD16EN	O4
26	SD4	I/O16	58	TXD	O4	90	MICR	A	122	$\overline{\text{NINT}}$	I
27	SD5	I/O16	59	BCI1	I	91	MONO	A	123	GND2	G
28	GND4	G	60	RXD1	I	92	MICL	A	124	VD2	P
29	VD4	P	61	LRI1	I	93	LINL	A	125	$\overline{\text{ST0}}$	O4
30	SD6	I/O16	62	BCI2	I	94	AUX1L	A	126	$\overline{\text{ST1}}$	O4
31	SD7	I/O16	63	RXD2	I	95	AUX2L	A	127	$\overline{\text{ST2}}$	O4
32	BD7	I/O4	64	LRI2	I	96	AUX3L	A	128	$\overline{\text{ST3}}$	O4

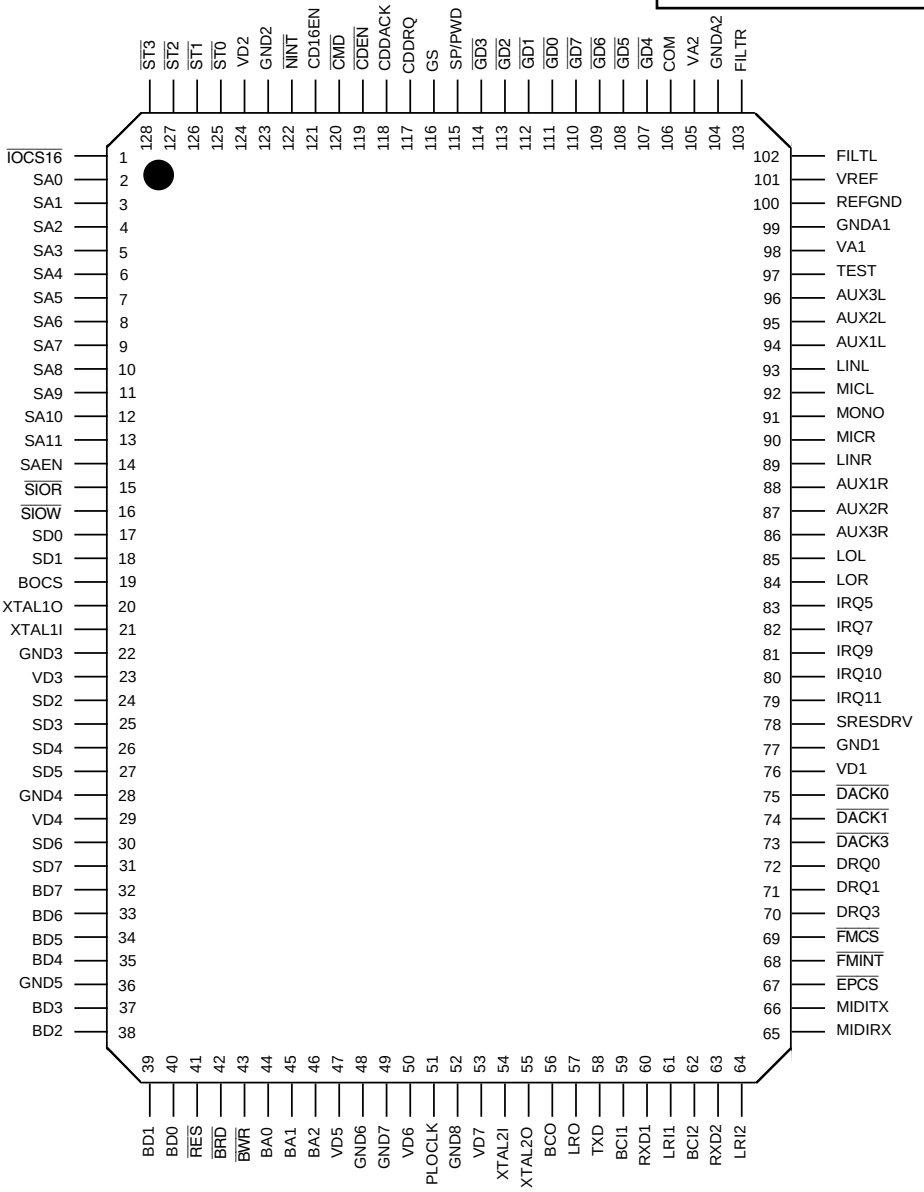
LEGEND:

I = Input (TTL Level)
I/O = Input (TTL Level) with 4 ma Output
AG = Analog Ground
O16 = Output with IOL = 16 ma
A = Analog I/O
P = Logic Power
O4 = Output with IOL = 4 ma
AP = Analog Power
G = Logic Ground

PACKAGE PIN DESIGNATIONS

(Top View)

CAUTION: Use handling procedures necessary for a static sensitive component.



128-Lead QFP

Advance Information: Indicates a product still in the design cycle, and any specifications are based on design goals only. Do not use for final design.

Silicon Systems, Inc., 14351 Myford Road, Tustin, CA 92680-7022 (714) 573-6000, FAX (714) 573-6914

Section 10

APPLICATION NOTES & GLOSSARY

We are sorry, the Setting DTMF Levels Application Note is not available in an electronic format. Please contact your local Sales office for more information or contact Silicon Systems directly to obtain a paper version.

Phone: (714) 573-6000
FAX: (714) 573-6914
E-mail: info@ssi1.com

Also, please visit SSi's World Wide Web home page at:

http://www.ssi1.com

Thank you.

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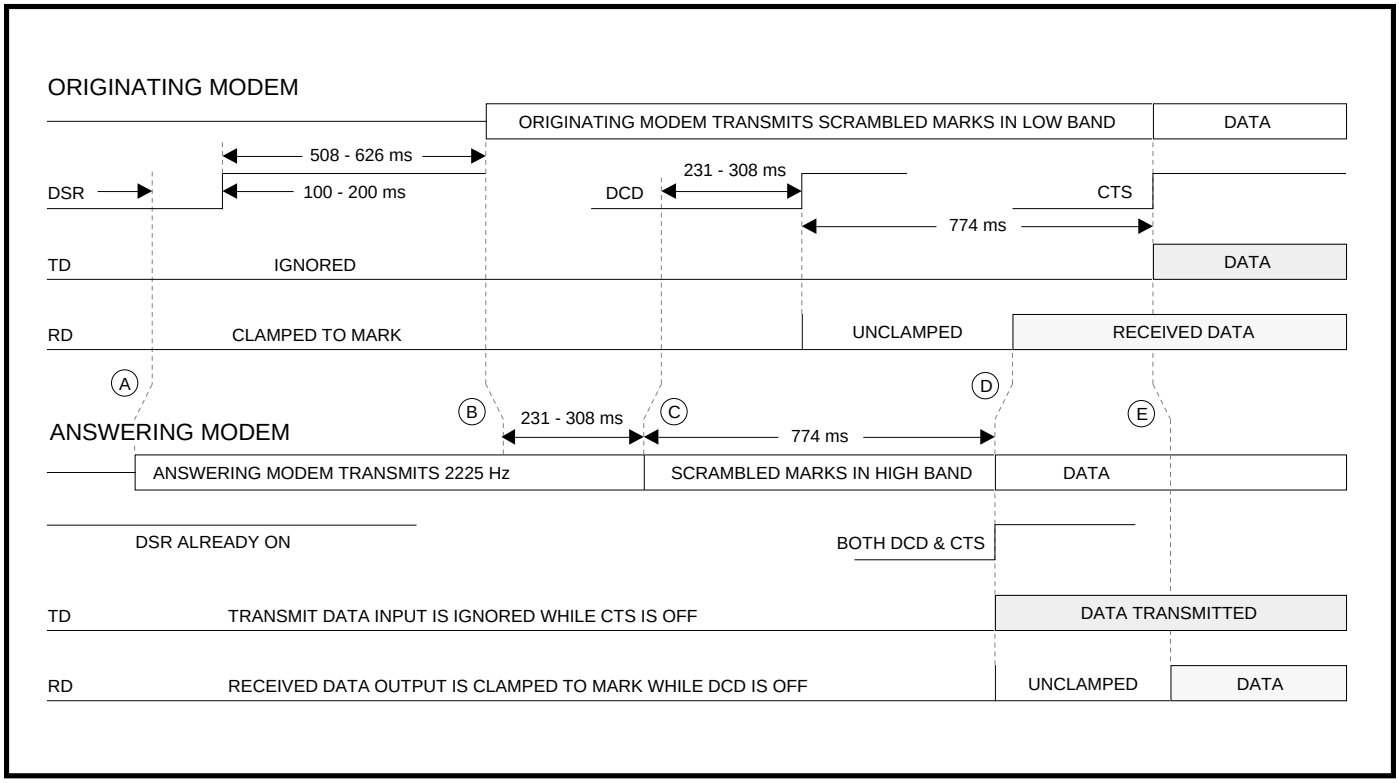
APPLICATION NOTE

SSI 73K212A High Speed Connect Sequence



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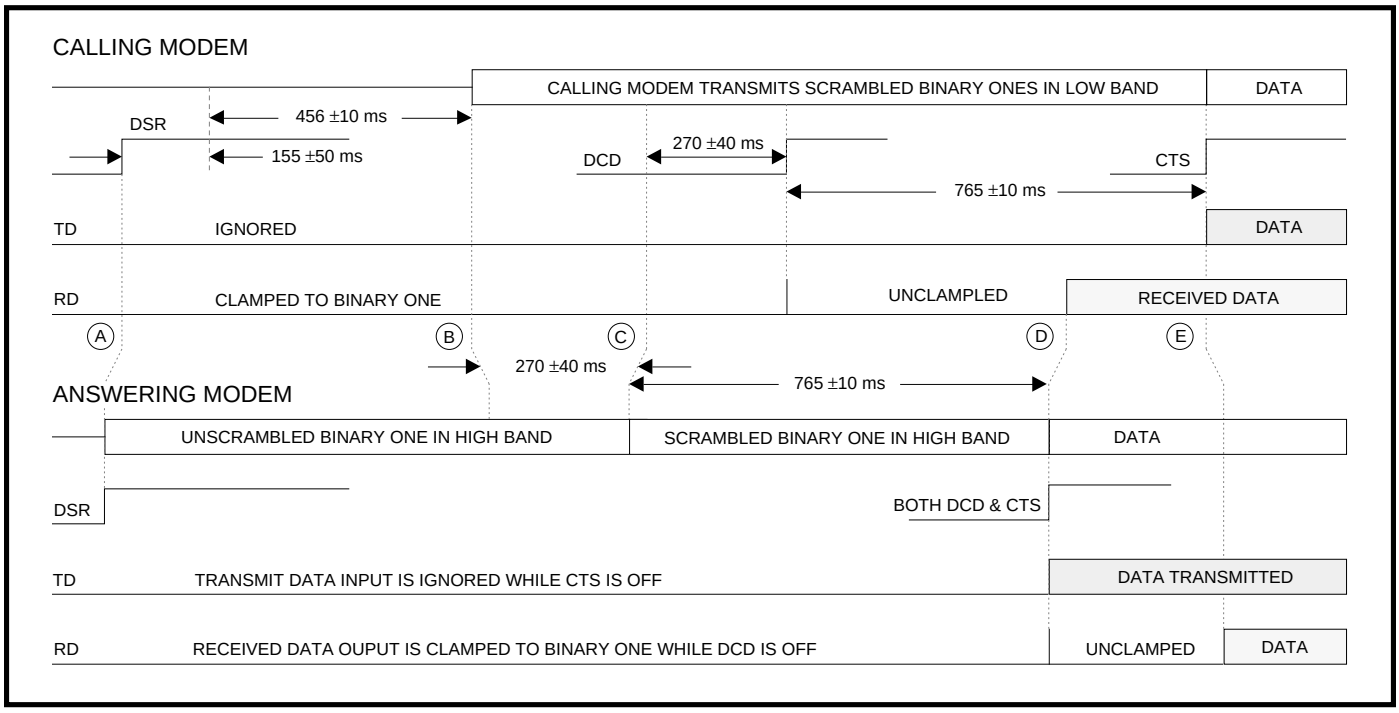
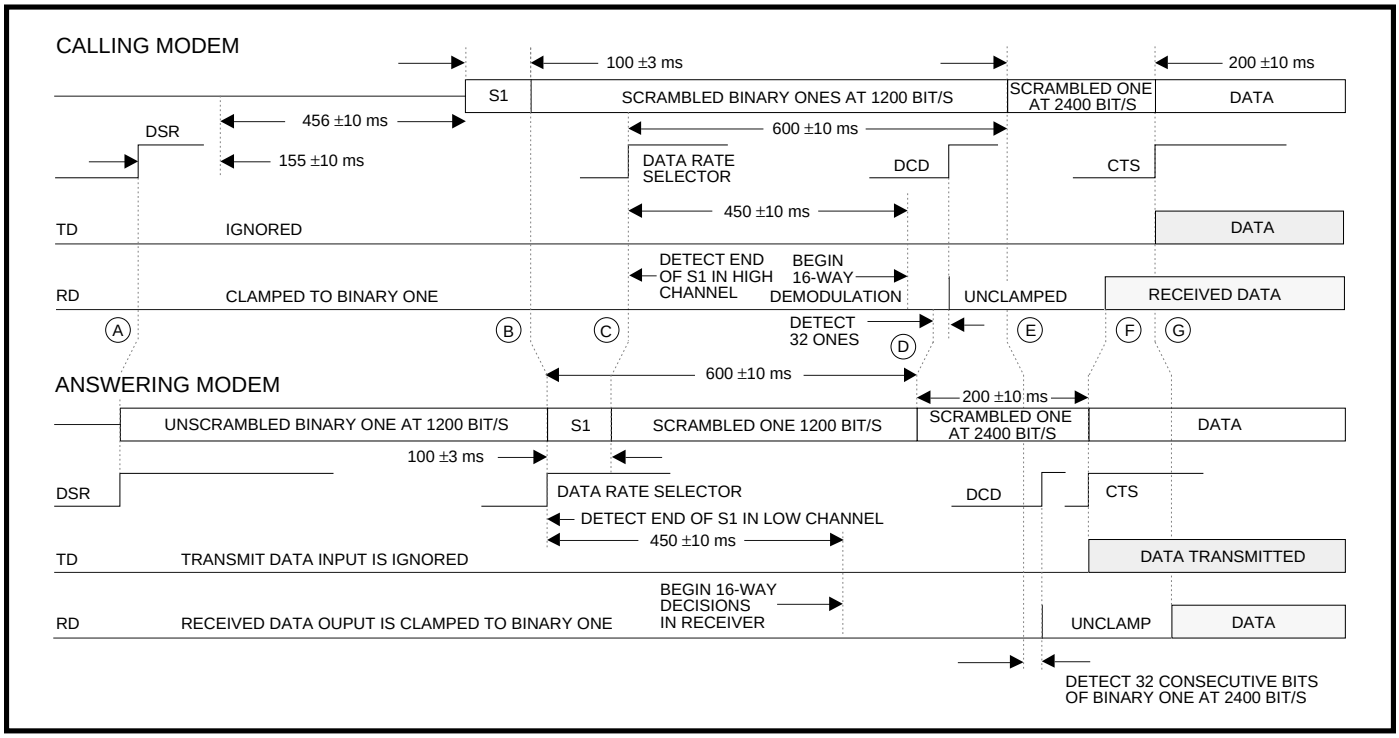
APPLICATION NOTE

V.22 & V.22bis Connect Sequences

V.22



V.22bis



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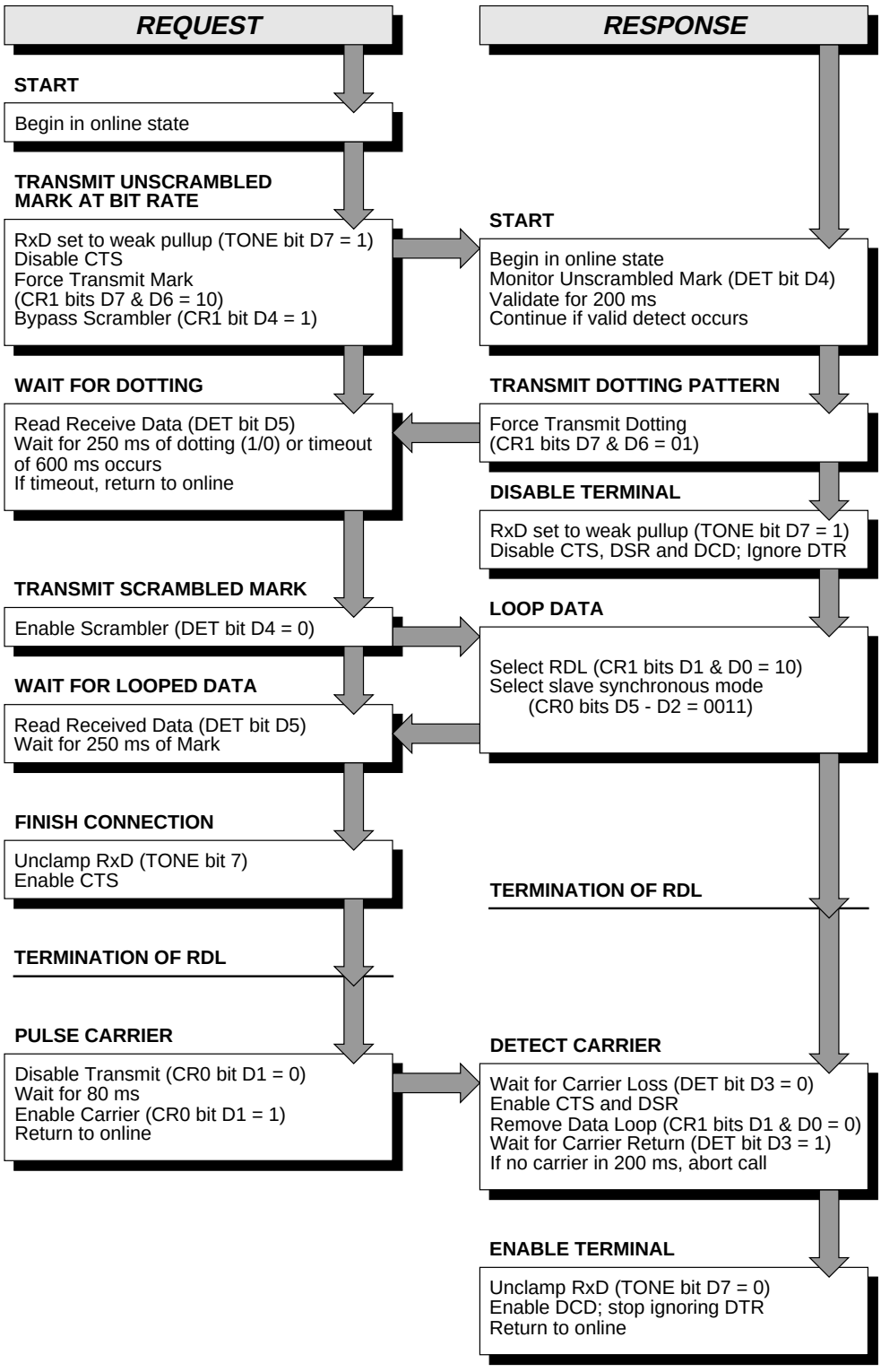
APPLICATION NOTE

Remote Digital Loop Back Handshake Sequence



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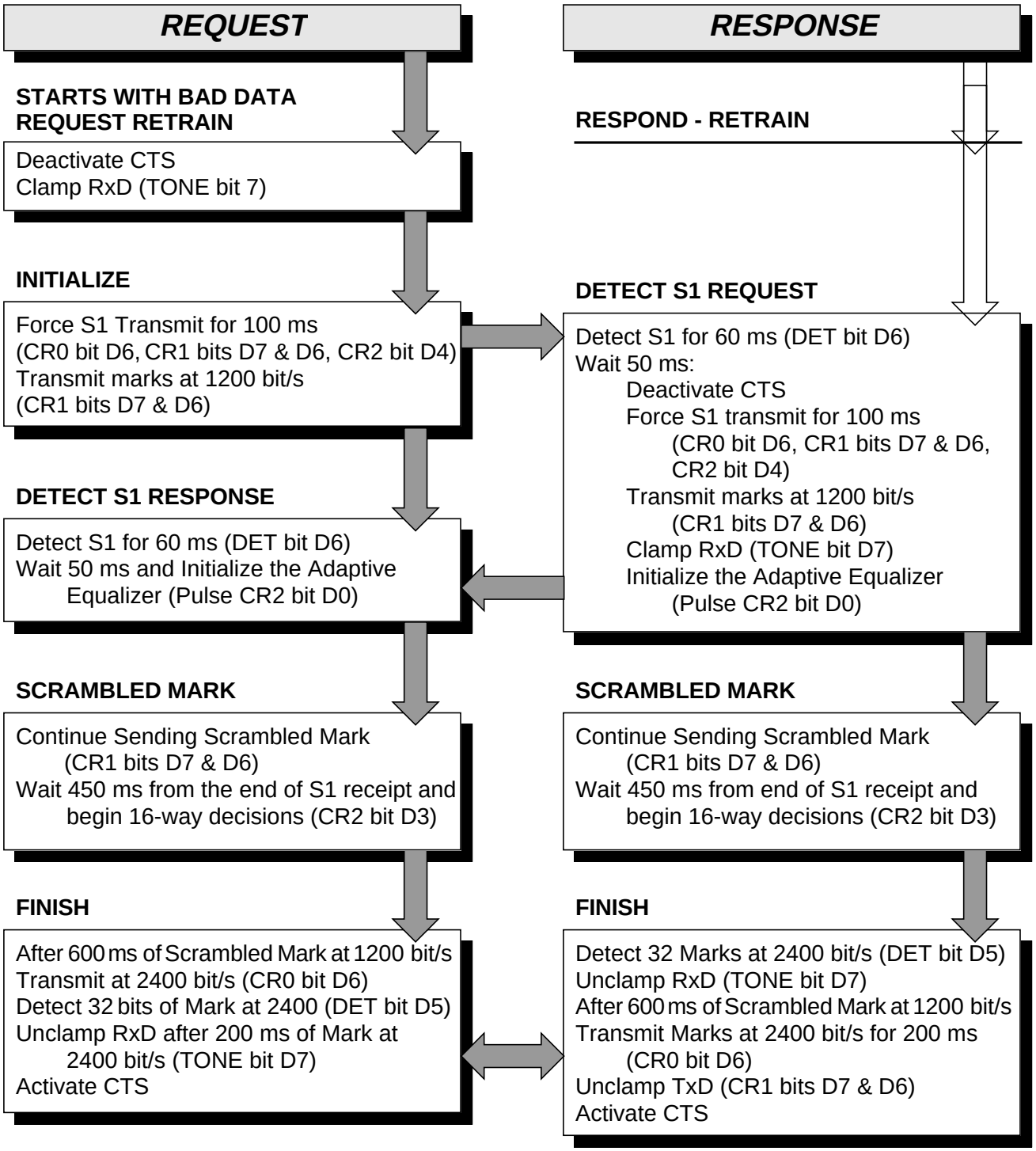
APPLICATION NOTE

SSI 73K224L
Retrain at 2400



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APPLICATION NOTE

SSI 73K212 & 73K222
Bell 212A, ITU V.22
Originate Handshake Sequence

(RXD is in tri-state mode, TONE bit D7=1)

DIAL
1. Go off hook
2. Bring out of power down mode (CR0 bits D5-D2)
3. Set DTMF tone (Tone bits D4-D0)
4. Turn on transmitter (Set CR0 bit D1)
5. Wait DTMF on time
6. Turn off transmitter (Clear CR0 bit D1)
7. Wait DTMF off time
8. Repeat 3-7 for all digits

WAIT FOR CARRIER
1. Start S7 (Wait for carrier) timeout
2. Set to Bell 103 originate mode (Set CR0 bits D5-D0 to 110001)
3. Wait for carrier detect bit (DR bit D3) to come on
4. Start sliding window counter (Wait through possible 2100 Hz answer tone period)
5. Qualify RXD mark* for 150 ms (DR bit D5) to detect answer modem (Carrier detect bit must also be on)
6. Raise DSR

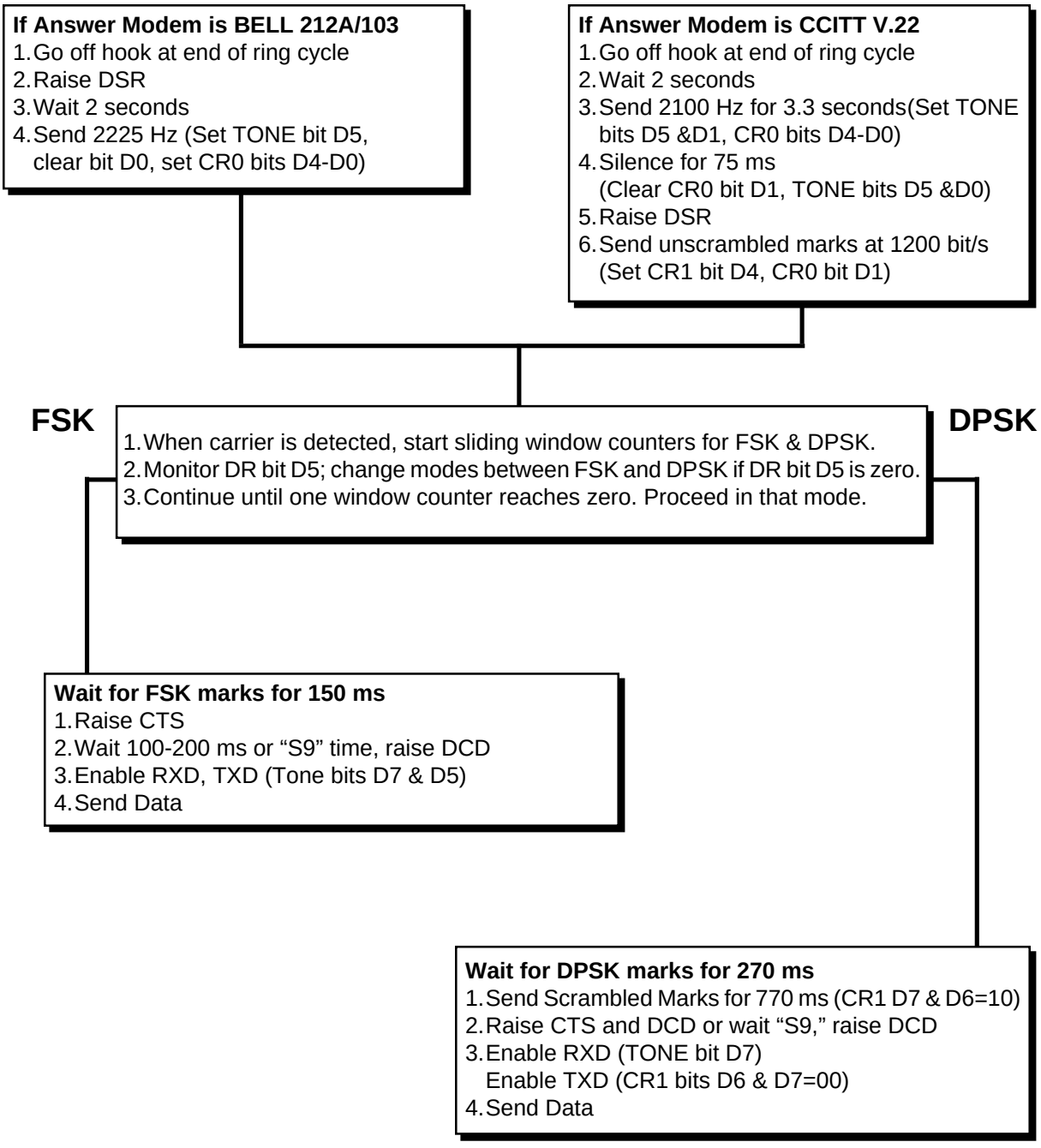
FSK
1. Wait 100-200 ms
2. Raise DCD, start 755-774 ms timer; wait 426-446 ms, send FSK marks (Set CR1 bits D7 & D6 to 10, set CR0 bit D1)
3. At end of 755-774 ms timer period (started in #2 above); raise CTS, unclamp RXD & TXD from marking (clear TONE bit D7; clear CR1 bits D7 & D6)

DPSK
1. Wait 456 (V.22) or 508-626 ms (212A), switch to DPSK
2. Send scrambled marks (Set CR1 bits D7 & D6 to 10)
3. Qualify scrambled marks from answer modem for 150 ms
4. Wait for 231-302 ms of scrambled marks, raise DCD
5. Enable RXD (Tone bit D7)
6. Wait 774 ms, raise CTS, enable TXD (Clear CR1 bits D7 & D6)

*This may be either answer tone from a Bell modem or unscrambled marks from a V.22 modem

SSI 73K212 & 73K222
Bell 212A, ITU V.22
Answer Handshake Sequence

(RXD is in tri-state mode, TONE bit D7=1)



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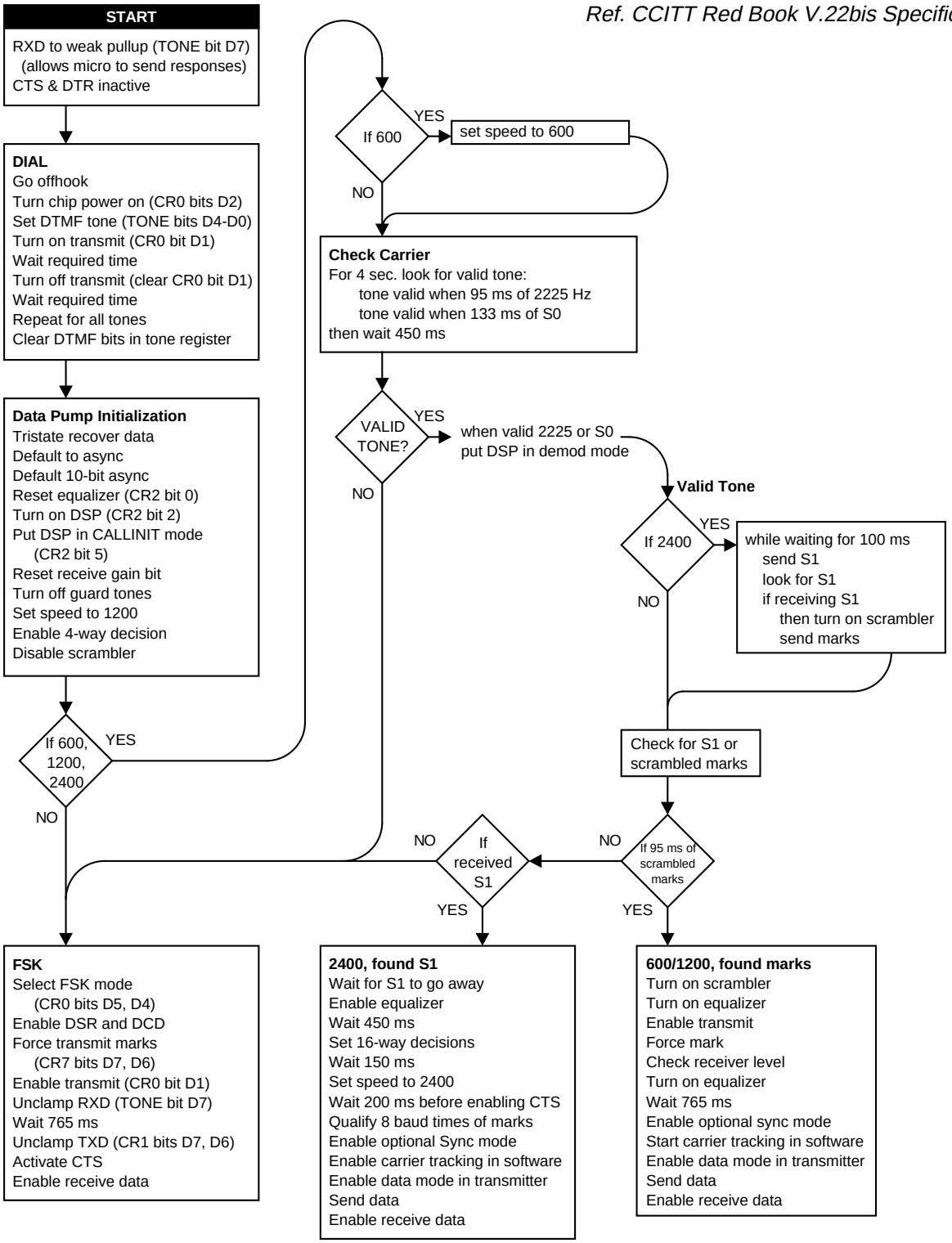
APPLICATIONNOTE

SSI 73K224L Originate Handshake Sequence

Ref. CCITT Red Book V.22bis Specification



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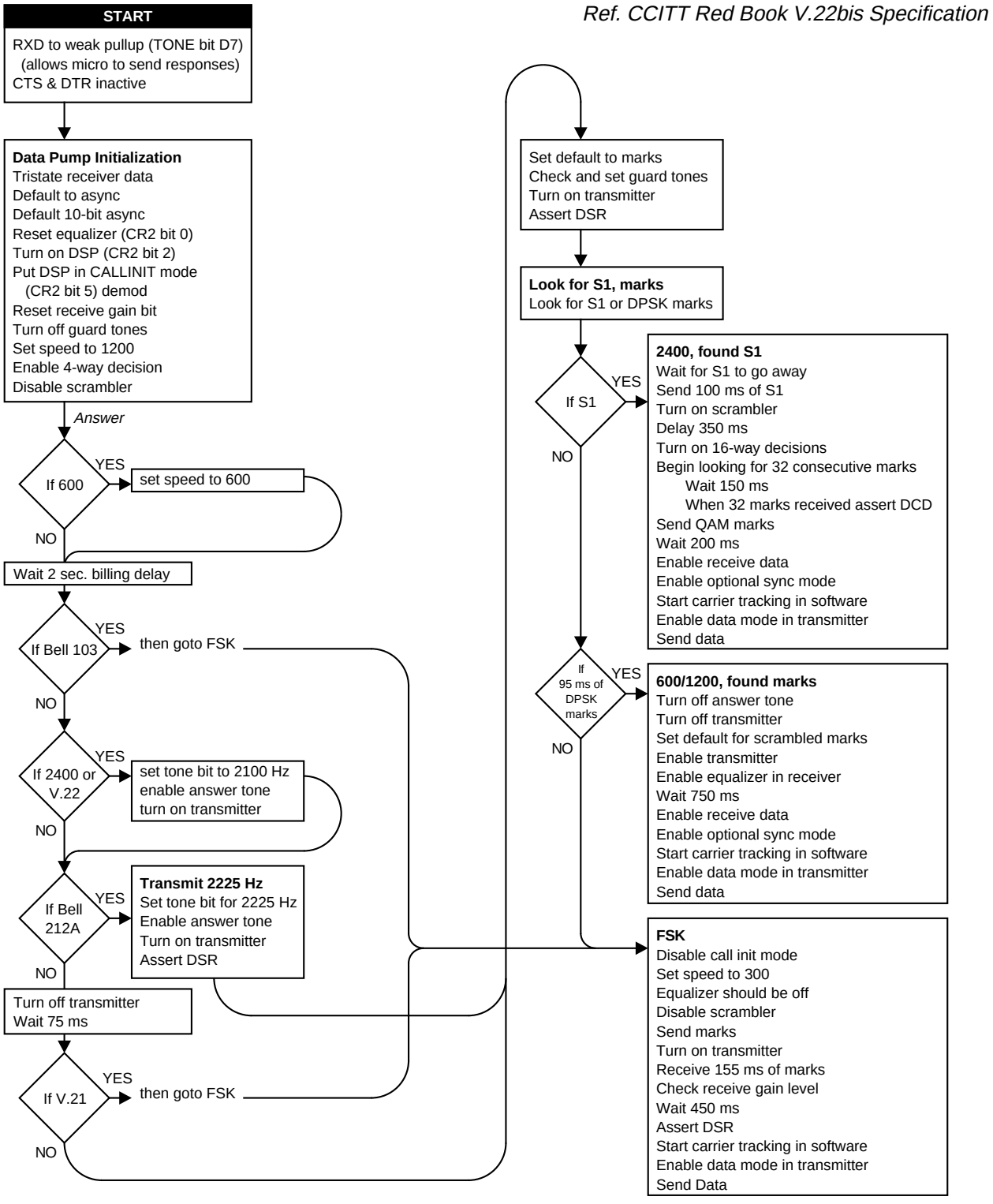
APPLICATIONNOTE

SSI 73K224L Answer Handshake Sequence

Ref. CCITT Red Book V.22bis Specification



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SSI 73K222U
Oscillator Start-Up

APPLICATION NOTE

March 1996

DESCRIPTION

There is an issue associated with oscillator start-up on some of the 73K222U devices. Some devices may require a 10 MΩ resistor in parallel with the capacitor on the XTL1 pin. As a precaution, we are advising customers to add this resistor to their designs.

The start-up problem is caused by negative feedback from the buffer stages following the oscillator inverter. This negative feedback cancels the desired positive feedback required for oscillation. This feedback exists only when the internal buffers are biased in their linear region as is the case on start-up. Once the oscillator has started, the buffer inverters act as digital switches and do not affect the sustained oscillation.

By adding the resistor from XTL1 to ground, the output bias point at XTL2 will shift upwards. There are several inverters connected in series buffering the crystal oscillator. Because the voltage at XTL2 has increased with the addition of the resistor, the input to the first buffer will be above its Vih threshold causing its output to be very close to ground. All subsequent inverters will be railed at their positive or negative limits.

When an inverter's output is railed high or low, the current through it will also be low. When the current fed into the chip internal power connections is low, the resulting feedback will also be low. The oscillator is then allowed to start properly.

Eventually the amplitude of the oscillations will grow to the point that all of the inverters in the chain start to switch. Feedback will be minimal because the inverters will be acting as switches swinging to the rails and not as linear amplifiers which consume more current and generate the negative feedback preventing oscillator start-up.

The addition of the 10 MΩ resistor has been proven to be effective in eliminating any oscillator start-up issues.

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APPLICATION NOTE

Troubleshooting the Modem Design

Excerpt from the Silicon Systems ***K-Series Modem Design Manual***

Possible Causes of a Totally Dead System

It is always particularly depressing when you power–up a new design for the first time and absolutely nothing happens. However, this is often the easiest type of fault to find. We will try to think of a few things that could cause this problem (apart from the obvious, like the plug falling out of the wall socket).

The K-Series Modem IC is Stuck in the Reset State

You will generally get very little cooperation from a K–Series modem IC while it is in the power-down state. It enters this state when a reset operation is performed, either by writing to the Reset bit (bit 2) in Control Register 1 or by taking the RESET input pin to logic ONE. Make sure that your firmware is bringing the part out of this state by writing something other than all ZEROs to bits 5 to 2 in Control Register 0. Also, make sure that this happens after the RESET pin has been returned to logic ZERO. A capacitor from this pin to VDD can hold the part in the reset state for many seconds. Attempts to program the part during this time will not take effect. For products with a DSP, check that the $\overline{\text{RESET}}$ $\overline{\text{DSP}}$ bit (CR2 bit D2) is also written with ONE when appropriate.

Crystal Oscillator Fails to Start

If a complete crystal oscillator is used to directly drive the K-Series modem, any starting problem should be addressed to the manufacturer of that device. If the internal oscillator is used with a crystal, there may be situations in which it will not start. Check the values of the capacitors from XTL1 and XTL2 to ground. If these are too high in value, 40 pF or above, the oscillator may not start. Such large values are not recommended and should not be necessary if the crystal is correctly specified. Also ensure that the circuit board is designed to minimize stray inductance and capacitance in the area of the oscillator. The crystal and both capacitors should be placed as close as possible to the XTL pins of the K-Series modem IC and connected by direct traces. The ground connection of the capacitors should be via wide traces to the nearest digital grounding system. It is also possible that the oscillator will not start or will be slow to start if the risetime of the power supply voltage is very long. The starting properties are helped by the asymmetry in the load capacitor values, the capacitor at XTL2 should be about twice as large as that at XTL1.

Clock to Microcontroller Isn't Getting Through

Using the K-Series modem ICs on-chip clock oscillator to generate timing for the entire system is very efficient from the point of view of component count and EMI generation. However, note that the CLK output of the modem chip is specified only to drive TTL compatible inputs. Many common microcontrollers require CMOS clock inputs that rise closer to the supply voltage for logic ONE. We have seen applications which use the CLK pin to drive these inputs without problem, however, parts may give a lower logic ONE level than is necessary at elevated temperature. We recommend that you use a TTL to CMOS level converting buffer between the CLK pin and the controller clock input in 5V systems. A pull-up resistor to the 5V supply is not effective in increasing the logic high voltage. In some cases capacitive coupling to a CMOS input is also ef-fective if the controller clock input is properly biased.

Connect Handshake Fails

If your system seems to be working well but cannot get into the situation of exchanging data with another modem, it is likely that you have a problem in the connect handshake. It is better to examine handshake problems using a "known good" modem at the remote end rather than another of your own systems. This helps isolate problems if more than one are present. Use a modem from an established and reputable manufacturer, as discounted generic modems may not conform fully to established specifications. Depending on the modulation mode, there may be many or few opportunities to fail so we can only offer general pointers to problems we have encountered in the past. It is very helpful to build extra diagnostic code into the handshake to diagnose unexpected conditions.

If things never start, check that the initial set-up of the chip is correct. The chip must be taken out of power-down before it will do anything and in DSP-based chips the DSP must have been reset after any previous call and then taken out of the reset state. (A DSP–based part cannot be used in a non-DSP socket without many such changes to the controller code; watch this when upgrading a 73K222L system to use a 73K224L.) If in CALLINIT mode the answer tone is not detected, check that you have selected the desired answer tone frequency by programming in the Tone Register. The selectivity of the answer tone detector is quite high, so verify that your answering modem is generating a frequency within the specifications of the modulation standard. You should be able to verify the operation of your various signal detectors with breakpoints in the controller code. If these do not fire at the appropriate point, the handshake is likely to hang-up or get out of step with the other modem. Be especially careful with the S1 detector, if this is failing you may get connections at 1200 bit/s which were supposed to be at 2400 bit/s. With DSP-based chips in QAM or DPSK modes, make sure that you are enabling the adaptive equalizer at the appropriate time. Enabling it too early, when the received signal is unsuitable for training, and too late, when there is too little time left before the gear shift to 2400 bit/s, can both give connect problems. Finally, make sure the crystal oscillator frequency is in specification as a error here can cause failure of the handshake.

Errors Committed Immediately After Handshake, With Later Improvement

We have seen situations in which a K-Series modem makes many data errors during the first few seconds of a connection, but then shapes up and performs normally thereafter. This is generally due to some problem in equalizer training in a DSP-based chip. The equalizer must be held in the initial state (bit 0 of CR2 = ZERO) up to the point in the handshake when scrambled DPSK binary ONES first appear at the receiver. It must then be released promptly (bit 0 of CR2 = ONE) and allowed to adapt so that it is fully trained before the gear shift to 2400 bit/s and the transition to data mode occurs. Enabling the equalizer too early will cause it to train on an unsuitable unscrambled signal. Because it adapts more rapidly immediately after being enabled, it may take a long time to recover from a bad solution when the correct receiver signal arrives. Enabling the equalizer too late reduces the time available for training before the received data is relied upon to be correct. If you have to put the equalizer back into the initialized state after a period of training, make sure that Equalizer Enable (bit 0 of CR2) stays at ZERO for at least 2 ms. It is better to have the Receiver Gain Boost bit dealt with before the equalizer is enabled, otherwise transients caused by changing this bit may upset the equalizer solution.

Errors Experienced at High Receive Signal Levels

If the error rate gets worse at high receive signal levels, you should look for some source of clipping in the receive path. Injecting a signal of known level at the line coupling transformer and looking at the RXA pin with an oscilloscope should enable you to isolate any problem in the line interface. Look for excessive gain in the receiver buffer amplifier or other causes of clipping at this point such as badly chosen op-amps for single 5V supply operation. If the signal at RXA looks good and you are using a DSP-based modem chip, it is possible that the controller is incorrectly inserting the 12 dB receiver gain boost even if the Receive Level bit in the Detect Register is set. Only set Receive Gain Boost if this bit is ZERO.

Errors Experienced at Low Receive Signal Levels

There can be many causes of data errors at low receive signal levels, almost all associated with the presence of some level of interference or noise in the receive path. If you are performing tests over the telephone network, make sure that the error rate you are experiencing is not to be expected from the background noise level on the line. It is best to use a line simulator or a direct connection through an attenuator if looking for system noise problems. The capacitor across the feedback resistor of the receiver buffer amplifier is important to attenuate out-of-band noise at the modem chip receiver input.

Distortion in the telephone line interface can be located by injecting low-level signals into the line terminals and examining the signal at the RXA pin with a spectrum analyzer. Look for crossover distortion in the receiver buffer amplifier. This can arise from a poorly chosen op–amp type, such as the LM324 which makes a transition from class A to class AB operation at low signal levels and is not suitable for this application. We have found LM348 and LM1458 type op-amps to be free from this problem. It is also possible for the line coupling transformer to introduce harmonic distortion, particularly when a large D.C. holding current is flowing.

In the absence of significant distortion, look for a high noise level at the RXA pin. Another symptom of this problem, apart from data errors, is that the Carrier Detect bit (bit 3 in DR) comes on or blinks when no signal is applied to the modem receiver. The system may also fail to disconnect at the end of a call. If this is

your experience don't confine your search to the normal carrier bandwidth because the modem chip will also be susceptible to higher frequencies. Op-amps may be noisy or may self-oscillate at low level due to poor layout. If the op-amps themselves are not causing the noise, it may be due to poor circuit layout or grounding. If, finally, nothing suspicious is visible at the RXA pin then the noise must be getting into the receive signal inside the modem IC. This can be from the power supply and bias pins or from signals routed under the chip. Check the connections to GND, VDD, VREF and ISET pins for component values and placement and routing of decoupling components. You are more likely to have problems with supply noise if you are using a switching power supply. Look also for fast digital signals routed under the modem IC; these should be re–routed and a ground plane placed under the chip. Serious interference pickup problems can be created by two crystal oscillators producing beat frequencies in-band to the modem. We strongly recommend using one master crystal in the system. Check the gain in the receive path from the line terminals and, in DSP-based parts, the state of the Receive Gain Boost bit set by the controller. If either of these are incorrect, then noise in the chip will appear more significant compared to the signal.

The transmitter of the modem can be a source of noise in the receiver. It should not generate signals that are in–band to the receiver, but this can happen if either the buffer amplifier or the line transformer are causing harmonic distortion. This will be most noticeable in call mode, when the low band transmit signal has harmonics in the high band of the receiver. For 5V only systems, the choice of op-amps in the buffer amplifier and their D.C. bias point is crucial to obtaining a sufficient voltage swing without distortion. Because of its internal operation, a small amount of switching noise is present at the TXA pin. The capacitor across the buffer amplifier feedback resistor is important to prevent this signal from reaching the receiver. It is difficult to obtain good rejection of the transmit signal at the receiver for all practical line conditions, but you should check that your two-wire to four-wire hybrid circuit is operating correctly. For most terminations, the transmit signal at the RXA pin minus the receive buffer gain should be 6 dB below the level at the line.

Modem Works in Loopback but Fails to Connect or Makes Errors in Bursts with Some Other Modems

If anything appears "flaky" about the modem operation it is a good idea to check the oscillator frequency with a counter capable of resolving to at least ten parts per million. Using an oscilloscope is of no use whatsoever. Many systems that use crystal oscillators are not very particular about the exact frequency; this is not so of modems. Measure the frequency at the CLK pin and verify that it is between 11.0581 MHz and 11.0603 MHz. Do not measure at the XTL1 or XTL2 pins as the probe capacitance will alter the frequency of oscillation. Some causes of out–of–specification readings are: a) the wrong crystal frequency entirely, b) a series-resonant crystal, or c) a parallel-resonant crystal unmatched to the circuit capacitance.

Problems Unique to FSK Modes

The SSI 73K224L does not permit answer tone detection in FSK modes, so ensure that a mode other than FSK is selected before attempting to detect answer tones.

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SSI 78P7200
Demo Board

APPLICATION NOTE

March 1996

DESCRIPTION

The 78P7200 demo board is designed to facilitate the evaluation of the SSI 78P7200 single chip DS3/E3/STS-1 transceiver IC. The demo board includes all of the necessary discrete components for the interface to a coded AMI line. A DIP switch allows easy control of the option pins on the IC. A loopback function is easily implemented using jumpers. The 78P7200 Demo board accepts 28-pin PLCC ICs.

FEATURES

- **Allows easy evaluation of the 78P7200**
- **Includes all necessary external components**
- **Includes digital loopback jumpers**
- **Can be modified to work at DS3, E3 and STS-1 rates**
- **Allows the use of either the receive clock or an external clock as the transmitter clock**
- **4 layer PC board construction**

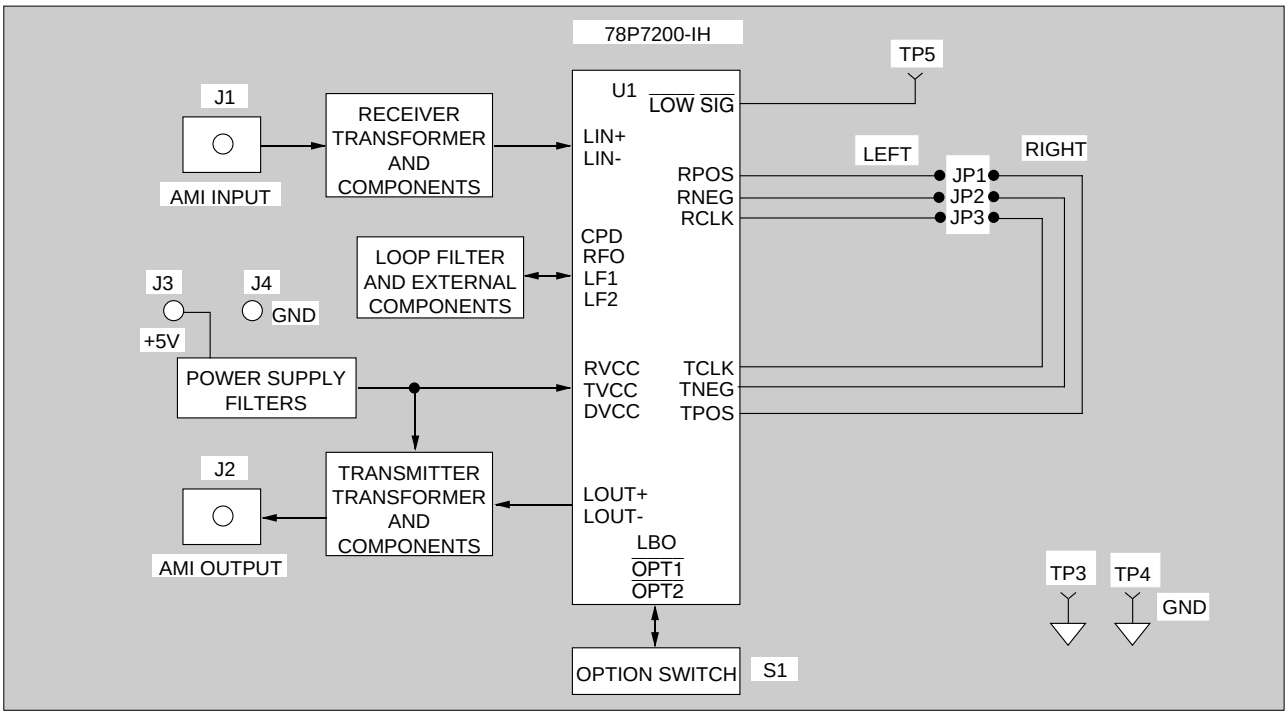

FIGURE 1: Demo Board Block Diagram

SSI 78P7200
Demo Board

POWER SUPPLY CONNECTION

The demo board is constructed as a four layer PC board. The outer two layers carry the signals. The internal two layers are the ground and power supply planes. The power supply planes are connected to a single +5V banana jack (J3) using LC filters of 4.7 μH and 0.1 μF.

RECEIVE SIGNAL PATH

The AMI signal is connected to the BNC connector J1. The maximum recommended distance of the demo board to a DSX crosspoint is 450 feet. The IC can handle added resistive attenuation. The IC recovers clock, positive and negative data from the AMI signal. The following table shows the available receiver logical signals on the test points.

TEST POINTS	SIGNAL	
TP5	$\overline{\text{LOW}}$ $\overline{\text{SIG}}$	U1-27
JP1_Left	RPOS	U1-25
JP2_Left	RNEG	U1-24
JP3_Left	RCLK	U1-23

The AMI input signal should be properly coded to prevent a long run of zeros on the line. The proper code should limit the number of zeros to three. The following table shows the proper coding required:

78P7200 RATE	SPEED Mbit/s	MAX zeros	CODE NAME
DS3	44.736	2	B3ZS
STS-1	51.840	2	B3ZS
E3	34.368	3	HDB3

The input circuit for DS3 and STS-1 versions of the demo board uses a 1:1 transformer and termination resistor (R4) and capacitor (C2).

The E3 version of the demo board is loaded with components which form a descrete filter. The AMI input signal to the IC can be monitored using a high impedance FET probe such as TEKTRONIX P4064 or HP 1141A.

The input signal is coupled through wideband transformer. The following table shows some of the suggested manufacturers of this part:

Receiver transformer DS3 and STS-1

MANUFACTURER	PART NO.
Pulse Engineering	PE-65966
Mini-Circuits	T1-1
Coilcraft	WB1010-PC
Valor	PT5044
VITEC	14Z3276

Receiver transfromer E3

MANUFACTURER	PART NO.
Pulse Engineering	PE65969
Mini-Circuits	T4-1
Valor	PT5045
VITEC	14Z3277

Table 1 shows the required external components for different speeds. Resistor R5 sets the center frequency of the oscillator. Resistors R12, R13 and capacitor C8 controls the jitter characteristic of the IC.

TRANSMIT SIGNAL PATH

The IC accepts CMOS level NRZ logical inputs (TCLK,TPOS,TNEG) and converts them to the proper AMI signal. Inserting jumpers JP1, JP2, JP3 allows a digital loop back. The following table shows the test points used for the transmitter.

TEST POINT	SIGNAL	
JP3-Right	TCLK	transmit clock input
JP2-Right	TNEG	transmit negative data
JP2-Right	TPOS	transmit positive data

The output pins of the 78P7200, LOUT+ and LOUT-, are connected to a 1:1:1 wideband transformer. The following table shows some of the suggested transmitter transformers:

MANUFACTURER	PART NO.
Pulse Engineering	PE-65969
Mini-Circuits	T4-1
Valor	PT-5045
VITEC	14Z3277

The transformer center tap is connected to the +5V supply through a filter comprised of a 4.7 μH inductor and a 0.1μF capacitor. The capacitor C6, when added to the PC board trace and the transformer input capacitances, will effect the pulse shape. This capacitor should be selected for individual PC boards. The objective is to meet a pulse template at any cable length up to a maximum of 450 feet. The generated AMI signal is available on the BNC connector, J2, and it can be monitored using a high impedance probe.

OPTION PINS CONTROL

Switch S1 changes the logic level of the option pins which control the transmitter. Table 2 shows the function of this switch.

PERFORMING TESTS WITH DEMO BOARD

The general test setup using the demo board is shown in Figure 2. When jumpers JP1, JP2, JP3 are inserted (loopback), the receiver logic output signals (RCLK, RPOS, RNEG) from the IC are connected to the transmitter logic inputs (TCLK, TPOS, TNEG). As a result, the received AMI signal is transmitted back to the test equipment. Monitoring bit error rate indicates the ability of the IC to receive and transmit the AMI signal with no errors.

As shown in Figure 2, 450 feet of 75 ohm coaxial cable (type RG59B) and resistive attenuation are inserted in the receive path to exercise the IC for its lowest input level. The following tests are performed on the receiver:

BIT ERROR RATE TEST

A pseudo-random pattern is generated by the test equipment. This pattern is created using a shift register of N bits. Preventing an all zero pattern, a combination of 2**N-1 patterns of N bits is created in a random manner. This pattern is used to simulate the live traffic on the AMI line. The following table shows the mostly used patterns to test the IC:

SPEED	RANDOM PATTERN	FIXED PATTERN
DS3	2**15-1	100100…
STS-1	2**15-1	100100…
E3	2**23-1	10001000

When running these patterns, no bit errors are expected in the absence of any noise. The test is repeated for fixed patterns to exercise the IC for any pattern sensitivity.

JITTER TOLERANCE

Telecommunication equipment should be able to recover clock and correct data even if the AMI signal includes a reasonable amount of timing jitter. For this test, the test equipment adds jitter to the random AMI signal. For jitter at a set frequency, the jitter amplitude is slowly increased until bit errors are observed. This process is repeated at different frequencies and a plot of the maximum tolerated jitter vs the jitter frequency is made as shown in Figure 3. The system should tolerate jitter in excess of specified requirements.

INTRINSIC JITTER

The jitter generated by the IC in the absence of any jitter on its transmitter logical input (TCLK, TPOS, TNEG) is minimal.

JITTER TRANSFER FUNCTION

The IC should not cause any amplification of the system jitter, i.e., very small peaking should be observed in the jitter transfer function. This objective is achieved by selecting the PLL filter components for an overdamped response. The test equipment adds jitter to the AMI signal received by the IC. Measuring the jitter transmitted by the IC in the digital loopback mode indicates the shape of the transfer function. As shown in Figure 4, the IC adds very small peaking and higher frequency jitter is attenuated.

TRANSMITTER TESTS

The AMI pulse generated by the IC can be tested for its shape, amplitude and frequency content over different lengths of cable. The demo board is usually placed in the loopback mode (by adding jumpers JP1, JP2, JP3).

PULSE FREQUENCY CONTENTS

For an AMI signal with an "all ones" pattern, the transmitted signal should have a frequency spectrum with the main component at half of the bit rate. The signal power at the harmonics including the component at the bit rate should be at least 20 dB lower than the main component. A spectrum analyzer is used for this purpose.

PULSE AMPLITUDE

The pulse amplitude for a pattern of 100100... is measured at different cable lengths by connecting the end of the cable to the scope using a 75 ohm termination adaptor (POMONA 4119). For the E3, speed, the transmitted pulse amplitude needs to be fairly exact (2 Vp-p ± 10%). For DS3 and STS-1, the transmit amplitude may fall in a wide range of amplitudes from 0.72 to 1.7 Vp-p.

PULSE TEMPLATE

The shape of the signal at the end of a 75 ohm cable is examined by comparing it to the published templates. The test setup is shown in Figure 2. The program resident in the computer reads the transmitter waveform from the scope, scales it vertically, and plots it together with the published template masks. The pulse shape should meet the mask for all cable lengths from zero to 450 feet. The LBO pin as controlled by switch S1-1 should be properly set as shown in Table 2. A typical pulse shape for the 78P7200 at the end of 450 feet of cable is shown in Figure 5.

PULSE IMBALANCE

The AMI pulse generated by the IC includes pulses of both negative and positive polarities. The pulse imbalance is examined by inverting the negative pulse using the scope and overlaying it on a typical positive pulse. No significant imbalance is observed.

TABLE 1: External Components List for Different Speeds

Data sheet ref.	CTR	RFO	RTR	E3 FILTER					T_1	C_{TT}	R_{TT}
Demo board ref.	C2	R5	R4	R1, R2	C_1	C_X	L_1	L_X	T_1	C6	R8
Unit	PF	kΩ	Ω	Ω	PF	PF	µH	µH	-	PF	Ω
Tolerance	10%	1%	1%	1%	5%	5%	5%	5%	3%	10%	1%
DS3	5	5.23	75	SHORT	OPEN	OPEN	OPEN	OPEN	1:1	15	301
STS-1	5	4.53	75	SHORT	OPEN	OPEN	OPEN	OPEN	1:1	15	301
E3	Open	6.81	422	75	82	1000	0.47	6.8	1:2	3	604

Note 1: C_{TT} should be selected to meet the template at short cable. CTR and CTT values are selected for SSi 78P7200 demo board and may need to be modified for the customer PC board.

TABLE 2: Function of the DIP Switch S1

Position	IC Pin	Function	Open	Closed
S1-1	LBO	TX cable length	L < 225'	L > 225'
S1-2	$\overline{\text{OPT1}}$	TX amplitude	Normal	Boost 2.7 dB
S1-3	$\overline{\text{OPT2}}$	TX disable	Enable	Disable

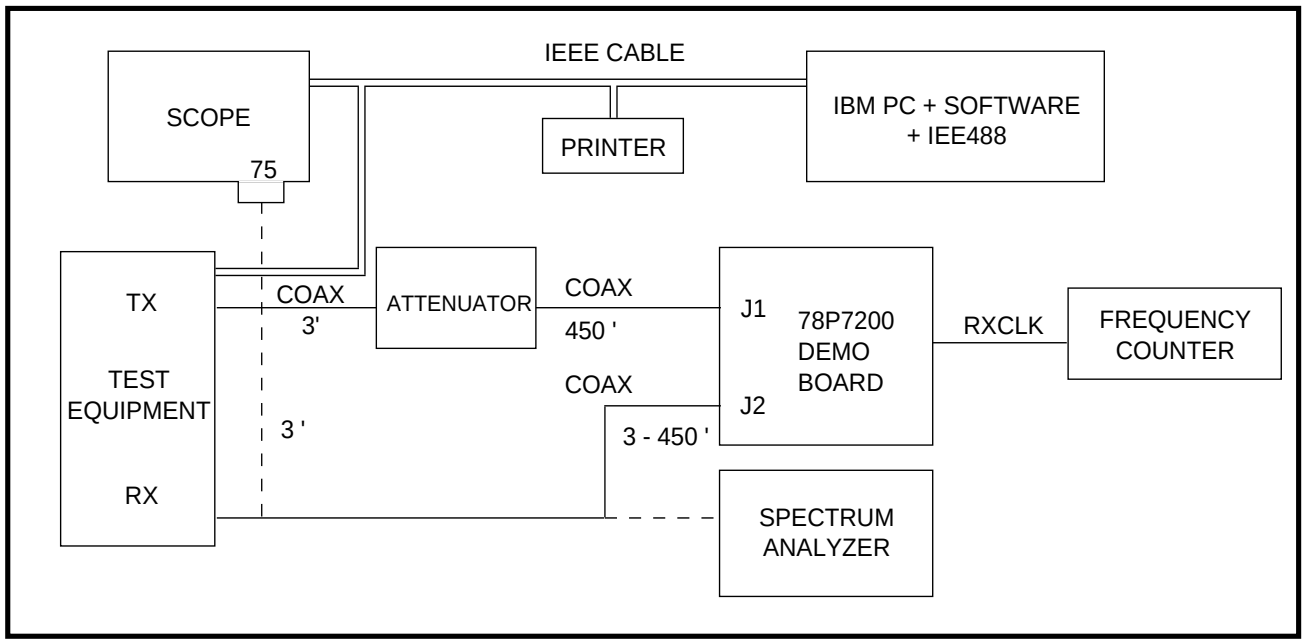

FIGURE 2: General Test Setup

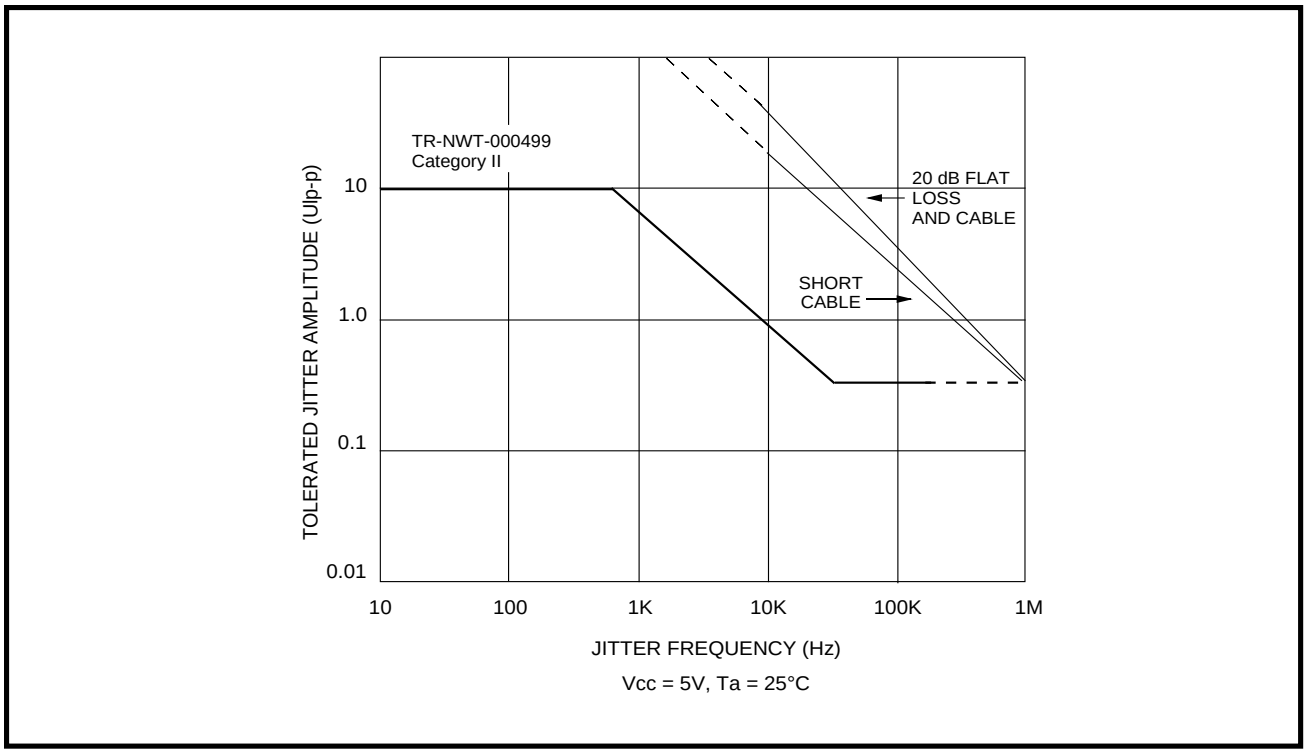

FIGURE 3: Jitter Tolerance for 78P7200 at DS3 Short Cable

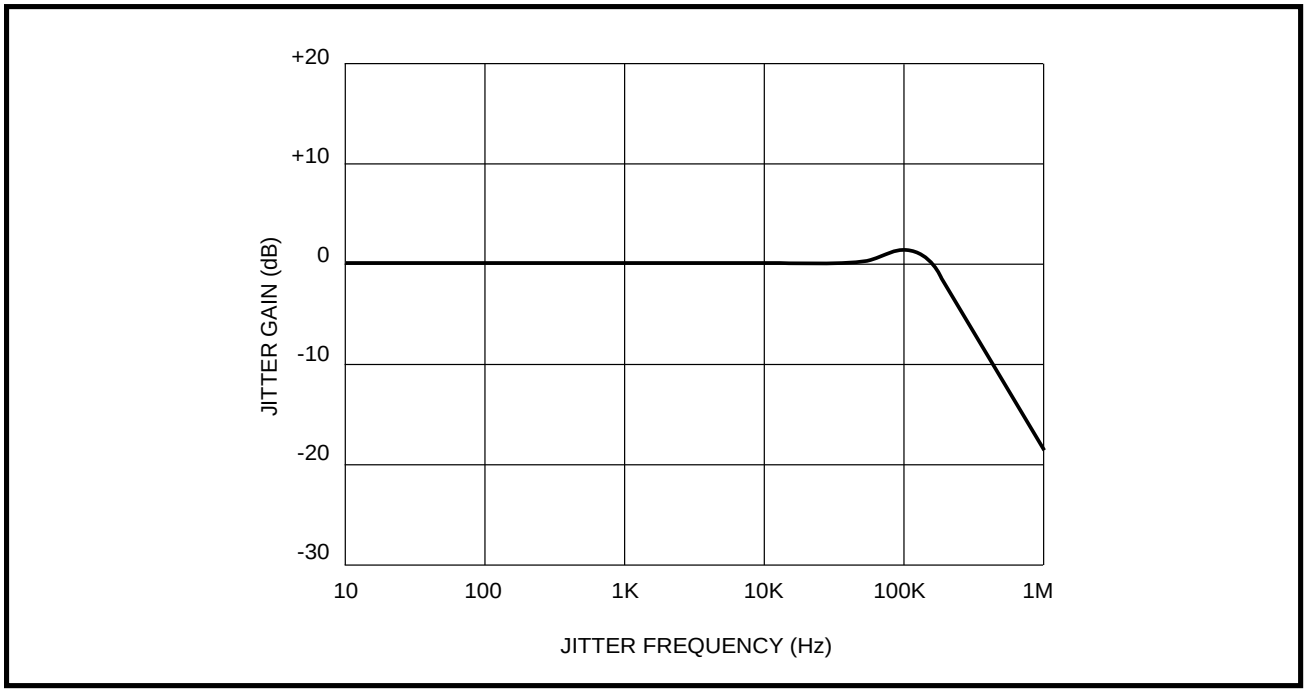

FIGURE 4: 78P7200 Jitter Transfer Function
Loop Filter BW = 165 kHz

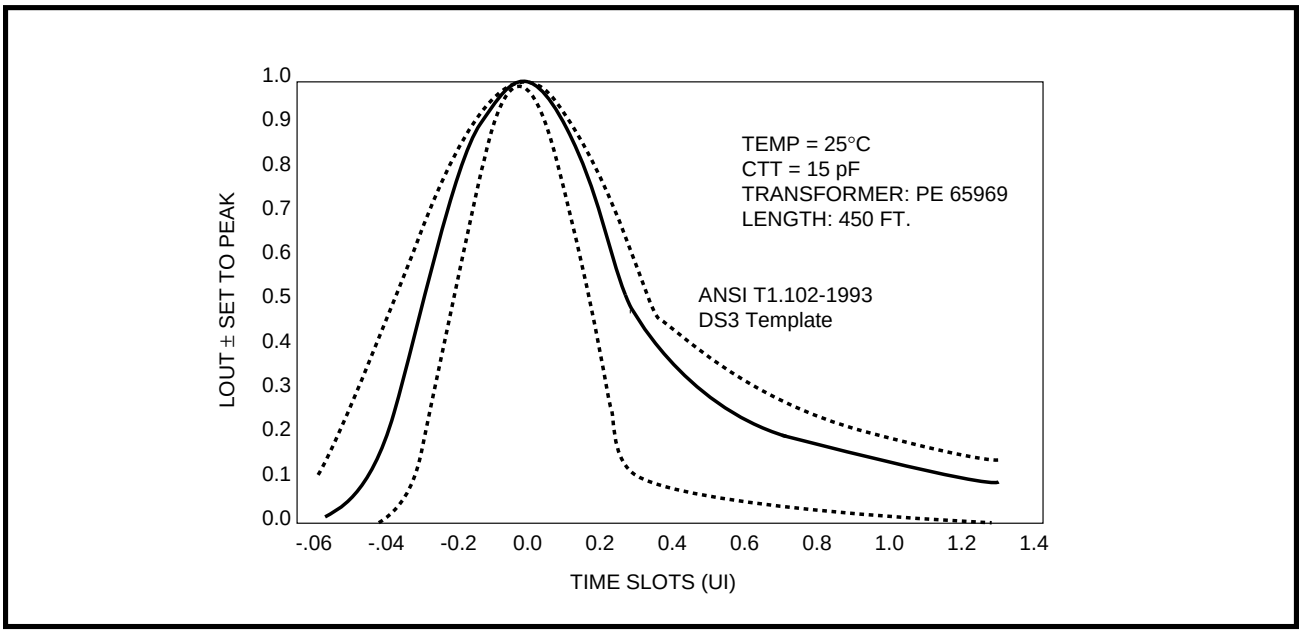

FIGURE 5: Transmitter Pulse Shape for 78P7200

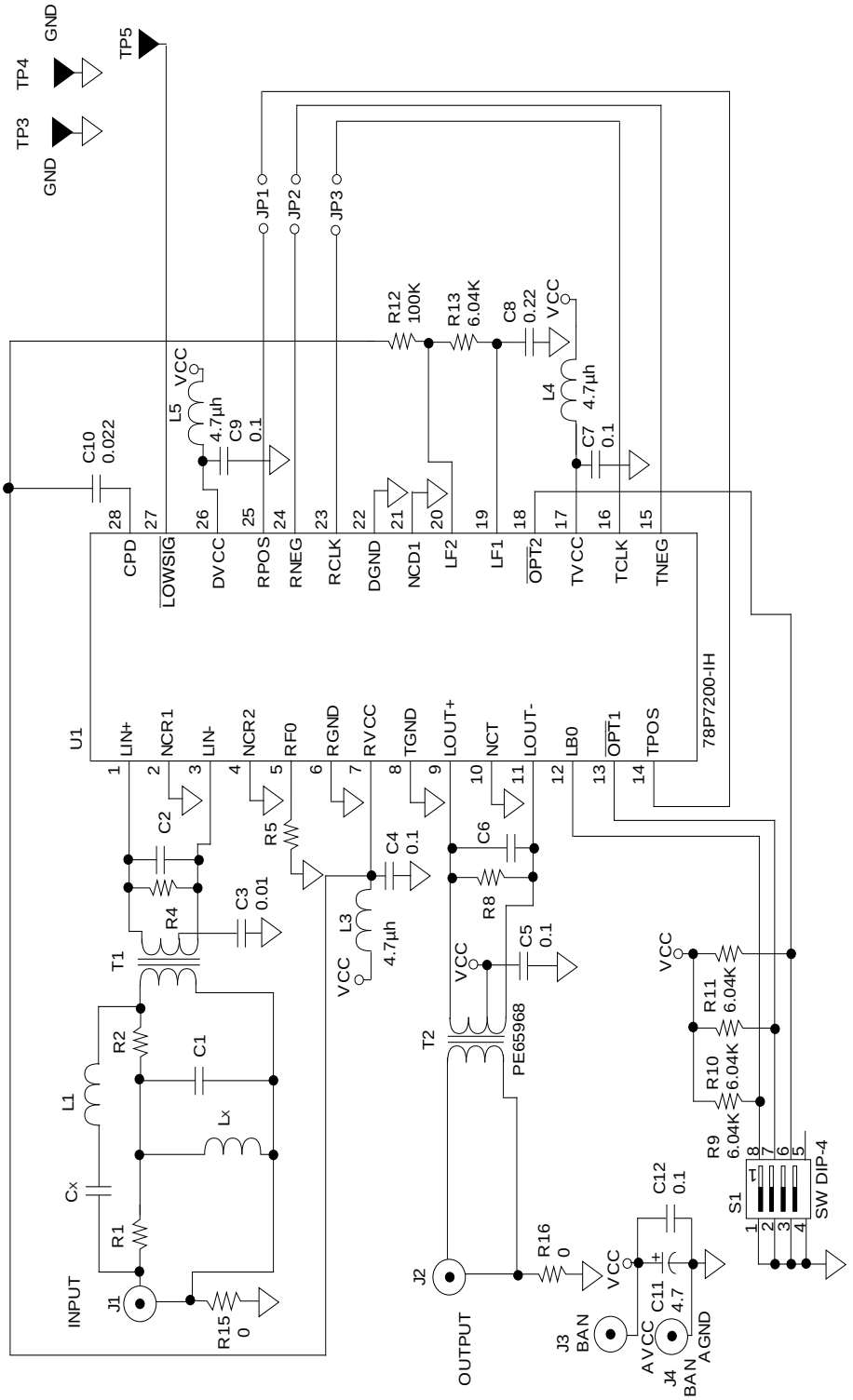

FIGURE 6: Demo Board Schematics

ORDERING INFORMATION

SSI 78P7200 DEMO BOARD	
SPEED	**PART NUMBER**
DS-3	78P7200-28H (DS3)
STS-1	78P7200-28H (STS-1)
E-3	78P7200-28H (E3)

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SSI 78Q8373

Technical Reference Guide

SSI 78Q8373

Technical Reference Guide

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Overview

Section 1

1 OVERVIEW

1.1 INTRODUCTION

The SSI 78Q8373 is a device for Ethernet LAN applications that consists of an Ethernet protocol controller, Manchester Encoder/ Decoder, 10BaseT transceiver, AUI port, and PCMCIA Bus Interface logic on one chip. It can operate using a 5-volt or 3.3-volt supply. This document contains detailed descriptions of key parts of the protocol controller block, namely, the Buffer Manager block and the Data Link Controller block, along with bit descriptions of all of the control and status registers. In addition, there is information on the power management capabilities of the SSI 78Q8373, how to configure the part for host and medium connections, information about how a host processor would handle packet transmission and reception on a network, and descriptions of the media interfaces (10BaseT and AUI) and PCMCIA Bus Interface. For detailed pin descriptions, electrical and timing parameters, please refer to the SSI 78Q8373 Data Sheet.

1.2 GENERAL DESCRIPTION

The SSI 78Q8373 combines the Ethernet network interface together with packet data management and consists of six major blocks:

- Buffer Manager (and SRAM Interface)
- Data Link Controller
- Host/PCMCIA Interface
- Manchester data Encoder/Decoder (ENDEC)
- Twisted-pair Transceiver
- Power Management

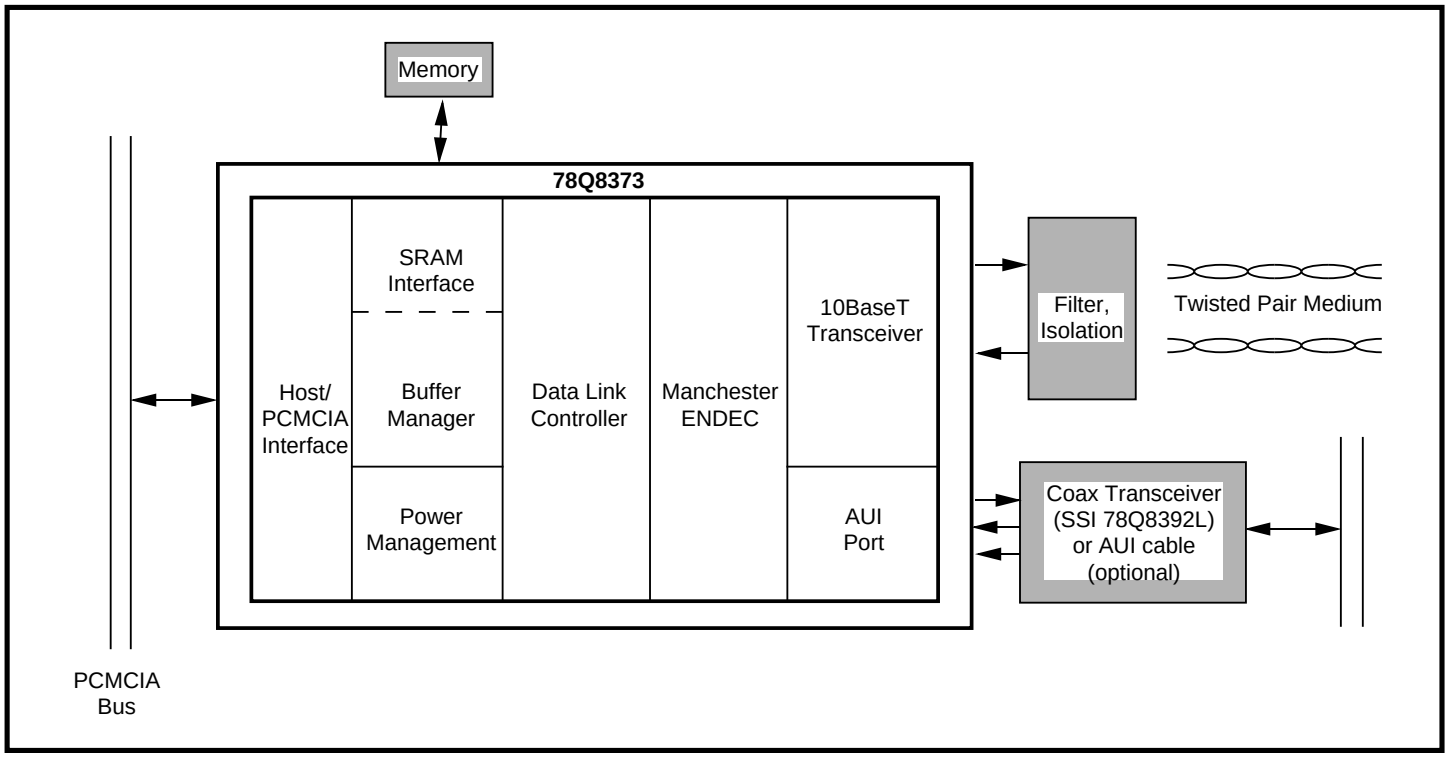

Figure 1-1: Block Diagram (78Q8373)

1.2.1 Buffer Manager

The Buffer Manager manages all accesses to the buffer memory through the SRAM interface. The buffer memory is connected directly to the Data Link Controller (DLC), thus eliminating the need for a local microprocessor. The Buffer Manager also keeps track of all buffer memory pointers automatically; simplifying the software driver task. Together with intelligent arbitration, the SSI 78Q8373 is a high performance LAN controller.

The buffer memory is divided into a transmit memory section and a receive memory section. The transmit memory section can be partitioned into 2K, 4K, 8K or 16Kbyte buffer sizes. If the transmit buffer size is greater than 2KB, then the transmit buffer is

1.2.1 Buffer Manager (continued)

configured into two banks of equal size. There is only one transmit bank if a 2KB buffer size is selected. With the two bank configuration, one transmit bank may be tied up during transmission but the host can still continue to load data packets into the second transmit bank to be tranmitted later. The receive buffer has a ring architecture which can be configured from 4K to 62KB depending on the buffer memory configuration, which can range in size from 8K to 64KB.

A central arbitrator inside the Buffer Manager prioritizes and services requests for access to the buffer memory from four sources: the Transmitter, the Receiver, Host Read and Host Write. If necessary, the SSI 78Q8373 will assert a 'not ready' handshake to the host while servicing the Transmitter and/or Receiver. The SSI 78Q8373 arbitration mechanism provides packet management by interleaving packet data accesses to the buffer memory such that the operation appears to be simultaneous.

For instance, in the situation where 2 transmit banks are configured, the host can load the first transmit bank and initiate a transmission. While the first transmit bank is being transmitted, the host can continue to load packets in the second transmit bank. At this stage, the SSI 78Q8373 can potentially be receiving data from the medium and loading it into the receive buffer (if the SSI 78Q8373 is in a loopback mode or if self-reception occurs).

1.2.2 Data Link Controller

The Data Link Controller (DLC) implements the ISO/ANSI/IEEE 8802-3 CSMA/CD protocol. It consists of a Transmitter and a Receiver, each with its own independent CRC logic. Automatic generation and stripping of the 64-bit preamble and the 32-bit CRC code are provided on-chip.

1.2.3 Host/PCMCIA Interface

The Host Interface provides connection to the host system. It consists of the various registers, DMA circuits and ready logic. Both word and byte interfaces are supported as well as big endian and little endian data ordering. Host access to the buffer memory is through BMR8 (and BMR9). Reading from BMR8 will read a byte or word from the receive buffer and writing to BMR8 will write a byte or word to the transmit buffer. The ready logic is capable of delaying host access to the buffer memory with a time-out mechanism. Both single and burst DMA transfer modes are supported.

The PCMCIA interface circuitry builds on top of the SSI 78Q8373 generic host interface and is only active if the MODE pin is left unconnected (internally pulled-up). The SSI 78Q8373 can thus connect directly to a PCMCIA release 2.1 compliant bus. It also supports decoding for the external CIS memory (both ROM and Flash types). The SSI 78Q8373 pinout has been defined to minimize criss-crossing connections to the PCMCIA connector. This allows for a cost effective 2-layer PCB design.

1.2.4 Manchester ENDEC

This block implements Manchester encoding and decoding. Serial NRZ data from the DLC is converted to Manchester encoded data and sent to either the twisted-pair transceiver block or to the Attachment Unit Interface (AUI) driver, depending on which is active. The decoder section performs three functions: clock recovery, carrier detection and Manchester decoding. The recovered receive clock will be low at the end of reception and during idle to save power. Jitter of up to ±18 nsec can be tolerated by the decoder. This block also translates a 10MHz collision signal to a logic-level signal before sending it to the DLC block if the AUI port is selected.

1.2.5 Twisted-Pair Transceiver

The on-chip Twisted-Pair module consists of the following functions. It has a smart squelch circuitry to determine valid data present on the differential receive inputs (TPIP/N). Its transmit and pre-distortion drivers connect to the twisted-pair network via the summing resistors and transformer/filter. The link detector/generator circuitry checks the integrity of the cable connection the two twisted-pair MAUs. Collision, jabber and SQE are also incorporated.

1.2.6 Power Management

One very useful and important feature that the SSI 78Q8373 offers is intelligent power management. It supports three different power saving modes: Intelligent, Standby, and Full Shutdown. All modes are configurable through registers. In the Intelligent mode, clocks are active only when they are needed. For example, when not transmitting, the clock supplied to the transmitter circuit in the DLC block is not active while host read from buffer memory may be active. In Standby mode, the oscillator clock is disconnected from the rest of the circuits, so that only the oscillator circuits draw power. Full Shutdown turns off the oscillator, resulting in maximum power savings. Note that this mode is not available when using an external clock source.

1.2.7 Pin Assignments

Following are the pin assignments for both PCMCIA and Generic bus modes of the SSI 78Q8373.

TABLE 1: Pin Assignment Table - PCMCIA Bus Mode - 100-Lead TQFP

PIN#	PIN NAME	TYPE	PIN#	PIN NAME	TYPE	PIN#	PIN NAME	TYPE	PIN#	PIN NAME	TYPE
1	D1	IO4	26	$\overline{OE}$	I	51	RA4	O4	76	DON	AO
2	D8	IO4U	27	$\overline{WE}$	I	52	RA5	O4	77	DOP	AO
3	D0	IO4	28	$\overline{INPACK}$	O4	53	RA6	O4	78	AGND	P
4	A0	I	29	$\overline{REG}$	I	54	GND	P	79	REXT	R
5	A1	I	30	$\overline{ROMG}$	O4	55	VDD	P	80	AVDD	P
6	A2	I	31	$\overline{FCE}$	O4	56	RA7	O4	81	TPIN	AI
7	A3	I	32	$\overline{XPD}$	O4	57	RA12	O4	82	TPIP	AI
8	RESET	SI	33	XRST	O4	58	RA14	O4	83	MODE	TI
9	VDD	P	34	GND	P	59	$\overline{RWE}$	O4	84	DIN	AI
10	GND	P	35	RD0	IO4U	60	RA13	O4	85	DIP	AI
11	$\overline{IOWR}$	I	36	RD1	IO4U	61	RA8	O4	86	CIN	AI
12	$\overline{IORD}$	I	37	RD2	IO4U	62	RA9	O4	87	CIP	AI
13	$\overline{CE2}$	I	38	RD3	IO4U	63	RA11	O4	88	GND	P
14	D15	IO4U	39	RD4	IO4U	64	$\overline{ROE}$	O4	89	SPKRIN	SI
15	$\overline{CE1}$	I	40	RD5	IO4U	65	RA15	O4	90	$\overline{SPKR}$	O8
16	D14	IO4U	41	RD6	IO4U	66	OSCI	CI	91	CCRA	I
17	D7	IO4	42	RD7	IO4U	67	OSCO	O	92	RRST	O4
18	GND	P	43	GND	P	68	VDD	P	93	LEDLT	OD16
19	D13	IO4U	44	$\overline{RCS0}$	O4	69	GND	P	94	CB	O4
20	D6	IO4	45	$\overline{RCS1}$	O4	70	GND	P	95	$\overline{IOIS16}$	O4
21	D12	IO4U	46	RA10	O4	71	TPDN	AO	96	$\overline{IREQ}$	O8
22	D5	IO4	47	RA0	O4	72	TPDP	AO	97	$\overline{WAIT}$	O4
23	D11	IO4U	48	RA1	O4	73	TPON	AO	98	D10	IO4U
24	D4	IO4	49	RA2	O4	74	TPOP	AO	99	D2	IO4
25	D3	IO4	50	RA3	O4	75	VDD	P	100	D9	IO4U

Legend:

I:	Input (TTL level)
O4, O8:	Output with IOL = 4 or 8 mA
OD16:	Output Open Drain with IOL = 16 mA
IO4, IO4U:	Input (TTL level) and Output with IOL = 4 mA; IO4U refers to IO4 with an internal pull-up resistor
CI:	CMOS level input
SI:	Schmitt trigger input
TI:	Three-state input. May be connected to low, high, or left open.
AI:	Analog input
AO:	Analog output
P:	Power
R:	Resistor to ground
O:	Output

TABLE 2: Pin Assignment Table - Generic Bus Mode - 100-Lead TQFP

PIN#	PIN NAME	TYPE	PIN#	PIN NAME	TYPE	PIN#	PIN NAME	TYPE	PIN#	PIN NAME	TYPE
1	HD1	IO4	26	RD8	IO4U	51	RA4	O4	76	DON	AO
2	HD8	IO4U	27	RD9	IO4U	52	RA5	O4	77	DOP	AO
3	HD0	IO4	28	RD10	IO4U	53	RA6	O4	78	AGND	P
4	HA0	I	29	RD11	IO4U	54	GND	P	79	REXT	R
5	HA1	I	30	RD12	IO4U	55	VDD	P	80	AVDD	P
6	HA2	I	31	RD13	IO4U	56	RA7	O4	81	TPIN	AI
7	HA3	I	32	RD14	IO4U	57	RA12	O4	82	TPIP	AI
8	RESET	SI	33	RD15	IO4U	58	RA14	O4	83	MODE	TI
9	VDD	P	34	GND	P	59	$\overline{\text{RWE}}$	O4	84	DIN	AI
10	GND	P	35	RD0	IO4U	60	RA13	O4	85	DIP	AI
11	$\overline{\text{WR}}$	I	36	RD1	IO4U	61	RA8	O4	86	CIN	AI
12	$\overline{\text{RD}}$	I	37	RD2	IO4U	62	RA9	O4	87	CIP	AI
13	$\overline{\text{BHE}}$	I	38	RD3	IO4U	63	RA11	O4	88	GND	P
14	HD15	IO4U	39	RD4	IO4U	64	$\overline{\text{ROE}}$	O4	89	$\overline{\text{DMACK}}$	SI
15	$\overline{\text{CS}}$	I	40	RD5	IO4U	65	RA15	O4	90	DMREQ	O8
16	HD14	IO4U	41	RD6	IO4U	66	OSCI	CI	91	EOP	I
17	HD7	IO4	42	RD7	IO4U	67	OSCO	O	92	RRST	O4
18	GND	P	43	GND	IO4U	68	VDD	P	93	LEDLT	OD16
19	HD13	IO4U	44	$\overline{\text{RCS0}}$	P	69	GND	P	94	CB	O4
20	HD6	IO4	45	$\overline{\text{RCS1}}$	O4	70	GND	P	95	HWORD	O4
21	HD12	IO4U	46	RA10	O4	71	TPDN	AO	96	$\overline{\text{INT}}$	O8
22	HD5	IO4	47	RA0	O4	72	TPDP	AO	97	READY	O4
23	HD11	IO4U	48	RA1	O4	73	TPON	AO	98	HD10	IO4U
24	HD4	IO4	49	RA2	O4	74	TPOP	AO	99	HD2	IO4
25	HD3	IO4	50	RA3	O4	75	VDD	P	100	HD9	IO4U

Legend:

I: Input (TTL level)
O4, O8: Output with IOL = 4 or 8 mA
OD16: Output Open Drain with IOL = 16 mA
IO4, IO4U: Input (TTL level) and Output with IOL = 4 mA; IO4U refers to IO4 with an internal pull-up resistor
CI: CMOS level input
SI: Schmitt trigger input
TI: Three-state input. May be connected to low, high, or left open.
AI: Analog input
AO: Analog output
P: Power
R: Resistor to ground
O: Output

Buffer Manager

Section 2

2 BUFFER MANAGER

The Buffer Manager manages accesses to the buffer memory through the SRAM interface. The buffer memory is connected directly to the Data Link Controller (DLC), thus eliminating the need for a local microprocessor. The Buffer Manager keeps track of all buffer memory pointers automatically, simplifying the software driver task. Together with intelligent arbitration for accesses to the buffer memory, this makes the SSI 78Q8373 a high performance LAN controller.

2.1 BUFFER MEMORY CONFIGURATION

There are 13 different ways in which to configure the transmit and receiver buffer SRAM for the SSI 78Q8373. This is done using 4 register bits, DLCR6<3:0>. DLCR6<1:0> sets the total buffer memory size and DLCR6<3:2> sets the transmit buffer size. If the transmit buffer is greater than 2KBytes, it is divided into two transmit banks as shown in the table below.

BS1 DLCR6⟨1⟩	BS0 DLCR6⟨0⟩	TS1 DLCR6⟨3⟩	TS0 DLCR6⟨2⟩	TOTAL BUFFER MEMORY	TRANSMIT BUFFER MEMORY		RECEIVE BUFFER MEMORY
					TX BANK #1	TX BANK #2	
0	0	0	0	8KBYTES	2KBYTES	–	6KBYTES
0	0	0	1	8KBYTES	2KBYTES	2KBYTES	4KBYTES
0	0	1	0	Illegal set-up			
0	0	1	1	Illegal set-up			
0	1	0	0	16KBYTES	2KBYTES	–	14KBYTES
0	1	0	1	16KBYTES	2KBYTES	2KBYTES	12KBYTES
0	1	1	0	16KBYTES	4KBYTES	4KBYTES	8KBYTES
0	1	1	1	Illegal set-up			
1	0	0	0	32KBYTES	2KBYTES	–	30KBYTES
1	0	0	1	32KBYTES	2KBYTES	2KBYTES	28KBYTES
1	0	1	0	32KBYTES	4KBYTES	4KBYTES	24KBYTES
1	0	1	1	32KBYTES	8KBYTES	8KBYTES	16KBYTES
1	1	0	0	64KBYTES	2KBYTES	–	62KBYTES
1	1	0	1	64KBYTES	2KBYTES	2KBYTES	60KBYTES
1	1	1	0	64KBYTES	4KBYTES	4KBYTES	56KBYTES
1	1	1	1	64KBYTES	8KBYTES	8KBYTES	48KBYTES

The remaining buffer memory that is not used by the transmit memory will be used as the receive memory. Figure 2-1 shows an example of a buffer memory configuration of 64 KBytes.

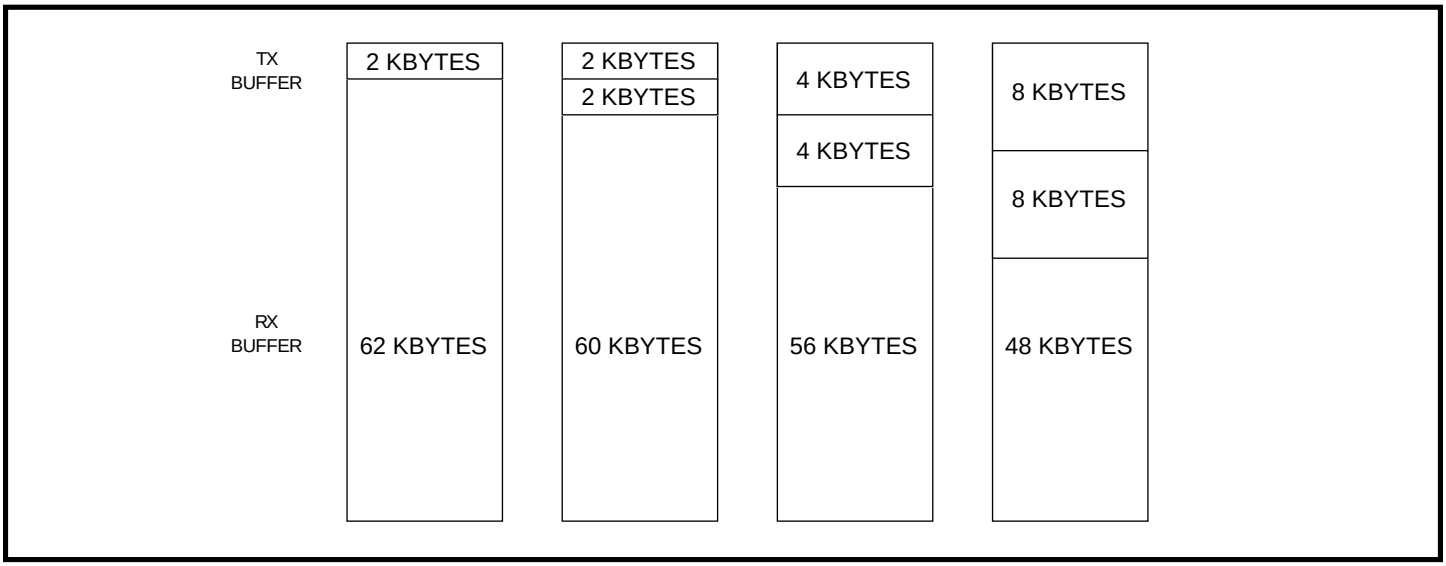

Figure 2-1: Maximum Buffer Size (64 KBytes) for Transmit and Receive Buffers

2.1 BUFFER MEMORY CONFIGURATION (continued)

The buffer memory path of the SSI 78Q8373 is 8 bits wide in PCMCIA Bus mode and can be either 8 or 16 bits wide in Generic Bus mode (The 8-bit path in PCMCIA mode is imposed due to the lack of enough pins). In the Generic Bus mode, the buffer memory data path width is selected through DLCR6<4>. If DLCR6<4> is set to a 1, then the SSI 78Q8373 data path will be byte-wide. There are eight different SRAM configurations depending on whether the data path is 8- or 16-bit (refer to Figure 2-2). The $\overline{RCS0}$ and $\overline{RCS1}$ are the SRAM chip select pins. In the 8 bit-data bus for 8KByte and 32KByte configurations, only $\overline{RCS0}$ is used and the address least significant bit starts from A0. Figure 2-2 shows the configurations possible for the SRAM.

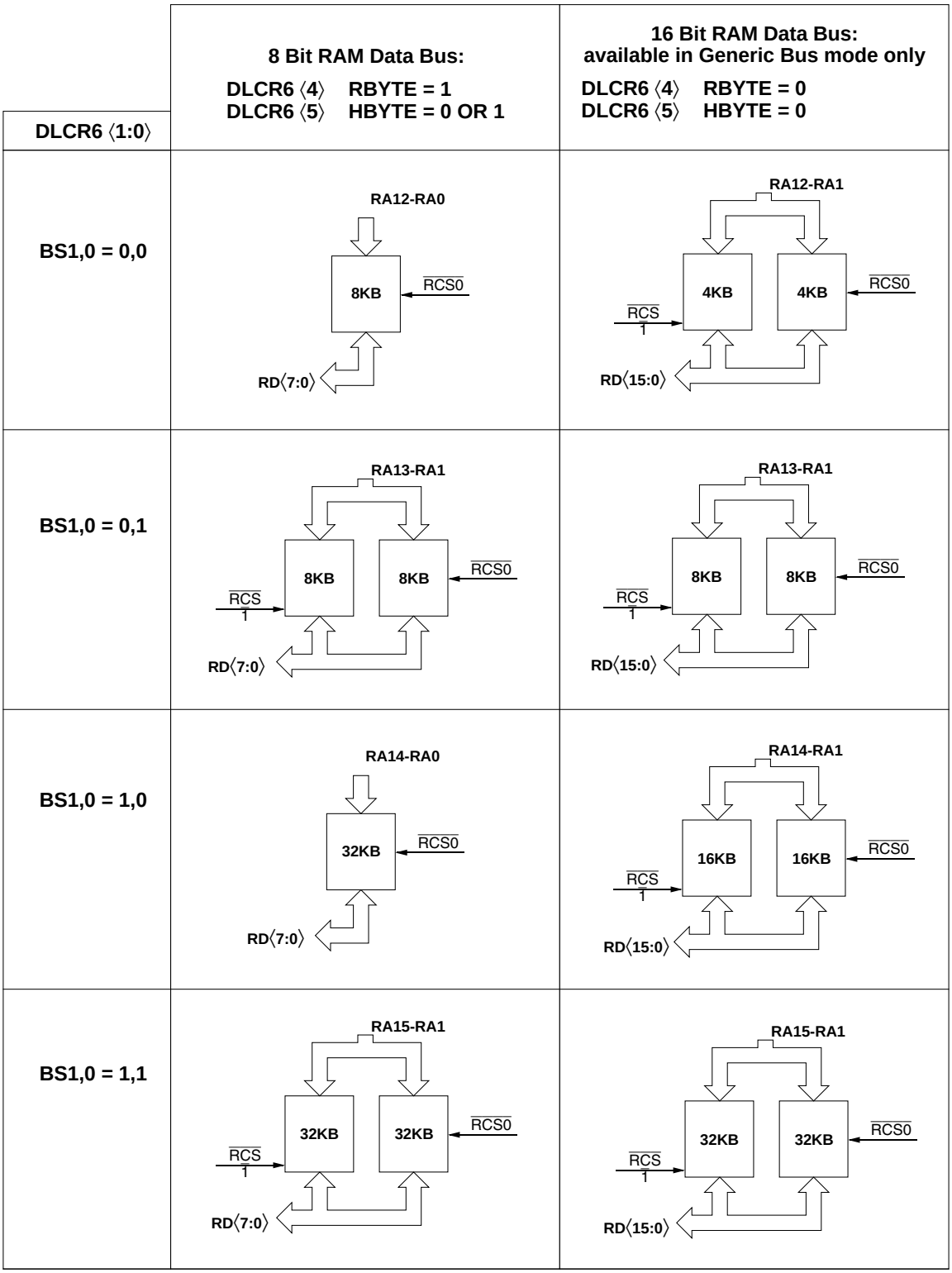

Figure 2-2: SRAM Configurations

2.2 TRANSMIT OPERATION

The SSI 78Q8373 complies with the IEEE 802.3 CSMA/CD specifications with a transfer rate of 10Mbit/s through the transmission medium. It will assemble all packets from the host and append a 64-bit preamble and a 32-bit CRC to the head and tail of each packet respectively before transmitting to the medium. As mentioned in the Buffer Memory Configuration section, one or more packets can be written by the system within a transmit memory bank until the remaining space is insufficient for another packet. The host can then issue a signal, called "Transmit start" which is stored in BMR10<7> to initiate a transmission to the medium. All packets within the same bank will thus be transmitted and followed by the status update or an interrupt if it is enabled. With the two transmit banks configuration, one bank can be transmitting and the second bank can be loading data from the system. This concurrent operation of transmitting and host writing will improve transmission throughput.

If the transmit packet encounter a collision in the medium, the SSI 78Q8373 will perform a truncated binary exponential backoff routine up to 16 attempts. After the 16th attempt, the SSI 78Q8373 will either skip the current packet or re-transmit the packet again depending on the status of BMR11<2:0>.

2.3 TRANSMIT PACKET DATA FORMAT

The packet to be transmitted is first loaded into the transmit buffer together with a 2-byte header of data length in bytes. Figure 2-3 shows an example of how 3 packets are stored within a single transmit buffer:

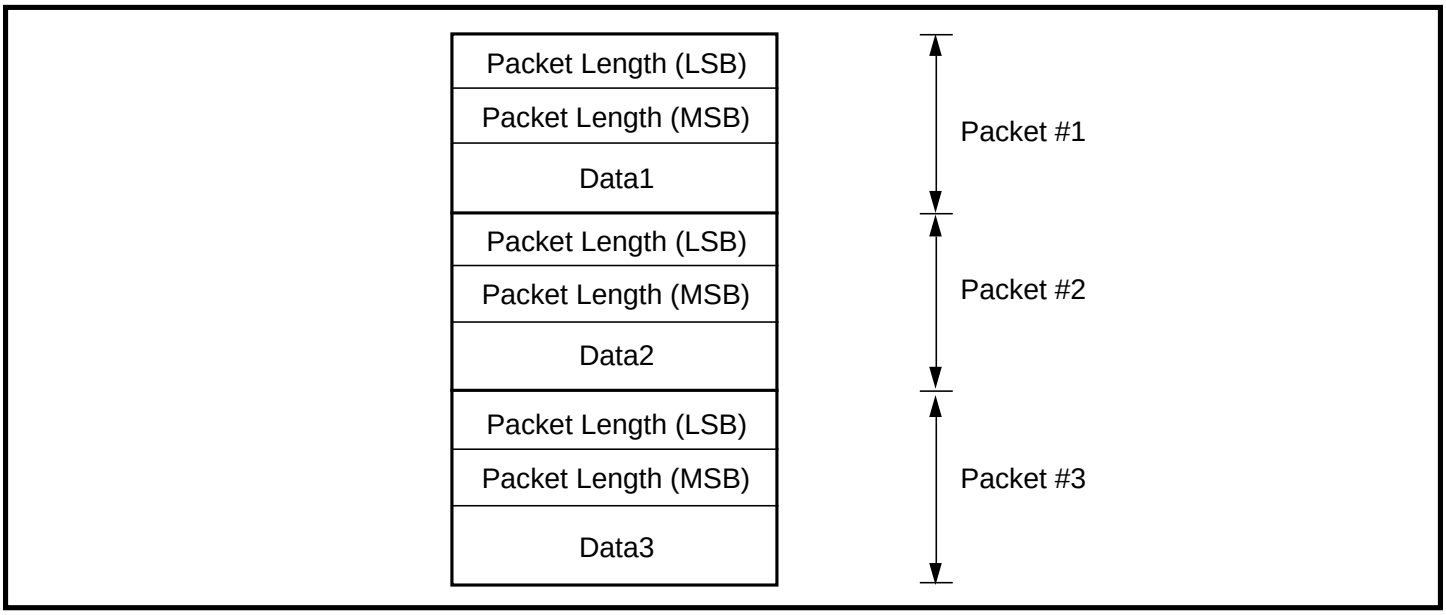

Figure 2-3: Packet Format in Transmit Buffer

After the packets are loaded, the host will write the number of packets to be transmitted into BMR10 and initiate transmission. At this stage, if a two transmit banks configuration is chosen, any new packets can now be loaded into the second bank.

2.4 RECEIVE OPERATION

The receive memory is configured as a ring structure which means the bottom of the memory is wrapped around to the top of the receive memory. There are two pointers to handle incoming packet management and they are the receive pointer and the host read pointer. The receive pointer will always point to the next empty location in the receive memory. The host read pointer is used by the host to retrieve accepted packets from the receive memory.

Initially, the values of the two pointers are equal which implies that the receive buffer is empty. As soon as data is loaded into the receive bank from the medium, the receive pointer will move away from the host read pointer. The preamble and the CRC bits are automatically removed by the data link controller (DLC) before storing the data to the receive buffer. While accepting the data, the size of the packet is checked. Under the IEEE specifications, the valid packet size is between 60 bytes to 1500 bytes (minus the preamble and CRC portions). However, if set to 1, the SSI 78Q8373 can accept packet sizes ranging from 6 bytes (by setting "accept short packet" in DLCR5<3> [ENA_SRTPKT] to a 1) to 2047 bytes. When a packet is successfully stored in the receive memory, the host can begin to read this packet. However, if there is more than one incoming packet or the packet size is too large, the receive pointer may override the host read pointer after wrapping around the ring structure. This situation is avoided with a buffer overflow flag, OVRFLO. When this flag is high, the receive pointer will not store any more data until the host read has cleared the memory.

2.4 RECEIVE OPERATION (continued)

Figure 2-4 shows the configuration of the transmit and receive buffer memory in the situation where the 2 transmit banks are selected and explains the concept of a ring architecture of the receive buffer. The received packets are stored as they are accepted by the SSI 78Q8373. The unused buffer space in the diagram shows that the host have read packets before 'Packet P-1' hence relieving that buffer space. Therefore the received packet 'Packet P+2' can be wrapped around the end of the receive buffer to the start once again.

The SSI 78Q8373 also checks the incoming packet for short packet errors, alignment errors and/or CRC errors. After one successful packet reception, the SSI 78Q8373 will perform an 8-byte re-alignment for the next packet in the receive buffer.

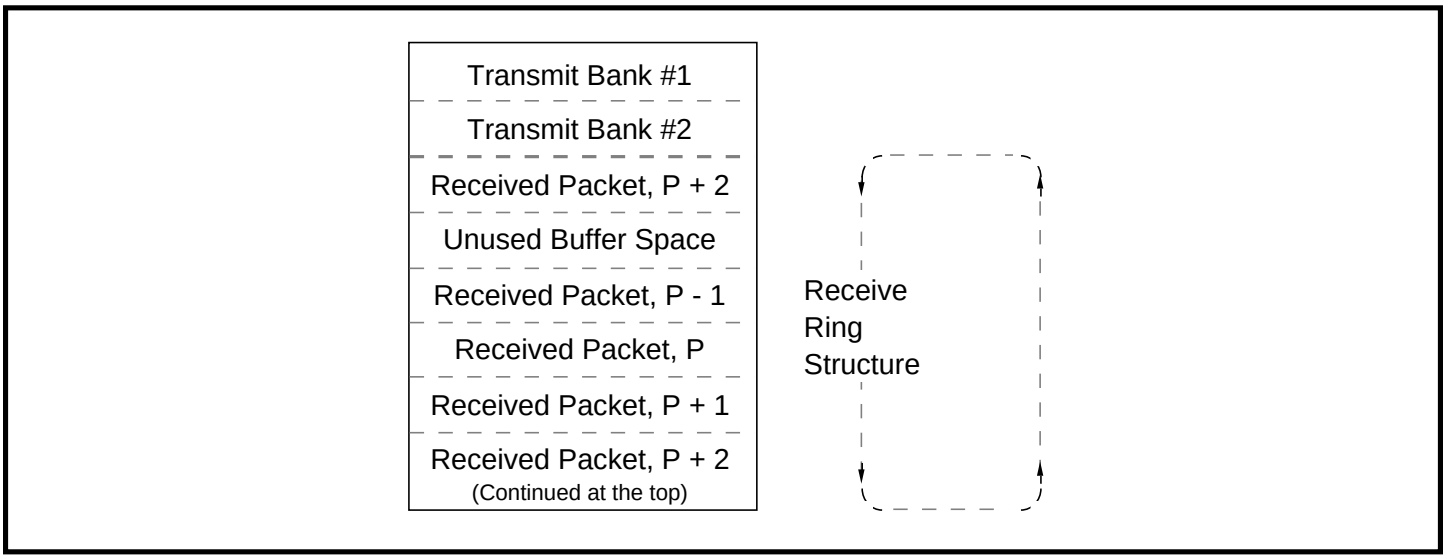

Figure 2-4: Transmit and Receive Buffer Organization

2.4.1 RECEIVER BUFFER DATA FORMAT

The receive packet has a 4-byte header which consists of the status of the receive packet, a reserved byte, and the 2 bytes of data length. Regardless of the SRAM word or byte configuration, the data length is always in terms of bytes. The data packets are linked by the internal pointers which use the data length value in the header to calculate the length of the data packet. Then the receiver will perform an 8-byte boundary alignment and the new address is generated. Under normal operation, any packets that have errors will be discarded. Figure 2-5 shows how accepted packets are stored in the receive buffer.

The SSI 78Q8373 provides a means to accept erroneous packets, mainly for testing purposes. If the DLCR5<5> bit (ACPT_BADPKT) is set to a 1, short packets or packets with alignment or CRC errors will be accepted. In these circumstances, the respective bits of the receive status registers will not be set. But the status byte to the host will still indicate that the packet has error(s).

The format of the status byte is as shown below. Note that the bit names are similar to that of the DLC register bits. However, some of these bits are not a mirror image of the corresponding register bits and this is elaborated on in the Status Byte Format section.

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	0	*PACKET OK*	*REMOTE RESET*	*SHORT ERROR*	*ALIGN ERROR*	*CRC ERROR*	*OVER FLOW*

2.5 DMA OPERATION

Data transfer via Direct Memory Access is available only in the Generic Bus mode. The DMA write or DMA read operation is similar to the I/O write or I/O read except that the handshake is done using DMREQ, $\overline{\text{DMACK}}$ and EOP signals. The DMREQ signal is used to request for DMA transfers and the $\overline{\text{DMACK}}$ signal acts like the CS to access the BMR8 and BMR9 register pair. The $\overline{\text{WR}}$ or $\overline{\text{RD}}$ signals accompany the $\overline{\text{DMACK}}$ to perform host write or host read operations respectively.

An EOP signal is asserted during the last data word or byte transfer to terminate the process (the DMA_EOP register bit [DLCR1<5>] will be set when EOP is asserted). The SSI 78Q8373 will not assert further DMREQs when EOP has been asserted by the host DMA. If the DMA interrupts are enabled, the assertion of the EOP will also cause the SSI 78Q8373 to generate an interrupt to the host.

2.5 DMA OPERATION (continued)

Single or burst DMA operations are supported for data transfer between the host and the SSI 78Q8373. In single byte or word accesses, the SSI 78Q8373 asserts the DMREQ signal and waits for the host to respond with a $\overline{\text{DMACK}}$ acknowledge and a $\overline{\text{WR}}$ or $\overline{\text{RD}}$ signal. Upon acknowledgment, the SSI 78Q8373 negates the DMREQ until the host completes the data transfer. The $\overline{\text{DMACK}}$ signal is set high when the transfer is complete. To start another DMA cycle, the SSI 78Q8373 will assert the DMREQ signal again. This continues until the host asserts the EOP signal during the last access cycle after which the SSI 78Q8373 will not make further DMREQ requests.

In burst modes, the DMA operation can be programmed for 4, 8 or 12 data transfers per DMREQ request. In these cases, the SSI 78Q8373 will negate DMREQ two cycles before the end of each burst. An EOP assertion will terminate a DMA operation anytime during the burst data transfer.

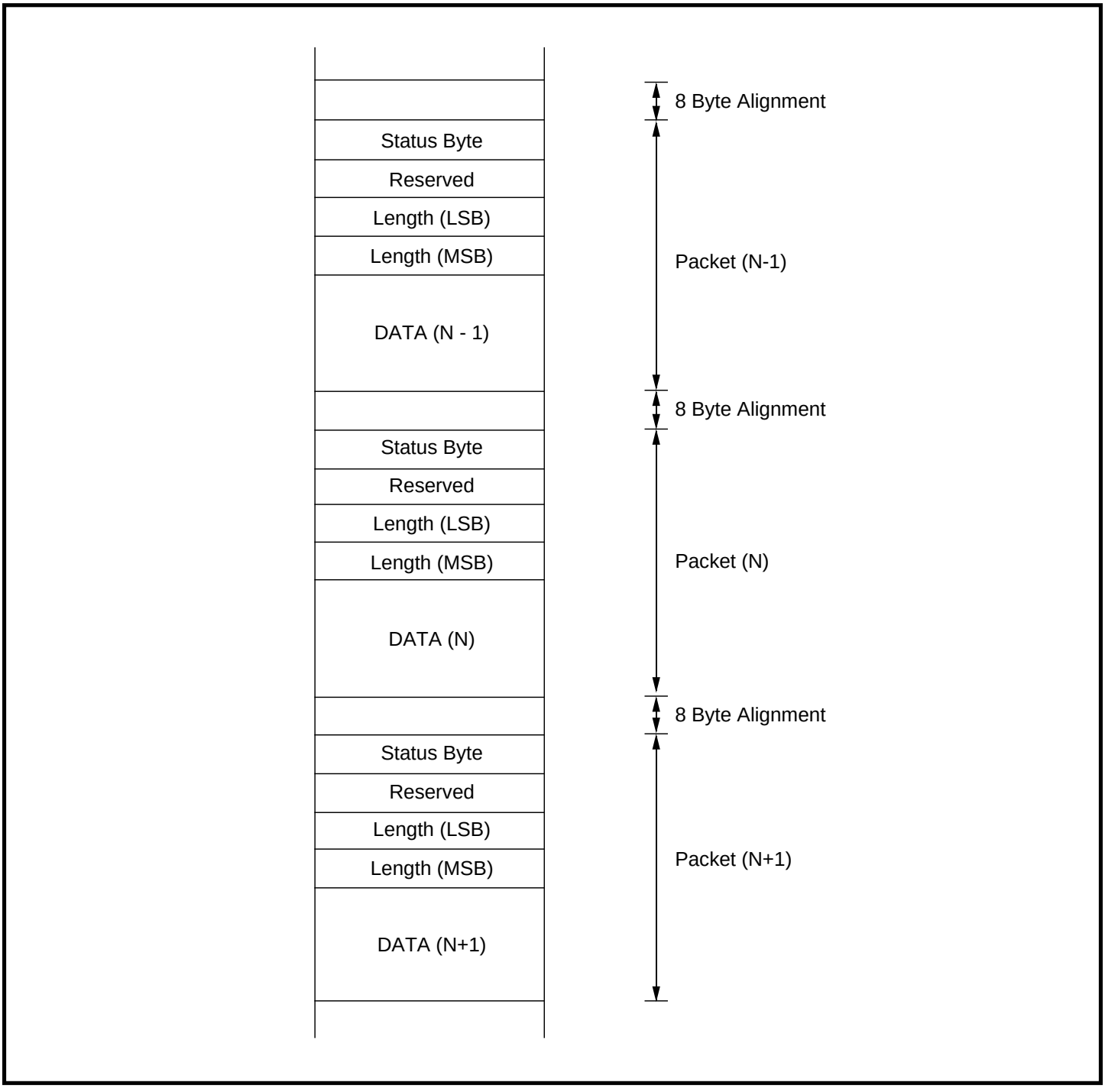

Figure 2-5: Packet Format in Receive Buffer

2.5.1 DMA WRITE (TRANSMIT)

In a DMA write mode, the host performs the same function as an I/O write to load the transmit bank with one or multiple packets of data. Typically the host has its own DMA controller which it programs to handshake with the DMA operation in the SSI 78Q8373. The host can use a combination of I/O and DMA to write a packet into the transmit buffer.

The following depicts an example of how to perform a DMA write mode using a combination of I/O and DMA operation. First, the host determines the size of the packet and writes the byte length into the SSI 78Q8373's transmit buffer using I/O access. Subsequently, the host DMA is programmed with this length information. To start a DMA transfer, the host writes a 1 to the DMA_TENA bit (BMR12<0>). The SSI 78Q8373 will assert a DMREQ request and wait for the $\overline{\text{DMACK}}$ acknowledgment to start the DMA write process. When the acknowledgment is confirmed by the host DMA, the data packets are transferred into the transmit buffer. An EOP signal is asserted when the last byte is written to the SSI 78Q8373. If the DMA_EOP interrupt (DLCR1<5>) is enabled, the SSI 78Q8373 will interrupt the host upon completion. Writing a 0 to the DMA_TENA bit disables the DMA write operation. The host can then initiate the next DMA transfer.

When the host interface is configured for word mode, the packet length value written to the SSI 78Q8373 will still be in bytes. Hence, the host has to program the host DMA with half the byte count for word transfer. If the byte count is odd, the host should round it up before halving it. This results in an extra byte written to the transmit buffer which the SSI 78Q8373 discards during the transmit process. The internal transmit buffer alignment for odd size packets are automatically handled by the SSI 78Q8373.

2.5.2 DMA READ (RECEIVE)

In a DMA read mode, the host performs the same function as an I/O read to retrieve the data from the SSI 78Q8373's receive buffer. The following depicts an example of how to perform a DMA read mode using a combination of I/O and DMA operation.

If the receive buffer is not empty, the host will read the status and packet length information in the 4-byte header of the receive packet using I/O access. This length information is then programmed into the host DMA. To initiate a DMA transfer, the host writes a 1 to the DMA_RENA bit (BMR12<1>). The SSI 78Q8373 will assert the DMREQ request and wait for the $\overline{\text{DMACK}}$ acknowledgment to start the DMA read process. Upon the $\overline{\text{DMACK}}$ acknowledgment, the packets are retrieved from the receive buffer. The EOP signal is asserted on the last byte read from the receive buffer. If DMA_EOP interrupt (DLCR1<5>) is enabled, the SSI 78Q8373 will interrupt the host. The host will write a 0 to the DMA_RENA bit to disable the DMA read operation. It can then initiate the next DMA transfer.

When the host interface is configured for word mode, the host DMA is programmed with the half the byte length as described in the DMA write section. In the case of an odd packet length, the host will read an extra byte and discard it. The SSI 78Q8373 will also manage its internal receive buffer alignment for odd size packets.

Data Link Controller

Section 3

3 DATA LINK CONTROLLER

The Data Link Controller (DLC) implements the ISO/ANSI/IEEE 8802-3 CSMA/CD protocol. It consists of a Transmitter and a Receiver, each with its own independent CRC logic. Automatic generation and stripping of the 64-bit preamble and the 32-bit CRC code are provided on-chip.

3.1 IEEE PACKET FORMAT

The DLC of the SSI 78Q8373 complies with the international standards for Ethernet, ISO/ANSI/IEEE 8802-3. The IEEE 802.3 Media Access Control (MAC) frame format is shown in Figure 3-1.

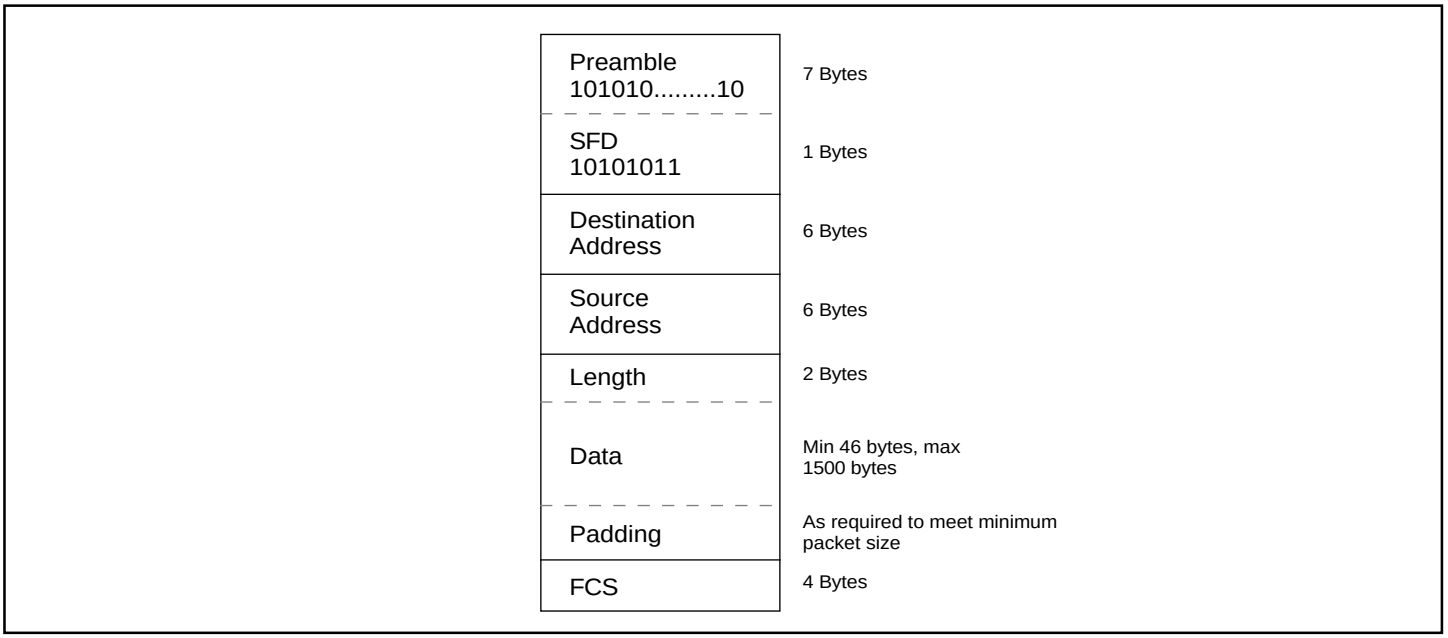

Figure 3-1: IEEE 802.3 Media Access Control (MAC) Frame Format

3.1.1 ELEMENTS OF THE MAC FRAME

The MAC frame size is defined to cover the Destination and Source Address fields, Length Field, Data Field, Padding (if necessary) and Frame Check Sequence Field (CRC Code). The minimum frame size defined in the IEEE Media Access Control Protocol is 64 bytes and the maximum frame size is 1518 bytes.

Preamble Field:

This is a 7-byte field consisting of alternating 1's and 0's to allow synchronization of phase lock loop (PLL) circuitry in the receiver.

Start Frame Delimiter (SFD) Field:

The SFD sequence is 10101011. This immediately follows the preamble and the double 1's signify the start of the frame.

Address Fields:

Each MAC frame consists of two address fields. The Destination Address Field specifies the destination address(es) for which the frame is intended and the Source Address Field specify the node that is transmitting the packet. The first bit (LSB) of the Destination Address is used to identify individual or group addressing. LSB = 0 indicates an individual address and LSB = 1 indicates a group address. The SSI 78Q8373 offers 3 types of group addressing called multicast group, multicast hash and broadcast addressing. A broadcast address consists of all 1's in the Destination Address field and is used to broadcast to all active stations on the network. Please refer to Node ID and Hash Table Configuration Registers for detailed information on the other two multicast addresses.

Length Field:

This is a 2-byte field whose value indicates the number of data bytes in the Data Field. The Length Field is transmitted with the high order byte first. However, some protocols use this field for other purposes (Ethernet calls this a **Type Field** instead). This is achieved by using values greater than the allocated values for a valid Length Field (value < 1500) to distinguish the protocol used. The SSI 78Q8373 does not perform a consistency check on the length of the data field that follows this field.

Data and PAD Fields:

The data field may contain any data from a minimum of 46 bytes to a maximum of 1500 bytes. If necessary, the data field is extended to meet the minimum frame size requirement. These extra bits are called Padding. The SSI 78Q8373 does not perform automatic padding. Upper layer software is responsible for this task.

Frame Check Sequence Field:

A cyclic redundancy check (CRC) is used by the transmit and receive algorithms to generate a CRC value for the FCS field. This is a 32-bit sequence that is computed as a function of the addresses, length, data (and pad) fields. The SSI 78Q8373 has a CRC circuitry that generates the CRC for the packet to be transmitted and checks the CRC of the received packets for transmission errors.

3.2 TRANSMITTER CIRCUITS

Circuits within the transmitter include a transmit state machine, pseudo-random number generator, preamble generator, inter-frame gap timer, exponential backoff generator and a time domain reflectometry counter. The CRC logic is shared by the transmitter and the receiver. Any transmit errors will be reported via the DLCR status registers.

The CRC logic calculates the IEEE 32-bit Frame Check Sequence (FCS) for the entire data packet (from the destination address to the end of the data field) and appends the FCS to the end of the packet. In the event of self-reception in 'accept all packets' modes or loop back, the CRC logic is used by the transmitter only.

3.2.1 Transmit Media Access Management

The SSI 78Q8373's DLC block implements the ISO/ANSI/IEEE 8802-3 Media Access Protocol called the CSMA/CD. This is the acronym for Carrier Sense Multiple Access with Collision Detect. Abiding by this protocol requires the controller to monitor the presence of a carrier from other nodes on the network and deferring any transmission if a carrier is 'sensed' on the network. A collision is defined by the situation whereby two nodes transmit at nearly the same time and try to drive the network together which results in garbled data. In the event that a collision occurs, this is detected via the collision detection mechanism. A node that is involved in a collision will transmit a 32-bit Jam Pattern to reinforce the collision such that every node on the network detects it. It will then cease its transmission and wait a pseudo-random backoff interval before attempting to transmit the packet again.

According to the ISO/ANSI/IEEE 8802-3, there must be a 9.6 msec interval between the transmission of packets for the network to recover. This is called the Inter-Frame Gap (IFG) and the SSI 78Q8373's DLC utilizes the IFG timer in the transmitter to record the interval starting from the end of the last packet on the network. The DLC will not transmit before this interval expires. If another node happens to transmit during the first 2/3 of the IFG interval, the SSI 78Q8373 will reset its IFG counter and start again at the end of this new transmission. However during the last 1/3 of the IFG interval, the SSI 78Q8373 will ignore any transmission on the network that occurs during that time in accordance with the IEEE standard. This is to assure fairness and equality in accessing the network. With two nodes transmitting at nearly the same time, a collision would occur resulting in pseudo-random backoff intervals for each node to resolve the contention.

The SSI 78Q8373's TDR counter keeps track of the number of bits that has been transmitted. The counter maintains the count of the actual number of bits transmitted just before a collision or loss of carrier occurs. The count can then be used to diagnose the medium as shown.

Estimating the distance, D (m) from the transmitting node to a fault:

N = number of bits transmitted (TDR Count)

R = transfer rate, 10 Mbit/s

S = signal propagation for coaxial cable (in the region of 2×10^8 m/sec

D = (N x S)/(2 x R) meters

A pseudo-random number generator is used for collision backoffs. The range of the random number interval increases with each collision with the maximum range occurring for the 10th collision through the 16th collision. Hence it is called the truncated binary exponential backoff. The value obtained from the pseudo-random number generator is counted down every slot-time (512 bits). When the interval expires, the SSI 78Q8373 will check the IFG timer and attempt to re-transmit.

3.2.2 Transmit Errors

There are 4 transmit error status bits in DLCR0. These cover the loss of carrier during collision, collision on the network, 16 consecutive collisions and host write error. The loss of carrier usually indicates a fault on the network (open or shorted medium). The 16 collisions error indicates that host intervention may be necessary pertaining to the next step that the SSI 78Q8373 should take. Please refer to Buffer Memory Registers Section (BMR11<2:0>). Host write error occurs when the host tries to write beyond the end of the allocated transmit buffer. Interrupts can be generated for the collision, 16 collisions and host write errors.

The collision counter DLCR4<7:4> with DLCR4<7> as the most significant bit, automatically increments every time a collision occurs. Upon the 16th collision, it will roll over to zero and set the 16COL bit (DLCR0<1>) to 1. The 16 collisions error could be an indication of a faulty medium or an overloaded network.

3.2.3 Encoder/Decoder

The SSI 78Q8373 includes an internal Manchester Encoder/Decoder (ENDEC) which converts the serial NRZ bit stream for transmission to a format used on the network. This conversion is known as Manchester Encoding which uses edges at the mid-point of a bit interval to signify a 1 or a 0. A low-to-high transition at the mid-point indicates a 1 and a high-to-low transition indicates a 0.

3.3 RECEIVER CIRCUITS

Circuits within the receiver include a receive state machine, preamble and start of frame delimiter recognition, address recognition, error detection logic, byte alignment checking, serial to parallel converter and receive FIFO. Receive errors such as short packet error, CRC error, alignment error, and buffer overflow error are reported via the DLCR status registers and the status byte header preceding each packet stored in the RAM.

The receive FIFO provides buffering while the Buffer Manager is servicing another resource and enables the loading of data into the SRAM only when necessary, i.e., on the acceptance of a packet. The preamble and start of frame delimiter is stripped from the packet before loading it into the receive buffer. The last four bytes of the packet (CRC) remain in the receive FIFO and are not transferred to the receive buffer.

The CRC logic calculates the IEEE 32-bit Frame Check Sequence (FCS) for the entire data packet (from the destination address to the end of the packet including the transmitted CRC) and the resultant should be a fixed constant if no errors occurred during the transmission.

3.3.1 Receive Media Access Management

As a bit stream is present on the network, the PLL in the internal ENDEC of the SSI 78Q8373 will lock-on to the stream of alternating 1's and 0's (the preamble pattern). The ENDEC performs the decoding function of the Manchester encoded data on the network for the receiver. The receiver monitors the decoded bit stream (NRZ format) for the end of the preamble pattern i.e. the start of frame delimiter byte pattern which is '10101011'. The two consecutive 1's in this pattern signifies the start of the first bit of the first byte of the destination address field.

The SSI 78Q8373 allows the acceptance of packets with physical or logical addressing. Physical addressing requires the exact matching of the entire 6 bytes of destination address and the Node ID. Logical addressing comes in three forms for the SSI 78Q8373: broadcast, multicast group and multicast hash addressing. The first bit of the 48-bit destination address is a 0 if the address is a physical address . If the address is a logical address then the first bit of destination address is a 1. Broadcast messages are messages that are meant for all nodes on the network and the destination address of a broadcast packet consists of all 1's. A multicast group address has the first bit of the destination address as a 1 and the receiver will only match the first 3 bytes of the incoming address before deciding to accept or reject the packet. For multicast hash addressing, the CRC logic performs the calculation for the 48-bit address and the least significant 6 bits are used to hash into the SSI 78Q8373's 64 element hash table. If the hashed element has been set to a 1 then the packet will be accepted. If the hashed element has been set to a 0, the packet will be rejected.

During initialization, appropriate bits are set in the Address Mode registers (DLCR5<1:0>) and command bits in DLCR5 for 'bad packet' (packets with errors) acceptance and so forth. As a packet is received from the network, its destination address will be matched following the criteria of the Address Mode and DLCR5 registers. Once the destination address matches according to that criteria, the packet is accepted and is loaded into the receive buffer. The last 4 bytes of the received packet (32-bit CRC) are not transferred to the receive buffer. If the destination address fails to meet the criteria, the packet is rejected and the receiver continues to monitor the network.

3.3.2 Receive Errors

There are 5 receive status errors in DLCR1. These include the host read error, short packet error, alignment error, CRC error and buffer overflow error. Host read error results when the host attempts to read from an empty receive buffer. RX_BUFMTY bit in DLCR5<6> is set to 1 by the SSI 78Q8373 when the receive buffer is empty. Short packet error occurs when a packet is less than the IEEE minimum of 60 bytes in length is received. This packet will not be accepted unless the ENA_SRTPKT bit (DLCR5<3>)

has been activated. Packets with alignment or CRC or short packet errors are accepted only if the ACPT_BADPKT bit (DCLR5<5>) is set to a 1. Alignment error indicates an incomplete byte frame at the end of a packet and CRC error indicates an error has occurred during transmission. A CRC error occurs when the received packet is checked by the CRC logic (from destination address to the end of the packet including the appended CRC) and the resultant is not the fixed constant expected in a no-error transmission. Short packet error is set if the received packet is less than the minimum length of 60 bytes. Buffer overflow error signals insufficient space in the receive buffer for the current packet and requires the host to read packets from the receive buffer to relieve more buffer space.

3.3.3 Encoder/Decoder

The internal ENDEC performs the recovery of the receive clock RXC, carrier detection and Manchester decoding of the data stream from the network. The received data stream is transferred to the ENDEC circuit block via either the on-board twisted-pair transceiver circuit or the AUI circuit, depending on which is active. When the ENDEC block receives a signal from the twisted-pair transceiver or the AUI circuit, it converts this carrier detection into the CRS signal for the controller. The recovered clock, RXC is achieved through the digital phase lock loop (DPLL) in the ENDEC which tries to synchronize to the incoming 5 MHz stream. (The preamble consists of alternating 1's and 0's when converted to Manchester encoding produces this waveform). The data stream is then decoded to NRZ format with the recovered RXC. This is passed to the controller as the received data, RXD. During idle periods, the RXC is not active.

3.4 LOOP BACK MODES

The SSI 78Q8373 provides for 2 types of loop back testing. They are defined as follows:

i) ENDEC Loop Back

ii) Media Loop Back (Twisted-pair transceiver or AUI Port)

Loop back i is used for testing functionality of the Manchester Encoder/Decoder (ENDEC). This can be invoked by setting the appropriate bit in the DLCR4<1>, but is intended for diagnostic testing only, and should not be set during normal operation. The Media Loop Backs are basically a normal transmission with a self-addressed packet or setting the Address Modes to an "accept all packets" mode (i.e. promiscuous mode occurs when AM<1,0> = 11). All of these loopbacks are illustrated in Figure 3-2.

For the ENDEC loop back, data is routed from the transmit buffer to the transmitter of the DLC, through the Manchester Encoder which loops the decoded data back to the Manchester decoder. The decoder decodes the Manchester code and passes the NRZ data to the receiver of the DLC which then stores it in the receive buffer. The $\overline{\text{EDLOOP}}$ bit (DLCR4<1>) is set to 0 for this loop back mode. This permits testing of the DLC's transmit and receive sections and the Manchester encoding and decoding sections. The host software can then read and verify the received data.

For the Media loop backs, data is routed from the transmit buffer to the transmitter of the DLC through the ENDEC and the medium (via either the internal twisted-pair transceiver or the AUI port, depending on which interface is selected) then back to the receiver of the DLC. This occurs when the SSI 78Q8373 is in the 'accept all packets' mode (promiscuous) where all packets that the transmitting node sends are accepted. Another way of achieving this effect is to send a packet with the destination address equal to the source address. This permits testing of the entire loop starting from the DLC to the medium and back. The host software can then read and verify the received data.

3.4.1 Self-Reception Criteria

In a normal operating mode, self-reception is only possible when the destination address of the transmitted packet matches the transmitting station's Node ID (physical address match). In this case, the transmitting station will not receive its own multicast (group or hash) or broadcast messages.

If the ENDEC Loopback mode is activated, the address recognition logic in the receiver will treat the loop back message as if it was coming from the medium. Thus if a match occurs (physical, multicast or broadcast), self-reception will take place.

In the 'accept all packets' mode, self-reception is guaranteed to happen for any transmission.

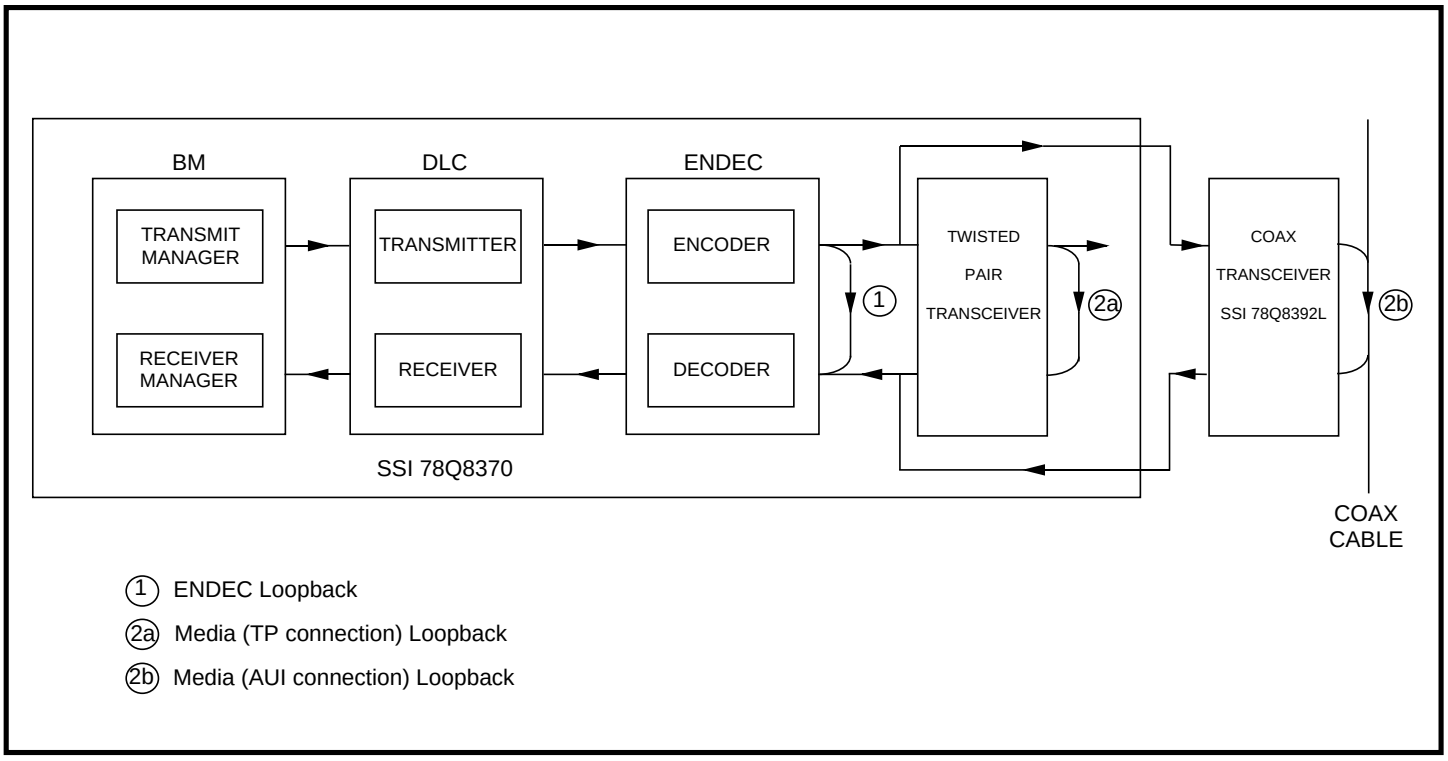

Figure 3-2: 78Q8373 Loop Back Modes

Power Management

Section 4

4 POWER MANAGEMENT

SSI 78Q8373 provides 3 modes of intelligent power management:

1) Auto power down mode through BMR11<6>.

This mode is the default at reset/power up. The clocks are active only when they are needed. This auto power down mode can be disabled by programming a 1 which can be useful for chip debugging and maximum power consumption estimation.

2) Standby mode through DLCR7<5> or through CCR1<2>.

Set DLCR7<5> = 0 to enter this mode, or, if the SSI 78Q8373 is in PCMCIA mode, set CCR1<2> = 1. This de-gates the oscillator clock without shutting it off. All the internal clocks are not active with the oscillator still running. Using full static design, the SSI 78Q8373 remembers all of the register settings, memory pointer values and the status of the state machines prior to entering standby mode. It can resume normal operation again when this bit is disabled.

3) Oscillator shut off through BMR11<7>.

WARNING: This bit may only be set if using the internal oscillator. Setting this bit while using an external canned oscillator can damage the chip.

Due to the above danger, this bit can only be set (hardware protected) after the standby mode has been entered. Thus, accidental write can be prevented. The users need to be aware that the oscillator needs some time to stabilize. This startup time is typically 2 msec for SSI 78Q8373.

The following programming sequence is recommended for entering this mode:

i) Check that SSI 78Q8373 is idle (i.e. not in the middle of an operation).

ii) Set DLCR7<5> to ‘0’ to enter standby mode.

iii) Set BMR11<7> to ‘1’ to shut off the internal oscillator.

(SSI 78Q8373 is now in its lowest power consumption configuration).

The ‘wake up’ sequence is as follows:

i) Set BMR11<7> to ‘0’ to turn on the internal oscillator.

ii) Allow some time for the internal oscillator to stabilize. This is typically 2 msec.

iii) Set DLCR7<5> to ‘1’ to go back to the normal mode.

Control & Status Registers

Section 5

5 CONTROL AND STATUS REGISTERS

The registers in the SSI 78Q8373 can be divided into six groups: 1) Data Link Control Registers (DLCR0-7); 2) Node ID registers (IDR8-13); 3) Time Domain Reflectometry Registers (TDR14-15); 4) Hash Table Registers (HTR8-15); 5) Buffer Memory Registers (BMR8-15); 6) PCMCIA Registers (CCR0-1).

The Data Link Control Registers contain the transmit and receive status information, interrupt enable, SSI 78Q8373 setup and software reset bit (DLCR6<7>). They are accessed through direct register addresses xxx0H through xxx7H. The Ethernet Node ID is stored in IDR(8-15). The TDR(14-15) registers are used to provide the count value of the number of bits transmitted for each packet. This value can indicate whether a packet has completed its transmission or has encountered a collision. Both the Node ID and the Time Domain Reflectometry Registers can be accessed through direct register addresses xxx8H through xxxFH.

The Hash Table Registers (HTR8-15) provides a means for filtering incoming multicast packets. Any packet that does not match the hash table coding will be rejected. The HTR8-15 can be accessed by the bank-switching addresses RBNK1,0 (DLCR7<3:2>).

The tasks performed by the Buffer Memory Registers (BMR8-15) include transferring of packets between the host and SSI 78Q8373 (via BMR8-9), collision control, DMA operations and activation of the transmit operation including control of the internal 10BaseT transceiver.

The final group of the registers belongs to the PCMCIA Registers (CCR0-1), which are used for controls specific to operation in a PCMCIA card environment.

A summary table of the registers and their addresses are tabulated below:

CCRA	RBNK1, 0	HA3	HA2	HA1	HA0	ADDRESS	DESCRIPTION
X	XX	0	0	0	0	DLCR0	Transmit Status
X	XX	0	0	0	1	DLCR1	Receive Status
X	XX	0	0	1	0	DLCR2	Transmit Interrupt Mask
X	XX	0	0	1	1	DLCR3	Receive Interrupt Mask
X	XX	0	1	0	0	DLCR4	Transmit Mode
X	XX	0	1	0	1	DLCR5	Receive Mode
X	XX	0	1	1	0	DLCR6	Configuration 0
X	XX	0	1	1	1	DLCR7	Configuration 1
X	00	1	0	0	0	IDR8	NODE ID 0
X	00	1	0	0	1	IDR9	NODE ID 1
X	00	1	0	1	0	IDR10	NODE ID 2
X	00	1	0	1	1	IDR11	NODE ID 3
X	00	1	1	0	0	IDR12	NODE ID 4
X	00	1	1	0	1	IDR13	NODE ID 5
X	00	1	1	1	0	TDR14	TDR 0 (LSB)
X	00	1	1	1	1	TDR15	TDR 1 (MSB), select 3V
X	01	1	0	0	0	HTR8	Hash Table 0
X	01	1	0	0	1	HTR9	Hash Table 1
X	01	1	0	1	0	HTR10	Hash Table 2
X	01	1	0	1	1	HTR11	Hash Table 3
X	01	1	1	0	0	HTR12	Hash Table 4
X	01	1	1	0	1	HTR13	Hash Table 5
X	01	1	1	1	0	HTR14	Hash Table 6
X	01	1	1	1	1	HTR15	Hash Table 7
X	10	1	0	0	0	BMR8	Buffer Memory I/O Port
X	10	1	0	0	1	BMR9	Buffer Memory I/O Port (word mode)
X	10	1	0	1	0	BMR10	Transmit Start + Packet Count
X	10	1	0	1	1	BMR11	16 Collisions Control
X	10	1	1	0	0	BMR12	DMA Enable
X	10	1	1	0	1	BMR13	DMA Burst & Transceiver Mode
X	10	1	1	1	0	BMR14	Receiver Filter & Interrupt Enable
X	10	1	1	1	1	BMR15	Transceiver Status
X	11	X	X	X	X	–	RESERVED
1	XX	0	0	0	0	CCR0	PCMCIA Configuration Option
1	XX	0	0	0	1	CCR1	PCMCIA Card Config. & Status

Note: All registers are both word and byte accessible. In word mode, register bytes are paired up. In the case of odd-byte packet, the odd-address byte becomes the high byte of the word. In byte mode, only BMR8 will be used. IDR and HTR can only be accessed when $\overline{\text{ENADLC}}$ (DLCR6<7>) is a '1.' The CCR0 and CCR1 registers are visible only if the chip is configured in PCMCIA mode.

5 CONTROL AND STATUS REGISTERS (continued)

A register bit-map is also included for the Data Link Controller Registers, Buffer Manager Registers, and PCMCIA registers. Also shown are the default values for each register. Shaded bits are non-writeable.

Register Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit3	Bit 2	Bit 1	Bit0
Transmit Status **DLCR0**	TXOK 0	NET_BSY 0	SELF_RX 0	TX_ERR 0	JABBER 0	COL 0	16COL 0	HWR_ERR 0
Receive Status **DLCR1**	PKT_RDY 0	HRD_ERR 0	DMA_EOP 0	RMTRST 0	SRT_ERR 0	ALG_ERR 0	CRC_ERR 0	OVRFLO 0
Tx Interrupt Enable **DLCR2**	TXOK INT ENABLE 0	RESERVED BIT 0	SELF_RX INT ENABLE 0	RESERVED BIT 0	JABBER INT ENABLE 0	COL INT ENABLE 0	16COL INT ENABLE 0	HWR_ERR INT ENABLE 0
Rx Interrupt Enable **DLCR3**	PKT_RDY INT ENABLE 0	HRD_ERR INT ENABLE 0	DMA_EOP INT ENABLE 0	RMTRST INT ENABLE 0	SRT_ERR INT ENABLE 0	ALG_ERR INT ENABLE 0	CRC_ERR INT ENABLE 0	OVRFLO INT ENABLE 0
Transmit Mode **DLCR4**	COL 3 0	COL 2 0	COL 1 0	COL 0 0	NO_BACK 0	NOT_CB 1	$\overline{\text{EDLOOP}}$ 1	DSC 0
Receive Mode **DLCR 5**	RESERVED BIT 0	RX_ BUFMTY 1	ACPT_ BADPKT 0	ADD_SIZE 0	ENA_ SRTPKT 0	ENA_ RMTRST 0	AM1 0	AM0 0
Config. 0 **DLCR6**	$\overline{\text{ENADLC}}$ 1	RAMSP 0	HBYTE 1	RBYTE 1	TS1 0	TS0 1	BS1 1	BS0 0
Config. 1 **DLCR7**	CTM 1 0	CTM 0 0	NOT_ STDBY 1	RDYSEL 0	RBNK1 0	RBNK0 0	EOPSEL 0	INTLMOT 0
Tx Packet Counter **BMR10**	TXST 0	PACKET CNT 6 0	PACKET CNT 5 0	PACKET CNT 4 0	PACKET CNT 3 0	PACKET CNT 2 0	PACKET CNT 1 0	PACKET CNT 0 0
16 Collision Control **BMR11**	OSC_OFF 0	$\overline{\text{AUTOPD}}$ 0	RESERVED BIT 0	RESERVED BIT 0	RESERVED BIT 0	$\overline{\text{HALT}}$ 0	RESTART 0	SKIP 0
DMA Enable **BMR12**	RESERVED BIT 0	RESERVED BIT 0	RESERVED BIT 0	RESERVED BIT 0	RESERVED BIT 0	RESERVED BIT 0	DMA_RENA 0	DMA_TENA 0
DMA Burst Control **BMR13**	$\overline{\text{APOL}}$ 0	RTH 0	$\overline{\text{ENLI}}$ 0	PORT_SEL 0	$\overline{\text{ASEL}}$ 0	DMT 0	DMAB1 0	DMAB0 0
Rx Pointer Control **BMR14**	RESERVED BIT 0	LD INT ENABLE 0	RESERVED BIT 0	RESERVED BIT 0	RESERVED BIT 0	SKP_RX 0	SQE INT ENABLE 0	RXF 1
Tranceiver Status **BMR15**	RESERVED BIT 0	LD 0	OWCOL 0	RESERVED BIT 0	RPI 0	RESERVED BIT 0	SQE 0	RESERVED BIT 0
Config. Option **CCR0**	SRESET 0	LEVIREQ 0	CI 5 0	CI 4 0	CI 3 0	CI 2 0	CI 1 0	CI 0 0
Card Config. & Status **CCR1**	RESERVED BIT 0	RESERVED BIT 0	IOIS8 0	RESERVED BIT 0	AUDIO 0	PWRDWN 0	INTR 0	RESERVED BIT 0

5.1 LEGEND DESCRIPTION

The legend (column L in the register tables) used to describe register initial values, readability and writeability are denoted by the following abbreviations:

R: READABLE
W: WRITABLE
C: CLEARABLE: Writing a '1' clears this bit; writing a '0' has no effect
H: CONDITIONALLY WRITABLE: The default values can only be changed depending on other conditions
0/1: Power-up/Reset Default value

5.2 DATA LINK CONTROLLER REGISTERS

There are 8 Data Link Controller registers that will provide the status and control signals between the SSI 78Q8373 and host. In the following sections, each register bit will be explained.

5.2.1 DLCR0 - Transmit Status Register

This register provides the transmit status to the host. These status bits can also produce interrupts if DLCR2 interrupt enable signals are set (see DLCR2 for details). The status bits can be cleared by writing a '1' to the respective bit but writing a '0' has no effect on it. Note that more than one status bit can produce a common interrupt signal. Hence it is advisable for the host to check this register to find out how many of the status bits could have caused the generation of the interrupt signal.

BIT	SYMBOL	L	DESCRIPTION
7	TXOK	R,C,0	TRANSMIT OK: When the packet is transmitted through the medium without any errors or skipped due to excessive collisions, this bit is set high. If DLCR2<7> is enabled, then the bit can trigger an interrupt to the host.
6	NET_BSY	R,0	NET BUSY: If this bit is read as 1, it indicates that the network is busy at the receiver. This bit reflects the status of the CRS signal.
5	SELF_RX	R,C,0	SELF RECEPTION: The bit is used to indicate that self-reception has occurred. Writing a 1 or power reset will clear this bit. If DLCR2<5> is enabled, it can trigger an interrupt to the host.
4	TX_ERR	R,0	TRANSMIT ERROR: When read as a 1, this bit indicates a possible collision on the network or a loss of carrier during transmission. Automatically cleared on the next transmission. Writing a '1' or a '0' has no effect.
3	JABBER	R,0	JABBER: When high, it indicates that excessive transmit length is detected by the internal jabber timer. This is a serious error condition which only occurs when the chip malfunctions. Can generate interrupts if enabled by the corresponding interrupt enable bit in DLCR2. This jabber error can only be cleared by hardware or software reset through DLCR6<7>.
2	COL	R,C,0	COLLISION: This bit is set high when a collision occurs on the data packet during transmission. The 78Q8373 performs up to 16 re-transmissions. If DLCR2<2> is enabled, it can trigger an interrupt to the host. The number of collisions is stored in DLCR4<7:4>.
1	16COL	R,C,0	16 COLLISIONS: If a data packet has suffered 16 unsuccessful transmission then this bit will set high. Generates an interrupt to the host if DLCR2<1> is enabled.
0	HWR_ERR	R,C,0	HOST WRITE ERROR: When the host attempts to write data to the transmit buffer memory and did not get the response from 78Q8373 after 2.4 msec, this flag is set. This is to indicate that the transmit buffer is full. If DLCR2<0> is enabled, it can trigger an interrupt to the host.

5.2.2 DLCR1 - Receive Status Register

This register provides the receive status to the host. These status bits can also produce interrupts if DLCR3 interrupt enable signals are set (see DLCR3 for details). The status bits can be cleared by writing a '1' to the respective bit. Writing a '0' has no effect on the register bit. Note that more than one status bits can produce a common interrupt signal. Therefore it is best for the host to check this register to find out how many of the status bits could have caused the generation of the interrupt signal.

In this register, DLCR1<3:0> are status bits for the current received packet. If any of these bits are set then the packet will be discarded. However, 'bad packets' can be accepted by the SSI 78Q8373 under the following settings:

(1). DLCR5<5>, ACPT_BADPKT set to high allows the acceptance of short packets and packets with alignment or CRC errors

(2). DLCR5<3>, ENA_SRTPKT set to high allows the acceptance of packets with length between 6 bytes and 2047 bytes.

BIT	SYMBOL	L	DESCRIPTION
7	PKT_RDY	R,C,0	PACKET READY: When a data packet is successfully loaded into the buffer memory, this bit is set. Can generate an interrupt if DLCR3<7> is enabled.
6	HRD_ERR	R,C,0	HOST READ ERROR: If the receive buffer is empty and the host has waited for the response from 78Q8373 for more than 2.4 msec during host read then this bit is set. Can generate an interrupt if DLCR3<6> is set.
5	DMA_EOP	R,0	DMA END OF PROCESS: When a DMA process is over, the host will assert a high to the EOP pin to indicate the end of process. Can generate an interrupt if DLCR3<5> is set. To clear this bit, a value of 00H must be written into BMR12. Writing either a '1' or '0' has no effect.
4	RMTRST	R,C,0	REMOTE RESET PACKET RECEIVED: This bit is set if a packet received contains the pattern 0900H in its Type Field and ENA_RMTRST (DLCR5<2>) is set to a 1. Can generate an interrupt if enabled by DLCR3<4>. The value on this bit is mirrored onto the pin RRST (pin 96).
3	SRT_ERR	R,C,0	SHORT PACKET ERROR: This bit is set when the received packet is less than 60 bytes (excluding preamble and CRC). 60 bytes is the IEEE minimum frame size. Can generate an interrupt if enabled by DLCR3<3>.
2	ALG_ERR	R,C,0	ALIGNMENT ERROR: Set when the receive packet has 1 to 7 extra bits at the end of the packet. This may be due to collision or faulty transceiver. Can generate an interrupt if enabled by DLCR3<2>.
1	CRC_ERR	R,C,0	CRC ERROR: Set when the packet has CRC errors indicating that the packet is corrupted. Can generate an interrupt if enabled by DLCR3<1>.
0	OVRFLO	R,C,0	RECEIVE BUFFER OVERFLOW: Set when the receive buffer is full. Can generate an interrupt if enabled by DLCR3<0>.

5.2.3 DLCR2 - Transmit Interrupt Enable Register

This register contains the bits to enable the status bits in DLCR0 to generate interrupts to the host.

BIT	SYMBOL	L	DESCRIPTION
7	TXOK INT ENABLE	R,W,0	TXOK INTERRUPT ENABLE: When set high, it enables transmit OK signal, TXOK to generate an interrupt.
6	0	N,0	RESERVED BIT.
5	SELF_RECP INT ENABLE	R,W,0	SELF RECEPTION INTERRUPT ENABLE: Enables the transmit receive in loop back to produce an interrupt.
4	0	N,0	RESERVED BIT.
3	JABBER INT ENABLE	R,W,0	JABBER INTERRUPT ENABLE: When high, enables JABBER to generate an interrupt.
2	COLLISION INT ENABLE	R,W,0	COLLISION INTERRUPT ENABLE: When high, enables COL to generate an interrupt.
1	16 COL INT ENABLE	R,W,0	16 COLLISION INTERRUPT ENABLE: When high, enables 16COL to generate an interrupt.
0	HWR_ERR INT ENABLE	R,W,0	HWR_ERR INTERRUPT ENABLE: When high, enables host write error signal, HWR_ERR to produce an interrupt.

5.2.4 DLCR3 - Receive Interrupt Enable Register

This register contains the bits to enable the status bits in DLCR1 to generate interrupts to the host.

BIT	SYMBOL	L	DESCRIPTION
7	PKT_RDY INT ENABLE	R,W,0	PKT_RDY INTERRUPT ENABLE: When this bit is set high, it will enable PKT_RDY (Packet Ready signal) to generate an interrupt.
6	HRD_ERR INT ENABLE	R,W,0	HRD_ERR INTERRUPT ENABLE: When high, enables HRD_ERR (Host Read Error) to generate an interrupt.
5	DMA_EOP INT ENABLE	R,W,0	DMA_EOP INTERRUPT ENABLE: When high, enables the DMA_EOP to generate an interrupt.
4	RMTRST INT ENABLE	R,W,0	RMTRST INTERRUPT ENABLE: When high, allows the RMTRST (Remote Reset Packet Received) to generate an interrupt.
3	SRT_ERR INT ENABLE	R,W,0	SRT_ERR INTERRUPT ENABLE: When high, enables SRT_ERR (Received Short Packet) to generate an interrupt.
2	ALG_ERR INT ENABLE	R,W,0	ALG_ERR INTERRUPT ENABLE: When high, enables ALG_ERR (Alignment Error) to generate an interrupt.
1	CRC_ERR INT ENABLE	R,W,0	CRC_ERR INTERRUPT ENABLE: When high, enables CRC_ERR to generate an interrupt.
0	OVRFLO INT ENABLE	R,W,0	OVRFLO INTERRUPT ENABLE: When high, enables OVRFLO (Receive Buffer Over flow) flag to generate an interrupt.

5.2.5 DLCR4 - Transmit Mode Register

This register contains the collision count value (up to 16 collisions). SSI 78Q8373 will attempt to re-transmit the current packet up to 16 times. After which, depending on the values setting in BMR11<2:0>, the host can either skip the current packet and continue to transmit remaining packets in the transmit buffer or re-transmit the current packet again.

BIT	SYMBOL	L	DESCRIPTION
7-4	COL3-0	R,0	COLLISION COUNT: These 4 bits store the collision counter value. Bit 3 is the most significant bit of the count.
3	NO_BACK	R,W,0	NO BACKOFF ENABLE: When set to 1, it will disable the binary exponential backoff circuitry.
2	NOT_CB	R,W,1	NOT_CONTROL BIT: The inverse of this bit is available for general use on th CB pin.
1	EDLOOP	R,W,1	ENDEC LOOP BACK: Active low. This bit enables the loop back function of the 78Q8370-ENDEC. Loop back is active when this bit is set to ‘0’.
0	DSC	R,W,0	DISREGARD CARRIER: Program this bit to zero for normal network operation. When set to high, the transmitter will not defer to traffic on the network.

5.2.6 DLCR5 - Receive Mode Register

This register controls the way that SSI 78Q8373 receives a packet. DLCR5<5> set high allows SSI 78Q8373 to accept packets that contains alignment or CRC errors. DLCR5<3> set high allows SSI 78Q8373 to accept packets with packet length that is between 6 bytes and 2047 bytes (excluding preamble and CRC). Allowing the acceptance of a 6-byte packet is usually a diagnostic mode. The Receive Buffer Empty (DLCR5<6>) informs the host when there is no more data in the receive buffer memory.

<table>
<tr><th>BIT</th><th>SYMBOL</th><th>L</th><th>DESCRIPTION</th></tr>
<tr><td>7</td><td>RESERVED</td><td>0</td><td>RESERVED BIT.</td></tr>
<tr><td>6</td><td>RX_BUFMTY</td><td>R,1</td><td>RECEIVE BUFFER EMPTY: When the receive bufffer has no data for the host, this is set to a high by 78Q8373.</td></tr>
<tr><td>5</td><td>ACPT_BADPKT</td><td>R,W,0</td><td>ACCEPT BAD PACKET: If this bit is set high, short packets and packets with alignment and/or CRC errors will be accepted. Otherwise, errorneous packets are rejected.</td></tr>
<tr><td>4</td><td>ADD_SIZE</td><td>R,W,0</td><td>ADDRESS SIZE: When set high, only the first 40 bits of the destination address are compared to the Node ID (normal mode requires the comparison of all 48 bits).</td></tr>
<tr><td>3</td><td>ENA_SRTPKT</td><td>R,W,0</td><td>ENABLE SHORT PACKET: When set high, allows short packets (packet length between 6 and 2047 bytes minus the preamble and CRC) to be stored in the receive buffer memory. When this bit is set low, any packets with less than 60 bytes in length will be rejected.</td></tr>
<tr><td>2</td><td>ENA_RMTRST</td><td>R,W,0</td><td>ENABLE REMOTE RESET: When set to a 1, enables other nodes on the network to reset external peripheral(s) connected to this node. If set to a 0, a received packet with the 0900h pattern in the Type Field will not succeed in resetting these peripherals</td></tr>
<tr><td>1,0</td><td>AM1,0</td><td>R,W,0,1</td><td>ADDRESSING MODE BITS: These two bits control the address filtering of the incoming packets.
<table>
<tr><th>AM1</th><th>AM0</th><th>ADDRESSES ACCEPTANCE MODES</th></tr>
<tr><td>0</td><td>0</td><td>REJECT ALL PACKETS</td></tr>
<tr><td>0</td><td>1</td><td>NODE ID, BROADCAST and MULTICAST GROUP</td></tr>
<tr><td>1</td><td>0</td><td>NODE ID, BROADCAST and MULTICAST HASH TABLE</td></tr>
<tr><td>1</td><td>1</td><td>ACCEPT ALL PACKETS</td></tr>
</table>
</td></tr>
</table>

5.2.7 DLCR6 - Configuration Register 0

<table>
<tr><th>BIT</th><th>SYMBOL</th><th>L</th><th>DESCRIPTION</th></tr>
<tr><td>7</td><td>$\overline{\text{ENADLC}}$</td><td>R,W,1</td><td>ENABLE DATA LINK CONTROLLER: Active low. Enables the receiver and transmitter of 78Q8373. Setting this bit to high will reset all the state machines to their idle states and allows access to Node ID and Hash Table registers (depending on DLCR7<3:2> settings).</td></tr>
<tr><td>6</td><td>RAMSP</td><td>R,W,0</td><td>RAM SPEED: When set to 1, selects 100 nsec cycle SRAM. Otherwise, the SRAM is of 150 nsec cycle.</td></tr>
<tr><td>5</td><td>HBYTE</td><td>R,W1</td><td>HOST BYTE/WORD SELECT: If set high, host system bus will operate in byte mode. If set to 0, it will operate in word mode.</td></tr>
<tr><td>4</td><td>RBYTE</td><td>R,H,1</td><td>RAM BYTE: When set high, the RAM databus will operate in byte mode, otherwise it will be word mode. In PCMCIA mode, this bit will be internally hard set to 1. This is because PCMCIA pinout makes use of the higher RAM databus. The following table is valid ONLY for Generic Bus mode:
<table>
<tr><th>HBYTE</th><th>RAMBUS</th><th>HOST</th><th>BUFFER</th></tr>
<tr><td>0</td><td>0</td><td>word</td><td>word</td></tr>
<tr><td>0</td><td>1</td><td>word</td><td>byte</td></tr>
<tr><td>1</td><td>0</td><td colspan="2">DO NOT USE</td></tr>
<tr><td>1</td><td>1</td><td>byte</td><td>byte</td></tr>
</table></td></tr>
<tr><td>3,2</td><td>TS1,0</td><td>R,W,0,1</td><td>TRANSMIT BUFFER SIZE: Sets configuration of transmit buffer.
<table>
<tr><th>TS1,0</th><th>TX BANKS</th><th>SIZE OF TX BANK</th><th>TOTAL TX BUFFER</th></tr>
<tr><td>00</td><td>1</td><td>2 KB</td><td>2 KB</td></tr>
<tr><td>01</td><td>2</td><td>2 KB</td><td>4 KB</td></tr>
<tr><td>10</td><td>2</td><td>4 KB</td><td>8 KB</td></tr>
<tr><td>11</td><td>2</td><td>8 KB</td><td>16 KB</td></tr>
</table></td></tr>
<tr><td>1,0</td><td>BS1,0</td><td>R,W,0,1</td><td>BUFFER MEMORY SIZE: Sets configuration of total Buffer Size.
<table>
<tr><th>BS1</th><th>BS0</th><th>SRAM SIZE</th></tr>
<tr><td>0</td><td>0</td><td>8 KB</td></tr>
<tr><td>0</td><td>1</td><td>16 KB</td></tr>
<tr><td>1</td><td>0</td><td>32 KB</td></tr>
<tr><td>1</td><td>1</td><td>64 KB</td></tr>
</table></td></tr>
</table>

5.2.8 DLCR7 - Configuration Register 1

BIT	SYMBOL	L	DESCRIPTION
7,6	CTM1,0	R,H,00	CONTROLLER TEST MODES: Write 00 for normal operation.
5	NOT_STBY	R,W,1	NOT STANDBY (POWER DOWN): Active low. The power down mode is for energy saving. If set high, it enables power to the chip for all functions.
4	RDYSEL	R,—	READY SELECT: Reflects the real time image of the RDYSEL pin (pin 94). If RDYSEL pin is high, READY interface with the host is active high. Otherwise it is active low.
3,2	RBNK1,0	R,W,0,0	REGISTER BANK SELECT: To select the upper 8 registers as shown below:
1	EOPSEL	R,W,0	END OF PROCESS PIN SIGNAL POLARITY: When high, EOP pin is active high. When low, EIP pin is active low.
0	INTLMOT	R,W,0	INTEL or MOTOROLA MODE: System must be in word mode. This applies to the non-transmitted buffer header and the packet data. When this bit is low (INTEL MODE), the least significant byte will occupy the even address. Otherwise, the most significant bytes will occupy the even address (MOTOROLA MODE).

RBNK1	RBNK0	REGISTERS
0	0	DLCR0-7 + IDR8-13 + TDR14,15
0	1	DLCR0-7 + HTR8-15
1	0	DLCR0-7 + BMR8-15
1	1	RESERVED

5.3 NODE ID REGISTERS

5.3.1 IDR 8:15 - Node ID Registers

IDR	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
8	ID7	ID6	ID5	ID4	ID3	ID2	ID1	ID0
9	ID15	ID14	ID13	ID12	ID11	ID10	ID9	ID8
10	ID23	ID22	ID21	ID20	ID19	ID18	ID17	ID16
11	ID31	ID30	ID29	ID28	ID27	ID26	ID25	ID24
12	ID39	ID38	ID37	ID36	ID35	ID34	ID33	ID32
13	ID47	ID46	ID45	ID44	ID43	ID42	ID41	ID40

The Node ID registers (IDR8-13) are located in register bank '00' (DLCR7<3:2> = 00) at address xxx8H through xxxDH. The unique Ethernet address is written into these registers during the initialization of the node with the first byte of the Ethernet address at IDR8. The IDR registers are readable and writeable only when $\overline{\text{ENADLC}}$ = 1 (DLCR6<7>). When $\overline{\text{ENADLC}}$ = 0, normal network operations resume with the DLC controller.

During the reception of a packet, the destination address of the packet is matched with the Node ID in the IDR registers. Depending on the Address Mode (DLCR5<1:0>) selected for the node, either all or some of the six bytes of the incoming destination address are compared to the Node ID. If they match then the packet is accepted. Any mismatch in the addresses would result in the rejection of the packet.

5.4 TIME DOMAIN REFLECTOMETRY REGISTERS

5.4.1 TDR 14,15 - Time Domain Reflectrometry (TDR) Registers

TDR	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
14	TD7	TD6	TD5	TD4	TD3	TD2	TD1	TD0
15	SELECT 3V		TD13	TD12	TD11	TD10	TD9	TD8

The Time Domain Reflectometry (TDR14-15) registers provide a means of locating a fault on the network. The TDR registers are located in the same register bank as the IDR8-13 but at address xxxEH through xxxFH. This 14-bit diagnostic counter keeps a count of the number of bits that has been transmitted during transmission of a packet starting from the preamble and including the CRC bits. TDR14 is the least significant byte and TDR15 is the most significant byte of the counter. Fourteen bits are sufficient for the packet transmission of an IEEE compliant LAN. The remaining 2 bits (TDR15<7:6>) are used to select 3-volt operation of the 78Q8373.

BIT	SYMBOL	L	DESCRIPTION
7,6	SELECT3V	R,W,0	SELECT 3V. Programming these bits to 11 will select the 3-volt operating mode. All other combinations will select the default 5-volt operating mode.

The TDR count is cleared on the transmission of the next packet. A short or open on the network would cause reflections of the signal on the network that can be detected as a loss of carrier sense or a false collision respectively. In the event that a fault occurs on the network, the error messages in DLCR0<2> or DLCR0<4> will be able to indicate the type of fault. The TDR count can then be used to estimate the distance from the node to the fault location along the network cable.

5.5 HASH TABLE REGISTERS

5.5.1 HTR 8:15 - Hash Table Registers

HTR	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
8	HT7	HT6	HT5	HT4	HT3	HT2	HT1	HT0
9	HT15	HT14	HT13	HT12	HT11	HT10	HT9	HT8
10	HT23	HT22	HT21	HT20	HT19	HT18	HT17	HT16
11	HT31	HT30	HT29	HT28	HT27	HT26	HT25	HT24
12	HT39	HT38	HT37	HT36	HT35	HT34	HT33	HT32
13	HT47	HT46	HT45	HT44	HT43	HT42	HT41	HT40
14	HT55	HT54	HT53	HT52	HT51	HT50	HT49	HT48
15	HT63	HT62	HT61	HT60	HT59	HT58	HT57	HT56

The Hash Table Registers (HTR8-15) are located in register bank '01' (DLCR7<3:2> = 01) at address xxx8H through xxxFH. The Hash Table allows group addressing by filtering multicast addressed packets on the network. The 64-element table provides the host to select which of the the node should belong to and sets the appropriate groups to a 1. If the host does not want to belong to any groups, the entire table will be set to 0.

As a packet is received, the bit stream goes through the CRC block. If the incoming address is a multicast address (least significant bit of the destination address is a 1) then the following occurs. After the last bit of the 48-bit destination address has passed through the CRC block, the least significant 6 bits of the CRC at that point is used to index one of the 64 elements of the Hash Table. If that Hash Table element is set to a 1 then the packet is accepted. If it is set to a 0 the packet is rejected.

The Hash Table is readable and writeable when $\overline{\text{ENADLC}}$ = 1 and the DLCR7<3:2> = 01. Selecting the Address Mode to include multicast hash addressing would enable this filtering. For instance, AM<1:0> = 10 (DLCR5<1:0>) allows for physical, broadcast and multicast hash addressing but AM<1:0> = 01 does not i.e. the hash filter would not be utilized in these situations. (AM<1:0> = 01 only allows for physical, broadcast and multicast group addressing).

5.6 BUFFER MEMORY REGISTERS

There are 8 registers for buffer memory interface, 16 collision control and DMA control in this set of register bank. Each bit is explained in the following sections.

5.6.1 BMR8, 9 - Buffer Memory Port

Reading or writing between the host and SSI 78Q8373 buffer memory is done via these two registers. The location for the buffer memory is dependent on the address unit of SSI 78Q8373. When SSI 78Q8373 is configured as byte mode, only BMR8 is used. Both BMR8 and BMR9 are used when the SSI 78Q8373 is set to word mode configuration.

BIT	SYMBOL	L	DESCRIPTION
7-0	BMR8<7:0> BMR9<7:0>	R,W,_	PACKET RECEIVE and TRANSMIT REGISTERS for the host and 78Q8360.

5.6.2 BMR10 - Transmit Packet Counter

This register consists the TRANSMIT START BIT (TXST) and the total packet count for the SSI 78Q8373 to transmit. The packet count is the number of packets that the host wants to transmit. To activate transmission, the packet count must be written the same time that the TXST bit is set to a 1. The user should not write into this register until the packet count has reached zero.

BIT	SYMBOL	L	DESCRIPTION
7	TXST	R,W,0	TRANSMIT START BIT: When the packet(s) in the transmit buffer is ready for transfer to the network, this bit is set to 1 in order to activate the transmit operation. Always read as a 0.
6-0	PACKET CNT<6:0>	R,W,0	TRANSMIT PACKET COUNT: The total number of packets to be transmitted to the network. Each time a packet is successfully transmitted, the packet count is decremented. The host can read this register to check how many packets have not been transmitted.

5.6.3 BMR11 - 16 Collision Control

The setting of this register determines the actions of the controller to be taken after 16 consecutive attempts to transmit a packet. There are four modes (controlled by $\overline{\text{HALT}}$, RESTART and SKIP bits in the register) to be selected:

(1) automatic re-transmission of colliding packet
(2) automatic skip of the colliding packet after 16 attempts
(3) Halt for host intervention and retry transmission of colliding packet
(4) Halt for host intervention and discontinue transmission of colliding packet.

<table>
<tr><th>BIT</th><th>SYMBOL</th><th>L</th><th>DESCRIPTION</th></tr>
<tr><td>7</td><td>OSC_OFF</td><td>R,H,0</td><td>OSCILLATOR SHUTOFF: When enabled (‘1’), this bit shuts off the internal oscillator. Setting this bit while using an external canned oscillator can damage the chip. For this reason, this bit can only be set after the standby mode is entered (by setting DLCR7<2> = ‘1’)</td></tr>
<tr><td>6</td><td>$\overline{\text{AUTOPD}}$</td><td>R,W,0</td><td>AUTO POWER: Upon power-up/reset, the chip is in automatic power management mode. This mode can be disabled by writing a ‘1’ to this bit.</td></tr>
<tr><td>5-3</td><td>RESERVED</td><td>-</td><td>RESERVED BIT.</td></tr>
<tr><td>2
1
0</td><td>HALT
RESTART
SKIP</td><td>R,W,0</td><td>16 COLLISION CONTROL: These three bits control the action to be taken by 78Q8373 in the event that 16 collisions occur in the transmission of a packet. Host intervention is possible as shown below.
<table>
<tr><th>HALT</th><th>RE-START</th><th>SKIP</th><th>DESCRIPTION OF ACTION TAKEN</th></tr>
<tr><td>1</td><td>X</td><td>1</td><td>Do not halt. Skip colliding packet and continue transmitting.</td></tr>
<tr><td>1</td><td>X</td><td>0</td><td>Do not halt. Retry transmission of colliding packet.</td></tr>
<tr><td>0</td><td>X</td><td>X</td><td>Halt and await instruction from host for BMR11<1:0>. 11’ : results in colliding packet skipped and transmission resumed.10’: results in colliding packet re-transmitted.</td></tr>
</table>
</td></tr>
</table>

5.6.4 BMR12 - DMA Enable

The DMA RENA and DMA TENA activates the DMA operation as follows:

BIT	SYMBOL	L	DESCRIPTION
7-2	RESERVED	-	RESERVED BIT.
1	DMA_RENA	R,W,0	RECEIVE READ DMA ENABLE: When enabled (active high), it activates receive read DMA from the host.
0	DMA_TENA	R,W,0	TRANSMIT WRITE DMA ENABLE: When enabled (active high), it activates transmit write DMA from the host to ICE's buffer memory.

5.6.5 BMR13 - DMA Burst & Transceiver Mode Register

BIT	SYMBOL	L	DESCRIPTION
7	$\overline{\text{APOL}}$	R,W,0	AUTO POLARITY: When set to 0, it enables the automatic polarity correction of the received data. The reverse polarity is identified from either the start of idle signal or link pulses.
6	RTH	R,W,0	REDUCED THRESHOLD: When set high, twisted pair receive threshold is reduced by 3 dB (for longer than the recommended 100 meters cable).
5	$\overline{\text{ENLI}}$	R,W,0	ENABLE LINK INTEGRITY: When set low, both transmit and receive link test functions are enabled. When high, no link test is performed and the link status is assumed to be up and twisted pair port is selected if auto select mode is enabled. When this bit is enabled, the transmit link pulses function is always active regardless fo the status of the link.
4	PORT_SEL	R,W,0	PORT SELECT: This bit manually selects between Twisted Pair (when 0) or AUI (when 1) and is only applicable when ASEL bit (BMR13<3>) is high (disabled).
3	$\overline{\text{ASEL}}$	R,W,0	AUTO PORT SELECT: When set to 0, automatic port selection mode is in effect. The selection is based on the state of link integrity status. Twisted pair port is selected or a good link and AUI port is selected for a link down condition. When set to 1, manual port selection is in effect through POrT_SEL bit (BMR13<4>).
2	DMT	R,W,0	DMA DMREQ DROP TIME: When set low, DMREQ drops at the next-to-last transfer of DMA burst (same with 78Q8360). When set high, DMREQ drops at the last transfer of the burst.
1,0	DMAB1,0	R,W,0	DMA BURST: This two bits select the burst length for DMA operation. The burst length transfer can either be byte mode or word mode depending on the system bus setting (SYSBUS in DLCR6<5>).

DMAB1	DMAB0	BURST LENGTH
0	0	1
0	1	4
1	0	8
1	1	12

5.6.6 BMR14 - Receive Filter & Interrupt Enable Register

BIT	SYMBOL	L	DESCRIPTION
7	RESERVED	-	RESERVED BIT.
6	INT ENABLE	R,W,0	LINK DOWN INTERRUPT ENABLE: When high, enables LD (BMR15<6>) to generate an interrupt. Since LD cannot be cleared, the interrupt can be deactivated by clearing this enable bit.
5-3	RESERVED	-	RESERVED BIT.
2	SKP_RX	R,W,0	SKIP RECEIVE PACKET: If the host is reading the received packets in the buffer and decides to skip the current packet then this bit is set to high. The 78Q8373 controller will perform a hardware skip on the internal pointer within 200 ns to the next packet start address if there is another packet in the buffer.
1	INT ENABLE	R,W,0	SQE INTERRUPT ENABLE: When high, enables SQE (BMR15<1>) to generate an interrupt.
0	RXF	R,W,1	RECEIVE FILTER: When set to 1, disables the reception of own transmitted packet in the ACCEPT ALL PACKETS mode. When set to 0, enables the reception of own transmitted packet in the ACCEPT ALL PACKETS mode. (1)

(1) *Power up value for this bit is a '1' for SSI 78Q8373 and '0' for SSI 78Q8360. This may be used by the software driver to differentiate between the two chips.*

5.6.7 BMR15 - Transceiver Status Register

BIT	SYMBOL	L	DESCRIPTION
7	RESERVED	-	RESERVED BIT.
6	LD	R,0	LINK DOWN: When high, it indicates that the twisted pair port is in link down condition. Can generate an interrupt if enabled by BMR14<6>. The chip powers up in link up condition. When ENLI (BMR13<5>) is high (disabled), this bit is forced to a '0' (link up condition).
5	OWCOL	R,C,0	OUT OF WINDOW COLLISION: Indicates that a collision occurred after the slot time (51.2 μs). Transmissions terminated and rescheduled as in normal collision. Writing a '1' will clear this bit. For software compatibility with the 78Q8360, writing a '1' to the COL bit (DLCR0<2>) will also clear this bit.
4	RESERVED	-	RESERVED BIT.
3	RPI	R,0	REVERSE POLARITY INDICATION: When high, it indicates that inverted data is being received over the twisted pair wire due to wiring error. This bit is only applicable when APOL (BMR13<2>) is low (enabled). When APOL is high (disables) this bit can never be set.
2	RESERVED	-	RESERVED BIT.
1	SQE	R,C,0	SIGNAL QUALITY ERROR: When high, indicates detection of SQE signal at the end of a transmission. This bit applies to both the AUI and TP ports. Can generate interrupt if enabled by BMR14<1>. Writing a '1' clears this bit.
0	RESERVED	-	RESERVED BIT.

5.7 PCMCIA REGISTERS

There are 2 registers for the PCMCIA interface. Each bit is explained in the following sections.

5.7.1 CCR0 - Configuration Option Register

BIT	SYMBOL	L	DESCRIPTION
7	SRESET	R,W,0	SYSTEM RESET: Setting this bit high is equivalent to assertion of hardware reset (except that this bit is not cleared). This bit is also reflected at the XRST pin to reset the rest of the devices on the card.
6	LevIREQ	R,W,0	LEVEL MODE INTERRUPT REQUEST: When high, level mode interrupt is selected. When low, pulse mode interrupt is selected.
5:0	CI(5:0)	R,W,0	CONFIGURATION INDEX: This field is written with the index number of the entry in the Card's Configuration Table that corresponds to the configuration which the system chooses for the card. When CI(5:0) is 0, the chip does not respond to any I/O cycle, but will use the memory cycle.

5.7.2 CCR1 - Card Configuration and Status Register

BIT	SYMBOL	L	DESCRIPTION
7	NI	R,0	NOT IMPLEMENTED
6	NI	R,0	NOT IMPLEMENTED
5	IOis18	R,W,0	I/O is 8 bit: This bit set high indicates to the host that the system is only capable of 8-bit transfer on its data bus. Since the 78Q8373 can support 16-bit transfer, the default value of this bit is '0.' This bit does not affect the host byte/word mode setting of the 8373 which is set by HBYTE (DLCR6<5> bit).
4	RESERVED	R,0	RESERVED.
3	Audio	R,W,0	Audio Enable: This bit set to one will enable signals from SPKRIN to SPKR.
2	PwrDwn	R,W,0	Power Down: This bit has the same function as the NOT_STBY bit (DLCR7<5>) but with different polarity. The chip will be powered down if either this bit is set to '1' or NOT_STBY bit is set to '0.' When configured for PCMCIA interface mode and power down is activated, the $\overline{\text{XPD}}$ pin will indicate it by going low.
1	Intr	R,0	Interrupt Request Status: This bit represents the internal state of the interrupt request. This signal remains true (high) until the condition which caused the interrupt request has been serviced.
0	RESERVED	R,0	RESERVED.

78Q8373 & Host Interface Configuration

Section 6

6 78Q8373 & HOST INTERFACE CONFIGURATION

6.1 PCMCIA INTRODUCTION

PCMCIA is an acronym for Personal Computer Memory Card International Association. Its goal is to promote interchangeability of PC Cards among a variety of computer and other electronic products.

PC Cards are approximately 54 by 85 millimeters, but differ in thickness. Type 1 cards are 3.3 mm thick and type 2 cards are 5.0 mm. All have a 68-pin interface at one end.

6.1.1 Memory and I/O Address Space

A Memory Address Space of 64 Mbytes (A0-A25) is permitted for each memory card installed in a system. The Memory Address Space consists of Common Memory and Attribute Memory. The Common Memory may be accessed by a host for memory read and write operations.

There is an additional 64 Mbytes address space for Attribute Memory which is selected by the $\overline{REG}$ signal at the interface. The Attribute Memory is divided into

- Card Information Structure (CIS) - contains the manufacturer's description of card capabilities and specifications.
- Card Configuration Registers (CCR) - a set of registers that allows the card to be configured by the host.

The I/O Address Space of 64 Mbytes is shared and divided among all cards installed in the system. The I/O interface requires that the Memory-Only Interface also be implemented within the same socket, and that the Memory-Only Interface be selected in the socket when no card is inserted and immediately following Card reset and the application of Vcc to the card. The I/O interface also supports additional signals like $\overline{IREQ}$, $\overline{IOIS16}$, $\overline{IOWR}$, $\overline{IORD}$, $\overline{SPKR}$, $\overline{INPACK}$ and $\overline{STSCHG}$.

The following diagram summarizes which address space that the host is accessing depending on the logic values of REG, I/O read/write and Memory read/write signals.

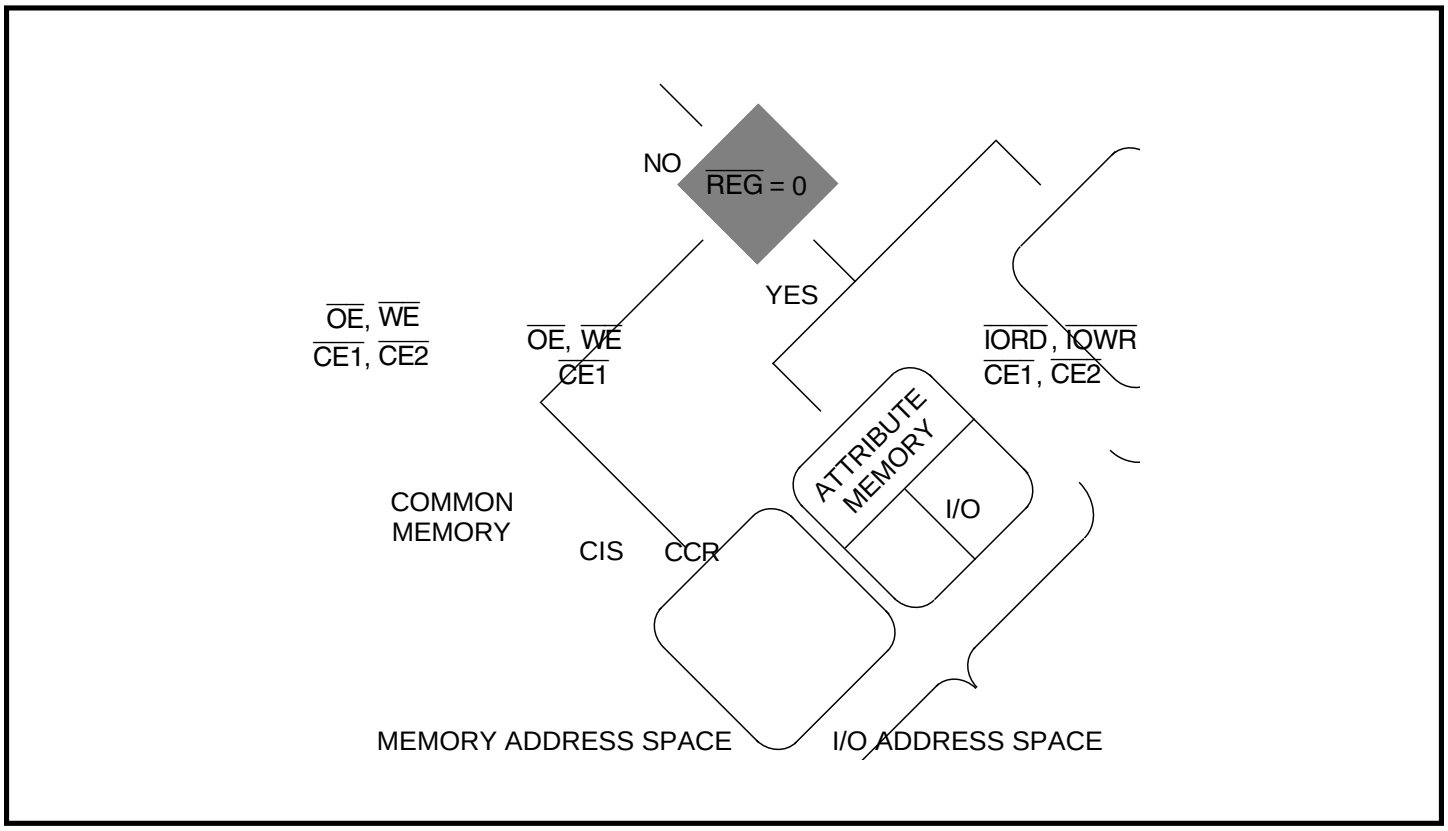

Figure 6-1. Host Address Space Accessing

6.2 PCMCIA INTERFACE FOR SSI 78Q8373

SSI 78Q8373 complies to the PCMCIA Release 2.1 Specifications and powers up as a memory card when in PCMCIA mode. To enter the I/O mode, the Configuration Index CI(5:0) in the CCR0 register must be written with a non-zero value. Only then can the other registers of SSI 78Q8373 be accessed by the host.

In the Attribute Memory Address Space, the CIS is located at address 0 and the CCR is located at an offset value determined by the CCRA pin, illustrated in Figure 6-2 below.

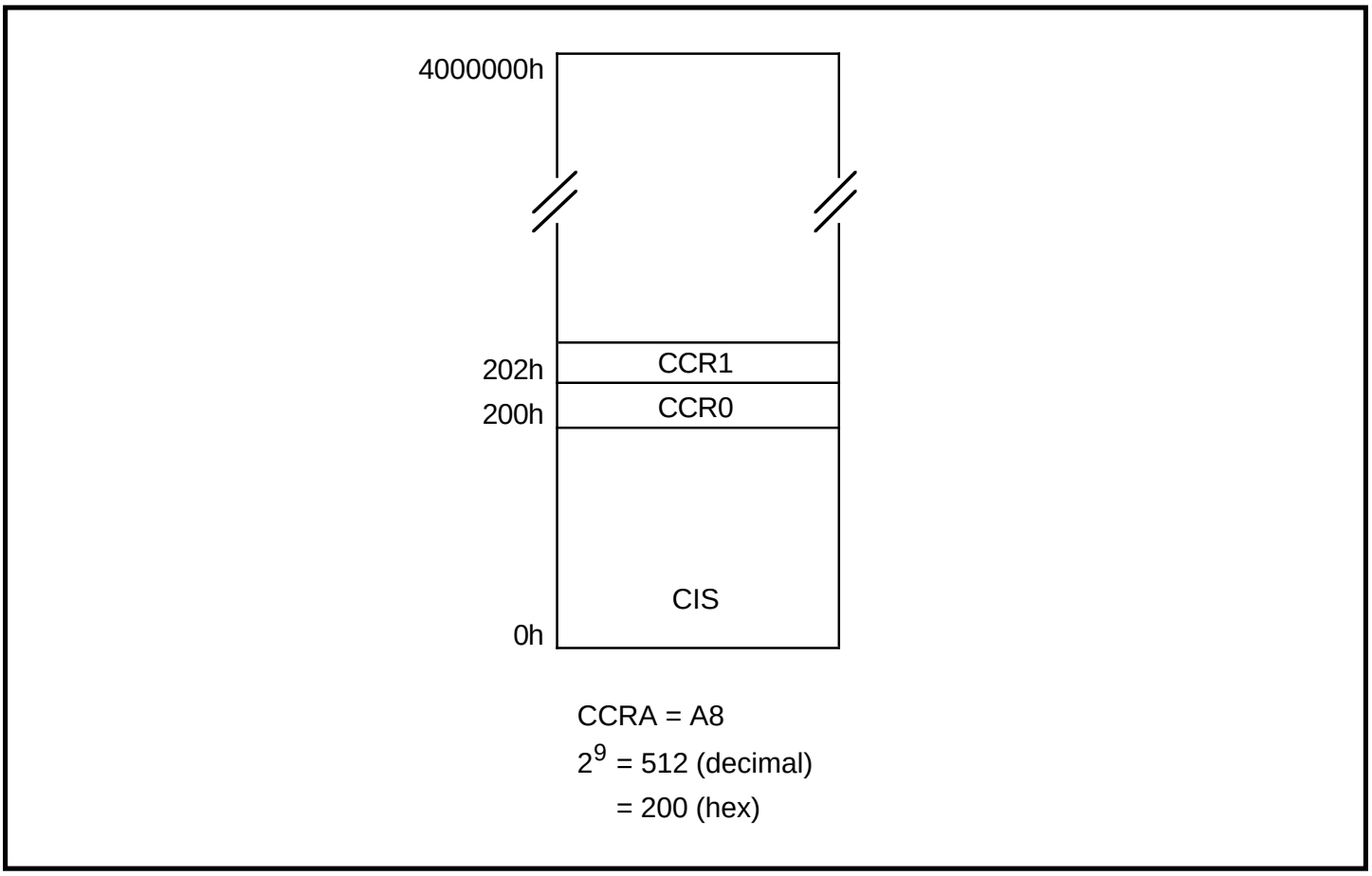

Figure 6-2. Attribute Memory Address Space

CCRA pin must be connected to another address pin apart from A(3:0). For instance, if CCRA is connected to A8, then CCR0 is located at address 200h, an offset of 200h from address 0. An example of how to use the SSI 78Q8373 with a Flash Memory or EEPROM is shown below.

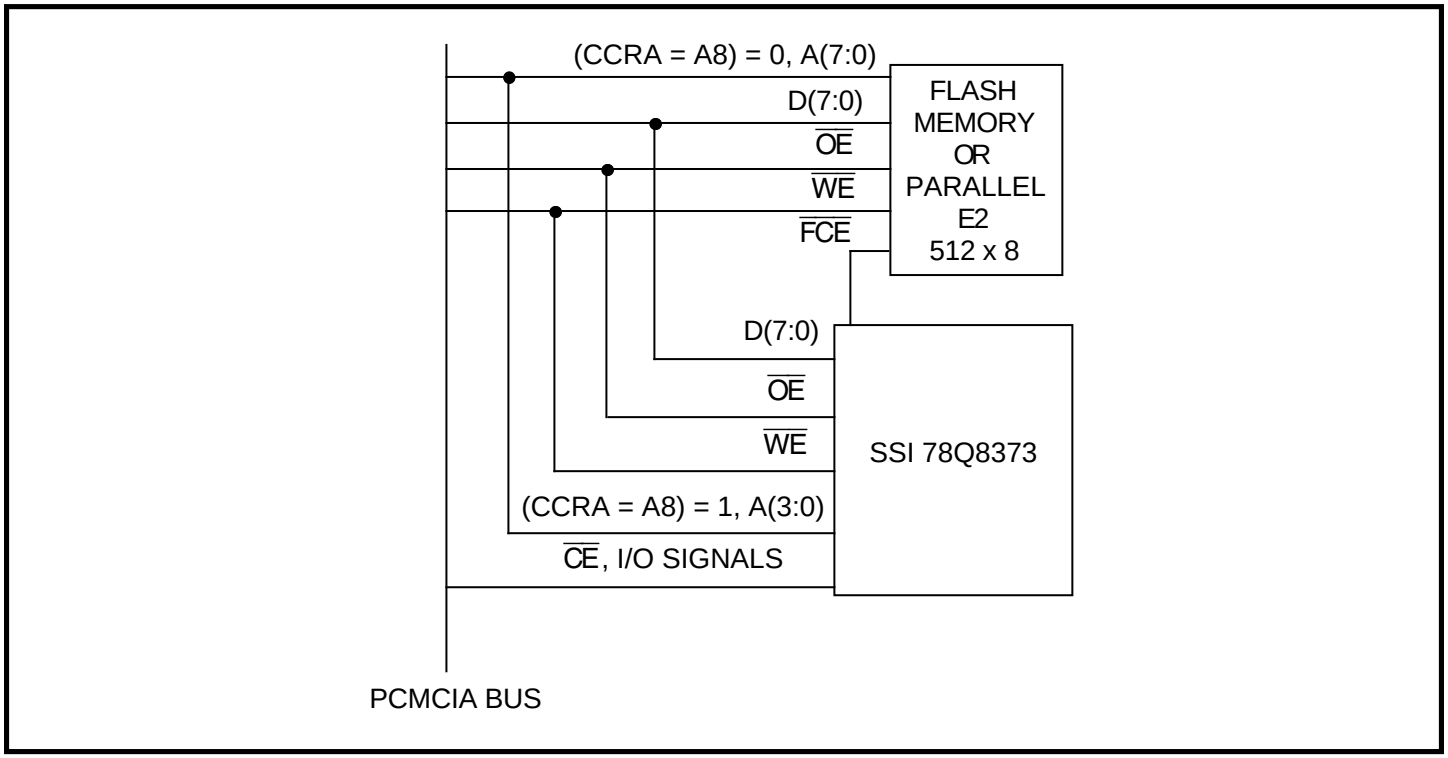

Figure 6-3. SSI 78Q8373 Interface to Flash Memory or EEPROM

6.3 GENERIC BUS INTERFACE FOR SSI 78Q8373

For non-PCMCIA applications, the SSI 78Q8373 can interface with the host via a 'generic' bus interface. Transferring of data, packet status, packet sizes and so on can be accessed easily by the host either by using programmed I/O or DMA modes. Packets to be transferred to the network must first be stored in the buffer memory via a register called Buffer Memory Register 8 (BMR8). Similarly, packets to be read by the host is retrieved via the BMR8. Thus BMR8 acts as a window to the buffer memory.

To interface with the host, the SSI 78Q8373 has 4 host address pins (HA<3:0>), 16 host data pins (HD<15:0>), 3 status pins ($\overline{\text{SWSB}}$, EOP, $\overline{\text{INT}}$) and handshake/chip select signals ($\overline{\text{CS}}$, DMREQ, $\overline{\text{DMACK}}$, $\overline{\text{RD}}$, $\overline{\text{WR}}$, READY). The host is also able to access the SSI 78Q8373's internal registers to retrieve more information (refer to the Register section).

78Q8373 & Medium Interface Configuration

Section 7

7 78Q8373 & MEDIUM INTERFACE CONFIGURATION

The SSI 78Q8373 has an integrated twisted pair transceiver and supports interface to coax transceiver through AUI signaling. The two port selection (either AUI or TP) is done automatically based on the status of link integrity. In a link-good state, the TP port is selected and in a link-fail state, the AUI port is selected. This automatic selection can be disabled by writing a '1' to register bit BMR13<3> and manual selection is in effect. In manual selection mode, the AUI or TP port may be selected by writing appropriate value to BMR13<4>.

7.1 TWISTED PAIR TRANSCEIVER

The TP transceiver supports complete IEEE 10BASE-T functionality as well as several enhanced functions such as autopolarity detection and correction, smart-squelch logic and long distance mode.

7.1.1 Link Integrity

During idle periods, link pulses are generated and received by both MAUs (Medium Attachment Units) at either end of the twisted pair to ensure that the cable has not been broken or shorted. A positive, 100 ns Link Integrity signal is generated and transmitted by the SSI 78Q8373 every 13 ms during idle periods. The chip assumes a link-good state if it receives valid link pulses or a packet. If neither is received for 105 ms, the SSI 78Q8373 enters a link-fail state. It then needs 4 consecutive positive link pulses (or 8 negative link pulses) to resume link-good state. Only link pulses spaced between 3 ms and 105 ms are considered valid.

In a link-fail state, the SSI 78Q8373 disables normal Transmit, Receive, Collision, loopback and SQE test functions. The reception of a packet will put the device in a link-good state. However, that packet will not be relayed to the Manchester ENDEC unit. Subsequent packets will be relayed as per normal as long as the device remains in a link-good state.

The link status is flagged by register bit BMR15<6> as well as the LEDLTR pin. The Link Integrity function can be disabled by writing a '1' to BMR13<5> which forces the SSI 78Q8373 into a link-good state.

7.1.2 Autopolarity

Because twisted pair differential signals can easily be inverted due to wiring errors, the SSI 78Q8373 incorporates autopolarity detection and correction circuitry. Polarity circuitry monitors the polarity of the received SOI (Start Of Idle) and link pulses and corrects the data internally if the signal is inverted. The inverted polarity is flagged by register bit BMR15<3> and the autopolarity function may be disabled by writing a '1' to BMR13<7>.

7.1.3 Smart Squelch Logic

The twisted pair squelch logic dynamically adjusts the sensitivity and threshold of the receiver. Before signals begin to arrive at the TPIP/TPIN pins, the SSI 78Q8373 is in a high noise rejection, squelch state and no data is passed through. A valid incoming data needs to trip the threshold detectors with three peaks of alternating polarity occurring within a 400 ns window. Once a signal has been qualified by the squelch circuitry, the SSI 78Q8373 assumes an unsquelch state with reduced threshold. See the datasheet for the squelch and unsquelch threshold levels.

At the beginning of each packet there is a preamble consisting of alternating ones and zeros resulting in a 5 MHz Manchester signal on the twisted pair. The SSI 78Q8373 uses the standard 10BASE-T specified threshold levels to unsquelch the incoming preamble. As data begins to arrive, the 10 MHz component of the Manchester encoded signal may have less amplitude since it is attenuated more than the 5 MHz component. For this reason, the threshold levels are reduced in the unsquelch state. This greatly reduces the chance of prematurely detecting the SOI by the threshold detectors.

The twisted pair smart squelch circuitry is returned to a squelch state by any of these conditions: a normal SOI signal, an inverted SOI signal or a missing SOI signal. A missing SOI signal is assumed when no transitions crossing the threshold detectors have occurred for 250 ns after a packet has been received. In this case, a normal SOI signal is generated and appended to the received data.

7.1.4 Long Mode

Writing a '1' to BMR13<6> places the SSI 78Q8373 in long mode where the thresholds of the detectors are lowered to support longer cable length than the recommended 100 meters. Dynamic squelch circuitry is still functional in long mode. The squelch threshold of the long mode is the same as the unsquelch threshold of the normal mode and the unsquelch threshold of the long mode is another 3 dB down.

7.1.5 Collision Detection

A collision happens when both transmitting and receiving functions occur simultaneously in the twisted pair transceiver. The collision signal originating from the twisted pair transceiver is multiplexed together with the collision signal from the AUI module and is relayed to the controller. Collisions will not be reported when the device is in a link-fail state. The internal collision signal is also activated when a jabber condition occurs or when the SQE test is being performed.

7.1.6 SQE Test

An internal Signal Quality Error (SQE) test is also provided on chip. After each packet transmission, an SQE signal (also referred to as “heartbeat” signal) is sent internally to the controller. This feature is provided to match the coax transceiver functionality.

7.1.7 Jabber

An independent circuit monitors the length of each transmission and inhibits it if it surpasses a 26.2 ms maximum allowed transmit time. This function keeps a damaged node from continuously transmitting on the network. When jabber occurs, the transceiver also discontinues loopback and sends a collision signal to the controller. The jabber status is flagged by register bit DLCR0<3>.

7.1.8 Normal Loopback

The twisted pair transceiver provides the normal loopback function specified by the 10BASE-T standard. The normal loopback function is disabled when a collision occurs during which the received data from TPIP/N is passed through instead. Link fail and jabber states also disable the normal loopback.

7.1.9 LED

The LEDLT pin serves functions. A connected LED lights up during link-good state and blinks off temporarily during transmission activity.

7.1.10 TP Driver

The transmit driver consists of four differential signals, the true and complement transmit data TPOP, TPON and their respective 50 ns delayed signals TPDP, TPDN. These drivers, when combined with the resistor network shown in Fig 7.1, provide the signal pre-equalization required by the 10BASE-T standard.

A Manchester encoded data consists of 10 MHz (50 ns) component as well as 5 MHz (100 ns) pulses. A twisted pair cable attenuates a 10 MHz signal more than a 5 MHz signal. Equalization is required to decrease the relative power in the 5 MHz component transmitted by the SSI 78Q8373. This causes the 10 MHz and 5 MHz components of the signal to have approximately the same power

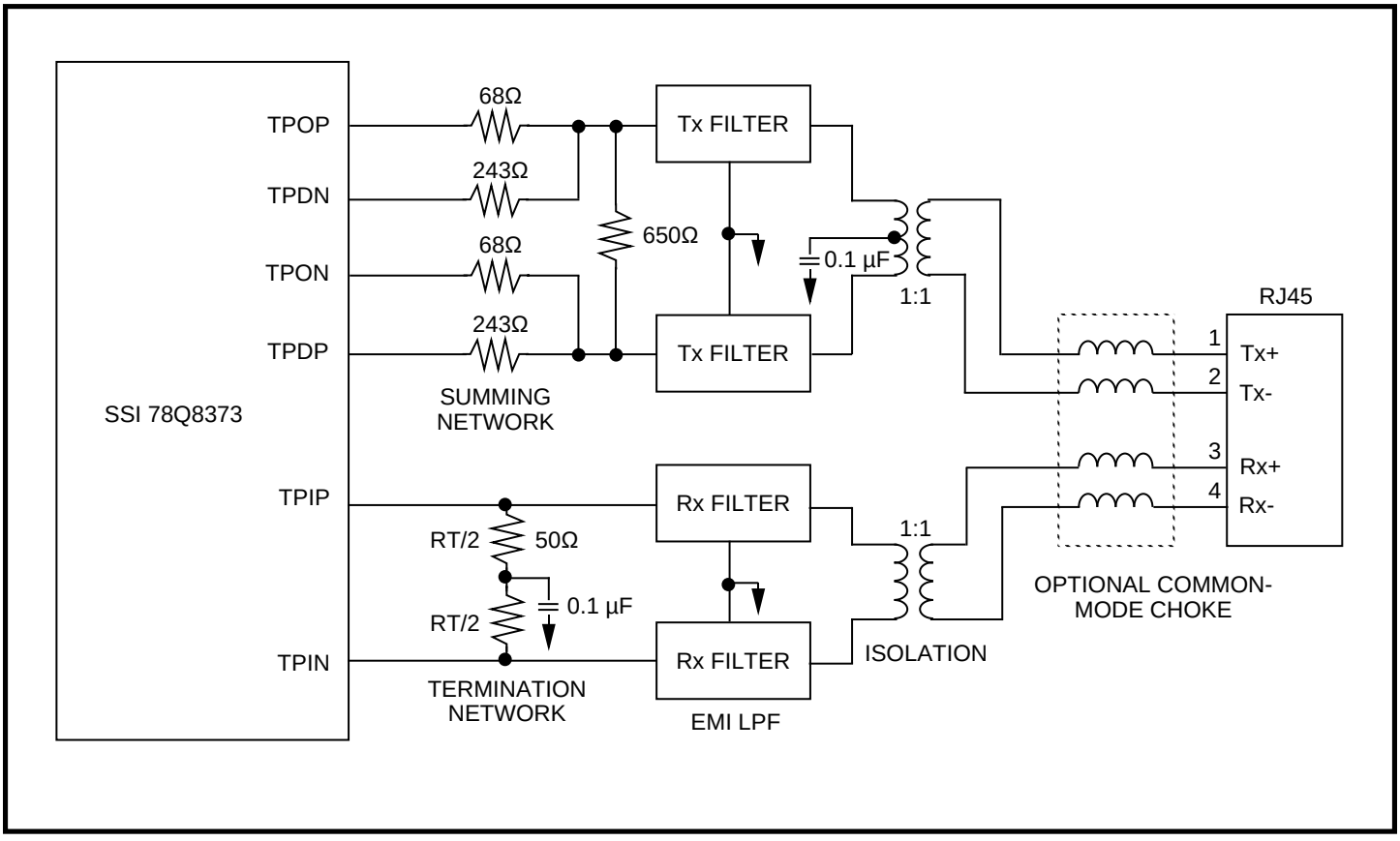

Figure 7.1. Twisted Pair Interface Connections (5 volts)

(contact Silicon Systems for 3-volt connections)

content at the far end of the twisted pair. To achieve the power reduction of the 5 MHz component, the four transmit signals are summed resistively as shown in Fig 7.2. The values of the five network resistors are selected to allow the twisted pair line to be terminated in 100 ohm.

The drivers are designed to have equal rise/fall times as well as balanced low-to-high and high-to-low propagation delays to minimize common-mode energy. It is also important to maintain equal load capacitance from the board layout for each data output so as to maintain the equal rise/fall times and propagation delays.

The twisted pair magnetics and filters shown in Fig 7.2 isolate the SSI 78Q8373 from the twisted pair media and reduce the radiated emissions. As a result of the well matched drivers, the common-mode choke is optional and the device still meets the 10BASE-T standard of +/- 50 mV of common-mode energy. Various integrated modules are available with different level of integration from a few vendors listed in Table 7.1.

Table 7.1

Option	Resistor Network	EMI Filter & Isolation	Common-mode Choke
1	Discrete	1) Pulse PE65421 2) Valor PT3877 3) BelFuse A556-2006-DE 4) FilMag 78Z1120B	(Optional)
2	Discrete	1) Pulse PE65431 2) Valor FL1012 3) Bel Fuse 0556-2006-01, 0556-3392-00	
3	1) Pulse PE65485 2) PCA EPE6052G		

7.1.11 TP Receiver

The SSI 78Q8373 twisted pair receiver uses a high-speed differential comparator designed to preserve the edge timing of the incoming data. The comparator architecture significantly minimizes the bit jitter added by the transceiver. Dual threshold detectors are used by the twisted pair smart squelch circuitry to qualify both positive and negative signal peaks. The threshold levels are dynamically controlled to further enhance the immunity to noise. Refer to the smart squelch logic section.

7.2 ATTACHMENT UNIT INTERFACE (AUI)

AUI is a standard Ethernet interface that connects Data Terminal Equipment (DTE) to a Medium Attachment Unit (MAU). There are 3 pairs of differential signals that connect to an AUI: one pair for transmission, one pair for reception and the other one pair for collision indication. A typical AUI connection diagram is given in Fig 7.2.

7.2.1 AUI Driver

The SSI 78Q8373 AUI drivers have been designed to provide balanced differential voltage levels when signaling. The drivers have equal low-to-high and high-to-low propagation delays to provide minimal skew.

At the end of transmission, the AUI drivers ramp to VDD slowly to avoid undershoot. An internal digital to analog converter ensures that the driver ramp-up occurs over approximately 8 µs resulting in a smooth transition into an idle state.

7.2.2 AUI Receiver

The AUI receiver uses high-speed differential comparator to preserve the edges and duty cycle of the incoming data. A threshold detector and squelch circuit are used to qualify valid data from noise. During idle, the AUI is in a high noise rejection squelch state. When the first negative edge crosses the threshold of the threshold detector, the AUI enters into unsquelch state and begins receiving data. The AUI reverts back to squelch state by a normal Start-Of-Idle (SOI) signal or a missing SOI signal. A missing SOI signal is assumed when no transitions have occured on the receiver inputs for 175 ns. In this case, an SOI signal is generated and appended to the received data.

7.2.3 Termination and Isolation

The AUI cable is specified by the standard to have characteristic impedance of 78 ohms. For minimal reflection, the AUI cable has to be terminated with a 78 ohm resistance at the far end. A 0.1 µF capacitor connected to the mid value point of the termination resistor helps to bypass common mode noise picked up by the AUI cable. This capacitor is optional for on-board transceiver because there will be minimum common mode noise.

The SSI 78Q8373 AUI supports both transformer coupling as well as capacitive coupling as shown in the figure. Please note that for capacitive coupling, the termination resistors have to reside at the inputs of the SSI 78Q8373 AUI receivers.

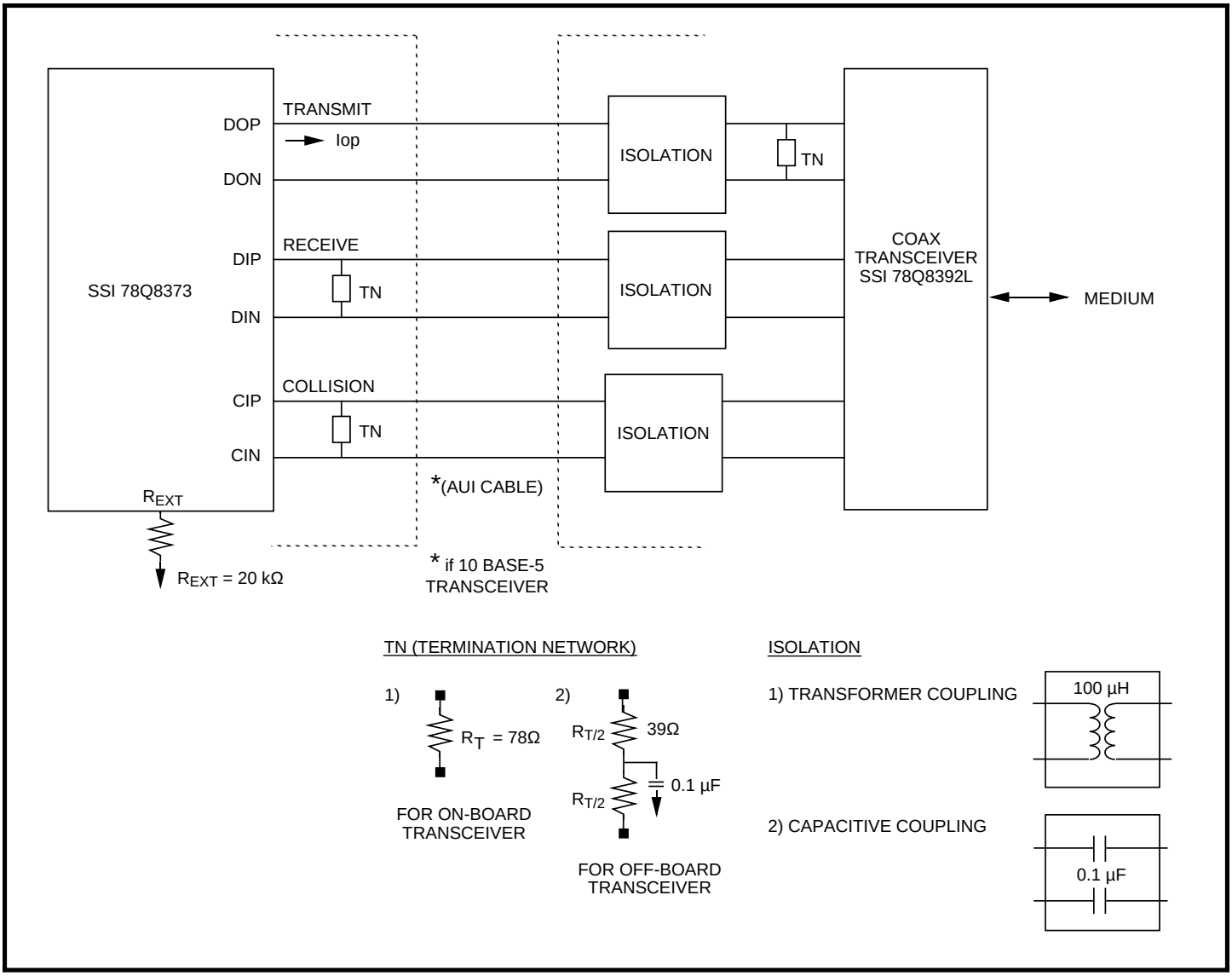

Figure 7.2. Attachment Unit Interface (AUI) Connections

Using the 78Q8373 on the Network

Section 8

8 USING THE SSI 78Q8373 ON THE NETWORK

This section deals with the transmission of data using the SSI 78Q8373 from the host point of view. It will cover the interaction of register configurations and the actual transmission executed. For more detailed information on the function of the Data Link Controller in this respect (with regards to Inter-Frame Gap, fairness and equality of the line, Jam Pattern, Backoff Algorithm etc.), please refer to the Transmitter Circuits Section.

8.1 INITIALIZATION

Initialization begins with a hardware reset immediately after power on. A pulse with a minimum of 200 nanosecond duration is required to be applied to the RESET pin. This resets ICE's internal pointers and registers to their initial state. $\overline{\text{ENADLC}}$, DLCR6<7> = 1 acts as a software reset resetting all buffer memory pointers. The software reset does not change the contents of the status and control registers or the DLCR 0-7, IDR8-13, TDR14-15, HTR8-15 and BMR10-15 registers. Hardware reset sets the $\overline{\text{ENADLC}}$ bit high.

The initialization of the 8373 by the host include the loading of the Ethernet Address of the node into IDR8-13 with IDR8 as the least significant byte of the address and group addressing in the Hash Table registers (if desired). To access the Node ID registers, (or any of the other bank of registers) the following is executed. Please note that all register values are in hexadecimal notation unless otherwise stated.

a) Disable the DLC by setting DLCR6<7> = 1

b) Select the register bank by setting DLCR7<3:2> as required.

DLCR7<3:2> = 00 (default setting after hardware)
DLCR7<3:2> = 01 (selects Hash Table registers)
DLCR7<3:2> = 10 (selects Buffer Memory registers)
DLCR7<3:2> = 11 (Reserved)

The host should load the Ethernet Address and Hash Table Configurations at this stage.

c) The default settings of DLCR0-7 after a hardware reset or power on are as follows:

DLCR0 = 00 (Transmit Status)
DLCR1 = 00 (Receive Status)
DLCR2 = 00 (Transmit Interrupt Mask)
DLCR3 = 00 (Receive Interrupt Mask)
DLCR4 = 06 (Transmit Mode)
DLCR5 = 41 (Receive Mode)
DLCR6 = B6 (Configuration Register 1)
DLCR7 = 20 (Configuration Register 2)

The host can now select the type of interrupt enables that should be activated in DLCR2-3. Unless a loop back mode is required in a testing environment, DLCR4 need not be changed.

d) The default setting of DLCR5 allows the reception of normal packets i.e. packets that meet the IEEE requirements and does not contain any errors. The host can enable the 'remote reset' capability of SSI 78Q8373 or enable the reception of 'bad packets' with the activation of appropriate bits in this register. The Address Mode bits can be reprogrammed for hash table acceptance if necessary. Please refer to the Data Link Controller Registers Section for details.

e) DLCR6 configures the size of the transmit buffer and overall buffer size. This should be changed according to the host's requirements. DLCR6<7> is reset to 0 for transmission and reception activities and set to 1 for access to the Node ID and Hash Table Register Banks.

f) DLCR7 configures the access to the 3 register banks. To access the Node ID and Hash Table Register Banks, DLCR6<7> = 1 must be set to 1. DLCR7<0> sets the big endian and little endian byte ordering depending on the host's configuration.

g) BMR11 denotes the action to be taken by SSI 78Q8373 should a 16 collision happen on the network. This should be programmed accordingly before transmission or the default setting will be used.

8.2 PACKET TRANSMISSION USING THE SSI 78Q8373

8.2.1 Transmission Without Contention

Before initiating a transmission, the host will load in the data packet(s) into the transmit buffer via BMR8 (and BMR9 if in word mode). Each data packet will contain a 2-byte header of the total packet length, destination and source addresses and the data to be transmitted. The host initiates transmission by writing the number of packets into BMR10 and setting TXST bit = 1 (BMR10<7>).

The 2-byte header is loaded into a counter within the transmit circuit. The counter will decrement its value as each byte is transmitted to the medium. When it reaches zero, this signifies that an entire data packet has been transmitted. At the same time, the packet count value (PACKET CNT<6:0>) in BMR10 will decrement by 1 each time a data packet is transmitted. When packet count is zero, this indicates that there are no more packets in the transmit buffer. SSI 78Q8373 will enter its idle state and wait for the TXST bit to be set high again and the process is repeated.

SSI 78Q8373 will wait for a 'free' medium before transmitting to the network. When the network is free, SSI 78Q8373 will generate and append the preamble and start frame delimiter to the beginning of the packet (the 2-byte header is stripped off and not transmitted) and generate the CRC for the packet. The entire packet starting from the preamble to the CRC is encoded by the ENDEC to Manchester Encoding and output to the external transceiver via the TDN and TDP pins.

The HWR_ERR bit (DLCR0<0>) indicates a host write error if it is a 1. This means that the transmit bank is full and has insufficient buffer space for the next packet that the host is writing. When this happens, the host will have to initiate a TXST to start transmission hence clearing the transmit bank. In the case of a single transmit bank, the host will have to wait until this bank is cleared before writing another packet into the transmit buffer. SSI 78Q8373 can also be configured into two transmit banks. In this case, when the first bank is being transmitted (by initiating TXST), the host can continue writing to the second transmit bank. Similarly, when the second transmit bank is being transmitted (by initiating another TXST), the host can write to the first bank that had been cleared. It should be noted that the TXST can be initiated whenever the host wishes to transmit (even when the transmit banks are not full).

8.2.2 Collision and Recovery

While transmitting, SSI 78Q8373 monitors the network for collisions. In the event of a collision, the collision counter in DLCR4<7:4> is incremented and the transmission terminated. The COL bit (DLCR0<2>) will be set to indicate that at least one collision has occurred during the transmission of that packet. After the random interval deferment, SSI 78Q8373 will attempt to re-transmit the collided packet and all other packets in the transmit buffer until the PACKET CNT in BMR10<6:0> reaches zero. In the event of 16 collisions, SSI 78Q8373 will take appropriate action according to the 16 collision control register set in BMR11. There are four different actions for SSI 78Q8373 to choose when a packet has attempted 16 re-transmissions. The actions and bit settings are shown in the register section for BMR11. The 16COL bit (DLCR0<1>) will be set when 16 attempts was reached. Otherwise if SSI 78Q8373 successfully transmits all the packets in the transmit buffer, the TXOK (DLCR0<7>) bit will be set to signal a transmission completion and the collision counter will be reset to zero.

8.2.3 How the SSI 78Q8373 Handles Other Situations

Whether the buffer memory setup is in a word or byte mode, SSI 78Q8373 will always access the buffer memory in byte format and convert it into a serial bit stream before transmitting to the network. In the situation where a packet is of odd byte length for a word mode system, SSI 78Q8373 will transmit this packet properly and perform an even byte alignment. This will ensure that the new packet will always start at the even address location.

In reference to the DLCR7<0> bit for the INTEL or MOTOROLA format, the data order swapping only applies to the host that is configured in word format. DLCR7<0> set to 0 refers to the INTEL format and DLCR7<0> = 1 refers to the MOTOROLA format. In the INTEL format, the least significant byte is transmitted first then followed by the most significant byte. In the MOTOROLA format, the data order is reversed. Note that all the data stored in the buffer memory is affected, including the non-transmitted 2-byte headers for the length of the data packet. Only BMR8 and BMR9 are affected by this control bit.

The following tables describe the ordering of the packets depending on which format the host is configured. SSI 78Q8373 defaults to the INTEL format upon power up.

TRANSMIT PACKET:

INTEL FORMAT	
HIGH BYTE	LOW BYTE
TX MSB length	TX LSB length
Destination address 2nd byte	Destination address 1st byte
Source address 2nd byte	Source address 1st byte
Length field LSB	Length field MSB
Data field 2nd byte	Data field 1st byte

MOTOROLA FORMAT	
HIGH BYTE	LOW BYTE
TX LSB length	TX MSB length
Destination address 1st byte	Destination address 2nd byte
Source address 1st byte	Source address 2nd byte
Length field MSB	Length field LSB
Data field 1st byte	Data field 2nd byte

RECEIVE PACKET:

INTEL FORMAT	
HIGH BYTE	LOW BYTE
Reserved	Packet status
Data length high byte	Data length low byte
Destination address 2nd byte	Destination address 1st byte
Source address 2nd byte	Source address 1st byte
Length field LSB	Length field MSB
Data field 2nd byte	Data field 1st byte

MOTOROLA FORMAT	
HIGH BYTE	LOW BYTE
Packet status	Reserved
Data length low byte	Data length high byte
Destination address 1st byte	Destination address 2nd byte
Source address 1st byte	Source address 2nd byte
Length field MSB	Length field LSB
Data field 1st byte	Data field 2nd byte

8.3 PACKET RECEPTION USING THE SSI 78Q8373

8.3.1 Reception Without Contention

When not transmitting, SSI 78Q8373 will consistently monitor the network. To determine if a packet on the network is for the node, SSI 78Q8373 will check the destination address of the packet. Depending on the Address Modes (DLCR5<1:0>) of the node (set during initialization), SSI 78Q8373 will accept the packet if the destination address meets the criteria.

Upon a successful reception, the received packet is stored in the receive buffer. An internal counter in SSI 78Q8373 keeps track of the length of the packet. SSI 78Q8373 allocates 4 bytes in the receive buffer before storing the accepted packet in the receive buffer. This is for a 4-byte header of the accepted packet to the host (refer to Receive Buffer Data Format Section). The 4-byte header contains the packet length and the status (CRC error, alignment error etc.) of the packet. At the end of the packet reception, SSI 78Q8373 writes the status of the accepted packet in the allocated space. By default, if a packet contains any errors, it will be discarded and the receive buffer pointers will be restored automatically.

When a packet is accepted, the PKT_RDY (DLCR1<7>) bit is set and the RX_BUFMTY (DLCR5<6>) bit is cleared to indicate to the host that there is a packet in the Receive Buffer. The host will then proceed to read the packet from the buffer memory. When all the data packets in the receive buffer are read, the RX_BUFMTY (DLCR5<6>) is set to '1' again. An OVRFLO, DLCR1<0> error occurs when the receive buffer is full or has insufficient space for the next accepted packet. This will result in the rejection of the packet and the host would have to read the receive buffer to free some buffer space. Due to the ring structure of the receive buffer, once the host has read some packets, that buffer space becomes available for the future packets.

After accepting a packet, the receiver will perform an 8-byte alignment in the receive buffer. An 8-byte alignment means that the start address of the next packet will always begin at the 8-byte boundary (for example at address locations: 0000H, 0008H, 0010H....etc.). The execution of 8 byte alignment must be consistent between the receiver and the host read circuit. In the host read circuit, there is a counter that loads the packet length value from the 4-byte header of the receive packet (3rd and 4th bytes of the 4-byte header). In a byte configuration, the counter will decrement each time a byte has been read out by the host. When the counter reaches zero, this signifies that the entire packet has been read by the host. The host can continue to read the next packet if no other resource requires the attention of SSI 78Q8373.

8.3.2 Collision and Recovery

In the event of a collision, the receiver accepts the fragmented bits of the collision and decodes it just like a valid frame. A CRC check would inform the host that the received packet has CRC errors by setting the CRC_ERR (DLCR1<1>) to a 1. The host will then discard this packet and the receive buffer memory pointers will be adjusted accordingly for the reception of the next packet.

8.3.3 How the SSI 78Q8373 Handles Other Situations

When the host is configured as word mode, there will be a situation whereby there are packets in the receive buffer are of odd byte length. The host should discard the excess byte of the last word. SSI 78Q8373 maintains an internal counter and re-aligns accordingly.

SSI 78Q8373 has the capability of accepting packets with errors or perform an extra group addressing mode depending on the bits set in the Receive Mode Register, DLCR5. The effects on packet reception with reference to each specific bit is elaborated below.

If ACPT_BADPKT (DLCR5<5>) is activated, SSI 78Q8373 will accept short packets or packets with alignment and/or CRC errors. These errors may be due to network corruption or packet collision. In this case, the corresponding bits are not set when the packet is accepted. However, the status byte to the host in the receive buffer will continue to indicate these errors as they occur.

SSI 78Q8373 may be programmed to accept packets with a minimum length of 6 bytes to a maximum of 2047 bytes (excluding CRC bits). If ENA_SRTPKT is set to a 1, packets that are less than 60 bytes in length (from destination address to end of data field) will

be accepted by SSI 78Q8373. The SRT_ERR bit (DLCR1<3>) will not be set when the packet is accepted in this case. Similar to the case of ACPT_BADPKT, the status byte to the host will continue to indicate the error. If ENA_SRTPKT is set to 0, SSI 78Q8373 will reject this packet setting SRT_ERR bit (DLCR1<3>) to 1 to indicate the error. It should be noted that SSI 78Q8373 does not check for long packet errors (greater than the IEEE maximum length) and has no error flags for such packets .

The ADD_SIZE bit (DLCR5<4>) allows the multiplexing of the last byte of the destination address. When activated, it configures SSI 78Q8373 to match only 5 bytes of the destination address before deciding to accept the incoming packet.

The ENA_RMTRST bit (DLCR5<2>) enables other nodes on the network to remotely reset an external peripheral connected to this node. This is achieved by sending a packet to this node (using individual/physical addressing only)with a Type Field containing the 0900H pattern. The least significant bit (LSB) of the most significant byte (MSBYTE) of Type Field is transmitted first. Thus the 0900H pattern (09H is the most significant byte) would be transmitted as follows from left to right:

1001 0000 0000 0000

8.3.4 Status Byte Format

The status byte to the host has several bits that flag error messages or report the status of the accepted packet. It should be noted that these error and status bits do not reflect the settings of the corresponding register bits in DLCR0 and DLCR1. This is outlined below.

The format of the status byte is as follows:

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	0	*PACKET OK*	*REMOTE RESET*	*SHORT ERROR*	*ALIGN ERROR*	*CRC ERROR*	*OVRFLO*

Bit 7 and 6 are not used and always set at '0.' The settings of the status bits: 5, 3, 2 and 1 depend very much on the settings of ACPT_BADPKT (DLCR5<5>) and ENA_SRTPKT (DLCR5<3>). When ACPT_BADPKT is set to a 1, a packet that has any errors (such as short packet, alignment or CRC errors), will set the respective status bits (*SHORT ERROR, ALIGN ERROR, CRC ERROR)* to a 1 and the *PACKET OK* (bit 5) to a 0. The value in DLCR1 will not indicate any errors and DLCR1<7> is set to 1. Hence, the status byte of the RAM is not a mirror image of DLCR1. Similarly, this applies when ENA_SRTPKT (DLCR5<3>) is set to enable SSI 78Q8373 to accept short packets.

As for the *OVRFLO* bit, it will be set under the following conditions. When the receive buffer memory is too small to accommodate any in-coming packet, then DLCR1<0> will be set (but not bit0 of the status byte as the packet has already rejected). Later, if a subsequent packet is successfully loaded into the receive buffer memory then the *OVRFLO* bit in the status byte will be set (but not DLCR1<0>). This is to indicate to the host that one or more packets have been reject by the receiver due to memory overflow problems.

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Glossary

A

ACK - "Acknowledge" character. A transmission control character transmitted by a station as an affirmative response to the station with which a connection has been set up. An acknowledge character may also be used as an accuracy control character.

ACOUSTIC COUPLER - A type of low-speed modem interface frequently used with portable terminals. It sends and receives data using a conventional telephone handset and does not require an electrical connection to the line.

ADAPTIVE DIFFERENTIAL PULSE CODE MODULATION (ADPCM) - An encoding technique, standardized by the CCITT, that allows an analog voice conversation to be carried within a 32K bps digital channel. Three or four bits are used to describe each sample, which represents the difference between two adjacent samples. Sampling is done 8,000 times per second.

ALGORITHM - A prescribed set of well-defined rules for the solution of a problem in a finite number of steps, e.g., A full statement of an arithmetic procedure for evaluating sine x to a stated precision.

AMPLITUDE - Magnitude or size. In waveforms or signals occurring in a data transmission, a complete definition of the waveform can be made if the voltage level is known at all times. In this case, the voltage level is called the amplitude.

AMPLITUDE MODULATION - Method of modifying the amplitude of a sine wave signal in order to encode information.

ANALOG LOOPBACK - A technique used for testing transmission equipment that isolates faults to the analog signal receiving or transmitting circuitry. Basically, where a device, such as a modem, echoes back a received (test) signal that is then compared with the original signal.

ANALOG SIGNAL - Signal in the form of a continuously varying physical quantity such as voltage, which reflects variations in some quantity.

ANSI - American National Standards Institute. A highly active group affiliated with the International Standards Organization (ISO) that prepares and establishes standards for transmission codes (e.g., ASCII), protocols (e.g., ADCCP), media (tape and diskette), and high level languages (e.g., Fortran and Cobol), among other things.

ANSWERBACK - A reply message from a terminal that verifies that the correct terminal has been reached and that it is operational.

APPLICATION LAYER - The top of the seven-layer OSI model, generally regarded as offering an interface to, and largely defined by, the network user; in IBM's SNA, the end-user layer.

ASCII - American Standard Code for Information Interchange. A 7-bit binary code that defines 128 standard characters for use in data communications.

ASYNCHRONOUS - Occurring without a regular or predictable time relationship to a specified event, e.g., The transmission of characters one at a time as they are keyed. Contrast with synchronous.

ASYNCHRONOUS TRANSMISSION - Transmission in which each information character, or sometimes each word or small block, is individually synchronized, usually by the use of start and stop elements. Also called start-stop or character asynchronous transmission.

ATM (Asynchronous Transfer Mode) - A high bandwidth, low-delay, packet-like switching and multiplexing technology. Selected by ITU as the basis of future broadband network.

ATM FORUM - An industry organization with some 450 members, focused on speeding the developement, standardization and deployment of ATM products.

ATTENUATION - A decrease in the power of a current, voltage, or power of a received signal in transmission between points because of loss through lines, equipment or other transmission devices. Usually measured in decibels.

AUI - Attachment unit interface. The electrical interface between the traditional line electronics (transceiver) and the DTE components (ENDEC & MAC).

AUTO-ANSWER - Automatic answering; the capability of a terminal, modem, computer, or a similar device to respond to an incoming call on a dial-up telephone line, and to establish a data connection with a remote device without operator intervention.

AUTOBAUD - The generally used term for automatically detecting the bit rate of a start/stop (character asynchronous) communication format by measuring the length of the start bit of the first character transmitted. Some modems extend this to additionally determine the parity in use by stipulating that the first two characters from the DTE should be "AT." The word autobaud comes from a popular misuse of baud rate to mean the same as bit rate.

AUTODIAL - Automatic dialing; the capability of a terminal, modem, computer, or a similar device to place a call over the switched telephone network, and establish a connection without operator intervention.

AUTOMATIC DIALER, OR AUTODIALER - Device which allows the user to dial preprogrammed numbers simply by pushing a single button.

B

BANDPASS FILTER - A circuit designed to allow a single band of frequencies to pass; neither of the cut-off frequencies can be zero or infinite.

BANDWIDTH - 1) The range of frequencies that can pass over a given circuit. The bandwidth determines the rate at which information can be transmitted through the circuit. The greater the bandwidth, the more information that can be sent through the circuit in a given amount of time. 2) Difference, expressed in hertz (Hz), between the highest and lowest frequencies of a transmission channel.

10Base-T - Ethernet on unshielded twisted pair.

10Base-2 - Ethernet on thin coax.

10Base-5 - Ethernet on thick coax.

BASEBAND - Pertaining or referring to a signal in its original form and not changed by modulation. A baseband signal can be analog or digital.

BASEBAND SIGNALING - Transmission of a digital or analog signal at its original frequencies, i.e., a signal in its original form, not changed by modulation; can be an analog or digital signal.

BAUD - A measure of data rate, often misused to denote bits per second. A baud is equal to the number of discrete conditions or signal events per second. There is disagreement over the appropriate use of this word, since at speeds above 2400 bit/s, the baud rate does not always equal the data rate in bits per second.

BELLCORE - Bell Communications Research; organization established by the AT&T divestiture, representing and funded by the BOCs and RBOCs, for the purposes of establishing telephone network standards and interfaces; includes much of former Bell Labs.

BERT - Bit Error Rate Test. A test conducted by transmitting a known, pattern of bits (commonly 63, 511, or 2047 bits in length), comparing the pattern received with the pattern transmitted, and counting the number of bits received in error. Also see bit error rate. Contrast with BLERT.

BINARY CODE - Representation of quantities expressed in the base-2 number system.

BINARY SYNCHRONOUS COMMUNICATIONS - A half-duplex, character-oriented data communications protocol originated by IBM in 1964. It includes control characters and procedures for controlling the establishment of a valid connection and the transfer of data. Also called bisync and BSC. Although still enjoying widespread usage, it is being replaced by IBM's more efficient protocol, SDLC.

BIPOLAR - 1) The predominant signaling method used for digital transmission services, such as DDS and T1, in which the signal carrying the binary value successfully alternates between positive and negative polarities. Zero and one values are represented by the signal amplitude at either polarity, while no-value "spaces" are at zero amplitude. 2) A type of integrated circuit (IC or semiconductor) that uses NPN, PNP, and junction FET's as the primary active devices, as opposed to CMOS, which uses MOS FET's. See Alternate Mark Inversion.

BISDN - Broadband integrated services digital network.

BIT - The smallest unit of information used in data processing. It is a contraction of the words "binary digit."

BIT ERROR RATE (BER) - In data communications testing, the ratio between the total number of bits transmitted in a given message and the number of bits in that message received in error; a measure of the quality of a data transmission.

BITS PER SECOND (BIT/S) - Basic unit of measure for serial data transmission capacity; Kbit/s, or kilobits, for thousands of bits per second; Mbit/s, or megabit/s, for millions of bits per second, etc.

BOC - Bell Operating Company. One of 22 local telephone companies spun off from AT&T as a result of divestiture. The 22 operating companies are divided into seven regions and are held by seven RBHCs (Regional Bell Holding Company).

BROADBAND - Referring or pertaining to an analog circuit that provides more bandwidth than a voice grade telephone line, i.e., a circuit that operates at a frequency of 20 kHz or greater. Broadband channels are used for high-speed voice and data communications, radio and television broadcasting, some local area data networks, and many other services. Also called wideband.

BUFFER - A storage medium or device used for holding one or more blocks of data to compensate for a difference in rate of data flow, or time of occurrence of events, when transmitting data from one device to another.

BUS - 1) Physical transmission path or channel. Typically an electrical connection, with one or more conductors, wherein all attached devices receive all transmissions at the same time. Local network topology, such as used in Ethernet and the token bus, where all network nodes listen to all transmissions, selecting certain ones based on address identification. Involves some type of contention-control mechanism for accessing the bus transmission medium. In data communications, a network topology in which stations are arranged along a linear medium (e.g., a length of cable). 2) In computer architecture, a path over which information travels internally among various components of a system.

BYTE - Group of bits handled as a logical unit; usually 8.

C

CABLE - Assembly of one or more conductors within a protective sheath; constructed to allow the use of conductors separately or in groups.

CALL PROGRESS DETECTION (CPD) - A technique for monitoring the connection status during initiation of a telephone call by detecting presence and/or duty cycle of call progress signaling tones such as dial-tone or busy signals commonly used in the telephone network.

CALL PROGRESS TONES - Audible signals returned to the station user by the switching equipment to indicate the status of a call; dial tones and busy signals are common examples.

CAP MODEM - Carrierless amplitude phase modem.

CCITT - Comite Consultatif International de Telephonie et de Telegraphie. Telegraph and Telephone Consultive Committee. An advisory committee to the International Telecommunications Union (ITU) whose recommendations covering telephony and telegraphy have international influence among telecommunications engineers, manufacturers, and administrators.

CDPD - Cellular digital packet data 19.2 Kbit/s wireless modem.

CENTRAL OFFICE (CO) - See Exchange

CHANNEL BANK - Equipment typically used in a telephone central office that performs multiplexing of lower speed, digital channels into a higher speed composite channel. The channel bank also detects and transmits signaling information for each channel, and transmits framing information so that time slots allocated to each channel can be identified by the receiver.

CHANNEL SERVICE UNIT (CSU) - A component of customer premises equipment (CPE) used to terminate a digital circuit, such as DDS or T1 at the customer site; performs certain line-conditioning functions, ensures network compliance per FCC rules and responds to loopback commands from central office; also, ensures proper ones density in transmitted bit stream and performs bipolar violation correction.

CHANNEL, VOICE GRADE - Channel suitable for transmission of speech, analog data, or facsimile, generally with a frequency range of about 300 to 3000 Hz.

CHARACTER - Letter, figure, number, punctuation, or other symbol contained in the message. In data communication, common characters are defined by 7- or 8-bit binary codes, such as ASCII.

CHIP - A commonly used term which refers to an integrated ciruit.

CIRCUIT, TWO-WIRE - A circuit formed by two conductors insulated from each other that can be used as either a one-way or two-way transmission path.

CLOCK - In logic or transmission, repetitive, precisely timed signal used to control a synchronous process.

CMOS - Complementary Metal-Oxide Semiconductor. A type of transistor, typicallly used in low-power integrated circuits.

COAXIAL CABLE - Cable consisting of an outer conductor surrounding an inner conductor, with a layer of insulating material in between. Such cable can carry a much higher bandwidth than a wire pair.

CPE - Customer Premises Equipment

CROSSPOINT - 1) Switching array element in an exchange that can be mechanical or electronic. 2) Two-state semiconductor switching device having a low transmission system impedance in one state and a very high one in the other.

CROSSTALK - Interference or an unwanted signal from one transmission circuit detected on another, usually an adjacent circuit.

CYCLIC REDUNDANCY CHECK (CRC) - A powerful error detection technique. Using a polynomial, a series of two 8-bit block check characters are generated that represent the entire block of data. The block check characters are incorporated into the transmission frame, then checked at the receiving end.

D

DATA COMMUNICATIONS EQUIPMENT (DCE) - Equipment that performs the functions required to connect data terminal equipment (DTE) to the data circuit. In a communications link, equipment that is either part of the network, an access-point to the network, a network node, or equipment at which a network circuit terminates; in the case of an RS-232C connection, the modem is usually regarded as DCE, while the user device is DTE, or data terminal equipment; in a CCITT X.25 connection, the network access and packet-switching node is viewed as the DCE.

DATA LINK - Any serial data communications transmission path, generally between two adjacent nodes or devices and without any intermediate switching nodes.

DATA SET - A synonym for modem used by AT&T and a few other vendors.

DATA SERVICE UNIT (DSU) - A device that replaces a modem on a Digital Data Service (DDS) line. The data service unit regenerates the digital signals for transmission over digital facilities.

DATA TERMINAL EQUIPMENT (DTE) - Equipment which is attached to a network to send or receive data, generally end-user devices, such as terminals and computers, that connect to DCE, which either generate or receive the data carried by the network; in RS-232C connections, designation as either DTE or DCE determines signaling role in handshaking; in a CCITT X.25 interface, the device or equipment that manages the interface at the user premises; see DCE.

dB - Decibel; unit for measuring relative strength of a signal parameter such as power, voltage, etc. The number of decibels is ten times the logarithm (base 10) of the ratio of the power of two signals, or ratio of the power of one signal to a reference level.

dBm - Decibels relative to one milliwatt.

DDS - 1) Digital Data Service. A digital transmission service supporting speeds up to 56 Kbit/s. 2) Dataphone Digital Service. An AT&T leased line service offering digital transmission at speeds ranging from 2400 to 56 Kbit/s.

DECT - Digital European cordless telephone.

DJCT - Digital Japanese cordless telephone.

DELAY DISTORTION - The change in a signal from the transmitting end to the receiving end resulting from the tendency of some frequency components within a channel to take longer to be propagated than others.

DIAL-UP - The process of, or the equipment or facilities involved in, establishing a temporary connection via the switched telephone network.

DIAL TONE (DT) - Signal sent to an operator or subscriber indicating that the switch is ready to receive dial pulses.

DIGITAL - Referring to communications procedures, techniques, and equipment whereby information is encoded as either binary “1” or “0”; the representation of information in discrete binary form, discontinuous in time, as opposed to the analog representation of information in variable, but continuous, waveforms.

DIGITAL LOOPBACK - A technique for testing the digital processing circuitry of a communications device. It may be initiated locally, or remotely via a telecommunications circuit. The device being tested will echo back a received test message, after first decoding and then re-encoding it, the results of which are compared with the original message.

DIGITAL SIGNAL - Discrete or discontinuous signal; one whose various states are discrete intervals apart.

DIP - Dual-In-Line Package. Method of packaging electronic components for mounting on printed circuit boards.

DISTORTION - The modification of the waveform or shape of a signal caused by outside interference or by imperfections of the transmission system. Most forms of distortion are the result of the characteristics of the transmission system to the different frequency components.

DOTTING, DOUBLE DOTTING, PATTERN - The term "dotting" was coined by Bell to describe a data pattern consisting of alternate marks and spaces. The CCITT uses the full description of "alternating binary ones and zeros" on first needing this idea in a recommendation, but then abbreviate this to "reversals." By extrapolation, "double dotting" has come into use to refer to the data pattern termed "S1" which is used in V.22bis to indicate 2400 bit/s capability. The full description is "unscrambled double dibit 00 and 11 at 1200 bit/s for 100 $\pm$ 3 ms."

DS-1 - Digital Signal level 1; telephony term describing a digital transmission format in which 24 voice channels are multiplexed into one 1.544 Mbit/s (U.S.) T1 digital channel.

DS-3 - Digital Signal level 3; telephony term describing the 44.736 Mbit/s digital signal carried on a T3 facility.

DSP RTOS - Digital signal processing real time operating system.

DTMF - Dualtone Multifrequency (DTMF) - Basis for operation of most push button telephone sets. An in-band signalling technique in which a matrix combination of two frequencies, each from a group of four, are used to transmit numerical address information; it encodes 16 possible combinations of tone pairs using two groups of four tones each. The two groups of four frequencies are 697 Hz, 770 Hz, 852 Hz, and 941 Hz, and 1209 Hz, 1336 Hz, 1477 Hz, and 1633 Hz. DTMF is used primary for call initiation in GSTN telephone applications.

E

ECHO - The distortion created when a transmitted signal is reflected back to the originating station.

ECHO CANCELLER - A devise used to reduce or eliminate echo. It operates by placing a signal that is equal and opposite to the echo signal on the return transmission path.

ECHO SUPPRESSOR - A mechanism used to suppress echoes on long-distance analog connections. The device suppresses the transmission path opposite in direction to the one being used. This feature, although necessary for voice transmission, often interferes with data transmission.

EIA - Electronic Industries Association

EIA INTERFACE, EIA232D, RS 232C - The logical, electrical and physical characteristics of the connection between a DTE and a modem is set out in EIA specification 232D. Previously this has been known as RS232C. The logical characteristics are essentially similar to those specified in CCITT recommendation V.24 and the electrical characteristics to those in V.28.

ELECTROMAGNETIC INTERFERENCE (EMI) - Radiation leakage outside a transmission medium that results mainly from the use of high-frequency wave energy and signal modulation. EMI can be reduced by appropriate shielding.

EMI - See Electromagnetic Interference.

ENDEC - Encoder/Decoder. The 10 Mbit/s Manchester encoder and decoder circuit for Ethernet signalling.

ENVELOPE DELAY - An analog line impairment involving a variation of signal delay with frequency across the data channel bandwidth.

EQUALIZATION - The introduction of components to an analog circuit by a modem to compensate for the attenuation (signal loss) variation and delay distortion with frequency (attenuation equalization) and propagation time variations with frequency (delay equalization). Generally, the higher the transmission rate, the greater the need for equalization.

ERROR - In data communications, any unwanted change in the original contents of a transmission.

ERROR BURST - A concentration of errors within a short period of time as compared with the average incidence of errors. Retransmission is the normal correction procedure in the event of an error burst.

ERROR CONTROL - A process of handling errors, which includes the detection and in some cases, the correction of errors.

ETHERNET - A media-access specification for local area networks, developed by IEEE and known as the IEEE 802.3 spec.

EXCHANGE - Assembly of equipment in a communications system that controls the connection of incoming and outgoing lines, and includes the necessary signaling and supervisory functions. Different exchanges, or switches, can be costed to perform different functions, e.g., Local exchange, trunk exchange, etc. See Class of Exchange. Also known as Central Office (U.S. Term).

EXCHANGE, PRIVATE AUTOMATIC BRANCH (PABX) - Private automatic telephone exchange that provides for the switching of calls internally and to and from the public telephone network.

EXCHANGE, PRIVATE BRANCH (PBX) - Private, manually operated telephone exchange that provides private telephone service to an organization and that allows calls to be transmitted to or from the public telephone network.

EXCHANGE AREA - Area containing subscribers served by a local exchange.

F

FILTER - Circuit designed to transmit signals of frequencies within one or more frequency bands and to attenuate signals of other frequencies.

FIRMWARE - Permanent or semi-permanent control coding implemented at a micro-instruction level for an application program, instruction set, operating routine, or similar user-oriented function.

FLOW CONTROL - The use of buffering and other mechanisms, such as controls that turn a device on and off, to prevent data loss during transmission.

FOUR-WIRE CIRCUIT OR CHANNEL - A circuit containing two pairs of wire (or their logical equivalent) for simultaneous (i.e., full-duplex) two-way transmission. Contrast with two-wire channel.

FRAME - 1) A group of bits sent serially over a communications channel; generally a logical transmission unit sent between data-link-layer entities that contain its own control information for addressing and error checking. 2) A piece of equipment in a common carrier office where physical cross connections are made between circuits.

FRAMING - Control procedure used with multiplexed digital channels such as T1 carriers, whereby bits are inserted so the receiver can identify the time slots allocated to each subchannel. Framing bits can also carry alarm signals indicating specific alarm conditions.

FREQUENCY - Rate at which an event occurs, measured in hertz, kilohertz, megahertz, etc.

FREQUENCY BANDS - Frequency bands are defined arbitrarily as follows:

Range (MHz)	Name
0.03-0.3	Low frequency (LF)
0.3-3.0	Medium frequency (MF)
3-30	High frequency (HF)
30-300	Very High frequency (VHF)
300-3000	Ultra high frequency (UHF)
3000-30,000	Super high frequency (SHF) (micro wave)
30,000-300,000	Extremely high frequency (EHF)(millimeterwave)

FSK - Frequency Shift Keying. A method of modulation that uses two different frequencies, usually phase continous, to distinguish between a mark (digital 1) and a space (digital 0) when transmitting on an analog line. Used in modems operating at 1200 bit/s or slower.

FULL-DUPLEX - Pertaining to the capability to send and receive simultaneously.

G

GAIN - Denotes an increase in signal power in transmission from one point to another, usually expressed in dB.

GUARD TONE - In CCITT recommendations V.22 and V.22bis, guard tones may optionally be transmitted along with the data signal from the answering modem. A single frequency of either 1800 or 550 Hz is used and the data signal power must be reduced to keep the overall energy level the same as for transmission without guard tone. The purpose of the guard tone is to prevent the high-band data signal from interfering with the operation of billing apparatus in certain countries.

GSTN - General Switched Telephone Network

H

HALF-DUPLEX - Pertaining to the capability to send and receive but not simultaneously.

HANDSHAKE - An exchange of control sequences between two locations to set up the correct parameters for transmission.

HDLC - High-level Data Link Control. Bit-oriented communication protocol developed by the ISO (International Standards Organization).

HARMONIC DISTORTION - A waveform distortion, usually caused by the nonlinear frequency response of a transmission.

HERTZ (Hz) - A measure of electromagnetic frequency; one hertz is equal to one cycle per second.

HF - High Frequency.

HIGH FREQUENCY (HF) - Portion of the electromagnetic spectrum, typically used in short-wave radio applications. Frequencies in the 3 to 30 MHz range.

Hz - See Hertz.

I

IEEE - Institute of Electrical and Electronics Engineers.

IEEE 802.11 - Wireless local area network IEEE standard.

INITIALIZE - To set counters, switches, addresses, or contents of storage to zero or other starting values at the beginning of, or at prescribed points in, the operation of a computer routine.

INTERFACE - A hardware and/or software link between two devices. The interface defines all signal characteristics and other specifications for physical interconnection of the devices.

INTEROFFICE TRUNK - Direct trunk between local central offices (Class 5 offices), or between Class 2, 3, or 4 offices; also called intertoll trunk.

IS54 - Interim standard 54 - half analog/digital, second-generation North American standard.
ISO - International Organization for Standardization.

ITU - International Telecommunications Union. The parent organization of the CCITT.

J

JITTER - Slight movement of a transmission signal in time or phase that can introduce errors and loss of synchronization for high-speed synchronous communications. See Phase jitter.

K

KEY PULSING (KP) - Manual method of sending numerical and other signals by the operation of nonlocking pushkeys. Also called Key Sending.

KEY SERVICE UNIT (KSU) - Main operating unit of a key telephone system.

KEY TELEPHONE SYSTEM (KTS) - When more than one telephone line per set is required, pushbutton or key telephone systems offer flexibility and a wide variety of uses, e.g., pickup of several exchange lines, PABX station lines, private lines, and intercommunicating lines. Features of the system include pickup and holding intercommunications, visual and audible signals, cutoff, exclusion, and signaling.

KP - Key Pulse (signaling unlocking signal). See Key Pulsing.

kHz - Kilohertz, kilocycles per second.

KTU - Key Telephone Unit. See Key Service Unit.

L

LEASED LINE - A line rented exclusively to one customer for voice or data communications; dedicated circuit, typically supplied by the telephone company or transmission authority, that permanently connects two or more user locations and is for the sole use of the subscriber. Such circuits are generally voice grade in capacity and in range of frequencies supported, are typically analog, are used for voice or data, can be point-to-point, or multipoint, and can be enhanced with line conditioning. Also called private line, tie line, or dedicated facility.

LED - Light-Emitting Diode.

LIGHT-EMITTING DIODE (LED) - Semiconductor junction diode that emits radiant energy and is used as a light source for fiber optic communications, particularly for short-haul links.

LIMITED-DISTANCE MODEM - A short-haul modem or line driver that operates over a limited distance. Some limited-distance modems operate at higher speeds than modems that are designed for use over analog telephone facilities, since line conditions can be better controlled.

LINE HIT - A transient disturbance causing a detectable error on a communications line.

LINE-LOADING - The process of installing loading coils in series with each conductor on a transmission line. Usually 88 milliHenry coils installed at 6,000 foot intervals.

LINK - 1) A physical circuit between two points. 2) A logical circuit between two users of a packet switched (or other) network permitting them to communicate (although different physical paths may be used).

LINK LAYER - The logical entity in the OSI model concerned with transmission of data between adjacent network nodes. It is the second layer processing in the OSI model, between the physical and the network layers.

LOADING COILS - An inductance coil installed at regular intervals along a transmission line. Used to improve the quality of voice grade circuits.

LOCAL EXCHANGE - Exchange in which subscribers' lines terminate. The exchange has access to other exchanges and to national trunk networks. Also called local central office, end office.

LOCAL LOOP - The part of a communications circuit between the subscriber's equipment and the equipment in the local exchange.

LOCAL TRUNK - Trunks between local exchanges.

LOSS (TRANSMISSION) - Decrease in energy of signal power in transmission along a circuit due to the resistance or impedance of the circuit or equipment.

M

MAC - Media access controller - a protocol controller IC that implements the 802.3 CSMA/CO protocol.

MARK - The signal (communications channel state) corresponding to a binary one. The marking condition exists when current flows (current-loop channel) or when the voltage is more negative than -3 volts (EIA RS-232 channel).

MATRIX - In switch technology, that portion of the switch architecture where input leads and output leads meet, any pair of which may be connected to establish a through circuit. Also called switching matrix.

MAU - Media attachment unit - a transceiver that connects to the AUI port on an Ethernet interface card.

Mbit/s - Megabits per second.

MEGAHERTZ (MHz) - A unit of frequency equal to one million cycles per second.

MF - 1) Medium Frequency. 2) Multifrequency. See Dualtone Multifrequency Signaling (DTMF).

MODEM - A contraction of modulate and demodulate; a conversion device installed in pairs at each end of an analog communications line. The modem at the transmitting end modulates digital signals received locally from a computer or terminal; the modem at the receiving end demodulates the incoming signal, converting it back to its original (i.e., digital) format, and passes it to the destination business machine.

MODULATION - The application of information onto a carrier signal by varying one or more of the signal's basic characteristics (frequency, amplitude, or phase); the conversion of a signal from its original (e.g., digital) format to analog format.

MODULATION, PULSE CODE (PCM) - Digital transmission technique that involves sampling of an analog information signal at regular time intervals and coding the measured amplitude value into a series of binary values, which are transmitted by modulation of a pulsed, or intermittent, carrier. A common method of speech digitizing using 8-bit code words, or samples, and a sampling rate of 8 kHz.

ms - Millisecond. One-thousandth of a second.

MULTIPLEXER - Device that enables more than one signal to be sent simultaneously over one physical channel.

MULTIPLEXING - Division of a transmission facility into two or more channels either by splitting the frequency band transmitted by the channel into narrower bands, each of which is used to constitute a distinct channel (frequency-division multiplex), or by allotting this common channel to several different information channels, one at a time (time-division multiplexing).

MUX - See Multiplexer.

N

NAK - "Negative acknowledge" character. A transmission control character that indicates a block of data was received incorrectly.

NOISE - Undesirable energy in a communications path, which interferes with the reception or processing of a signal.

ns - Nanosecond; also nsec. One-billionth of a second.

O

OFF HOOK - By analogy with the normal household telephone, a modem is off-hook when it is using the telephone line to make a call. This is similar to raising the telephone handset, or taking it off the hook. Going off-hook is also known as “seizing the line.”

ON-HOOK - By analogy with the normal household telephone, a modem is on-hook when it is not using the telephone line. As with a telephone where the handset is on the hook, the line may be used by other equipment to make a call. Going on-hook is also known as “dropping the line.”

OSI - Open Systems Interconnection. Referring to the reference model, OSI is a logical structure for network operations standardized within the ISO; a seven-layer network architecture being used for the definition of network protocol standards to enable any OSI-compatible computer or device to communicate with any other OSI-compliant computer or device for a meaningful exchange of information.

OVERFLOW - Excess traffic on a particular route, which is offered to another (alternate) route.

P

PABX - Private Automatic Branch Exchange. See Exchange, Private Automatic Branch (PABX).

PACKET - A group of binary digits including data and call control signals that is switched as a composite whole. The data, call control signals, and error control information are arranged in a specified format.

PBX - Private Branch Exchange. See Exchange, Private Branch.

PCMCIA - Personal Computer Memory Card International Association. Type 1: 3.3 mm thick
Type 2: 5.0 mm thick

PHASE JITTER - In telephony, the measurement, in degrees out of phase, that an analog signal deviates from the referenced phase of the main data-carrying signal. Often caused by alternating current components in a telecommunications network; or: a random distortion of signal lengths caused by the rapid fluctuation of the frequency of the transmitted signal. Phase jitter interferes with interpretation of information by changing the timing.

PHASE MODULATION - One of three ways of modifying a sine wave signal to make it carry information. The sine wave or “carrier” has its phase changed in accordance with the information to be transmitted.

PROPAGATION DELAY - The period between the time when a signal is placed on a circuit and when it is recognized and acknowledged at the other end. Propagation delay is of great importance in satellite channels because of the great distances involved.

PROTOCOL - A set of procedures for establishing and controlling communications. Examples include BSC, SDLC, X.25, V.42, V.42bis, MNP, V.22bis handshake, etc.

PSK - Phase Shift Keying. A method of modulation that uses the differences in phase angle between two symbols to encode information. A reference oscillator determines the phase angle change of the incoming signal, which in turn determines which bit or dibit is being transmitted. DPSK (Differential Phase Shift Keying) is a variation of PSK which changes the phase relative to the previous phase.

PULSE CODE MODULATION (PCM) - A method of transmitting information by varying the characteristics of a sequence of pulses, in terms of amplitude, duration, phase, or number. Used to convert an analog signal into a digital bit stream for transmission.

R

REGENERATIVE REPEATER - 1) Repeater utilized in telegraph applications to retime and retransmit the received signal impulses and restore them to their original strength. These repeaters are speed- and code-sensitive and are intended for use with standard telegraph speeds and codes. 2) Repeater used in PCM or digital circuits which detects, retimes, and reconstructs the bits transmitted.

REGENERATOR - Equipment that takes a digital signal that has been distorted by transmission and produces from it a new signal in which the shape, timing, and amplitude of the pulses are that same as those of the original before distortion.

REPEATER - 1) In analog transmission, equipment that receives a pulse train, amplifies it and retimes it for retransmission. 2) In digital transmission, equipment that receives a pulse train, reconstructs it, retimes it, and often then amplifies the signal for retransmission. 3) In fiber optics, a device that decodes a low-power light signal, converts it to electrical energy, and then retransmits it via an LED or laser-generating light source. See also Regenerative Repeater.

REVERSE CHANNEL - A simultaneous low speed data path in the reverse direction over a half-duplex facility. Normally, it is used for positive/negative acknowledgements of previously received data blocks.

RINGER EQUIVALENCE NUMBER - This is a number that the FCC assigns to approved telecom equipment that measures how much load it places on the network during ringing. In the U.S.A., you can connect telephones, modems, FAX machines etc. In parallel to the same telephone line only as long as the sum of their ringer equivalence numbers is less than five. Most countries have a similar regulating system in force, although the methods used to arrive at the number vary widely.

RINGING SIGNAL - Any AC or DC signal transmitted over a line or trunk for the purpose of alerting a party at the distant end of an incoming call. The signal can operate a visual or sound-producing device.

RINGING TONE - Tone received by the calling telephone indicating that the called telephone is being rung. Also called Ringback.

RSSI - Receive signal strength indicator (i.e., go to gain control in AM signal).

S

SCRAMBLER/DESCRAMBLER - A scrambler function uses a defined method for modifying a data stream, in order to make the altered data stream appear random. A descrambler reverses the effect of the scrambler using the previously defined method to recover the original data stream. Most often used for data encryption, or to avoid transmitting repetitive data patters that can adversely affect data recovery in modems and other data transmission equipment.

SDLC - Synchronous Data Link Control. IBM bit oriented protocol providing for half-duplex transmission; associated with IBM's System Network Architecture (SNA).

SHIELDED PAIR - Two insulated wires in a cable wrapped with metallic braid or foil to prevent interference and provide noise-free transmission.

SIGNAL-TO-NOISE RATIO - The relative power of a signal as compared to the power of noise on a line. As the ratio decreases, it becomes more difficult to distinguish between information and interference.

SIMPLEX - Pertaining to the capability to move in one direction only. Contrast with half-duplex and full-duplex.

SIGNALING - Process by which a caller or equipment on the transmitting end of a line informs a particular party or equipment at the receiving end that a message is to be communicated.

SMART IF - Microcontroller bus interface for program control of RF components.

SONET - Synchronous optical network.

SPACE - Opposite signal condition to a "mark." The signal (communications channnel state) corresponding to a binary zero. In an EIA RS-232 channel, the spacing condition exists when the voltage is more positive than +3 volts.

SS - Spread spectrum.

ST - Start (signal to indicate end of outpulsing).

STS1 - 51.84 Mbit/s, Sonet.

START-STOP (SIGNALING) - Signaling in which each group of code elements corresponding to a character is preceded by a start signal that serves to prepare the receiving mechanism for the reception and registration of character, and is followed by a stop signal that serves to bring the receiving mechanism to rest in preparation for the reception of the next character. Also known as asynchronous transmission.

STOP-BIT - In asynchronous transmission, the quiescent state following the transmission of a character; usually 1-, or 2-bit times long.

STOP ELEMENT - Last bit of a character in asynchronous serial transmission, used to ensure recognition of the next start element.

SUBSCRIBER LINE - Telephone line connecting the exchange to the subscriber's station. Also called (U.S. term) access line and subscriber loop.

SW56 - Switched 56 Kbit/s digital transmission.

SYNCHRONOUS - Having a constant time interval between successive bits, characters, or events. Synchronous transmission doesn't use non-information bits (such as the start and stop bits in asynchronous transmission) to identify the beginning and end or characters, and thus is faster and more efficient than asynchronous transmission. The timing is achieved by transmitting sync characters prior to data or by extracting timing information from the carrier or reference.

SYNCHRONOUS NETWORK - Network in which all the communications links are synchronized to a common clock.

SYNCHRONOUS TRANSMISSION - Transmission process where the information and control characters are sent at regular, clocked intervals so that the sending and receiving terminals are operating continuously in step with each other.

T

T-CARRIER - A time-division multiplexed, digital transmission facility, operating at an aggregate data rate of 1.544 Mbit/s and above. T-carrier is a PCM system using 64 Kbit/s for a voice channel.

T1 - A digital facility used to transmit a DS-1 formatted digital signal at 1.544 Mbit/s; the equivalent of 24 voice channels.

T1C/T2/T3/T4 - Digital carrier facilities used to transmit signals at 3.152M, 6.312M, 44.736M, 274.176 Mbit/s, respectively.

T3 - A digital carrier facility used to transmit a DS-3 formatted digital carrier signal at 44.736 Mbit/s; the equivalent of 672 voice channels.

TACS - Total access communications system. (U.K. analog cellular standard).

TDMA - Time division multiple access.

TCVCXO - Temperature-compensated, voltage - controlled crystal oscillator.

TOUCH-TONE - An AT&T trademark for dualtone multifrequency signaling equipment. Use of tones simplifies the switching system design and greatly expands the potential for adding features to telephone systems. It also speeds up the dialing operation for a person making a call.

TRANSCEIVER - Device that can transmit and receive traffic.

TRUNK - Transmission paths that are used to interconnect exchanges in the main telephone network, two switching centers, or a switching center and a distribution point, such as a telephone exchange line that terminates in a PABX network.

TTL - Transistor-Transistor Logic. Digital logic family having common electrical characteristics.

TURNAROUND TIME - The time required to reverse the direction of transmission, e.g; to change from receive mode to transmit mode in order to acknowledge on a half-duplex line. When individual blocks are acknowledged, as is required in certain protocols (e.g., IBM BSC) the turnaround time has a major effect on throughput, particularly if the propagation delay is lengthy, such as on a satellite channel.

TWO-WIRE CIRCUIT - Circuit formed of two conductors insulated from each other, providing a send and return path. Signals may pass in one or both directions.

V

VIDEOTEX - An interactive data communications application designed to allow unsophisticated users to converse with remote databases, enter data for transactions, and retrieve textual and graphics information for display on subscriber television sets or low-cost terminals.

VSLI - Very Large Scale Integration.

V SERIES RECOMMENDATIONS -
(CCITT V.xx Standards)
Also see Voiceband Modem Standards chart on page 9-12.

V.1 - Definitions of key terms for binary symbol notation, such as binary 0 = space, binary 1 = mark.

V.2 (1) - Specification of power levels for data transmission over telephone line.

V.4 - Definition of the order of bit transmission, the use of a parity bit, and the use of start/stop bits for asynchronous transmission.

V.5 - Specification of data-signaling rates (bit/s) for synchronous transmission in the switched telephone network.

V.6 - Specification of data signaling rates (bit/s) for synchronous transmission on leased telephone circuits.

V.7 - Definitions of other key terms used in the V-series recommendations.

V.10 - Description of an unbalanced physical level interchange circuit (unbalanced means one active wire between transmitter and receiver with ground providing the return).

V.11 - Description of a balanced physical level interchange circuit (balanced means two wires between the transmitter and receiver with both wires' signals constant with respect to Earth).

V.15 - Description of use of acoustic couplers for data transmission.

V.16 - Description of the transmission of ECG (electrocardiogram) signals on the telephone channel.

V.19 - Description of one-way parallel transmission modems using push-button telephone sets.

V.20 - Description of one-way parallel transmission modems, excluding push-button telephone sets.

V.22 - Operating at 1.2 Kbit/s, encodes two consecutive bit (dibits); the dibits are encoded as a change relative to the previous signal element.

V.22bis - Operating at 2.4 Kbit/s, encodes four consecutive bits (quadbits); the first two bits are encoded relative to the quadrant of the previous signal element, the last two bits are associated with the point in new quadrant.

V.24 - Definition of the interchange circuit pins between DTEs (data terminal equipment) and DCEs (data circuit-terminating equipment).

V.25 - (2) - Specifications for automatic-answering equipment.

V.25bis - (2) - Specifications for automatic-answering equipment.

V.28 - Description of unbalanced interchange circuits operating below 20 Kbit/s.

V.29 - Operating at 9.6 Kbit/s, encodes four consecutive bits (quadbits); the first bit determines the amplitude, the last three bits use the encoding scheme of V.27.

V.29 - Operating at 4.8 Kbit/s, encodes two consecutive bits (dibits); amplitude is constant and phase changes are the same as V.26.

V.31 - Description of low-speed interchange circuits (up to 75 Bit/s).

V.31bis - Description of low-speed interchange circuits (up to 1.2 Kbit/s).

V.32 - Operating at 9.6 Kbit/s, encodes four consecutive bits (quadbits); the bits are mapped to a QAM signal.

V.32 - Operating at 9.6 Kbit/s with Trellis-coded modulation (TCM), encodes four consecutive bits, two of which are used to generate a fifth bit; the bits are mapped to a QAM signal.

V.32 - Operating at 4.8 Kbit/s, encodes two consecutive bits (dibits), which are mapped to a QAM signal.

V.42 - Defines a method of error control.

V.42bis - Defines a method of data compression.

Note: In the United States, EIA RS-496 specifies these measurements and RS-366 specifies these procedures.

VOICE-GRADE CHANNEL - a channel with a frequency range from 300 to 3000 Hz and suitable for the transmission of speech, data, or facsimile.

W

WORD - A group of bits handled as a logical unit; usually 16.

Voiceband Modem Standards

CCITT Standard	Data Rate (Bit/s)	Full- or Half-Duplex	Channel Separation	Carrier Frequency (Hz)	Modulation Method	Modulation Rate (Baud)	Bits Encoded	Synchronous or Asynchronous	Back Channel	GSTN	Leased Lines	Equalization	Scrambler
V.21	300	Full	Frequency Division	1080, & 1750	Frequency Shift	300	1:1	Either	ND	Yes	No	ND	ND
V.22	1200	Full	Frequency Division	1200, & 2400	Phase Shift	600	2:1	Either	ND	Yes	Point-to-Point 2-Wire	Fixed	Yes
V.22	600	Full	Frequency Division	1200, & 2400	Phase Shift	600	1:1	Either	ND	Yes	Point-to-Point 2-Wire	Fixed	Yes
V.22bis	2400	Full	Frequency Division	1200, & 2400	Quadrature-Amplitude Modulation	600	4:1	Either	ND	Yes	Point-to-Point 2-Wire	Fixed/ Adaptive	Yes
V.23	600 (1)	Half	N/A	1300, & 1700	Frequency Modulation	600	N/A	Either	Yes	Yes	No	ND	ND
V.23	1200 (1)	Half	N/A	1300, & 2100	Frequency Modulation	1200	N/A	Either	Yes	Yes	No	ND	ND
V.25	2400	Full	4-Wire	1800	Phase Shift	1200	2:1	Synchronous	Yes	No	Point-to-Point Multipoint 4-Wire	ND	ND
V.26bis	2400	Half	N/A	1800	Phase Shift	1200	2:1	Synchronous	Yes	Yes	No	Fixed	ND
V.26bis	1200	Half	N/A	1800	Phase Shift	1200	1:1	Synchronous	Yes	Yes	No	Fixed	ND
V.26ter	2400	Either	Echo Cancellation	1800	Phase Shift	1200	2:1	Either	ND	Yes	Point-to-Point 2-Wire	Either	Yes
V.26ter	1200	Either	Echo Cancellation	1800	Phase Shift	1200	1:1	Either	ND	Yes	Point-to-Point 2-Wire	Either	Yes
V.27	4800	Either	ND (3)	1800	Phase Shift	1600	3:1	Synchronous	Yes	No	Yes (3)	Manual	Yes
V.27bis	4800	Either	4-Wire (4)	1800	Phase Shift	1600	3:1	Synchronous	Yes	No	2-Wire, 4-Wire	Adaptive	Yes
V.27bis	2400	Either	4-Wire (4)	1800	Phase Shift	1200	2:1	Synchronous	Yes	No	2-Wire, 4-Wire	Adaptive	Yes
V.27ter	4800	Half	None	1800	Phase Shift	1800	3:1	Synchronous	Yes	Yes	No	Adaptive	Yes
V.27ter	2400	Half	None	1800	Phase Shift	1200	2:1	Synchronous	Yes	Yes	No	Adaptive	Yes
V.29	9600	Either	4-Wire	1700	Quadrature-Amplitude Modulation	2400	4:1	Synchronous	No	No	Point-to-Point 4-Wire	Adaptive	Yes
V.29	7200	Either	4-Wire	1700	Phase Shift (5)	2400	3:1	Synchronous	ND	No	Point-to-Point 4-Wire	Adaptive	Yes
V.29	4800	Either	4-Wire	1700	Phase Shift (5)	2400	2:1	Synchronous	ND	No	Point-to-Point 4-Wire	Adaptive	Yes
V.32	9600	Full	Echo Cancellation	1800	Quadrature-Amplitude Modulation	2400	4:1	Synchronous	ND	Yes	Point-to-Point 2-Wire	Adaptive	Yes
V.32bis	14400	Full	Echo Cancellation	1800	Trellis-Coded Modulation	2400	6:1	Synchronous	ND	Yes	Point-to-Point 2-Wire	Adaptive	Yes
V.32	9600	Full	Echo Cancellation	1800	Quadrature-Amplitude Modulation	2400	4:1	Synchronous	ND	Yes	Point-to-Point 2-Wire	Adaptive	Yes
V.32	4800	Full	Echo Cancellation	1800	Quadrature-Amplitude Modulation	2400	2:1	Synchronous	ND	Yes	Point-to-Point 2-Wire	Adaptive	Yes
V.33	14400	Half						Synchronous	ND	Yes		Adaptive	Yes
V.34	28800	Full	Echo Cancellation	1800	Trellis-Coded Modulation	2400	12:1	Synchronous	ND	Yes	Point-to-Point 2-Wire	ND	Yes
Bell (U.S.) Standard													
103	300	Full	Frequency Division	2225 & 1270(m) 2025 & 1070(s)	Frequency Shift	300	1:1	Either	No	Yes	No	Fixed	No
201	2400	Half	None	1800	Phase Shift	1200	2:1	Synchronous	No	Yes	Point-to-Point 2-Wire	Adaptive	Yes
202	1200	Half	None	1200 & 2200	FSK	1200	1:1	Either	Yes	Yes	Point-to-Point 2-Wire	Fixed	No
208	4800	Half	None	1800	Quadrature-Amplitude Modulation	1600	3:1	Synchronous	No	Yes	Point-to-Point 2-Wire	Adaptive	Yes
212	1200	Full	Frequency Division	1200 & 2400	Phase Shift	600	2:1	Either	No	Yes	No	Fixed	Yes

1. Bit/s not used in specification; rate stated in baud. Low speed 75 bit/s back channel for asymetric full-duplex

2. Half-duplex may still use a backward channel

3. Makes no mention of 4-wire (must be assumed)

4. For half-duplex, 2-wire used

5. Amplitude is constant on a relative basis

ND = Not defined (i.e., not specified in the recommendation)

Section 11

PACKAGING / ORDERING INFORMATION

Silicon Systems
Packaging Index

DUAL-IN-LINE PACKAGE (DIP)	PINS
Plastic	8, 14, 16 & 18
	20, 22, 24 & 24S
	28, 32 & 40
Ceramic	8, 14, 16 & 18
	22, 24 & 28
SURFACE MOUNTED DEVICES (SMD)	
Quad (PLCC)	20, 28
	32 & 44
	52 & 68
Quad Flatpack (QFP)	52 & 10
	128
Thin Quad Flatpack (TQFP)	32 & 48
	64, 80 & 100
	120 & 128
	144
Very Thin Quad Flatpack (VTQFP)	32, 48 & 64
	100
	120
Ultra Thin Quad Flatpack (UTQFP)	64 & 100
Small Outline (SOIC)	8, 14 & 16 SON
	16, 18, 20, 24 & 28 SOL
	34 SOL
	32 SOW
	36 SOM
	44 SOM
Very Small Outline Package (VSOP)	16, 20, 24 & 28
Very Thin Small Outline Package (VTSOP)	16, 20 & 32
Ultra Thin Small Outline Package (UTSOP)	24 & 36

Package	Width (mil)	Pitch (mil)
SON	150	
SOL	300	
SOW	400	
SOM	300	0.8

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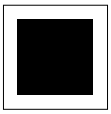
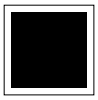
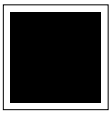
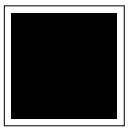
Small Form Factor Package Selector Guide

Quad Flatpack Packages

PACKAGE TYPE	ACTUAL SIZE (AREA)	BODY SIZE (PITCH) mm	LAYOUT AREA mm^2	ACTUAL SIZE (THICKNESS)	THICKNESS mm
52 G (QFP)		10.0 x 10.0 (0.65)	13.9 x 13.9 = 193.21		2.2
100 G (QFP)		20.0 x 14.0 (0.65)	23.9 x 17.9 = 427.81		2.9
128 G (QFP)		20.0 x 14.0 (0.5)	23.2 x 17.2 = 399.04		2.9
32 GT (TQFP)		7.0 x 7.0 (0.8)	9.0 x 9.0 = 81		1.4
48 GT (TQFP)		7.0 x 7.0 (0.5)	9.0 x 9.0 = 81		1.4
64 GT (TQFP)		10.0 x 10.0 (0.5)	12.0 x 12.0 = 144		1.4
80 GT (TQFP)		12.0 x 12.0 (0.5)	14.0 x 14.0 = 196		1.4
100 GT (TQFP)		14.0 x 14.0 (0.5)	16 x 16 = 256		1.4

 = Actual Body Size

 = Full Layout Area

All dimensions are nominal values.

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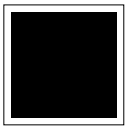
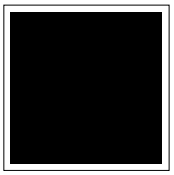
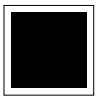
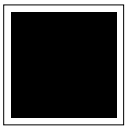
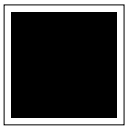
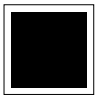
Small Form Factor Package Selector Guide

Quad Flatpack Packages

PACKAGE TYPE	ACTUAL SIZE (AREA)	BODY SIZE (PITCH) mm	LAYOUT AREA mm^2	ACTUAL SIZE (THICKNESS)	THICKNESS mm
120 GT (TQFP)		14.0 x 14.0 (0.4)	16.0 x 16.0 = 256		1.4
128 GT (TQFP)		20.0 x 14.0 (0.5)	22.0 x 16.0 = 352		1.4
144 GT (TQFP)		20.0 x 20.0 (0.5)	22.0 x 22.0 = 484		1.4
48 GV (VTQFP)		7.0 x 7.0 (0.5)	9.0 x 9.0 = 81		1.0
64 GV (VTQFP)		10.0 x 10.0 (0.5)	12.0 x 12.0 = 144		1.0
100 GV (VTQFP)		14.0 x 14.0 (0.5)	16.0 x 16.0 = 256		1.0
120 GV (VTQFP)		14.0 x 14.0 (0.4)	16.0 x 16.0 = 256		1.0
64 GU (UTQFP)		10.0 x 10.0 (0.5)	12.0 x 12.0 = 144		0.7

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Small Form Factor Package Selector Guide

Small Outline Packages

PACKAGE TYPE	ACTUAL SIZE (AREA)	BODY SIZE (PITCH) mm	LAYOUT AREA mm^2	ACTUAL SIZE (THICKNESS)	THICKNESS mm
16 SON		9.8 x 3.9 (1.27)	9.8 x 6.0 = 58.8		1.65
16 SOL		10.2 x 7.5 (1.27)	10.2 x 10.2 = 104		2.54
20 SOL		12.8 x 7.5 (1.27)	12.8 x 10.2 = 130.6		2.54
24 SOL		15.4 x 7.5 (1.27)	15.4 x 10.2 = 157		2.54
20 SOV (VSOP)		7.2 x 5.4 (0.65)	7.9 x 7.2 = 56.9		1.9
24 SOV (VSOP)		7.8 x 5.6 (0.65)	7.8 x 7.6 = 59.28		1.15
36 SOM (SSOP)		15.1 x 7.5 (0.8)	15.1 x 10.2 = 154		2.54
44 SOM (SSOP)		18.3 x 7.5 (0.8)	18.3 x 10.2 = 186.7		2.54
16 VT (VTSOP)		5.0 x 4.4 (0.65)	6.4 x 5.0 = 32		0.9
20 VT (VTSOP)		6.5 x 4.4 (0.65)	6.5 x 6.4 = 41.6		0.9

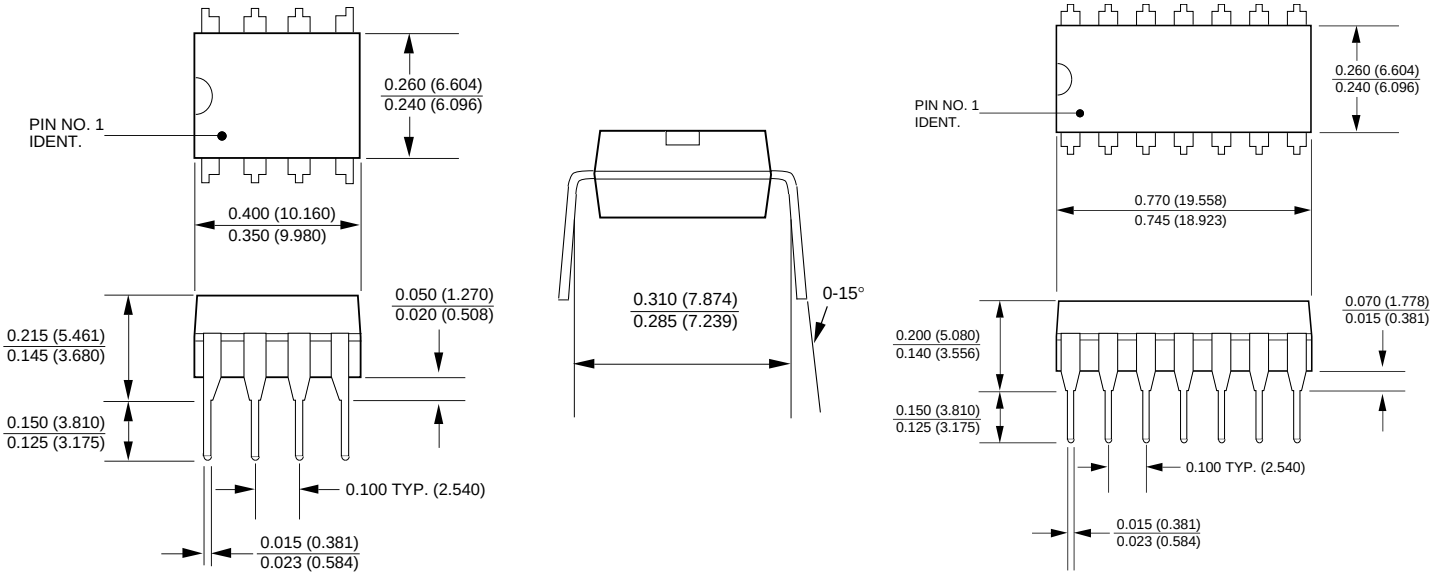
 = Actual Body Size

 = Full Layout Area

All dimensions are nominal values.

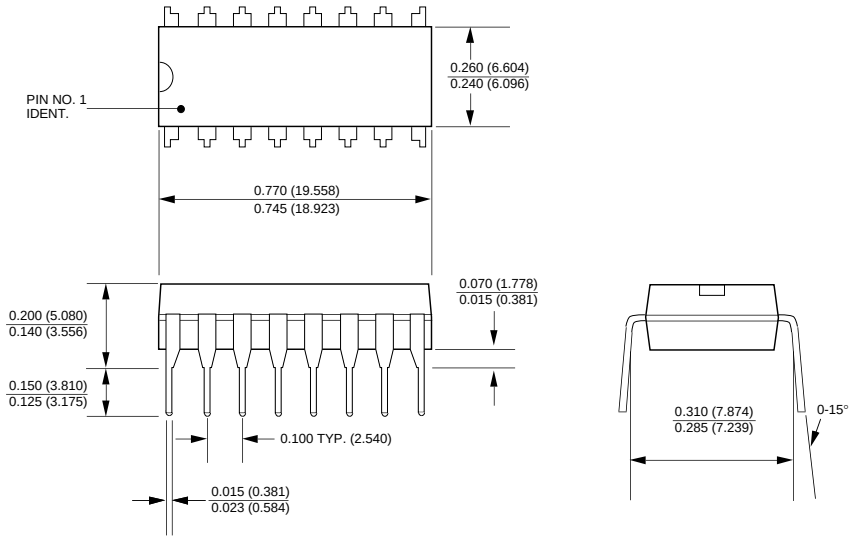
Package Information

Plastic DIP

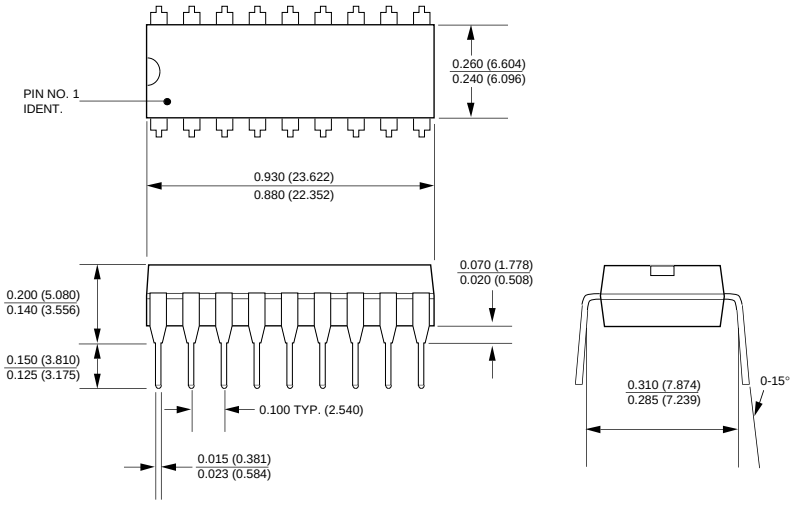


8-Pin Plastic

14-Pin Plastic

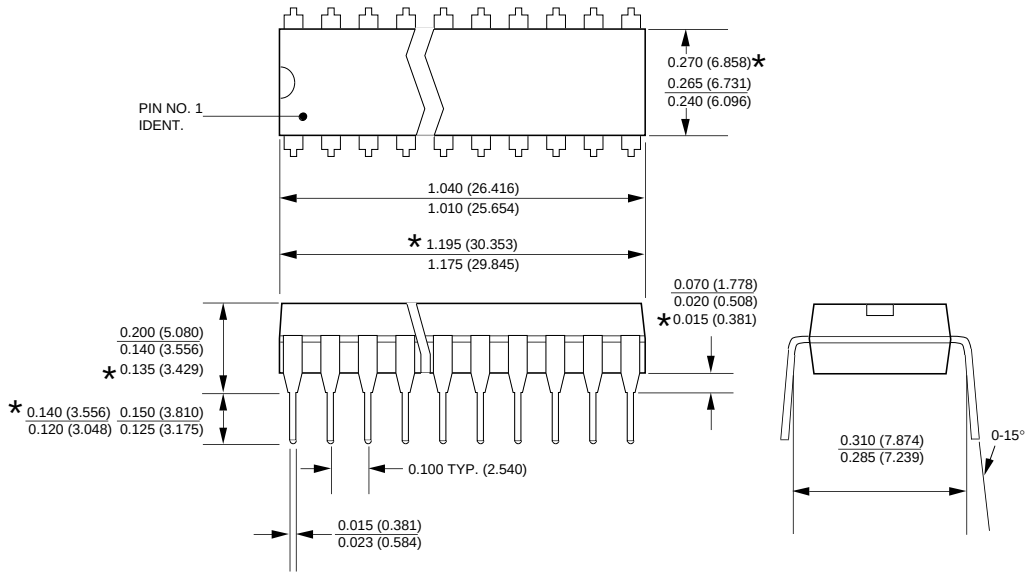


16-Pin Plastic

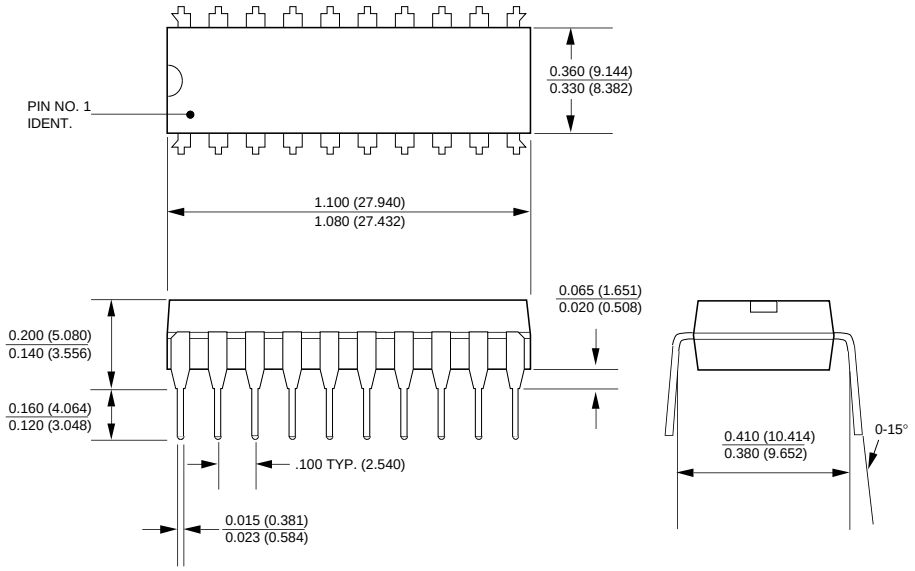


18-Pin Plastic

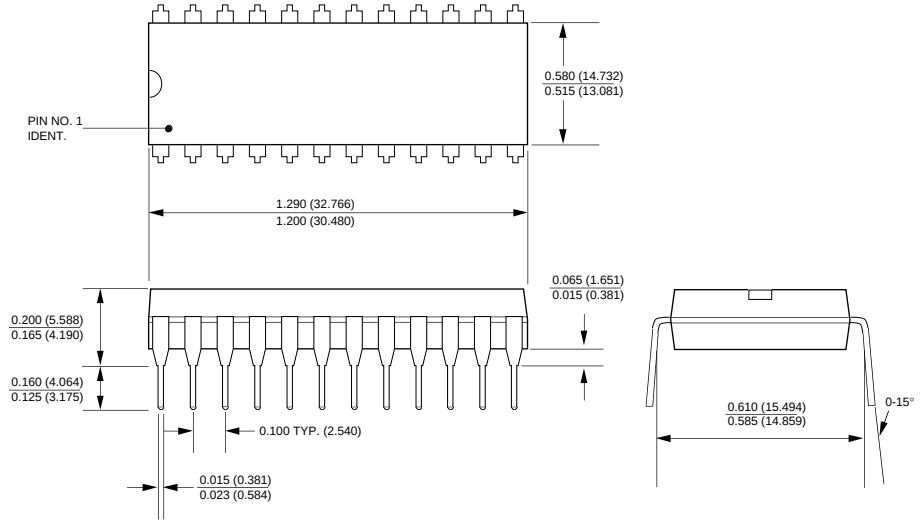
Package Information



20 Pin Plastic
***24S Pin Plastic**

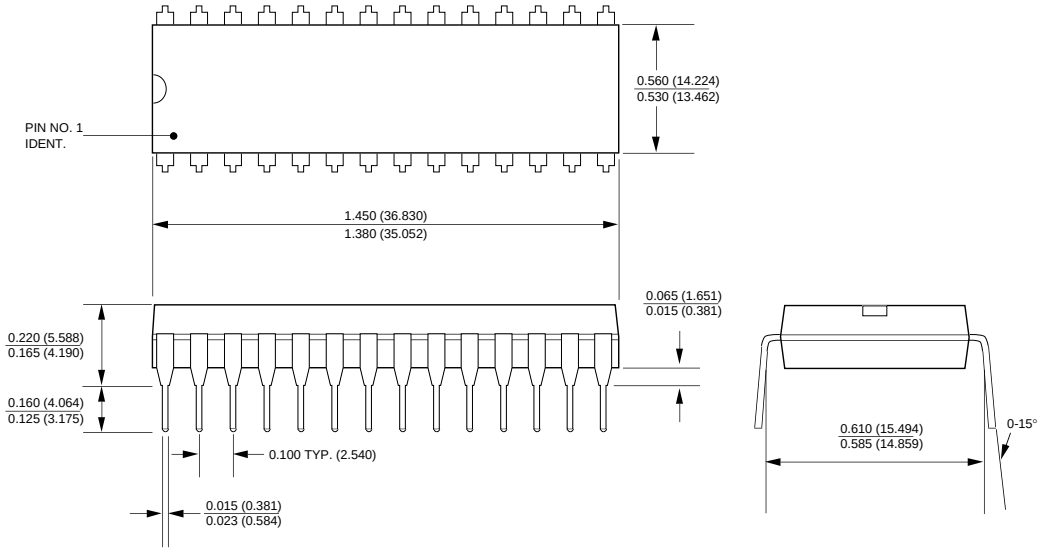


22-Pin Plastic

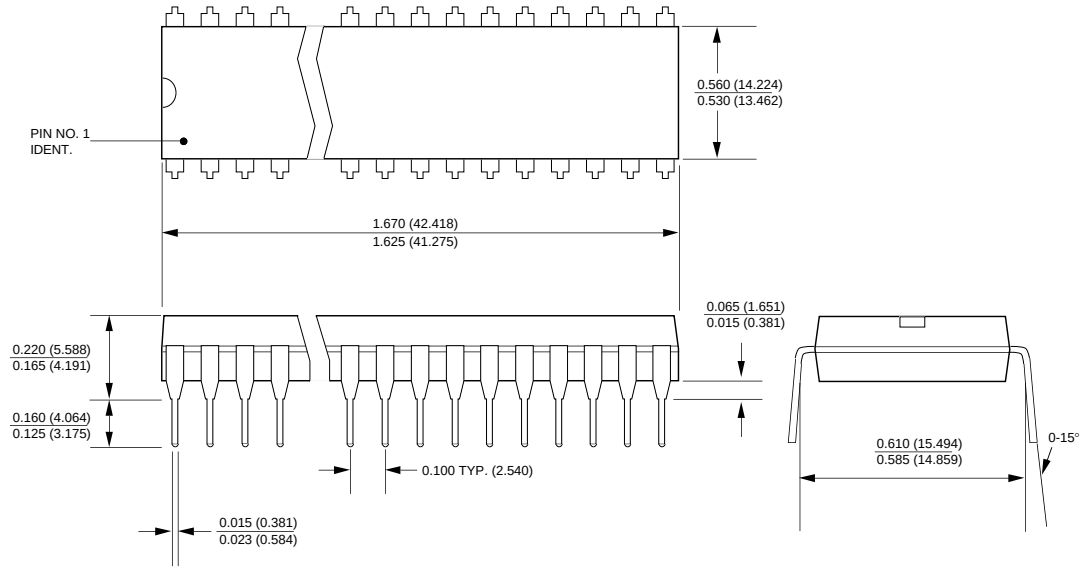


24-Pin Plastic

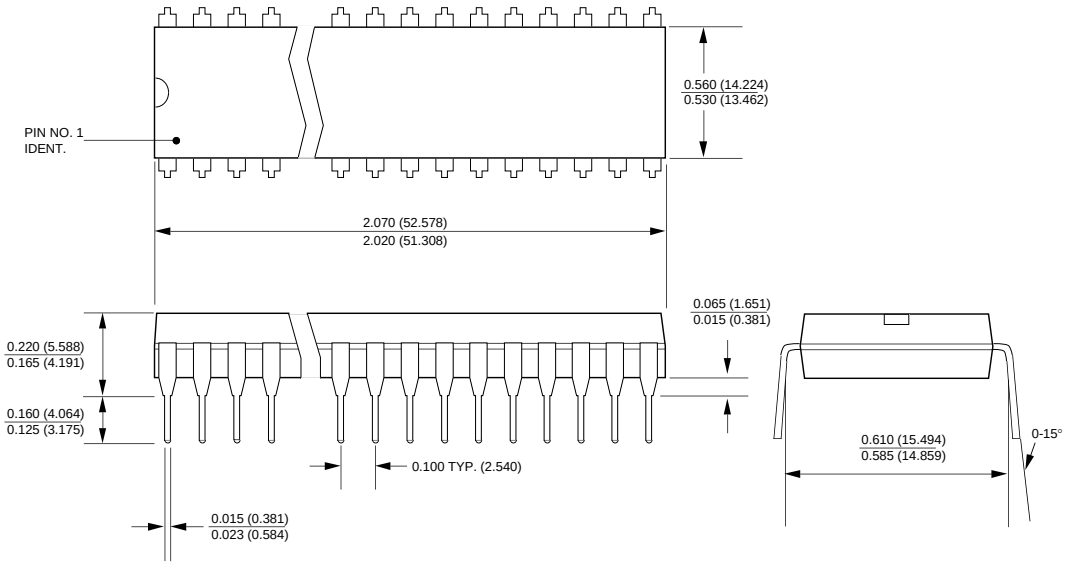
Package Information



28-Pin Plastic

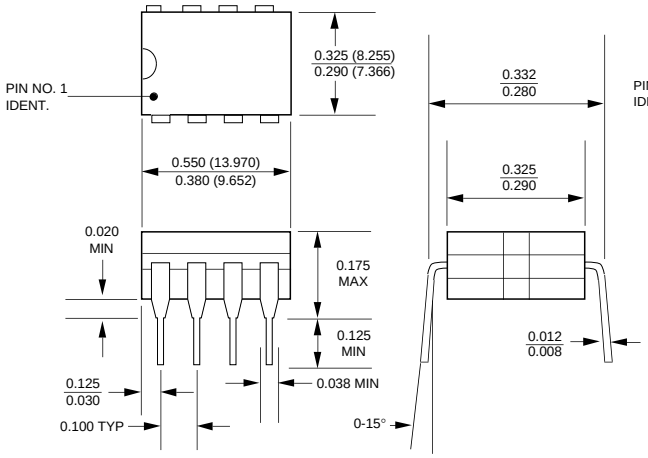


32-Pin Plastic

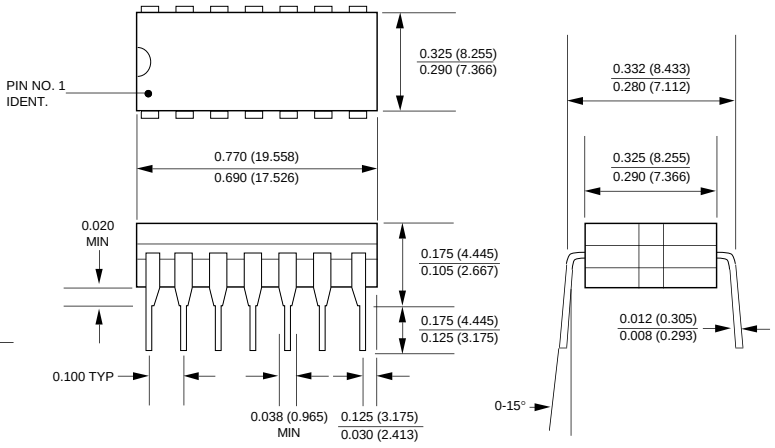


40-Pin Plastic

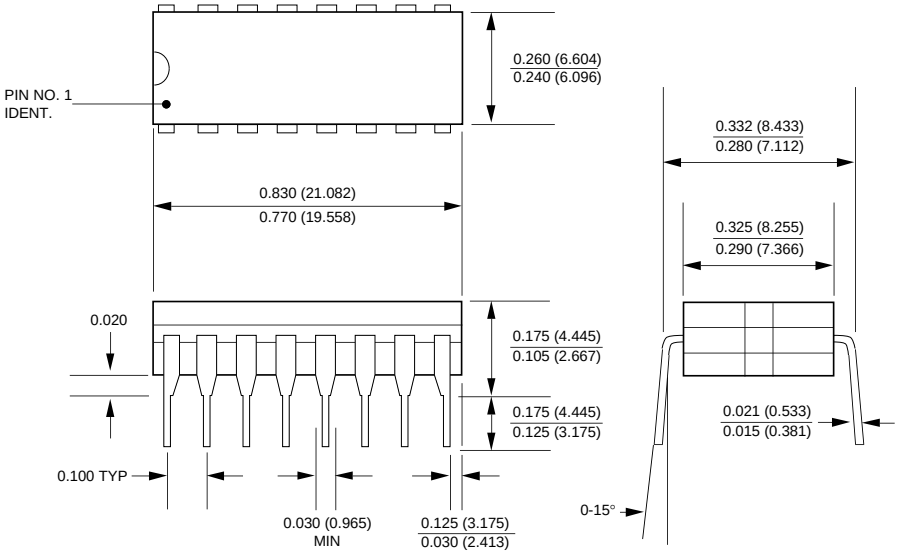
Package Information Cerdip



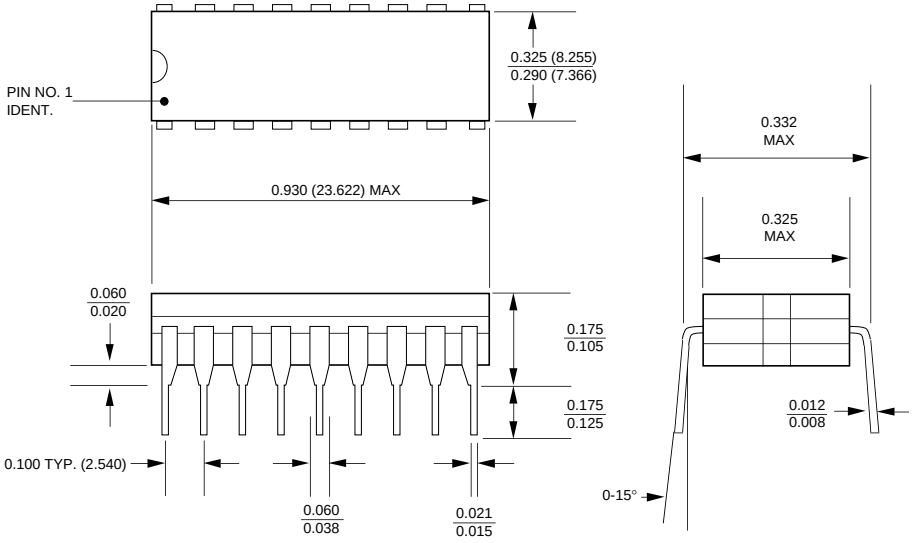
8-Pin Cerdip



14-Pin Cerdip

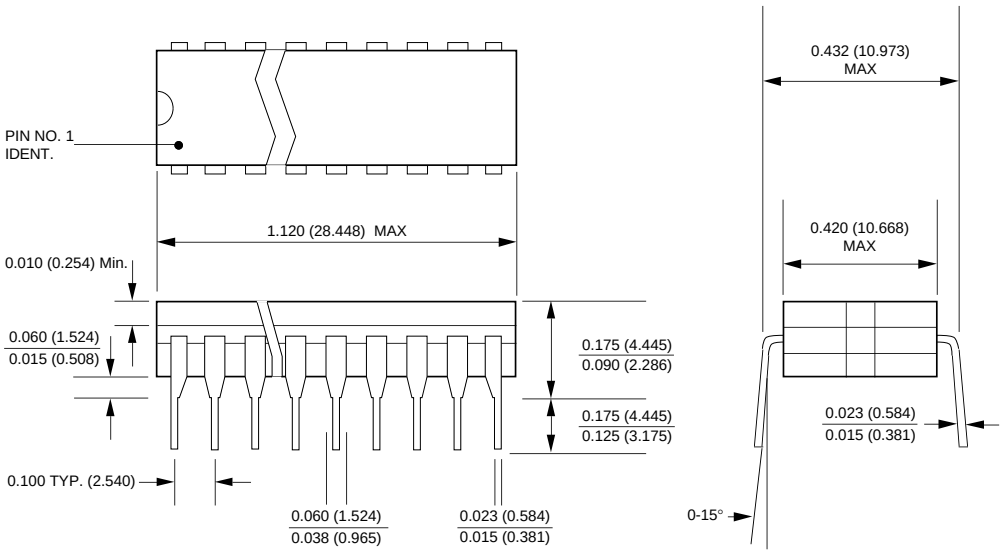


16-Pin Cerdip

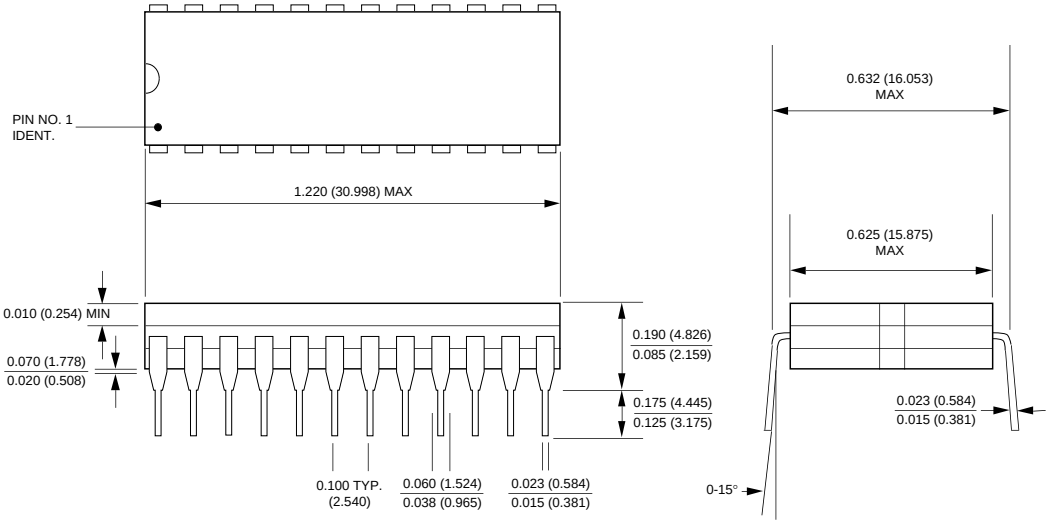


18-Pin Cerdip

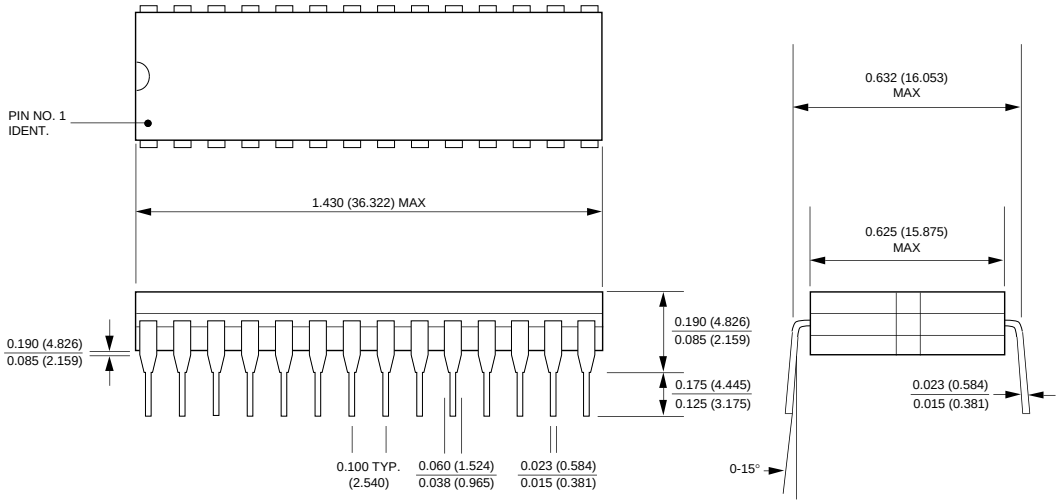
Package Information



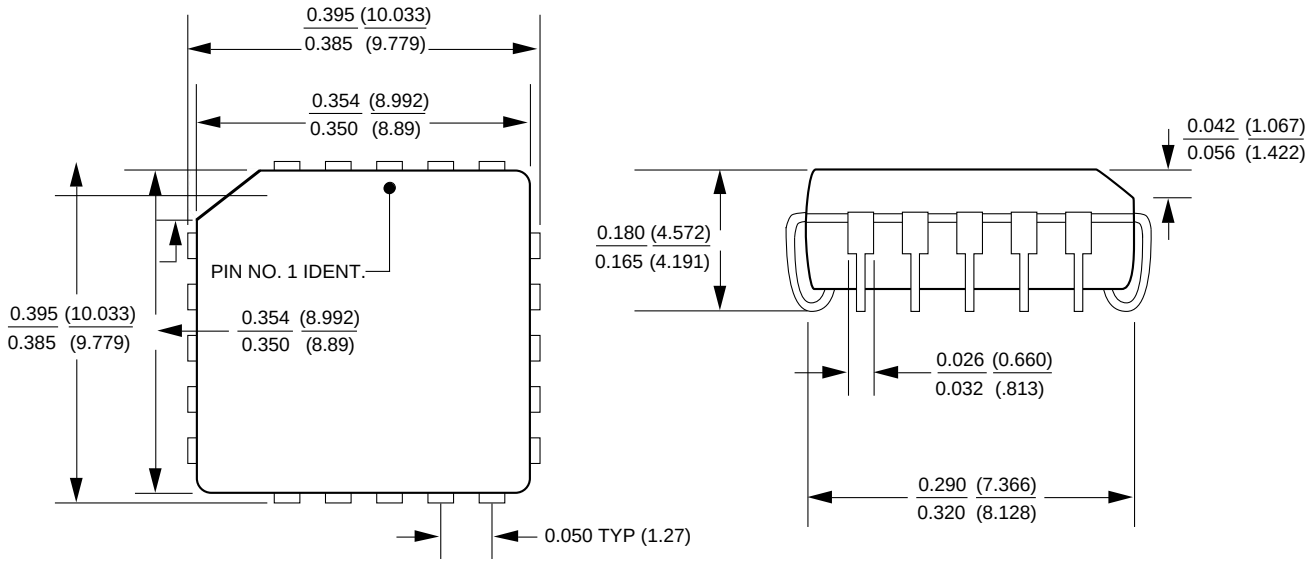
22-Pin Cerdip



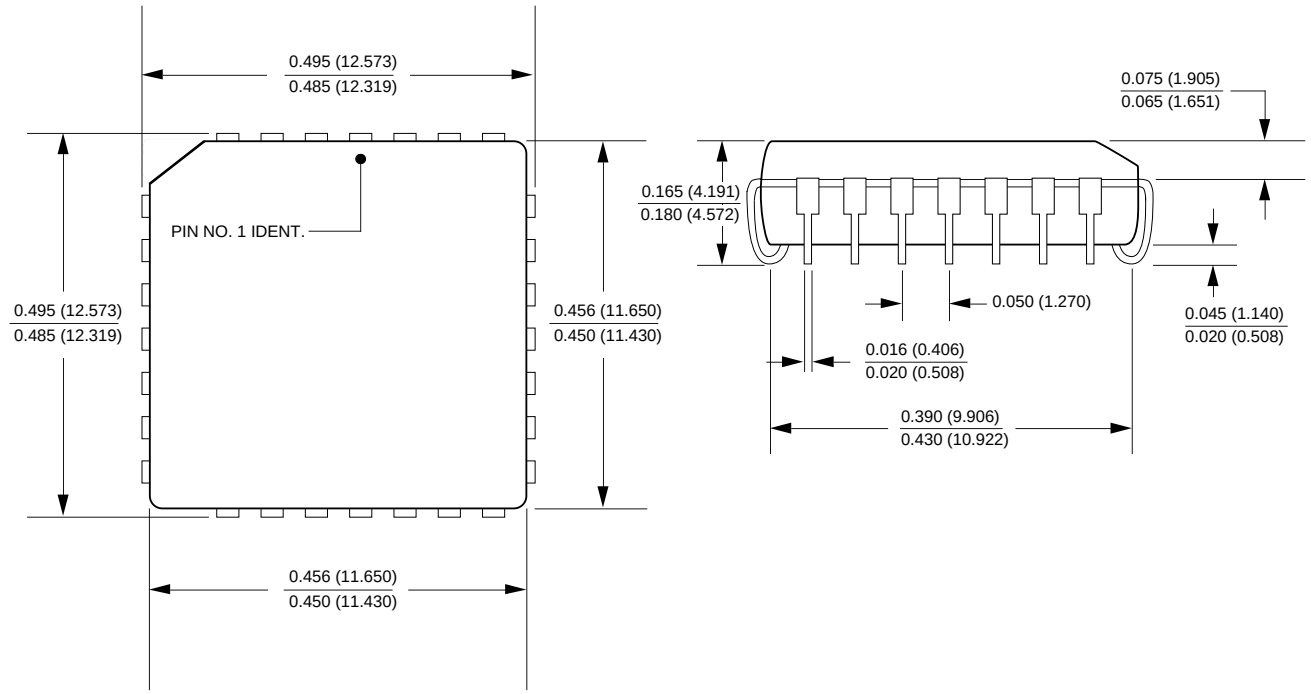
24-Pin Cerdip



28-Pin Cerdip

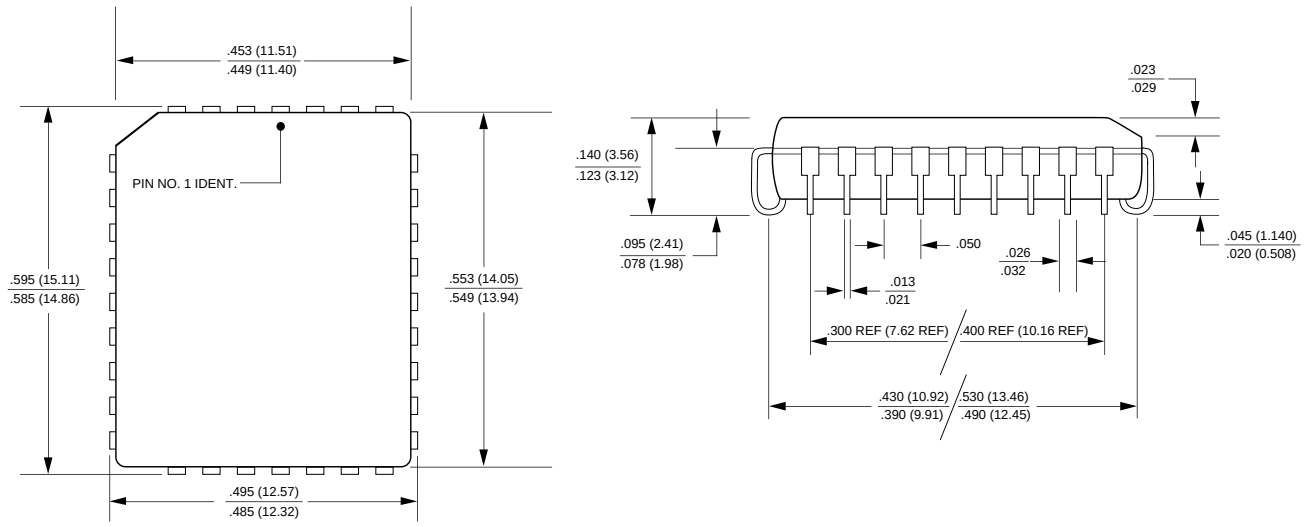


20-Pin Quad PLCC

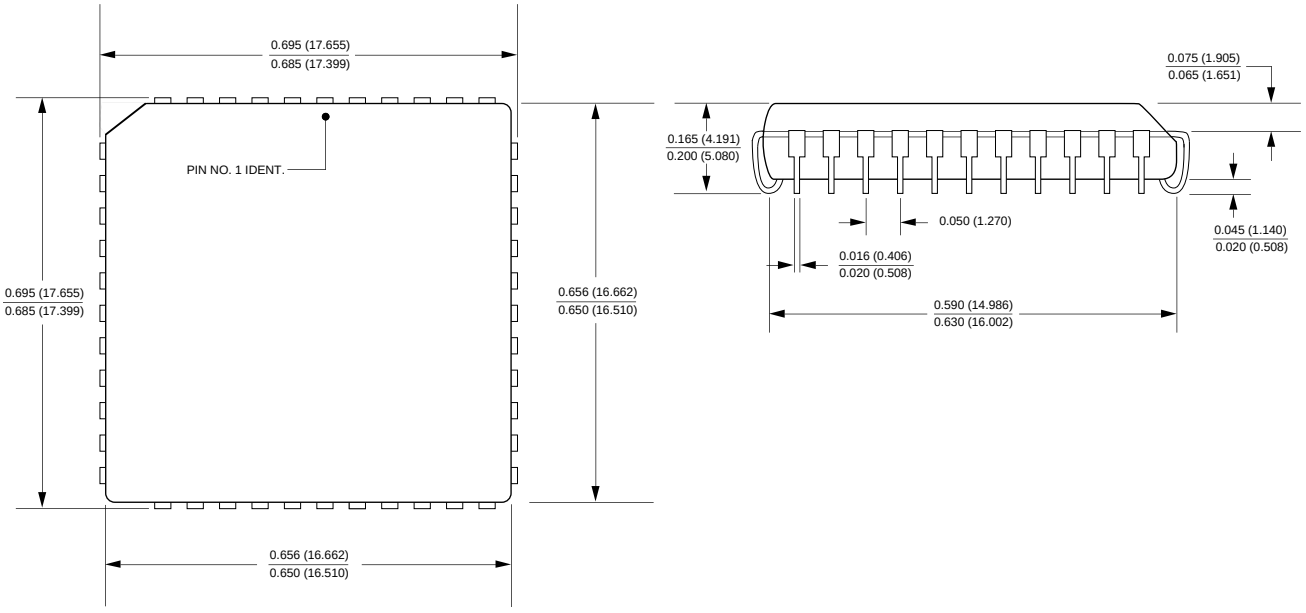


28-Pin Quad PLCC

Package Information

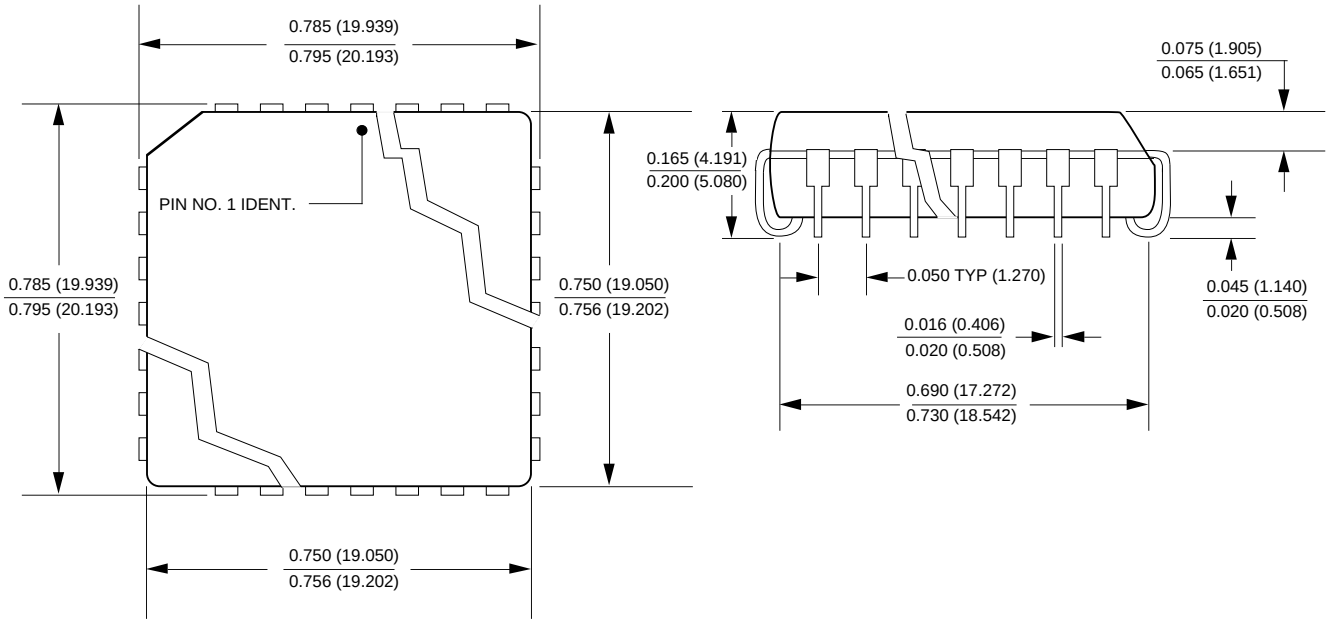


32-Pin Quad PLCC

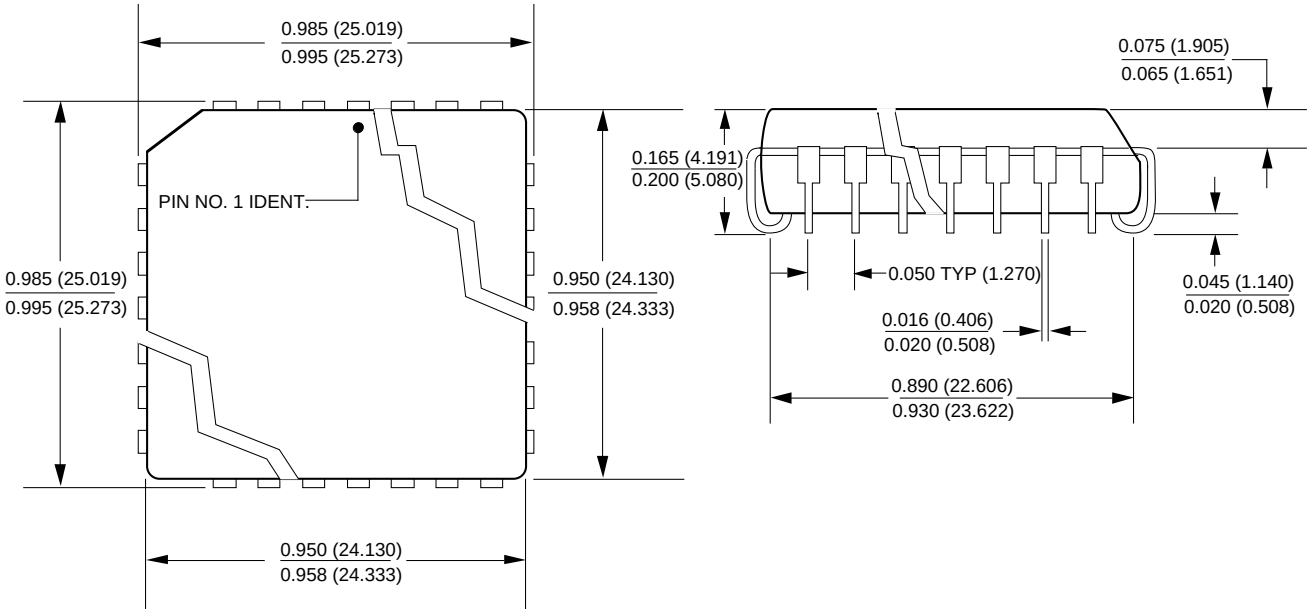


44-Pin Quad PLCC

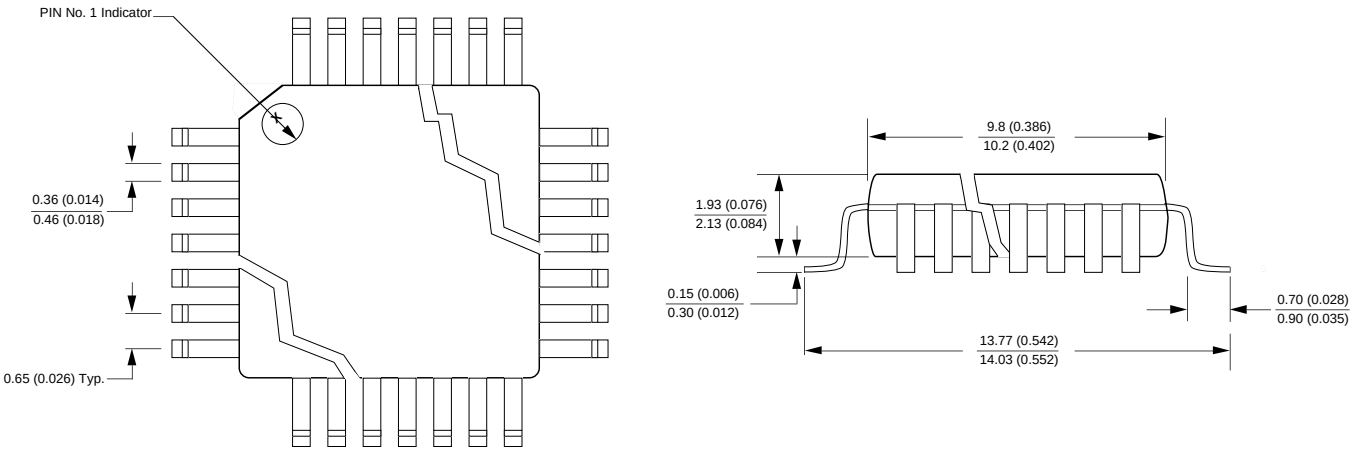
Package Information



52-Pin Quad PLCC

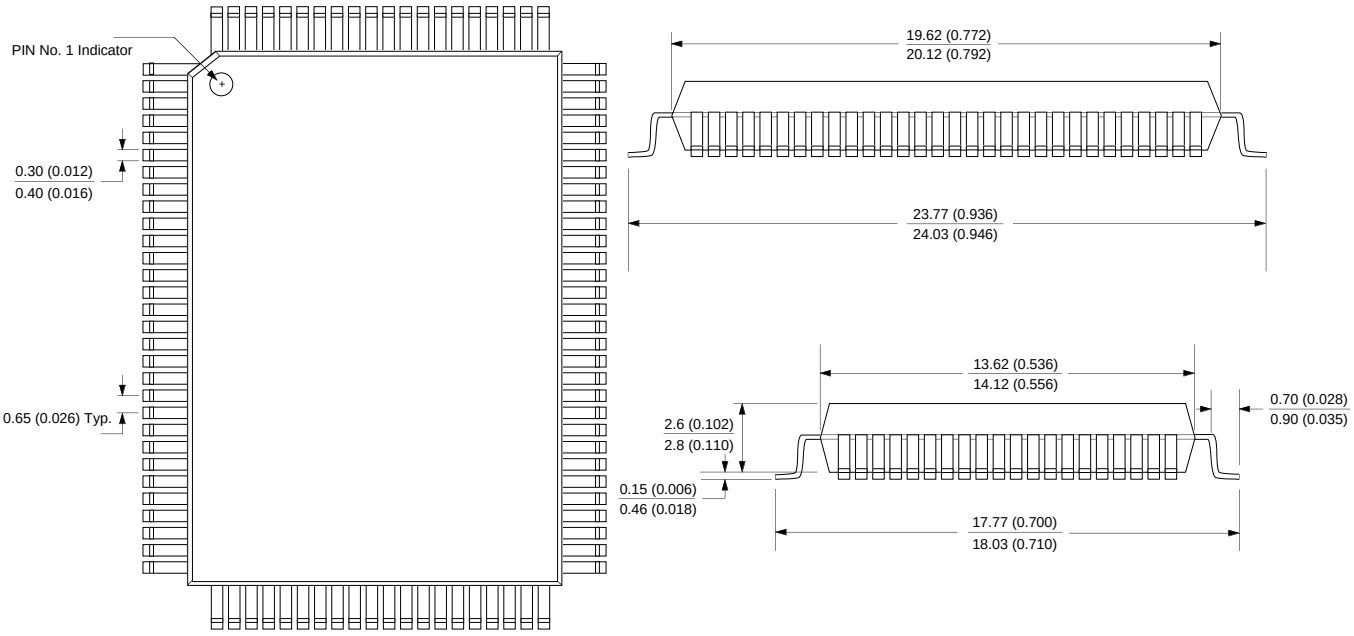


68-Pin Quad PLCC



52-Lead Quad Flatpack

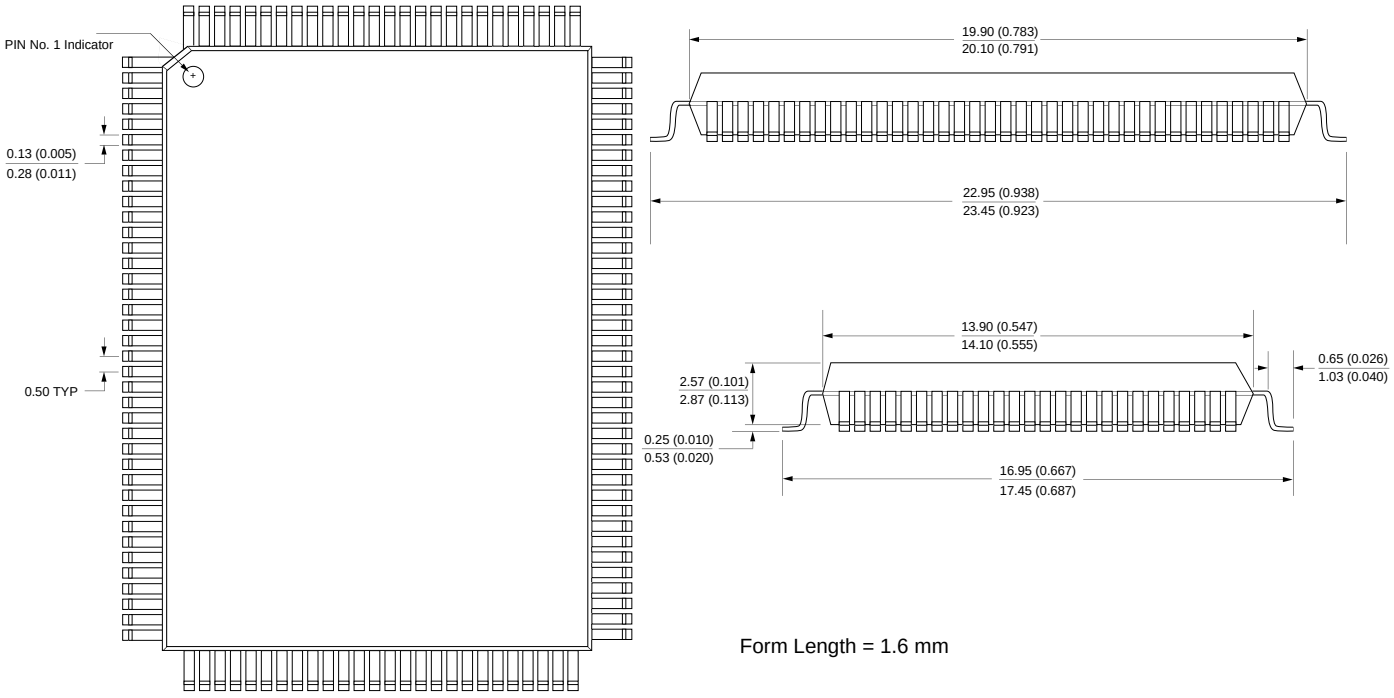
NOTE: Controlling dimensions are in mm



100-Lead Quad Flatpack

NOTE: Controlling dimensions are in mm

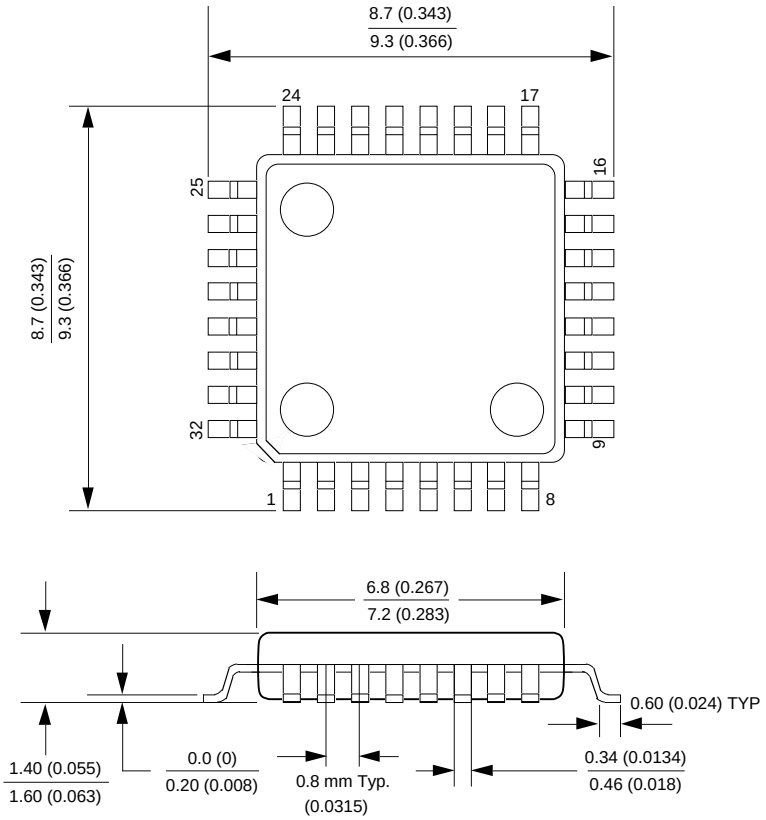
Package Information



Form Length = 1.6 mm

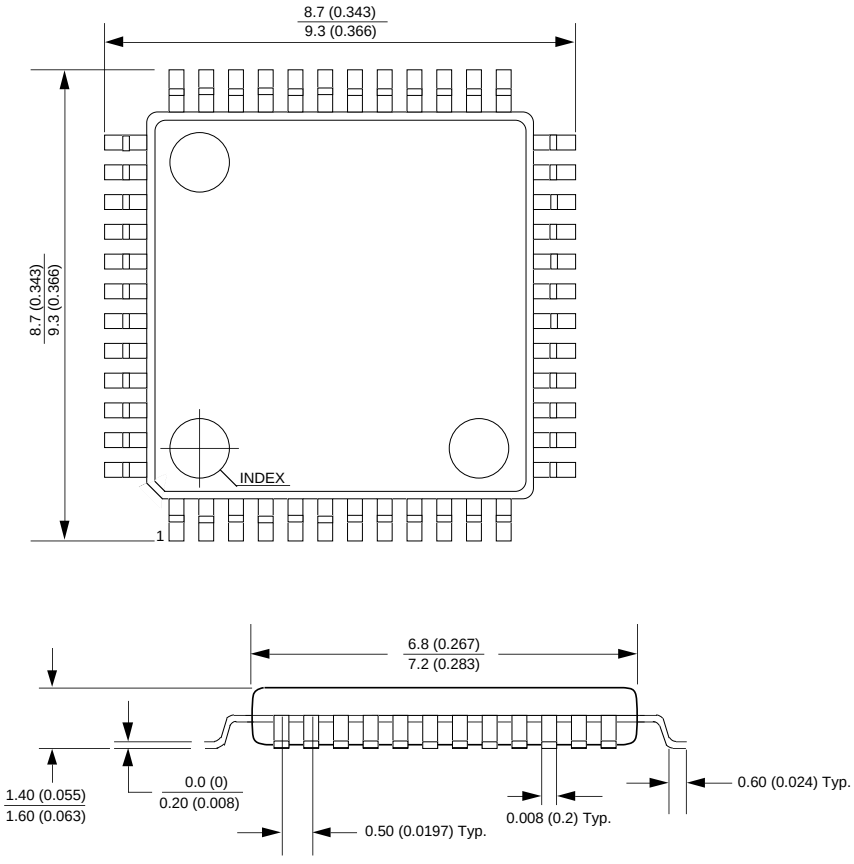
128-Lead Quad Flatpack

NOTE: Controlling dimensions are in mm



32-Lead Thin Quad Flatpack

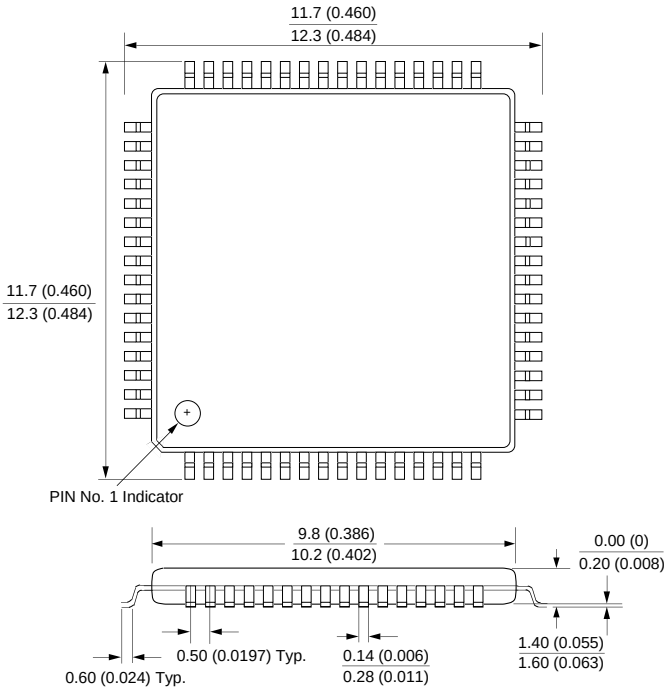
NOTE: Controlling dimensions are in mm



48-Lead Thin Quad Flatpack

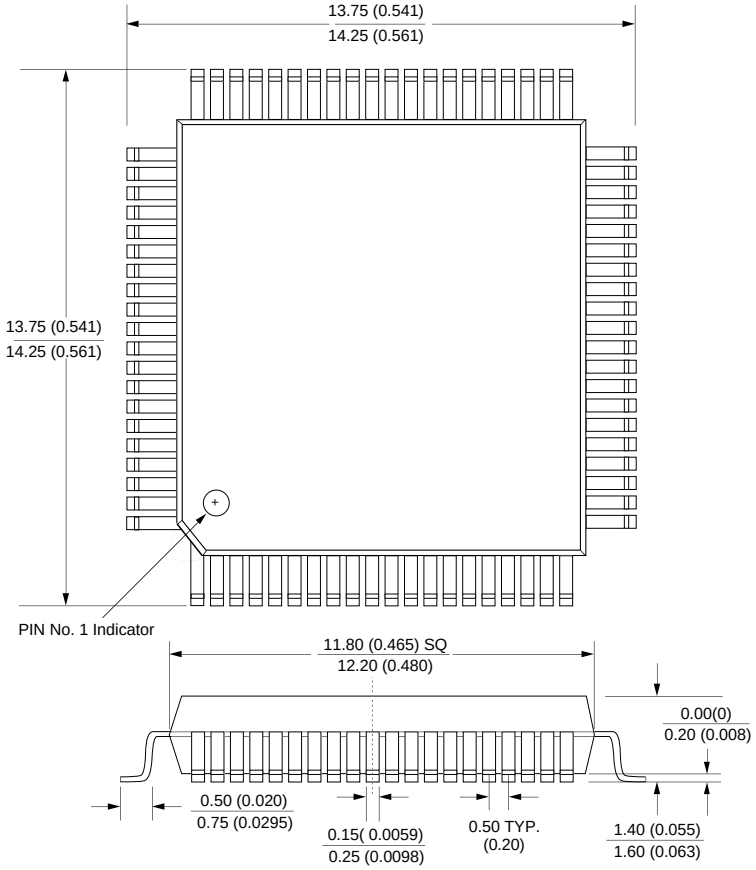
NOTE: Controlling dimensions are in mm

Package Information



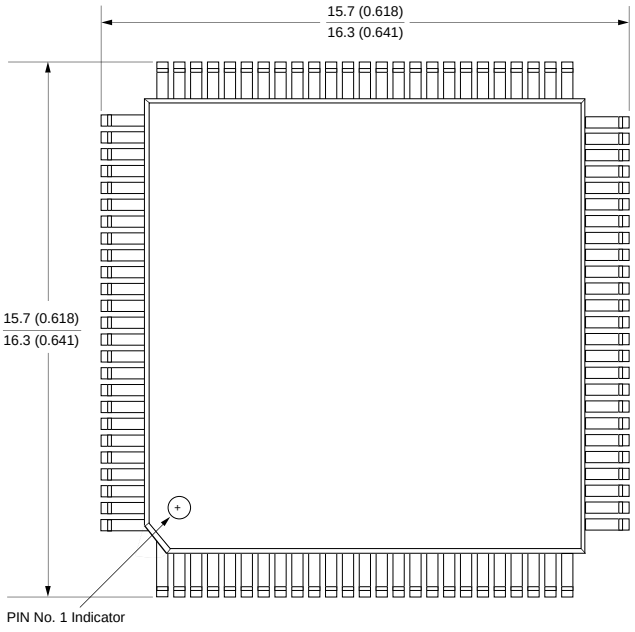
64-Lead Thin Quad Flatpack

NOTE: Controlling dimensions are in mm



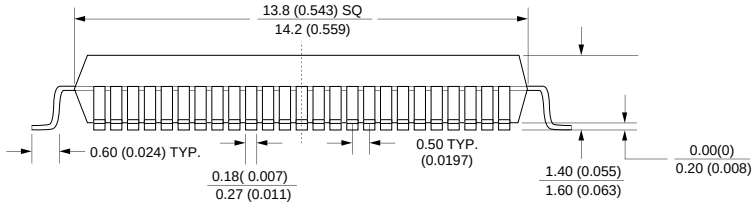
80-Lead Thin Quad Flatpack

NOTE: Controlling dimensions are in mm

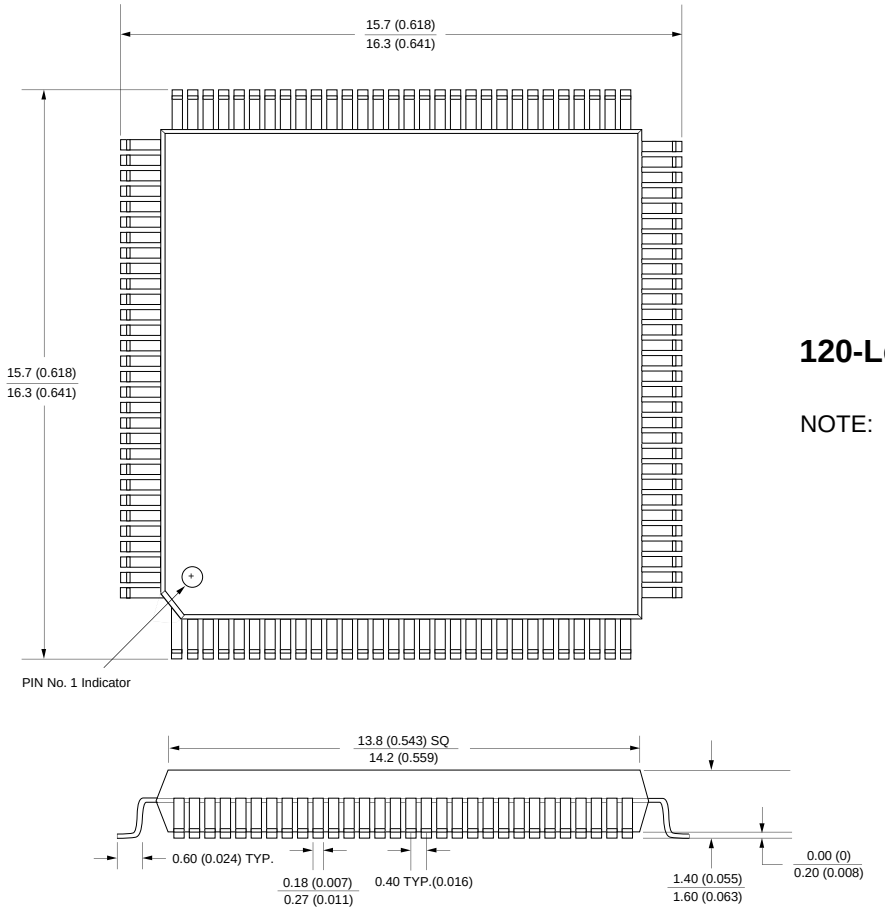


100-Lead Thin Quad Flatpack

NOTE: Controlling dimensions are in mm

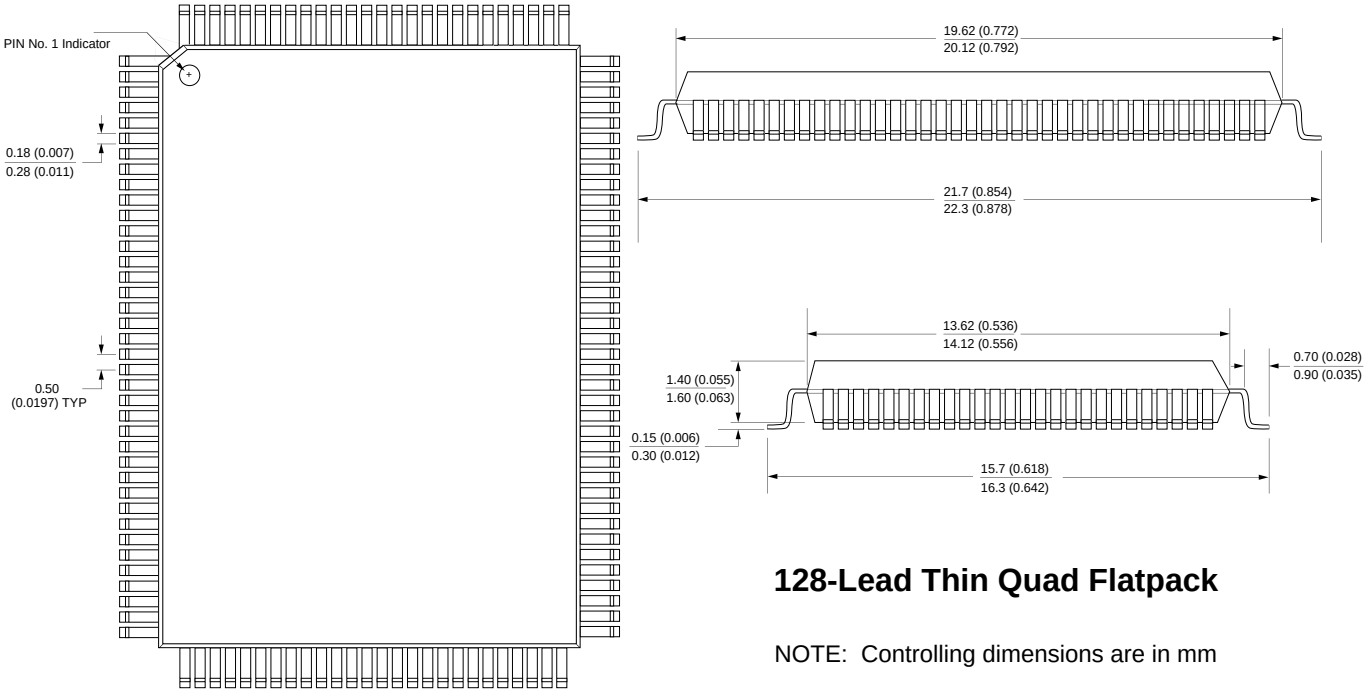


Package Information



120-Lead Thin Quad Flatpack

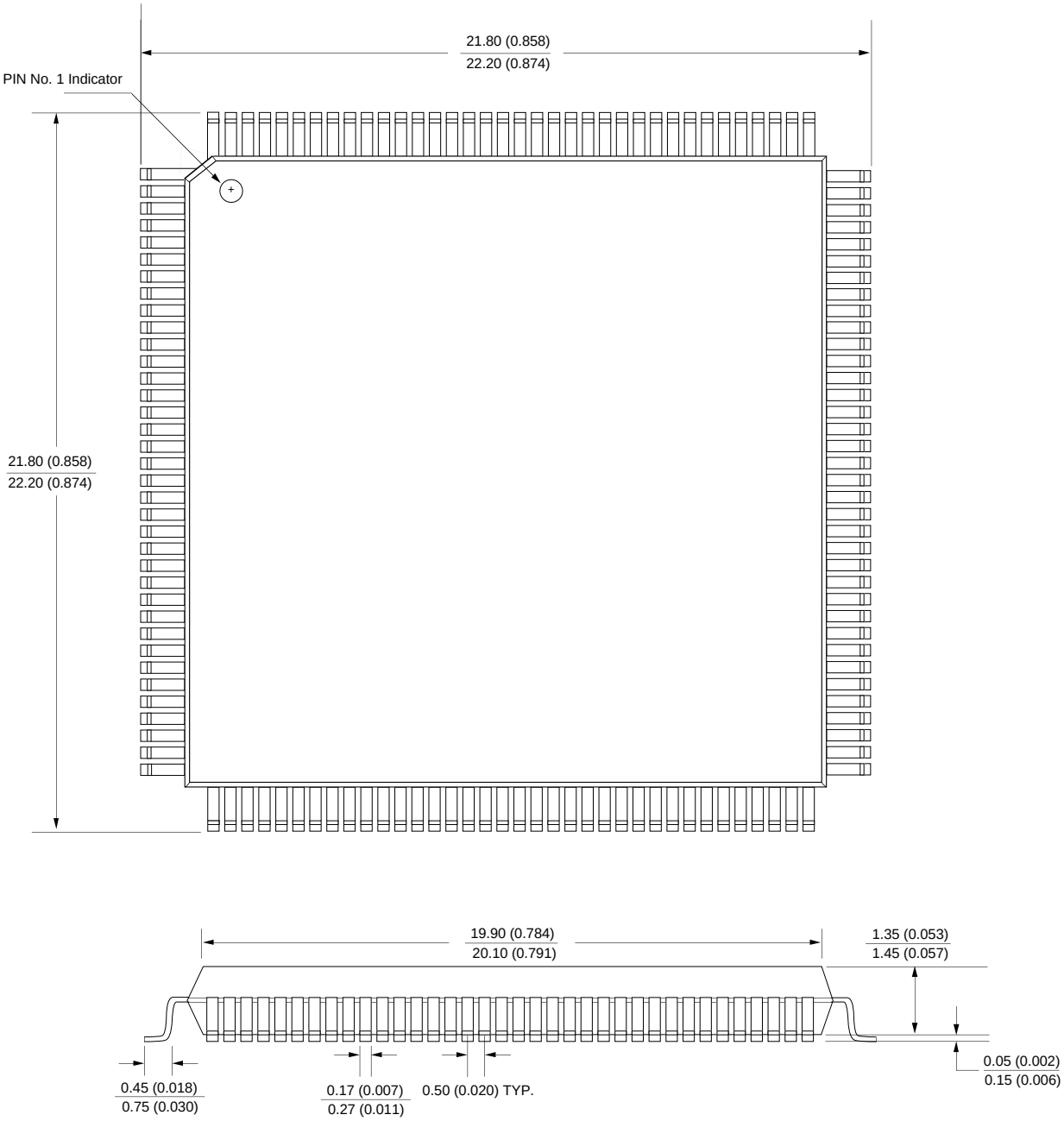
NOTE: Controlling dimensions are in mm



128-Lead Thin Quad Flatpack

NOTE: Controlling dimensions are in mm

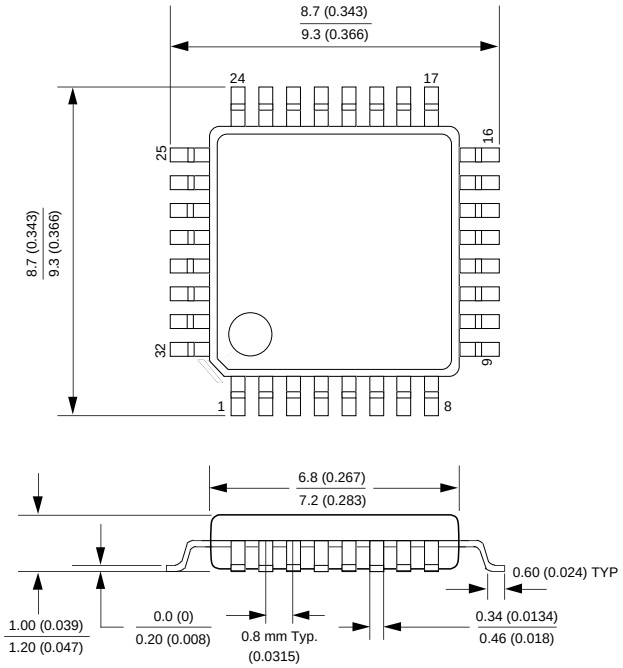
Package Information



144-Lead Thin Quad Flatpack

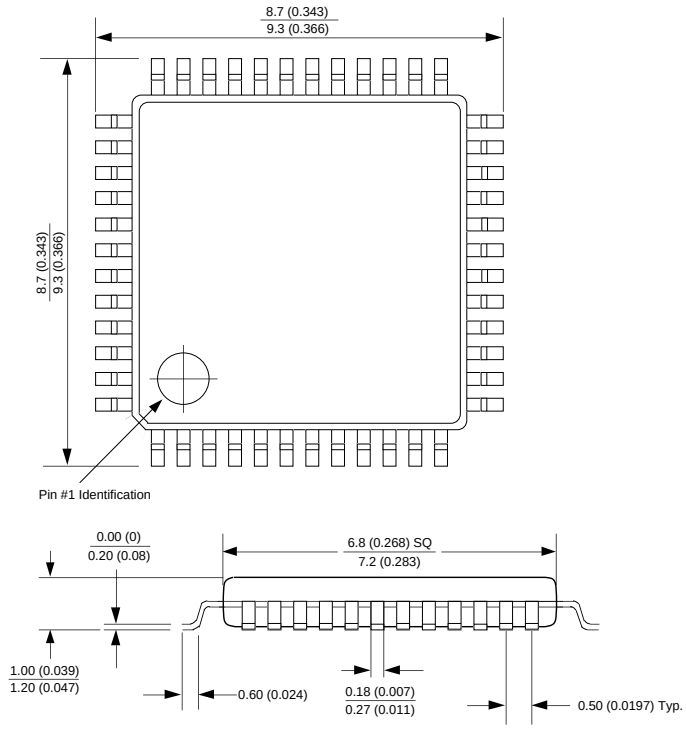
NOTE: Controlling dimensions are in mm

Package Information Very Thin Quad Flatpack (VTQFP)



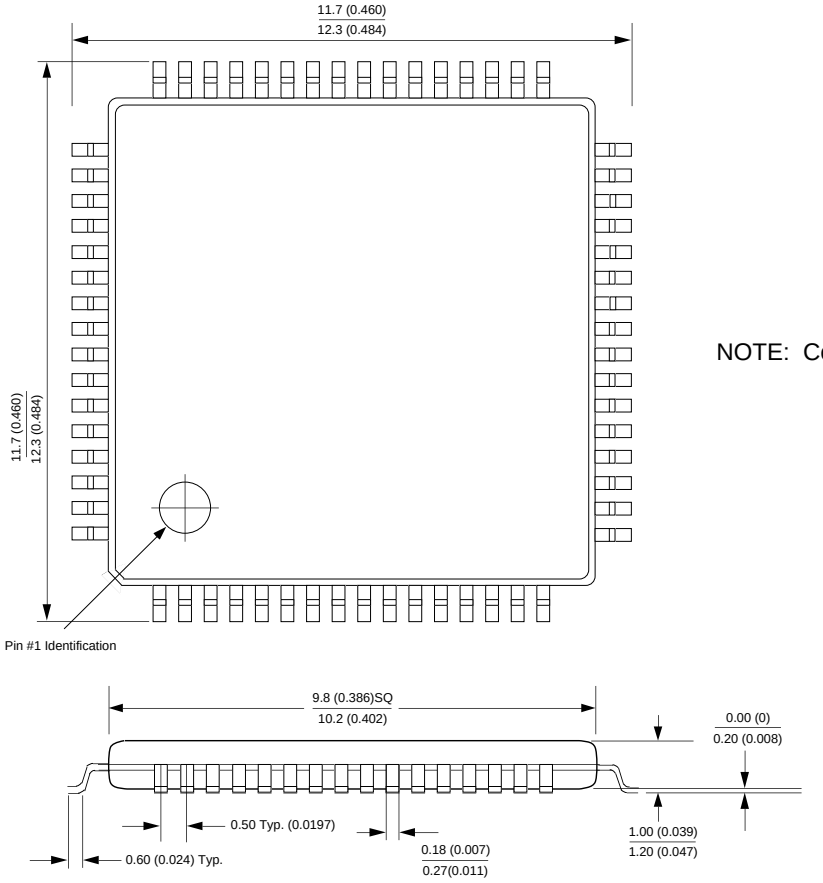
32-Lead VTQFP

NOTE: Controlling dimensions are in mm



48-Lead VTQFP

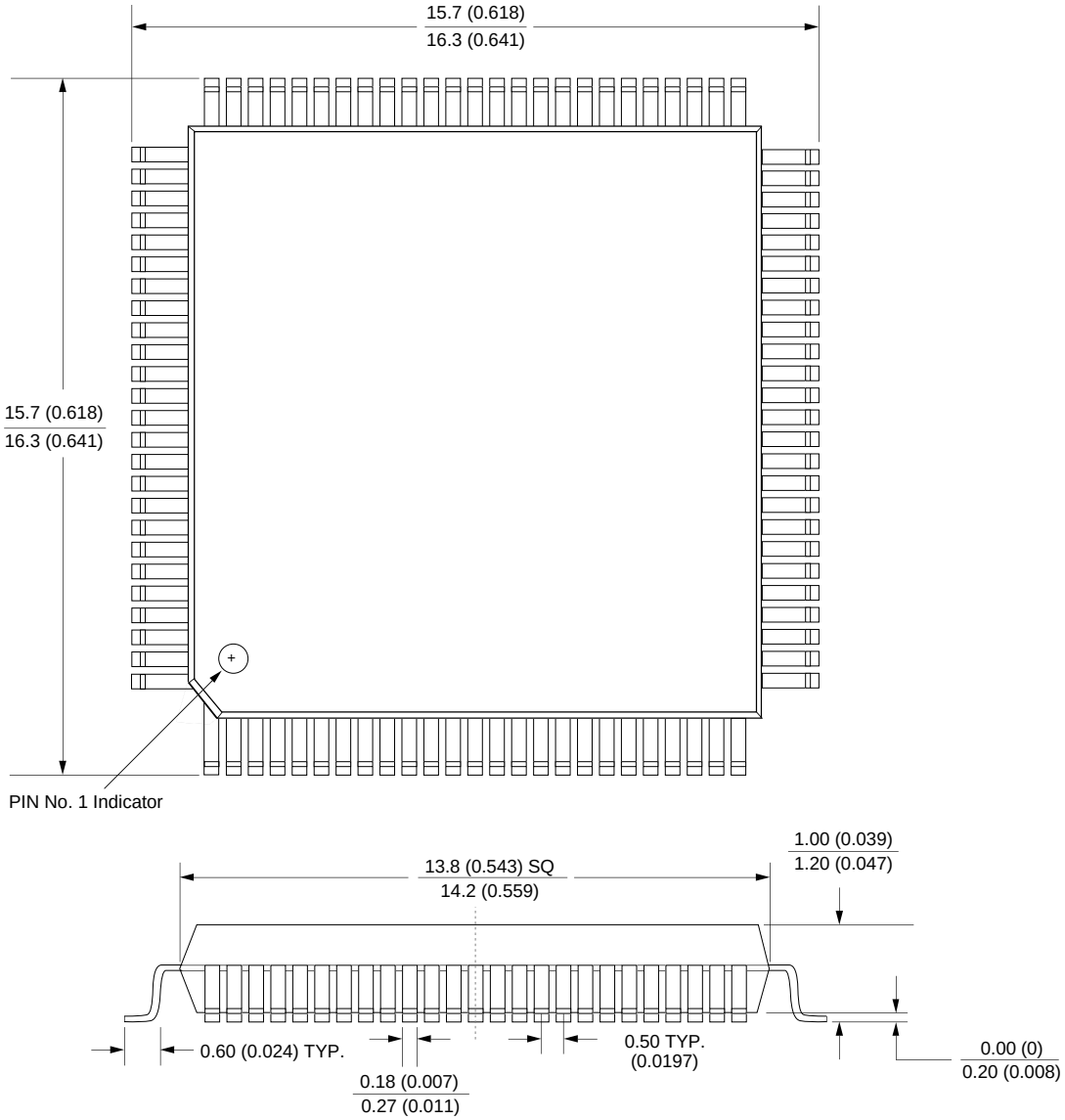
NOTE: Controlling dimensions are in mm



64-Lead VTQFP

NOTE: Controlling dimensions are in mm

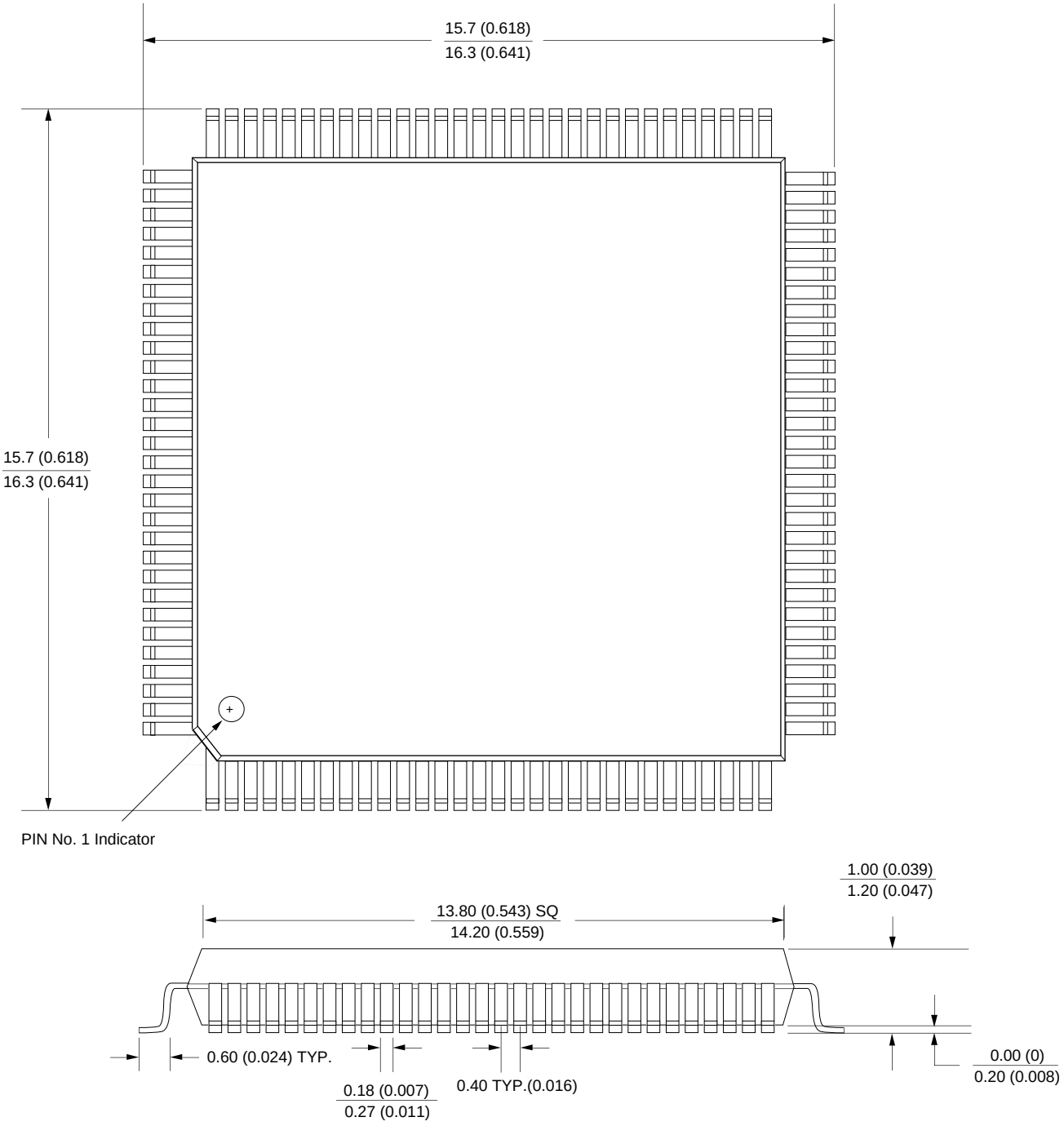
Package Information



100-Lead VTQFP

NOTE: Controlling dimensions are in mm

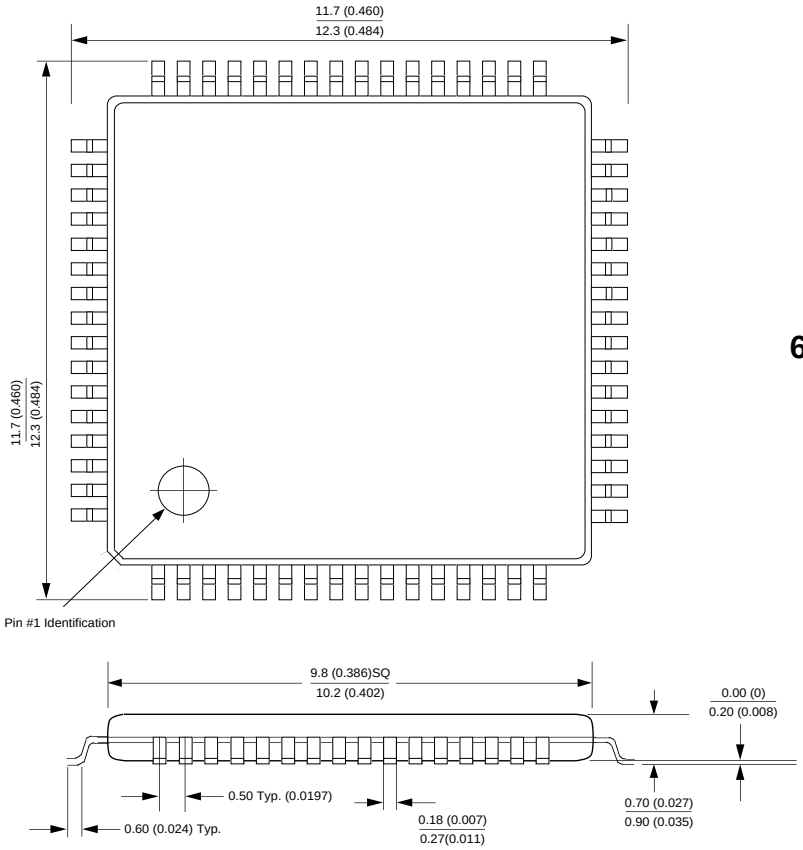
Package Information



120-Lead VTQFP

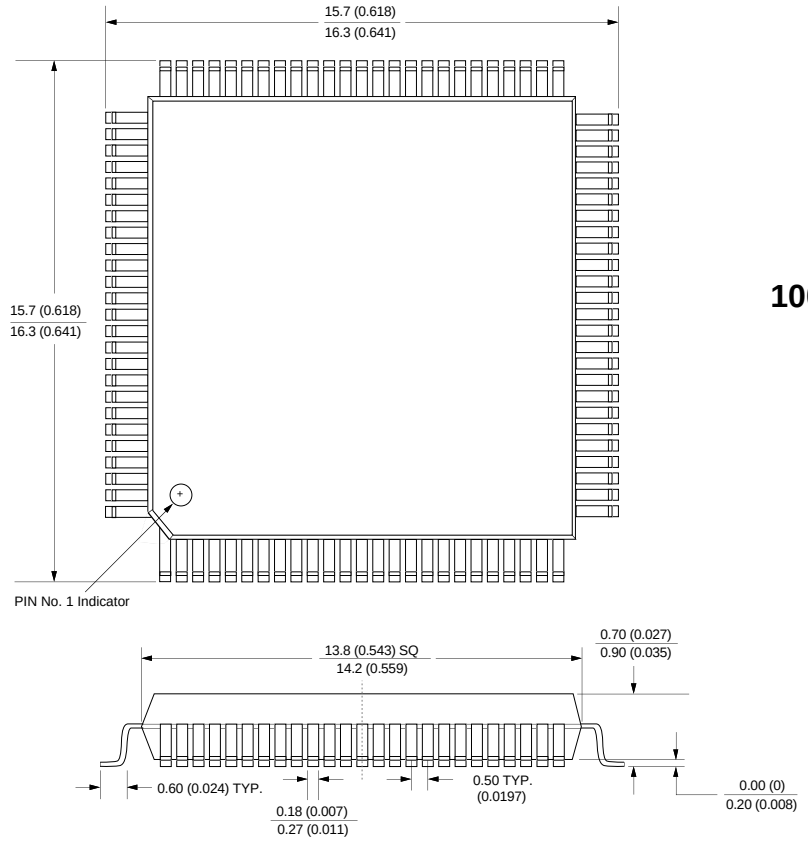
NOTE: Controlling dimensions are in mm

Package Information Ultra Thin Quad Flatpack (UTQFP)



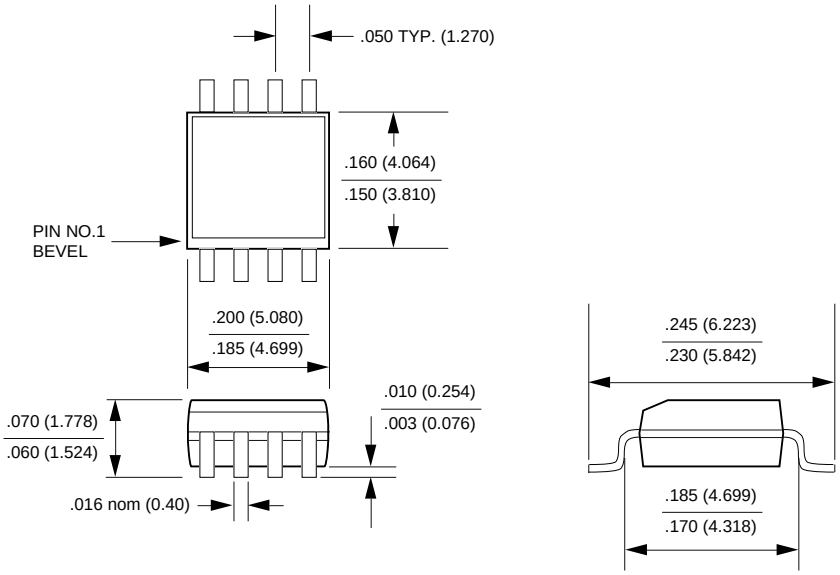
64-Lead Ultra Thin Quad Flatpack

NOTE: Controlling dimensions are in mm

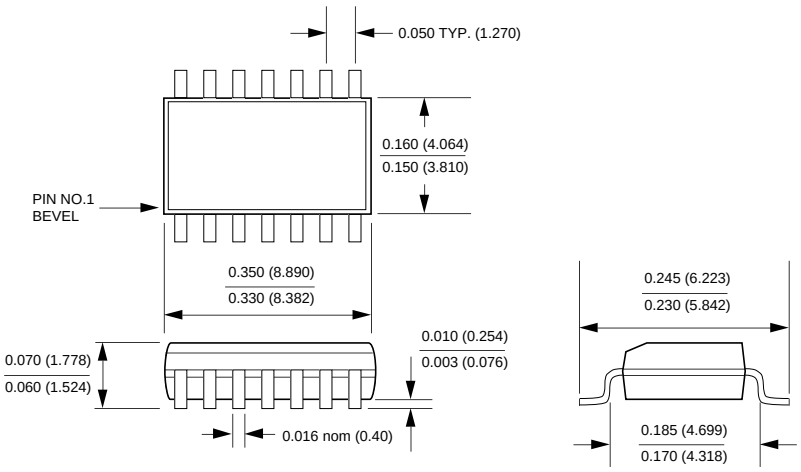


100-Lead Ultra Thin Quad Flatpack

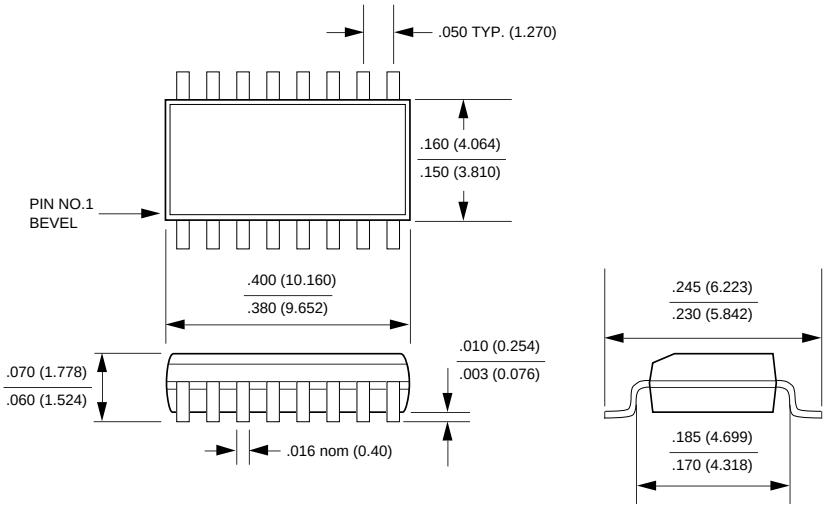
NOTE: Controlling dimensions are in mm



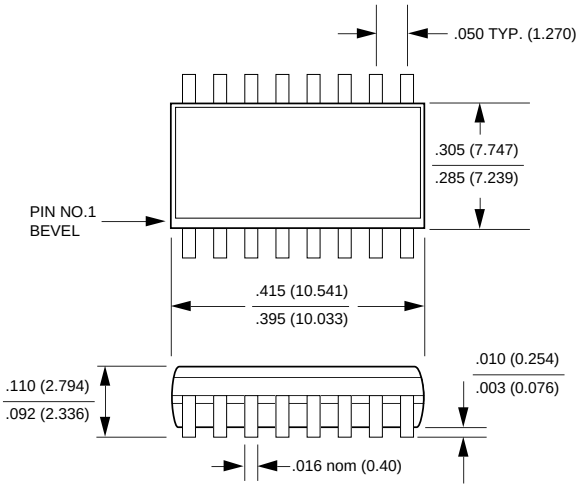
8-Lead SON



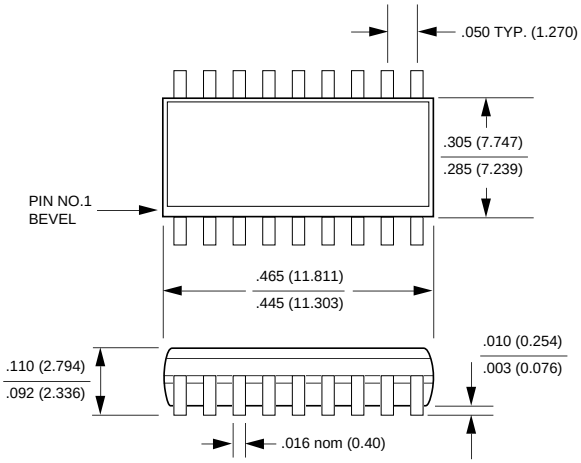
14-Lead SON



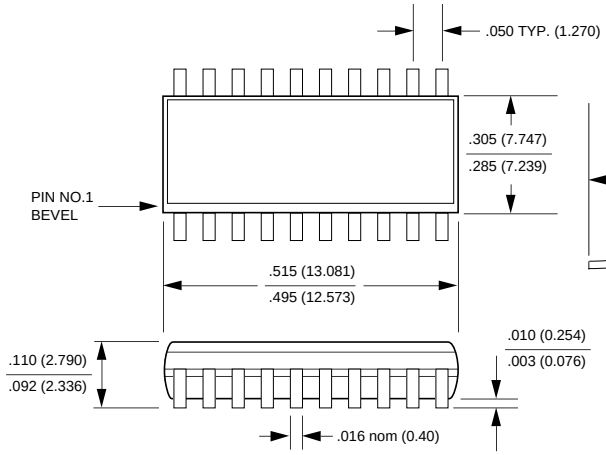
16-Lead SON



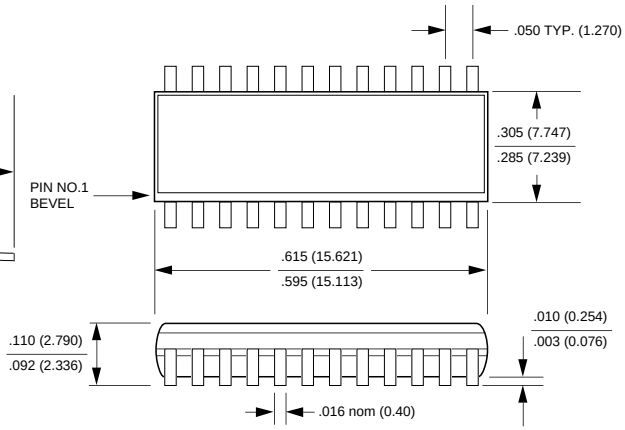
16-Lead SOL



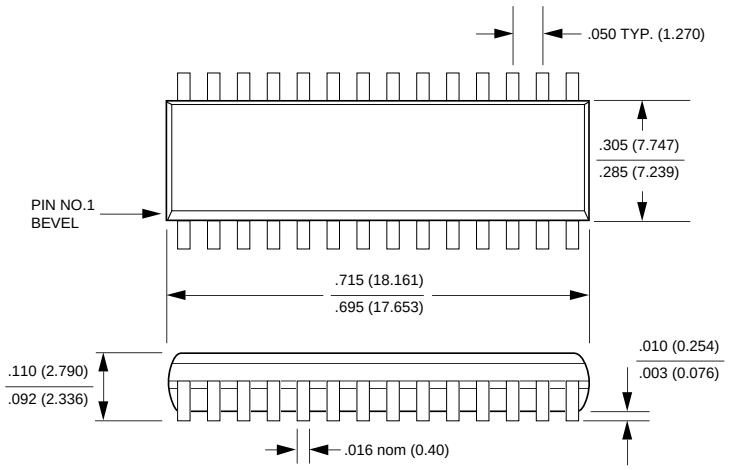
18-Lead SOL



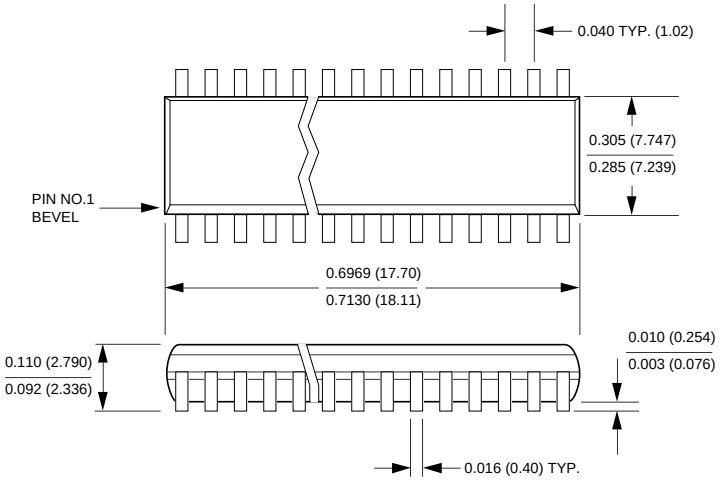
20-Lead SOL



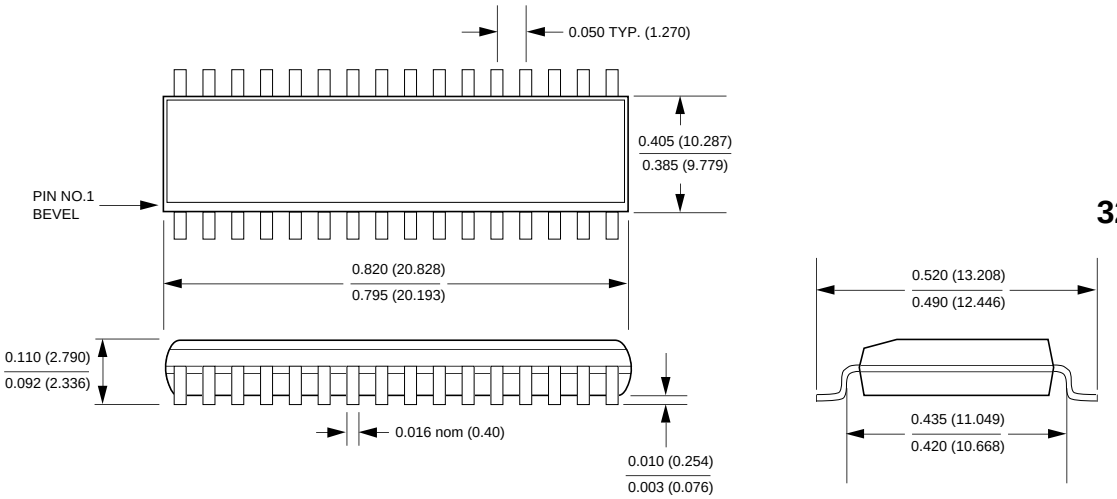
24-Lead SOL



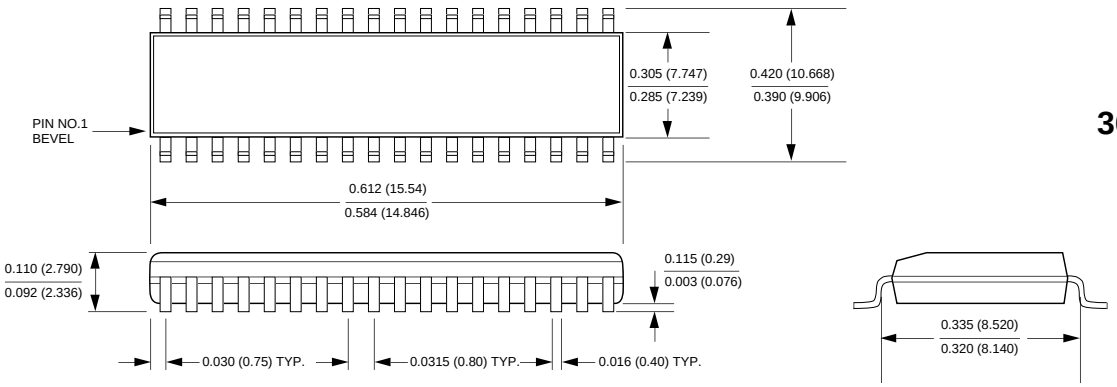
28-Lead SOL



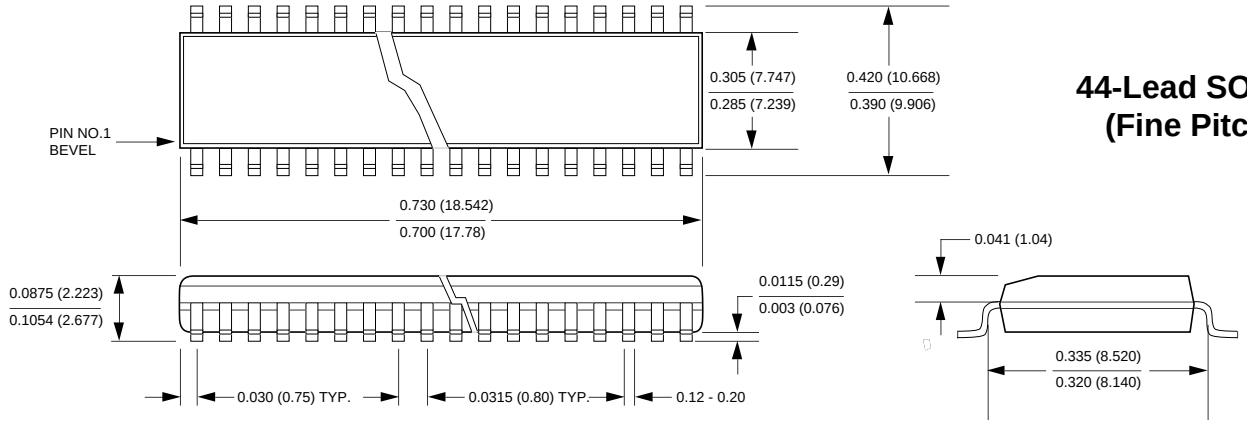
34-Lead SOL



32-Lead SOW



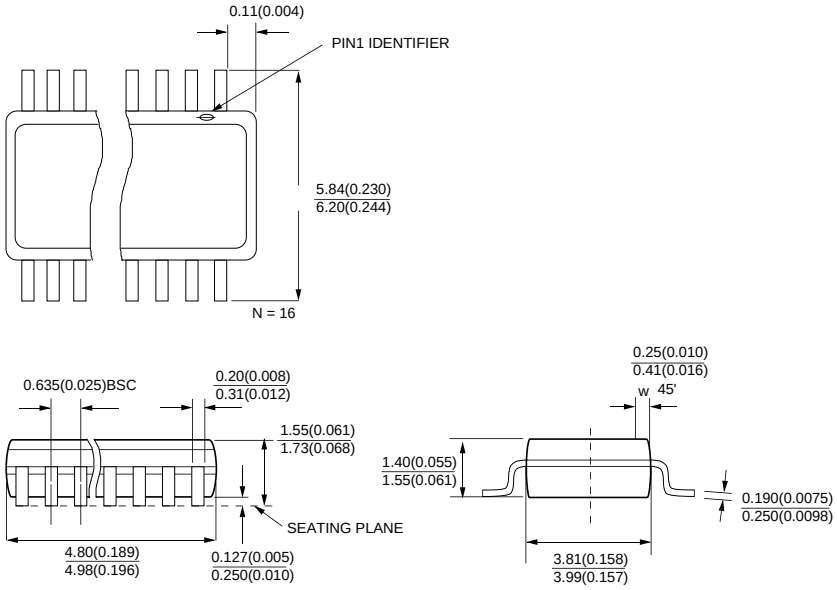
36-Lead SOM (Fine Pitch)



44-Lead SOM (Fine Pitch)

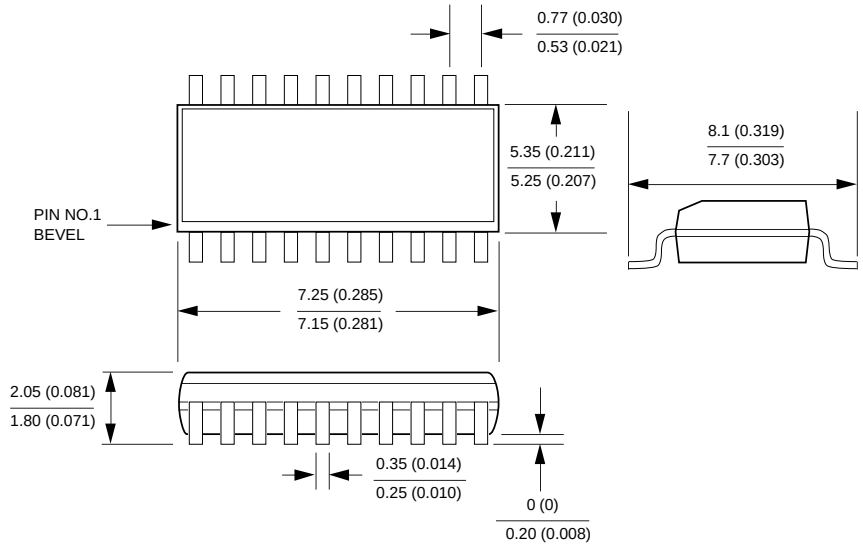
NOTE: Controlling dimensions are in mm

VSOP



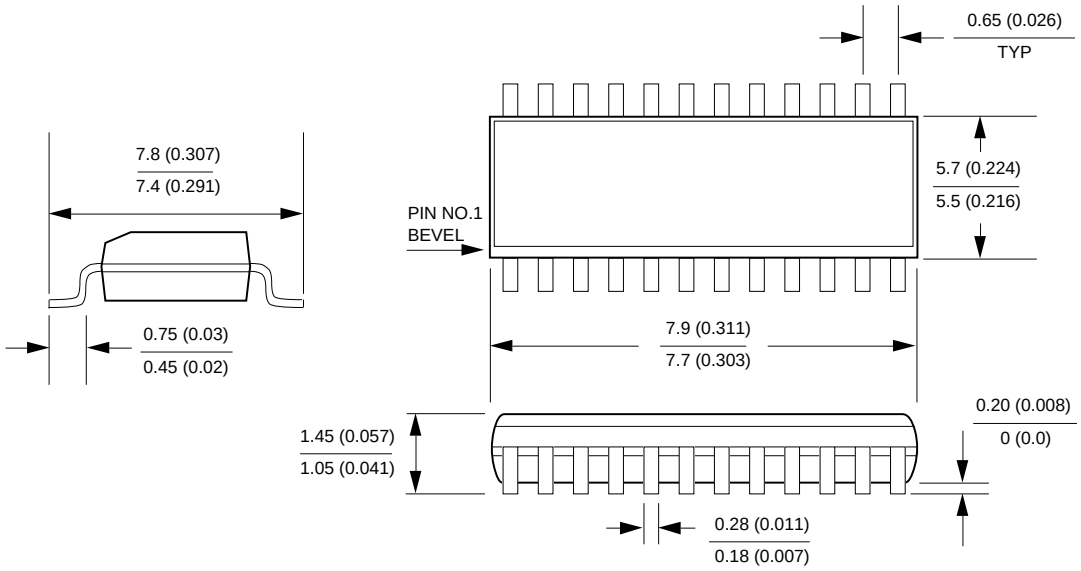
16-Lead VSOP

NOTE: Controlling dimensions are in mm



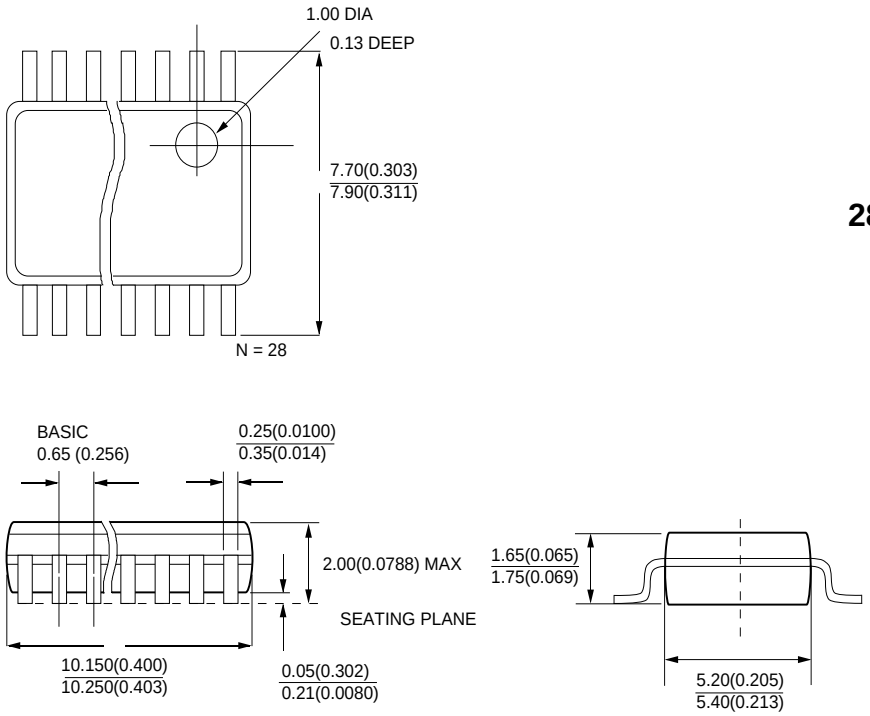
20-Lead VSOP

NOTE: Controlling dimensions are in mm



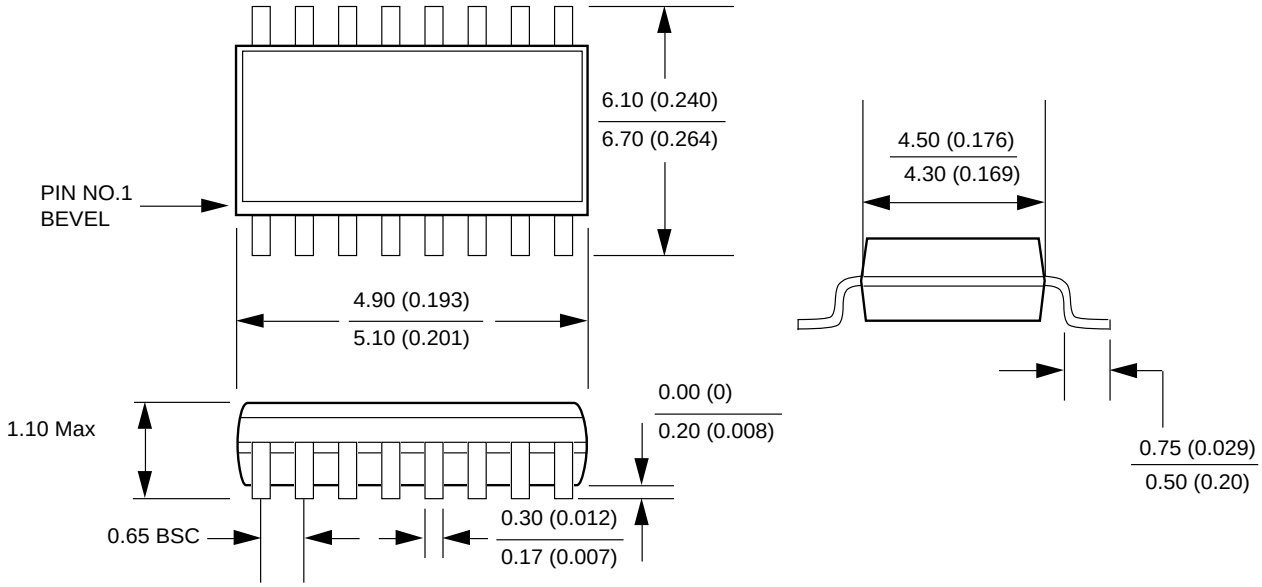
24-Lead VSOP

NOTE: Controlling dimensions are in mm



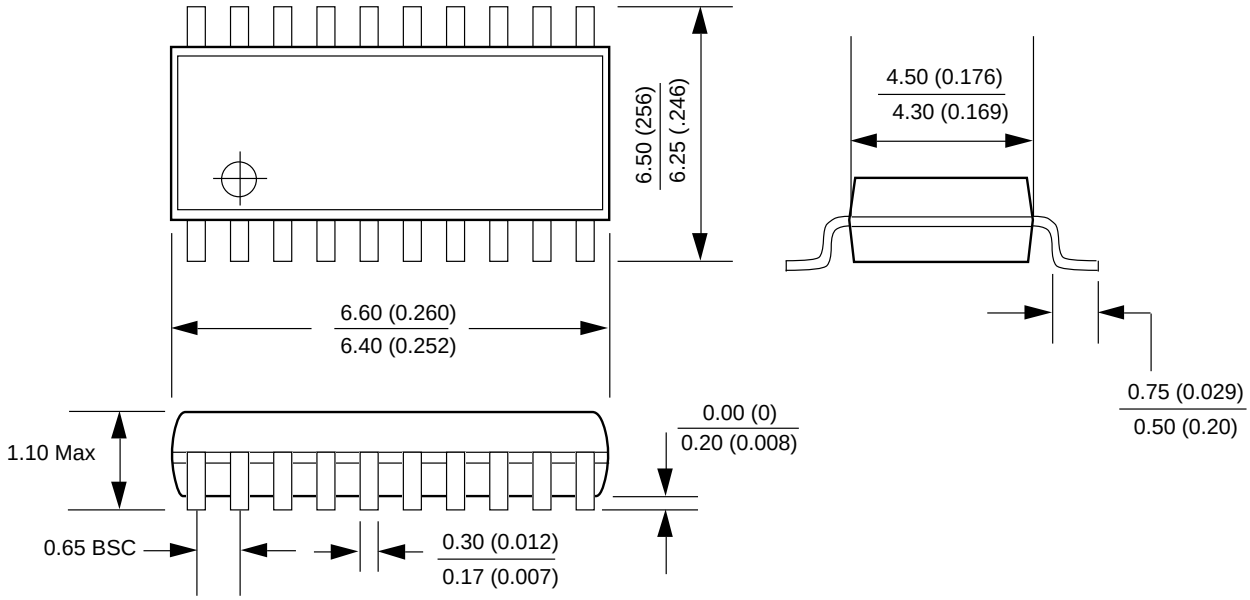
28-Lead VSOP

NOTE: Controlling dimensions are in mm



16-Lead VTSOP

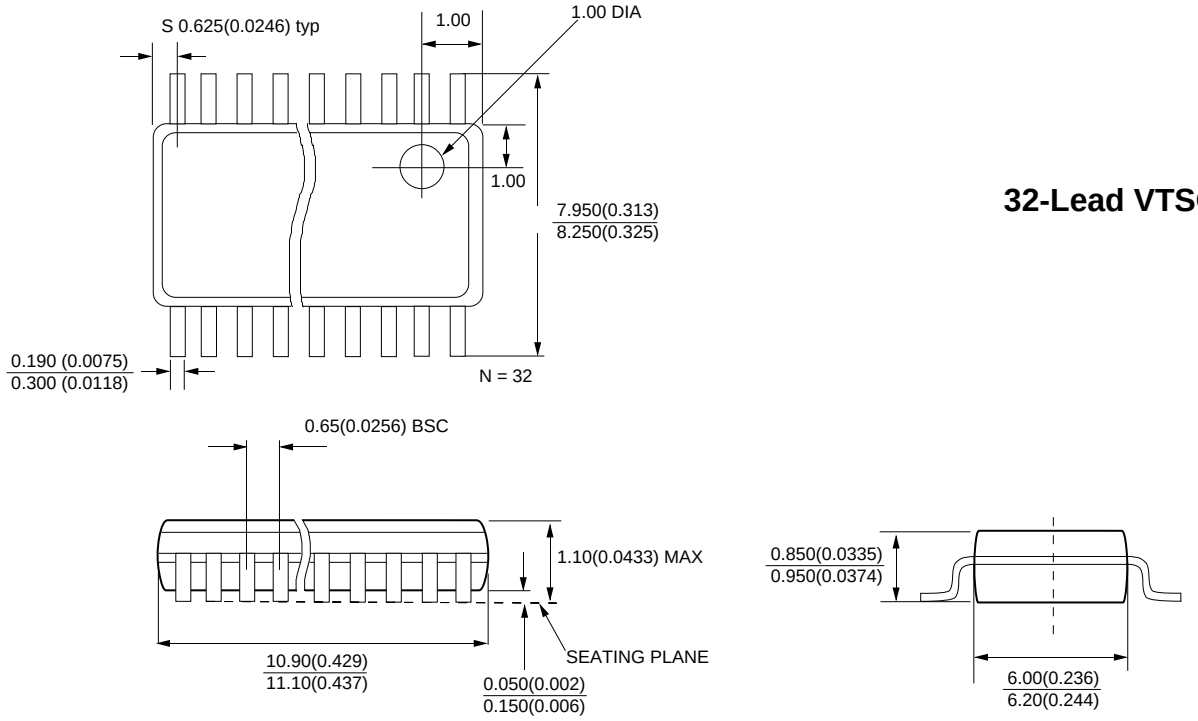
NOTE: Controlling dimensions are in mm



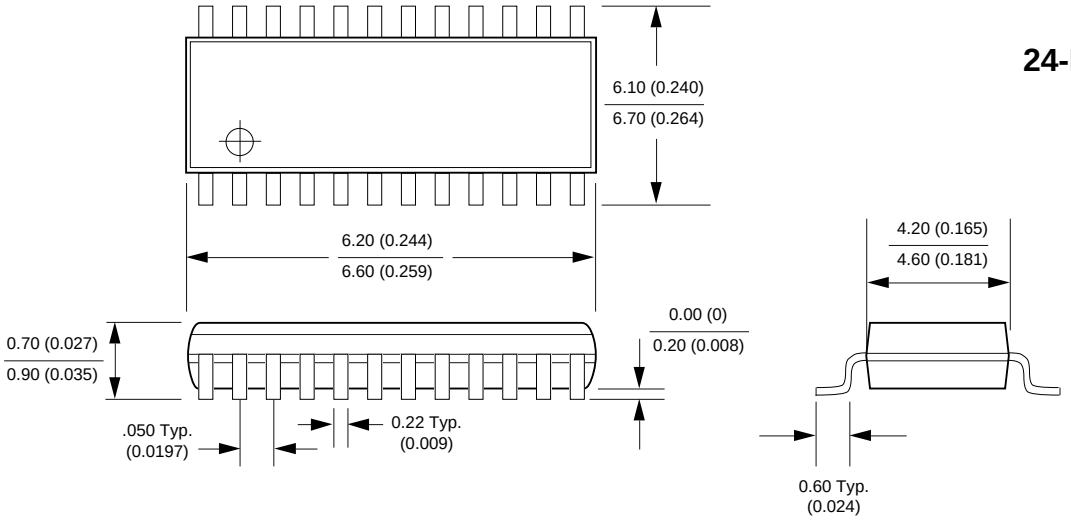
20-Lead VTSOP

NOTE: Controlling dimensions are in mm

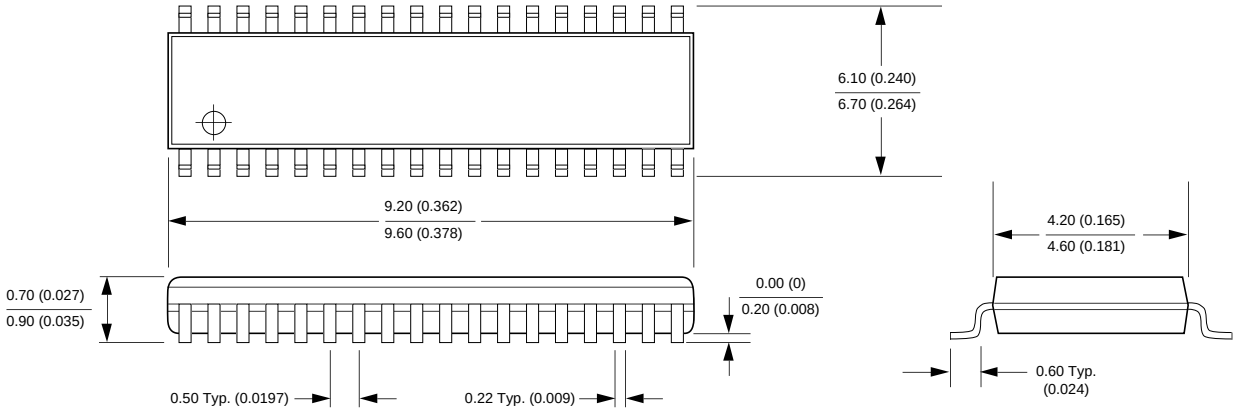
32-Lead VTSOP



24-Lead UTSOP



36-Lead UTSOP



Recommended Reflow Conditions

The following figures shown below are the recommended standard soldering conditions for Silicon Systems products. Recommended temperature profiles are specified using the upper limits of the surface temperature of the body. Actual soldering conditions should be determened as shown by the dotted line.

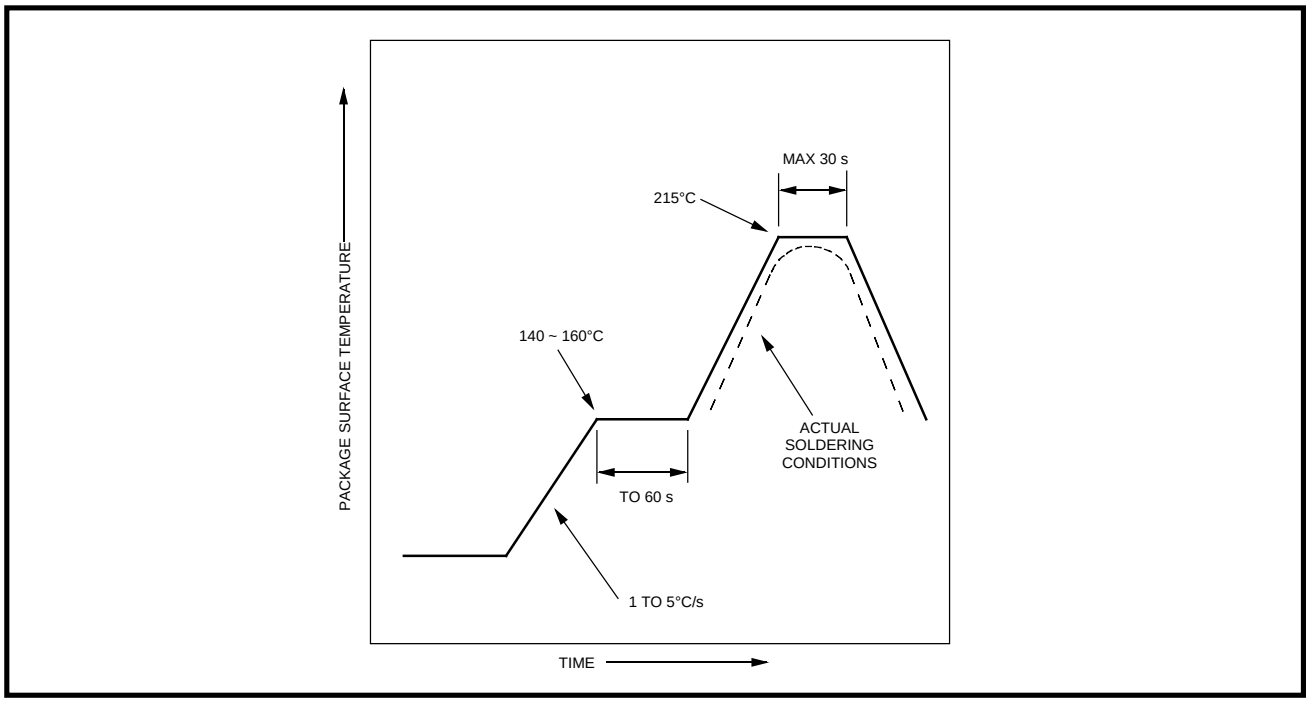


FIGURE A: Temperature Profile for VPS (Vapor Phase Reflow Soldering)

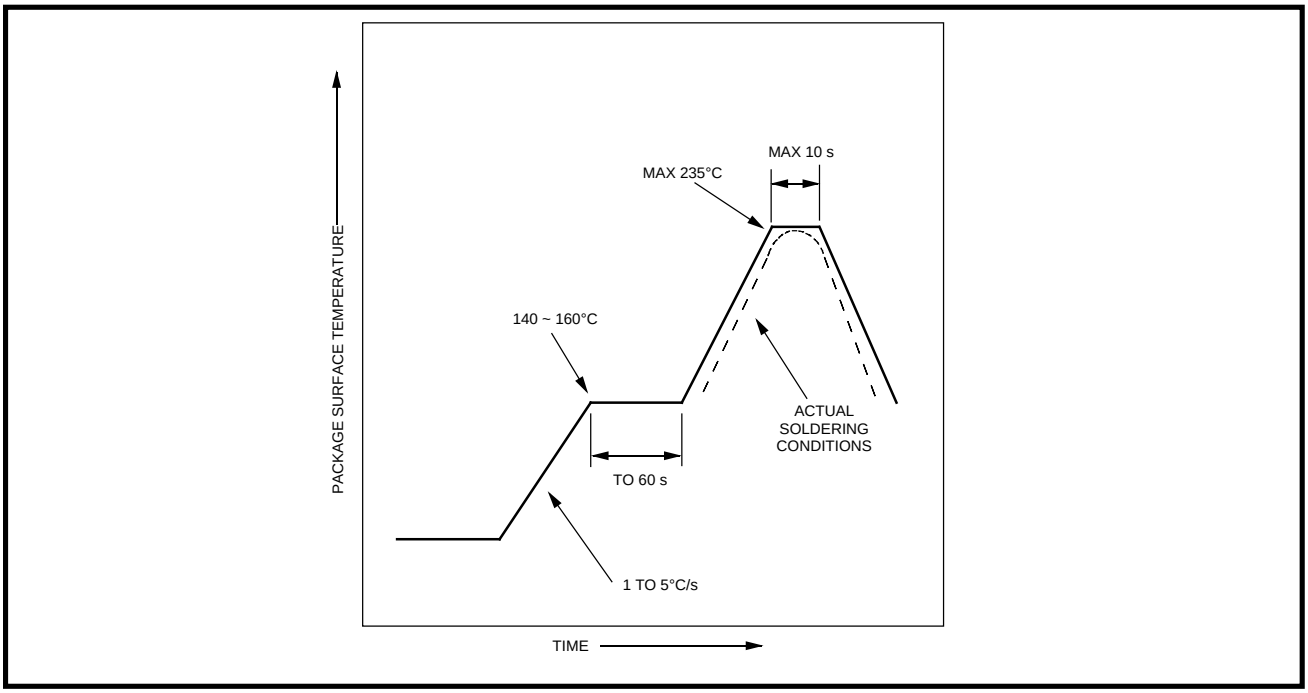
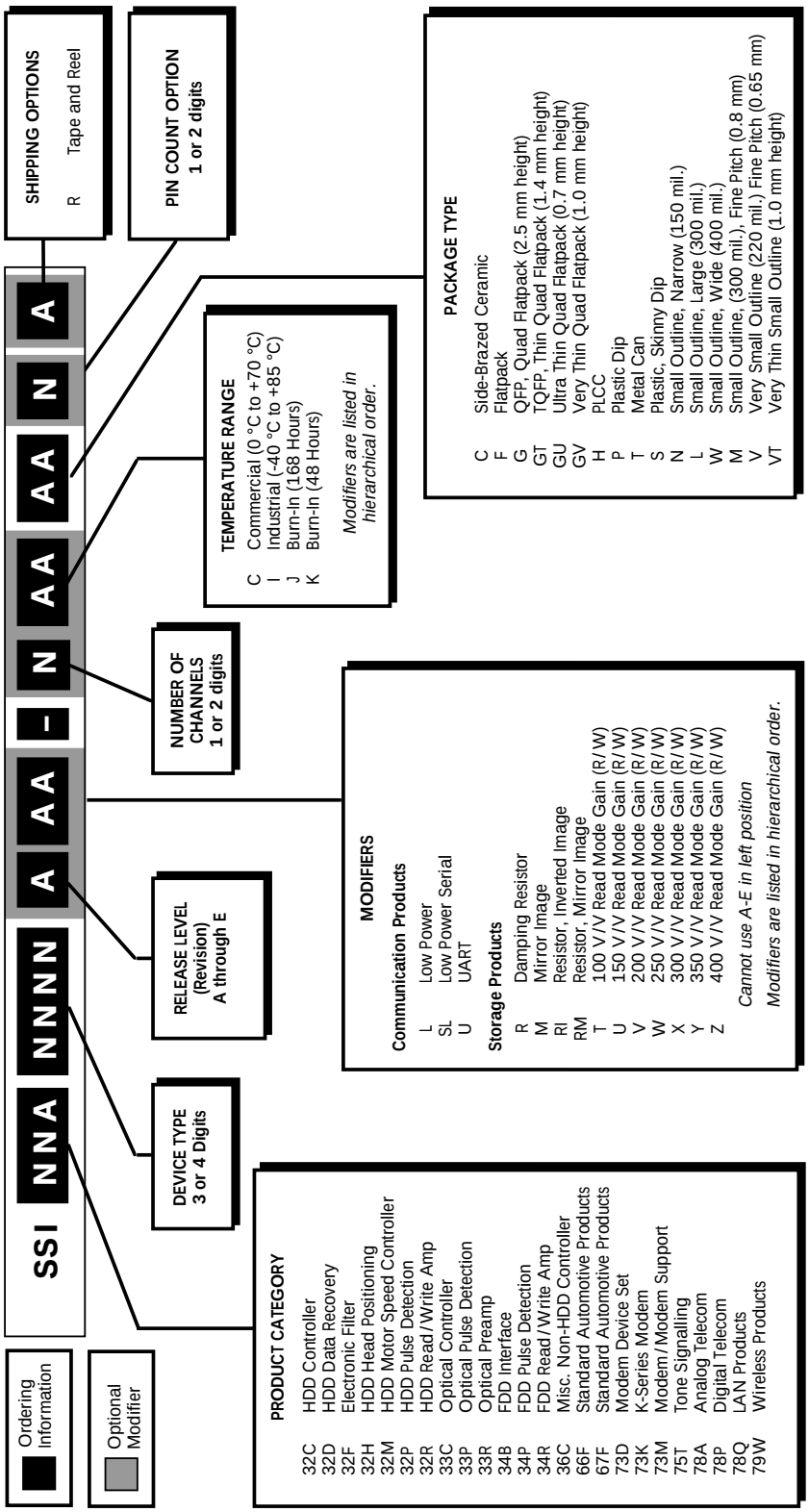


FIGURE B: Temperature Profile for Infrared Reflow Soldering


SSI NNA NNNN A AA – N AA AA N A
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32D HDD Data Recovery
32F Electronic Filter
32H HDD Head Positioning
32M HDD Motor Speed Controller
32P HDD Pulse Detection
32R HDD Read/Write Amp
33C Optical Controller
33P Optical Pulse Detection
33R Optical Preamp
34B FDD Interface
34P FDD Pulse Detection
34R FDD Read/Write Amp
36C Misc. Non-HDD Controller
66F Standard Automotive Products
67F Standard Automotive Products
73D Modem Device Set
73K K-Series Modem
73M Modem/Modem Support
75T Tone Signalling
78A Analog Telecom
78P Digital Telecom
78Q LAN Products
79W Wireless Products
DEVICE TYPE 3 or 4 Digits
RELEASE LEVEL (Revision) A through E
NUMBER OF CHANNELS 1 or 2 digits
MODIFIERS
Communication Products
L Low Power
SL Low Power Serial
U UART
Storage Products
R Damping Resistor
M Mirror Image
RI Resistor, Inverted Image
RM Resistor, Mirror Image
T 100 V/V Read Mode Gain (R/W)
U 150 V/V Read Mode Gain (R/W)
V 200 V/V Read Mode Gain (R/W)
W 250 V/V Read Mode Gain (R/W)
X 300 V/V Read Mode Gain (R/W)
Y 350 V/V Read Mode Gain (R/W)
Z 400 V/V Read Mode Gain (R/W)
Cannot use A-E in left position
Modifiers are listed in hierarchical order.
TEMPERATURE RANGE
C Commercial (0 °C to +70 °C)
I Industrial (-40 °C to +85 °C)
J Burn-In (168 Hours)
K Burn-In (48 Hours)
Modifiers are listed in hierarchical order.
PACKAGE TYPE
C Side-Brazed Ceramic
F Flatpack
G QFP, Quad Flatpack (2.5 mm height)
GT TQFP, Thin Quad Flatpack (1.4 mm height)
GU Ultra Thin Quad Flatpack (0.7 mm height)
GV Very Thin Quad Flatpack (1.0 mm height)
H PLCC
P Plastic Dip
T Metal Can
S Plastic, Skinny Dip
N Small Outline, Narrow (150 mil.)
L Small Outline, Large (300 mil.)
W Small Outline, Wide (400 mil.)
M Small Outline, (300 mil.), Fine Pitch (0.8 mm)
V Very Small Outline (220 mil.) Fine Pitch (0.65 mm)
VT Very Thin Small Outline (1.0 mm height)
PIN COUNT OPTION 1 or 2 digits
SHIPPING OPTIONS
R Tape and Reel

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Section 13

MANUALS

K-SERIES MODEM DESIGN MANUAL

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K-SERIES MODEM DESIGN MANUAL

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Section 1.0

DOCUMENT OVERVIEW

1.0. DOCUMENT OVERVIEW

1.1. OBJECTIVE

In publishing the K-Series Modem Design Manual, Silicon Systems is drawing together in one place a large body of applications literature for its K-Series family of single chip modem products. Our objective in doing this is to give maximum assistance to our customers in designing systems incorporating our products. Single chip modem design solutions are encouraging the use of data communication over the telephone network in an ever expanding range of new applications. This Manual is intended as a tutorial for those users who may be designing with modems for the first time, and also as a helpful guide for more experienced modem designers.

1.2. USE OF THIS DOCUMENT

The Silicon Systems K-Series Modem Design Manual is very likely the first attempt by a semiconductor company to set down a comprehensive guide to the design of modems using its products. Although the subject matter of this document is fairly sophisticated, an effort has been made to organize and present the material logically, providing cross–references, footnotes, a glossary, and a complete index to assist understanding and help the reader locate specific information.

We recommend, in addition to this manual, that you have at hand the most recent data sheet of the K-Series products that are of interest to you. Data sheets may be found in the current Silicon Systems Communication Products Data Book or can be obtained separately. Before beginning a particular product design, check with your local Silicon Systems Area Sales Office or the Applications Group in Tustin, CA, to make sure that you have the current version of the data sheet. If you are using a Silicon Systems Design Evaluation Kit (DEK) refer also to the User's Guide supplied with it for information that will not appear in this manual.

We want to forewarn you that from time to time we will be discussing some fairly esoteric design topics—many of which may not relate to your application. As you are reading through this manual you will have to do some evaluation as to whether or not the material is relevant to your requirement. Some of the more involved discussions relate only to higher data rate K-Series parts, and connection to modems outside your control. Also, if your product will be sold or used only within the U.S.A., much of what we have presented about the design of the international telephone line interface will not apply to your design. The U.S.A. has relatively lenient requirements for connection to the telephone network compared with other countries. We included this information, however, for the benefit of those designing high-speed, fully-featured modems for international use or sale.

1.3. LANGUAGE AND TERMINOLOGY

To a large extent, telecommunications, and by extension data communications, has developed terminologies distinct from the rest of the electronics engineering community. The lack of worldwide standards until recent years has also hampered the adoption of widely accepted terms. The U.S.A., dominated by the earlier influence of Bell Telephone, has developed terminology which differs from that now used by the CCITT, the industry group responsible for setting international standards. As international data exchange grows in importance, the CCITT can be expected to grow in influence, even in the U.S.A.; for this reason we have chosen to use the CCITT terminology in most cases. The glossary will assist you in cross-referencing certain terms with which you may be unfamiliar, and an attempt has been made to frequently define terms before they are used. There will be some exceptions to our use of CCITT terms. For example, "mark" and "space" are much shorter than "binary one" and "binary zero" and these have been used where appropriate. Also, we may use Bell terminology when discussing Bell specifications. The U.S.A. terminology is so pervasive that it is used by default in areas where the CCITT has yet to venture.

We also want to draw attention in this section to the popular misuse of two data communications terms. We will try to use the correct term in this manual, although in speech we often fall prey to bad habits as does the industry at large. First, a baud is not the same as a bit–per–second. The glossary clarifies these two terms, but here we will almost always be concerned with the data rate, which is measured in bits-per-second (bit/s). Secondly, the serial data transfer format commonly known as "asynchronous" is more properly termed "character–asynchronous." Again the glossary clearly explains the distinction. This point is important because in frequency-shift keying (FSK) modes, data transfer via modem is truly asynchronous. Instead of character- asynchronous, the CCITT uses the shorter but less clear term "start/stop" and we may also use this alternative.

1.4. REGISTERED TRADEMARKS

Throughout this Design Manual, we wish to acknowledge the following: Hayes, Hayes AT, Smartcom and Smartmodem are registered trademarks of Hayes Microcomputer Products; IBM, IBM PC, IBM AT and PS/2 are registered trademarks of International Business Machines; Microcom, MNP and Microcom Networking Protocol are registered trademarks of Microcom, inc; Tri–state is a registered trademark of National Semiconductor Corporation; Walkman is a registered trademark of Sony Corporation.

1.5. COPYRIGHT

Section 2.0

K-SERIES OVERVIEW

2.0. K-SERIES OVERVIEW

The Silicon Systems K-Series modem ICs incorporate all the signal processing functions needed to implement a modem for use with the general switched telephone network. In addition to the K-Series part, a complete system will require a control microprocessor (which may already be present) and a telephone line interface. An SSI Companion Controller may be used in place of the Control Microprocessor to eliminate the need for actual software development. Most K-Series ICs are available in 28-pin DIP or PLCC (surface mount) packages. Integral Universal Asynchronous Receiver-Transmitter versions are in 40-pin DIP and 44-lead PLCC packages. Versions with only the serial control interface are available in narrower 22-pin, 0.4" wide DIP packages for use with through-hole circuit boards.

2.1. IMPORTANT FEATURES

Each member of the K-Series family is a single chip integrated circuit designed to be used in a system which incorporates a microprocessor or microcontroller. This controller programs the chip through a set of registers and similarly reads back the chip status. Under this control, the modem IC performs dial tone detection, Dual Tone Multi–Frequency dialing, call progress tone detection, answer tone generation and detection, handshaking between modems, and data transfer. Each part in the family supports a number of modulation modes which conform to established Bell standards and / or CCITT recommendations. This ensures that K-Series modems can exchange data with a large installed base of modems throughout the world. Data can be transferred in character asynchronous format in all modulation standards and also in bit synchronous format in synchronous (DPSK and QAM) standards. (See 4.1.4 and 4.1.5.)

2.2. COMMON FAMILY CHARACTERISTICS AND COMPATIBILITY

A unique feature of the Silicon Systems K-Series modem ICs is pin-for-pin and control register compatibility between family members. This means that you can preserve your investment in hardware and software design while changing the modem standards and speeds supported to meet the demands of new applications. The K-Series family can be divided into sub-families which may operate from different supply voltages, use different control interface structures or include additional features on-chip. Obviously, parts cannot be exchanged between these families without hardware changes. However, within families, there are versions which support different groups of modulation standards. These can be exchanged with few or no changes to the hardware and, in many cases, few changes to the controller software also. As one of the internal registers contains an identification code, software can be written to work with different Silicon Systems products and to automatically sense which is connected. A uniform register structure across the entire family makes sure that software written to control one family member can be easily used with another. You will find a full discussion of this subject in section 7.1.1, K–Series Registers and Designing for Interchangeability. Even the difference between the bus control interface and the serial control interface can be accounted for in a few subroutines. Note, however, that when upgrading a product with a chip that supports new modulation modes, (for example upgrading a 1200 bit / s product to 2400 bit / s) the controller firmware must be reviewed and support added for the new mode.

2.3. 12 VOLT SUPPLY K-SERIES MODEM ICs

K-Series parts with no suffix on the part number, for example the SSI 73K222, are designed to operate from a single 12 volt supply.

2.4. 5 VOLT, LOW POWER VERSIONS

K-Series parts with an “L” suffix on the part number, for example the SSI 73K222L, are designed to operate from a single 5 volt supply and consume significantly less power than the 12 volt equivalent.

2.5. VERSIONS WITH INTEGRAL UART

K-Series parts with a “U” suffix on the part number, for example the SSI 73K222U, have a 16450 compatible UART integrated on chip. Because the UART requires a normal logic supply, these family members also operate from a single 5 volt supply.

Section 3.0

K-SERIES PRODUCT SELECTION AND COMPARISON CHARTS

3.0. K-SERIES PRODUCT SELECTION AND COMPARISON CHARTS

The part numbers of Silicon Systems K-Series modem ICs have been devised to make it easy for you to choose the product best suited to your application. The "SSI 73K" at the start of the part number indicates that the component is a member of the K-Series family. The next three digits indicate the modulation standards supported as described in section 3.1. After these three digits, there may be "L," "S," "SL," or "U." This letter, or its absence, indicates the hardware configuration in which the part will work. The letter "L" means 5V supply, "S" indicates a serial control only version and "U" means integral UART. Next comes a dash ("-"), then the temperature range which will be "I" for industrial (-40 to +85°C) or "C" for commercial (0 to 70 °C). Finally, the last letter is the package style, "P" for plastic DIP, "C" for ceramic DIP and "H" for plastic leaded chip carrier (PLCC). Package markings differ from the part number only in that the "SSI" is omitted at the front.

Please note that Silicon Systems has previously used a numbering scheme in which the number of pins or leads on the package appeared after the dash. If you find references to products using this scheme, ignore the number if it is 28, 40 or 44. If the number is 22, this indicates a serial control interface only version, which is now denoted by an "S" before the dash as described above. The old product numbering scheme was discontinued after release of the 1989 Communication Products Data Book. Subsequent literature should reflect the correct marking.

3.1. SELECTION BY MODULATION STANDARDS SUPPORTED

Table 3-1 shows the relationship between the K-Series part numbers and the modulation standards they support. The Modulation Group column shows the three digits in the part number which follow the "SSI 73K" header. The Bell Standards and CCITT Recommendations columns are blocked if supported by a part and left blank if not supported. The DSP column indicates which groups use a chip which has a DSP (Digital Signal Processor). You will notice that the presence of a DSP corresponds to 2400 bit/s capability (V.22bis). An adaptive equalizer is implemented in the DSP to allow operation at this higher data rate. Because this feature is also used at 1200 bit/s for V.22 (see CCITT) and Bell 212A operation, the performance of the DSP parts is typically better than the non-DSP parts in these modes. Thus, you may choose, for example, the 73K224L over the 73K222L to get the lowest error rates over poor quality telephone circuits.

Please note that we offer a number of products in each modulation group, representing the different combinations of hardware design features listed below. However, not every combination is available in all the groups. For example, at present the 73K224L has no 22-pin serial control interface only version. (The serial control mode is nevertheless available on the 28-pin part.) Consult a Silicon Systems sales representative for up-to-date availability information.

Modulation Group	On-Chip DSP?	Bell Standards			CCITT Recommendations			
		103	202	212A	V.21	V.23	V.22	V.22bis
73K212	NO	■		■				
73K221	NO				■		■	
73K222	NO	■		■	■		■	
73K224	YES	■		■	■		■	■
73K302	NO	■	■	■				
73K312	NO	■	■		■	■		
73K321	NO				■	■		
73K322	NO				■	■	■	
73K324	YES			■	■	■	■	■

TABLE 3 – 1: K-Series ICs – Modulation Standards Supported

3.2. SELECTION BY HARDWARE DESIGN FACTORS

There are three factors you should consider in choosing a K-Series part, and these relate to the hardware used in your system. First, do you want the modem to operate from a 5V or a 12V supply? Second, is there a need for a UART in the system? Third, do you want to use a parallel (bus) or a serial control interface?

3.2.1. 5V or 12V Power Supply

The choice of power supply voltage will probably depend on what is available elsewhere in your system. As we develop higher speed modem ICs, we may use new process technologies which will make it difficult or impossible to continue the 12V versions of these new parts. Thus if you are hoping to use higher data rates at some time with minimal hardware design changes, you may want to use the 5V parts. The 5V parts consume considerably less power and are the obvious choice for power sensitive applications. They are also suited for systems where no supply voltage above 5V is to be provided, however, in this situation the design of the interface to the telephone line becomes more difficult. To get the best signal-to-noise ratios, we have designed both the 12V and 5V versions to use analog signal levels close to the maximum swing between power and ground. Thus, the gain required in the external telephone line interface components is different. 12V parts require a 10 dB loss in the transmit path to the telephone line and a 9 dB gain in the receive path. 5V versions require no loss in the transmit path and only 2 dB of gain in the receive. With a supply of only 5V it is not possible to get enough signal amplitude from a simple buffer amplifier to drive the line-coupling transformer through its matching resistor to the required level. Thus it may become necessary to use a bridged configuration of two amplifiers, which complicates the design. If you have positive and negative supplies in your system you should use them for the amplifiers in the telephone line interface even if you are using a 5V modem IC.

3.2.2. UART Requirement

Most modem systems need a UART somewhere to convert the data for transmission from the parallel format in which it is stored into the serial format for transmission. Even if this is done outside your equipment, it may be necessary to monitor the serial data stream to look for embedded commands. Some members of the K-Series family are available with an 8250 / 16C450 compatible UART integrated onto the chip. These are packaged in a 40-pin DIP or 44-lead PLCC and are only available for 5V supply operation. As well as the UART, some other additional functions are included with the modem. A speaker amplifier with programmable gain allows audio monitoring of the signals on the telephone line. An “off-hook” output and a “ring-indicator” input form part of the control to the telephone line interface so that microcontroller ports need not be used for these functions. Also, a bridged driver amplifier is included to supply the necessary drive to the line-coupling transformer and its matching resistor without external op-amps.

3.2.3. Parallel or Serial Control Interface

The basic design of the K-Series modem IC requires a microcontroller to read and write a number of 8-bit internal registers. Thus, the natural control interface is over an 8-bit multiplexed address / data bus. Each control and status register has a separate address and can be written or read as an I/O or memory location. However, if desired, the K-Series modems can be controlled over a seven-wire serial interface. This is useful where the microcontroller bus is not available externally or is non-multiplexed. Also, for those wanting a smaller DIP-style package, some K-Series parts are available in a 22-pin, 0.4" wide DIP which makes only the serial control interface available. The 28-pin package versions can also be operated in the serial control mode by tying the ALE address latch enable (ALE) pin HIGH and the chip select (CS) pin LOW.

The integral UART versions have two modes of control interface operation. The UART control and status registers are always available over an 8-bit, 8250-like control bus. In the Standalone or Single Port mode, when STNDLN is tied HIGH, the modem control interface is also available over this bus. In the non-standalone or Dual Port mode, when the STNDLN pin is LOW, a separate serial control interface is used to control the modem.

Table 3-2 summarizes the availability of parts in the various hardware configurations for each group of modulation standards. The columns describe the package options, which include the availability of control interface options and the integral UART. Each box is marked with the part number if a part is available in that combination or planned for the near future. The part is for 5V operation if there is an “L” or a “U” after the three digit group number and 12V otherwise. Blank boxes indicate that a part is not available or planned at the time of writing, but check with the Silicon Systems Sales and Marketing organization for up-to-date information and additional products not shown. Special versions of all products may be made available to volume customers.

The 73K224L has been offered in 44-, 32- and 28- (Fall 91) lead PLCCs for surface mount applications. The pinout of the 44- and 32-lead versions has been arranged with the unused pins at the corners. By extending the copper lands under the package, it is possible to accommodate 28-, 32- and 44- or just 28-, 32-lead PLCC K-Series parts on the same printed circuit boards. Note that extending the lands may give problems for your inspection department because they will not be able to check for solder bridges under the chip. You may prefer to design for the 32-lead package and change to the 28-lead package by a slight alteration to the artwork of the component side of the board.

Modulation Group	Bus or Serial Control			Serial only	Integral UART	
	28 pin DIP	28 lead PLCC	44 or 32 lead PLCC	22 pin DIP	40 pin DIP	44 lead PLCC
73K212	73K212-IP 73K212L-IP	73K212-IH 73K212L-IH	N/A	73K212S-IP 73K212SL-IP		
73K221	73K221-IP 73K221L-IP	73K221-IH 73K221L-IH	N/A	73K221S-IP 73K221SL-IP		
73K222	73K222-IP 73K222L-IP	73K222-IH 73K222L-IH	N/A	73K222S-IP 73K222SL-IP	73K222U-IP	73K222U-IH
73K224	73K224L-CP	73K224L-CH	73K224L-CH	73K224SL-IP*		
73K302	73K302L-IP	73K302L-IH	N/A	73K302SL-IP		
73K312	73K312L-IP	73K312L-IH	N/A	73K312L-IP		
73K321	73K321L-IP	73K321L-IH	N/A	73K321SL-IP		
73K322	73K322L-IP	73K322L-IH	N/A	73K322SL-IP		
73K324	73K324L-IP	73K324L-IH		73K324SL-IP		
* Available Fall '91						

TABLE 3 – 2: Hardware Features

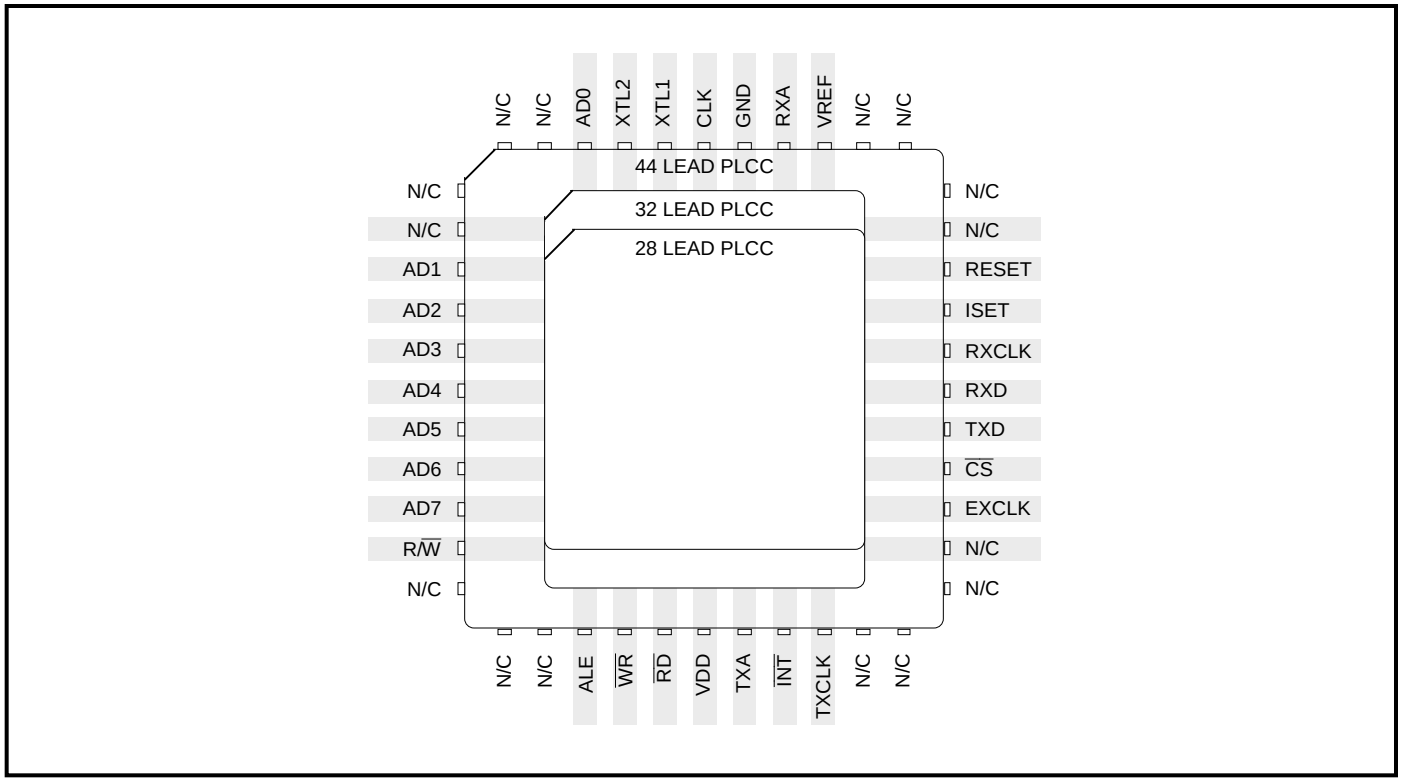

FIGURE 3 – 1: 44-, 32- and 28-Lead PLCC Compability

Section 4.0

OPERATION OF K-SERIES MODEM INTEGRATED CIRCUITS

4.0. OPERATION OF K-SERIES MODEM INTEGRATED CIRCUITS

4.1. DATA TRANSFER ACROSS THE TELEPHONE NETWORK

This section discusses how the K-Series modem ICs actually get data from one modem to another across a voiceband telephone connection. All parts operate in compliance with published data communications standards from Bell in the U.S.A. and the CCITT in Europe. Several different standards are supported by each member of the K–Series family, see K-Series Product Selection and Comparison Charts section for further information.

4.1.1. Full-Duplex Operation by Frequency Division Multiplexing

All K-Series modems are capable of passing data in both directions simultaneously over a single, two-wire telephone connection (full-duplex). This is achieved by dividing the available bandwidth into separate bands for data to flow in either direction. The signals are kept separate by filters in the transmitters and receivers to block any energy from the alternate band. This technique is known as frequency division multiplexing. Not all modulation schemes allocate the same bandwidth to each direction. For example, CCITT V.23 as normally used gives almost everything (1200 bit/s) to the main channel with a very slow (75 bit/s) data rate in the back channel. This is called asymmetric full-duplex transmission.

4.1.2. Bandpass Filters

To separate the high- and low-band signals, the K-Series modem ICs incorporate two band-pass filters. In the call mode, the lower frequency band filter is placed in the transmitter output path and the higher frequency band filter in the receiver input path. In the answer mode, the positions of the two filters are reversed. For local analog loopback testing, where the receiver operates in the same band as the transmitter, the receiver filter is bypassed and is unused. The filter positions and bandwidths are adjusted automatically according to the modulation mode selected. The shape of the filters is optimized for DPSK and QAM transmission so that, in conjunction with filtering in the modulator, the transmitted spectrum is shaped to a square-root of raised cosine with 75% excess bandwidth as required by V.22 and V.22bis. In addition, each filter includes compromise equalization to correct for the frequency response of a typical local loop in the telephone network. Both amplitude and group delay variation are corrected over the band covered by the filter so that the total distortion of the signal from modulator to demodulator is in most cases kept to a minimum.

4.1.3. FSK Modulator and Demodulator (300 bit/s and 1200 bit/s asymmetric)

CCITT Recommendations V.21 and V.23 and Bell Standards 103 and 202 specify the transmission of data using Frequency Shift Keying (FSK). The incoming data directly controls the frequency of an oscillator and switches its phase continuously between one frequency to represent binary ZERO data and another to represent binary ONE. Any bit rate may be used up to the maximum for the standard selected. Also, the bit rate and modulation rate (baud rate) are the same, which could explain why baud rate is often thought to be synonymous with bit rate. V.21 uses 980 Hz and 1180 Hz for ONE and ZERO, respectively, in the calling modem transmitter and 1650 Hz and 1850 Hz in the answering modem. Bell 103 uses 1270 Hz and 1070 Hz (calling) and 2225 Hz and 2025 Hz (answering), respectively. Note that for Bell 103, the ONE frequency is higher than the ZERO frequency, whereas for all other FSK schemes it is the other way around. Both Bell 103 and V.21 have a separation of 200 Hz between the ONE and ZERO frequencies and operate at a modulation rate of up to 300 bit/s. V.23 uses 390 Hz and 450 Hz for ONE and ZERO, respectively, in the backward channel (usually transmitted by the calling modem) which has a maximum data rate of 75 bit/s. 1300 Hz and 2100 Hz are used in the forward channel (usually the answering to calling modem) with a maximum rate of 1200 bit/s. Bell 202 is similar to V.23 but uses slightly larger separations to make higher data rates possible. The frequencies, in the same order as for V.23, are 387 Hz, 487 Hz, 1200 Hz and 2200 Hz. The FSK receiver operates by detecting the frequency of the received signal and outputting a ONE if it is closer to the ONE frequency or a ZERO otherwise. Again, this frequency discriminator output connects directly to the received data output pin so that any data rate up to the maximum will pass through the transmitter, telephone line and receiver.

4.1.4. DPSK Modulator and Demodulator (1200 bit/s)

Both the CCITT V.22 Recommendation and Bell Standard 212A specify the transmission of data at 1200 bit/s using four-phase Differential Phase Shift Keying (DPSK). There are differences between these two standards in the connect handshake and lower speeds supported, but these do not affect operation. Incoming data is collected in two–bit groups called dibits which are coded into one of four possible symbols. Each symbol specifies the phase change to be applied to the carrier signal with respect to its previous phase (hence the differential in DPSK). The phase change may be 0°, 90°, 180° or 270°. Phase changes to the carrier are made at a rate of 600 per second, this is known as the symbol rate or modulation rate and is measured in baud. With two bits coded per symbol and symbols transmitted at 600 per second the data rate is, as expected, 1200 bit/s. The phase changes are made smoothly to limit the frequency spectrum generated, as required by V.22 and to allow the separation of call and answer bands. The calling modem transmits using a 1200 Hz carrier and the answer modem uses 2400 Hz.

The modem receiver looks for the phase changes in the incoming carrier to demodulate the data. The calling modem receives the 2400 Hz carrier and the answer modem the 1200 Hz carrier. The phase changes are detected and converted back to dibits and finally to the received serial data stream.

V.22 also specifies a 600 bit / s mode which is available on K-Series products supporting this recommendation. Individual bits in the incoming data are coded as either 90° or 270° phase changes, modulation and demodulation proceed as above. K-Series products which have an adaptive equalizer for V.22bis operation can also use this in DPSK modes, thus realizing a significant improvement in performance over poor telephone lines.

4.1.5. QAM Modulator and Demodulator (2400 bit/s)

The CCITT V.22bis Recommendation specifies the transmission of data at 2400 bit / s using 16-point Quadrature Amplitude Modulation (QAM). Incoming data is collected into four-bit groups or quadbits which are then coded into one of sixteen possible symbols. Each symbol specifies independently the amplitude of a cosine and a sine carrier signal of the same frequency which are added to each other at the transmitter output. Because cosine waves and sine waves have the mathematical property of being in quadrature, they remain distinct, even though added together, and can be separated at the receiver. Each carrier has four possible levels, thus making up the four times four or sixteen possible symbols transmitted. The levels can be represented by the numbers -3, -1, 1 and 3. Negative numbers indicate inversion of the carrier wave. As for DPSK, the quadrature carriers have their levels changed at the symbol rate of 600 times per second and the changes are smoothed by filtering. 1200 Hz carriers are used for the call mode transmitter and 2400 Hz for the answer mode.

A Digital Signal Processor is incorporated in the receiver of the K-Series modems which support V.22bis to perform adaptive equalization. This processes the received signal and adjusts itself until the result is as close as possible to the known set of symbols that the transmitter can send. Effectively, this "undoes" a lot of the distortion introduced by the telephone line and allows the receiver to distinguish the symbols. The symbols detected in the receiver are decoded to quadbits and finally to the received serial data stream.

4.1.6. Timing and Carrier Recovery in DPSK and QAM modes

In synchronous modulation modes (DPSK and QAM), the K-Series modem receiver automatically recovers and tracks the incoming data rate from the remote modem transmitter so that it knows when to expect the phase changes to occur. The timing recovery system operates within the ±0.01% limit on data rate specified by both Bell and CCITT standards. In fact, the tracking mechanism can tolerate a larger variation to allow for a similar deviation in the local reference clock frequency and to follow jumps in the timing at the receiver. We do not, however, recommend using a K-Series part to receive from a modem that does not meet the specifications for the synchronous data rate. In addition, the carrier of the received signal is recovered and tracked. The carrier frequency may deviate by ±7 Hz without a significant degradation to the modem performance. This allows a ±1 Hz tolerance in the transmitted carrier as specified plus a ±6 Hz shift in the telephone network.

4.1.7. Compromise Amplitude and Group Delay Equalization

In all modulation modes, the K-Series modems alter the transmitted signal to compensate for the expected distortion of part of the telephone network. This Compromise Equalization reduces the effect of the local loop on the signal reaching the central office and improves the performance of the receiving modem, especially when it does not have an adaptive equalizer. The loop characteristics we have used are typical of connections in the United States and therefore may be sub-optimal in countries or locations where the quality of the network plant is particularly poor.

4.1.8. Scrambler and Descrambler for DPSK and QAM

K-Series modem ICs incorporate the scrambler and descrambler required by the V.22, V.22bis and Bell 212A specifications. The special circuitry called for in V.22 and V.22bis to prevent lockup of the scrambler is effective whenever the scrambler is in operation. This circuit detects a sequence of 64 consecutive "ONES" entering the scrambler register and inverts the next bit. Although the matching circuitry in the receiver is optional, we have included it in the descrambler so that no bit error will occur when the lockup preventer fires. The purpose of the scrambler is to randomize the transmitted symbol sequence so that the receiver can recover symbol timing information from the data signal. The adaptive equalizer used in V.22bis also requires this randomization. Both scrambler and descrambler are automatically switched out of circuit in FSK modes. The scrambler can also be disabled by the controller as required during the initial connect handshake sequence.

4.2. GETTING DATA INTO AND OUT OF THE K-SERIES MODEM IC

The user's data passes into and out of the K-Series modems on a conventional serial interface. If the data source is external to the equipment, as in a box modem, only the V.28 drivers and receivers are needed to implement a V.24 (EIA232-D) interface to conventional data terminal equipment (DTE). If the data source is inside the equipment, as in a PC card modem or embedded modem, a UART is needed to convert the data into a serial stream. K-Series products with integral UARTs incorporate this function on the chip, but the serial interface is still there and can be used separately. Data to be transmitted should be presented at the transmit data (TXD) pin and received data is output at

the receive data (RXD) pin. When using bit-synchronous data format (see below), clocks are provided for the transmit and receive data on the TXCLK and RXCLK pins, respectively. The transmit clock may alternatively be provided externally and applied at the external clock (EXCLK) pin.

4.2.1. Character Asynchronous Format in FSK modes

In FSK modulation modes, the data input at TXD is connected directly to the oscillator that generates one of two tones for transmission. Similarly at the receiver, the frequency discriminator output passes directly to the RXD pin. The K-Series modem IC does not attempt to align the data with any clocks, so that the transitions pass through the system from one end to the other with minimal timing distortion. Thus, character asynchronous (start / stop) data can be applied to the TXD pin at any bit rate up to the maximum for the modulation mode selected, and will appear at the same rate at the RXD output of the remote modem. FSK modes are not well suited to the transmission of bit-synchronous data.

4.2.2. Bit-Synchronous Format in DPSK and QAM modes

In contrast to FSK modes, DPSK and QAM modulation rely for their operation on a very closely controlled data rate. The symbol rate (or modulation rate) is specified in V.22, V.22bis and Bell 212A to be 600 ±0.01% symbols per second (or baud). As a fixed number of bits must be coded per symbol, the bit rate must also be controlled to this accuracy. In bit-synchronous mode, the K-Series modem IC provides a clock for the transmitted data bits at the TXCLK pin and a new bit is taken from TXD on every rising edge. A similar clock is recovered from the remote modem's transmit rate and is presented at RXCLK. A new received bit is placed at RXD on each falling edge of this clock. If the source of data cannot accept a clock from the modem, an external clock may be applied at the EXCLK pin and the K–Series modem IC programmed to synchronize to this. The clock must be at the nominal bit rate to the required accuracy of ±0.01%. The modem IC may also be programmed to use the RXCLK signal instead of EXCLK in which case, the transmitted data rate will become identical to the received data rate, i.e., the transmit rate of the remote modem.

4.2.3. Character Asynchronous Format in DPSK and QAM modes

The convenience of the character asynchronous (start / stop) data format is not easily given up, even in the face of superior performance from synchronous modems. Therefore both Bell and the CCITT specify methods for passing data in this format over a synchronous modem connection. Fortunately (and perhaps surprisingly) Bell and CCITT methods are entirely compatible. The K-Series modem ICs can be programmed to operate in character asynchronous data mode even in DPSK and QAM modulation modes. A data format converter (async / sync converter) is placed in series with the data stream at the TXD input and the RXD output. The modem IC must be programmed to use a particular character length of 8, 9, 10 or 11 bits, including start and stop bits. Data can now be presented in start / stop format with an intra-character bit rate reasonably close to the nominal operating data rate. The converter adjusts the bit rate to the synchronous data transfer rate by deleting or adding stop bits as necessary. At the receiver, the converter reinserts deleted stop bits and accelerates the intra-character bit rate to squeeze out the higher data rate. The normal range of acceptable bit rates is from 2.5% below nominal to 1% above nominal. Some K-Series family members also provide an extended overspeed mode in which data at up to 2.3% above the nominal can be accepted. In this case, the receiver converter may reduce the length of stop bits by up to 1 / 8 to avoid an excessive increase in the intra-character bit rate. Special techniques are used to pass break signals which require some help from the data source. More information on this subject should be obtained from the CCITT Recommendations of the V-Series, V.22bis.

4.2.4. K-Series Modem ICs with Integral UART

Some products in the K-Series family are available in versions which incorporate a UART on the same die as the modem. The UART is compatible with the industry standard 8250 and 16450 UARTs used in the IBM PC™. When appropriately programmed, the serial data transfer occurs within the chip and the entire system operates as if it were an 8250 UART.

4.3. DIALING A CALL ON THE SWITCHED TELEPHONE NETWORK

Exchanging data from one end to the other of a data connection is not the whole story in dial-up communications. It is also necessary to establish the connection in the first place. The K-Series products include functions to facilitate the selection and monitoring of a call on the general switched telephone network.

4.3.1. Call Progress Monitoring

The Call Progress Monitoring system looks for energy in the receive signal in a band from approximately 350 Hz to 620 Hz. Most K-Series products incorporate a bandpass filter dedicated to this function although the DSP-based versions scale down the lower bandpass filter normally used in data mode. The controller may read a bit in the status registers to see if energy above the threshold is present in the call progress band. The network in most countries emits tones in this band to indicate the progress of a call and the controller can identify these indications by the cadence of the tones. Thus the system can wait for a dial tone before dialing, sense the ringback on a successful call or the busy signals when the call cannot be completed.

4.3.2. DTMF Tone Generator

For dialing a telephone number using the standard Dual-Tone Multi-Frequency signals (DTMF), the K-Series modem ICs include a pair of tone generators. The controller can program the modem IC to produce any one of sixteen tone pairs and can turn the transmitter on and off to time the tone burst. DTMF signals appear at the TXA analog output pin at a higher level than data signals to take advantage of the higher power allowed in most countries for network signalling information.

4.4. CONTROLLING THE K-SERIES MODEM ICs

K-Series modem ICs are designed to operate with a controlling microprocessor or microcontroller. The controller selects and configures the available functions of the part by writing to internal registers and can find out what signals are being received from the line by reading other registers. The firmware for the controller must step the system through the process of seizing the telephone line, placing a call, connecting with the remote modem, monitoring the connection and terminating the call. It will typically also implement some other desired functionality of the product, such as the Hayes AT™ command set, data buffering, error control, etc.

4.4.1. Parallel Control Bus

The K-Series products can be connected to an 8-bit data bus. The internal registers are then accessible to the controller as if they were input / output or memory locations. The ALE (address latch enable) input allows the modem IC to operate directly with multiplexed address / data bus controllers. Non-multiplexed microprocessors require some additional logic to connect to the K-Series parts. Some guidance and examples for bus interfaces to popular microprocessors are given in section 6.3, Interface to the Control Microprocessor.

4.4.2. Serial Control Interface

The Serial Control Interface is offered as an alternative to the more direct bus connection where the bus is not available or the K-Series modem IC must be controlled over a limited interface. Seven signals are used, three address bits, the data line, a clock signal and the read and write control lines. In a typical application, all seven would be connected to programmable I / O ports of the microcontroller and firmware would administer the exchange of data. In section 6.3.4, Using the Serial Control Interface we discuss the timing of the signals.

4.4.3. Control and Status Registers

The controller programs the K-Series modem IC and monitors its status through a set of registers. Seven 8-bit registers are provided for, but the simpler parts in the family may omit certain registers or certain bits within registers. Control Registers are read / write so that the programming can be read back by the controller. The Detect Register is read only as it reflects the status of detectors internal to the modem chip. The ID Register is also read only and provides a code to identify the K-Series product modulation mode capability and a user-definable personality. The name and purpose of each bit in each register is given in the data sheets for each part. In Controller Firmware Design for K-Series Modems (section), the use of the control and status registers is covered in detail as they become necessary to perform a particular function.

Section 5.0

SYSTEM DESIGN OVERVIEW

5.0. SYSTEM DESIGN OVERVIEW

Before plunging into the hardware and firmware design in the next sections, we will try to take a look at some aspects of the overall system design. It is difficult for us to give you specific guidance in this area, as only you know your system requirements. However, products incorporating modems tend to fall into a few broad categories and we will base our discussion around these. Two questions that we'll try to answer for you in this section are: "Should you use your existing microprocessor to control the modem chip, or add another one?. . . and, "How do you interface your application data to the modem?"

5.1. HARDWARE FOR DEDICATED MODEM PRODUCTS

A dedicated modem product is one whose primary function and value is data communication. The data to be transmitted is the responsibility of the user of the product. The product may have its own enclosure and power source (a "box" modem) or it may be a module that attaches inside some other system such as a computer (a "card" modem). It may incorporate value added features such as error control or data compression, but its basic purpose is to move the user's data to some remote location over the telephone network.

A block diagram of a dial-line "box" modem using a K-Series modem IC is shown in Figure 5-1. It consists of four basic parts, the modem IC, a microcontroller, a four-wire / two–wire converter and the direct access arrangement (DAA). (See Section 6.5). The microcontroller is responsible for the control of the modem IC and interpreting commands delivered over the data wires from the user.

5.2. HARDWARE FOR PRODUCTS WITH EMBEDDED MODEMS

As the size and complexity of modems are reduced towards single chips by IC companies such as Silicon Systems, more system manufacturers are finding that they can usefully incorporate a data communication capability into their products. The primary function of the product remains unchanged, but the incorporation of a modem adds value and differentiates it from its competition.

5.3. FIRMWARE FOR DEDICATED MODEM PRODUCTS

The firmware needed for dedicated modems can be divided into three areas. First, a command processor of some sort is needed to enable the user to control the product and get it to operate in the intended manner. This will include an interpreter for a serial command set such as V.25bis or Hayes AT™, an interface to front panel switches, option switches and indicators, and the implementation of the V.24 data interface control signals. Secondly, in response to user commands, the firmware must control and monitor the K-Series modem IC to establish, maintain and test a communication link with a remote modem. This is the subject of section 1 in this Design Manual. Finally, there will be any added value features which are to be performed such as speed buffering, error control, data compression and encryption. Which (if any) of these features you choose will depend on your target market. Speed buffering is a useful feature for modems with V.23 or Bell 202 capability because it avoids the need to change the DTE data rate according to the direction of the forward channel (see "buffered" in the glossary).

5.4. FIRMWARE FOR PRODUCTS WITH EMBEDDED MODEMS

For embedded applications, the firmware can be divided into three areas as for dedicated modems. However, although the functions performed are similar, the emphasis changes considerably. First, the command processor becomes a simple interface between the application and the modem control code. The kind of flexibility of operation required in a dedicated modem would never be required where the modem and data source are designed together as one product. In some cases the interface may be as simple as a flag that causes the dialing of a fixed telephone number and a UART driver for the exchange of data. Secondly, the modem control firmware itself may be simplified because of the limited environments in which the modem will operate. Some applications may require call mode or answer mode operation but not both. Where the system designer has control over the modem to which the product will connect, he or she can also limit the variety of modulation standards that the firmware will attend to. Finally, instead of the added value features in the dedicated modem, we must include the primary functions of the product with an embedded modem.

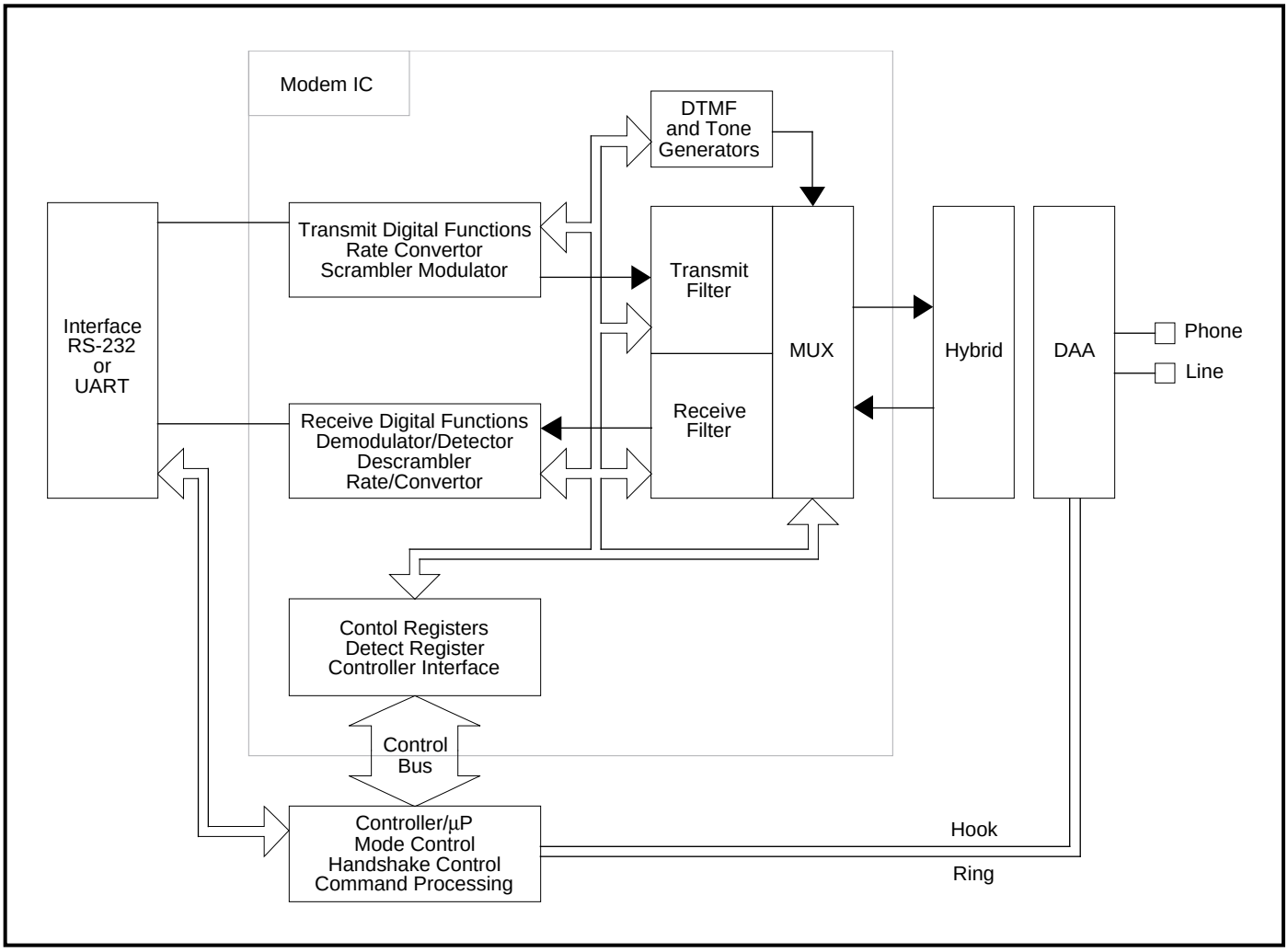

FIGURE 5 – 1: Basic Box Modem

Section 6.0

HARDWARE DESIGN USING K-SERIES PRODUCTS

6.0. HARDWARE DESIGN USING K-SERIES PRODUCTS

This section of the Design Manual is concerned with the details of designing a modem system around a K-Series IC. A complete schematic of a typical application is shown in Figure 6–1. You may want to refer to this while reading the following sections.

We have tried to organize the following material in a logical order, following a reasonable sequence of design decisions. Starting in the areas where there is little freedom, we discuss the power supply and oscillator. Then we consider the connection to a microprocessor or microcontroller and the hookup of the data to be transmitted and received. The most involved part of this section then describes the analog interface to the dial-up telephone network. Finally, we review some general design considerations, including control of interference and printed circuit board layout.

6.1. POWER SUPPLY AND POWER-ON RESET CIRCUIT

The first things that you should consider when starting a design with the K-Series products are the availability of a suitable power supply and how you will reset the modem IC to a safe and known state when power is first applied. In this section we will discuss connections to the ground (GND), voltage (VDD), ISET (see 73K224 data sheet), voltage reference (VREF), and RESET pins.

6.1.1. Power Supply

5V K-Series parts allow a tolerance of ±10% on the VDD supply which provides for a voltage of between 4.5V and 5.5V. 12V parts allow -20% and +10% so the voltage should be between 9.6V and 13.2V. The modem ICs perform according to their specifications over these full ranges, however, parameters will be closer to their typical values if the supply voltage is close to nominal. Protect the VDD supply pin from voltages in excess of 14V as these could damage the part or impair long-term reliability. Because

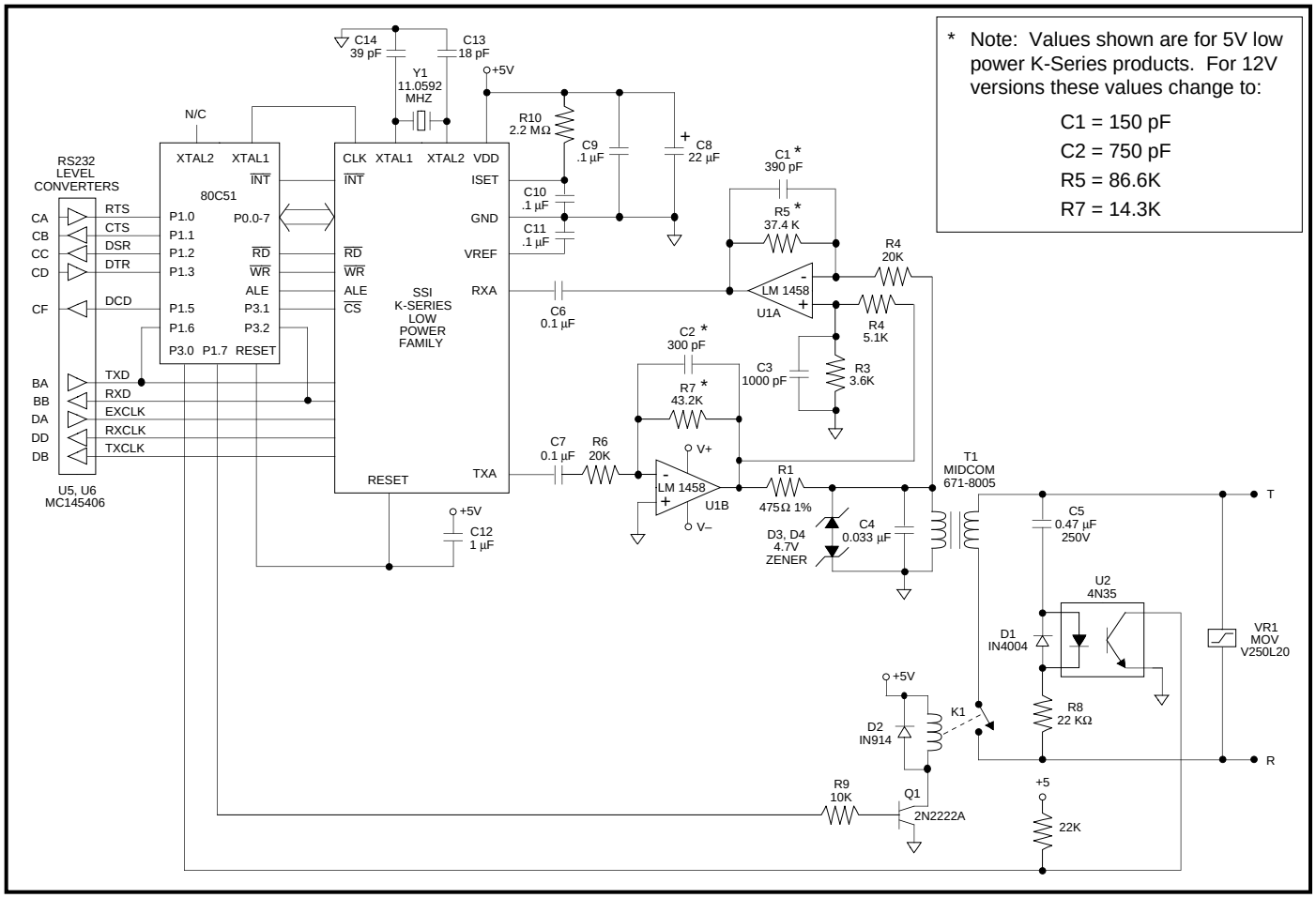

FIGURE 6 – 1: Typical Application Schematic

the K-Series modems combine analog and digital circuitry on the same silicon die, it is very important to ensure that the power supply is free from interference at all frequencies. We recommend that you decouple the VDD pin with both a low inductance type 0.1µF capacitor and a 22µF electrolytic capacitor. These capacitors should be placed close to the VDD pin and connect to a ground plane under the package which can act as a low impedance connection to the GND pin. If you are using the same supply for the K-Series IC and fast digital logic, you may consider placing a ferrite bead in series with the VDD connection to the modem IC to block high-frequency noise. We have experimented also with a small resistor of about 10Ω in this position, but have found this does not help in all cases and sometimes degrades performance.

6.1.2. Eliminating Stand-by Power Draw

All K-Series modem ICs have a power-down mode. For low-power (5V), non-DSP parts such as the 73K222L, using this can reduce stand-by power consumption to below 15 mW. We have seen applications where even this is not acceptable. Where portable, battery powered equipment is concerned and the modem is used for brief periods only, it makes sense to shut off all power to the chip. This can be done with metal-oxide-silicon, field-effect transistor (MOSFET) switches if you are careful about their on–resistance and supply decoupling. However, you will need to isolate both the VDD and GND pins of the K-Series IC so that it does not load the bus of the controller.

6.1.3. Connections to ISET and VREF pins

The ISET pin is used to supply a reference current to the chip so that a suitable operating current for the internal analog circuitry can be established. Connect this pin to the positive supply at VDD via a 2 MΩ, 5% metal film resistor. This tolerance is quite adequate to ensure a value in the specified range of 1.8 to 2.2 MΩ, but a closer tolerance can of course be used if required. To prevent the pick up of noise at this high impedance point, decouple the ISET pin with a 0.1µF, low inductance capacitor placed immediately at the pin and connected to the ground plane under the package. Not all K-Series parts actually require this resistor. The 73K222U, for example, allows the ISET pin to be connected directly to ground. This reduces the parts count by a resistor and a capacitor but we have to relax the maximum current consumption specification a little under these circumstances. The nominal current remains the same. See the data sheet for the part you have chosen to find out if you can use this feature.

The K-Series modem chip generates an internal reference voltage which is brought out to the VREF pin for decoupling. Again use a 0.1µF low inductance capacitor, such as a multilayer ceramic component, to decouple to GND. Position the capacitor as close as possible to the VREF pin and use the ground plane under the package to connect to GND. Using as much ground plane as possible ensures a low impedance connection to the GND pin from these important decoupling capacitors, see also Ground Connections at the K-Series Modem IC, section 6.7.2.

6.1.4. Resetting the K-Series Modem IC at Power-Up

All K-Series products have an active-high RESET input pin which can be used to force the chip into a safe and known state when power is first applied. This input is normally held at a logic LOW level by an metal-oxide semiconductor MOS transistor on chip. Taking this input to a logic HIGH level resets the chip. Note that the RESET input requires a logic HIGH voltage of at least 3V and is therefore not TTL level compatible. This reset by hardware performs exactly the same functions as setting the Reset bit (bit 2) in Control Register 1 in the controller firmware. All bits in Control Registers 0 and 1 and the Tone Register are cleared to ZERO. This includes the Reset bit itself, however, the modem chip remains in a power-down state by virtue of bits 5 to 2 in Control Register 0 being all ZERO. In the products equipped with a Digital Signal Processor (DSP), the additional Control Registers 2 and 3 are reset to a condition which makes these parts compatible with the lower speed families. Control Register 2 is cleared to all ZEROs and Control Register 3 is all ZEROs except for bit 2 so that the Transmit Attenuator selects a -10 dBm0 output. The state of the Detect Register at power-up and even after a reset operation is not well defined. In K-Series parts with an on-chip DSP, all bits will be undefined until the DSP is taken out of reset. In parts without a DSP, after taken out of reset most bits will settle down within a few tens of milliseconds to the value you would expect according to the signal at the RXA pin. The Receive Data bit will be in an unknown state, but will not change as long as the part remains in power-down. After a firmware reset, the modem chip may be programmed as required immediately. However, make sure that a hardware reset has properly ended (the RESET pin is below 0.8V) before attempting to program the chip.

Because it is difficult for us to control the strength of the internal pull-down current at the RESET pin we recommend that you drive this pin with a complementary metal-oxide semiconductor (CMOS) logic level from a separate reset circuit or use an external resistor to ground. Equally, you can ignore this pin and reset the K–Series IC via Control Register 1, which is recommended. A brief period after power-up, during which the state of the chip is unknown, is unlikely to cause any problems as long as the system cannot go off-hook. If, however, you want to use a capacitor to VDD to perform power-on reset, then the following section will help you choose a value.

6.1.5. Using a Capacitor for Power-On Reset

The simplest way of resetting the K-Series modem IC on first application of power is to connect a capacitor between the RESET pin and the positive supply voltage at VDD. A 1 µF capacitor is recommended and will be effective in most cases. The reset will occur correctly as long as the supply voltage rises rapidly enough to reach the minimum

operating voltage of the part (4.5 or 9.6V) before the capacitor collects enough charge to drop the RESET pin below the logic HIGH level of 3.0V. The maximum current drawn by the internal pull-down resistor is 50 µA for any version although some family members have a smaller upper limit. This current will charge a 1 µF capacitor to 1.5V in 30 ms so if the VDD of a 5V part reaches 4.5V in this time, then the RESET pin will be at 3.0V and a reset will occur. For a 12V part, the capacitor can collect a voltage of 6.6V before reset fails, allowing the VDD supply to take 132 ms to reach 9.6V. A smaller capacitor can be used if a faster risetime can be guaranteed.

Now we must calculate how long the reset condition can persist after the application of power. Don't try to program the modem IC while it may still be in reset because it will overwrite anything written to the registers. To determine this time, we must find out how long the capacitor will take to allow the RESET pin to fall below the logic LOW level of 0.8V. It would be safest to assume that the power supply rises rapidly to the maximum operating voltage. The minimum pull-down current for any version is 1 µA although some family members have larger lower limits. Using a 1 µF capacitor, the 5V part will come out of reset in 4.7 seconds and the 12V part in 11.7 seconds. This is a long time, which is why we would prefer you use the Reset bit in Control Register 1. Actually, these times could be optimistic because the pull-down current could fall off as the voltage at RESET drops. An external pull-down resistor of 100 KΩ or below between RESET and GND would reduce the possible variation in pull-down current, but you must calculate the exponential decay of the voltage at RESET to make sure that the capacitor is large enough for your power supply risetime.

If a power-on reset function is performed elsewhere in the system, you can avoid using a capacitor at the RESET pin. The same signal that is used to reset the rest of the system can be used to put a logic HIGH at RESET for a period after the application of power. Remember that the VDD supply must reach the minimum operating voltage and the RESET pin must be taken to 3.0V or above for a reliable reset to occur.

6.2. CRYSTAL OSCILLATOR

The Silicon Systems K-Series single-chip modems can use an external 11.0592 MHz reference clock or can generate such a clock using only a crystal and two capacitors. If an external clock is used, it should be applied to the XTAL2 pin. This is a change from our former recommendation, but has been found to give superior performance to applying the clock at XTAL1. The XTAL1 pin should be left floating. Like XTAL1, the XTAL2 input is not compatible with TTL logic levels, but requires 3.0V minimum for a logic HIGH. Many benefits, however, are to be gained by using the on–chip oscillator. Crystal resonators are normally cheaper than complete crystal oscillator modules and using the internal oscillator can result in less radiated interference. This is because the drive capability is exactly adjusted to the load whereas a separate oscillator will have excess drive power to meet wider load requirements and will therefore produce higher slew rates and result in more electromagnetic interference (EMI) (see section 6.6.1, Electrical Design for Low EMI).

6.2.1. Frequency Accuracy

Whichever source of reference clock is chosen, however, it is important that the frequency be maintained within 0.01% of 11.0592 MHz. In synchronous modulation modes (QAM and DPSK), the modem's data rate is obtained by dividing down the reference clock and if this is in error then the modem will not conform to the published specifications. The maximum allowable deviation of the bit rate from the nominal value of 2400 bit / s (V.22bis) or 1200 bit / s (V.22 and Bell 212A) is 0.01%, so that the reference clock must be at least this accurate. This should apply across the full range of temperature, operating voltage and other environmental factors in which the product is expected to work. Note also that even if the data transmitted is in start / stop (character asynchronous) format, the modem converts it to a synchronous bit stream for transmission and the accuracy of the data rate is just as important as for direct synchronous data.

Typically, you should specify the oscillator or crystal to have an initial frequency accuracy of plus or minus 50 parts per million and a temperature drift low enough so that it will not drift more than an additional 50 parts over the desired temperature range.

The effect of the reference frequency being out of specification is not catastrophic and could go entirely unnoticed even into the production phase. Many modems, including the Silicon Systems K-Series, are able to work with other modems which deviate far more than 0.01% from the nominal data rate. However, it would be unwise to put a product into the field which showed a larger deviation as the customer has every right to test this parameter. Also, some modems will not tolerate wide deviations and will make errors in bursts or may fail to connect. In this situation, the blame can quickly be traced to the modem with the wrong data rate. We therefore recommended that you make careful measurements of the clock frequency on product prototypes using a high-quality frequency counter. Also, unless you can guarantee tight control of the oscillator specifications by procurement policies or incoming inspection procedures, you should make this measurement as part of the manufacturing test. Measurement should be made at the CLK pin for minimal interference with the circuit operation, an accurate measurement cannot be obtained at XTAL1 or XTAL2 when using the on-chip oscillator. The frequency should be between 11.0581 MHz and 11.0603 MHz for all expected environmental conditions. Make an allowance also for the accuracy of the measuring instrument.

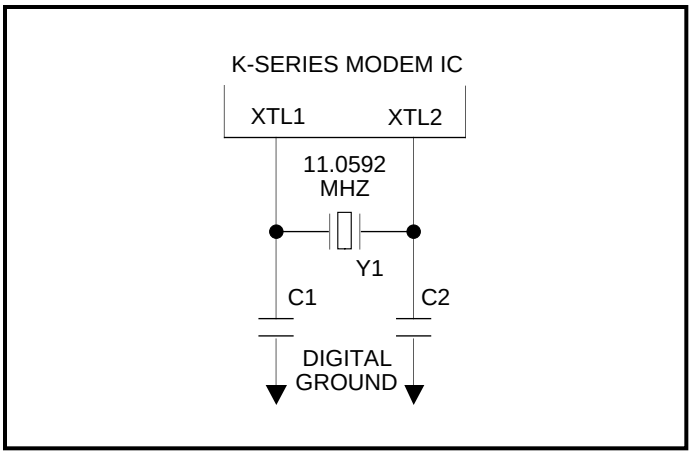

FIGURE 6 – 2:
External Components for use of One–Chip Oscillator

6.2.2. Using the On-Chip Oscillator

If the on-chip oscillator is used, some additional care is needed to ensure that the desired frequency is obtained.

6.2.2.1. Specifying a Crystal

The manufacturer of the crystal resonator verifies its frequency of oscillation in a test setup, but to ensure that the same frequency is obtained in the application, the circuit conditions must be the same. The Silicon Systems K-Series modems require a parallel mode (antiresonant) crystal, the important specifications of which are as follows:

Mode	Parallel (antiresonant)
Frequency	11.0592 MHz
Frequency tolerance	±50 ppm at nominal temperature
Temperature drift	±50 ppm additional over full range
Load capacitance	18 or 20 pF (see below)
Series resistance	50Ω maximum
Drive level	Less than 1 mW

Several manufacturers offer standard products that will meet these specifications. The MP-1 is calibrated at 18 pF load capacitance and is available by calling M-tron at (605) 665-9321. A similar part calibrated at 20 pF is available from Saronix at (415) 856-6900, part number NYP111-20. Your own preferred supplier of crystals should have no problem making a part to the above specification.

6.2.2.2. Determining the Values of Capacitors C1 and C2

The load capacitance of a parallel-mode crystal is of great importance in obtaining the correct frequency of oscillation. The manufacturer will test the crystal at the value you specify, but if the capacitance presented by your circuit is different from this, then the frequency of oscillation will also be different. This capacitance is not the same as the value of the capacitors from XTL1 and XTL2 to ground (C1 and C2). The crystal load capacitance is made up from the capacitance between XTL1 and XTL2 inside the K-Series modem chip, the circuit parasitics between these two points and the effect of C1 and C2. In a good design, the effect of the capacitors will dominate, but is difficult to analyze and so is normally set by experimentation. We suggest a starting point of 39 pF for C1 from XTL1 (pin 2) to ground and 18 pF for C2 from XTL2 (pin 3). This works well with a crystal rated for an 18 pF load, allowing for average parasitic oscillation in the layout. The asymmetry of the capacitor values is helpful in ensuring that the oscillator starts up quickly when power is applied. If, after trying several crystals, you find the frequency at CLK to be consistently low, then reduce the values of the capacitors. If the frequency is high then increase them. It is impossible for us to give you definitive values for these components as they are required to compensate for variation in parasitic effects from one circuit layout to another.

6.2.3. Possible Problems

A problem with the crystal oscillator can be very difficult to identify as it may only appear when the modem tries to make a connection to certain other modems. We strongly recommend that you explicitly check that the oscillator is working properly, and at the correct frequency, in your production tests. For troubleshooting information see section 11, Troubleshooting the Modem Design.

6.3. INTERFACE TO THE CONTROL MICROPROCESSOR

We have designed the K-Series family of modem integrated circuits to interface easily with microcontrollers which have a multiplexed address / data bus. The bus control signals provided are optimized for controllers with separate read and write lines, however the logic needed to generate these signals from a read / write and strobe architecture is very simple. With some tri-state buffers and a little more logic it is also possible to use microprocessors or controllers which have separate address and data busses, but see our alternative suggestions below.

To design an interface to a microprocessor bus, you must be aware of the timing requirements. All the K-Series parts, except those with integral UARTs, have the same requirements (the integral UART versions have a bus structure based on the 8250 / 16450 UART). We will briefly describe the bus interface operation here. Refer to the data sheet of the part you have chosen for timing diagrams and use those delay times if they differ from what we present here. To perform a read or write to an internal register, the address of the register must first be placed on the address / data bus. As only eight register locations are used, only the bottom three bits, AD2, AD1 and AD0, are significant. ALE should be pulsed HIGH for 60 ns minimum to latch the address into an internal register in the chip. The address must be valid for at least 30 ns before and for 20 ns after the

falling edge of ALE. Chip Select ($\overline{CS}$) should be treated as an address line for timing purposes. After the falling edge of ALE, 40 ns must be allowed for the address to be decoded before either Read ($\overline{RD}$) or Write ($\overline{WR}$) are put LOW. Do not put them both LOW together, or the chip will enter a factory test mode. For a read operation, $\overline{RD}$ should be put LOW for at least 200 ns. The addressed register's contents will appear on the bus if $\overline{CS}$ was LOW when latched by ALE. Data is valid from 140 ns after $\overline{RD}$ goes LOW to the time it goes HIGH. The bus may not return to the high-impedance state for 200 ns after $\overline{RD}$ goes HIGH so do not allow another source of data to drive the bus during this time. For a write operation, $\overline{WR}$ should be put low for at least 140 ns. The data to be written to the addressed register must be valid on the bus 150 ns before the end of the write pulse (the rising edge) and for 20 ns after. The data will be written to the register only if $\overline{CS}$ was LOW when latched by ALE. Do not put ALE HIGH again for a new cycle until at least 10 ns have elapsed since either $\overline{RD}$ or $\overline{WR}$ have returned HIGH in the present cycle.

As an alternative to the parallel, bus oriented control interface, you can use a serial control interface to link the K-Series part to the controller. All versions make this serial interface available, even if the full parallel interface is present on the pinout. You may prefer to use this interface if the bus architecture of your chosen controller does not hook up efficiently to the K-Series parallel bus architecture. Also, the parts with integral UARTs use the same serial control interface in the dual-port mode to allow a controller to look after the modem independently of the bus interface to the UART. For a full description of the serial interface, see section 6.3.4, Using the Serial Control Interface.

6.3.1. Using the 80C51 Microcontroller

The K-Series modem ICs can be connected to 8039 / 48 or 8031 / 51 microcontrollers without any interface logic components. Figure 6-3 shows the schematic of such a connection. In this example we assume that the system clock is generated by the K-Series part using its on-chip oscillator and the controller clock is taken from the CLK pin. Make sure that you configure the chip so that the signal at the CLK pin is the crystal frequency and not sixteen times the data rate. The CLK Control bit (bit 3) of Control Register 1 must be ZERO, this is the default state achieved on reset. You could also drive the XTAL2 pin of the K-Series IC and the XTAL1 pin of the controller from an oscillator module. See section 6.2, Crystal Oscillator for more information. The 80C51 is operated so that the address / data bus appears at the PORT 0 pins. Ports P3.7, P3.6 and P3.2 are configured to operate as the read and write control lines and an interrupt input, respectively. Usually a high order bit of Port 2 is used as the chip select for the K–Series part, and this pin must be put LOW by the controller firmware whenever the modem IC is to be accessed.

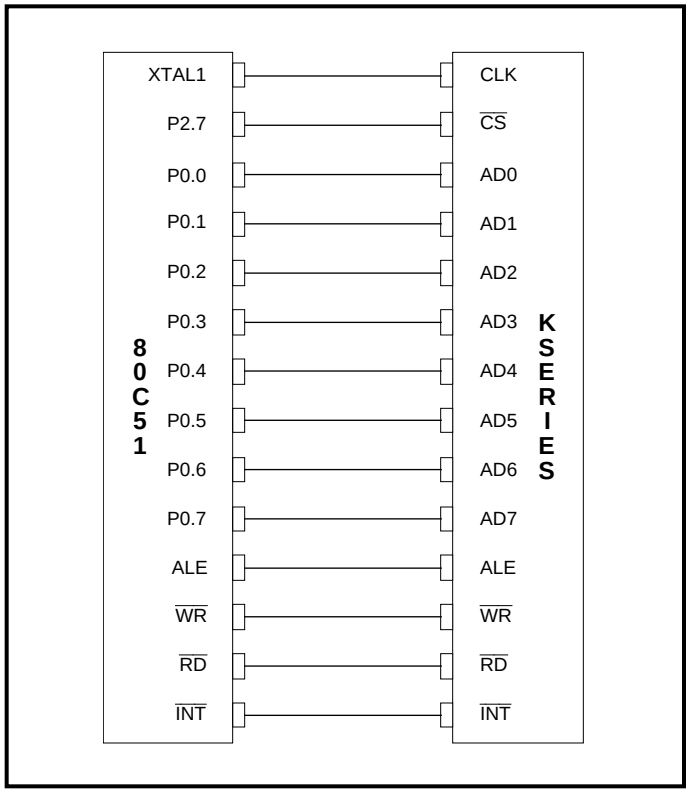

FIGURE 6 – 3: Interface to 80C51 Microcontroller

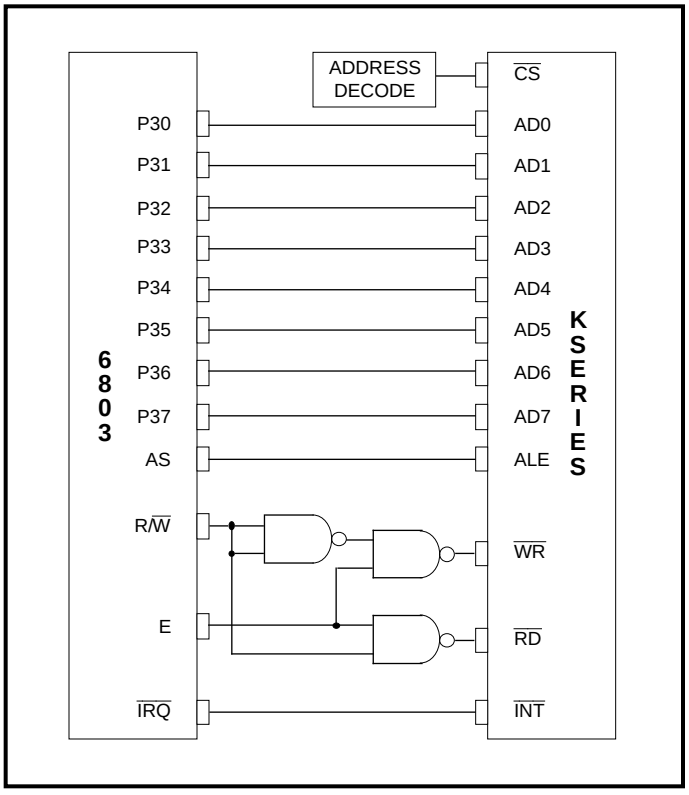

FIGURE 6 – 4: Interface to 6803 Microprocessor

6.3.2. Other Multiplexed Bus Controllers

Connecting a K-Series modem IC to a multiplexed bus controller other than the 8031 type should be no problem if it provides control signals compatible with the ALE, $\overline{RD}$ and $\overline{WR}$ lines. Check both the polarities of the signals and see that they conform to the timing requirements as described above and detailed in the data sheet. Some controllers, however, use a read / write control line and a strobe in place of separate read and write lines. Such a choice will require a little more thought, so we will work through an example using the 6803 / 6303 microprocessor. Since this component can operate either in a multiplexed or non-multiplexed mode, we assume here that it is initialized for the multiplexed address / data mode.

The 6803 / 6303 has an Address Strobe line, AS, which is directly useable for ALE. It puts either a ONE or ZERO on its R / W line to indicate a read or a write cycle, respectively. This signal is valid for the whole cycle, including the time that AS is HIGH, so that it cannot be used directly to control the $\overline{RD}$ or $\overline{WR}$ lines of the K-Series IC. Fortunately, the microprocessor also provides an Enable signal, E, which goes HIGH in both read and write cycles, but does not occur until AS has ended. Using the simple arrangement of gates shown in Figure 6-4, signals suitable for $\overline{RD}$ and $\overline{WR}$ can be generated from R / W and E.

6.3.3. Non-Multiplexed Bus Controllers

If you decide to use a controller that has a separate address and data bus you have three alternatives for interfacing the K-Series modem IC. You can design a circuit of multiplexing buffers to present address and data in sequence to the modem chip and generate address latch, read and write signals with the appropriate timing. This circuit will not be simple nor elegant, and getting the timing right requires careful study.

The simplest approach from a hardware viewpoint is to use the serial control interface. You will need to allocate six output port bits and one bi-directional port bit (or one input and one tri-state output) to connect to the K-Series IC. Subroutines in the controller firmware will manipulate these ports to transfer data. We discuss this more fully below and in section 7.1.2, Subroutines for the Serial Control Interface. An approach which avoids this complication in the firmware is to treat both the address and the data of the K-Series interface as ports at the controller. Depending on the bus timing, the hardware interface may be quite simple, needing no buffers but only address and control decode logic. The firmware would execute an output instruction to the address port to write the address of the desired register before an output or input at the data port which writes or reads the register. The first instruction would cause a HIGH-going write pulse to be applied at ALE by the hardware. The second instruction would cause a LOW–going pulse at $\overline{WR}$ or $\overline{RD}$. We might note, before we leave this subject, that the 16450-style bus interface of the integral UART K-Series parts allows them to be used directly with non-multiplexed bus controllers.

6.3.4. Using the Serial Control Interface

The serial control interface to a K-Series modem IC consists of seven signals. A2, A1 and A0 are address lines and select one of the internal registers to be written or read. DATA is a bidirectional line across which the data for both read and write operations flows. $\overline{RD}$ is held LOW for a read operation and $\overline{WR}$ is pulsed LOW for a write operation. The data is clocked into or out of the chip using a clock applied at the EXCLK pin (DCLK on the integral UART parts in dual-port mode). Versions with the full parallel bus interface can also be used with the serial control interface by tying ALE HIGH and $\overline{CS}$ LOW. The AD7 pin now becomes DATA and AD2, AD1 and AD0 become A2, A1 and A0. $\overline{RD}$, $\overline{WR}$ and EXCLK have the same names in either control mode but their use and operation is different. The signals required for using the serial control interface could be provided by a circuit of your own design, for example, a digital gate array, or by a microcontroller at its I / O ports. The latter case is useful if you are using a controller which does not bring its bus to its external pins or the bus is not multiplexed and therefore difficult to interface directly. See section 7.1.2, Subroutines for the Serial Control Interface for more details, the rest of this section is more important for hardware interface design.

To perform a read operation using the serial control interface, you should present the address of the register you wish to read at A2 to A0 and take the $\overline{RD}$ input LOW. The address will be latched on the falling edge of $\overline{RD}$ if EXCLK is LOW, or on the next HIGH to LOW transition of EXCLK if it is HIGH. The address must be valid for at least 50 ns before and after the latching event, whichever it is. The address need not remain valid for the entire read operation but $\overline{RD}$ must be held LOW. The least significant bit (bit 0) of the addressed register will appear at the DATA pin at worst 160 ns after $\overline{RD}$ goes LOW. To read further bits, EXCLK must undergo a HIGH to LOW transition and the new bit will appear at worst 200 ns after such a transition. Another restriction is that after $\overline{RD}$ has gone LOW to start the read operation, EXCLK must not undergo a LOW to HIGH transition for at least 200 ns. We recommend that EXCLK makes a HIGH to LOW transition just before $\overline{RD}$ goes LOW and that the value of DATA is read on the next eight LOW to HIGH transitions. If EXCLK is a square wave of period 500 ns or longer, a number of the above timing rules will then automatically be met. Figure 6-5 is drawn according to this recommendation. After the most significant data bit (bit 7) has been read, $\overline{RD}$should be returned to the HIGH state and the DATA line will become high-impedance after 80 ns maximum.

To perform a write operation, start by applying data to the DATA line during the HIGH to LOW transitions of the clock. Present the least significant bit (bit 0) first, followed by consecutively higher order bits. Each bit must be valid for 150 ns before and 20 ns after the HIGH to LOW transition of EXCLK. We recommend that you apply each bit more or less at each LOW to HIGH transition of EXCLK for eight such transitions. A minimum of 150 ns after the HIGH to

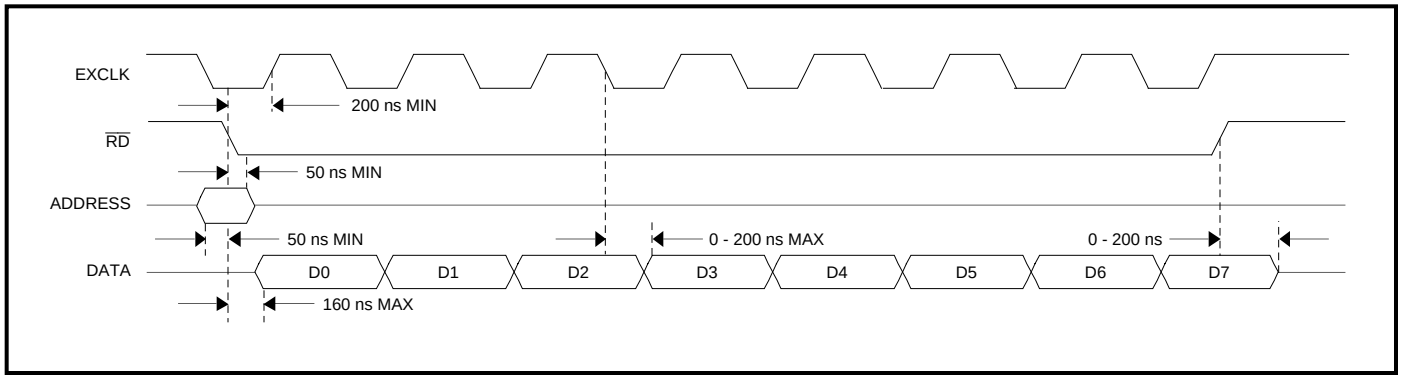

FIGURE 6 – 5: Serial Control Interface Read Timing

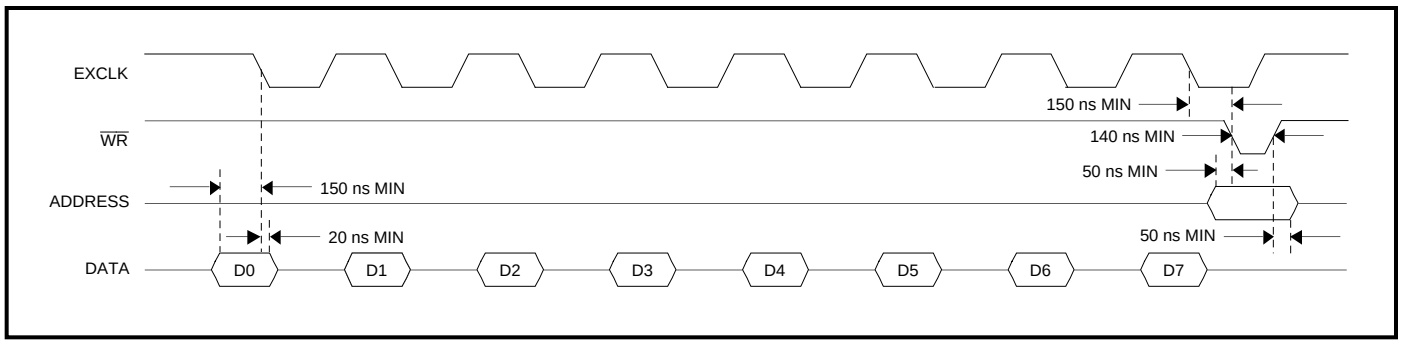

FIGURE 6 – 6: Serial Control Interface Write Timing

LOW transition which latches the most significant data bit (bit 7), put $\overline{WR}$ to the LOW state for at least 140 ns. You can apply the address of the register to which you want to write at any time as long as it is valid for at least 50 ns before you put $\overline{WR}$ LOW and for 50 ns after you put it back to HIGH.

The EXCLK pin is used by the K-Series modem IC in the bit-synchronous data format mode when the timing source is to be supplied externally. A clock must be applied at this pin at the bit rate of the connection. This makes it difficult to use the serial control interface if you want to operate in this mode. However, this is not a very commonly used mode, character asynchronous data transfer is far more prevalent than bit-synchronous and even in bit-synchronous mode, the data clock is normally supplied internally.

6.4. THE DATA INTERFACE

The K-Series modem ICs are designed to operate with a serial data stream. This is most convenient for standalone or box modem applications where the data to be sent is already in this form when it enters the unit. For applications where the data is passed to and from the modem over a parallel bus, a means of converting the data to serial format is needed. This can be a UART, a USART, a serial communications controller (SCC), or this function may be performed by code in the microcontroller. The K-Series parts with the "U" suffix incorporate an 8250/16450 compatible UART on-chip to perform this function in these applications, see section 6.6.4. Even in standalone modems, where the data is in serial form, conversion back to parallel may be needed when the controller intercepts the user data and performs command interpreting, buffering, error control or data compression. Whatever else you read or don't read in this section, take a look at section 6.4.8., Floating and Clamping the RXD Pin.

6.4.1. Serial Connection to a DTE (Data Terminal Equipment)

Where the system is to operate on data that is already in serial form, and no modification of the data format in the microcontroller is planned, the K-Series modem IC directly implements the required interface. Data for transmission is accepted at the TXD pin and received data is passed out at the RXD pin. In both cases, a ONE is represented by a logic HIGH level and a ZERO by a logic LOW. The data rate at which the interface operates is defined by the programming of the modem IC by the controller using Control Register 0. Data may flow in character asynchronous (start/stop) format in any modulation mode.

In DPSK and QAM modulation modes, which are synchronous modulation modes, it is also possible to transfer data synchronously at the modem/DTE interface. This means that the data is accompanied by a clock to define the timing of the data bits. In this case, three additional signals must be considered. The TXCLK pin carries the transmit bit rate clock and outputs a square wave with frequency equal to the configured bit rate. On the rising edge of this clock,

the K-Series IC samples the TXD input and places a bit of this value in the transmitted data stream. The data source should present new data bits on TXD around the TXCLK falling edge. RXCLK is a similar signal that provides the bit rate clock for the received data. A new received bit is presented by the K-Series IC on RXD at the falling edge of RXCLK. The data destination equipment should sample the received data line around the rising edge of RXCLK. RXCLK will be at a frequency very close to TXCLK but not normally identical to it. A separate clock must be provided because the modem receiver has to recover the precise data rate of the remote modem and output data at this rate. The remote modem has its own crystal reference clock, which may be up to 0.02% different in frequency from the local modem. The frequency of TXCLK is normally derived from the crystal clock in the modem. This is the case when the K-Series modem is placed in internal synchronous mode by writing 0001_2 to bits 5 to 2 of Control Register 0. In cases where the data source provides its own bit rate clock for transmitted data, put the modem in the external synchronous mode by writing 0010_2. Apply the DTE clock to the EXCLK pin of the K-Series IC, which then makes TXCLK fall into time with this clock. The relationship of TXD to TXCLK remains as described above. Note that the applied clock must be within 0.01% of the exact data rate in use. In certain circumstances, it is necessary to have the modem transmit data at the exact rate it is being received. By placing the modem in the slave synchronous mode by writing 0011_2 at bits 5 to 2 of CR0, it can be made to put TXCLK in step with RXCLK. An example of a situation in which this is needed is in remote digital loopback tests. This mode is also known as loopback timing or receiver timing.

6.4.2. V.28 (EIA232D) Drivers and Receivers

If the DTE is physically separate from the modem, the serial data is normally not moved between units at digital logic levels. Almost universally, at data rates at least up to 19,200 bit / s, the interface levels used are those specified in CCITT Recommendation V.28. These are entirely compatible with Electronics Industry Association (EIA) specification 232D, which also encompasses the signal definitions of CCITT V.24 and the pin definitions of International Standards Organization (ISO) 2110. You will therefore need to interpose drivers and receivers between the K-Series data interface pins and the DTE connector. The ubiquitous 1488 and 1489 ICs contain four drivers and four receivers, respectively. CMOS versions are available. A CMOS chip, the MC145406, with three receivers and three drivers is also available from Motorola. Table 6-1 summarizes some signals from the EIA232D and V.24 definitions that you may wish to include in your DTE interface. The terms DTE (Data Terminal Equipment) and DCE (Data Circuit-terminating Equipment) are used in V.24 to describe the terminal / computer and the modem, respectively. For a full explanation of these terms, refer to the glossary.

6.4.3. Connection to a UART

In an embedded modem application, where the modem forms a part of a larger system, the data for transmission is typically held in a memory and must be accessed over a parallel bus. A UART (Universal Asynchronous Receiver / Transmitter) is a device for converting byte-by-byte data into a serial start / stop format data stream. The 8250 UART is widely used and is the industry standard used in IBM PC™ personal computers. IBM AT™ class systems use an enhanced but compatible version of this UART, the 16450. The Silicon Systems 73M450 is a CMOS, 16450 compatible product that we would like you to consider using. The only necessary connections between the UART and the K-Series modem IC are the two data lines. Connect SOUT of the 73M450 to the TXD K-Series input and the RXD output to the SIN pin of the 73M450. Leave the TXCLK and RXCLK K-Series outputs unconnected as the UART cannot operate in the bit-synchronous data transfer format that requires these signals. The EXCLK input may be wired HIGH or LOW or used in the serial control interface, refer back to section 6.3.4, Using the Serial Control Interface.

6.4.4. K-Series Parts with Integral UART

Where a UART is needed as described above, you may choose a K-Series modem IC with an integral UART such as the 73K222U. This UART is functionally compatible with the 16450 standard but the IC as a whole has a very different pinout. The UART serial output (normally SOUT) is internally wired to the modem transmit data input at TXD. The UART serial input (normally SIN) can be taken from the modem received data output, from the RXD pin or in digital loopback from the UART serial output. The parallel bus interface to the UART section of the chip allows the data for transmission to be written as if to a 16450. Similarly, received data is presented at this interface as if it came from a 16450 UART.

6.4.4.1. Use of the UART Independent of the Modem

The design of the Integral UART family allows the UART to be used conventionally when the modem function is idle. When bit 7 of the Tone Register in the modem section is set to ONE by the controller, the UART serial data output appears at the TXD pin and the data input is taken from the RXD pin. If the part is to be used in the dual-port mode, RXD will be an output during the operation of the modem. You must therefore drive the RXD pin through a tri-state buffer which is put in the high impedance state for normal operation and is enabled for separate use of the UART.

6.4.5. Microcontrollers with Integral UART

Many microcontrollers, including the 8051 family, include a UART function on-chip. If such a controller is chosen, this can be made use of in a variety of ways. If the data for transmission is in the controller memory, it is simple to connect the on-chip UART to the K-Series part as described above in Connection to a UART. Alternatively, if

Pin #	Mnemonic	CCITT V.24 Circuit Number and Name	EIA 232-D Circuit Designation and Name	Direction
1	FG	Electrical equipment frame/power ground and shield	AA Frame Ground	N/A
2	SD (TD)	103 **Transmitted Data** Data originated by the DTE for transmission by the DCE	BA Send Data	DTE > DCE
3	RD	104 **Received Data** Data received by the DCE is sent to the DTE here	BB **Received Data**	DTE < DCE
4	RTS	105 **Request to Send** ON condition enables the DCE for data transmission	CA **Request to Send**	DTE > DCE
5	CTS	106 Ready for Sending ON condition indicates that the DCE can accept data	CB **Clear to Send**	DTE < DCE
6	DSR	107 **Data Set Ready** ON condition indicates that the DCE is ready to exchange control or data signals	CC **Data Sent Already**	DTE < DCE
7	SG	102 Common Return Common ground reference potential for all circuits	AB Signal Ground	N/A
8	DCD	109 Data Channel Received / Line Signal Detector ON - the received signal meets criteria for data reception	CF **Data Carrier Detect**	DTE < DCE
15	TC	114 Transmitter Signal Element Timing (DCE source) Synchronous transmit data bit clock provided by DCE to DTE	DB **Transmitter Clock**	DTE < DCE
17	RC	115 Receiver Signal Element Timing (DCE source) Synchronous receive data bit clock provided by DCE to DTE	DD **Receiver Clock**	DTE < DCE
20	DTR	108/2 **Data Terminal Ready** ON indicates that DTE is ready to transmit and receive data	CD **Data Terminal Ready**	DTE > DCE
21	SQ	110 Data Signal Quality Detector ON condition indicates that errors are not likely, off indicates high error probability	CG **Signal Quality Detect**	DTE < DCE
22	RI	125 Calling Indicator ON condition indicates that the DCE is receiving a ring signal on the telephone line.	CE **Ring Indicator**	DTE < DCE
23		112 Data Signalling Rate Selector (DCE Source) The DCE tells the DTE which data rate it is using, ON selects the higher rate or rates. (111) (DTE Source)	CI Data Rate Selector (CH Data Rate Selector)	DTE < DCE (DTE > DCE)
24	TC	113 Transmitter Signal Element Timing (DTE Source) Synchronous data bit clock provided by the DTE to the DCE	DA External Transmitter Clock	DTE > DCE

TABLE 6-1: V.24 / EIA232D Interface Definition

the data is transferred in serial form to another system (as in a standalone modem), the controller UART can pick up the data in parallel with the modem IC for examination by the controller firmware. In this case, connect the DTE transmit data to the UART serial data input as well as the K-Series TXD pin and connect the RXD pin and the UART serial data output in parallel to the DTE receive data. The controller can now receive and interpret commands from the DTE and send messages back. This, of course, is what the Hayes AT™ command set is all about. Make sure that the firmware enables only one of the K-Series RXD output or the controller UART output (not both) to drive the DTE receive data line at a time. A third possibility is to dedicate the controller UART to the DTE interface. The data would then be passed on to the modem IC by a second UART, perhaps integral in the K-Series chip, or a USART or SCC. With this arrangement you can process the DTE data before and after transmission to add data rate buffering, error control and compression to your system.

6.4.6. Connection to an SCC or USART

The K-Series modem can directly interface with a bit–synchronous data stream from the DTE as discussed above. Where bit-synchronous data is to be generated inside the equipment, an SCC (Serial Communications Controller) or USART (Universal Synchronous / Asynchronous Receiver / Transmitter) provides a means of interfacing to a parallel data bus. You will probably use such an arrangement to implement an error control protocol such as CCITT Recommendation V.42 or MNP™ in the controller. After the controller has divided up the data to be sent into packets and added address and control fields, it can send the data in bytes to the SCC. This device will then convert it to a bit-synchronous serial data stream, add the frame check sequence, add the frame flags and perform zero insertion. At the receiver, the SCC reverses this process and delivers the address, control and data to the controller in parallel with an indication of whether the packet contained any errors. In spite of the packet overhead, such a scheme achieves a higher character transmission rate than plain start / stop because the start and stop bits need not be sent with each character.

6.4.7. Direct Data Connection to the Microcontroller

If the data to be passed over the modem link is to come from and go to the microcontroller, it is also possible to dispense with an external device to format the data. The controller itself then must format the data as a serial bit stream for transmission and convert back to parallel storage at the receiver. This places a heavy processing load on the controller as it must manipulate the data at the bit rate and monitor the data interface. However, the cost savings achieved by eliminating the UART or SCC may make this worthwhile, particularly for the implementation of synchronous error control protocols.

6.4.8. Floating and Clamping the RXD Pin

Unless you have some other means of ignoring the data at the RXD pin, there will be times when you will have to make sure that it is held at ONE. The CCITT Recommendations V.22 and V.22bis and Bell specification 212A stipulate times during the connect handshake and retrain when the received data to the DTE must be clamped to binary one (mark). The K-Series modem ICs indirectly support this function with their capability to float (tri-state) the RXD pin. The RXD Output Control bit (bit 7) in the Tone Register controls this function. This bit is cleared to ZERO on reset and in this state, RXD is driven. The Receive Data bit is in an unknown state after reset so that the RXD pin will also be unknown. However, while in power-down, the chip's internal clocks are not running so at least RXD doesn't change. The controller should set the RXD Output Control bit to ONE to float the RXD pin before taking the chip out of power-down. This pin has a weak internal pullup which holds it at logic ONE if nothing else drives it. Thus, the controller can effectively clamp this signal as required without special logic. The internal pullup current may have a wide variation from 1 µA to 50 µA in some parts (check the data sheet), so you may want to supplement this with a resistor to VDD. Note that the K-Series chip itself clamps RXD to binary one when no carrier is detected by the receiver. The controller should nevertheless take over this function as described above before going off-hook.

6.5. THE INTERFACE TO THE TELEPHONE LINE

A certain amount of circuitry is necessary outside of the K-Series modem chip in order to form the interface to the telephone line. This consists of a two-to-four-wire hybrid and a DAA. The hybrid combines the modem's separate TXA output and RXA input into a signal which can be connected to the single pair of wires used to carry messages in both directions over the telephone local loop. This is done in such a way as to minimize the interference of the outgoing (transmitted) signal with the incoming (received) signal. This cancellation of the transmit signal can be done using a transformer with multiple windings (section 6.5.4) or differential amplifier circuits (section 6.5.5). The DAA, or Direct Access Arrangement, connects the combined signal to the telephone network without the use of a telephone handset. This method of connection is electrically far superior to the use of acoustic couplers, but requires the equipment manufacturer to take special care to preserve the safe operation of the network. After some preliminary paragraphs, we will discuss first the design of a DAA and then a hybrid circuit. We choose this order because we need to fix some component values in the DAA before we can calculate the gains required of the amplifiers in the hybrid.

6.5.1. Acknowledgements and Disclaimer

Silicon Systems wishes to acknowledge the invaluable help of the publications of Compliance Engineering, (271 Great Road, Acton, Massachusetts, 01720) in preparing this information. You can obtain a free subscription to the annual magazine, *Compliance Engineering*, by writing to the above address or telephoning (508) 264-4208. Also the Technical Support department of Midcom, Inc. has been of great assistance in the preparation of the information on line-coupling transformers.

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6.5.2. Important Design Considerations

When designing the telephone line interface, it is important to keep in mind four separate requirements for this circuit.

1. First, the circuit must not degrade the modem signals. The signal from the modem's transmit output (TXA) must reach the network with a minimum of distortion. Similarly, the received signal from the network must reach the input (RXA) with a minimum of distortion, noise and interference from the transmit signal. In both directions, the gain between the network and the K-Series IC must be correct. These requirements ensure the best performance of the modem system.

2. The connection to the telephone network (the DAA) must allow the network to continue to operate normally in all respects, even in the event of the failure of the modem itself. Before it can be sold in the U.S.A., any system intended for connection to the telephone network must be tested for compliance with FCC Regulations Part 68 which are concerned with this requirement. Other countries have their own, and generally more stringent, testing procedures.

3. The DAA must be designed to conform to safety regulations in force in the country of sale. In the U.S.A. it is advantageous to have equipment UL approved for safety.

In the U.K., safety testing is an integral part of the telecom approval process.

4. Finally, precautions must be taken to prevent radio frequency interference generated within the equipment from radiating from the wires connecting it to the telephone wall socket or other network terminal. FCC Regulations Part 15 concern themselves with electromagnetic interference. Part 15 class A approval is needed for sale in the U.S.A. and the more stringent class B approval is needed if the product is for use in a domestic environment.

6.5.3. The Direct Access Arrangement (DAA)

Figure 6-7 shows a basic Direct Access Arrangement with provision for detection of the ringing signal. The transformer T1 is the same one that appears later in the hybrid schematics as this component connects the two parts of the telephone line interface together. T1 couples the transmit signal from the hybrid to the network and the receive signal from the network to the hybrid while providing a high degree of common mode isolation. The primary of T1 (on the network side) also carries the D.C. "loop current" that flows in the network when the connection is active. The relay RL1 must be closed to activate the connection in the same way that a telephone handset must be lifted from the hook to place a voice call. For this reason, this relay is known as the "hookswitch" or "hook" relay and its closure is known as "going off-hook." When RL1 is open, or "on-hook," no current can flow in T1 primary and the line is freed in the same way a telephone frees the line when the handset is replaced on the hook. At this time, other equipment connected to the line may use the same line. The relay coil is normally operated via a driver circuit from a programmable output of a microprocessor, "OH" in the Figure. The capacitor C1, diode D1, resistor R1 and opto–isolator OP1 form a ring-detect circuit. When RL1 is on-hook (open) and a call arrives, a high voltage A.C. signal is placed on the line by the central office to activate the telephone bell or ringer. C1 separates this A.C. signal from the D.C. voltage on the line and causes a current to flow through R1. On alternate half cycles, the current is shunted through D1 and passes around the light emitting diode in the opto-isolator OP1. During the half cycles when the LED carries the current, the photo-transistor on the other side of the opto-isolator conducts and this is arranged in a circuit so as to change a logic signal to the microprocessor. By analyzing the pattern of this signal the microprocessor can tell that a ringing signal is being received and take the appropriate action.

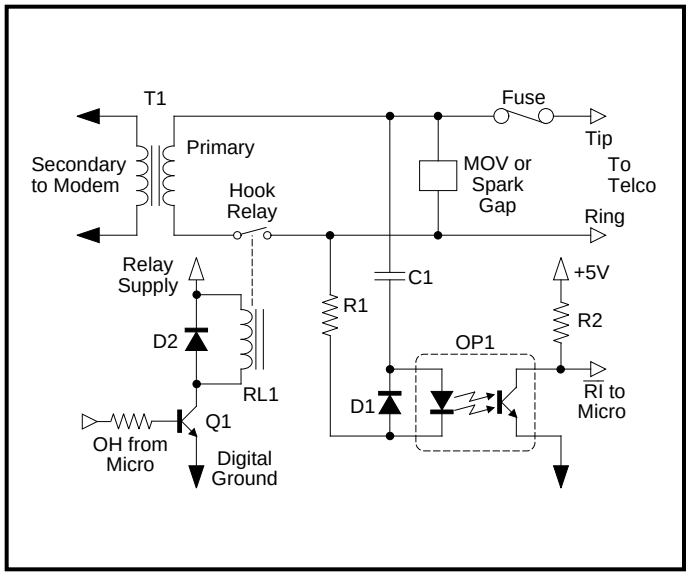


FIGURE 6 – 7: Simple DAA with Ring Detection

6.5.3.1. Choosing a Line-Coupling Transformer

It is essential to choose a line-coupling transformer that has been designed and manufactured specifically for this purpose. Since the transformer crosses the division between the network side of the DAA and the equipment side (see section 6.5.3.5, Using Protection Devices and an Isolation Barrier) it must be able to withstand large voltages between primary and secondary and also between either winding and the core. In the U.S.A., an isolation voltage of 1000 VAC is required although manufacturers generally offer 1500 VAC. Many countries are far more exacting. Australia, for example, requires a dielectric isolation of 3750 VAC. The U.K. requires a 2200 VDC dielectric strength test and an insulation resistance of over 100 MΩ with 500 VDC applied. In any case, ensure that the component you choose has been approved by the safety bodies of the countries in which you wish to sell your equipment.

The A.C. characteristics, such as the flatness of the frequency response and harmonic distortion levels, are important and must hold for the full range of loop currents expected in the primary. For use at 2400 bit/s, these qualities are more important than at lower rates so that your cost/performance tradeoff must be made with knowledge of the required data rates. You will probably want to speak to the transformer manufacturer on this subject; some publish recommendations in their data sheets. Silicon Systems has used extensively the Midcom 671-8005 transformer which is both UL recognized and CSA approved for use in telephone line interfaces. It is also physically small, but has good A.C. characteristics with up to 100 mA D.C. flowing in the primary. Midcom recommends this component for data rates up to 1200 bit/s and says that it is useable at 2400 bit/s (V.22bis). For the highest performance at 2400 bit/s, you will need a physically larger transformer such as the Midcom 671-8215.

The signal characteristics of the line-coupling transformer will be very important when designing the hybrid circuit. You will need to know how to load the transformer secondary in order that the primary presents the correct impedance to the network. You will also need to know the insertion loss of the transformer circuit, with its appropriate loads, in both the transmit and receive directions. It is therefore worthwhile to obtain an equivalent circuit from the manufacturer so that computer analysis may be used to obtain these figures and evaluate the result.

C_P	=	Primary Capacitance	150 pF
R_P	=	Primary D.C. Resistance	108Ω
L_P	=	Primary Leakage Inductance	0.224H
R_C	=	Core Loss Resistance	18 kΩ
L_L	=	Secondary Leakage Inductance	5.38 mH
R_S	=	Secondary D.C. Resistance	120Ω
C_S	=	Secondary Capacitance	180 pF

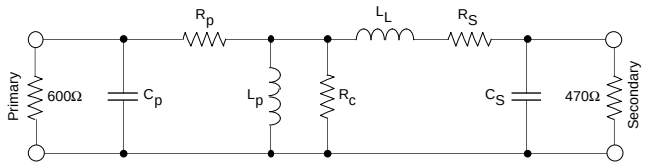


FIGURE 6 – 8: Midcom 671-8005 Equivalent Circuit

The alternative is to measure these values in a bench set-up. Midcom supplies an excellent equivalent circuit for the 671–8005, which is shown in Figure 6-8.

The transformer primary normally must be able to carry the D.C. loop current required to hold the telephone line, but see below for an alternative. The core and windings must have been designed so that the largest expected current can flow without saturating the core and compromising the A.C. characteristics. Loop current can vary widely, but in the U.S.A. is generally in the range from 20 to 80 mA although 110 mA is often reported as the absolute maximum. The D.C. resistance of the primary, plus any other components in series with the network connection, must be sufficiently low to allow the central office equipment to reliably sense the off-hook state. As a general guideline, below 200Ω is adequate, but see section 6.5.11, Special International Requirements, for a more detailed discussion of off-hook impedance in countries other than the U.S.A.

An alternative to allowing the loop current to flow in the transformer primary is to use some other circuit to pass this current and to A.C. couple the transformer. The transformer is still necessary to provide the isolation between the network and the equipment. The loop current may be drawn by an inductor called a holding coil or by an "electronic holding coil" circuit. Because the DC current in the local loop is also known as "wetting current," a transformer which carries this current in the primary is known as a "wet" transformer. Conversely, if the current is drawn elsewhere and no DC current flows in the primary, it is a "dry" transformer. The advantage of the dry transformer arrangement is that no gap is needed in the magnetic circuit to avoid saturation, so that much higher inductance is possible. This makes it possible to achieve better return loss characteristics in countries where this is important. For more information on this subject see section 6.5.11.1, Achieving High Return Loss Figures.

6.5.3.2. The Hook Relay

The purpose of the hook relay is to enable the equipment to gain the use of a normal switched telephone line to make a call and to release it at the end of the call. The network considers a line idle if over some period of time very little D.C. current is flowing in it. Conversely, it considers the line in use if the current flowing is large. The network equipment effectively limits the maximum current (except in France!) so that to gain the use of a line or "seize" the line, the equipment normally connects a D.C. path of low resistance between the network terminals (tip and ring). In the DAA shown in Figure 6-7, this is the primary of the line-coupling transformer. The hook relay closes (the equipment goes "off-hook") to seize the line, current flows and the central office senses that a call is to be made and allocates call routing equipment. At the end of a call, the relay opens (goes "on-hook") to drop the line, current ceases and after a short delay the central office disconnects the call and stops billing.

The relay contacts are on the network side of the DAA as discussed in section 6.5.3.5, Using Protection Devices and an Isolation Barrier, and the coil is on the equipment side. The component chosen must be able to withstand the high voltages between contacts and coil that are applied as part of FCC Part 68 testing. It should be approved for use in telephone line interfaces by the safety organizations of the countries in which you wish to sell your equipment.

Use a relay that has a wide separation between the coil and contact pins to prevent arc-over in the event of a surge on the network. Avoid reed relays which put the coil pins in among the contact pins; it is impossible to devise a good layout with these. See section 6.7.3, Layout Considerations in the Telephone Line Interface. Also make sure that the contacts themselves are of good quality and capable of carrying large current surges, another reason to steer clear of reeds. A very common failure mode for telecommunication equipment is the hook relay freezing closed after a current surge on the line.

In power sensitive applications, choosing a hook relay presents something of a dilemma. Most relays that are robust enough to offer a high survival capability in the field take a lot of current to drive the coil. This is especially true where the isolation requirements are greater than in the U.S.A. Only you can make the correct compromise for your product. A suggestion is to run the relay from the supply before the regulator and use a higher coil voltage so that it draws less current. American Zettler make a series of relays that use magnetic bias and a sensitive polarized coil to pick up on only 100 mW of power. The AZ 830 series has double-pole, changeover contacts, meets FCC requirements and has UL and CSA approval for use in the U.S.A. and Canada. The AZ 830-2C-6DSE is for a nominal coil voltage of 6V but

has a "must operate" voltage of 4.2V and so could be driven from a 4.5V minimum supply allowing a 0.3V drop in the switching device. With a coil resistance of 180Ω, the current drawn is only 26 mA. If you think this sounds like the output of the Hoover Dam, you have some difficult design compromises ahead of you.

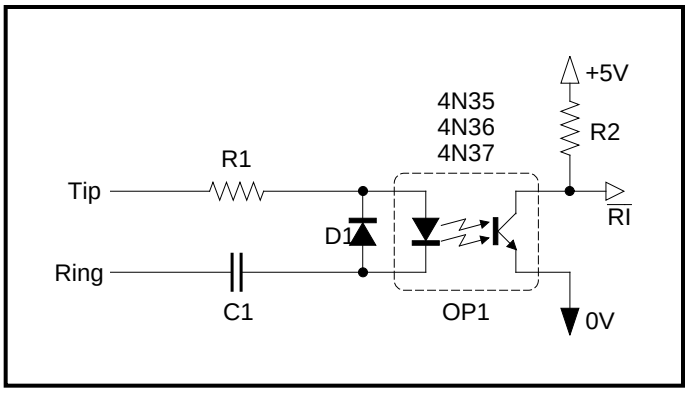
It is possible to use a solid state relay as the hook relay if certain precautions are taken. The switching device should be of a bi-directional type, such as back-to-back MOSFETS, as it is not always possible to predict the polarity of the loop current. The switch's OFF resistance should be large enough to meet the FCC requirements, see section 6.5.7.4, and the switch should be able to withstand the tip-to-ring high voltage tests. It is advisable to use a tip-to-ring protection device (see section 6.5.3.7) if a solid-state relay is chosen. In the off-hook state, the switch's ON resistance is in series with the network connection. This resistance is often quite significant compared to the 600Ω line impedance and should be taken into account when establishing transmit and receive path gains and impedance reflected at the line. Also, any uncertainty in the ON resistance will reflect in an uncertainty in the DAA insertion loss and hence in transmit level and receive gain. If you wish to explore this possibility further, you could start by looking at the Theta-J product line and compatible parts from AT&T Microelectronics.

If the hook relay is also to be used to perform pulse dialing, see section 6.5.3.4. For this use, the activation and deactivation times will have to be taken into account. Also, you may want to connect a snubber circuit across the relay contacts to soak up voltage transients generated by the inductance in the loop plant. Note, also in section 6.5.3.4., that more complex pulse dialing circuits are needed in some countries.

6.5.3.3. Designing the Ring Detection Circuit

The ring detection components from Figure 6-7 have been separated out and redrawn in Figure 6-9. As described above, the A.C. ring signal is separated from the battery voltage on the line and alternate half-cycles cause the opto–isolator to conduct and pull the output to logic low. A typical ring signal in the U.S.A. is 90 to 100V at 20 Hz. There are no legal requirements for the detection of the ring signal (neither the FCC nor UL are the least bit concerned whether or not your product actually works), so it is wise to make the ring detection circuit capable of detecting a broad range of signals. The broadest class of ring signals used in the FCC tests of on-hook A.C. impedance is type "B." This specifies a frequency range of 15.8 to 68 Hz and a voltage range of 40 to 150V RMS. If your ring detect circuit operates over this class of signals then it is very unlikely your product will ever fail to detect a valid ring. See also section 6.5.11.4, International Ring Detection Requirements.

We will now describe the design of a ring detection circuit which will operate with ring signals down to 40V RMS at 15.8 Hz and below but also has a low Ringer Equivalence Number of 0.36"B." This means that up to 13 such detectors could be connected to the same telephone



circuit without overload (13 times 0.36 is less than five), see On-Hook Impedance to the Network, section 6.5.7.4.

Choosing the Opto-Isolator:

The opto-isolator must be approved by the safety organizations of the countries in which the product is to be sold. The opto-isolator couples the ring signal from the network to the intelligent part of the product, enabling it to sense an incoming call. In doing so, it crosses the division between the network part of the DAA and the equipment part, see section 6.5.3.5, Using Protection Devices and an Isolation Barrier. It must therefore be specified to withstand the required isolation voltage between the LED on the network side and the photo-transistor on the equipment side.

Current Transfer, Saturation Voltage, and Leakage Current:

The second parameter of importance is the current-transfer ratio. This is the ratio of the current that flows in the photo-transistor to the forward current flowing in the LED. A high ratio will allow us to choose a higher impedance for C1 and R1 and achieve a lower ringer equivalence. Thirdly, we must check the saturation voltage of the photo-transistor to ensure that when it is turned on a good logic ZERO level will be presented. Only Darlington opto-isolators will normally fail this test, having a saturation voltage of about 1.0V, which is above the normal TTL logic low output voltage of 0.4 or 0.5V. Therefore, avoid parts such as the TIL119 or the 4N32 in the circuit. Lastly, we need to know the dark current, or the leakage current in the photo transistor when no current is flowing in the LED. For this example, we will choose a part from the 4N35, 4N36 and 4N37 family. These are available from several manufacturers with UL and V.D.E. approval and have isolation voltages of 3550V, 2500V and 1500V peak, respectively. The current-transfer ratio of all types is 100% at 10 mA in the LED, 25 °C at 10V collector voltage at the transistor. The saturation voltage is 0.3V maximum and the dark current is 2 µA maximum at 10V, 70 °C.

Selecting Resistor R2:

Resistor R2 can now be chosen to ensure that the signal is at a logic ONE when no current flows in the ring detect circuit. Both the dark current of the opto-isolator and the

input leakage current of the logic circuit must be allowed. Don't choose too high a value as this could lead to noise pick-up problems, but otherwise a high value will allow you to achieve a low ringer equivalence, e.g., use 20 kΩ, which is suitable for a total leakage of at least 50 µA. To bring the signal down to a logic ZERO, the photo transistor must draw a current of 0.25 mA, assuming a +5V supply. Now we can decide upon the required LED activation current. We should not rely upon the 100% current transfer ratio of the 4N36 family holding down to lower operating currents, higher temperatures or saturation of the transistor. However, after examining the graphs in the data book, 25% seems to be a reasonable compromise between caution and extreme pessimism. Thus you need 1 mA in the LED to be absolutely certain that it is at logic ZERO.

Selecting Diode D1:

Diode D1 is used to shunt current in the ring detection circuit during the half cycles when the LED in the opto–isolator does not conduct. A half-cent diode is quite adequate but it cannot be omitted for two reasons. First, the LED would probably go into reverse breakdown at the high voltages present. Secondly, if current were to flow in one half-cycle only we would have a rectifier. C1 would accumulate charge and current would flow in the LED for a smaller part of the cycle. Also, the product would fail FCC part 68 for drawing D.C. during ringing.

Selecting Capacitor C1:

The capacitor C1 is required to pass the A.C. ringing current from the network while blocking the D.C. battery voltage that is present at the network terminals when the line is idle (all connected equipment is on-hook). A large capacitance is needed because of the low frequency of the ring signal. Further, the capacitor should not dominate the impedance of the ring detect circuit because this would lead the double penalty of poor sensitivity at low frequencies and a high ringer equivalence. We will choose a value of 0.47 µF which has an impedance of 21.4 kΩ at 15.8 Hz. The battery voltage is 50 volts or so but this is not the limiting factor when choosing the working voltage of C1. The greatest stress is applied during the FCC Part 68 environmental tests when an 800 volt pulse is applied between tip and ring to simulate a lightning strike. To withstand this, a working voltage of at least 250VAC is recommended and furthermore the capacitor should have a self-healing dielectric so that if it does break down it does not become shorted.

Selecting Resistor R1:

We can finally choose the value of resistor R1 to make sure that enough current flows at the lowest ring voltage and frequency to pull the opto output low. We will use 22 kΩ because it is similar in impedance to C1 at 15.8 Hz and results in a total impedance of 30.7 kΩ at this frequency. A 40V RMS ring signal will cause 1 mA to flow in this impedance over about 30% of the cycle, thus ensuring enough current in the LED to activate the photo transistor. The impedance should not be over 40 kΩ to comply with FCC rules. At the other end of the frequency scale, the impedance of C1 and R1 in series at 68 Hz is 22.557 kΩ. This sets the minimum A.C. impedance of the DAA when in the on-hook state and gives a ringer equivalence number of 0.36 "B." Note that if C1 were smaller, a lower value for R1 would be necessary to get enough sensitivity at low frequency and the Ringer Equivalence Number (REN) would then be higher. During ringing, resistor R1 will dissipate a surprising amount of power. C1 will do little to reduce the power at 68 Hz, so for a conservative design, assume 150V RMS can appear across R1. 1 watt will be dissipated in a 22 kΩ resistor. It is true that the ringing signal is not present for long, so a 1/2 watt resistor could probably be used, but, in the interests of long-term reliability, you may not want to cut this corner.

If, after reaching the end of the design, you cannot get the REN you want and reliably pull $\overline{RI}$ to logic ZERO at the lowest ring frequency and voltage, then you must go back and choose an opto-isolator with higher current transfer ratio and increase the value of R2. You may decide that detection of ring signals down to the lowest frequency and voltage is not necessary in your application. In this case, you can adjust the design method above to use your own limits, but you will still have to meet the FCC impedance requirements over the full range, see On-Hook Impedance to the Network, section 6.5.7.4. In some countries, specifications must be met on what signals will be detected as a ring and what signals will not. Sometimes it is difficult to achieve the necessary sensitivity without being susceptible to false detection. In this case it is helpful to put series back-to-back Zener diodes in series with the ring current path to block all signals below the Zener threshold voltage. Calculating the REN with such a circuit is quite difficult.

Many variations on the basic ring detector circuit are possible although few offer any real advantages. Rewiring the opto-isolator so that the transistor pulls up on a resistor to ground allows you to get an active-high ring detect logic signal. This arrangement is not suitable for current-input logic such as the TTL families, but is perfectly suited for CMOS. You can use a Darlington opto-isolator in this configuration, obtaining a higher current-transfer ratio, but watch out for the higher dark current. If you are concerned about international markets, don't be tempted to use an opto-isolator with parallel back-to-back LEDs. It is not always enough to detect ringing by observing that the opto has turned on, the frequency and cadence of the signal may have to be analyzed by the microprocessor to avoid false ring detects. In the U.S.A. there are no tests for false ring detection, but you may want to guard against them anyway in the interests of product quality.

6.5.3.4. Pulse Dialing Circuits

The hook relay is often used to perform pulse dialing. In this situation, the relay is first closed to seize the line. After a delay to allow the central office to allocate switching circuits, the dial tone appears. The relay is then pulsed open in a carefully controlled pattern to indicate the telephone

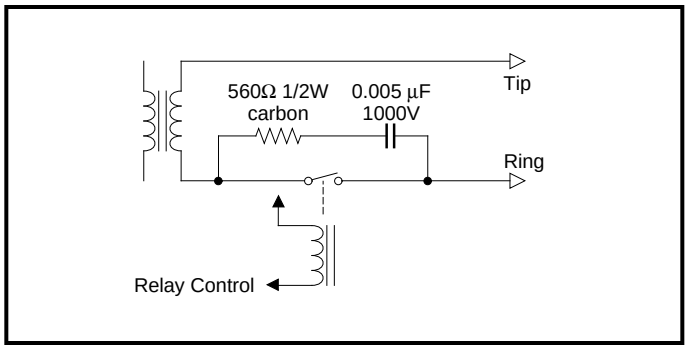


FIGURE 6 – 10: Pulse Dial Snubber Circuit

number dialed. The central office does not disconnect the line on the short breaks in the loop current, but counts them to determine the telephone number required. Unfortunately, the inductance of the transformer primary and the loop plant in the central office resists attempts to rapidly change the loop current for pulse dialing. In some countries, a spark quench circuit (snubber) consisting of a series resistor and capacitor placed across the relay contacts is sufficient to solve this problem. For the U.S.A. and Canada, a 560Ω, 1⁄4 watt carbon composition resistor and a 0.005 µF capacitor of 1 kV working voltage may be used as shown in Figure 6-10 to protect the relay contacts against spark-over. In other countries (e.g., Germany) it is necessary to switch any inductive elements out of circuit during pulse dialing, which requires an additional relay.

The RC network across the relay contacts serves another purpose as well; it absorbs enough of the energy stored in the magnetic field of the transformer to prevent locally generated fields from resetting the controlling microprocessor.

The U.S.A. has no regulations which specify the pulse rate and make/break ratio required for pulse dialing, although other countries do. Control over the make and break times to an accuracy of ±3 ms is needed in Canada, Japan and elsewhere, so a relay with reliable and repeatable activation and deactivation times is necessary. Where the pulse dialing circuit is separate from the hook relay, a bi–directional solid-state relay may be used. For information on controlling the relay, see section 7.2.3.1, Pulse Dialing.

6.5.3.5 Using Protection Devices and an Isolation Barrier

In designing a telephone line interface, you are arranging to pick up from the network signals as small as 5 mV and recover data from them. At the same time, the wires carrying these signals travel for many miles to the central office, frequently supported in the air on poles and in close proximity to power cables. You should not neglect the possibility of voltages greatly in excess of 5 mV appearing at the network terminals of your product. If the product fails due to a lightning strike or power cross, the customer will usually require you to fix it. Even if you don't charge for the service, frequent failures will reduce the perceived reliability of the product. Note that your product is unlikely to survive a direct hit on the telephone wires by lightning, but a far more common occurrence is the induction of high voltage surges by an electrical storm in close proximity.

6.5.3.6. High-Voltage Short-Duration Surge Protection

Three types of protection are advisable in the DAA, protection against high voltage, short duration surges between the network and earth, against surges between tip and ring and finally against sustained medium voltages between tip and ring.

Electrical storms in the vicinity of telephone cables are likely to cause large voltage surges on the network wires. The same surge appears at both tip and ring with respect to earth ground (free space) so that the entire network side of the DAA sees the voltage pulse in common mode. It is quite likely that some path will exist from other equipment circuitry to earth. Thus, a large voltage stress appears from the network connections to the rest of the equipment and an arc-over is possible. This can easily destroy components and cause the unit to fail. To protect against common mode surges, we recommend that you put as much physical distance as possible between components connected to the network and the rest of the equipment. This can be done by dividing the DAA circuitry in two; the network side and the equipment side. The line and phone jacks, the ring signal coupling components and some protection components will be on the network side. The hybrid, relay drivers, the rest of the electronics, the power supply and any conductive mechanical parts are on the equipment side. The product should be constructed so as to isolate the network components from the equipment parts via a definite physical separation or “barrier.” Obviously, some components will have to cross the barrier, in these are the line coupling transformer, the hook relay and the ring detect opto-isolator. These parts must be chosen to be able to withstand high voltages between their terminals which connect on the network side and those which connect on the equipment side. This construction technique is discussed in more detail in section 6.7.3, Layout Considerations in the Telephone Line Interface and shown in Figure 6-22. If you have an earth ground connection available in the equipment, it is possible to add surge arresters from tip to ground and from ring to ground as protection devices. Note that an earth (safety or protective) ground is essential for this purpose; do not use devices in this position connected to signal ground or isolated metal. The surge arresters should not conduct as a result of the application of the AC power line voltage between the network and the earth ground connection. In the U.S.A. this means that they should not begin to turn on at the peaks of 120VAC. Check UL regulations very carefully before using devices in this position, the wiring to earth ground must itself conform to very specific UL requirements.

6.5.3.7. Short-Duration Surges Between Tip and Ring

Protection against high voltages between tip and ring with a surge arrester such as a voltage-dependent resistor (varistor) or spark gap is generally a good idea. The device should be placed close to the network terminals or jack and connected via heavy traces. To limit the energy dissipated in this device, you may wish to add current limiting resistors in series with tip or ring or both on the network side of the protection device. A total resistance of 10Ω is typical. The arrester should not begin to conduct current during the various FCC Part 68 tests for on-hook impedance, see section 6.5.7.4. There should be no problem if the current is under 1 mA for applied voltages up to 200V. Outside of the U.S.A., a higher turn-on voltage may be needed. A varistor used as a surge arrester will offer only moderate protection to differential surges because of its rather rounded "knee" characteristic. A high voltage pulse from a low impedance source will still produce 400 to 500V between tip and ring in spite of the varistor. However, varistors have a fairly fast response time and turn on within the first 50 ns of the pulse. On the other hand, a spark gap actually reduces the voltage once it has turned on and can keep the peak voltage much lower than a varistor for a given threshold voltage. Against this weighs the fact that a spark gap will take about 100 ns to turn on and allows the full value of the surge across its terminals for that time. Avalanche diodes, having very fast response times and a hard clamping action, would solve this dilemma but for the fact that they are not robust enough to soak up the energy of lightning induced surges. Overall, we recommend a spark gap for tip-to-ring protection unless a solid-state relay is used, in which case we would suggest a spark gap plus a faster, clamping-type device.

6.5.3.8. Long-Duration Voltages between Tip and Ring

To protect your product against sustained power line voltages between tip and ring is not easy. The usual solution is to insert a sacrificial component, such as a fuse or resistor, which will open circuit before anything more costly to repair is damaged.

6.5.3.9. Using a Packaged DAA

DAA modules are available which include most or all of the functionality you may need. The manufacturers of these modules should have obtained partial FCC Part 68 approval for them and you can obtain a free pass on certain of the tests because of this. However, your system will still need to be tested and certified before you can sell it. Incorporating a modular, "pre-approved" DAA does not certify your system.

An example is the Midcom Series 681-0001 through 681-0099 "Registered Protective Devices" (RPDs). These modules not only provide the electrical characteristics required by FCC Part 68, but enforce a two second billing delay before transmission is permitted and automatically attenuate transmit levels above -9 dBm. About the only thing remaining for the testing laboratory to check is the transmitted spectrum.

6.5.4. Electromagnetic (Transformer) Hybrids

Having completed the design of the DAA, we must now think about the connection of the transmit and receive signals of the modem IC to the network via the line coupling transformer. This must be done so as to minimize the interference of the transmit signal on the receiver. The cancellation of the transmit signal from the receive path can be accomplished using special hybrid transformers. Circuits exist with either one or two transformers. In both cases, the balancing load absorbs half the power sent into the circuit from either direction so that an insertion loss of over 3 dB is unavoidable. Two transformer circuits offer a fully balanced four-wire port and are used in the network plant but are rarely used in modems because of their cost. A circuit using a single transformer is shown in Figure 6-11 for your reference. You will probably find an electronic hybrid preferable because of its lower loss and simpler transformer construction.

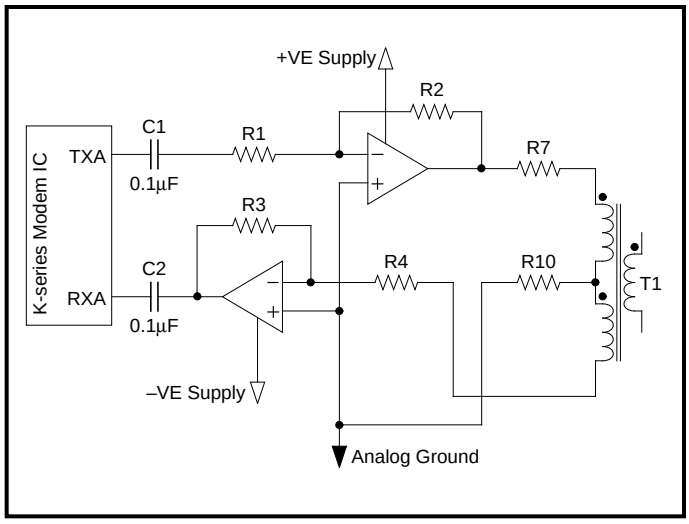


FIGURE 6 – 11: Transformer Hybrid Circuit

6.5.5. The Electronic Hybrid

Figure 6-12 shows a simplified schematic of a typical hybrid circuit using MC1458 operational amplifier, refer also to section 6.5.5.7, Capacitors in the Hybrid Circuit. The signal from the TXA pin of the K-Series modem is A.C. coupled to an inverting buffer amplifier consisting of R1, R2 and an op-amp. This adjusts the signal level as required and drives the low impedance of the line coupling transformer (T1) through the matching resistor (R7). The receive signal is taken from the transformer and passes through an inverting buffer amplifier consisting of R3, R4 and an op–amp. This adjusts the gain of the receive path and the signal is then A.C. coupled to the RXA pin of the modem. The signal at the junction of R7 and T1 will consist of the desired receive signal plus the transmit signal, which is not wanted in the receive path. R5 and R6 form a voltage divider to present some of the transmit signal to the non–inverting

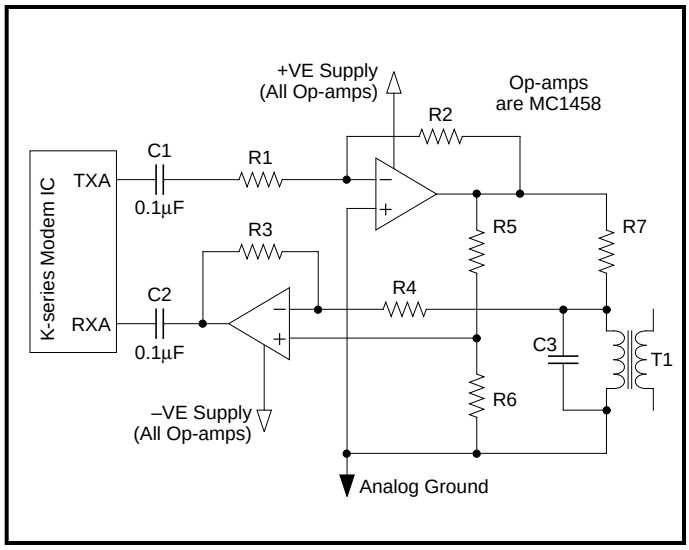


FIGURE 6 –12: Dual Supply Electronic Hybrid

input of the op-amp. In principle, this can remove the transmit signal from the output of the op-amp and therefore the RXA input of the modem. In practice, the operation of this circuit is compromised by the uncertainty in the impedance that the transformer will reflect at its secondary when connected to an actual telephone line. C3 compensates for the inductance of T1 which causes the transformer's insertion loss to vary with frequency. Without C3, the gain from TXA to the line and from the line to RXA will be different in the high and low bands used by the modem.

6.5.5.1. Choosing the Matching Resistor and Compensation Capacitor

The first step in designing the hybrid circuit is always to set the values of the matching resistor, R7, in series with the transformer secondary and the impedance compensation capacitor, C3. The purpose of both R7 and C3 is to ensure that the impedance seen by the telephone network looking into the DAA is within the desired limits. Almost universally, the nominal impedance is 600Ω resistive but different countries allow different degrees of deviation. The U.S.A. is unusual in not publishing any particular requirement. Most countries express their needs as the "Single Frequency Return Loss" or as the "Echo Return Loss" over a range of frequencies, both of which require interpretation (see section 6.5.11.1, Achieving High Return Loss Figures. The transformer manufacturer may give a recommended value for R7. For example, Midcom says that the 671-8005 is designed to reflect 600Ω at the primary with a 470Ω load on the secondary, thus we have used 475Ω for R7. If this parameter is not available, then it will have to be measured on the bench. Be sure to allow for any current limiting resistors in series with the telephone line on the primary side, the impedance required at the transformer primary will be reduced by the additional series resistance.

In the U.S.A. you are unlikely to run into problems if you choose R7 to give an impedance close to 600Ω at 1200 Hz and then choose C3 to give the same impedance at 2400 Hz. For the Midcom 671-8005 transformer, a value of about 0.047 µF is a good starting point and the final value can be determined by experiment. Some small adjustment to R7 may be necessary after connecting C3. In some countries, the impedance seen by the network at the equipment DAA terminals is very important. The inductance of the line coupling transformer tends to pull the impedance away from being purely resistive and makes the impedance increase with increasing frequency. This is compensated for only to a certain extent by capacitor C3 across the transformer secondary. You should also be aiming at this time to level out the insertion loss of the transformer across the band. This should be possible at the same time as leveling the impedance, but you may have to decide which takes priority. A powerful way of getting this all done is by modeling the circuit and using a linear circuit analysis program such as SPICE. The availability of models for line coupling transformers has already been mentioned in section 6.5.3.1. You will be able to try out various combinations of components and evaluate the impedance match and insertion losses in both directions before constructing the circuit.

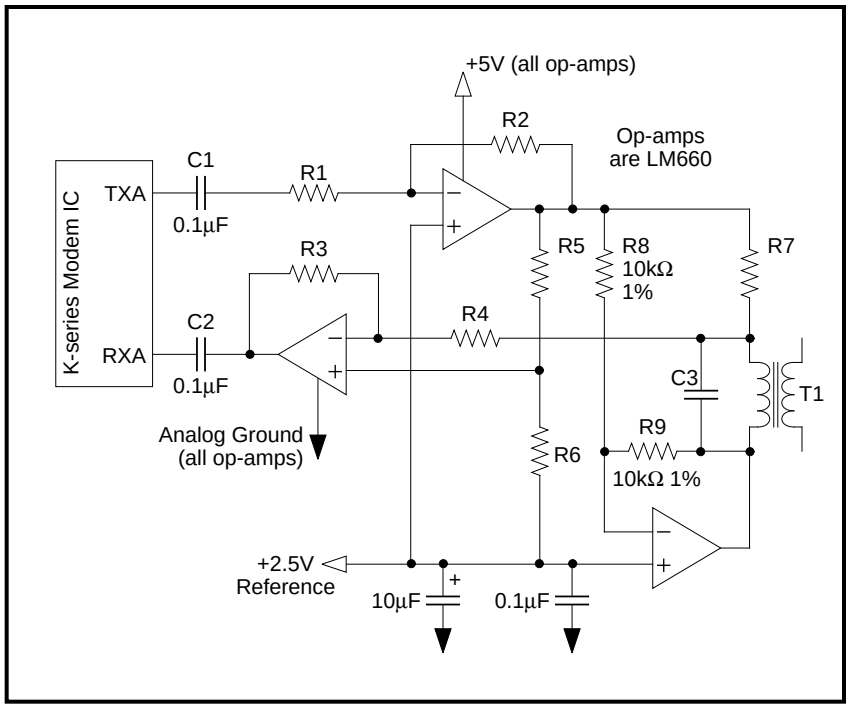
6.5.5.2. Designing a Hybrid for Dual Supply Operation

The schematic of Figure 6-12 is suitable for use when both positive and negative supplies of at least 5 volts are available for the operational amplifiers. These provisions ensure that no D.C. current flows in the secondary of the transformer and that a sufficient voltage swing is available at the output of the transmit buffer op-amp for the transmission of DTMF signals at 0 dBm. To choose values for the components you must have available the specifications of the line coupling transformer T1 and a preliminary design of the DAA. The data sheets of the K-Series modems indicate the gains needed from the TXA output pin to the line (transmit path) and from the line to the RXA input pin (receive path). These gains are also summarized in Table 6-2 for easy reference.

K-Series Family	Transmit Path Gain	Receive Path Gain
12 V (no suffix)	-10 dB	+9 dB
5 V ("L" suffix)	0 dB	+2 dB
UART (internal hybrid)	-8 dB	-3 dB
UART (external hybrid)	-2 dB	-3 dB

Table 6-2: Transmit and Receive Gain to and from the Line

6.5.5.3. Setting Transmitter Gain



The transmit buffer amplifier must be designed to give the correct gain from the TXA pin of the K-Series modem IC to the line terminals as above. The insertion loss of the transformer from secondary to primary must be known and allowance made for any series current limiting resistors in the DAA. Also, the impedance reflected at the secondary when the line terminals are correctly loaded with 600Ω must be known or measured. Let this impedance be RT1SEC. Now, the attenuation from the output of the buffer amplifier to the transformer secondary can be calculated as RT1SEC / (RT1SEC + R7). Adding the transformer and DAA insertion loss gives the attenuation from the buffer amplifier output to the line. The gain of the buffer amplifier must be chosen to give the required overall gain from TXA to the line specified in the data sheet. For example, in Figure 6–12, the Midcom transformer reflects 770Ω at the secondary when the primary is loaded with 600Ω so that the attenuation across a matching resistor (R7) of 475Ω is about 4.1 dB. The insertion loss of the transformer adds a further 2.9 dB of attenuation giving 7 dB total. The DAA circuit of Figure 6–7 introduces no additional loss after the transformer primary. To ensure a -10 dB gain from TXA to the line (assuming a 12V K-Series part) the buffer amplifier must introduce a further 3 dB of attenuation. The values of R1 and R2 have been chosen for this result. An alternative to all this mathematics is to build the circuit up and play with the resistor values until -10 dB gain to the line is achieved. The network terminals must be connected to a 600Ω resistive load. Keep the value of R1 at 10 kΩ or above to avoid overloading the TXA pin but otherwise choose low values to keep circuit impedances down. Be aware that by using bench methods you are not taking into account any variations in insertion loss that the transformer manufacturer may allow in his production process.

6.5.5.4. Setting Receiver Gain

Now the receive path gain may be set by choosing values for R3 and R4. To do this we must know or measure the insertion loss of the transformer from the line terminals to the secondary allowing for the load of the matching resistor value we have chosen. Again, any series current limiting resistors in the DAA must be included in the loss calculation. The gain of the receive buffer amplifier is simply the value of this insertion loss plus the required total receive path gain specified in the data sheet. The ratio of R3 to R4 can be chosen to provide this gain without reference to the balancing resistors R5 and R6. Note that R4 will add to the load on the transformer secondary so keep its value large compared to R7 in its effect when choosing R7. (In this discussion, we assume that its value is large.) For example, in Figures 6-12 and 6-13, the insertion loss from the line to the junction of R7 and the transformer secondary is 3.5 dB. To compensate for this and achieve the desired receive path gain of 9 dB (for a 12V part), the amplifier gain is 12.5 dB. Again, an attractive alternative to calculating the values may be to make bench measurements. Inject a signal at the line terminals from a 600Ω source impedance and make measurements at many frequencies in the 300 Hz to 3 kHz band. Keep the values of resistors R3 and R4 below 100 KΩ to maintain low signal impedances. It will in some cases be possible for the voltage supplied by the buffer via C2 to reach the maximum recommended voltage at the RXA pin of the chip. This is 0.3V outside the chip supply voltages, -0.3V and +12.3V with respect to GND for a 12V part. It is, however, safe to allow this if the current from the buffer is limited to 10 to 15 mA as the internal protection diodes at RXA can take this without adverse affect. If you are concerned that excessive current may flow on transients in the received signal, you can use Zener diodes to clamp the signal at a lower voltage or place a current limiting resistor in series with the op-amp output. The impedance at the RXA input is at least 50 kΩ, so a resistor of about 1 kΩ should be effective.

6.5.5.5. Optimizing Rejection of Transmitted Signal in Receive Path

The final part of the hybrid design is optimizing the rejection of the transmitted signal in the receive path. To do this we must first calculate the gain in the inverting path from the output of the transmit buffer amplifier to RXA assuming that the non-inverting input of the op-amp is grounded. Remembering the definition of RT1SEC from above, this gain is given by the formula R3•RT1SEC / R4(RT1SEC + R7). Now we must choose the ratio of R6 and

R5 so that the gain from the top of R5 to RXA, assuming the inverting path is disabled by grounding the junction of R7 and R4, is the same as the gain in the inverting path. This gain is given by R6(R3 + R4) / R4(R5 + R6). Equating these two formulae, it is easy to solve for R6 / (R5 + R6) = R3•RT1SEC / (RT1SEC + R7)(R3 + R4). Having decided on a value for either R5 or R6, we can then find a value for the other. Because the inverting and non-inverting path gains are now designed to be the same, the transmit signal is common mode, the net gain will be zero and no transmit signal will appear at RXA. This sounds good in theory, but in practice the telephone line presents anything but a 600Ω resistive load to the DAA line terminals. This, of course, means that the impedance reflected at the secondary will not be what we expected and an imbalance in the gain paths will occur, causing the appearance of some of the transmit signal at the receiver input. Even with a 600Ω resistor, the inductance of the transformer will cause phase shifts which will prevent the perfect cancellation of the transmit signal. The modem is able to separate the received signal from the transmit signal because it occupies a different frequency band so the modem will still operate correctly. Balancing the hybrid is a compromise at best but for the price of two resistors and a little math we might as well try. If you want to skip the math, experimentation is a perfectly good way to find values for R5 and R6 but make sure that the line terminals are loaded with a 600Ω resistor or any other model of the telephone network you may deem more appropriate. Choose values around 10 kΩ for the resistors; it is the ratio that affects the hybrid balance.

6.5.5.6. Designing a Hybrid for Single 5V Supply Operation

Operating the electronic hybrid from a single supply presents additional problems, especially if that supply is of a low voltage. The operational amplifiers have to be biased to operate with their outputs at around half the supply voltage to accommodate the A.C. signal. Also, for low voltages, there is not enough swing available at the output to drive the output to the correct power level. Figure 6-13 shows the schematic of a hybrid circuit that solves both these problems at once.

An additional op-amp is used to invert the signal from the normal transmit buffer amplifier so that the transformer and matching resistor can be driven differentially (also known as a "bridged" configuration). This doubles the available voltage swing at the transformer. Furthermore, as both op-amps are biased to the same D.C. level, there will be no net D.C. voltage between their outputs and the transformer may be driven without a blocking capacitor. We used to recommend an LM660 operational amplifier for use in this circuit because its output is able to swing close to both supply rails without distortion. However, we have had problems with this op-amp. For stability it requires a 68Ω resistor in series with the output pin and a 10 pF capacitor from the free end of this resistor back to the op–amp inverting input. We are working on a new recommendation. The reader is advised to keep pace with new operational amplifiers which may become available and offer better performance.

A value for the matching resistor, R7, should be arrived at by the same method as described in section 6.5.5.1. The gain of the transmit buffer amplifier should be made half of that calculated as described in section 6.5.5.2 because of the differential drive. The receive path gain is calculated exactly as before. Optimizing the transmit signal rejection is carried out in basically the same manner except that care must be exercised in calculating the transmit signal level at the junction of R7 and the transformer secondary because of the differential drive.

6.5.5.7. Using the On-Chip Hybrid of the Integral UART Versions

The K-Series family members with integral UARTs are 5V parts and aim to minimize component count in an embedded modem application. Therefore, the amplifiers required to implement the 5V single supply electronic hybrid have been included in the ICs. It is only necessary to calculate the values of the matching resistor and compensation capacitor as in section 6.5.5.1 to complete the connection to the DAA. Because the gain of the transmit and receive buffers are set internally, some assumptions are made about the attenuation from the transmit outputs through the DAA to the line, and from the line to the receive input. It is expected that the signal arriving at the line terminals, when loaded correctly with 600Ω, will be 8 dB below the differential output of the on-chip hybrid (TXA1 - TXA2). Also, it is assumed that the signal arriving at RXA will be 3 dB below the signal applied at the line terminals. Small deviations from these figures are unlikely to cause problems, however a transmit path gain higher than recommended may result in an unacceptably high power level into the network, which is cause for failure of FCC Part 68. You may have to use a higher value for the matching resistor than is necessary for the best return loss in order to ensure 8 dB of attenuation to the line. For example, you can't use the 475Ω that we chose above for the 671-8005 transformer because then the loss is only 7 dB.

Note that it is no longer possible to optimize the rejection of the transmitted signal in the on-chip hybrid circuit. The receive buffer amplifier is buried inside the chip and its non-inverting input is not available. However, the differential drive arrangement means that the junction of the matching resistor and transformer secondary stays close to the mid-point with only a small part of the transmit signal present. As this is where the receive signal is picked up, interference from the transmit signal is much reduced with respect to the dual supply hybrid circuit of Figure 6-12. In practice, the telephone network presents an impedance far removed from the ideal 600Ω so that efforts to precisely cancel the transmit signal in the laboratory are likely to fail in the field. No performance loss should ever be observed in field conditions as a result of the simplification of the hybrid circuit. It is, of course, possible to use an external

hybrid as for other K-Series families, just ignore the TXA2 pin and use TXA1 as the normal TXA output. The required transmit and receive path gains are given in Figure 6-2.

6.5.5.8. Capacitors in the Hybrid Circuit

To simplify the schematics, only components needed for fundamental circuit operation have been shown in Figures 6-12 and 6-13. There are several places where additional capacitors can be used to good effect.

A capacitor across R2 can be used to turn the transmit buffer amplifier into a low-pass filter. This is helpful in reducing the level of spurious signals sent to the line above the intended frequency range and is strongly recommended. FCC Part 68 specifies maximum levels for signals above 4 kHz and a capacitor in this position is necessary to meet this requirement. The filter corner frequency should be a couple of octaves above the maximum frequency transmitted so as not to interfere with the signal, i.e., at about 12 kHz. Some countries have very stringent requirements for low out-of-band signal levels transmitted to the network. For approval in these countries, it may be beneficial to replace the buffer amplifier with a higher order low-pass filter circuit. The filter must still have the gain required to adjust the transmit signal level as described in section 6.5.5.3. A second order filter, which still uses only one op-amp, enables the corner frequency to be moved lower and rolls off the high frequencies twice as fast as a first order circuit. For more on this topic see section 6.5.11.2, Reducing Out-of-Band Signal Levels.

In the same way, a capacitor across R3 turns the receive buffer amplifier into a first order low-pass filter. This can help to prevent any high-frequency interference coming in from the telephone network from entering the modem receiver. The corner frequency should be chosen in the same way as on the transmit side.

An alternative to balancing the hybrid with a 600Ω resistive load at the line terminals as described above is to balance it for a typical telephone line. If you can find out what a typical line looks like, it will probably be slightly capacitive. To compensate for this, it will be necessary to put a capacitor in parallel with R6.

6.5.6. Four-Wire Operation

Although all K-Series parts are designed for use on two-wire telephone circuits, there is no reason why they should not be used on four-wire circuits if this is desired. Any of the electronic hybrid circuits already described can be used with some simple modifications. Separate line coupling transformers are needed for the transmit and receive pairs. Obviously, the transmit buffer amplifier should drive the transmit transformer via the matching resistor as before. The receive transformer will require a load resistor and capacitor across its secondary equal in value to R7 and C3 on the transmit side. The receive buffer amplifier input at R4 is taken from one side of the receive transformer, the other side being grounded. The non–inverting input of the receive buffer amplifier should not receive a portion of the transmit signal via R5 and R6 but instead should be connected to a signal ground. Four wire circuits are normally leased and therefore do not carry loop signalling current. Thus it is possible to use inexpensive "dry" transformers with excellent A.C. characteristics which are not designed to carry D.C. current in the primary.

6.5.7. Compliance with FCC Regulations Part 68

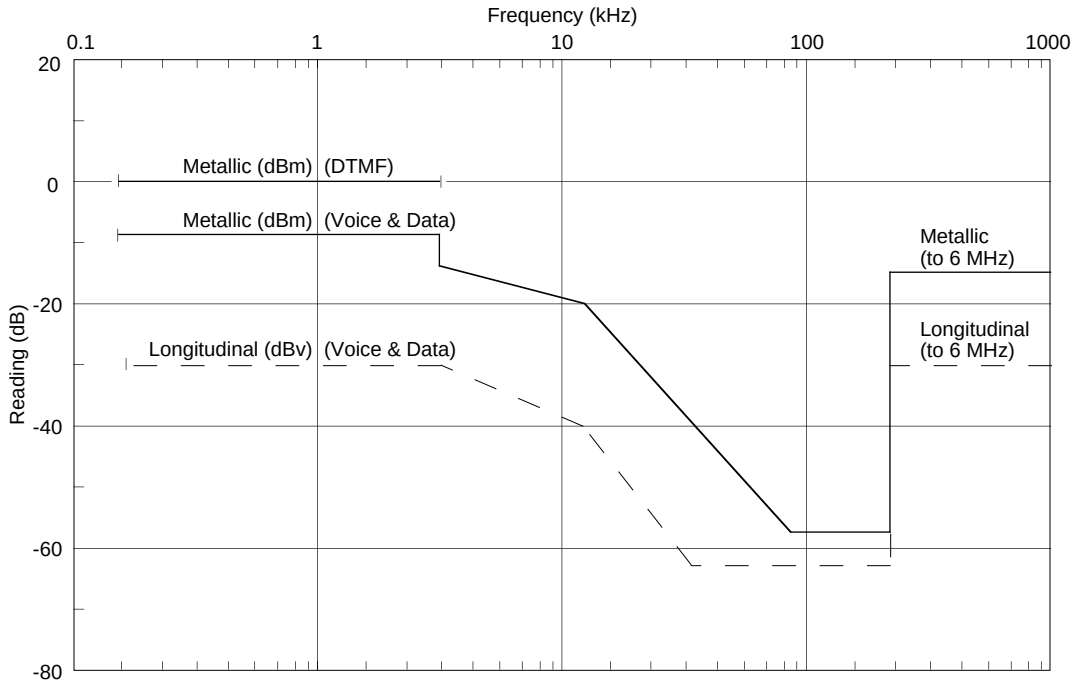
Before a product which may be connected to the telephone network can be offered for sale in the U.S.A., it must be tested by an approved laboratory for compliance with FCC rules, Part 68. Once a representative production unit has been passed for sale, it is not necessary for the manufacturer to perform ongoing testing unless a design change is made which may affect compliance. However, the FCC may obtain a field sample of the product and re-test at their own expense at any time. In the event of a non–approved product being offered for sale or an approved product failing the tests, the FCC can require the manufacturer to withdraw the product from sale and recall any units already in the field. This sort of situation is to be avoided at all costs so that a proper understanding of the requirements of Part 68 are important at the time of initial product design.

6.5.7.1. Hazardous Voltage and Current Tests

Part 68 specifies tests designed to ensure that any likely fault conditions developing in the tested product (or any equipment to which it may be connected) do not give rise to hazardous voltages in the telephone network. Full details of the tests are beyond the scope of this text, however, the DAA circuit must be able to withstand the application of 1000V A.C. at 60 Hz between the telephone line connections and ground. Ground includes signal ground for any input / output connections to the unit and also any exposed metal surfaces. On the application of such voltages, the current flow must not exceed 10 mA.

It is very unlikely that your product will fail these tests if you have constructed it with a view to avoiding damage from common mode surges at the network. Section 6.5.3.5, Using Protection Devices and an Isolation Barrier and section 6.7.3, Layout Considerations in the Telephone Line Interface describe how you can physically separate network and equipment components with a barrier. It is not a good idea to cross this barrier with any components that are not absolutely necessary and might cause current flow during these tests.

Similar tests are performed to demonstrate dielectric strength in the power supply if line power enters the unit. 1500V A.C. is applied between the power supply input leads and signal grounds, the power supply secondary ground and exposed conductive surfaces. As before, not more than 10 mA can flow.



Signal Power Limits for DTMF Signalling

The permissable level from 100 Hz to 4 kHz must be less than 0 dBm averaged over a 100 msec period. It is measured with the same test set-up used for in-hand voice or data transmission. No limits are prescribed for signals above 4 kHz, however.

FIGURE 6 – 14: U.S.A. Power to Network Limitations

6.5.7.2. Power Levels Transmitted to the Network

For a variety of sound engineering reasons, the amount of power that can be applied to the telephone network is limited, both in the useful audio frequency range and outside this. In the U.S.A., Canada and the U.K., in the band 200 to 4000 Hz, the total RMS power, averaged over any 3 second period, may not exceed –9 dBm into a 600Ω load. This is equivalent to a power of 9 dB below one milliwatt, which is 0.125 mW. This doesn't sound like much, especially if you own a Hi-Fi. For obvious reasons, you will want to transmit at as high a level as possible but the quickest way to fail Part 68 is to transmit at -8.99 dBm. The usual solution is to give away 1 dB and aim for –10 dBm, keeping manufacturing tolerances tight enough to ensure that no units slip over the limit. This power level limit applies to all transmitted signals in all modes of operation at all times with the exception of DTMF signalling. The testing laboratory may want you to be able to put the system into some special test modes for continuous transmission of answer tones and calling tones. Countries other than the U.S.A. may have different limits on power level, for example, in Germany you can transmit at up to -6 dBm and in Japan the level reaching the central office must not exceed -15 dBm.

The power limit above does not apply to DTMF tones sent at the establishment of a connection to indicate the telephone number required because these travel only as far as the local central office. These can be at a level of up to 0 dBm. The use of DTMF tones to convey information to the remote station is becoming very popular these days with automatic voice messaging systems, telemarketing systems and answering machines which you can program remotely. According to a strict interpretation of FCC Rules Part 68, the use of these systems is illegal because the level transmitted over the network can be above -9 dBm. Nothing much is being done about this because the installed base is so large and diverse, but if your product has the capability to send DTMF tones once the connection is established, you may want to consider limiting the power at that time to the usual -9 dBm.

In the U.S.A. it is possible to order a special telephone service for data transmission where the loss of the wires as far as the central office can be offset by increased transmit level. This is known as "programmed" level as opposed to the normal service which is "permissive" level. A special wall jack (RJ45) and cable must be used with extra circuitry inside the modem to read the value of a resistor installed inside the jack by the telephone company. With line quality as good as it is these days, the benefits of this arrangement are substantially offset by the extra complexity.

The signal spectrum in the normal transmission band is largely defined by the modulation standard in use. However, you should be aware that in all countries that use an in-band signalling scheme to communicate between exchanges, there are certain restrictions on what you can transmit. In the extreme case, a modulation standard may be unusable where it violates these restrictions, for example, Bell 103 cannot be used in most European countries. The U.S.A. and Canada use a 2600 Hz tone for signalling and a restricted band is defined from 2450 to 2750 Hz around this frequency. The power transmitted in this band must not, on average, exceed the power in the 800 to 2450 Hz band or the signalling

system will be falsely triggered. All common modulation standards automatically obey this requirement. In the rest of the world, the most common signalling frequency is 2280 Hz and the controlled band is typically 2130 to 2430 Hz. The United Kingdom requirement, for example, is that the power in this band be no more than 12 dB above the power from 900 to 2130 Hz. This explains the absence of Bell 103 modems in the U.K. as the high band marking tone falls right in the restricted band. There is another restricted band in the U.K. from 450 to 900 Hz and this also rules out Bell 202 reverse channels. In some countries, it is also considered possible for a V.22 spectrum to trigger the signalling system. On average, the high band energy is spread wider than the restricted band, but due to its random nature it can heap up in the narrower band for short periods of time. To prevent this from interfering with signalling, a guard tone must be transmitted along with the high band data signal to hold up the energy outside the restricted band. Information on the guard tone is provided in the V.22 and V.22bis recommendations and all K-Series modem ICs that use these modulation modes can provide either the 1800 or 550 Hz tone.

Above 4 kHz, the objective should be to transmit as little power as possible. Figure 6-14 shows a graph from FCC Part 68 of maximum permissible power as a function of frequency up to 6M Hz. Note that these interference signals are measured in dBV (decibels below one volt) rather than dBm and that the tests are performed with a lower value load resistor connected in the circuit that simulates the local loop. Other countries have similar requirements, the most stringent being that for the United Kingdom. See section 6.5.11.2, Reducing Out-of-Band Signal Levels.

In addition to the signal level between the tip and ring network connections, the testing includes any common mode signals (signal components identical in amplitude and duration) present from tip and ring to earth ground. The DAA circuit design should avoid any asymmetry between tip and ring that could give rise to common mode signals.

6.5.7.3. Maintaining Balance in the Network

The telephone network maintains its freedom from crosstalk and power-line hum pickup by being well balanced with respect to earth ground or free space. The DAA must be designed so that each side of the telephone network connection has the same impedance with respect to earth ground. This is easily done if no connection is made from the network part of the DAA to anywhere else except through relays, the opto-isolator and the coupling transformer. If it is absolutely necessary to make such a connection, for example to decouple EMI (see section 6.6.4, Suppression at the Telephone Cables), the same configuration must be used on both tip and ring. Measuring balance on the bench is not easy, although circuits are available, so we recommend total avoidance of anything that might cause imbalance.

Any product which is allowed to connect to the public switched telephone network is assigned a ring equivalence number (REN). The REN denotes the fraction of the permissible on-hook load that any given unit of the customer premises is putting on the public network.

REN for a loop-start circuit is calculated from the following four values:

1. The on-hook DC resistance (using up to 100 volts as a source) compared to 25 MΩ.
2. The on-hook DC resistance (using from 100 to 200 volts as a source) compared to 150 kΩ.
3. The DC current that flows as a result of applied AC ringing compared to 0.6 mA.
4. The impedance during the application of AC ringing compared to 8000Ω.

Equaling each of the listed values will give a REN of 1; lower values of resistance or higher values of current will cause the REN to increase.

The sum of RENs of all units which bridge a telephone line may not exceed 5.0. If an equipment has a REN of 5.0, no other equipment can be connected to the same line. In order not to load down a telephone line, it is desirable to keep the REN low. The desirable value for REN is about 1.0.

6.5.7.4. On-Hook Impedance to the Network

In order for the network central office equipment to operate correctly, the DAA must present a high D.C. impedance to the network when in the on-hook (idle) state. By high, here, we mean at least 5 MΩ up to 100V between tip and ring. Between 100V and 200V, a lower impedance of at least 30 kΩ is permitted. If the modem is to share a line with any other equipment, every effort should be made to exceed these figures by a factor of at least five in order not to arrive at too large a Ringer Equivalence Number. If a circuit similar to Figure 6-7 is used, the only element that is likely to compromise the D.C. on-hook impedance is the protection device between tip and ring. This should be chosen not to pass more than a few milliamps at up to 200V D.C. applied.

In addition to the D.C. impedance requirement, the on–hook A.C. impedance must also be within a certain range. The minimum impedance is specified so that the central office can supply the ringing signal. Because of the wide variety of ringing signals in use in the U.S.A., it is customary to design to meet the most difficult, which is type “B.” This requires that the A.C. impedance (A.C. voltage applied divided by A.C. RMS current) be no lower than 3000Ω for frequencies between 15.3 Hz and 68 Hz and voltages between 40 and 150V RMS. A maximum impedance is also specified for equipment which is able to detect a ringing signal. This allows the network administration to easily detect the presence of such equipment on a phone line. Under the same set of conditions described above, the impedance must not be more than 40 kΩ. For more detail, please refer to standard EIA-496A, interface between DCE and PSTN.

As a part of the A.C. impedance tests, Part 68 also includes a test for D.C. current resulting from the application of the A.C. ringing signal to the unit. The current must not exceed 3 mA over the range of frequencies and voltages specified above. Only a poorly designed ring detection circuit or badly chosen tip-to-ring protection devices will cause this test to be failed. Finally, at this time the A.C. impedance from both tip and ring to earth ground is measured. This must not be less than 100 kΩ. If the ring detection circuit of Figure 6-9 is used, there can be no problem meeting this requirement.

6.5.7.5. Other Requirements of Part 68

Part 68 has a number of miscellaneous tests grouped under the general heading of Billing Protection. The purpose of these tests is to prevent you from building a device which can get use from the telephone network without you paying for it. Passing these tests is quite simple. In equipment that automatically answers an incoming call, do not allow any signal to be transmitted onto the line for at least 2 seconds after the hook relay has closed. When the equipment is on–hook, ensure that the spurious energy, if any, that is sent into the network is below -55 dBm. Make sure that the effective D.C. resistance from tip to ring in the off-hook state is less than 200Ω. The K-series modems themselves take care of certain requirements regarding the concentration of transmitted energy into bands used for in-band signalling, but make sure you turn on the V.22 guard tones where legally required.

If your product can be disconnected from the telephone network, Part 68 requires that the connection be made using the standard 6 position RJ11 jack. Many countries outside the U.S.A. are beginning to accept this connector also, but some like the United Kingdom have evolved different standards.

6.5.7.6. Part 68 and Environmental Stress

The FCC is interested in protecting the telephone network, even in the event of the failure of connected equipment. If your product meets the requirements of Part 68 on the first test, the laboratory will perform a second series of severe environmental tests. Your product must also pass this second series of tests to receive approval, although it need no longer function as designed.

To be more specific, attempts to make the product fail include vibration in its shipping container, temperature and humidity cycling, dropping it on a tiled concrete floor and simulated lightning strikes on the telephone line connections and the A.C. power connection. Any differences in the results of tests after the environmental stresses have been performed may require explanation before approval is obtained.

The lightning strikes consist first of 1500V pulses from tip and ring to ground. The components crossing the "high voltage isolation barrier" between the network side and the equipment side of the DAA should be chosen to withstand this voltage without failure. Absorbing these pulses in protection devices can seem like a good idea but first see sections 6.5.7.1, 6.5.7.3, and 6.5.8. Secondly, 800V pulses are applied between tip and ring. This isn't quite as bad as it sounds because the pulses are short enough not to burn up the transformer. In fact, it doesn't matter if the unit doesn't work after these pulses as long as it doesn't catch fire and passes all the other tests again. Capacitors in the DAA should be of fairly high working voltage to resist breakdown and in any case be constructed of a self-healing dielectric to avoid shorts. If you want your product to survive these tests and still work, some extra protection components are advisable. A metal–oxide varistor or spark gap from tip to ring can be effective in reducing the amplitude of the pulses and resistors of 5 or 10Ω and are often placed in series with tip and ring on the network side of this component. However, watch out for D.C. on-hook resistance, see section 6.5.7.4, On–Hook Impedance to the Network, and use 1/2 watt carbon composition resistors which have higher thermal inertia than small metal film types. Series back-to-back Zener diodes across the transformer secondary can be effective in preventing the pulses from getting into the sensitive electronics of the hybrid and modem, but choose values which will not interfere with normal modem signals.

The final tests are 2500V pulses applied from phase to neutral of the A.C. power input, if present. Be warned also that most countries in the world use higher voltages for all these tests.

6.5.8. Compliance with Safety Regulations in the DAA

All manufacturers of electronic equipment should be familiar with the product safety standards set out by UL and the benefits of conforming to these standards. Most of these standards relate to matters not unique to modems or connection to the telephone network and a discussion of them would be out of place here. However, UL Standard 1459 for Telecom Apparatus includes some interesting tests of which you should be aware. The performance of some tests will depend on whether or not power line voltage enters the unit.

In order to test for fire hazards, the testing laboratory will place the unit on a piece of cheesecloth and apply A.C. voltages at the network connections. The unit may cease to operate but a fire should not start. 240V A.C. is applied in common mode to the line terminals with respect to chassis ground through 10Ω resistors. This test is easy to pass unless some path exists from the network side of the DAA to ground, a good reason not to connect protection devices such as varistors here. The more disturbing test is the application of up to 600V A.C. between tip and ring through various current limiting resistors for various periods of time. A 1.6amp slow-blow fuse placed in the circuit should also not open during this test if the unit is designed to operate unattended. The test is performed with the unit in both the on-hook and off-hook states. Almost inevitably, large amounts of energy will be dissipated in the unit during these tests and something or other will burn out. A

fresh unit is required for each test in the series and this can get expensive and time consuming. Fortunately, there is a quick way out. Putting a suitable fuse in series with the network connection makes the unit exempt from this test. The fuse should be rated at 1A or below and can be of the slow-blow type. The harshness of the fire hazard tests has caused something of an outcry and the test procedure may still be evolving. Check with a competent consultant for the latest information in this area.

6.5.9. Compliance with FCC Regulations Part 15

Universally, prevention is better than cure so that the first line of defence against failure of Part 15 is to avoid the generation of any high-frequency radiations. In section 6.6, Design for Compliance with FCC Regulations Part 15, some techniques for minimizing EMI are discussed, however you should note that the connections to the telephone network provide an additional opportunity for interference to escape from the product enclosure and cause problems. The FCC regulations require that overall radiated emissions be measured with cables connected and that conducted emissions measurements be made on each cable. The cable from the line jack or terminal strip to the wall socket can act as an antenna and radiate high-frequency signals picked up from the electronics. If a telephone handset is connected for use when the modem is inactive, then its cables present a similar danger. Because of other engineering factors which must be considered in suppressing EMI at the telephone line interface, we have included section 6.6.4, Suppression at the Telephone Cables, to discuss this issue.

6.5.10. Printed Circuit Board Layout of the Telephone Line Interface

Because of particular engineering factors which must be considered in the layout of components and traces in the DAA, we have included Layout Considerations in the Telephone Line Interface, section 6.7.3, to discuss this issue.

6.5.11. Special International Requirements

Given the information presented in this section so far, you should have no real problems designing a telephone line interface for use in the U.S.A. Your skill and judgment will of course come into play in achieving the desired performance at the lowest cost and making other design tradeoffs. To obtain approval in Canada also, you must only be aware of the additional requirements for pulse dialing, return loss etc. The real challenge in DAA design lies in Europe and Australia. We have mentioned in passing some points of which you should be aware for international designs. Now we will look in more detail at certain areas where you must be particularly careful.

6.5.11.1. Achieving High Return Loss Figures

Although the U.S.A. has no special requirement for how well the impedance at the modem line terminals matches the nominal network impedance, most other countries do. Canada, for example, requires a Single Frequency Return Loss (SFRL) of better than 3 dB at all frequencies between 200 and 3500 Hz and an Echo Return Loss (ERL) of better than 11 dB from 500 to 2500 Hz. This turns out to be a breeze. On the other hand, the U.K. requires an SFRL of better than 14 dB from 200 to 4000 Hz plus the reactive component must not be greater than 50Ω. This turns out to be very difficult and requires special components.

Return loss is a measure of the match between the impedance of a line termination and the line itself. If the impedance of the line is Z_0 and the termination or load is Z_L then the return loss is given by the formula:

$$RL = 20 \log_{10} \left| \frac{(Z_0 + Z_L)}{(Z_0 - Z_L)} \right|$$

The network administration will choose a circuit to provide Z_0 that they feel is representative of their plant and perform the measurements using this as a reference. The most common values are 600Ω resistive and 600Ω in series with a capacitor of 2.16 µF. The Z_L presented by the equipment under test will typically vary widely with frequency. SFRL is the return loss measured at a particular frequency. To get the ERL, the SFRL figures are averaged over a specified frequency range.

The best way of achieving truly spectacular return loss is by using a "dry" line coupling transformer and an electronic holding coil. The schematic of a DAA using this arrangement is shown in Figure 6-15. The transformer is here, A.C. coupled to the line by capacitor C2 so that no D.C. current flows in the primary. Without the need to handle D.C., a transformer can be chosen which is un-gapped (has a continuous magnetic circuit) and therefore a much higher primary inductance. This makes its characteristics far more constant with frequency, particularly at the low end where gapped ("wet") transformers become lossy and inductive. The line holding current is now diverted through an electronic circuit designed to pass this current while reflecting a high A.C. impedance. This circuit simulates the effect of a large inductor and is often known as a gyrator.

The operation of this circuit is as follows. The diode bridge merely serves to make sure that whatever the sense of the voltage at the line terminals, the rest of the circuit gets the correct polarity. It adds a voltage drop of 1.4V, but apart from that, we'll ignore its presence. R5 and R4 form a voltage divider to present a proportion of the tip to ring voltage to the base of Q2. Q2 draws current from the line, lowering the tip to ring voltage to the point where the bias at its base is sufficient to maintain the current. R3 introduces negative feedback to stabilize this arrangement. If Q2 draws too much current, the extra voltage drop across R3 reduces the base to emitter voltage and the current is forced back to the correct value. The reverse happens if too little current flows. The purpose of C3 is to eliminate the A.C.

signal from the base bias of Q2. Without this component, the circuit would present a low impedance to A.C. signals because of the action described above for D.C. However, with a steady D.C. bias at the base, Q2 acts as a constant current sink and the fluctuation of the collector voltage due to signals on the line does not cause a change in the current drawn. Thus, to a first approximation, the A.C. load placed on the line by this circuit is equal to R5. Q2 is a Darlington so that reasonably large values of R5 and R4 can be used to supply the base current.

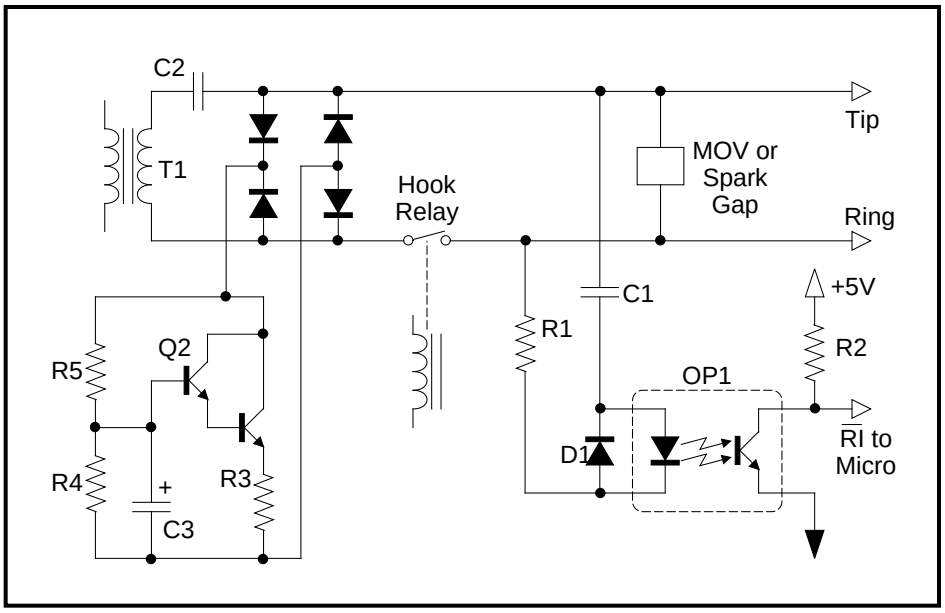


FIGURE 6 – 15: Electronic Holding Coil Circuit

To choose values for the components in this circuit, you need to know the required voltage / current characteristics and the peak signal amplitude at the line terminals. The D.C. and A.C. characteristic need to be carefully balanced. Since we cannot predict your requirements, we will pick some values out of a hat and analyze the results. First, the circuit will not even begin to conduct current until the tip-to-ring voltage reaches a certain level. This voltage can be easily calculated as VBRIDGE + VBE + VBE (R5 / R4). Using 1.4V for both the drop of the diode bridge and the VBE of the Darlington transistor and using 22 kΩ for both R4 and R5, the turn-on voltage is 4.2V. The increase in voltage with current is the circuit's dynamic resistance and is given by R3 + R3 •(R5 / R4) + R5 / ß. We should use as large a value for R3 as possible but still meet our goals. We will choose 22Ω and with a ß of 1000 the dynamic resistance of our circuit will be 66Ω. Note that these equations are first-order approximations and ignore the variation of V_{BE} and ß with current (and temperature!). Nevertheless, we can plot a graph of the tip-to-ring voltage against current that this circuit will give to see if it meets our needs. Figure 6–16 shows the graph for our circuit. Straight lines are shown for ß = 1000 and ß = ∞ and a curve is drawn to show the sort of characteristic that the circuit would have in practice, allowing for ß and VBE variations with current.

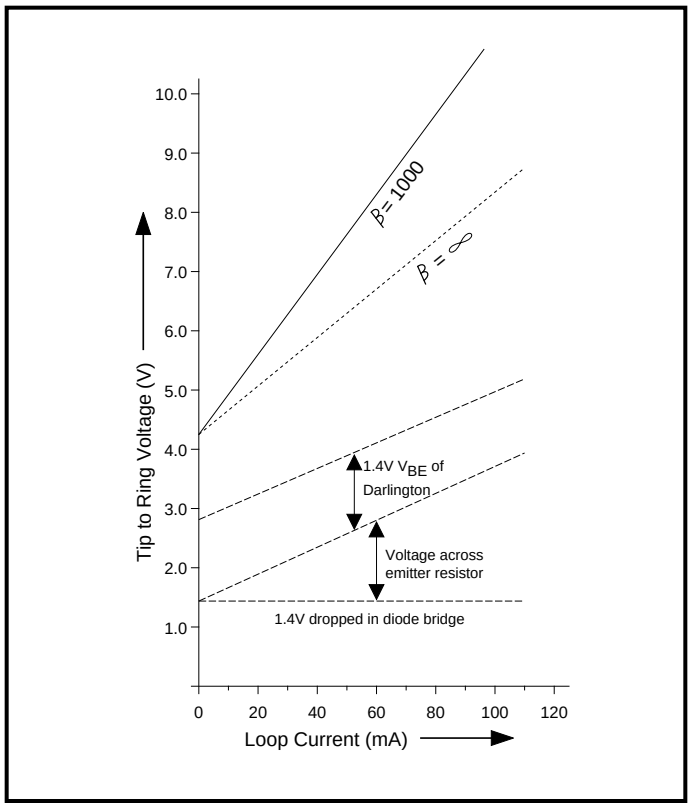


FIGURE 6 – 16: Voltage to Current Plot of Electronic Holding Coil

Now we have to predict the maximum signal levels with which our circuit can operate. The A.C. signal on the line, mainly the output of our modem transmitter, is superimposed on the D.C. level at the collector of Q2. If this signal causes the collector to emitter voltage of the transistor to fall too low, it will come out of its linear operating region and distortion of the signal will result. For a Darlington transistor, the collector should be at least 1.0V above the emitter. We can calculate that the maximum allowable peak voltage swing is 0.4V + i (R5 / ß) + VBE (R5 / R4) + i (R3) (R5 / R4), where i is the current flowing. Recognizing that ß could be very large and that the circuit could be expected to operate with no loop current flowing, this reduces to 0.4V + VBE • R5 / R4 which for our circuit is 1.8V. If you can guarantee some loop current, you can add in the i (R3) (R5 / R4) term. The peak amplitude of a DTMF signal at a level of 0 dBm into 600Ω is about 1.6V. Data signals at -9 dBm will be lower than this even though they can have a higher peak-to-RMS ratio. So our circuit is marginally suitable for general application in this respect.

A 10 µF capacitor for C3 gives a time constant of 0.11 seconds with R4 in parallel with R5. Unfortunately, this does not help us to find the lowest frequency at which the high A.C. impedance of the circuit is maintained. This calculation is more complex than it seems at first and requires SPICE analysis, which we have not done. You should perform some bench measurements to check this. The risetime of the loop current when the modem goes off-hook will be on the order of 100 ms. C2 couples the A.C. signal to the primary of the dry coupling transformer. Its impedance must be low compared to the 600Ω characteristic impedance of the signal down to the lowest signal frequencies; 10 µF is suitable here. A non-polarized capacitor must be used in the position shown for the same reason that we have a diode bridge. It is also possible to take the A.C. signal from the D.C. side of the bridge, in which case a polarized, electrolytic capacitor may be used. However, the signal will now be blocked and the modem will not work unless a D.C. current is applied, which prevents testing the system without a source of loop current.

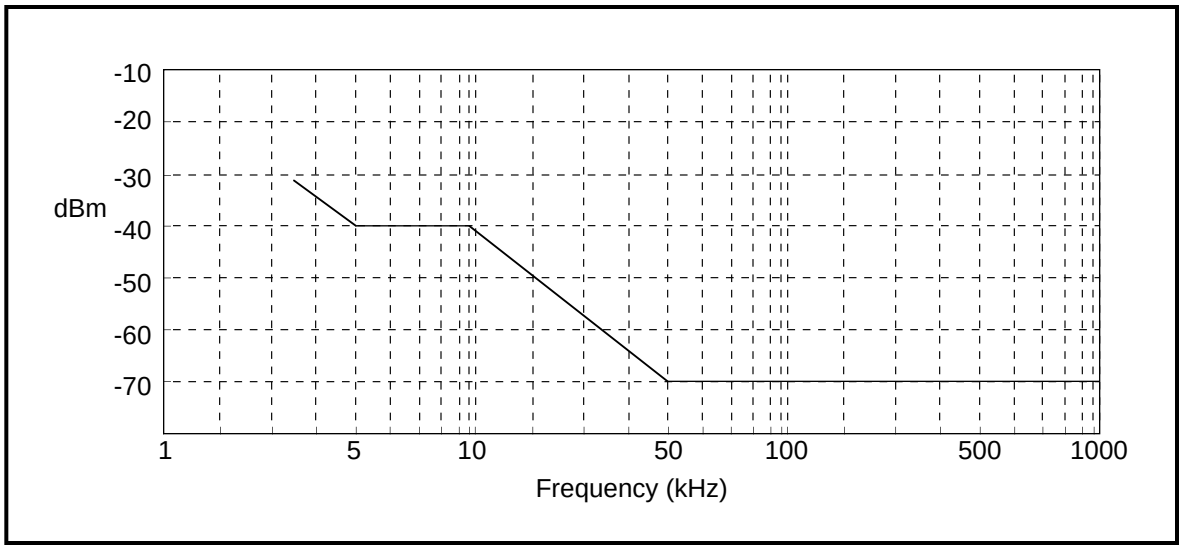


FIGURE 6 – 17: Out-of-Band Signal Power LImits for the United Kingdom

6.5.11.2. Reducing Out-of-Band Signal Levels

Many countries are more particular than the U.S.A. in respect to the level of signals above the normal audio band that are transmitted to the network. A particularly difficult specification to meet is that of the U.K. shown in Figure 6–17. This shows the maximum permissible power into a 600Ω load, measured in a 3 kHz bandwidth, up to 10 MHz. By 5 kHz the signal power must fall to -40 dBm, more than 20 dB below the level permitted in the U.S.A. From 5 kHz to 10 kHz the graph is flat, but then it plunges to -70 dBm at 50 kHz and stays there up to 1 MHz. Two measures are necessary to conform to this requirement. First, the transmitted signal must be buffered by a continuous time low-pass filter to reduce the level of switching signal breakthrough from the K-Series modem IC. Use at least a second order filter; this requires only the one op-amp already in circuit as a gain stage and buffer. Secondly, the circuit layout must be designed not only with a mind to EMI problems, but also to prevent signals below 1 MHz from coupling into the network connection. Such low frequencies rarely give EMI problems, but will easily cause failure of the signal power to line requirement.

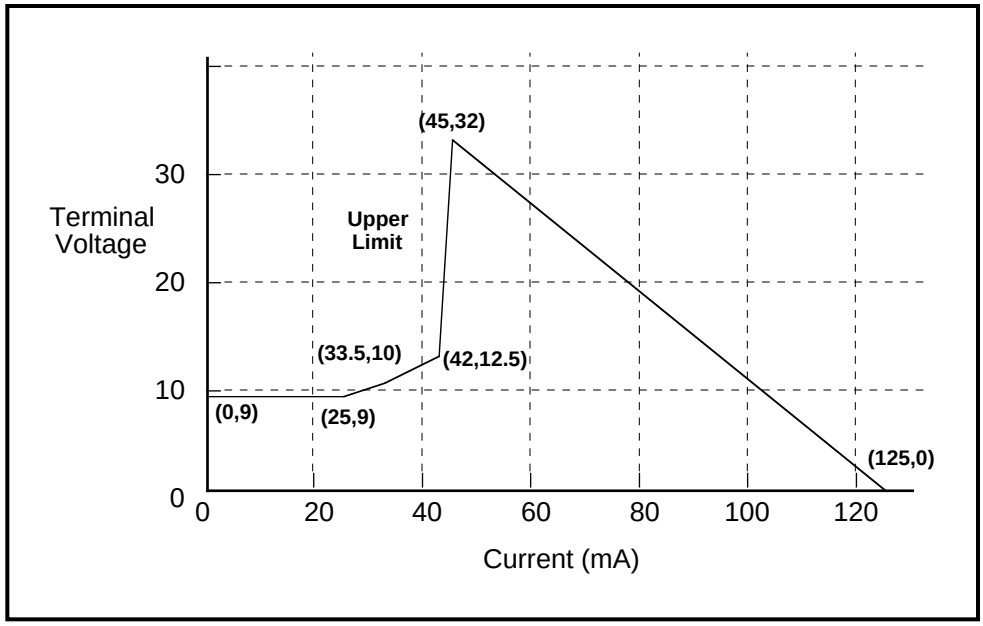


FIGURE 6 – 18: Off-Hook D.C. Characteristics, U.K.

6.5.11.3. Unusual Requirements for Off-Hook D.C. Characteristics

In the U.S.A., the FCC specifies the off-hook characteristics of equipment connected to the network in terms of the current waveform at the transition to the off-hook state. This is difficult to design for, so that most modems use the alternate test and draw more current from the line than a 200Ω resistor. Most other countries are more specific about their off-hook D.C. requirements and provide a graph of voltage against current with acceptable and unacceptable zones. For a change, the U.K. is extremely reasonable in their requirement, which is shown in Figure 6-20. The excluded region is an area in which there is no requirement to operate. The maximum battery voltage of 50V and minimum local loop resistance of 400Ω make conditions in this area impossible at the subscriber connection. The voltage / current curve of your equipment must pass through the allowable region and not enter the forbidden region. A resistor of 297Ω or below, including a short circuit, will meet this requirement. By allowing a voltage drop of up to 9V at low currents, the graph provides for electronic holding coils and line powered equipment. Also, by allowing the voltage to rise steeply for currents above 42 mA, the graph lets the designer incorporate current limiting devices to protect the equipment.

Unusual requirements in this area come this time from the French speaking countries. The off-hook D.C. characteristics required by Canada are shown in Figure 6-19. The most notable feature here is the forbidden region at the bottom of the graph. This means that there is a minimum off-hook resistance as well as a maximum. Resistors between 100Ω and 300Ω will work perfectly well, but a short circuit is not acceptable. Note also that many high quality line coupling transformers have primary D.C. resistances below 100Ω. Tests are not made at currents below 20 mA or above 130 mA or voltages above 56.5V. Electronic holding coils, line powered equipment and current limiting devices are all feasible in Canada. Because the minimum resistance drops to 50Ω at 30 mA and to zero at 50 mA, diodes may be used to increase the voltage drop for low resistance transformers.

The requirements of France are totally unique in that the French PTT imposes the responsibility of limiting the loop current on the subscribers equipment rather than the network.

The off-hook D.C. resistance required in Germany is unusual in that it is rather large. The resistance (as calculated by dividing voltage by current) for all expected operating currents (from about 17 to 43 mA) must be between 300 and 470Ω. Where the loop current is passed through the coupling transformer primary, this inevitably leads to extra resistors in series with the loop bypassed by large capacitors. An electronic holding coil can be designed to meet the requirement, but care is required.

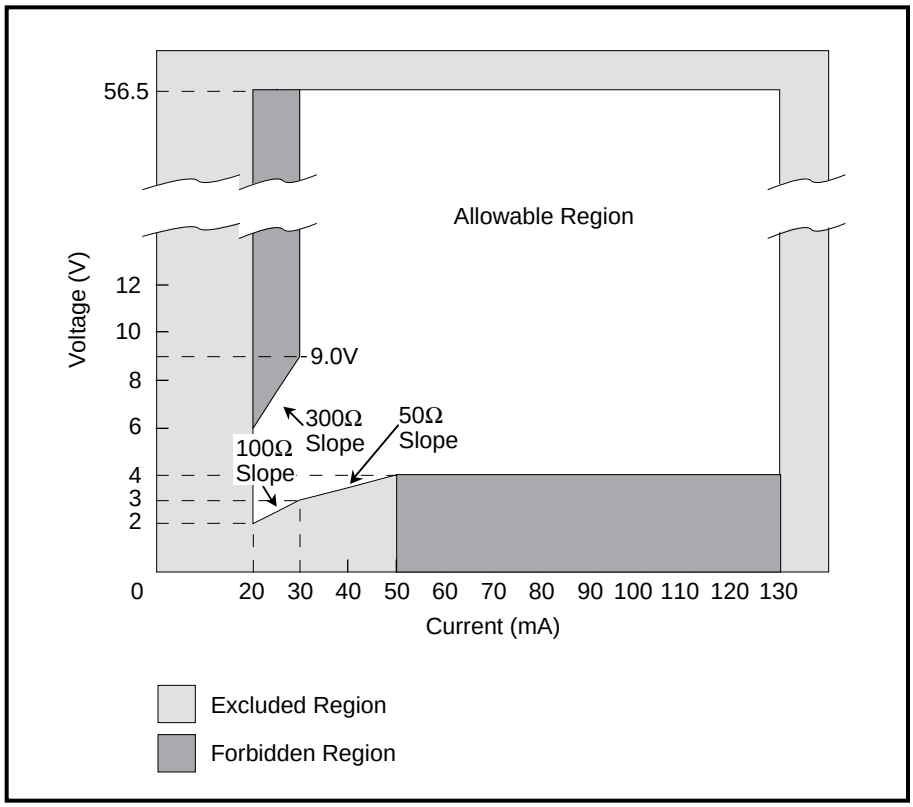


FIGURE 6 – 19: Off-Hook D.C. Characteristics, Canada

6.5.11.4. International Ring Detection Requirements

Many countries have very specific requirements for what range of signals should be detected as ringing and what signals should not. We can give no general guidelines as every requirement is different and even the setup used to perform the test is variable. Obtain the relevant documentation from the countries in which you are interested; a competent international telecommunications compliance consultant will be able to help you get English translations. If your product is capable of automatically going off-hook to answer incoming calls, it must be tested by an approved laboratory and meet the requirements before it can be sold for connection to the network. Usually, a range of frequencies and a minimum voltage is specified for a positive ring indication. For example, in Germany, signals of 50 VRMS and above at 23 to 54 Hz applied to the line terminals via a certain network must cause the unit to sense ringing. For frequencies below 18 Hz or above 60 Hz, the unit must not indicate ringing for

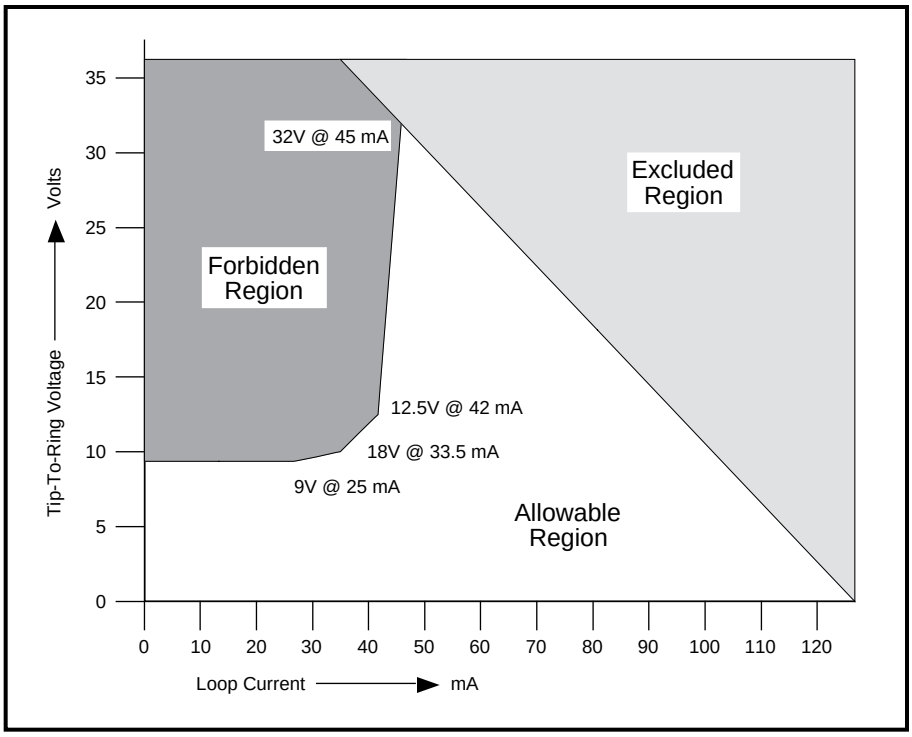


FIGURE 6 – 20: Off-Hook D.C. Characteristics, U.K.

voltages up to 75 VRMS. The frequency of the ringing signal can be measured by the controller firmware as described in section 7.3.1.2, Ring Signal Frequency. An additional test in Germany applies the same 50 VRMS via a modified network that reduces the level at the line terminals. For all frequencies, now, the unit must not indicate a valid ring. A limit to the sensitivity of the ring detection circuit must be established to meet this requirement. Back-to-back Zener diodes can be used as mentioned in section 6.5.3.3, Designing the Ring Detection Circuit. Just to complicate the issue, the German tests are performed with interference signals added at 6.5 VRMS from D.C. to 20 kHz with sine, square, triangular and rising and falling sawtooth waveforms. Some countries will also throw all kinds of transients at your product and look for false ring detects. You should therefore aim for some margin of safety in your design.

6.5.12. Miscellaneous Considerations in the Telephone Line Interface

This section contains items about connecting a modem to existing telephone lines and supplements the preceding headings.

6.5.12.1. Designing Line-Powered Equipment

The original intention of the public switched telephone network was that the central office would supply all energy required to operate the system. Even today, when most telephones incorporate electronic ringers and signal amplifiers, all power is obtained from the local loop battery. It is clearly attractive to design data communication equipment that can operate in the same way. Extreme caution is needed, however, to ensure that the equipment will work over the likely range of loop voltages and currents and that it will meet the requirements of FCC Part 68.

First, the amount of current that can be drawn from the line in the on-hook state is minuscule. Part 68 requires that the on-hook D.C. resistance be greater than 5 MΩ for applied voltages between 0 and 100V. To obtain a Ringer Equivalence Number of one, this must be increased to 25 MΩ. Thus, as the voltage approaches zero, the current also must vanish. However, in the field, your equipment will usually see a battery voltage of at least 40V so that you can rely on 8 µA being available for an REN of 5 or 1.6 µA for an REN of one. You must get at this current in such a way that as the voltage decreases, the current shuts down also so that the required D.C. resistance is measured down to zero volts. With a microamp or so you can keep a CMOS memory alive but not much else. Strangely, this is one area in which the requirements of the U.S.A. are more restrictive than elsewhere. In the United Kingdom, for example, you can draw up to 30 µA from the network at an REN of one for any voltage.

Assuming that your equipment can somehow get into the off-hook state without power, the situation improves slightly. Telephones, of course, get off-hook by someone lifting the handset and can then draw some power from the line. Thus you can only really consider line-power if you have some mechanical means of activating the hook switch. Now a current of milliamps is available as long as you can keep the tip to ring voltage low enough.

6.5.12.2. Providing a Jack for the Telephone Handset

When you buy a modem, you will often connect it to an existing telephone line which is presently used for normal voice calls. Having disconnected the phone and plugged in the modem instead, it will occur to you that it would be nice if the phone could be left connected so that you could use it for voice when the modem is not operating. A two-way telephone jack adapter from Sears will allow you to do this, but many modems have a phone jack on them for this purpose. The simplest way to provide this facility on your product is to wire the phone jack in parallel with the connection to the telephone line. Often, this connection is from a similar jack on the modem marked “line” or “telco.” It is important to realize that the standard cable supplied with telephones and modems to plug into the equipment at one end and the wall jack at the other is a twisted cable. By this, we mean that the pin numbers at one end do not

become connected to the like pin numbers at the other end, but they are all crossed over. For the normal six-way RJ11 cable, pin 1 becomes connected to pin 6, pin 2 to pin 5, 3 to 4 and so on. In order that your phone jack looks exactly the same (electrically) as the wall jack, we recommend that you twist the connections between the line and the phone jack on your product. For the tip and ring connections, wire pin 3 of the line jack to pin 4 of the 'phone jack and vice-versa. Most telephones are not sensitive to polarity, so don't do a redesign if you already have it the other way, but it's easy enough to do on new designs.

If you have chosen a hook relay that has changeover contacts, it is very worthwhile using them to disconnect the phone jack when the modem goes off-hook. Connect the pole of the relay to the line, the normally-closed contact to the phone and the normally-open contact to the DAA. It will now be impossible to disrupt a data call by picking up the telephone and bellowing, "This doesn't sound like a dial tone!" into the mouthpiece. Also, connect the ring detection circuitry to the phone side of the relay so that it gets switched out of circuit. It's not needed once the modem has gone off-hook and if it's not there it can't interfere with the signal.

6.5.12.3. A/A1 Switching Via an Auxiliary Relay

Hayes AT™ compatible modems give you the capability to operate an auxiliary relay via the AT&Jn command. The auxiliary relay shorts together pins 2 and 5 of the line jack. These pins are described in FCC Part 68 as "A" (pin 2) and "A1" (pin 5) of the USOC (Universal Service Ordering Code) RJ12 and RJ13 jacks. These pin numbers are with reference to the wall jack and will be reversed at the modem line jack when the normal twisted cable is used. This feature is used to permit proper operation of the "hold" functions of multi-line key telephone systems. The AT&J0 command causes the modem to assume that a normal RJ11 jack is in use and the auxiliary relay remains open at all times. The AT&J1 command allows the use of a RJ12 or RJ13 jack and the auxiliary relay operates along with the hook relay so as to acquire a line from the key system.

6.5.12.4. Using the $\overline{OH}$ Output and $\overline{RI}$ Input of the Integral UART Parts

In order to further reduce the system parts count, K-Series modem ICs with integral UARTs provide an output designed for controlling the hook relay and an input for the ring detect signal. The state of the $\overline{OH}$ output pin is controlled by the value written to bit 5 of the Modem Control Register 3. If this bit is ZERO, the open drain output floats and a relay connected from here to +5V will be open. If this bit is ONE, the open drain output pulls down to 0V and the relay will close. The maximum current that the $\overline{OH}$ output can safely sink is 20 mA and we admit that it is not easy to find a physically robust relay that will operate on this current. Where a larger current is required, an external current amplifier must be used. Note that the $\overline{OH}$ output is clamped to VDD by an internal diode in the high state and therefore can not be used to directly drive relays fed from voltages higher than the 5V chip supply. The logic state at the $\overline{RI}$ input can be read from bit 6 of the Modem Status Register in the UART register bank in the single port mode (STNDLN=1). If the $\overline{RI}$ input is below 0.8V then a ONE will be read and if it is above 2.0V a ZERO will be read. Thus the sense of the signal is inverted. Note that a Darlington opto–isolator such as the TIL119 cannot reliably pull $\overline{RI}$ to a low logic level and should not be used in the ring detection circuit of Figure 6-9. Bit 2 of the Modem Status Register is set to ONE whenever the $\overline{RI}$ input changes state. If it is not used for ring detection, this input can be used for something else. For details, refer to Silicon Systems Communication Products Data Book.

6.6. DESIGN FOR COMPLIANCE WITH FCC REGULATIONS PART 15

The FCC is empowered to regulate the sale and use of what it terms "Computing Devices" for use in commercial or domestic situations based on their potential for interfering with the legitimate use of the electromagnetic spectrum. Computing devices are defined by the FCC as any equipment that generates and uses a timing signal of above 10 kHz and uses digital techniques. Thus, if you're using a K-Series modem IC, you need to comply with FCC Regulations Part 15. Two classes of computing device are defined. Products marketed for use in commercial, industrial or business applications are Class A and those for use by the general public in the home are Class B. The Class B requirements are more stringent than Class A, however if it is conceivable that your product could fall into domestic use it is advisable to seek Class B approval.

The emission of EMI (electromagnetic interference) should be controlled by good practices in both the electrical design of the system and the mechanical design of the circuit board. Electrical design rules can sometimes be contrary to performance factors required of the system and the mechanical requirements can lead to increased cost so that a careful compromise is often necessary to obtain the best design.

6.6.1. Electrical Design for Low EMI

In designing an electrical system to avoid EMI problems it is only necessary to minimize the generation of periodic, fast, high current switching events. This leads us to a total preoccupation with systems clocks as most other signals in the system will not be as fast or as periodic. Other signals such as busses and random logic circuits will generate high–frequency energy if they are switching rapidly, but the non-periodic nature of the signals spreads the energy in the spectrum. Failure of FCC tests is almost always caused by discrete lines in the emissions spectrum which are above the permitted levels. Having said this, it is advisable to keep an eye open for any signals which might stay periodic at high-frequency for some period of time and switch some

current rapidly. An example of such a signal would be a strobe to a memory or a low order address bit to a sequentially addressed memory where the bus capacitance is large. In these cases, the same considerations should be applied as for system clocks.

If possible, use only one system clock. Two or more asynchronous clocks can beat together and give rise to frequencies higher than either clock's fundamental. If more than one clock must be used, try to keep them in separate parts of the circuit, perhaps using separated ground networks, so that they do not mix together. Never pass asynchronous system clocks through the same chip to buffer them.

Don't supply more drive capability to the system clock line than is absolutely necessary and avoid rise and fall times that are faster than you need. In this respect, using the on-chip oscillator of a microprocessor or the K-Series modem chip is much better than using a separate oscillator. Canned oscillator circuits attempt to supply the maximum drive and fastest slew rates to appeal to more applications and will increase your EMI problems.

Avoid situations where the power supply current changes between the high and low states of the clock. An example of this situation is the use of a pullup resistor to get a CMOS logic high level from a TTL output. A high current through the resistor is switched at the clock rate and can cause significant EMI. The same effect using less current and causing little EMI can be obtained with an active constant current source as the pullup.

Choose a logic family that has good EMI properties, if you have that freedom. TTL has a very fast fall-time and causes short current pulses in ground connections when a logic level goes to zero. Obviously, the faster Schottky families are more of a problem in this respect than LSTTL. NMOS is better because MOS transistors are not as able as bipolar to pass high currents when the output level approaches the supply rail so that the waveform rounds off at the end of the transition. CMOS shares this advantage, the symmetric P- and N-channel switches at the gate output give well controlled slew rates and no change in static current draw from logic one to logic zero. However, recent developments in higher speed CMOS such as the 74HC and especially the 74AC families have negated this advantage by allowing both output devices to be on simultaneously during the logic transition. This short circuits the power supply briefly and causes very large current spikes through the logic gate. If it seems impossible to go fast without EMI problems, take heart, because emitter-coupled logic (ECL) is not a great source of EMI. Signals are carried differentially internally so that a transition is generally balanced by an opposite transition. During switching, current is transferred from one transistor to another, rather than turned on or off, so that current draw is substantially constant. However, as you probably know, ECL is a great source of heat.

As a final caution, there are many reasons to be careful about bus contention; current draw, component reliability, etc. If these don't make you double check your bus timing, then EMI should. If two circuits try simultaneously to drive the same bus, even for a brief instant, current pulses will result which will cause strong broadband radio frequency emissions.

6.6.2. Mechanical Design for Low EMI

Having done as good a job as we can at avoiding fast current changes in our circuit design we have to remember something when designing the circuit board; don't build antennas.

The usual antenna structure that arises spuriously in a circuit board layout is the loop antenna. If a trace carrying a fast periodic signal is not close to a power or ground trace, then the return current will be forced to flow at some distance from the signal. The tendency of the signal to radiate will be proportional to the area enclosed by the signal trace and the return path. To minimize this, dangerous signals should be routed as directly as possible to their destination and a ground trace placed very close by.

An alternative to pairing ground traces with signals is to adopt a distributed grounding approach. In its most understandable form, this is a continuous ground plane on a separate layer of the circuit board. Here, the return currents for each signal will automatically tend to flow under the signal trace, thus minimizing loop area. If a dedicated layer is not available, an approximation can be constructed using a grid of heavy horizontal and vertical traces connected at all intersections. Return currents will tend to distribute themselves over the grid, forming smaller antennas which radiate in opposition.

Another antenna structure which occurs is a connecting cable acting as a simple wire antenna. Common mode high–frequency signals present on signal and ground leads within the cable cause the whole structure to radiate. These signals are often caused by ground return currents flowing back to the system power supply causing voltages across the ground circuit inductance. Ground planes or grids can help to reduce this problem by lowering the impedance of the ground connection.

6.6.3. Suppression of EMI

Prevention is almost always cheaper than cure when it comes to EMI in a mass produced electronic system. However, sometimes circumstances will arise when the product generates more EMI than is acceptable by FCC tests. It is then necessary to use screening and filtering to block the emitted interference.

Screening is simple to achieve if your product is to be made in a metal enclosure. The conductive case acts as a Faraday shield and blocks the passage of high-frequency EMI. The same effect is obtained with a plastic enclosure by coating the inside with a conductive layer. The resistivity of this layer must be low, of the order of a few ohms-per-square or less. Be warned, however, that conductive coatings are scrutinized by safety organizations. Make sure that the

coating, base material, method of application and the total combination are approved by UL or another appropriate safety body. Ideally, the screen should be complete around the equipment and all its cables. It is normal to require openings here and there for switches and displays to protrude. If these are kept less than a few inches in their longest dimension, no problem should result. Even the narrowest slot, however, can act as an antenna, so pay attention to electrical contact at frequent intervals around different parts of the case if it is used as a shield. Finally, no currents should flow in the shield which contain high–frequency components as they will radiate as well from the shield as from a wire. It is best to connect all metallic hardware together and, if desired, connect it to circuit ground at one point only.

Filtering is used to reduce the level of EMI getting out of the equipment enclosure on cables. This EMI can directly cause failure of Part 15 conducted emissions tests, or by using the cables as antennas, can add to radiated interference levels. Filtering can be achieved by blocking high-frequency signals or shunting them to a "free space" ground.

High-frequency signals can be blocked before they get onto cables by placing inductors in series at the cable exit point. The form of inductor most commonly used is the ferrite bead because it has low parasitic capacitance and therefore is effective to quite high frequencies. A bead should be wired in series with each lead that exits the equipment, signal leads and ground or return leads. Choose beads with an effective impedance of about 500Ω over the frequency range of interest. As a long connecting wire has an impedance to free space of about 50Ω, the bead will attenuate both conducted and radiated interference by about 20 dB.

Capacitors can be used to bypass high-frequency signals to earth. Circuit ground is often mistakenly used to decouple EMI signals, but the truth is that at high-frequency it can be as dirty as the signal you're trying to clean up. What is needed is a connection to "free space" since it is a potential difference to free space that causes an antenna to radiate. The closest we can practically come to this is a substantial conductive body in which no currents are flowing. A metal or coated case, front or rear panels or an isolated metal shield can all be used as a free space ground so long as they are not used elsewhere to carry currents with high-frequency components. The decoupling capacitors must be connected to this ground by circuit traces, straps or clips which are no longer than about four times their width. Otherwise the effectiveness of the connection can be reduced at high–frequency by its self-inductance.

Whichever method of filtering is chosen, the connection of the capacitor or bead must be as physically close to the exit point of the cable as possible. Any length of wire after the decoupling point that is close to a source of EMI is liable to pick up more high-frequency signals. At this point it is worth saying again that the best approach is to avoid the generation of high-frequency radiations by good circuit and layout design. If all system clocks are generated from the 11.0592 MHz clock of the K-Series modem using the on–chip oscillator, then a good layout will pass FCC Class B tests without further precautions.

6.6.4. Suppression at the Telephone Cables

We have considered above some alternatives for reducing the levels of EMI. However, because of the special concerns we have about isolation in the telephone line interface, we will look more closely at this area.

If it is suspected that extra precautions will be needed to block the passage of high-frequency signals out onto the network wires, the same two methods of filtering mentioned above are possible. Decoupling each wire with a small value capacitor, about 470 pF, has proven successful and is often easiest if the emissions problem is discovered at a late stage in the design. However, the capacitors must cross over from the network side of the DAA to the equipment side, crossing the barrier described in section 6.5.3.5. Therefore, they must be able to withstand the 1000V A.C. applied during the hazardous voltage and current tests. Also, having reached the equipment side, remember that the capacitors must connect to a solid "free space" earth potential.

A more elegant solution to EMI radiation through the telephone line cables is to use series ferrite beads. This, however, requires that space on the circuit board be more carefully allocated if you are trying to do without them and find that you need them after the FCC tests. Ferrite beads require no free space reference and stay entirely on the network side of the barrier.

6.7. PRINTED CIRCUIT BOARD LAYOUT CONSIDERATIONS

An aspect of electronic system design which often receives far less attention than it warrants is the layout of the printed circuit board and the pattern of interconnects. In systems including a modem function, five factors should be considered during PC design.

1. Careful consideration of grounding and the routing of high-frequency clocks is needed to control EMI. This has been covered in section 6.6.2, Mechanical Design for Low EMI, so the reader should refer back to this section.

2. As with all electronic systems, the power supplies must be kept reasonably free of A.C. signals by appropriate decoupling. You may be surprised to see this subject under the heading of PCB layout considerations, but the placement of decoupling capacitors is at least as important as their number and position in the circuit. We will suggest an approach to decoupling of the K-Series modem IC in section 6.7.1 and assume that you will follow good engineering practices elsewhere in your system.

3. The separation of digital and analog circuit areas is important to prevent coupling of unwanted signals. Any digital signals coupling into the sensitive analog receive

circuits will degrade the modem's performance at low receive signal levels. This aspect of PC design is discussed here in sections 6.7.1 and 6.7.2. Nothing new is offered here over and above generally accepted good engineering practices, but it is felt that a discussion specific to systems using the Silicon Systems K-Series products may focus attention on this important area at an early stage in the design.

4. It is important to achieve effective isolation of the system electronics from the telephone network connections.

5. In order to obtain the approvals needed for sale in many countries, the system must be inspected for conformance to safety standards. This involves the measurement of "creepage" and "clearance" distances between conductive elements on the circuit board and components where the isolation of dangerous voltages is required. The primary areas of concern are the power supply and the telephone line interface. We do not discuss power supply design here as it is in no way unique to systems including modem functions.

6.7.1. Designing to Avoid Coupling of Circuit Noise

Any electronic system should be designed so that signals generated in one part do not unintentionally couple into another part and thus compromise system reliability or performance. In this and the next section we discuss printed circuit board design practices which will result in reduced coupling of undesired signals from place to place within the system. Almost all of the guidelines given in section 6.6.1 to reduce EMI will also help in reducing the levels of signals generated by the digital part of the system and coupled into the analog part. The additional rules presented here are concerned with separation of analog and digital circuits and the distribution of power and ground lines. Here we are also concerned with signals of all frequencies, since resistive coupling takes place at low frequencies as well as high.

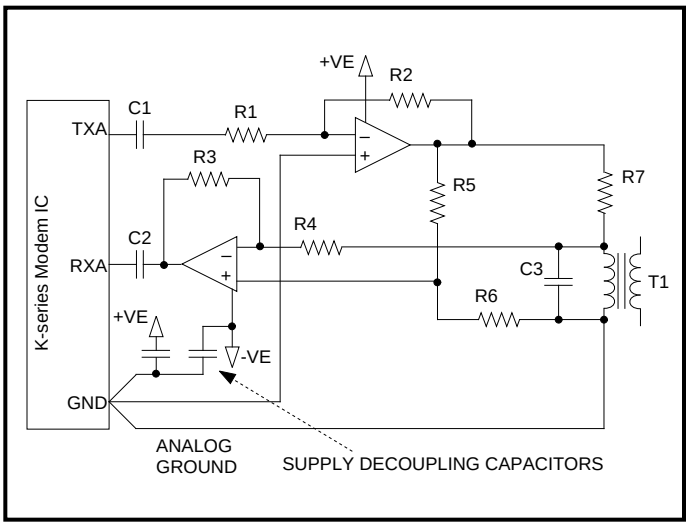


FIGURE 6 – 21: Good Grounding Practice in the Electronic Hybrid Circuit

The supplies to the sensitive analog components in the system must be kept separate from supplies to digital or high-current analog components. It is preferable for the K-Series modem IC and the operational amplifiers in the line interface hybrid not to share a supply with any digital circuitry or a relay or speaker driver circuit. They may, if convenient, share the same supply with each other. These supplies should be carefully decoupled with both a high-value tantalum electrolytic capacitor of value about 22 µF and a low inductance solid dielectric capacitor (such as ceramic) of value 0.1 µF. The positive supply, which powers the K-Series part, must be decoupled directly at the VDD pin of the package. The ground side of the capacitors must connect solidly to the GND pin and not use any part of the digital ground network.

Low-power and integral UART ("L," "U" and "SL" suffix) K-Series parts can be powered from a +5V logic supply if properly decoupled as above. If you are using a fast logic family you may consider putting a ferrite bead in series with the connection to VDD to block high-frequency noise created by the digital circuits. We no longer recommend the use of a 10Ω resistor in this position. The 22 µF and 0.1 µF capacitors must be connected as above directly at the VDD pin. Using the logic supply is particularly attractive when the rest of the analog circuitry is powered from a higher voltage and no "clean" +5V supply is available.

The speaker ground and amplifier power connections are quite capable of influencing the performance of the modem since they typically involve amplifying the receiver input by 20 to 40 db and dumping that current into the ground system at the speaker. The effect is particularly severe because the signals are, by definition, all in the modem bandpass and generally contain the transmitter signal which you are trying to elimate from the receiver input. In addition, the speaker is normally on during the handshake, a time when the modem knows the least about the amplitude and phase of the incoming signal.

Keeping the speaker wiring away from the DAA and the hybrid, giving the amplifier isolated power and grounding the speaker at the common point of the digital and analog ground systems would be appropriate. If the amplifier has a differential input, the low side could be connected to the ground pin of the modem to reduce spurious pickup.

The design of the circuit board grounding system is often a compromise between getting a low impedance path and isolating circuit areas which must not interfere. For small circuit boards, "flooding" as much otherwise unused board space with ground trace has proven successful. This approach minimizes connect impedance in the ground paths. However, depending on the relative placement of circuit functions, it is possible to have the return paths of high current or fast switching signals crossing sensitive areas on their way back to the source.

A more rigorous approach is to isolate the ground circuits of sensitive circuit areas from components which

generate disturbances on the ground and power lines. In a typical system using a K-Series modem IC, this will mean isolating the ground of the analog hybrid circuit from the rest of the electronics, which will be predominantly digital. Each ground circuit should be as low-impedance as possible, but they should connect at one well chosen point only. Note: Because the K-Series products use only one pin for both analog and digital ground, this GND pin absolutely must be the common point. This is most important; ignore this at your peril!

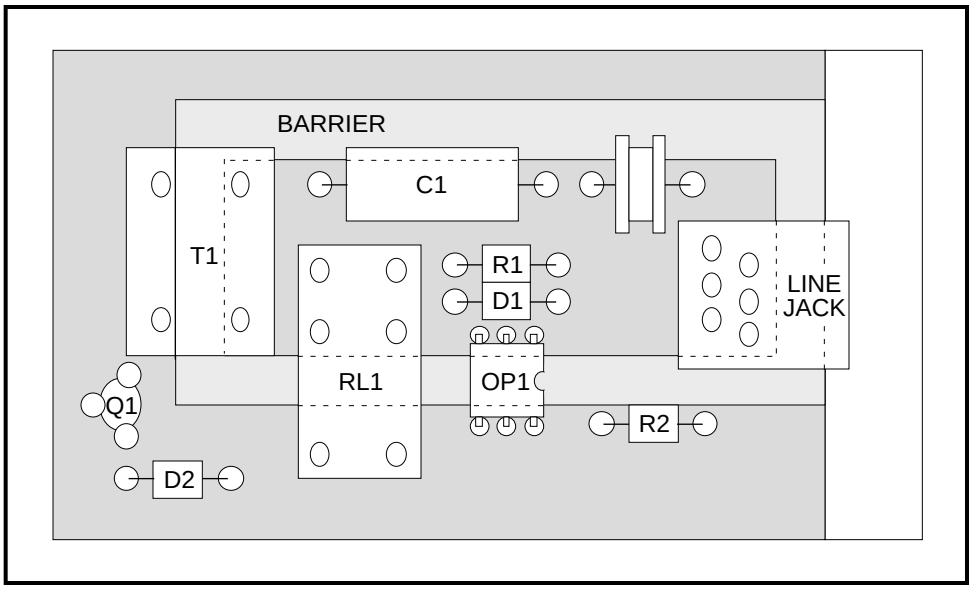


FIGURE 6 – 22: Layout of Simple DAA Circuit Showing Barrier

The power supply ground connection should be made into the digital ground system. The usual techniques of distributing power and ground in this area should be used to ensure low levels of logic switching noise. Four-layer printed circuit board construction is the best and easiest to design but costs significantly more than double sided. On double-sided boards, the digital power and ground traces should be gridded. Decoupling capacitors of low self-inductance should be used for every two or three ICs, more for faster logic families, fewer for four-layer boards. These precautions will ensure that the digital circuitry will operate reliably as it has an inherent immunity to disturbances on ground and power as long as they are kept to a low level.

6.7.2. Ground Connections at the K-Series Modem IC

In contrast to digital circuitry, analog circuits offer no immunity to disturbances on the ground (unless differential signals are used). Therefore the ground should be treated similarly to other signal paths. Figure 6-21 shows the circuit redrawn to stress good grounding practices. The analog signals TXA and RXA of the K-Series modem IC are referenced to the ground pin GND. The signal ground of the transmit buffer amplifier therefore goes directly to this pin, no other signal currents share this wire so that no unwanted potential differences can arise. The ground connection of the transformer T1 is made separately to the GND pin so that the relatively large drive signal current can flow directly back to the power supply through the digital ground path. The ground reference for the receive buffer amplifier is the grounded end of the transformer secondary so R6 is connected at this point.

The positive and negative analog supplies must be decoupled to maintain a low A.C. impedance but note that the capacitors perform this task by shunting the unwanted signals to ground. These currents will give rise to voltage drops in whatever trace they use. Unless this ground connection is made separately to the GND pin as in Figure 6-21 , the voltage will disturb other signals. Because the approach described implies handcrafting the printed circuit board layout, many designers will resort to connecting all the analog ground points with wide traces but in an arbitrary topography. Because of the simplicity of the circuit, this is unlikely to cause problems so long as the analog ground network connects to the digital ground only at the K-Series GND pin. The one thing we are trying to avoid at all costs is any digital signal return currents flowing in the analog ground network. This cannot happen if the grounds join at only one point as described.

We suggest placing a solid patch of ground plane underneath the K-Series modem IC package on the component side of the PCB. This should be a part of the analog ground system and can be used as an attachment point for the positive supply decoupling capacitors at the VDD pin and the ISET and VREF decoupling capacitors. Note that the pinout of the K-Series products makes it easy to run the fast digital signals away from the chip on the side of pins 1 to 14. The digital signals on the other side are slower and can run under the package on the solder side.

6.7.3. Layout Considerations in the Telephone Line Interface

The concept of a barrier between the "network" and the "equipment" was introduced in section 6.5.3.5, Using Protection Devices and an Isolating Barrier. The barrier protects your equipment from high voltage common mode surges on the network, including the FCC Part 68 environmental tests, and ensures that the hazardous voltage and current tests are passed. Surges will arise from electrical storms and damage to line plant, which often runs close to power lines. The telephone company attempts to protect your equipment with spark gaps at the point where the line enters customer's premises. However, considerable residual surges can reach your unit and your customer will probably hold you responsible if your product stops working

whatever the cause. As discussed in section 6.5.3.6, it is possible to add your own protection devices to intercept common mode surges if you have a solid safety ground connection available in your system. This is often not the case and whether it is or not, we recommend the careful layout of the DAA on the "barrier" principle.

Many countries actually require this barrier in order to approve the unit for use on the public telephone network. Most of Europe and Australia specify a barrier width of 6 mm between the network side and the equipment side. The barrier must be clearly evident and actually marked on the PCB silk-screen in certain instances. No conductive parts can enter the barrier except components which cross the barrier. These must be specifically recognized by the local safety agencies as suitable for this application. The most stringent specification that we know of for devices crossing the barrier is dielectric isolation between the network and equipment sides of 3750 VAC for one minute, which is required for Australia. However, check not only that the device can withstand this voltage but that it is recognized by the appropriate safety agencies. Although the U.S.A. does not require a barrier and for UL approval an isolation of only 1000 VAC is needed, we recommend the use of a barrier to reduce the number of field failures of your product due to high voltage surges on the telephone lines.

To design a DAA layout with a barrier, first identify all the components on the network side and those that cross the barrier. On the network side will be the line and phone jacks, current limiting resistors, most of the ring detect circuit, surge protection devices, etc. Crossing the barrier will be the line coupling transformer, the hook relay and the ring detect opto-isolator. The electronic hybrid, the K-Series modem IC and the rest of the system are on the equipment side. Now group all the network side components around the line jacks or terminals. Then place the barrier crossing components around this group with their network side terminals facing inwards. Now mark the barrier as a pair of lines traveling under the barrier crossing components. When the lines turn corners or zig-zag, keep them far apart throughout the turn, the width of the barrier is the closest approach of these two lines. There should be no copper traces on the printed circuit board between these lines. Not only should traces not cross the barrier, but traces should not enter it on their way somewhere else. Remove all ground planes, including inner layers, from the network side and within the barrier zone. Once you have seen how the barrier concept applies to your DAA circuit, you will be able to move components around to get a compact layout with the barrier width you want without wasting a large amount of space. Figure 6-22 shows a layout of the DAA circuit given in Figure 6-7. Note that where the barrier is a national requirement, it must exist between the network components and all other metal parts that can be contacted from the outside of the equipment. This includes metal front and rear panels and mounting hardware.

Inside the barrier, the interconnection of the network interface components should present no great challenges. Use heavier than normal traces where the loop current flows, fine traces can too easily become fused when a current surge comes along. Don't use minimum copper spacing if you can avoid it. Run tip and ring traces parallel where possible to reduce the area of the loop between them which may pick up high-frequency signals from elsewhere in the equipment. Outside the barrier, use the usual good layout practices. However, remember to keep analog and digital separate by referencing the hybrid to analog ground and the hook relay and ring detect circuit to digital ground.

Section 7.0

CONTROLLER FIRMWARE DESIGN FOR K-SERIES MODEMS

7.0. CONTROLLER FIRMWARE DESIGN FOR K-SERIES MODEMS

In order to function as a modem, an Silicon Systems K-Series IC must be combined with a microprocessor or microcontroller of some sort. The K-Series part provides the capability to send and receive the signals needed to perform data communication over the telephone network, but the microcontroller decides how these signals will be used. This division of tasks allows you to design your system to your own requirements. Also, it means that we can concentrate on providing a high-performance data communication path without trying to second guess all the ways in which our product will be used.

In most cases you will want to use the K-Series modem in a way that we have already considered. Each member of the K-Series family has been designed to support a number of modem standards and to some degree we expect that you will want your system to conform to at least one of these. Therefore, in this section of the Design Manual, we will provide you with guidance on the control of a K-Series modem IC in what we consider a normal manner. We will try to show you why we suggest doing things a certain way so that if you wish to do things differently you will be aware of the tradeoffs involved.

We don't expect you to become an expert in the switched telephone network and / or data communications in order to use our modem chips. Thus we will additionally be dealing with matters not directly related to the control of the K-Series modem IC, but relating more to control of the telephone network. The same microcontroller that is connected to the modem IC will normally control the connection to the telephone network. Figure 7-1 illustrates the basic states that the controller will have to manage in addition to your particular application. We won't be going into detail about the interface to the application, this may be as complex as a serial command interpreter or as simple as a few flags in memory. Most of the following discussion focuses on the resources needed for the establishment and maintenance of the data connection. This will include the system timebase, status polling, timers and the sequence of operations needed to connect with another modem.

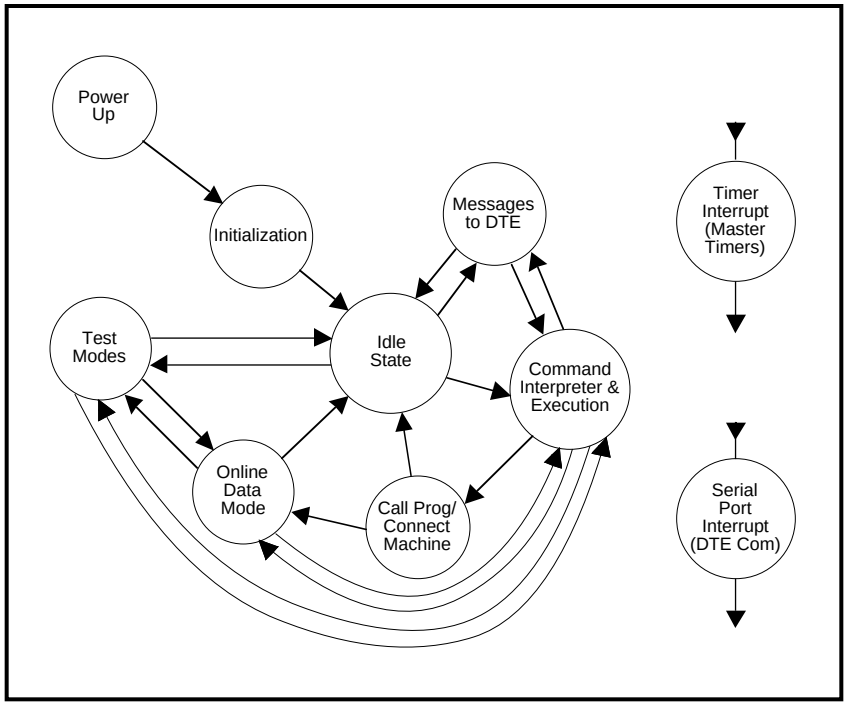


FIGURE 7 – 1: Basic States of a Modem Controller

7.1. GENERAL FIRMWARE DESIGN TIPS

In this section, before going through the firmware design function by function, we introduce some general points that you should know about before starting the design. In many cases, we will later refer back to techniques we have developed in this section to avoid repeating a concept everywhere it is used.

7.1.1. K-Series Registers and Designing for Interchangeability

In the introductory sections, we have pointed out that the K-Series modem family has been designed with pin and register compatibility in mind. This means that a product designed to use, say, the 73K212L could be made compatible with many international requirements by using the 73K222L and making small changes to the firmware. The data rate could also be increased by using the 73K224L, although more changes to the firmware would be needed and the external analog circuitry would have to be checked for suitability. If you plan to use this feature by upgrading or cost reducing at a later date, this section should help you design your firmware with this in mind. Also, if you already have products using K-Series modem ICs, you should find here an explanation of the small differences that you will have to accommodate in your code changes.

Figure 7-2 shows the register structure used in all K-Series modem products. A full description of the function of each bit in each register can be found in the device data sheets and would be out of place here. However, we will review the registers in turn and point out differences between family members. All writeable registers can be read back at the same address and will reflect the bit pattern previously written into it. Registers with unused bits will return ZERO in these places and should also be written with ZERO.

Control Register 0 (CR0) is written at address 0 and selects some basic operating modes of the IC. In all versions, bits 2 to 5 select power down (all ZERO) or the modulation mode, data transfer format and timing. When FSK modulation is selected in a part that supports two FSK standards, bit 7

chooses between them. A ONE here selects V.21, if available, and ZERO selects whichever of Bell 103 or V.23 is implemented in that chip. When DPSK is selected and both 1200 and 600 bit/s are supported (V.22 but not Bell 212), bit 7 again makes the choice. ONE here selects 600 bit/s operation. For DSP-based chips with 2400 bit/s capability, bit 6 is used to select the higher rate. It should be ONE for 2400 bit/s and ZERO for 1200 or 600 bit/s. Note that for chips that do not use bit 6 and/or bit 7, you should write ZERO here and the results will correspond to writing ZERO in a chip that does use the bit. You must know in advance, however, whether the chip supports Bell 103 or V.23 as you can't read this information from the chip. Bits 1 and 0 have identical functions in all family members, however, note that bit 0 also controls the forward and reverse channel assignments for V.23. A ONE here (normally call mode) selects transmission in the forward channel at 1200 bit/s and reception in the reverse channel at 75 bit/s. A ZERO (normally answer mode) selects the opposite. Mapping call and answer in this way is the other way around from normal usage, so watch out for this.

Control Register 1 (CR1) is written at address 1 and selects the transmitted data pattern and certain other features. This register operates identically in all K-Series modem ICs with one very small exception. Bit 4 is the Bypass Scrambler bit and has a second usage in those chips that support V.23. The scrambler is never used in FSK modulation modes, so when V.23 is selected at CR0, bit 4 in CR1 selects additional phase equalization at the receiver to improve performance over marginal lines.

The Detect Register (DR) is a read only register accessed at address 2 and allows the controller to obtain the status of certain detect functions in the chip. Most bits operate identically in all family members, however, the use of a few bits changes in those parts with V.22bis and/or V.23 capability. In the DSP-based parts that support V.22bis, bits 6 and 7 are used whereas in other devices they are invalid. Bit 6 is used to indicate the receipt of the S1 signal. Bit 7 allows the receive level to be estimated with a view to controlling the receiver analog gain. Bit 4 performs the same basic function, but the response time and the required treatment of this bit is quite different in DSP-based and non–DSP parts. In addition, the use of bit 0 differs slightly. In non-DSP parts this is the Long Loop bit and is ONE if the receive signal level is low, indicating the possibility of a high error rate. With a DSP, it is possible to make a much more accurate estimation of the likelihood of errors and this bit is redefined as Signal Quality. Do not confuse the Long Loop and Receive Level bits. They are never present in the same device, show up in different places, respond to signals at different thresholds and respond to high and low levels in the opposite sense. K-Series parts that have V.23 and V.25 calling tone capability make additional use of bit 2 in the Detect Register and it is therefore named Special Tone Detect instead of just Answer Tone Detect. Bit 0 in CR0 and bit 0 in the Tone Register both affect the precise use of this bit, refer to the data sheet for details. Bit 0 of the Tone register normally chooses Bell (2225 Hz) or CCITT (2100 Hz) answer tone detection, in parts without the choice the use of the Answer Tone bit is not affected by this bit.

The Tone Register (TR) is written at address 3 and controls the signal transmitted and certain other functions. Although the use of this register is fairly consistent across the family, it is complicated somewhat by having

	ADDRESS	DATA BIT NUMBER							
REGISTER	AD - A0	D7	D6	D5	D4	D3	D2	D1	D0
CONTROL REGISTER 0 CR0	000	MODULATION OPTION	MODULATION TYPE 1	MODULATION TYPE 0	TRANSMIT MODE 2	TRANSMIT MODE 1	TRANSMIT MODE 0	TRANSMIT ENABLE	ANSWER/ ORIGINATE
CONTROL REGISTER 1 CR1	001	TRANSMIT PATTERN 1	TRANSMIT PATTERN 0	ENABLE DETECT INTERRUPT	BYPASS SCRAMBLER	CLK CONTROL	RESET	TEST MODE 1	TEST MODE 0
DETECT REGISTER DR	010	RECEIVE LEVEL	PATTERN S1 DET	RECEIVE DATA	UNSCR. MARK DETECT	CARRIER DETECT	ANSWER TONE DETECT	CALL PROGRESS DETECT	SIGNAL QUALITY
TONE CONTROL REGISTER TR	011	RXD OUTPUT CONTROL	TRANSMIT GUARD TONE	TRANSMIT ANSWER TONE	TRANSMIT DTMF	DTMF3	DTMF2	DTMF1/ OVERSPEED	DTMF0/ GUARD/ ANSWER
CONTROL REGISTER 2 CR2	100	0	0	CALL INITIALIZE	TRANSMIT S1	16 WAY	RESET DSP	TRAIN INHIBIT	EQUALIZER ENABLE
CONTROL REGISTER 3 CR3	101	0	0	0	RECEIVE GAIN BOOST	TRANSMIT ATTEN. 3	TRANSMIT ATTEN. 2	TRANSMIT ATTEN. 1	TRANSMIT ATTEN. 0
ID REGISTER ID	110	ID	ID	ID	ID	USER DEFINABLE PERSONALITY			

FIGURE 7 – 2: K-Series Family Register Structure

multipurpose bits which have more than one function. Bit 6 is not used in parts without CCITT V.22 capability, in parts that have this, it enables guard tone transmission. If V.23 is also supported, guard tone is only transmitted in V.22 or V.22bis answer mode. In other modes, this bit enables the transmission of 1300 Hz calling tone. Bits 0 and 1 are the multipurpose bits. When bit 4 is set to enable DTMF tone transmission, these bits, along with bits 2 and 3, define the transmitted tone pair. Note that setting bit 4 causes DTMF to override transmission of guard tones, answer tones or the data signal as otherwise selected. In early data K-Series sheets, this comment was mistakenly associated with bits 0 to 3. When bit 4 is ZERO, bit 0 selects the guard tone and answer tone frequencies and certain other tone detection functions. Read the data sheet carefully for details. Bit 1 is more easily explained. When bit 4 is ZERO, this bit controls the overspeed capability of the data format converter for character asynchronous operation in DSPK and QAM modes. If bit 1 is ZERO, the normal overspeed range of 1% is selected. If it is ONE, then the extended overspeed range of 2.3% is selected. Not all K-Series devices have the extended overspeed capability, so check the data sheet for the specific part used.

Control Register 2 (CR2) at address 4 and Control Register 3 (CR3) at address 5 are unique to DSP-based K-Series parts. Other family members should not be written at these addresses. A full description of the functions of these registers can be found in the 73K224L data sheet.

The ID Register is a read only register at address 6 and allows the controller to access a bit pattern programmed into the chip during manufacture. The upper four bits are the family signature and can be used in part to determine the particular chip in use. A 73K212, 73K321 or 73K322 will show 00_2 in bits 7 and 6, respectively, a 73K221 will show 01_2 and a 73K222 will show 10_2. In these cases, bits 4 and 5 are undefined. A 73K224 will show 110_2 in bits 7, 6 and 5. You can't tell the difference between a 73K212, 73K321 and a 73K322 from the ID Register. The parts with integral UARTs, such as the 73K222U, do not implement the ID register. In fact, because of the need to control the UART, only CR0, CR1 and the Detect and Tone Registers conform to the architecture described above. A two bit signature has instead been placed in bits 6 and 7 of the Detect Register. In the ID Register, the bottom five bits are available for a customer specified code.

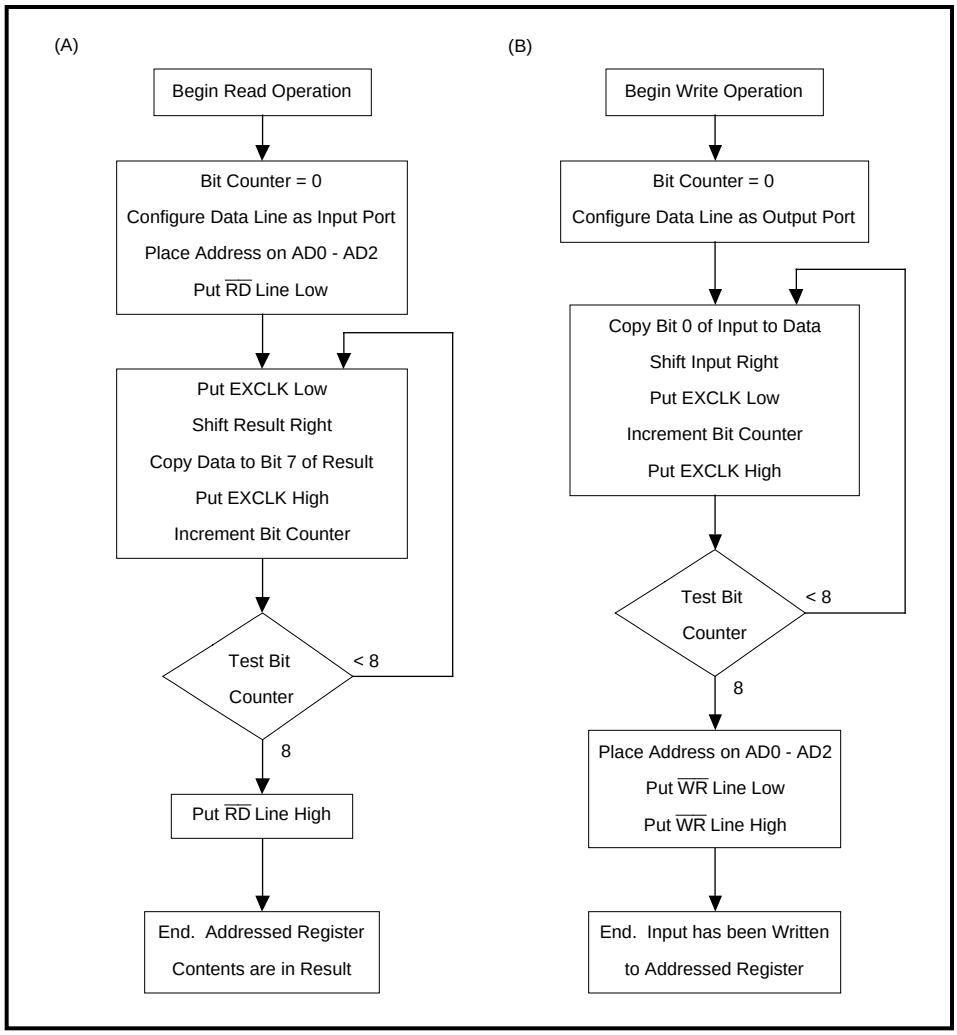


FIGURE 7 – 3: Flow-charts for Reading and Writing using the Serial Control Interface

7.1.2. Subroutines for the Serial Control Interface

The Serial Control Interface provided on the K-Series modems can result in a smaller system size as versions are available which support only this interface in smaller packages. However, as compared to the more straightforward parallel bus interface, the controller has the extra overhead of manipulating this interface. The code size overhead can be minimized by writing subroutines to write to and read from the K-Series serial control interface. Examples of flow-charts for such subroutines are shown in Figure 7-3. Controller I/O ports are dedicated to each of the seven lines of the interface, all are outputs except that the DATA line must also be programmed as an input for read operations. During power-on initialization, all lines should be put HIGH. There is a maximum rate at which the serial port can be accessed. Be sure that this timing specification is not exceeded in your design.

7.1.3. Setting Up the System and Data Transfer Format

Many of the bits in the control registers are not involved in the complicated process of establishing a call, but rather control such mundane things as the signal at the CLK pin or the data format. We will mention these bits now, because later we'll ignore them in the software discussion. Bit 0 of CR0 defines whether the modem will work as an answer modem or a calling modem. It is most important that this bit is correctly set because it controls many aspects of the chip's operation.

Selection of Data Transfer Format

Bits 2 to 5 in CR0 select the format of data transfer to and from the K-Series IC over the TXD and RXD pins. If the pattern is 1100_2, the FSK modulation modes are selected, which implicitly selects any character asynchronous data format of up to the maximum bit rate. In all other cases, DPSK or QAM modulation is selected and more care is required to establish a compatible data transfer format. Three synchronous modes are available in which data bits at TXD and RXD are timed by clocks at the TXCLK and RXCLK pins. The chip always provides receiver timing at RXCLK, however TXCLK may free-run or be brought into synchronism with an external clock at EXCLK or with receiver timing at RXCLK. All clocks must be within 0.01% of the nominal data rate. Four selections of character asynchronous formats are also available in which internal converters deal with any differences in the intra-character bit rate and the transmission rate to the remote modem. For these converters to work, the total character length, including start and stop bits, must be specified. 8, 9, 10 or 11 bit characters may be selected. Note that the integral UART versions use these bits slightly differently. Synchronous data transfer is not possible and in addition the character length is programmed into the UART and is read-only at CR0.

Reset Bit

The Reset bit (bit 2 in CR1) will normally be ZERO. Write a ONE here only to reset the entire chip and put it into power-down mode. The bit itself is automatically cleared back to ZERO. CLK Control at bit 3 in CR1 allows you to choose the signal presented at the CLK output pin of the chip. After a reset operation, it is ZERO and causes the crystal clock frequency to appear. By setting it to ONE, you can select the alternative of 16 times the bit rate in DPSK and QAM modes, which may be useful for driving a UART. You should program this bit consistently according to your hardware requirements. Note that by setting this bit after powering-down the K-Series part, you can slightly reduce idle power draw.

Tone Register

Moving on now to the Tone Register, Guard Tone (bit 6) should be set to enable the transmission of guard tones along with the answer modem's V.22 or V.22bis data signal if this is a requirement in the country of operation. Bit 0 in the TR allows you to choose the usual 1800 Hz guard tone (bit 0 = ZERO) or the 550 Hz guard tone (ONE) required in some Scandinavian countries. RXD Output Control allows you to put the RXD output pin into a high–impedance state so that it will float high as described in section 6.4.8, Floating and Clamping the RXD Pin. The reset state is ZERO which causes this pin to be driven. You should set it to ONE to float the pin as soon as possible on reset and leave it there until the point in the handshake when the received data line should be unclamped.

Control Registers

Control Registers 2 and 3 are only present in DSP-based parts. $\overline{\text{RESET DSP}}$ (bit 2 in CR2) is cleared to ZERO by a general chip reset operation and causes the DSP to initialize itself. It must be set to ONE before the chip is used to generate or detect any signals. If the DSP is to be reset, either with the reset of the chip or on its own, this bit must remain a ZERO for at least 2 ms. Call Initialize (bit 5 in CR2) is used in call mode to allow the DSP to perform certain functions at call establishment. The early 73K224L data sheet used the two terms call progress mode and call init mode to describe the state of the chip when this bit is ONE. These both mean the same thing, in this mode the chip is able to detect answer tones, call progress tones and unscrambled binary ONES only. When this bit is ZERO, the chip is in the demodulation mode and performs the normal receiver functions. Transmit Attenuator (bits 0 to 3 in CR3) allows the transmitter output level to be selected. On reset, these bits hold 0100_2 which selects the nominal level of -10 dBm at the line for compatibility with non-DSP K-Series parts.

7.1.4. Interrupts, Polling and the System Timebase

Your system will need some sort of timebase that can be used to time events in the handshake sequences and make sure that the status of the modem is polled regularly. In many cases, other requirements of your application will dictate the implementation. Each tick of the timebase will cause some code to be run which will update timers and look in the Detect Register for the status of the modem chip. The Receive Data bit changes at the data rate of up to 2400 bit/s for a V.22bis connection. During those phases when the data pattern must be monitored, some means of getting to the detect register at at least this rate must be found or the robustness of the handshakes will be compromised.

Detect Register Interrupt

Another means of getting at the modem status is to use the Detect Register Interrupt. The $\overline{\text{INT}}$ pin of the K-Series chip goes LOW when certain bits in the Detect Register change state under certain conditions. This pin can be connected to an interrupt input of the controller so that the firmware can read the register only when a significant change occurs. The Enable Detect Interrupt bit (bit 5 in

Control Register 1) must be set to ONE for the $\overline{INT}$ pin to go LOW and generate the interrupt. This bit is cleared to ZERO on reset and in this state inhibits the interrupt so that $\overline{INT}$ is held HIGH. Call Progress Detect (bit 1) and Answer Tone Detect (bit 2) can cause an interrupt only when the transmitter is disabled (bit 1 in CR0 = ZERO). Carrier Detect (bit 3) can interrupt when DTMF tones are not selected (Transmit DTMF, bit 4 in TR is ZERO). Unscrambled Marks Detect (bit 4) and Pattern S1 Detect (bit 6, where implemented) can interrupt at any time. $\overline{INT}$ goes active (LOW) on a change from ONE to ZERO or from ZERO to ONE of these bits and returns inactive (HIGH) when the controller reads the Detect Register or the K-Series chip is reset. The controller should read the Detect Register to determine which bit or bits have changed to cause the interrupt, whereupon the interrupt pin will return to the HIGH state. Long Loop Detect or Signal Quality (bit 0), Receive Data (bit 5) and Receive Level (bit 7) cannot generate interrupts. Using the interrupt, it is possible to watch for call progress tones, answer tone, carrier, unscrambled binary one and the S1 signal without regular polling. The problem with this is that all of these signals need to be qualified in some way by measuring their duration or cadence so that timers must be triggered by these changes of state rather than directly performing some action. We have found that once the timebase to run the timers is established, we might as well poll the Detect Register and ignore the interrupt. Depending on the interrupt handling capabilities of the controller you choose, you may decide to use the interrupt, or you may use polling during handshakes and the interrupt during data mode. Note that the Signal Quality bit and the Receive Data bit do not generate Detect Register Interrupts and if needed during data transfer must be polled anyway.

7.1.4.1. Sample Implementation Using Segmented Interrupts

A suitable implementation for the timebase and polling scheme of a K-Series modem is outlined here. It should support the 2400 bit / s data rate of the 73K224L and provide all modem related features such as signal quality monitoring and self-test pattern checking. An externally supplied timebase at 2400 Hz is assumed, perhaps from a timer in the microcontroller. The Detect Register Interrupt is not used, so we need to poll the Detect Marks, Detect Spaces, Detect Register for at least one purpose, since the Signal Quality bit cannot generate interrupts. To minimize the software overhead, things that only need to be done at 600 Hz are done only once every four timebase ticks. Furthermore, to prevent all the activity clustering in one interrupt, which would cause the next interrupt to be missed or the background activity to be starved of attention, these processes are distributed throughout the cycle of four ticks. Thus we arrive at the concept of segmented interrupts where the necessary processes are divided into segments and distributed to flatten the load placed on the CPU by interrupt activity.

When we (the controller) get the interrupt, we must first service the hardware timer causing the interrupt to re–initialize it for the next period. Then we can attend to the

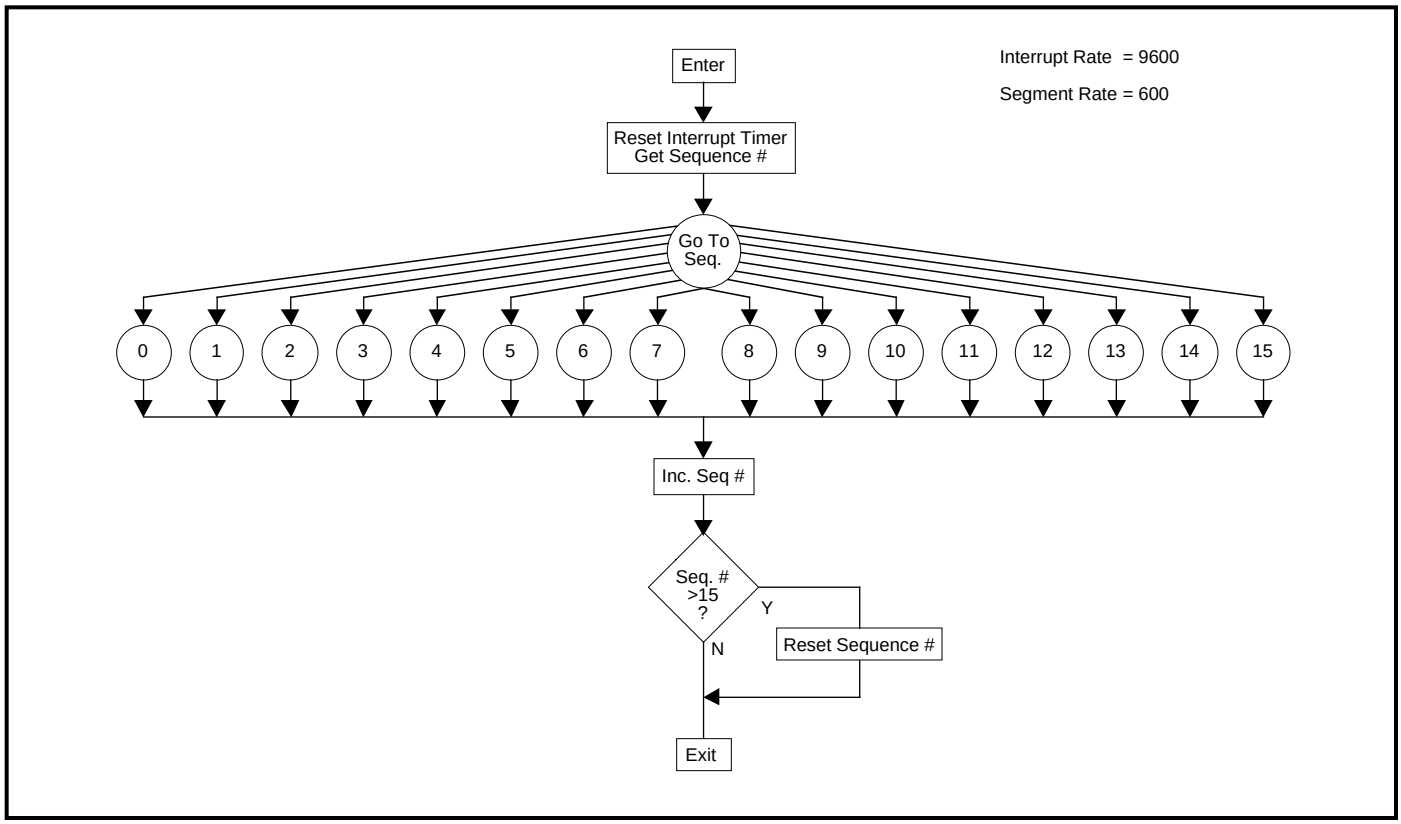


FIGURE 7 – 4: Flow-Chart of Segmented Interrupt Polling Scheme

modem chip. First, we read the Detect Register. Since the Receive Data bit is potentially flapping about at 2400 bit/s, we may have a new bit at each sample. We must therefore run some routines to look for patterns in the data according to the system state. For example, during handshaking we will have to recognize binary ONES at 1200 bit/s and later detect 32 consecutive ONES at 2400 bit/s. During data mode we may have to look for long strings of binary ZEROS to perform long space disconnect. As part of establishing a remote digital loopback test we will have to recognize reversals (alternating binary ONE and ZERO) and binary ONE in the initiating modem. When a self-test is in progress, we will have to check the received data against the test pattern, normally reversals. Each of these routines will have to be switched in and out as needed. Each will have its own method of detecting and qualifying its own pattern and coping with the possibility of slipping over bit boundaries as the interrupt rate and the data rate drift with respect to each other. To further reduce processor load, it is possible to collect four samples of the Receive Data bit and save them for processing at 600 Hz in a segment as below.

Having dealt with the received data pattern, the rest of the work can be done at 600 Hz. Rather than do everything in one interrupt out of four, we will divide up the tasks and perform a few at each interrupt in a cycle of four. For example, in interrupt one we could look at the Unscrambled Mark, Answer Tone and Pattern S1 bits. All three would not need to be qualified at all times, only the necessary routines would be run, however, we have gathered here all the information needed to start the connect handshakes. On interrupt two, we look at the Carrier Detect, Call Progress Detect and Signal Quality bits. The last two will never be needed together and with Carrier Detect we can complete call progress monitoring or signal quality, retraining and call termination functions. Interrupt three gives us an opportunity to update any timers we are using and check for expiration. We could also administer a state machine at this point and perform programming of the modem chip as states progress. Finally, we have reserved interrupt four for close examination of the received data bits collected at 2400 samples per second as above. The next interrupt will be interrupt one again and the sequence repeats. This is obviously not the only segmentation possible and may not be the optimum, but from this, the principle should be clear.

7.1.5. Using the Detect Register

In all K-Series family products, the status of the modem must be accessed by the controller via the Detect Register (DR) at address 010_2. The individual data sheets contain a description of the register but we will review each bit here to refresh our memories and point out the small differences within the K-Series family.

Bit 0: Signal Quality or Long Loop Detect

Once a connection has been established, this bit allows the controller to get an estimate of the likely error rate. In K-Series parts equipped with a DSP for 2400 bit/s demodulation, a fairly accurate indication is given by the Signal Quality, computed from the adaptive equalizer error. In parts without a DSP, a rough idea of how good the connection is can be obtained from Long Loop Detect which indicates the received signal strength.

Bit 1: Call Progress Detect

This bit indicates the presence of energy in the call progress band. By looking at the cadence of this bit, dial tones, ringback, busy tones, etc., can be detected. In DSP based parts, you must set the Call Init bit (bit 5) in Control Register 2 to ONE in order to get a valid reading from the Call Progress Detect bit.

Bit 2: Answer Tone Detect / Special Tone Detect

This bit is used for the detection of tones at specific frequencies. In most cases this is the answer tone from the other modem at 2100 Hz or 2225 Hz as selected by bit 0 in TR. For this to operate, the chip must be in call mode (bit 0 in CR0 = ONE). Parts with V.23 capability use this bit to indicate calling tone detection when the chip is in answer mode, refer to the data sheet.

Bit 3: Carrier Detect

The presence of a receive signal above the threshold in the selected band is indicated in this bit. The band will depend on the modulation mode selected and whether the chip is in call or answer.

Bit 4: Unscrambled Marks Detect

This bit indicates the presence of an unscrambled binary one signal at 600, 1200 or 2400 bit/s at the receiver for DPSK and QAM handshakes. It operates differently in DSP-based and non-DSP K-Series modems.

Bit 5: Receive Data

This bit exactly mirrors the received data presented by the chip at the RXD pin except that it is still valid when the RXD pin is floated. Note that when the Carrier Detect bit is ZERO, this bit and the RXD pin are clamped to ONE (mark). So don't qualify scrambled binary ONES without checking Carrier Detect first because you may find them even when they're not there.

Bit 6: Pattern S1 Detect

In DSP-based parts with V.22bis capability, this bit indicates that the received signal matches the spectrum of the S1 signal. As this signal is of very short duration in the handshake and the Pattern S1 bit may be triggered for short times during normal data transmission, it is important to qualify it carefully as discussed in section 7.4.6.

Bit 7: Receive Level

DSP-based parts use this bit to indicate that the received signal strength is above an acceptable threshold. It should be examined to see if it is safe to switch in the extra receiver gain to improve dynamic range.

Bits 6 and 7 are unused in 1200 bit/s non-UART versions and in integral UART versions, which provide a fixed device signature in lieu of the ID register.

During the connect handshake and monitoring of the data state, the modem must look for certain signals at its receiver. As discussed above, the controller examines bits in the DR, however, it is rarely sufficient to wait for the bit to go to ONE and immediately take the action associated with the receipt of the signal. There are two reasons for this. First, the specification of the handshake often requires you to detect the signal for a certain period of time before taking action. For example, during the V.22 connect handshake, the unscrambled binary ONES signal from the answering modem must be seen for 155 ms by the calling modem. The Unscrambled Mark detector bit in the 73K224L responds to the signal in a much shorter time, typically 20 ms. Secondly, some of the detectors can be triggered during normal data transmission. This is not a fault, but is caused by the random nature of the data signal. The controller must therefore recognize the change in a DR bit, but continue to examine the bit for a period of time before considering the signal to be present. We call this process qualifying a signal or DR bit.

The simplest method of doing this, which we have used with some success, is an "increment or dump" counter. A counter and a flag are associated with each signal to be qualified at any one time. Convert the time for which the signal must be present (the qualification time) into a number by subtracting the typical delay time of the K-Series chip detector (see the data sheet) and multiplying the result by the polling rate. In the firmware, at the established polling rate (e.g., 600 Hz), examine the bit that indicates the presence of the signal and if it is ONE, increment the counter. On the other hand, if it is ZERO, clear the counter. If the counter gets incremented to the number representing the qualification time, then set the flag to indicate the successful qualification of the signal. Whenever the counter is cleared, reset the flag and counter to indicate that the signal is not present or the detection of the end of the signal. This technique allows you to be sure that the signal has been present for the appropriate time and to reject spurious responses to normal data signals. In an application note on the 73K224L (AN100-1.0), this technique was described as a "sliding window counter." A true sliding window (where the number of ONES polled during a preceding fixed time period is counted) is too complex and unnecessary in this application. The "increment and dump" method can also be adapted to "ride out" a short loss of the signal due to a burst of noise on the line. When the flag is set, clear the counter and in future increment it when the DR bit is ZERO and clear it when it is ONE. Watch for the counter to hit a new, much smaller threshold and only clear the flag when that happens, reverting to the previous counter operation. A small delay, equal to the threshold times the polling period, will be added to the detector hold time, but the detector robustness is improved. The following sections expand on this discussion for a few of the DR bits, the proper qualification of which is particularly important.

7.1.5.1. Qualifying the Unscrambled Marks Detect Bit

The unscrambled binary ONES signal is recognized in K-Series modems by its spectrum rather than any data pattern generated so that its detection does not depend on the operation of an equalizer. In the non-DSP parts, which have an upper data rate limit of 1200 bit/s, the unscrambled ONES signal is fully qualified internally and the Detect Register bit does not go to ONE until the signal has been present for 159 to 172 ms. Thus for both the V.22 connect handshake and remote digital loopback requests, as soon as bit goes high the state machine should proceed. On the other hand, the DSP-based parts, such as the 73K224L, respond to the unscrambled ONES signal with a delay of about 20 ms. It is therefore necessary to qualify the signal further before taking any action. This is an important difference that should be allowed for when designing code to drive a variety of K-Series chips. The code can configure itself by reading the ID register. Note that in the parts using DSPs (such as the 73K224L), this bit is valid in both the demodulation and call initialization modes. Only in the very first engineering samples of the 73K224L was this bit not available in the call initialization mode, although documentation may still be in circulation which reflects this early situation.

7.1.5.2. Monitoring the Modem's Received Data Line

There are several circumstances in which the microcontroller needs to monitor the bit pattern that the modem is receiving over the telephone line. During the Bell 212A, V.22 and V.22bis connect handshakes, it is necessary to make sure that the received data, after the descrambler, has settled to a constant binary ONE. This is especially important when an attempt is being made to recognize the data rate of an unknown remote modem. Also, during the establishment of remote digital loopback, it is necessary to detect a pattern of alternate ONES and ZEROS in the initiating modem and the continuous ONES in both initiating and responding modems. In normal data transmission mode, the only reason to monitor the received data is to detect a long space disconnect signal (see section 7.7.2, Long Space Disconnect). This feature is not essential to a good implementation and is normally disabled by default in modems that provide it.

We know that we can read the state of the RXD line at Receive Data (bit 5) of the Detect Register, even if the RXD pin has been tri-stated. However, no direct means of indicating when a new data bit has been presented at RXD is provided and the Receive Data bit cannot generate a Detect Register Interrupt. This is not a problem if the controller can poll the DR and examine Receive Data

frequently enough. A rate of a little over the bit rate is adequate for unambiguous reading of the data if your algorithm is prepared for the inevitable drift of the polling time across the boundaries between bits. For detecting the (scrambled) binary ONES segments of the connect handshake, a rate of 1200 Hz is recommended. In the V.22bis handshake, you must detect 32 consecutive ONES at 2400 bit / s to confirm the "gear shift" to this data rate and a higher sampling rate is needed. In many instances, the provision of a 2400 to 2500 Hz polling rate will not be a problem. However, if the system architecture in some way precludes this, an alternative must be sought. You may be able to turn on a special timebase during those periods when the received data pattern must be examined. If your system will allow the data to be presented at the RXD pin during the handshake (normally, this pin is floated to ONE), then external circuitry, such as a UART, can monitor the data. If all else fails, you will have to design an algorithm to detect the pattern using the polling rates you can support and accept the reduced robustness of the handshakes.

If your hardware system cannot supply a constant polling timebase of suitable frequency, but you have a UART in the system, then we have a suggestion for you. Configure the UART for a bit rate of eight times the rate at which you wish to examine Receive Data. Set it for six data bits, one stop bit and no parity so that the serial data frame contains eight bits, including start and stop. The Transmit Buffer Register will now empty at the required rate and the Receive Data bit can be polled as part of the TBRE interrupt service routine. Remember to write some dummy data to the Transmit Buffer Register to clear the interrupt. Obviously, this procedure will interfere with normal use of the UART, but this may not matter as during the times when the received data pattern must be known, no user data is passing over the line.

The UART cannot be used as described above for the detection of long space disconnect as this must occur during normal data transmission. However, most UARTs, including the on-chip UART of the "U"-suffix K-Series modems, have a Break Interrupt. The onset of the long space disconnect signal at the receiver will trigger the Break Interrupt of a UART connected to the RXD output. If this happens persistently for 1.6 seconds, then a long space has been received.

If you pass the RXD output to the UART during the handshake you can use it to detect continuous binary ONES by measuring the time for which no received characters are indicated. By increasing the UART data rate, you can increase the speed of its response to a binary zero in the received data stream, which it will read as a start bit followed by some zero data bits. Increment the "increment and dump" counter at the polling rate while the UART stays quiet and clear the counter when the UART indicates a received character. If the counter reaches its threshold, then the required duration of binary ONES has been received. Some care will be needed if you want to qualify before the equalizer has been enabled in DSP-based parts and a few ZEROS are to be expected due to decision errors.

7.1.5.3. Qualifying the Pattern S1 Detect Bit

The S1 signal is recognized in DSP-based K-Series modems by its spectrum rather than any data pattern generated so that its detection does not depend on the operation of the adaptive equalizer. The duration of the S1 signal that must be detected is a brief 100 ms. The 73K224(L) detector takes from 15 to 32 ms to recognize the pattern, but, as discussed above, the controller should not assume that an S1 signal is present as soon as the Pattern S1 bit goes to a ONE. Normal data can look like S1 for short periods of time. We have found that if the controller looks for Pattern S1 to be constantly ONE for 50 ms, then the pattern will be reliably detected and no spurious indications will result. This bit is only changed by the 73K224(L) internal workings at 1.67 ms intervals, so it is sufficient to sample this bit at 600 Hz or above. At 600 Hz, if 30 consecutive 1's are received, then S1 may be considered valid.

In V.22bis modems, the end of the S1 signal is very important to establish system timing. The 73K224L has a hold time of 4 to 21 ms on the Pattern S1 bit. You can assume that S1 has ended if this bit is zero for three to five samples at 600 Hz. This will add only slightly to the hold time, which will appear in the handshake as an additional delay in the network. The "increment or dump" algorithm is highly suited to S1 qualification.

7.1.5.4. Use of Software Techniques in Actual Handshake Sequences

The preceding sections have discussed general software design considerations for modem products. The next sections show how these techniques would be used in a complete intelligent modem design. This discussion refers to the actual software used in Silicon Systems' demonstration boards for the 73K224L.

7.1.5.5. Handshake State Machine

The following is a description of the handshake state machine, which defines those decisions and actions that must be performed by controller software to execute the handshake. Each "state" typically refers to a set of software instructions, or module, which controls the functions specific to that state. This example uses the interrupt structure in the following interrupt description and conforms to the Protocols outlined in Appendix F. For a more in-depth understanding of how to use the 73K224 registers it is recommended that you use this section as a guide, referring back to it during your reading of the descriptive text, which starts in section 7.2.

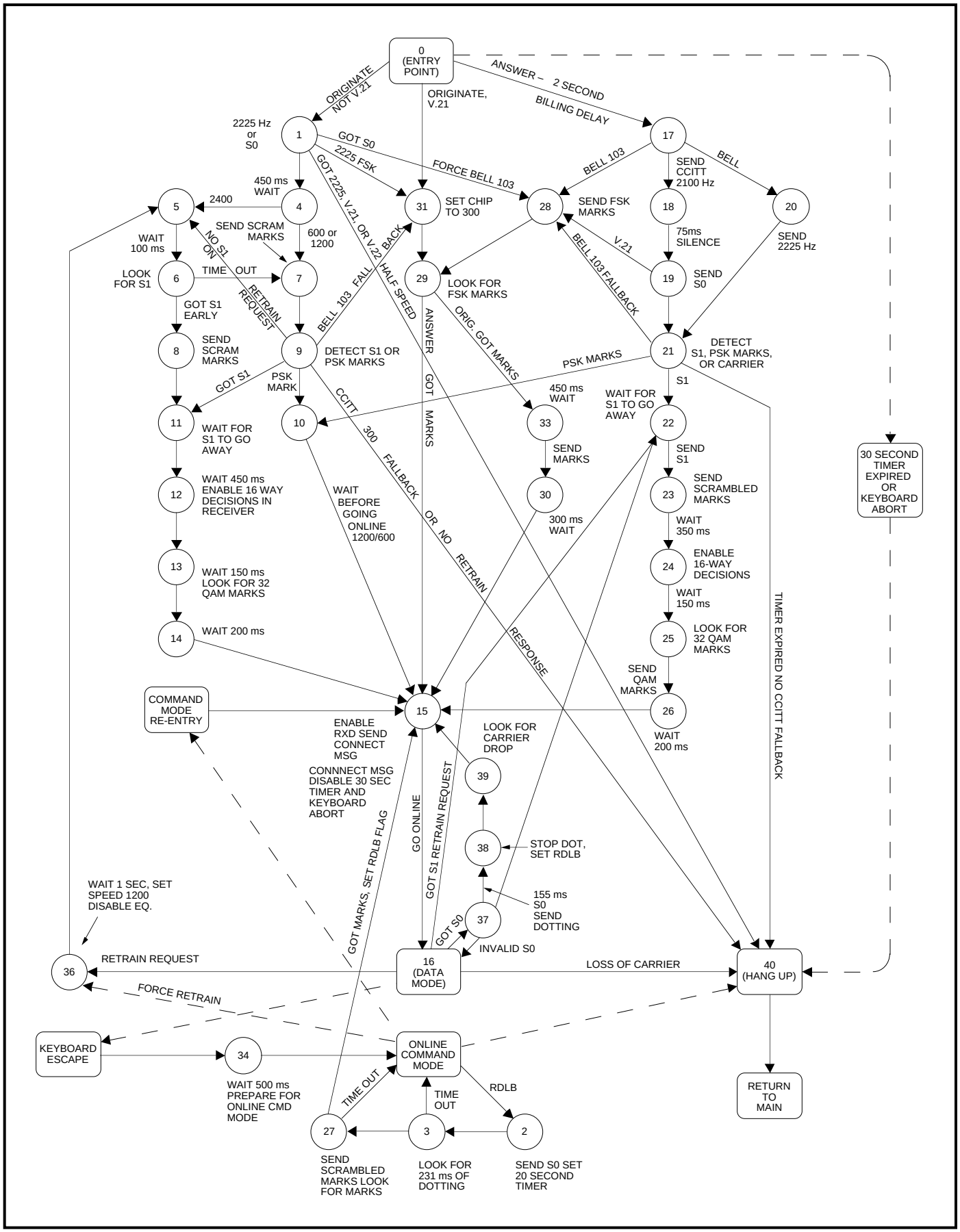


FIGURE 7 – 5: Flow Chart 73K224L State Machine

```
STATE_0:      ************ STATE_0 **************

        Main entry point into handshake routines
        start 30 second connect timer
            ***  if this timer expires before the handshake
                 is completed then the
                 connect sequence will be terminated.
        initialize K224
        set speed of chip to 1200
        enable S0 debounce timer
        clear DTMF0 bit to set answer tone detector to 2225 Hz

        if call / originate then
                if 1200 or 2400 goto STATE_1
            if Bell 103 goto STATE_1
            if V.21 then set V.21 mode and goto STATE_31
            if V.22 half speed then set chip speed to 600
                    and goto STATE_1
        if answer then
            if 600 then set chip speed to 600
            if Bell 103 then set Bell mode
            if V.21 then set V.21 mode
            set up 2 second billing delay and go start
            handshake
            goto STATE_17

STATE_1:      ************ STATE_1 **************

        Call / originate MODE ENTRY POINT
            search for 155 ms of Bell answer tone or
            PSK unscrambled marks (2225 Hz or S0)
                GOT 2225 Hz:
                    if we are 600 goto STATE_40 ( hang up )
                    if we are V.21 goto STATE_40
                    if we are Bell 103 set bell mode and goto STATE_31

                    otherwise set timer for 450 ms and goto STATE_4
                GOT S0:
                    if we are set to 300 go force 300 at STATE_28
                    disable call init mode
                    set up 450 ms delay
                    goto STATE_4

STATE_2:      ************ STATE_2 **************

        RDLB REQUEST ENTRY POINT....
            Send scrambled marks @ 1200 or 2400
            Set timeout timer to 20 seconds
            Clear baud counter
            Goto STATE_3
```

```
STATE_3:      ************ STATE_3 ***************

        If timeout timer is still valid
            look for 231 ms of dotting pattern
                if dotting received
                send scrambled marks
                goto STATE_27
        If timer times out
            send NO RDLB RESPONSE
            return to MAIN (STATE_16)

STATE_4:      ************ STATE_4 ***************

        wait out 450 ms delay and check speed
        if we are 2400 goto STATE_5 ( send S1 )
        else 600 or 1200 goto STATE_7 ( don't send S1 )

STATE_5:      ************ STATE_5 ***************

        we are 2400 so send 100 ms of S1
        set pattern to S1
        turn on transmitter
        Enable S1 debounce timer
        set wait timer to 100 ms and goto STATE_6

STATE_6:      ************ STATE_6 ***************

        it is possible to receive S1 while
        sending S1 so wait out 100 ms timer
        while looking for S1.
        If S1 received early goto STATE_8
        otherwise goto STATE_7

STATE_7:      ************ STATE_7 ***************

        SEND SCRAMBLED MARKS....
            enable equalizer
            turn on scrambler
            set pattern to marks
            turn on transmitter (in case we arrived from STATE_4)

            turn on the equalizer
            set up 2 second timer for fallback timeout
            clear baud timer
            goto STATE_9

STATE_8:      ************ STATE_8 ***************

            got S1 early so wait out 100 ms and send scrambled
            marks
            enable equalizer
            turn on scrambler
            set pattern to marks
            goto STATE_11
```

```
STATE_9:      ************ STATE_9 **************

        look for S1 or PSK MARKS while 2 second timer is
                running
            only look for S1 if we are 2400 or retrain
            If not RETRAIN then look for PSK MARKS
                GOT S1
                    goto STATE_11
                GOT MARKS
                    set timer to 765 ms and goto STATE_10
                TIMER EXPIRED
                    if retrain then
                        increment retrain counter
                        if retrain counter >= 40 then goto STATE_40
                    if we are CCITT then goto STATE_40 ( hang up )
                    otherwise set Bell mode and goto STATE_31

STATE_10:     ************ STATE_10 **************

        got MARKS must be 1200 or 600
        wait for timer to expire
        check RXLVL, set RXGAIN bit if needed
        enable equalizer
        if originally 600 then goto STATE_15
            else this could be a fallback from 2400
            so set speed bits to 1200
            goto STATE_15

STATE_11:     ************ STATE_11 **************

        got S1 so wait for S1 to go away
        check RXLVL, set RXGAIN bit if needed
        enable equalizer
        set speed to 2400 and set up 450 ms wait
        goto STATE_12

STATE_12:     ************ STATE_12 **************

        wait 450 ms
        enable 16 way decisions in receiver
        set up 150 ms wait
        goto STATE_13

STATE_13:     ************ STATE_13 **************

        wait out 150 ms
        set speed of chip to 2400 and send QAM marks
        set up wait timer for 200 ms
        clear baud counter
        goto STATE_14

STATE_14:     ************ STATE_14 **************

        look for 32 consecutive marks
        make sure timer has expired
        goto STATE_15
```

```
STATE_15:       ************ STATE_15 **************

        COMMON ENTRY POINT TO GO ONLINE
            send connect msg
            enable RxD
            allow transmitter to send data
            turn off the speaker
            clear the baud counter
            goto STATE_16

STATE_16:       ************ STATE_16 **************

        ONLINE DATA MODE MAIN LOOP STATE
        if not 1200 or 2400 then just check for carrier
            if RDLB flag is set then just exit (loop)
            if RETRAIN is enabled then
                    look for S1
                GOT S1...
                    set pattern to marks
                    DISABLE receive DATA
                    set speed to 1200
                    disable the equalizer
                    set for 4 way decisions
                    goto STATE_22
            if SQI bit set then set retrain flag
            if retrain flag is set (forced or SQI bit)
                    set wait timer to 1 second
                    go force a retrain (STATE_36)
            Look for S0....
            if S0 then
                    clear the baud counter
                    goto STATE_37 (could be RDLB or Hayes retrain)
        if LCD is enabled look for carrier
                if carrier goes away go hang up line
        otherwise loop forever...

STATE_17:       ************ STATE_17 **************

        ANSWER MODE
            wait for 2 second billing delay
            if not 2400 check if Bell or CCITT
            if 2400 assume CCITT
                CCITT...
                set wait timer to 3.3 seconds
                set tone bit to 2100 Hz
                enable answer tones
                turn on the transmitter
                goto STATE_18
                Bell...
                if 300 goto STATE_28
                if 1200 goto STATE_20
STATE_18:       ************ STATE_18 **************

        CCITT ANSWER MODE
            wait out 3.3 second timer
            turn off answer tone
            set up wait for 75 ms silence
            goto STATE_19
```

```
STATE_19:       ************ STATE_19 **************

        wait for 75 ms silence
        if 300 V.21 goto STATE_28
        else set TxD pattern to MARKS
            turn on transmitter
            enable equalizer
            start 3 second validation timer
            enable S1 debounce timer
            clear baud counter
            goto STATE_21

STATE_20:       ************ STATE_20 **************

        BELL MODE
            set 2225 hz answer tone bit
            enable answer tones
            turn on transmitter
            enable equalizer
            start 2 second validation timer
            enable S1 debounce timer
            clear baud counter
            goto STATE_21

STATE_21:       ************ STATE_21 **************

        during 3 second validation time
            if we are 2400, look for S1 or PSK MARKS
            if 1200, just look for PSK MARKS
                GOT S1. . .
                goto STATE_22
                GOT PSK MARKS, must be 1200 or 600
                enable equalizer
                set up 765 ms timer
                set DCD
                turn off answer tones
                set TxD pattern to MARKS
                turn on the scrambler
                goto STATE_10
            if 3 second timer expires . . . .
                look for carrier . . .
                CARRIER FOUND . . .
                    if we are CCITT then goto STATE_40 ( hang up )
                    otherwise set Bell mode in chip and go STATE_28

                CARRIER NOT FOUND . . .
                    reset 3 second timer and keep looking . . .

STATE_22:       ************ STATE_22 **************

        wait for S1 to go away
        check RXLVL, set RXGAIN bit if needed
        enable equalizer
        set pattern to S1
        set wait timer for 100 ms
        goto STATE_23
```

```
STATE_23:       ************ STATE_23 **************

        wait out 100 ms delay
        set TxD pattern to MARKS
        turn on the scrambler
        set up wait timer for 350 ms
        goto STATE_24

STATE_24:       ************ STATE_24 **************

        wait for 350ms
        enable 16 way decisions in receiver
        set up wait timer for 150 ms
        clear baud counter
        goto STATE_25

STATE_25:       ************ STATE_25 **************

        look for 32 consecutive QAM marks
        wait for timer to expire
        set TxD pattern to MARKS
        change chip speed to 2400 ( QAM MARKS )
        set wait timer for 200 ms
        goto STATE_26

STATE_26:       ************ STATE_26 **************

        wait out 200 ms delay
        goto STATE_15

STATE_27:       ************ STATE_27 **************

        Check for timer timeout...
            Look for 231 ms of MARKS
                GOT MARKS...
                    set RDLB flag
                    return to online state (STATE_15)
                NO MARKS...
                    reset baud counter and exit
        TIMER TIMEOUT...
            send no RDLB response
            return to MAIN (STATE_16)

STATE_28:       ************ STATE_28 **************

        300 BAUD ANSWER MODE ENTRY POINT
            disable call init mode
            set chip speed to 300
            disable equalizer
            disable the scrambler
            set pattern to MARKS
            turn on the transmitter
            clear the baud counter
            goto STATE_29
```

```
STATE_29:       ********** STATE_29 **********

        COMBINED ANSWER / Call/originate MODE
            look for 155 ms of FSK marks
                set speed bits to 300
                if call/originate mode
                    set up 450 ms timer
                    goto STATE_33
                if answer mode
                    goto STATE_15

STATE_30:       ********** STATE_30 **********

        wait for timer to expire
        make sure speed bits are set to 300
        goto STATE_15

STATE_31:       ********** STATE_31 **********

        300 BAUD Call/originate MODE ENTRY POINT
            disable call init mode
            disable equalizer
            disable the scrambler
            set chip speed to 300
            goto STATE_29

STATE_32:       ********** STATE_32 **********

        NOT USED AT THIS TIME

STATE_33:       ********** STATE_33 **********

        wait out 450 ms timer
        set pattern to MARKS
        turn on transmitter
        set up wait timer for 300 ms
        goto STATE_30

STATE_34:       ********** STATE_34 **********

        Exit point for online command mode
        When the serial interrupt routine gets an
        escape sequence it moves #34 into STATE and
        we exit through here.

        set up 500 ms wait
        wait out 500 ms timer
        tristate RxD
        set TxD pattern to MARKS
        set command mode flag
        reset receive and transmitter buffers
        exit state machine and go to MAIN

        reentry is done through STATE_15 (ONLINE)
        or STATE_40 (HANG UP).
```

STATE_35: ********** STATE_35 **********

NOT USED AT THIS TIME

STATE_36: ********** STATE_36 **********

Wait for timer to expire and initiate a RETRAIN

wait for timer to expire
Tristate RxD
set TxD pattern to marks
set speed to 1200
disable the equalizer
set for 4 way decisions
goto STATE_5

STATE_37: ********** STATE_37 **********

Look for S0 ON-TIME to distinguish between RETRAIN or RDLB requests.
Some modems send a double dotting pattern (S1) that is not synchronized with its BAUD clock. Because the K224 looks at spectral response for its detectors and not data patterns the S1 pattern for retrain sometimes looks like S0. Our solution for this problem is to qualify S0 so that a response of 100 ms or less is taken as an S1 or retrain request, and S0 of 155 ms or greater is of course defined as an RDLB request from the remote modem.

```
if s0 is on for at least 155 ms then
    send dotting pattern
    goto STATE_38
if s0 is on for 100 ms or less
    if retrain enable flag is set
        setup for retrain
        goto STATE_22
otherwise return to STATE_16 online...
```

STATE_38: ********** STATE_38 **********

```
Wait for S0 to go away
    set RDLB flag
    stop sending dotting
    put chip in RDLB
    goto STATE_39
```

STATE_39: ********** STATE_39 **********

Look for 77 ms carrier drop...

```
wait for Carrier to drop
    clear test modes
    clear RDLB flag
    wait 1 second for things to settle
        return online (STATE_15)
```

STATE_40: ********** STATE_40 **********

Turn off speaker
reset buffers
tristate RxD
turn off transmitter
go On-Hook
send “No Carrier” msg
clear DCD
clear CD LED
return to MAIN (STATE_16)

INTERRUPT STRUCTURE

The interrupt service routine is running at 9600 hz and is split into 16 parts, each part executing once every 16 interrupts to give a combined speed of 1.666 ms or 600 hz (one BAUD time at 600,1200 or 2400 bit/s rates).

The main loop first reads and updates the detect register. Then it looks for transitions (1 to 0 or 0 to 1) of the receive data bit for detection of dotting pattern used in RDLB handshake. When a transition occurs a counter is incremented. This counter is sampled and reset every eight BAUD times in segment 15. Since dotting pattern by definition is 10101010 the number of transitions should be equal to the bit rate, ie: 8 baud times @2400 bit/s= 32, 8 baud times @1200 bit/s = 16.

After looking for transitions of the receive data bit it then looks at the interrupt counter and jumps to the appropriate interrupt segment. The following is a description of each part:

********** INT 0 **********

Sample the detect register
get rxd bit and move it into marks1
(this is done 4 times in the interrupt routine
because at 2400 you get 4 bits per baud)

********** INT 1 **********

move detect bits to port for examination

********** INT 2 **********

if enabled debounce S0 detector

********** INT 3 **********

if enabled debounce answer tone detector

********** INT 4 **********

Sample detect register
get rxd bit and move it into marks2

********** INT 5 **********

output detect bits to port for examination

********** INT 6 **********

update carrier detect...
    if in command mode don’t update carrier
    if connected...
        if carrier detect drops then tristate rxd
        if carrier good enable rxd

```
********** INT 7 **********

service WAIT timer
service GP1 timer
service GP2 timer

********** INT 8 **********

Sample detect register
get rxd bit and move it into marks3

********** INT 9 **********

output detect bits to port for examination

********** INT 10 **********

if enabled do S1 debounce

********** INT 11 **********

enabled do CPD debounce (CPD = CALL PROGRESS
DETECT BIT)

********** INT 12 **********

Sample detect register
get rxd bit and move it into marks4
if marks1,marks2,marks3,marks4 = 1 then set marks
if not clear marks

********** INT 13 **********

output detect bits to port for examination

********** INT 14 **********

if enabled do SQI debounce (Signal Quality)
increment the BAUD COUNTERS

********** INT 15 **********

decrement the transition detector baud counter
if counter = 0 then
    reload counter to 8
    get the transition counter
    if not 1200 or 2400 then reset dotting bit and exit
        if 2400 then compare transition counter to 31
            if trcnt >= 31 then set dotting
            else reset dotting
            exit
    if 1200 then compare transition counter to 15
        if trcnt >= 15 then set dotting
        else reset dotting
        exit
```

K224DEMO originating as:			Bell			CCITT			
			300	1200	2400	300	600	1200	2400
Calling a:									
Bell	300	(103)	300	300	300				
	1200	(212A)	300	1200	1200			1200	1200
	2400	(224)**	300	1200	2400*			1200	2400*
CCITT	300	(V.21)				300			
	600	(V.22hs)					600		
	1200	(V.22)		1200	1200			1200	1200
	2400	(V.22bis)		1200	2400*			1200	2400
K224DEMO answering as:			**Bell**			**CCITT**			
			300	**1200**	**2400**	**300**	**600**	**1200**	**2400**
Calling a:									
Bell	300	(103)	300	300	300				
	1200	(212A)	300	1200	1200			1200	1200
	2400	(224)**	300	1200	2400*			1200	2400*
CCITT	300	(V.21)				300			
	600	(V.22hs)					600		
	1200	(V.22)		1200	1200			1200	1200
	2400	(V.22bis)		1200	2400*			1200	2400

NOTES: *2400 connect is always V.22bis
**Bell 224 is the same as V.22bis except it has a 2225 Hz answer tone instead of 2100 Hz preamble. The K224DEMO will handshake in call / originate mode but answer mode is V.22bis. The K224DEMO will not generate 2225 Hz in 2400 answer mode.

FIGURE 7-6: Handshake Protocols Supported in 73K224 Demo Code

7.2. ESTABLISHING A CALL - THE CALLING MODEM

In a data communication session, the first action is generally taken by the calling (originate) modem, so this is a good place to start our discussion of the work that the controller must do in the system. This neglects actions taken at power-on, but these will be very dependent on your system. Here we assume that the K-Series modem IC is in the power-down state. The way in which the process of making a call will be triggered is defined by the requirements of the system you are designing. In a simple modem application, it would be a command from the host computer to which the modem is connected. A Hayes™ compatible modem will respond in this way to the ATD<number> command. In an embedded application, where the modem function forms a part of a more complex system, the instruction to place a call could come from an operator or somewhere else in the system.

7.2.1. Going "Off-Hook"

On receiving the instruction to place a call, the controller should energize the hook relay to seize the telephone line. The closure of the relay causes current to flow in the local loop which connects you to the telephone company's central switching office or exchange. On detecting this current, the central office will present a dial tone on the line and will allocate switching plant to receive and act upon the number you dial. This is a convenient time to wake up the K-Series modem as we will need it to listen for the dial tone. Write something like 00000101_2 to Control Register 0 to bring the modem IC out of power-down mode. Bits 2 to 7 select the operating modes and don't really matter so long as bits 2 to 5 are not all ZERO, which would select power-down. If the controller knows what modes are to be used, you might as well set them at this point. Bit 1 should be ZERO as shown

to keep the transmitter quiet and bit 0 should be ONE to select the call (originate) mode. All the other Control Registers and the Tone Register will have been set to their safe default states while the IC was in power-down. You may have to change this now, in particular for DSP-based parts such as the 73K224L you will have to wake up the DSP and put it into Call Progress mode by writing 00100110_2 to Control Register 2. If the controller code is to use interrupts to monitor call progress tones, etc. they will have to be enabled by writing a ONE to bit 5 of Control Register 1.

7.2.2. Dial Tone Detection

When you pick up a telephone to make a call, you usually check to make sure that the dial tone is present in the earpiece. It is good practice for machines that use the network to wait for a dial tone in a similar way. The central office does not allocate switch gear to your loop immediately when you seize the line, there will be a short delay while it searches for available plant to connect to your line. If dialing begins during this time then a part of the number will be lost and the desired connection will not be made.

After going off-hook, then, a modem should wait until it has detected the dial tone before beginning to dial. Dial tone will typically appear about one third of a second after going off-hook. If it has not appeared after five seconds, then it probably never will, so the controller should put the modem back on-hook and follow some fault recovery procedure. This may be as simple as sending a NO DIAL TONE message to the operator. Hayes AT™ compatible modems wait five seconds for a dial tone before giving up (if dial tone detection is enabled with the ATX2 or ATX4 commands). The first time that the CALL PROGRESS bit in the Detect Register of the K-Series IC goes high should not be interpreted as a dial tone. Many other spurious signals on the line can trigger the call progress tone detector. The controller should wait for the CALL PROGRESS bit to stay continuously high for about one second before proceeding with dialing.

The nature of the dial tone varies from country to country. In this manual, we consider dial tone to be a call progress tone and further discuss its nature in section 7.2.4. It will usually be at a higher signal level than other tones because it originates at the local central office rather than at the remote office.

7.2.2.1. Blind Dialing

Some modems do not detect dial tone before they dial. This is known as blind dialing, although it would be more sensible to call it deaf dialing. Even so, a pause of several seconds is necessary to allow the central office to allocate switching plant to the line after line seizure and before dialing begins. Hayes compatible modems can be configured to dial from 2 seconds to 255 seconds after going off–hook by changing the value in "S" register S6. The default time is 2 seconds. As the K-Series modems have provision for dial tone detection we would suggest that blind dialing be avoided. In many countries it is not permitted and a modem with this capability will not be approved for sale. S6 would then become a minimum time after going off–hook and before dialing.

7.2.2.2. "One-Eyed" Dialing

A variation of blind dialing, which has on occasion been termed "one-eyed" dialing, may also be used in countries where blind dialing is permitted. In this case, if dial tone is detected for some short time, then dialing begins. If dial tone is not detected for a much longer period of several seconds, then dialing begins anyway. This combines the "might-as-well-go-for-it" attitude of blind dialing with the faster response of modems that can detect the presence of dial tone as soon as switching plant is allocated to the line. Again, some national administrations will not approve modems with this capability.

7.2.3. Dialing the Number

Having seized the line and seen that the central office has allocated switching plant by detecting dial tone, you must next give the office the telephone number to which you want to be connected.

The original method of sending telephone numbers to the network routing plant was by pulsing the loop current. Current has been drawn in the loop to seize the line, this is then interrupted for brief periods in a pattern to indicate the number desired (see section 7.2.3.1 below). The central office does not release the line during these short disruptions, but counts the pulses and measures the pauses between them to route the call. Pulse dialing is rapidly being replaced by tone dialing (see section 7.2.3.2 below) as central office plant is modernized.

Tone dialing is faster than pulse dialing and is normally used where available in the network. The K-Series modem ICs incorporate a DTMF (dual-tone multi-frequency) generator so that no extra hardware is needed to perform tone dialing. Most modems for broad markets will include capabilities for both pulse and tone dialing. For specific applications, where the user has control over the type of telephone line to be used, it may be possible to eliminate pulse dialing capability.

7.2.3.1. Pulse Dialing

The hardware needed for pulse dialing is discussed in section 6.5.3.4, Pulse Dialing Circuits. The K-Series modem IC is not involved in this process as the controller directly activates and deactivates the pulse dial relay. If a part with integral UART is used, however, it provides the hardware interface between the controller and the relay, see section 6.5.12.4.

The U.S.A. does not publish a requirement for the pulse rate or the make/break ratio for pulse dialing, therefore anything that works will do. We suggest that you use a pulse rate of 10 pulses per second and a make-to-break ratio of 39:61. Thus the separation from one pulse to the next is nominally 100 ms. This is divided into a "break" period of

nominally 61 ms during which the loop current is interrupted and a "make" period of nominally 39 ms during which it is restored. To make this scheme acceptable in Canada, it is sufficient to make sure that the pulse rate is accurate to ±1 pulse per second and that the break period of 61% is accurate to ±3%. The former requirement should present no problems but the latter may need the relay to be carefully chosen. In countries that follow CCITT recommendations, the "make" time should be 33% and the "break" time 67%. The accuracy of ±1 pps and ±3% will still be adequate in most cases. The Hayes AT™ command set provides a means of selecting the make-to-break ratio. The AT&P0 command selects 39:61 for the U.S.A. and Canada and AT&P1 selects 33:67 for the U.K. and Hong Kong. Note that not all countries of the world code the decimal digits into numbers of pulses in the same way. Most countries use one pulse to represent ONE etc. with ten pulses as ZERO. Some countries reverse this with one pulse as ZERO and ten pulses as ONE. Other countries move the ZERO to the other end of the dial so that all the others move along one pulse.

The pause between the end of the last break period of one digit and the start of the first break period of the next is the interdigit time.

7.2.3.2. Tone Dialing

To dial a number using tone signaling, the controller can make use of the internal DTMF generator of K-Series modems. To set up the IC for this function, write the binary pattern $1001NNNN_2$ to the Tone Register. The ONE at bit 7 controls the RXD pin as described in section 6.4.9, Floating and Clamping the RXD Pin. "NNNN" is the binary code for the digit to be dialed. The coding is described in the data sheets and in Table 7-1. Note that digits 1 to 9 correspond with their binary values but 0 is coded as 1010. The "1" in bit 4 selects the output of the DTMF generator as the transmitted signal, overriding all other possibilities. To turn the tone on and off, the Transmit Enable bit (bit 1) in Control Register 0 must be used. After the first digit is set up in the Tone Register as above, write this bit with a ONE to turn on the transmitter output (we assume it was ZERO because nothing has been transmitted up to this point in making a call). After the desired tone duration, clear the Transmit Enable bit back to ZERO. Only then should you place the next digit in the Tone Register. After the desired pause between digits, turn on the transmitter again so that the dialing of each digit proceeds. Do not try to turn off the DTMF signals with the Transmit DTMF bit (bit 4) in the Tone Register. If you write this with ZERO, then the DTMF will indeed disappear, but a different signal will take its place. You must use the Transmit Enable bit. Also, do not change the digit code ("NNNN") in the Tone Register while Transmit Enable is ONE. The new code will take immediate effect and truncate the previous digit.

Digit	Tone Register				Tone Pair	
	D3	D2	D1	D0	Low	High
1	0	0	0	1	697	1209
2	0	0	1	0	697	1336
3	0	0	1	1	697	1477
4	0	1	0	0	770	1209
5	0	1	0	1	770	1336
6	0	1	1	0	770	1477
7	0	1	1	1	852	1209
8	1	0	0	0	852	1336
9	1	0	0	1	852	1447
0	1	0	1	0	941	1336

TABLE 7 – 1: DTMF Digit Codes

Note: In some K-Series family members, the lower bits of the Tone Register serve other purposes after tone dialing is complete. Bit 0 may select guard tone and answer tone frequencies and bit 1 may select normal or extended overspeed ranges. You must make sure that these multipurpose bits get to the desired state before the handshake begins. The "clearing up" of these bits can be done at the end of the tone dialing routine when the transmitter is turned off and the Transmit DTMF bit (bit 4) in the Tone Register is put back to ZERO.

The minimum ON and OFF times for the DTMF signal are both 50 ms. In Hayes AT™ compatible modems, "S" register S11 controls the tone dialing rate. It contains a number from 50 to 255 which defines both the ON and OFF periods of the DTMF signal in milliseconds. A popular default for this register is 95 which gives DTMF ON and OFF times of 95 ms.

7.2.3.3. Adaptive Dialing

If it is inconvenient to make the choice between pulse and tone dialing before placing the call, you can use a technique called adaptive dialing. If the line to which the modem is connected does not have tone dialing available, it nevertheless causes no harm to send DTMF tones. Therefore, when dial tone is detected, send the first digit of the number to be called by DTMF. Then wait to see if dial tone disappears. If it does, then the central office recognized the DTMF pair as a digit and you can tone dial the rest of the number. On the other hand, if dial tone persists after the first digit then the central office is not equipped to sense DTMF on this line and the number must be dialed using pulse dialing. Of course in this case, you must dial the number from the beginning, including the digit that was sent as a DTMF signal.

After the end of the transmission of the first DTMF pair, allow the call progress detection system to settle for about 100 ms before the decision to continue tone dialing is made. If, during this time, the CALL PROGRESS bit in the Detect Register goes off and stays off, tone dialing may proceed. You may wish to wait longer than this as once the decision is made to pulse dial you are going to spend many seconds in doing it. A slight delay in starting doesn't matter much if there is a chance of catching a late dial tone disappearance and using the faster method of tone dialing.

This procedure must be modified if a second dial tone appears, as in dialing through a PBX. You normally know when this is happening, however, and you can start on the second digit. In Hayes™ serial dialing commands, the "W" dial modifier causes the modem to wait for an additional dial tone. This could restart the adaptive dialing algorithm.

7.2.4. Call Progress Monitoring

Again by analogy with people using the telephone for voice calls, an intelligent modem should not simply assume that the connection will go through on the completion of dialing. After a period of silence during which the call is routed you can expect to hear the ringback signal, a busy tone or more silence. In some countries there is also a "number unobtainable" tone. By detecting these tones you can monitor the progress of our call through the network.

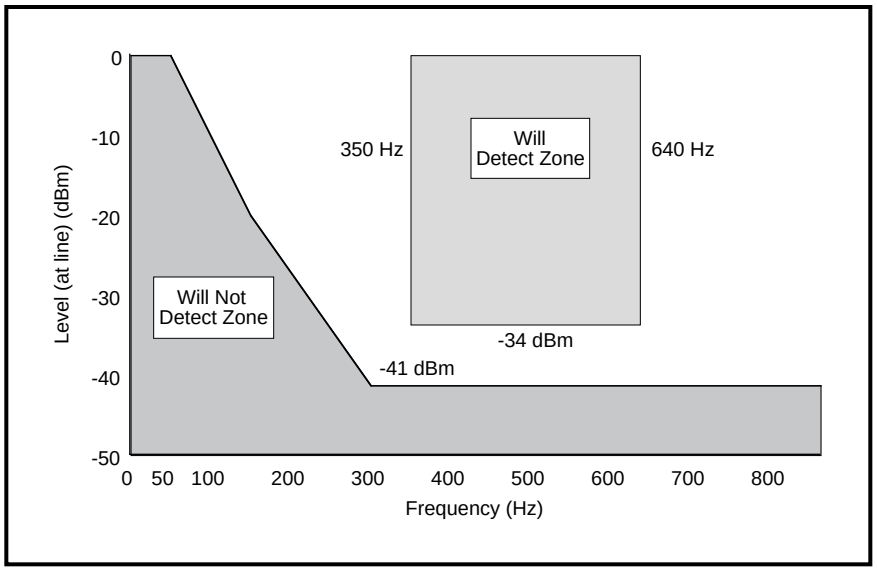


FIGURE 7 – 7: Typical K-Series Call Progress Tone Filter Template (73K222L)

The K-Series modem IC has been placed in a state suitable for call progress monitoring by the controller during dial tone detection (for DSP-based devices, this is the Call Init state selected by writing ONE to bit 5 in Control Register 2). Dial tone can be viewed as another call progress tone. After the completion of dialing, the controller should go back to watching the Call Progress bit in the detect register. However, unless you know something about the answering modem, you should make provision for detecting its answer tone or starting signal also. It may answer the call before you have seen ringback. Finally, in case you get no answer or the line is answered by something with which you can't connect (e.g., a human being), you should start an abort timer, see section 7.2.6. So, to sum up, you are looking simultaneously for ringback, busy, re-order, a signal from the answering modem and expiration of the abort timer. If you detect a ringback cycle, keep going and perhaps display a message such as the RING result code. If you detect busy or re-order, hang up and perhaps display BUSY. The system could be programmed to re-dial after a time period, but watch out for international restrictions on automatic retries. Detecting the signal from the other modem is covered in section 7.2.6. You may also choose to ride out a V.25 answer sequence in the Call Progress Monitoring phase before entering the handshake algorithm. Finally, if the abort timer expires, the calling modem should hang up.

Tone Type	Precision Frequencies	Old Signal	Cadence
Dial Tone	350 Hz & 440 Hz	600 Hz modulated with 120 Hz	Continuous
Busy Tone	480 Hz & 620 Hz		On 0.5 sec Off 0.5 sec
Reorder Tone			Period = 0.5 sec
Ring-Back	440 Hz & 480 Hz	420 Hz mw 40 Hz	On 2 sec Off 4 sec

TABLE 7 – 2: U.S.A. Call Progress Tones

7.2.4.1. International Call Progress Detection Criteria

One of the biggest problems in designing a modem for the international marketplace is call progress monitoring. Each country has installed its own network with its own standards for the signals sent by the switching offices to track call progress. Even when the signals themselves are similar from one country to another, the tests that the network administrations perform before certifying equipment for connection to the network can differ. However, the nature of the tests is fairly uniform so that it is possible to devise a set of requirements for call progress monitoring in each country. The administration usually presents the requirement as a condition under which the modem must detect the presence of a particular signal, such as busy tone, and a set of conditions under which it must not (falsely) detect that signal. There is usually a broad range of situations in which detection is neither required nor prohibited.

The requirement can be divided into two parts, the frequency band of interest and the cadences. Often, the requirements relating to frequency are similar for the various call progress tones and only the cadence is used to distinguish, say, busy tone from ringback. The frequencies are best represented as a "template" such as that shown in Figure 7-7. This represents the range of signals for which the 73K222L will definitely raise its Call Progress bit and the range for which the bit will stay ZERO. In between is the area where the bit is undefined. This template is excellent

for use in the U.S.A., but will not meet certain European requirements because of excessive sensitivity in the 150 Hz region and the absence of any real rejection of higher frequencies. Parts for international application such as the 73K322L provide high-frequency rejection and with a little support circuitry to attenuate low frequencies and adjust the threshold levels can meet most needs.

7.2.5. Transmitting the Calling Tone

The generation and detection of calling tones is explicitly supported only in K-Series parts designed specifically for international applications such as the 73K322(L). The 73K212, 221, 222 and 224L do not directly support this feature. In the international parts, select calling tone transmission by writing ?10000??1_2 to the Tone Register. Consult the device data sheets for details on specific modes that permit calling tone transmission. Bit 6 enables guard tone transmission in V.22 answer mode, but here it enables the calling tone. As usual, use Transmit Enable (bit 1 in CR0) to turn the signal on and off. Turn the tone alternately on for 0.5 to 0.7 seconds and off for 1.5 to 2 seconds as in V.25. You can optionally truncate an on period if you detect answer tone for 100 ms or more and in any case, calling tone transmission should stop when answer tone is received. V.25 is not terribly fussy about the calling tone frequency, except that it should be more than 250 Hz away from the 2100 Hz answer tone. In parts without 1300 Hz tone generators it is therefore acceptable to transmit an unmodulated FSK carrier in the low band. We would suggest a binary ONE in Bell 103 mode (1270 Hz) or, failing that, a binary ZERO in V.21 (1180 Hz). A problem with this, however, is that the 73K224L does not detect answer tones in FSK modes so you must switch to DPSK between calling tone bursts to listen for 2100 Hz.

7.2.6. Detecting Answer Tone from the Remote Modem

Ultimately you're hoping to hear something from the answering modem in response to your call. The first thing that the answering modem transmits is often referred to as the answer tone. Strictly, only the 2100 Hz tone specified in CCITT Recommendation V.25 and the 2225 Hz tone in Bell 212A are answer tones. Other signals would be better referred to as the answer modem starting signal. The range of signals that the calling modem must look for at this point will be very dependent on the application. If you have control of both ends of the call and you know that a V.22 modem without V.25 will be answering on the third ring, you can just detect a couple of ringback cycles and then wait for unscrambled binary ONES. On the other hand, if you've no idea what might be answering and when, then you may have to cover all the bases. You could find yourself looking for 2100 Hz and 2225 Hz tones, unscrambled ONES and call progress tones simultaneously.

Call progress tones have been dealt with in section 7.2.4, here we will assume that the answering modem response has been received. Qualify this signal before exiting the call initialization state to the handshake. The qualification time can conveniently be 155 ms as called for in Bell 103, V.22 and V.22bis. Both unscrambled binary ONES and answer tones can be monitored at the same time but if you want to automatically detect Bell and CCITT modems you will have to alternate between looking for 2100 Hz and 2225 Hz answer tone frequencies by toggling bit 0 of the Tone Register. Spend about 50 ms in each state to let the detector settle, but use the Carrier Detect bit to time the qualification period for accuracy. The end of the qualification may be a suitable time to raise the DSR line if you implement this in your data interface.

It is important to establish a maximum time that the calling modem will wait for a response from the answering modem, otherwise the system will hang and require operator intervention if the answering modem fails or is absent. In Hayes™ compatible modems, "S" register S7 contains the time, in seconds, that the modem will wait after completion of dialing for the answer tone or starting signal before aborting the call. When dial tone detection is enabled, this register may also be used as the wait time for dial tone after going off hook or the time to wait for ringback after dialing, which just shows how uneven command set implementations can be. The most popular default value of this register is 30 so that if nothing is heard from the answering modem for 30 seconds after dialing, the calling modem hangs up.

7.3. ANSWERING A CALL - THE ANSWER MODEM

The answer modem in a data communication session has no work to do until the line to which it is connected receives a ring signal. The modem may automatically detect this condition or may be configured to require operator action. A Hayes™ compatible modem can be placed in the auto-answer mode using the ATS0=n command to set the number of rings (n) greater than zero. ATS0=0 will disable auto-answer. A call must then be answered by entering the ATA command or pressing the TALK/DATA (or similar) button. We will assume that the controller has set up the system appropriately at power-on and that the K-Series modem IC is in its power-down state.

7.3.1. Ring Detection

In order to know that a call is coming in to a telephone line, it is necessary to detect the ringing signal placed on the line by the central office. In older telephones, the ringing signal directly activates an electromechanical bell. For that reason, the ringing signal is a fairly high A.C. voltage (about 100V RMS) of low frequency (about 20 Hz) that is superimposed on the battery voltage in bursts. The telephone separates the A.C. using a capacitor and supplies it to the bell. Modern telephones use the A.C. energy to power an electronic ringer with a speaker which emits a more high-tech sound than a bell. A modem with the capability to automatically answer an incoming call must be able to detect the presence of the ringing signal.

The design of hardware to allow ring detection is discussed in section 6.5.3.3, Designing the Ring Detection

Circuit. The output is a logic level which is examined by the microcontroller via an input port. During alternate half cycles of the A.C. ring signal, the logic level will go to the state that corresponds to the opto-isolator turning on. The switching of this input can be analyzed by the microcontroller to determine the presence of a ring signal with considerable immunity from false triggering by other signals on the line. Different national administrations require different degrees of immunity to false triggering and use different ring signal frequencies and voltages. The algorithm you use to detect the presence of ring signal will therefore depend on the countries in which you wish the system to operate, see section 6.5.11.4, International Ring Detection Requirements.

7.3.1.1. Ring Signal Cadence

The most powerful method of distinguishing a ring signal from other disturbances on the line is by its cadence. The central office places the ring signal on the line in a well defined pattern which varies from country to country. It is unlikely that signals on the line from other sources such as lighting, power line hum, etc. would emulate this cadence. To measure the cadence in the microcontroller, run timers coupled to the off-to-on transitions of the ring detector logic level output. We will call this signal RI (for ring indicator) and the off-to-on transition RI. This corresponds with the opto-isolator turning on due to the arrival of a ring signal half cycle of the appropriate polarity.

On the first RI, start timer A and timer B. Timer A is adjusted to expire in a time somewhat longer than the period of the lowest ring signal frequency we expect. Thus, during a valid ring, another RI will occur before timer A expires. Each time this happens, restart timer A but if timer B is running, leave it alone. When timer A expires, you know that the ring signal has stopped and by looking at timer B you can record the time for which it was on. Now restart timer B and let it run until the next RI. Then timer B will indicate the duration of the gap between rings. By comparing these times with predefined limits, the microcontroller decides whether or not a valid ring cycle has been received. The limits will depend on the country in which the modem is to be used.

7.3.1.2. Ring Signal Frequency

Measuring the ring signal frequency is definitely not compulsory in the U.S.A. because the FCC will not check that your ring detector works at all. Some countries set down the exact conditions under which a ring must be detected and further conditions under which it must not. Frequency is usually included. Even when not required by law, checking the ring frequency is a good idea because it allows you to discriminate against all sorts of disturbances on the network that could cause the detector circuit to be triggered.

The frequency of the ring signal can easily be estimated by measuring the time between similar transitions of the logic level from the ring detector. If cadence is being monitored as above, then you can keep a count of the number of times the ring signal goes on, off or changes state and compare it to the ring cycle duration to get the average period. In the U.S.A., you should accept frequencies in the range 15.8 to 68 Hz.

7.3.1.3. Ring Signal Amplitude

The most difficult parameter of the ring signal to validate in the microcontroller is the amplitude. If a target country has specifications in this area, then this should be taken into account in the ring detection circuit design (see section 6.5.3.3., Designing the Ring Detection Circuit). Use Zener diodes to prevent the opto-isolator from turning on until the ring signal reaches a certain peak voltage. The higher the ring signal rises above this threshold, the larger will be the part of the half cycle for which the opto-isolator is on. By measuring the on-to-off ratio of the ring detector output, you can gain extra information about the ring signal level.

7.3.2. Manual Answer

If a modem does not have the capability to detect the ringing signal, then a telephone would be connected to the same line so that it will sound its ringer on incoming calls. An operator would then hear the ring and force the modem to answer the call. Usually this is done by pressing a switch on the modem labeled TALK / DATA or something similar. This forces the modem to go off-hook and begin the answering procedure. If the telephone line is not dedicated to the modem and can be used for voice calls, the operator will answer the call normally. When he determines that the call is a data call, he first presses TALK / DATA to give the line to the modem and then hangs up the telephone handset. In this case the calling modem must be prepared for a large delay between its call being answered (ringback stops) and an answer tone being sent by the answering modem. It is very helpful for the calling modem to transmit a calling tone (see section 7.2.5., Transmitting the Calling Tone) so that the operator knows that a data call is being placed.

Modems today generally have automatic answer available and do not use manual procedures although the auto-answer feature usually can be disabled, turning the unit in effect into a manual answer modem. However, where there is a possibility of calling a manual answer modem, account must be taken of the potential long delay in answering a call. It is interesting that the default factory configuration for Hayes™ 2400 bit / s modems is manual answer (S0=0, see below), although lower speed versions were delivered set for auto-answer. This is probably so that the less sophisticated user doesn't have all his telephone calls intercepted when he first connects up the modem. Many countries specify rigorous tests for modems with automatic answering capability to ensure that they do not spuriously seize the line or otherwise interfere with network operation. If national requirements cannot be met, then the auto-answer capability can be permanently disabled and the product offered for sale as a manual answer modem.

7.3.3. Automatic Answer

If the modem is able to detect the ring signal and its automatic answer mode of operation is enabled, it will go off hook on detecting an incoming call. In the idle state of the microcontroller, examine the output of the ring detect circuit. When you see a signal that passes the criteria for ring signal (see section 7.3.1 above), record a ring cycle. Normally, a modem will not answer on the first ring but will wait until a certain number of cycles have been detected. The AT™ command set allows the user to decide how many rings the modem should detect before it answers. Put this number (n) in the "S" register S0 using the ATS0=n command. Placing n=0 here (ATS0=0) puts the modem into manual answer mode. As the modem records ring cycles, the number of ring cycles counted is available in "S" register S1 and can be examined by the operator using the ATS1? command. When enough cycles have been counted (the value in S1 matches that in S0), activate the hook relay to seize the line. It is good practice to go off-hook between ring cycles and not during a ring. Only the battery voltage is present at the relay contacts and the extra stress of the A.C. ring signal is avoided. Some countries require this restriction. When you answer the call, the K-Series Transmit Enable bit must be off (zero) so that it is not transmitting any signal to the line. You will normally have made sure of this in some initialization procedure well in advance of the incoming call.

7.3.4. Billing Delay

When the modem goes off-hook to answer a call (see section 7.2.1, Going Off-Hook), the network completes the connection between calling and answering modems. It is, however, a legal requirement in the U.S.A. and most other countries that the answering modem remain silent for a period of time to allow the network administration to send billing information between central offices. After it has gone off-hook, the answering modem must wait for the billing delay time of two seconds before sending its answer tone. The CCITT allows for a silent period of 1.8 to 2.5 seconds in the V.25 answering procedures, see below. You must therefore leave the Transmit Enable bit off for this time, but the K-Series modem IC can otherwise be readied to begin the connect handshake as an answer modem (see section 7.4., Managing the Connect Handshake).

7.3.5. V.25 Answering Procedures

The CCITT in Recommendation V.25 has put forward a standard procedure for establishing calls over the switched telephone network. It is applicable to both automatic and manual operation of both the calling and answering modem. From the point of view of the answering modem, it specifies the billing delay and proposes a 2100 Hz answer tone prior to the answering modem's normal response (the "starting signal"). The purpose of the 2100 Hz tone is to disable echo suppressors in international trunk connections. See also section 7.2.5., Transmitting the Calling Tone for the impact of V.25 on the calling modem.

If you are going to use V.25 answer procedures, the K-Series microcontroller should proceed as follows to answer a call:

1) Ensure that the K-Series modem IC is configured with Transmit Enable (bit 1 in CR0) at ZERO. At some time you must configure the chip to transmit 2100 Hz answer tone. Do this at any time before step 4 as long as the Transmit Enable bit remains ZERO. Write ?01000?1_2 to the Tone Register. Bit 5, being ONE, selects answer tone over other transmitted signals and bit 0 selects the frequency.
2) Activate the hook relay to go off-hook and seize the line.
3) Maintain silence for 1.8 to 2.5 seconds.
4) Set the Transmit Enable bit on (to ONE) to begin transmission of the 2100 Hz answer tone.
5) Hold answer tone on for 3.3±0.7 seconds. Some national administrations prefer durations towards the upper limit of this range.
6) Clear the Transmit Enable bit to ZERO to terminate the 2100 Hz answer tone.
7) Maintain silence for 75±20 ms. During this, reconfigure the K-Series modem IC to begin the answering response of the selected modulation mode. This is the response that the modem would make after the billing delay if V.25 answering procedures weren't used.
8) Set the transmitter Enable bit to ONE to begin the normal answering modem signal. For a V.22bis modem, for example, this would be Unscrambled Binary One in the high channel.

7.4. MANAGING THE CONNECT HANDSHAKE

The way in which two modems exchange signals at the establishment of a connection is vital to their operation. At this time, a modem sends signals which are characteristic of its operating modulation mode so that the other modem can work in a compatible mode. For DPSK and QAM modes, signals sent by one modem during the handshake also enable the other modem to acquire timing and carrier synchronization. If the modem incorporates an adaptive equalizer, it also uses this signal to measure and compensate for distortion of the data signals caused by the telephone line.

For modems attempting to establish a data connection using the same standard (in the same modulation mode), the handshake is well defined in the documentation of the appropriate standard. In some cases, the handshake includes the capability to sense the existence of different standards and adjust accordingly. However, modem technology has progressed in recent years faster than standards setting committees could keep up so that a number of incompatible modulation modes exist in the field. A large part of this is due to the divergence of Bell standards used in North America and CCITT standards used throughout most of the rest of the world.

Each member of the K-Series family of modem chips can operate in one or more of the common modes. Section 3.1, Selection by Modulation Standards Supported, contains tables which summarize the modes available in each part. The handshake sequence is not controlled by the K-Series modem IC itself to allow you maximum flexibility in your application. Instead, the sequence of signals must be controlled and monitored by the controller. This allows you to make your own tradeoffs in terms of supported modes, automatic mode detection, countries of operation, etc. Thus it is important to understand the handshake sequences of the various modes in order to design the controller code. This section discusses the handshakes with particular reference to the K-Series architecture. You may also want to refer to the relevant CCITT or Bell documentation.

7.4.1. Handshakes in FSK (Bell 103, 202, V.21 and V.23) Modes

FSK modulation modes do not require the modems to correct for disturbances in the telephone line or to establish timing synchronism with each other. The handshake is fairly simple and is concerned only with detecting the start of the other modem's carrier signal and allowing data into the modulator. CCITT recommendations for V.21 and V.23 do not describe how a connection should be started up at all. A procedure is described below and illustrated in Figure 7-7, but you should not rely on other modems following this. The procedure has been taken from Bell Technical Reference Publication 41214 and describes how a Bell 212A modem would work if the low-speed mode were selected. By implication, this is at least compatible with a Bell 103 modem.

When the calling (originating) FSK modem connects to the line it should remain silent after dialing until it receives a response from the answering modem. The first response may be the V.25 answering procedure, this should be ignored until signal returns after the 75 ms energy drop. In the calling modem, wait until you have received a binary ONE (marking) data signal from the answering modem for 155±50 ms. The appearance of Carrier Detect (bit 3 in DR) can be used to start the timer but poll Receive Data (bit 5 in DR) to ensure that the received signal matches the selected modulation mode. If this bit is mostly ONE, raise the data carrier detect (DCD) V.24 control signal and unclamp the RXD line by clearing bit 7 in TR to ZERO. Also, start timers of 456 ±10 ms and 765±10 ms. When the 456 ms timer expires, at point (B) in the figure, turn on the transmitter by setting bit 1 in CR0. As long as you have correctly set the modulation mode in CR0 and selected marks as the transmit pattern in CR1, the low band binary one signal will be transmitted to the answering modem. When the 765 ms timer expires at point (D), the clear-to-send (CTS) control line should be turned on and the binary one at the transmitter should be replaced with data from the TXD input by writing ZEROs to bits 6 and 7 in CR1. Data from the remote DTE has already arrived at the receiver at point (C).

After the answering modem has connected to the line and followed the billing delay or V.25 procedures, you should configure the K-Series chip for the desired mode by writing $?0110000_2$ CR0. Also select mark as the transmit pattern by writing 10_2 to bits 7 and 6 in CR1. When you enable the transmitter, the modem will send the high band tone corresponding to a binary ONE as defined by the selected standard. For Bell 212A / 103 this is 2225 Hz. Now watch Carrier Detect and Receive Data in DR and wait until you have received the binary ONE signal in the low band from the calling modem for 155±50 ms. At this point (C) in the answering modem, turn on the V.24 control lines DCD and CTS, unclamp the received data line (clear bit 7 in TR to ZERO) and send the high band signal modulated by the data arriving at the transmit data input pin (clear bits 7 and 6 in CR1 to ZERO). The DTE data from the calling

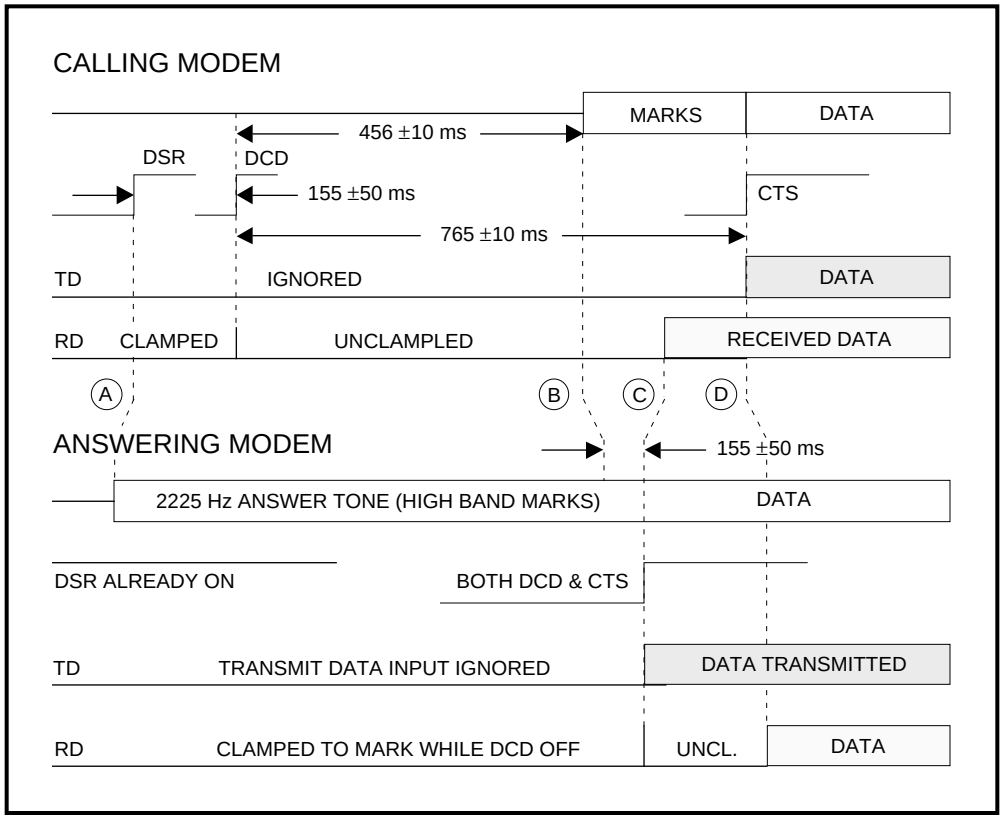


FIGURE 7 – 8: BELL 212A LOW SPEED CONNECT SEQUENCE FROM TECHNICAL PUBLICATION 41214

end will arrive at the receiver at point (D), a little after this, and the data link is complete.

7.4.2. The Connect Handshake for CCITT V.22 Modems

The CCITT publishes the recommendation for V.22 modems in one of the huge stack of books it puts out every four years. The following description of the connect handshake is based on Volume VIII - Fascicle VIII.1 of the Red Book series published in 1984. Figure 7-9 is taken from Figure 5 / V.22 in CCITT Recommendation V.22 with a few changes to make it easier to understand. For example, the time axis has been made proportional (for some reason it isn't in the Red Book) and commonly understood mnemonics are used for the V.24 interface signals instead of cryptic circuit numbers. Below, we will describe how the interface signals are manipulated, if your system does not require them, please ignore these instructions.

When we enter Figure 7-9 at the left, the calling modem has placed a call, heard ringback end (if it was listening) and is waiting to hear unscrambled binary one from the answering modem. If the V.25 answering sequence was selected, this has been detected, although it is not shown in the figure (see section 7.3.5, V.25 Answering Procedures). Set up the K-Series IC for this state by writing $000???01_2$ to CR0, $10?0?000_2$ to CR1 and $100000?1_2$ to the Tone Register. Run the routine that examines bit 4 of the Detect Register to wait for unscrambled binary ones, see section 7.1.5.1. The answering modem went off hook when it detected ringing (see section 7.3.3, Automatic Answer). The CCITT does not specify a silent period for billing protection if V.25 answering procedures are not used, however, we recommend that for U.S.A. compatibility, you keep the answering modem silent for two seconds after going off hook. Set up the K-Series IC at this end by writing $000???00_2$ to CR0, $10?1?000_2$ to CR1 and $1?0000??_2$ to the Tone Register. Set bit 6 in the Tone Register to ONE if you want to transmit a guard tone and select the 1800 Hz or 550 Hz tone with bit 0.

At point (A) in the figure, the answer modem puts DSR to the ON state and begins transmitting unscrambled binary ones. This is triggered by the end of the 75 ms pause after answer tone if V.25 was selected, otherwise the end of the two second billing delay. Write ONE to bit 1 of CR0 to enable the answer modem transmitter. The 10_2 in bits 7 and 6 and the ONE in bit 4 of CR1 (as this register was set up above) select unscrambled ONES as the transmitted signal. Also start running the routine that samples the Receive Data bit (bit 5) in the Detect Register and looks for constant ONES. The unscrambled ONES signal now propagates to the calling modem, where the Unscrambled Marks bit in the Detect Register responds. Section 7.1.5.1 describes how this bit should be qualified, note that it is different for DSP–based and non-DSP K-Series modem ICs. V.22 refers to V.25 to tell you when to put the V.24 control line DSR to the ON state. This is all very well if a V.25 sequence was received and you should put DSR ON 75 ms after the end of the 2100 Hz answer tone. However, if V.25 is not used the text of V.22 is not clear on what should be done. In Figure 7-9, V.22 offers little help but it looks as if DSR should come ON the instant unscrambled ONES is received so this is how we've drawn the figure. A more practical approach would be to put DSR ON at the end of the signal qualification, in this case after 155 ms of unscrambled ONES. At this time also, start a 456 ± 10 ms timer. When the timer expires, set bit 1 in CR0 to ONE to enable the calling modem transmitter. The signal transmitted is scrambled binary ONES because bit 4 of CR1 is ZERO, enabling the scrambler, and bits 7 and

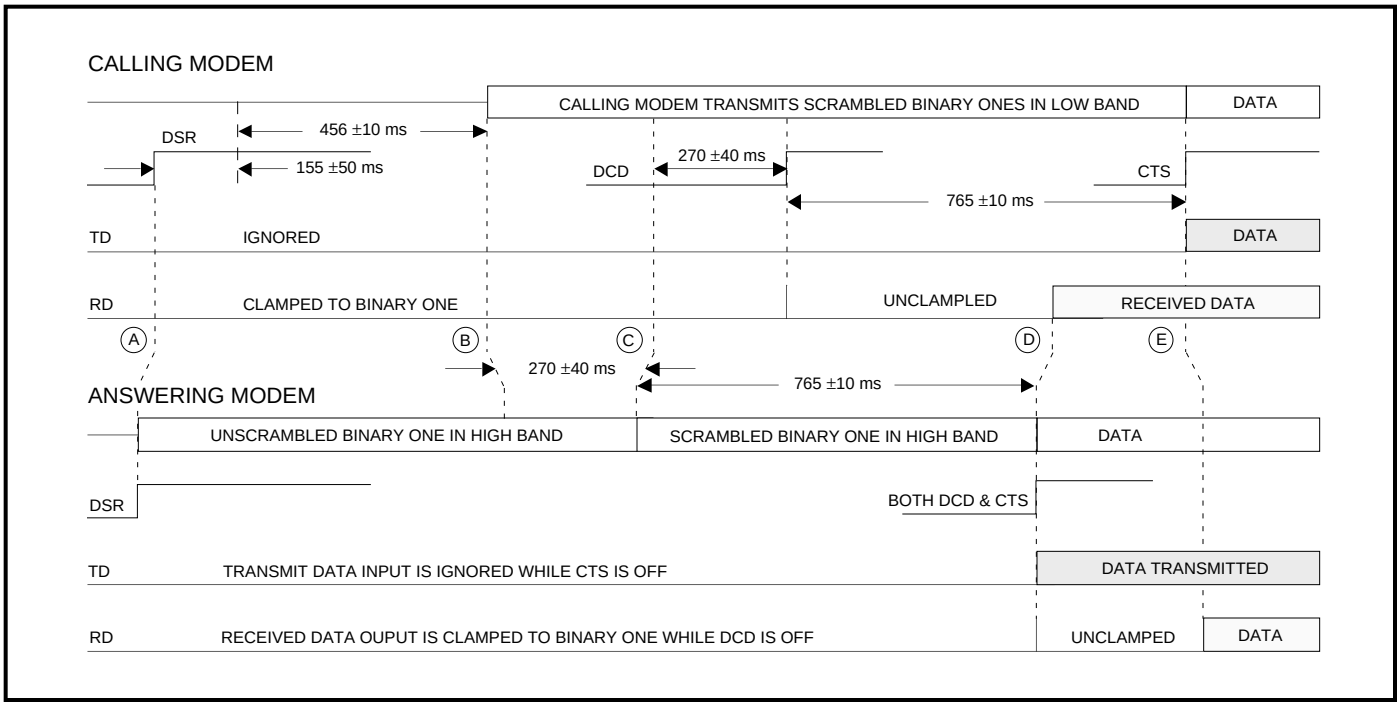


FIGURE 7 – 9: CCITT V.22 Connect Handshake Sequence

6 are 102, selecting constant binary ONES (marks) as the transmitted data pattern. Also, stop running the routine that looks for unscrambled binary ONES and instead run the routine that samples the Receive Data bit and looks for constant ones.

We are now at point (B) and the scrambled ONES signal from the calling modem propagates to the answering modem. At this end, we must detect and confirm this signal in 270 ± 40ms. The Receive Data bit in the Detect Register will typically not snap to ONE and stay there as you might expect. This is because the modem receiver has to obtain synchronization with the carrier frequency and modulation rate of the other modem before reliable data is received. In any case, on a noisy line, some bits will be in error. You can get by if you look for a period of 270 ms during which Receive Data was ONE constantly for a given period of time. It is better to use the Carrier Detect bit (bit 3) in the Detect Register in conjunction with Receive Data. Watch for Carrier Detect to go to ONE and start the 270 ms timer. If Carrier Detect goes back to ZERO for more than about 20 ms, assume that a noise pulse occurred and reset the timer. Meanwhile, if the Carrier Detect bit stays up, sample the Receive Data bit and add up the time it stays at one. Don't reset this count on single bit errors, just look for the data to be one, approximately 95% of the time. When the 270 ms counter expires, check that you've collected a healthy history of ones, say 100 ms worth, and proceed. If you don't have a preponderance of ONES at this time, the signal you're receiving is probably not from a V.22 modem. What you do then depends on the other standards with which you want to inter-operate. Assuming everything is OK, we are now at point (C) and we change the signal transmitted by the answering modem from unscrambled to scrambled binary ones. To do this, you only need to clear the Bypass Scrambler bit (bit 4) in CR1 to ZERO. Also at this time, start a 765 ± 10ms timer to tell us when to change to data transmission.

The scrambled ONES from the answering modem now propagates to the calling end. The receipt of this signal should be qualified in much the same way as at the answering modem. Since Carrier Detect is already up because of the unscrambled ones, the timer should start when the Unscrambled Marks bit in the Detect Register drops. Again, the time for which scrambled ONES should be confirmed is 270 ms (±40ms). Assuming that at the end of this time you are satisfied with the number of ONES received, it is now time to set DCD in the calling modem. This may seem a strange use of a control line called "Data Carrier Detect," but this is how the specification is written. It is common practice these days to tie DCD to the ON state all the time and ignore the specification. In Hayes™ compatible modems, the AT&Cn command allows several choices of the use of this signal. However you use DCD, the successful qualification of scrambled ONES for 270 ms is also the trigger for you to stop clamping the received data line. Clear bit 7 in the Tone Register to ZERO so that the RXD pin is driven and no longer floats to the ONE state. Finally, also at this time, start a 765 ± 10ms timer to indicate when the calling modem should change to data transmission.

The next significant event is at point (D) in the answering modem where its 765 ms timer expires. At this time, put both DCD and CTS to the ON state (but note the comments above on the use of DCD). Also release the received data line by clearing bit 7 in the Tone Register to ZERO so that RXD is driven. Finally, change the transmitted data pattern from ONES (marks) to be the data input at the TXD pin. To do this, clear bit 7 of CR1 to ZERO. The answering modem is now both transmitting and receiving user data, although the received data is still constant ones.

At last we reach point (E) where the 765 ms timer expires in the calling modem. Put CTS to the ON state and change the transmitted data pattern to the TXD data input as described above. The calling modem is now both transmitting and receiving user data and when the transmitted data propagates to the answer modem, the handshake is complete.

7.4.3. The Connect Handshake for Bell 212A Modems

AT&T originally published the specification of the Bell 212A modem in Compatibility Bulletin No. 109 (CB109). This is a difficult document to deal with because the text describing the high-speed (1200 bit / s) handshake does not agree with the diagram supposedly illustrating the same thing. Figure 7-10 is drawn for reference from Figure 2 in CB109 with a few changes to make it easier to understand. For example, the time axis has been made proportional and commonly understood mnemonics are used for the EIA232D interface signals. As you can see by comparing this with here, the order of signals is the same but the signal qualification times and delays differ. The text of CB109, however, refers to the times used in the CCITT V.22 handshake.

The Bell 212A specification was later supplemented by Technical Publication 41214, Data Set 212A Interface Specifications. This resolved the contradiction by replacing the timing diagram with a virtually unintelligible chart, but at least consistently used V.22 timings. The only residual difference is the 2225 Hz answer tone transmitted by the answering modem in place of the unscrambled binary ONES of V.22. Understanding Tech Pub 41214 is further complicated by its assumption that both modems are manually operated with a voice mode preceding the handshake. The DSR control line is clearly shown going ON 40 ms after the attendant presses the data key, but this gives no clue as to what should happen in the case of automatic operation. The following description of the connect handshake is based on Tech Pub 41214. You should read the section above on the V.22 handshake before proceeding here as we will refer back to a few things that we have already explained. We will also touch on compatibility with Bell 103. We will describe how the interface signals are manipulated, with some guesswork for DSR. If your system does not require them, please ignore these instructions.

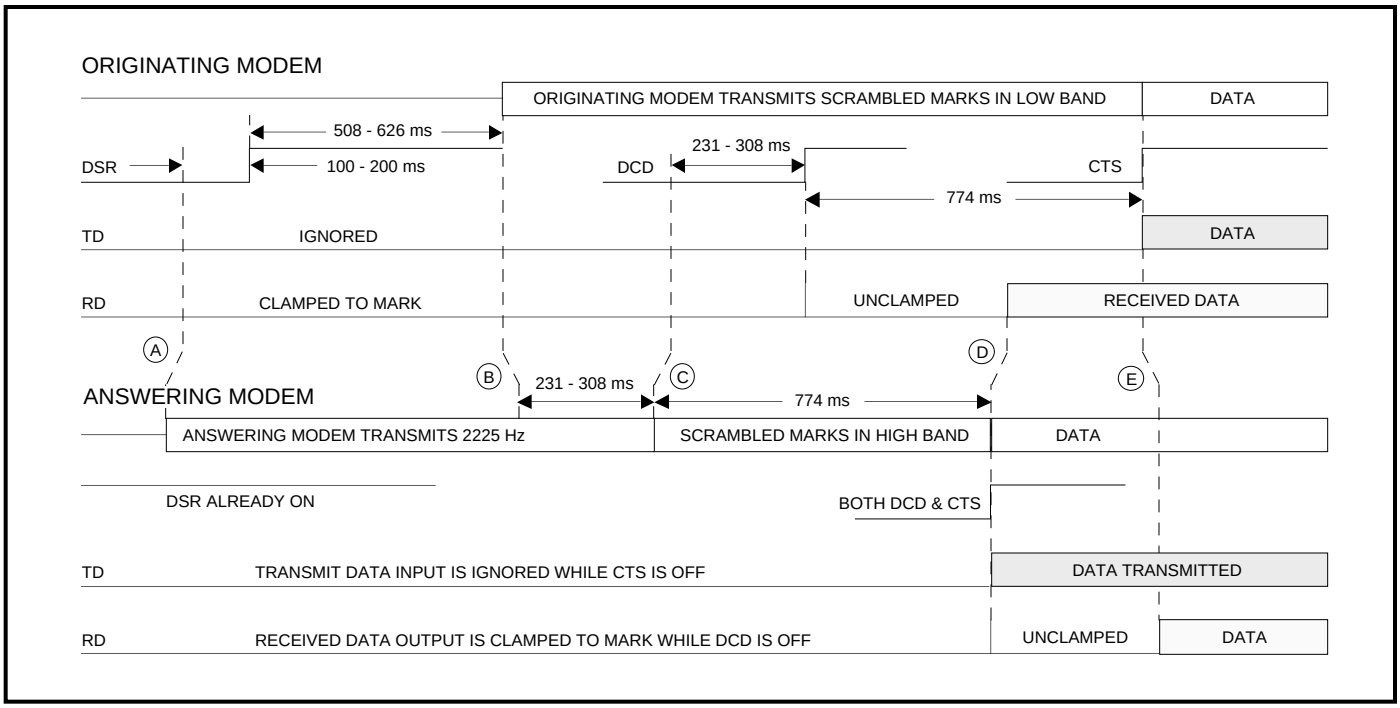


FIGURE 7 – 10: Bell 212A High Speed Connect Sequence from Diagram in CB109

When we enter at the left for a Bell 212A handshake, the calling (originating) modem has placed a call, heard ringback end (if it was listening) and is waiting to hear from the answering modem. Set up the K-Series IC for this state by writing $000???01_2$ to CR0, $10?0?000_2$ to CR1 and $100000?0_2$ to the Tone Register. Run the routine that examines bit 2 of the Detect Register to wait for a 2225 Hz answer tone. The answering modem went off hook when it detected ringing (either automatically or manually), put DSR (Data Set Ready) to the ON state and started the two second silent interval required for billing protection. Set up the K-Series IC at this end by writing $000???00_2$ to CR0, $10?0?000_2$ to CR1 and $101000?0_2$ to the Tone Register.

At point (A) in the figure, the two second delay ends and the answer modem begins transmitting the 2225 Hz tone. Write ONE to bit 1 of CR0 to enable the answer modem transmitter. The ONE in bit 5 and the ZERO in bit 0 of the Tone Register (above) select the 2225 Hz answer tone as the transmitted signal. Also start running the routine that samples the Receive Data bit (bit 5) in the Detect Register and looks for constant marks. The 2225 Hz tone now propagates to the calling modem, where, because bit 0 of the Tone Register is ZERO, the Answer Tone bit in the Detect Register responds. Examine this bit for 155 ±50ms in the calling modem to make sure that the signal is really there, then put the DSR EIA232D control line ON. Having put DSR ON, start a 456 ±10ms timer. When the timer expires, set bit 1 in CR0 to enable the calling modem transmitter. The signal transmitted is Scrambled Marks because bit 4 of CR1 is ZERO, enabling the scrambler, and bits 7 and 6 are 10_2, selecting constant marks as the transmitted data pattern. Also, stop running the routine that looks for the 2225 Hz answer tone and instead run the routine that samples the Receive Data bit and looks for constant marks.

We are now at point (B) and the scrambled marks signal from the calling modem propagates to the answering modem. At this end, confirm this signal in 270 ±40 ms. We have discussed the method of confirming the presence of scrambled marks above in the section on V.22 (7.4.2). You may wish to bear in mind that the Bell 212A answering modem is supposed to work with a Bell 103 calling modem, in which case the signal received at this time will be a 1270 Hz tone. For a full discussion of this topic, see section 7.4.4. Assuming, for our present purposes, that the signal matches our criterion for scrambled marks, we are now at point (C). Change the signal transmitted by the answering modem from 2225 Hz to scrambled marks. To do this, you only need to clear the Transmit Answer Tone bit of the Tone Register (bit 5) to ZERO. You have already set up everything else above before even turning on the transmitter. Also at this time, start a 765 ± 10 ms timer to tell you when to change to data transmission.

From point (C) on, the handshake proceeds identically with V.22, so refer back to the last few paragraphs of the previous section. The only exception is that the onset of scrambled marks at the calling modem receiver can be located by the loss of 2225 Hz rather than unscrambled ones, so you should watch the Answer Tone bit instead of the Unscrambled Marks bit.

7.4.4. Automatic Detection of Bell 103 from Bell 212A

Bell specification 212A was designed to offer a degree of compatibility with Bell 103 modems by allowing the answering modem to automatically recognize a calling modem of either type during the connect handshake. We will discuss here some strategies for implementing this process using the K-Series ICs. Please read over the preceding sections on Bell 103, V.22 and Bell 212A before starting this section.

Let us consider things from the point of view of the answering modem. After the billing delay, transmit the 2225 Hz tone to start the handshake. This tone is the same for Bell 103 and 212A modems, so the calling modem, whichever it is, will respond. Once it responds, you have about 300 ms to determine whether the response is scrambled marks from a Bell 212A modem or 1270 Hz from a Bell 103. The time limit comes from two considerations. If the calling modem is a Bell 212A, then you must detect the scrambled marks in less than 310 ms and then change the transmit signal to scrambled marks. If the calling modem is a Bell 103, then you have an absolute minimum of 289 ms after the start of the 1270 Hz marking tone before it begins sending data. You can't look for both possible received signals at once, so which should you look for first? We suggest looking for the easiest to recognize, the 1270 Hz tone from a Bell 103. If you want to perform automatic detection, therefore, configure the answer modem first as a Bell 103 and send the 2225 Hz answer tone normally. Now carefully watch the Carrier Detect bit in the Detect Register. When it becomes set, indicating the start of the calling modem's response, start a 270 ±40ms timer in case it turns out to be a Bell 212A. (Beware of noise bursts on the line, if Carrier Detect does not stay up, clear the timer and start again.) Sample the value of the Receive Data bit in the Detect Register at some suitable rate, above 300 times per second. If it settles down to be a ONE, then Bell 103 is the correct mode. Make the decision about 100 to 150 ms after Carrier Detect went active to comply with the Clear–To–Send timing of Bell 103. At the decision point, clear the Transmit Answer Tone bit in the Tone Register to allow the FSK modulator to take over the transmit signal. Because there may be a slight discontinuity in the transmitted signal at this point, hold the transmit signal at marks for about 10 ms before writing ZEROs to Transmit Pattern (bits 7 and 6) in Control Register 1. On the other hand, if Receive Data does not stay at ONE for most of the observation period, you must re-program the K-Series modem to Bell 212A mode to see if the receive signal is DPSK scrambled marks. Again, look at Receive Data (bit 5) in the Detect Register and see how well it settles to ONE, but now sample it more often because the data rate is 1200 bit / s. Make the decision to go with Bell 212A less than 310 ms after the first receipt of the calling modem response (270 ±40ms). Allowing 45 ms for the response time of carrier detection system, but otherwise taking as long as is allowed, decide when the timer reaches 260 ms after Carrier Detect was first seen at ONE. If Receive Data looks like ONE, then write to Control Registers 0 and 1 to configure the modem IC appropriately and proceed with the Bell 212A handshake. If the received data does not settle to ONE in this mode either, then give up the call or follow some recovery procedure. The simplest would be to alternate between 103 and 212A modes looking for ONEs.

A call mode Bell 212A modem, not knowing whether it is connected to another Bell 212A or a Bell 103 modem has something of a problem on its hands. Neither CB109 nor TP41214 discuss the possibility of a calling modem automatically recognizing the type of the answering modem. Either modem type, in answer mode, begins by transmitting a 2225 Hz tone, thus not giving any clue to its identity. The calling modem must detect this and about 600 ms later make its response. Should it respond as a Bell 103 or as a Bell 212A? There really is no right answer here, because you can have no idea how carefully the other modem will examine the signal to make sure that it is what it expects. We suggest responding as a Bell 212A modem, but setting a timer on the change of the answer modem signal to scrambled marks. If this change is not seen in a round trip delay plus 300 ms (about 1.5 seconds at the very outside), then switch to Bell 103. Unfortunately, a lot of garbage will have come out at the received data pin at the answering end already.

7.4.5. Compatibility Issues Between CCITT V.22 and Bell 212A Modems

It is simple to design a connect handshake that satisfies the requirements of both the CCITT and Bell specifications if you follow Tech Pub 41214 rather than CB109. Even with the timings of CB109, you can stray far enough from a strict interpretation to use the same procedure for both without ever actually failing to connect to normal implementations of either modem. Most of the timing differences are of little practical consequence, although someone could find them on close examination of the results. In the previous sections we have used common timings for V.22 and Bell 212A, leaving the only difference as the 2225 Hz answer tone vs unscrambled ONES. We will now go over the other areas in which V.22 and Bell 212A differ and suggest which route you follow for a common procedure.

V.22 specifies that the start / stop to bit-synchronous data format converter should be able to work with 9, 10 and 11 bit characters with 8 bits also optional. Bell 212A only mentions 9 and 10 bit characters. K-Series modems provide all four character lengths in both modes, you can prevent the controller from using any you don't want. While V.22 allows either increasing the intra-character bit rate or stop bit shaving as a means of squeezing the deleted stop bits back into the received data stream, Bell 212A only mentions the former. This is the method used by K-Series chips in their data format converters. The V.22 scrambler includes a function to prevent the scrambler from locking up and allowing continuous binary ONES into the modulator. The descrambler may optionally have extra circuitry to prevent a bit error from happening when the scrambler circuit steps in and flips a bit. Bell 212A does not have these features. K-Series modems have the scrambler lockup preventer in

circuit all the time, this will be of no consequence in all practical situations. Bell 212A carefully describes the termination of a data call, including the use of a long-space disconnect. V.22 doesn't address this issue, it's up to you whether you include it or not.

7.4.6. The Connect Handshake for CCITT V.22bis Modems

As for V.22, the following description of the V.22bis connect handshake, based on the 1984 Red Books, is based on Figure 5/V.22bis with a few changes to make it easier to understand. The most important change is that the durations of the various phases in the handshake have been drawn proportionally so that events appear in the order in which they will actually occur. A network transit time of 20 ms one-way has been assumed, a longer transit time may reverse the order of transmitter and receiver events in the answering modem. The connect sequence for V.22bis modems is similar to V.22 except that a special "S1" segment is introduced as an indicator of the 2400 bit/s capability and a "gear shift" occurs from 1200 bit/s to 2400 bit/s towards the end of the sequence. In this section, we assume that both modems are able to operate at 2400 bit/s, but refer also to the next section.

Starting at the left of Figure 7-11, the calling modem, as for V.22, is waiting for unscrambled binary ONE from the answering modem. However, while waiting, set it up ready to transmit the S1 signal. This signal is defined in Recommendation V.22bis as "Unscrambled double dibit 00 and 11 at 1200 bit/s for 100 ±3ms." The K-Series products supporting V.22bis can generate this signal internally and you must use this feature to ensure that the dibits are properly aligned. Do not inject a data pattern of 00110011_2 at TXD and turn off the scrambler as the 00 and 11 pairs may not be coded as dibits. Getting ready for S1 involves most of the Control Registers. Write $000???01_2$ to CR0 in the calling modem, where ??? is your choice and defines the data transfer mode. The rest of the pattern sets DPSK modulation at 1200 bit/s in call mode with the transmitter disabled. Write $01?0?000_2$ to CR1, again ? is your choice, to select the alternating transmit pattern. Note that the scrambler is enabled, but this will be overridden now by writing 00010100_2 to CR2. Bit 4 here is ONE to select the S1 transmit pattern in conjunction with the selection of the alternating transmit pattern in CR1. The scrambler is automatically bypassed. In the calling modem, run the routine that examines bit 4 of the Detect Register to wait for unscrambled binary ones.

At point (A) in the figure, the answering modem has begun transmitting unscrambled binary ONES and this signal propagates over the network to the calling modem. The routine monitoring for this signal must properly qualify it for 155 ms in the same way as for V.22, however, the tolerance on this time is ±10ms for V.22bis. The same problem exists with respect to raising the DSR line (if implemented). As for V.22, it makes sense to raise it after the qualification of unscrambled binary ONES although the figure follows the Red Book and shows it rising the instant that the signal from the answering modem is received. After the proper qualification, start the 456 ±10ms timer. When the 456 ms timer expires, turn on the transmitter by setting bit 1 in CR0 to ONE and the transmission of the S1 signal will begin. The S1 signal's duration must be 100 ±3ms, so immediately set a timer to 100 ms. At the end of this time, select constant binary ONES as the Transmit Pattern (D7=1, D6=0 in CR1) to end the S1 and begin the scrambled binary ONES signal, still at 1200 bit/s.

We are now at point (B) in the figure, an S1 segment has been sent to the answering modem to indicate that the calling modem wants to operate at 2400 bit/s. Now the calling modem must wait for the answering modem to respond by replacing its unscrambled binary ONES signal with something else. It will send back an S1 signal if it can complete the V.22bis handshake at 2400 bit/s or scrambled binary ONES if it can only operate at 1200 bit/s as in V.22. Therefore, run the routine that examines both bit 6 and bit 5 of the Detect Register in place of looking for unscrambled binary ones. We will assume that an S1 is sent, see the next section for interworking at 1200 bit/s. As described in section 7.1.5.3, the receiver routine running at this time must qualify the presence of S1 and indicate the end of the S1 segment. When the S1 segment has been received and the next signal, scrambled binary ones, replaces it at the receiver, we move on to point (C).

Now that the S1 segment has been received, it is known that the answering modem will also operate at 2400 bit/s. We have a lot to do at this time. Raise the Data Rate Selector control line in the V.24 interface (if implemented) to indicate the higher rate to the DTE. Even if your system does not use this control line, you may have some setting up to perform to establish the system data rate. Also at this time, start two timers to expire in 450 ±10ms and 600 ±10ms. The signal at the receiver is now scrambled binary ones. This is suitable for measuring the receiver input level and training the adaptive equalizer so after starting the timers, we next need to perform these functions.

Because these actions must be performed in a DSP–based K-Series modem for any QAM or DPSK mode, we have separated out the discussion of the equalizer and receiver gain boost into sections 7.4.8 and 7.4.9. Refer to these sections when you are familiar with the rest of the handshake procedure. When the 450 ms timer expires, set the receiver for 16-way decisions, i.e., receiving data at 2400 bit/s. To do this, set the 16 WAY bit (bit 3) in Control Register 2 to a ONE, the pattern here will now be 00001101_2. Although the modem IC is still transmitting data at 1200 bit/s, it is now attempting to receive data at 2400 bit/s so that it will be possible to tell when the answering modem's transmitter changes its data rate. Start running the routine to look for 32 consecutive binary ONES at 2400 bit/s by polling the Receive Data bit at a high rate.

At point (D) in the figure, the change from 1200 bit/s to 2400 bit/s scrambled binary ONES at the answering modem

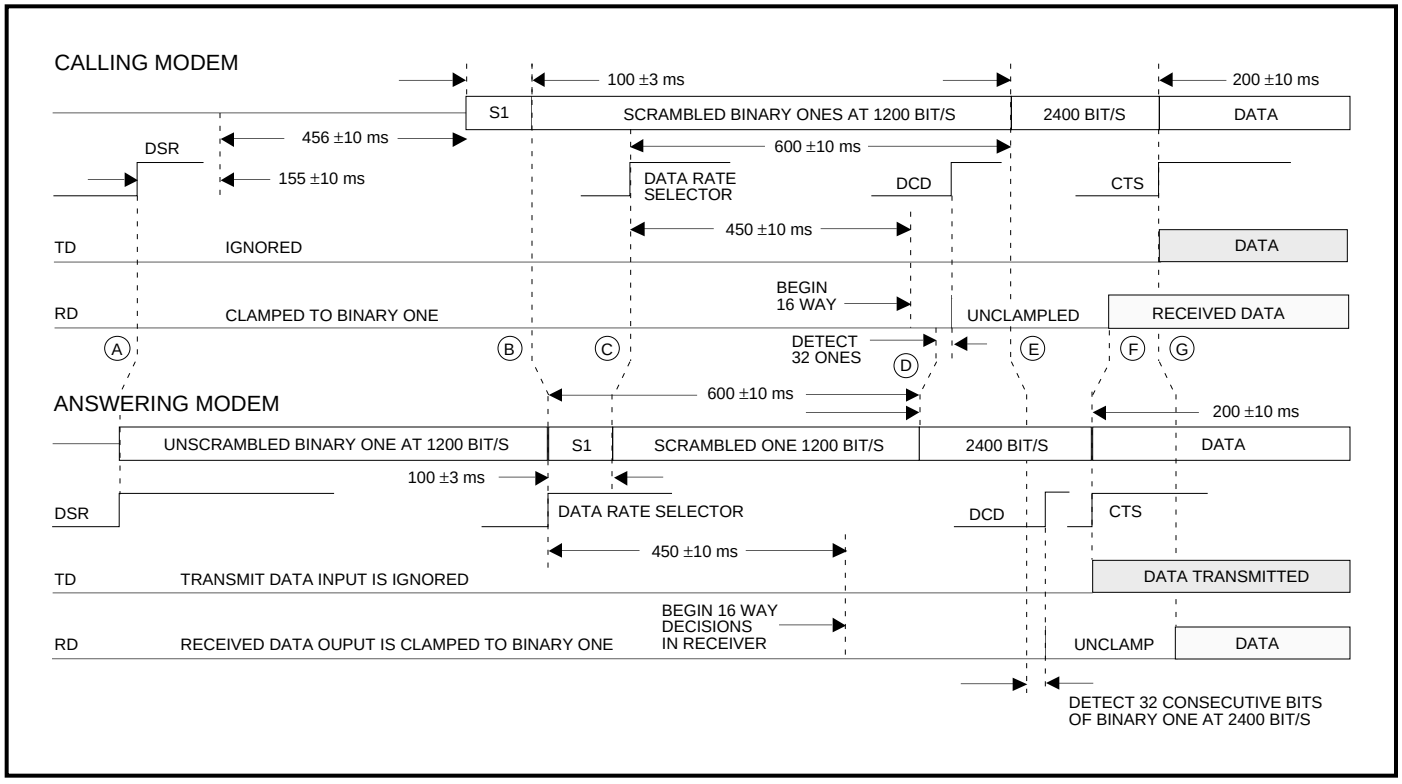


FIGURE 7 – 11: V.22bis Connect Handshake Sequence

arrives at the calling modem receiver. On receiving 32 consecutive binary ONES at this rate, unclamp the RXD output by clearing bit 7 of the Tone Register to ZERO. Also, raise the DCD control line to indicate that the data at RXD is coming from the remote modem. The RXD line should remain at binary one for almost 200 ms more, but at point (F) in the figure the data presented to the answering modem's TXD input will arrive and the handshake is complete in one direction. Referring back to the time when DCD was raised, the 600 ms timer set at the end of S1 (above) is still running. When it expires at point (E) in the figure, change the transmitter data rate to 2400 bit/s by setting bit 6 in Control Register 0. Also start a new 200 ±10ms timer here. When this last timer expires at point (G), change the transmitter from sending constant ONES to sending the data from the TXD pin by writing 00?0?000$_2$ to Control Register 1 and turn CTS ON to indicate that the modem is able to send data. When the data has propagated to the answering modem, the handshake is complete.

Now let us go back to the left of the figure and follow the progress of the answering modem. The answering modem begins the handshake at point (A), as for V.22, by transmitting unscrambled binary ONES. The next signal that it will send, however, will be the S1 signal so set up Control Register 2 as for the calling modem above with bit 4 set to ONE. Run the Pattern S1 monitoring routine to detect the S1 signal from the calling modem. If you want to interwork at 1200 bit/s with V.22 modems, the routine must also examine the Receive Data bit.

At the end of the S1 segment, we are at point (B) in the figure. All that you have to do to start the S1 response is to change the Transmit Pattern in Control Register 1 to "Alternate" (bit 7 = 0 and bit 6 = 1). However, while you're modifying CR1, enable the scrambler by clearing bit 4 to ZERO. The combination of CR2, bit 4=1 and transmitting the alternate pattern keeps the scrambler inactive in spite of this. Start the 100 ±3ms timer for the duration of S1. Also start the 450 ±10ms and 600 ±10ms timers as for the calling modem. If implemented, raise the Data Rate Selector V.24 control line and/or perform any other setting up for the system data rate. Now that the receive signal is scrambled binary ONES, you should also do something about the receiver gain boost and the adaptive equalizer. As explained above, defer looking at this until you've grasped the rest of the handshake procedure and then refer to the appropriate sections.

On the time-out of the S1 timer, at point (C), change the transmit signal to scrambled binary ONES, still at 1200 bit/s. This is done by writing to the Transmit Pattern bits in Control Register 1. When the 450 ms timer expires, set the receiver for 16 way decisions.

At point (D) in the figure, the 600 ms timer expires. Change the data rate to 2400 bit/s and start a new 200 ms timer. The first 32 consecutive binary ONES will be received at 2400 bit/s at point (E) after the transmitter has changed to 2400 bit/s. Then unclamp RXD. It may seem redundant to set the receiver to 2400 bit/s after the 450 ms timer expires, but the V.22bis recommendation says to do it and it does no harm.

The 200 ms timer expires at point (F). Change the transmitter from sending constant ONES to sending the data from the TXD pin and turn on CTS. The connection has now been established.

7.4.7. Automatic Rate Detection of V.22 from V.22bis

Above we followed the V.22bis handshake assuming that both modems were willing and able to communicate at 2400 bit/s. Here we discuss the provisions in V.22bis to inter-operate with V.22 modems at 1200 bit/s. You should include this capability unless you have control in your application over both ends of the connection and have no need for 1200 bit/s operation.

For a calling modem, everything will proceed as in up to point (B). The S1 segment has been sent, indication 2400 bit/s capability, and the answering modems response is awaited. The routine running at this time to examine the Detect Register should be looking at both Pattern S1 at bit 6 and Receive Data at bit 5. It may also be worth looking for Unscrambled Marks in bit 4 to turn off. If an S1 signal is received, the handshake proceeds as for V.22bis. If scrambled binary ONES are received, they should be qualified for 270 ±40ms and the handshake should proceed from point (C) in as for V.22.

Similarly, for an answering modem, V.22 and V.22bis are the same up to the point where the calling modem's signal is received and identified. The Detect Register routine should look for both S1 and scrambled binary ones. If an S1 signal is received, the handshake proceeds as for V.22bis. If scrambled binary ONES are received, they should be qualified for 270 ±40ms and the handshake should proceed from point (C) as for V.22. In this latter case, the answering modem does not transmit an S1 signal so that $10?0?000_2$ should be written to Control Register 1 to change from unscrambled to scrambled marks.

The only tricky part of all this is looking for S1 and scrambled marks at the same time and properly controlling the receiver gain boost and adaptive equalizer. Note that the adaptive equalizer and receiver gain boost features of DSP-based K-Series modems should be used even if the data rate is 1200 bit/s. See sections 7.4.8 and 7.4.9 for further discussion on how to program the equalizer and gain control bits.

7.4.8. Controlling the Adaptive Equalizer of 2400 bit/s Modems

Because of the large number of bits coded in each symbol of the V.22bis recommendation modem, it is important to minimize the distortion of the symbols by their passage over the telephone line. This is accomplished using an adaptive equalizer to "undo" the distortion of the line. Without this equalizer, the received symbols will be too different from those transmitted to be reliably identified with all but the very best telephone connections. The equalizer is implemented as an algorithm which processes the received signal and adjusts itself until the result is as close as possible to the known set of symbols that the transmitter can send. A Digital Signal Processor is incorporated in the K-Series modems which supports V.22bis to perform these mathematical manipulations.

For this equalization to work, the sequence of symbols being received must be fairly random. During data transmission, the scrambler makes sure that the data bits are fairly well randomized and random data gives rise to random symbols. However, during the initial handshake and at certain other times, the signals transmitted do not have this random quality. As the controller is in charge of stepping the K-Series modem through the connect handshake, it must also decide when the equalizer should start adapting itself and when it is necessary to reset it or hold the setting steady for a period. This section discusses how this is achieved.

The equalizer is controlled using two bits in Control Register 2. Bit 0 is the Equalizer Enable bit. When this bit is ZERO, the Adaptive Equalizer is placed in its initial state and held there. When it is changed to ONE, the equalizer begins to adapt to the signal it is receiving (bit 1 must be ZERO, see below). It adapts rapidly at first and then more slowly to close in on the correct setting. Clear this bit to wipe out the modem's memory of the telephone line characteristics on disconnecting a call or when a retrain is performed. Set the bit during the handshake for a new call or a retrain at the time when a scrambled signal is being received. Bit 1 of Control Register 2 is the Train Inhibit bit. When this bit is ZERO, the equalizer continuously adapts to the signal received from the telephone line (bit 0 must be ONE, see above). When it is changed to ONE, the equalizer is frozen and does not adapt but remembers things as they were when the bit was last ZERO. You will most probably keep this bit at ZERO all of the time. However there are special applications in which it might be useful to set it to ONE and freeze the equalizer, see below. Note that for the equalizer to work, the DSP must be running in the non-Call Init mode. This means that (bit 2) must be ONE and Call Init (bit 5) must be ZERO in Control Register 2. We mention this here for completeness, but you will have to get the DSP into this state long before it is time to mess with the equalizer. Note also that a reset operation on the entire K-Series IC, either using the RESET input pin or the Reset bit in Control Register 1, clears all Control Register and Tone Register bits to ZERO except that bit 2 in Control Register 3 is set to ONE.

7.4.8.1. Turning On the Equalizer in the Connect Handshake

The rule for starting up the equalizer in DPSK and QAM modes is very simple. Equalizer Enable should be set to ONE as soon as the received signal is scrambled binary ones. Whether the modem is heading for a V.22, V.22bis or Bell 212A connection, this is the first signal received that is suitable for training the equalizer. Furthermore, having got this far, you can leave the equalizer enabled into the data mode unless something goes wrong. Before going on to discuss how to find this point, we should repeat that

Equalizer Enable should be ZERO when beginning a connect handshake. Also, the equalizer does nothing for FSK modulation modes, so leave this bit alone, or, if you change your mind after setting it, clear it back to ZERO again.

The calling modem will at first receive unscrambled binary ONES or 2225 Hz answer tone from the answer modem. This is indicated in the Detect Register. The calling modem then sends out an S1 signal (or scrambled binary ONES if set for 1200 bit / s) and in response to this the answer modem will change its transmit signal to either scrambled binary ONES or the S1 signal. No detector is provided for scrambled ONES. In fact, the modem can't reliably tell that they're scrambled ONES until the equalizer is trained. Therefore, we suggest that you set Equalizer Enable when the Unscrambled Binary ONES or 2225 Hz answer tone detectors go back to ZERO. This is the right thing to do unless the S1 signal is being received. You need to know this anyway and can tell by looking at Pattern S1 (bit 6) in the Detect Register. If, after properly qualifying this bit for a period of time, (we recommend 50 ms, see section 7.1.5.3) it is apparent that S1 is being received, then clear Equalizer Enable back to ZERO and the equalizer will be back in its initialized state. When the S1 signal ends, according to our careful examination of Pattern S1, this is now the time to set Equalizer Enable again. If you rely on the duration of the received S1 signal being 100 ms and have qualified it for 50 ms, you could alternatively set Equalizer Enable 50 ms after the completion of qualification.

Follow a similar procedure in the answering modem. Instead of waiting for the end of the unscrambled ONES or 2225 Hz, wait here for the first signal received from the calling modem. This will be indicated by the Carrier Detect bit (bit 3) in the Detect Register. Again this signal will be either scrambled ONES or S1. If you turn on the equalizer in any case, you can correct your error if you find that it is S1 by turning it off and then on again at the end of S1 as described above.

7.4.8.2. Restarting the Equalizer for a Retrain

Retraining can be used in a 2400 bit / s data connection to restore a low data error rate after a disruption. When the controller of either modem suspects that the adaptive equalizer has lost its ability to correct the distortion of the received signal, it may initiate a retrain. The retrain inserts a period during which the variety of symbols transmitted is reduced from sixteen (2400 bit / s) to four (1200 bit / s) so that the equalizer can get back on track. For a full discussion of this process, refer to section 7.5.2, Retraining.

In the modem that decides to perform the retrain, the Equalizer Enable bit can be cleared immediately to initialize the equalizer. This modem (the initiating modem) then sends an S1 signal and waits for the responding modem to send one back. The responding modem follows its S1 with about 500 ms of scrambled binary ONES at 1200 bit / s. The initiating modem therefore should set Equalizer Enable when it detects the end of the S1 signal at its receiver (by qualification of the Pattern S1 bit in the Detect Register). Usually, the first thing the responding modem knows about the need for a retrain is that the routine monitoring Pattern S1 indicates that an S1 signal is being received (although you should ensure that the possibility of both modems deciding to initiate a retrain at the same time is catered for). When you are sure that a true S1 signal is being received, then you can clear Equalizer Enable. Again, just wait until the end of the S1 signal is detected and then turn it back on. The Equalizer Enable bit must be ZERO for about 2 ms to be effective in initializing the equalizer.

7.4.8.3. Freezing the Equalizer

During a data call on the switched telephone network, a lot of things can happen which temporarily disrupt data flow. The most obvious are a short break in the continuity of the line or a sudden burst of noise. A well designed modem will make errors during such a catastrophic event, but will quickly recover and restore reliable data transmission when the event has passed. The K-Series modems which have adaptive equalizers automatically freeze their settings when a catastrophe is detected. When everything is back to normal, the equalizer is unfrozen and since the characteristics of the line will be unchanged, the modem will very quickly pick up correct data again. If the equalizer were allowed to adapt during a gross disturbance on the line, its setting would drift away from the correct one. In this case, even after the disturbance has passed, the receiver would continue to make errors and a retrain would be necessary. You should not use the Train Inhibit bit in an attempt to freeze the equalizer during disruptions. The internal DSP is better equipped to decide when this should be done.

Some applications of the Train Inhibit capability are to turn off the equalizer adaptation if you know that the line characteristics are not going to change for some period of time. The process of adaptation itself introduces a small amount of noise into the data as the algorithm calculates new values for the tap coefficients. Performance can be marginally improved if the equalizer is frozen when adaptation is not needed. You could do this, for example, on a leased telephone line of known stability after a few seconds of data have passed. Also, you can freeze the equalizer to "remember" the line characteristics if you want to turn off the signal for some reason. This can happen in controlled carrier systems where the signal is turned on and off to convey signalling information between the DTEs. The use of the equalizer when the modem's first handshake ensures optimum performance over any connection but freezing the equalizer allows it to hold the line characteristics when the signal at the receiver is absent.

7.4.9. Using the Receiver Gain Boost of 2400 bit/s Modems

K-Series modem ICs with 2400 bit/s capability use Digital Signal Processing techniques to implement a receiver with the necessary immunity to channel distortion. The received signal must therefore be converted from analog to digital form via an on-chip A-to-D converter. To avoid loss of dynamic range and poor performance at low signal levels, the receiver gain can be boosted by 12 dB, (18 dB for 73K324L) before the converter. The 12 dB boost is out of circuit on power-up and at any time that the Receive Gain Boost bit (bit 4) of Control Register 3 is ZERO. It is placed in circuit by setting this bit to ONE. The controller is responsible for the decision whether to use the extra gain or not, based on its examination of the Receive Level bit (bit 7) in the Detect Register, and also the timing of the gain boost.

The Receive Level bit incorporates approximately 2 dB of hysteresis and is well filtered so that it will not tend to bounce around even if the receive level is close to the threshold of approximately -21 dBm (-25 dBm for 73K324L) at the line. However, you should examine it at a time when transients due to any mode changes have settled out and a steady signal, typical of the data signal, is present at the receiver input. Fortunately, it settles out more quickly than most of the other detectors so that by the time a suitable signal is sensed, this bit is ready to be examined. We recommend that you test the Receive Level bit once only when scrambled binary ONES are being received and before turning on the adaptive equalizer. If the Receive Level bit is a ONE, then the receive level is above the threshold so don't use the receiver gain boost. If the bit is ZERO, then the signal is below the threshold and you can insert the extra gain in the internal receiver circuitry by setting bit 4 of Control Register 3 to ONE. Unfortunately, the sense of the Receive Level bit was shown reversed in early data sheets of the 73K224L, check that your data sheet is correct as described above.

7.5. MONITORING THE CONNECTION

One of your primary concerns in the design of the firmware for the microcontroller will probably be "What must the controller do with the K-Series modem IC during normal data transmission?" It would be nice to answer "nothing," as the controller could then devote its energies to something else. Of course, if there is nothing much else to do, you don't have to worry. On the other hand, if the controller is also performing buffering, error control or compression on the data, for example, you will want to minimize the time that it has to spend checking up on the modem. This section discusses the things that the controller may have to keep an eye on once the connection has been made and data is flowing.

7.5.1. Signal Quality

K-Series modems which use DSP techniques are able to estimate the likelihood of errors in the received data. At the time of writing, this feature is only available in the 73K224L. Bit 0 in the Detect Register is the Signal Quality bit. The "Long Loop" bit takes the place of Signal Quality in other non-DSP-based parts. The Signal Quality bit will be ZERO during a good or average connection. When there are disturbances on the telephone line such that the received data error rate is likely to be high, this bit will toggle with a period of about 1.67 ms. If the disturbance is of such a high level that the received data is not worth having, then the Signal Quality bit will go to ONE and stay there. Table 7-3 shows the relationship between the activity of the Signal Quality bit and the signal-to-noise level on a number of simulated telephone lines for the 73K224L. The receive level in the tests used to compile this table was -20 dBm. A signal–to–noise ratio of 16 dB corresponds to a bit error rate of about 10-5, which is tolerable if error control is in use. A signal-to-noise ratio of 10 dB corresponds to a bit error rate of 10-2, which is too high to be useful.

Of course, the signal quality is only of concern if you have something you want to do with the information. Some standalone modems have a signal quality indicator on the front panel so that the operator can tell whether to expect a high error rate or not. If, after a period of acceptable reception, the signal quality takes a dive and stays poor, it may be a good idea to initiate a retrain, see section 7.5.2. If this doesn't fix the problem, then you might consider having the modem disconnect the call and dial a new connection. When modem standards are available that specify fallback and fallforward procedures, a persistently poor signal quality will be a primary reason for performing fallback.

Mode	Line	Toggle	One
Call (receive in high band)	Flat	19 dB	9 dB
	C2	22 dB	11 dB
	C1	23 dB	12 dB
	3002	23 dB	10 dB
Answer (receive in low band)	Flat	19 dB	10 dB
	C2	21 dB	10 dB
	C1	21 dB	11 dB
	3002	23 dB	10 dB

TABLE 7 – 3: Signal Quality Indications vs. Signal–to–Noise Ratio for various test lines with SQI set for the default (00) level in the special register (bits D2, D1)

7.5.2. Retraining

Of the modulation standards currently supported by K-Series modems, only V.22bis defines a retrain procedure. As explained below, the DPSK modes, such as V.22 and Bell 212, use sufficiently simple signals that the receiver can recover from loss of synchronization without special effort. If you are not interested in V.22bis operation, please skip over the rest of this section.

In DPSK or QAM modulation modes, bursts of interference on the telephone line or interruptions in the signal can frequently make a modem's receiver loose

synchronism with the data signal. FSK modems will make errors in the received data in these situations, but the errors will stop when the interference level drops. With synchronous modulation, however, the receiver must recover the exact carrier frequency and data rate of the transmitting modem and may use an equalizer to correct other distortions. At 1200 bit/s, the transmitter uses only one of four symbols to convey two bits of data in each symbol time (2 bits times the symbol rate of 600 baud equals 1200 bit/s). With such a simple variety of symbols,or constellation, the equalizer can quickly get back on track and a retrain is not needed. However, at 2400 bit/s, one of 16 symbols is transmitted to send four bits of data in each symbol period. Over most telephone lines, these symbols are too close to each other in appearance at the receiver for the equalizer to adjust itself when it has lost track of the approximately correct position. During a retrain, a part of the initial connect handshake is repeated so that the receivers can go back over the procedure they used to originally obtain synchronism. The exact function of a retrain is to insert a period during which only one of four symbols are transmitted so that the equalizer can get back on track. The passage of useful data is, of course, disrupted. After reading this section, refer also to section 7.4.8.2, Restarting the Equalizer for a Retrain.

Retraining in a V.22bis modem must be considered from three angles. First, how do you decide to do a retrain, then what do you do to make it happen and finally, what do you do if the other modem is the one to start things off. An operator may decide to perform a retrain if he notices that the error rate has become suddenly worse. A switch may be provided on the front panel of the modem or he may enter a command at the terminal. In Hayes AT™ compatible 2400 bit/s modems, you can escape to the command mode and enter ATO1 to return to the data mode with an equalizer retrain. An automatic retrain may be initiated when the controller firmware suspects that the adaptive equalizer has lost its ability to correct the distortion of the received signal. Some modems use an extension of the Hayes AT™ command set to enable or disable the controller's ability to automatically start retrains. The "auto-retrain" decision is usually based on Signal Quality, see section 7.5.1, although other means of detecting high error rates may be used. If the retrain fails to improve the error rate, the controller may try several times, but ultimately if things stay bad the only recourse is to disconnect and dial again.

The sequence of signals exchanged by V.22bis modems during a retrain is very similar indeed to the initial connect handshake already described. The modem requesting the retrain behaves as the calling modem, starting with the transmission of the S1 signal. The modem responding to the request behaves as the answering modem, again starting by transmitting S1 in response to the end of this signal at its receiver. A diagram of the sequence is shown in Figure 7-11. This is again drawn from the CCITT Red Book, but the time axis has been made proportional so that you can see the order of events more easily. Not shown is the fact that the DSR, DCD and Data Rate Selector control lines, if implemented, remain ON throughout the retrain. In the description below, we will refer you back to the description of the initial handshake to avoid repetition. You can design your code to merge at the appropriate point also.

At (A) in the figure, the requesting V.22bis modem begins the procedure of retraining the data link. It turns OFF CTS, clamps its received data line to binary one, and sends a 100 ±3ms period of the S1 signal. To do this, set bit 7 of TR to one (floats RXD), set bit 4 of CR2 to one (select S1 instead of reversals), clear bit 6 of CR0 to ZERO (data rate = 1200 bit/s) and write 01_2 to bits 7 and 6 of CR1 (select transmit pattern). Also start the 100 ms timer. On time-out of the timer for the S1 signal at point (B), change the transmitter to send scrambled binary ones, still at 1200 bit/s. To do this, write 10_2 to bits 7 and 6 of CR1 (select transmit pattern as marks). Having reached this point, the requesting modem must wait for the other modem to respond with an S1 signal. Begin running the routine that looks for S1 but don't accept scrambled binary ONES as you did for V.22 fallback in the initial handshake. It is also a good idea to start an abort timer at this point in case the other modem does not support retraining. If the S1 signal is returned, the other modem will cooperate. This is an excellent time to force the adaptive equalizer to its initial state and to turn off 16-way slicing so write 00000100_2 to CR2. If S1 is not received before the abort timer expires, you could go back to normal data transmission or hang up. As soon as the S1 qualification routine indicates the end of the signal we are at point (C) in the figure. From here, proceed as a calling modem in the initial handshake by starting timers of 450 ms for the receiver gear shift and 600 ms for the transmitter gear shift.

In order to tell that the remote modem wants to perform a retrain, the controller must be able to detect that an S1 pattern has been received. Section 7.1.5.1 discusses how this should be done, the routine that performs this function will have to be run at all times during the data transfer state in V.22bis mode. If the routine indicates that an S1 signal was received and has ended, then a retrain should be started. Remember that the K-Series S1 detector will be triggered for short periods of time by the normal data spectrum, so it is most important to properly qualify this bit to avoid spurious retrains.

At (B) in the figure, the end of the S1 signal has been indicated by the qualification routine and data transmission is rudely cut off for the retrain. In exactly the same way as for the initiating modem, the responding modem turns OFF CTS, clamps its received data line to binary one, and sends a 100 ±3ms period of the S1 signal. The register manipulations have been described above. In addition to the 100 ms S1 timer, 450 ms and 600 ms timers should be started for the receiver and transmitter gear shifts. The time to write to CR2 to initialize the equalizer and turn off 16-way slicing in the responding modem is also during or at the end of S1 (remember to turn the equalizer back on again, but not sooner than 2 ms after clearing bit 0 in CR2).

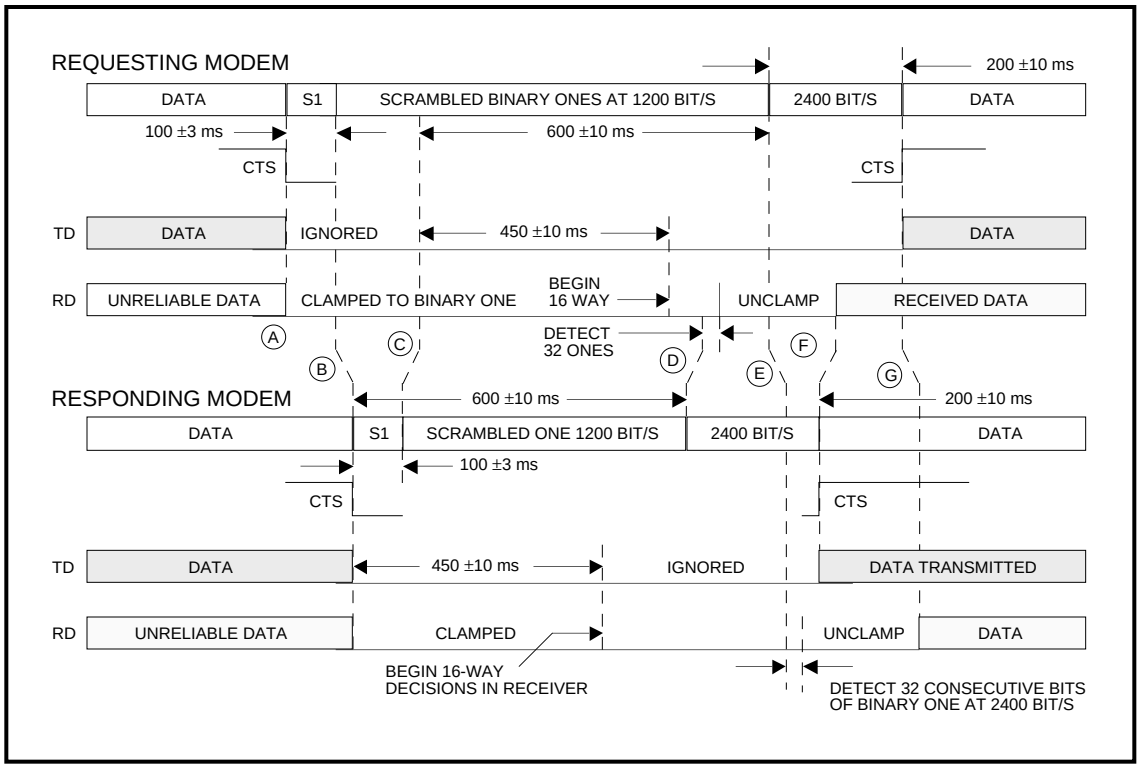


FIGURE 7 – 12: V.22bis Retrain Sequence

Change the transmitter to scrambled binary ONES, still at 1200 bit/s and everything proceeds as for the answering modem in the initial handshake.

7.5.3. Fallback and Fallforward

There is a proposed enhancement to CCITT Recommendation V.22bis which would allow a conforming modem to change data rate during a connection. Because this enhancement has not been approved by the CCITT at this time, we cannot tell you if fallback and fallforward can be supported by the existing K-Series modems.

7.5.4. Call Termination by Long Space Disconnect

If it is desired to implement the long space disconnect feature, see section 7.7.2, Long Space Disconnect, the controller must be able to tell when continuous zeros have been received for 1.6 seconds.

7.6. ESTABLISHING TEST MODES

We have so far discussed how to control the K-Series modem IC in the normal process of exchanging data between two modems. There are also several modes of operation available the purpose of which is not to exchange data but to make sure that the system is operating correctly. You may want to add these test modes to your product as automatic power-up tests or operator selectable diagnostics. Local loopbacks test your system's internal workings and are easy to perform automatically or on demand. The remote loopback tests your system, much of the remote system and also the connection over the telephone line. As a data connection must be established before starting the test, it is more difficult to perform automatically.

7.6.1. Local Digital Loopback

In a Local Digital Loopback test (CCITT V.54 Loop 1), the data sent to the modem to be transmitted is also sent back to the data source on the received data wire. This is not a very useful test, but it can allow you to make sure that your data is getting as far as the modem IC if some other test makes you suspect that it isn't. To put a K-Series part into this mode, simply write 11_2 to the Test Mode bits (bits 0 and 1) in Control Register 1. Whatever you apply to the TXD pin will now be sent back to you at the RXD pin. This is done with a multiplexer just inside the chip so the RXD pin will follow the TXD pin exactly, very little circuitry intervenes. It doesn't matter what else is going on in the modem at this time, whether the transmitter is on or off, etc., but if a full–duplex call is in progress you will, of course, lose your received data.

Hayes AT™ compatible modems can initiate a digital loopback in response to the AT&T3 command. Note, however, that this is generally not implemented as a Local Digital Loopback as defined by CCITT V.54 loop 1 and discussed above. It is rather used to set up a loop 2 type test (Remote Digital Loopback) from the looping modem, in other words the one from which the test is not normally controlled. This facility is useful if you choose not to monitor for automatic RDL requests or if the other modem is unable to issue them.

7.6.2. Local Analog Loopback

A more useful internal system test is the Local Analog Loopback test (CCITT V.54 Loop 3). Here, the modem transmitter operates normally, but the receiver, instead of looking at the alternate frequency band for the remote modem's signal, looks at the signal from its own transmitter. With this test, you can check the operation of the system up to the telephone line interface. The Hayes AT™ command set provides for Local Analog Loopback with the AT&T1 command. This test should be launched from the idle state in the K-Series modem, not during an existing call. There is no need to go off-hook. If you want to perform this test and you are already off-hook, you should go back on-hook first. Follow more or less the same procedure as you would to make a normal call, but when it is time to set the Transmit Enable bit, leave it off and instead write 01 to the Test Mode bits. The test can be made in either the high or low band according to the setting of Answer/Originate (bit 0) in Control Register 0. If this bit is ZERO, selecting answer mode, the test is made in the high band. If it is ONE, call mode, the test is in the low band. In either case, it is easier to re-use the normal connect handshake sequence if the transmitter behaves as a calling modem and the receiver follows the logic of an answering modem. Note that the receiver will have to detect the S1 signal at the same time that the transmitter is sending it. This is not very likely in normal operation, but must be allowed for here. As an alternative to the normal connect handshake, you may devise your own procedure, since there is no need to accommodate an unknown remote modem. A shorter sequence is possible, omitting S1 even for a 2400 bit/s connection, but you may reason that the test is most effective if it uses as much of the normal procedure and logic as possible.

7.6.3. Remote Digital Loopback

Remote Digital Loopback (CCITT V.54 Loop 2 or "RDL") is by far the most sophisticated and comprehensive test that can be applied to a normal dial-line modem. Once established, it makes apparent any problem in either the local or remote modem and the connection between them. The data input to the local modem is sent to the remote modem where it is received and decoded normally. Instead of sending this data to the remote user, the modem re–modulates it and sends it back down the telephone line to the local modem. Thus, at the local modem, any difference between what is received and what was sent is an immediate sign of a problem somewhere. The local modem can also send a test pattern and monitor the returned data for deviations in order to measure the error rate in both directions at once. FSK modulation standards such as Bell 103, V.21 and V.23 do not specify a method for establishing RDL, so this section does not apply. In fact, this section only applies to Bell 212A, V.22 and V.22bis because their loop 2 procedure is unique and is described as part of the standard. Other synchronous modulation standards generally follow CCITT Recommendation V.54 for establishing loop 2, but since the K–Series products available at the time of writing do not work this way, we will not cover this.

A Hayes AT™ compatible modem provides commands for controlling Remote Digital Loopback tests. A call must be requested and successfully established using the normal dial and answer commands before an RDL test can be contemplated. Then, in order to regain control of the modem, the DTE must issue the escape sequence, normally "+++." Once in command mode, an RDL test can be initiated with the AT&T6 command. For the test to work, the other modem must cooperate. If it has not been designed to support RDL, then your test will fail and you will get a report to this effect. Even if the other modem does support RDL, its response may have been turned off with an AT&T5 command entered by its operator during configuration. It can be turned back on by the AT&T4 command, but, of course, only at its DTE, not yours. The AT&T0 command (or just AT&T) terminates all tests, including RDL.

We will now look at the method of establishing an RDL test to see what action the microcontroller must take in controlling the K-Series part. The sequence of signals transmitted and received is specified as part of the CCITT and Bell standards.

7.6.3.1. Establish a Normal Data Connection First

It is important to realize that a connection must already exist between the two modems before an attempt is made to start an RDL test. The two must handshake normally and be exchanging data at a reasonably low error rate. Thus, RDL cannot be used to diagnose a situation in which the modems fail to synchronize or have error rates so high that the data is unrecognizable. Do not engage any other test mode before an RDL test, neither modem should be in analog loopback or local digital loopback.

In the following discussion, we will refer to the unit initiating the RDL test as "modem A" and the other unit as "modem B." In a typical situation, an operator takes control of modem A during a data connection and by entering a command or pressing a switch starts the process of establishing RDL. Modem B is unattended at a remote site and completes its part of the process without operator intervention. It could be that the operator of modem A is using this procedure to test modem B. The test cannot work if modem B has not been designed to automatically enter into an RDL test or has been disabled from doing so. In this latter case, an operator at modem B will have to ensure that this facility is enabled before the operator of modem A begins the test.

7.6.3.2. Summary of the Signals Exchanged Between the Modems

To set the scene, we will first step back from either modem and see what goes on as a whole. Refer to Figure 7-14, which shows the timing of signals exchanged between the initiating and responding modems. At point (A), the

instruction to initiate an RDL test takes effect. Modem A stops accepting user data for transmission and instead transmits unscrambled binary ones. This is called the initiation signal. Without the scrambler, the continuous ONES are modulated as a constant shift of the carrier and, if an audio monitor is connected, you can hear a tone replace the normal hiss of the scrambled data signal. Modem B detects this signal and at point (B), if it is allowed to enter into RDL tests, will also stop accepting data and will instead transmit the acknowledgement signal of alternating ONES and zeros (reversals). This is just what modem A is waiting for and having received this at point (C), modem A changes its transmitted signal to scrambled binary ones. Modem B, in turn, is waiting for the initiation signal to go away. This happens when the scrambled ONES arrive and at (D) Modem B begins "looping back" its received data to its transmitter. Modem A's scrambled ONES therefore replace the reversals as modem B's transmit signal and when modem A receives this it knows that the RDL is established. At point (E) it accepts user data again. This data will be sent to modem B which will loop it back to modem A so that after the "round trip delay" modem A's receiver will repeat what went into the transmitter.

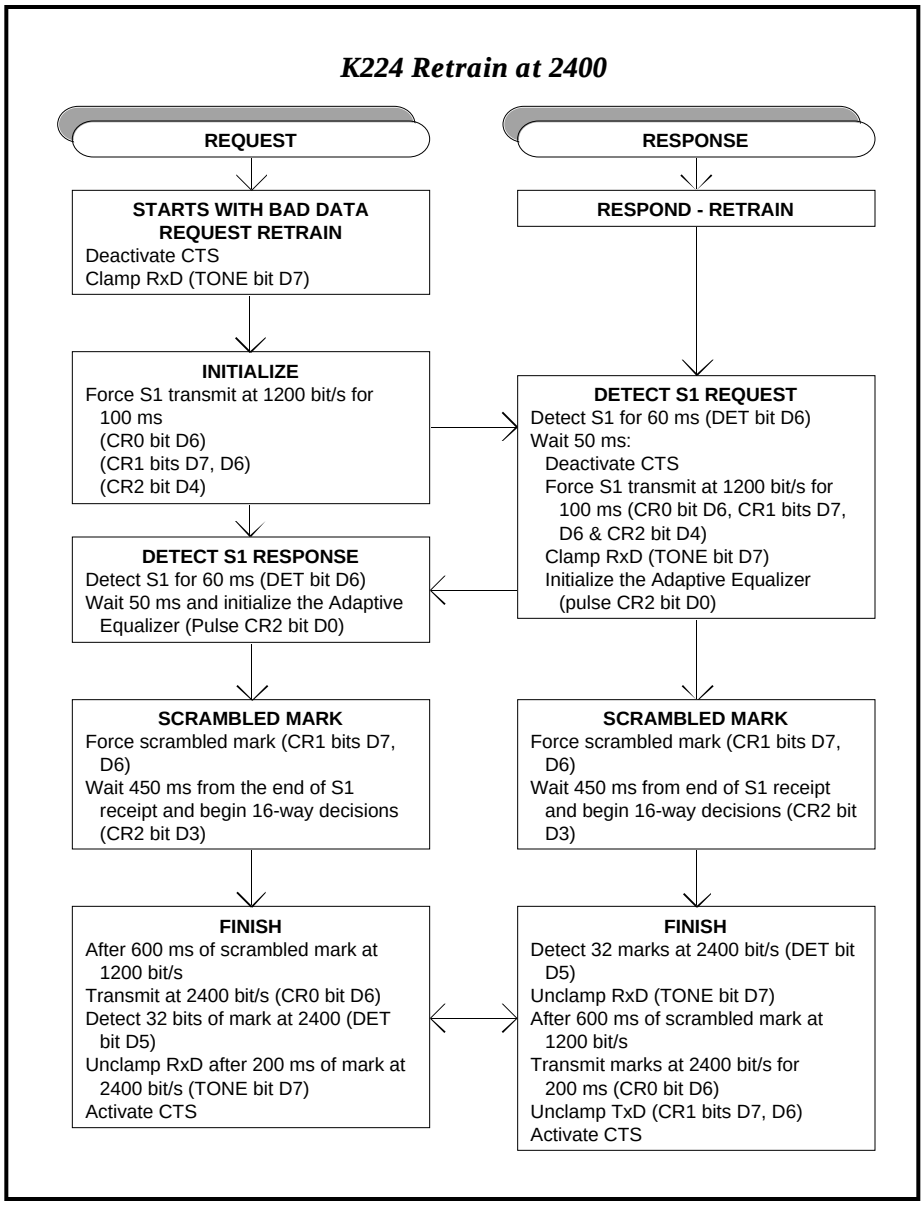


FIGURE 7 – 13: Flow-Chart for V.22bis Retrain

When modem A is instructed to end the RDL test, it briefly quiets its transmitter at point (F). Modem B detects the loss of signal at the receiver and its reappearance a short time later. It terminates the test at point (G) by reverting to passing received data to the user and accepting user data for transmission.

The figure shows the V.24 control lines CTS, DSR, DCD and TI being used in accordance with CCITT V.54. Both V.22 and V.22bis defer to this Recommendation in this regard, although since the initiation and termination handshake is different from V.54, some licence must be used in its interpretation. In outline, the responding modem places itself out of service as far as its DTE is concerned as soon as it recognizes the initiation signal. It does this by putting DSR, CTS and DCD to the OFF state. These signals return to their normal function when the test is over and normal data flow resumes. The initiating modem keeps DSR and DCD ON throughout the test, but lowers CTS from the time it starts the initiation signal to the time it begins transmitting test data from the normal data input. TI (test indicator) is ON from the time that CTS is put back ON to the end of the terminating signal drop. While CTS is OFF, in either modem, the received data is ignored and RXD is clamped to binary one. To avoid further complicating the following detailed descriptions, we will not mention these control signals again.

7.6.3.3. Control of the Initiating Modem (Modem "A")

The need to start an RDL test must be determined by the microcontroller in modem A. Check that a connection exists to another modem in a DPSK or QAM mode before proceeding. You will probably do this by testing status information held within the microcontroller itself. Also you can read the K-Series registers to determine the modulation mode (CR0 bit 5 = 0 for DPSK and QAM) and other status information. If all is well, send the initiation

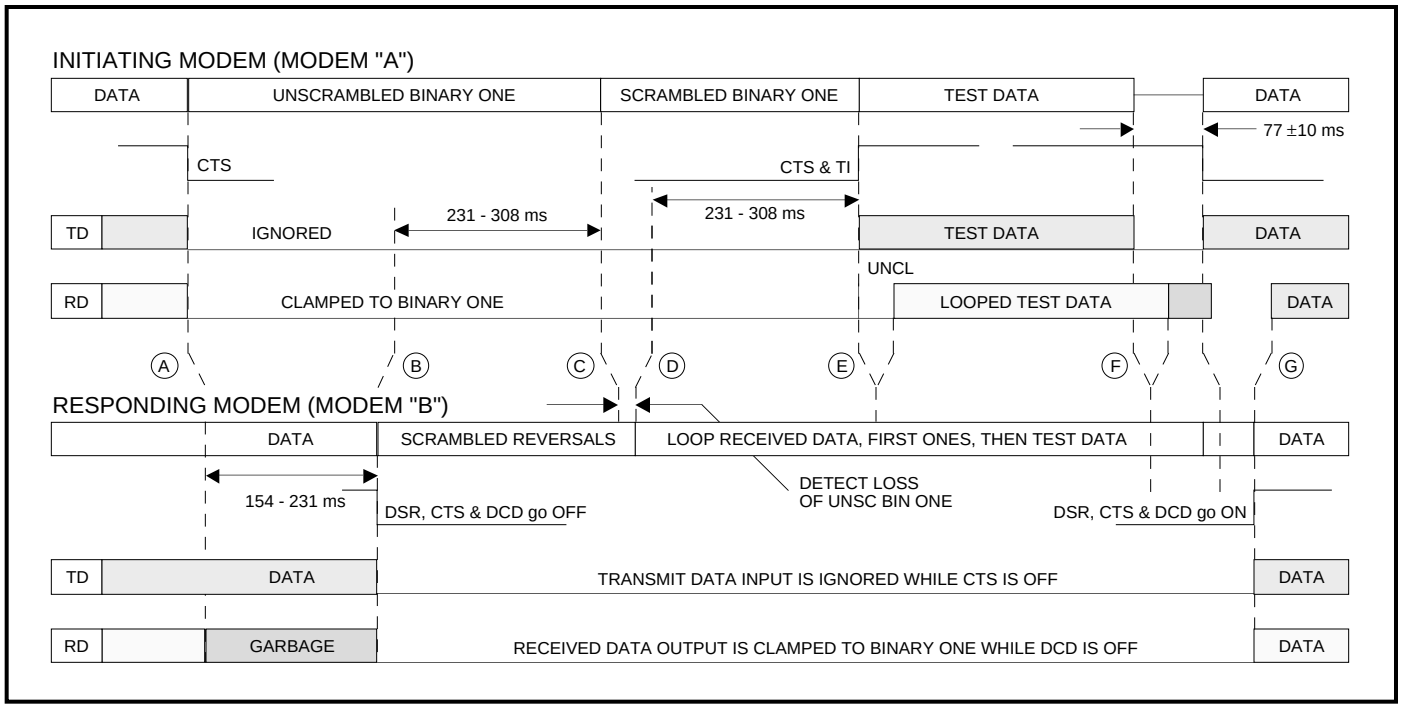


FIGURE 7 – 14: Establishing and Terminating Remote Digital Loopback

signal by writing to CR1. Write bits 7 and 6 with 10_2 to transmit binary ONES and bit 4 with 1 to bypass the scrambler. We have put these control bits in the same register so that they can be written together, thus avoiding a brief period in which some other signal is transmitted. Note that the data rate should remain at the rate of the connection, either 1200 or 2400 bit / s.

At point (A) in the figure, having started transmitting the initiation signal, modem A must monitor the received data for the acknowledgement signal. Do this by looking at Receive Data in the Detect Register. At point (B), this signal arrives from the remote modem and the Receive Data bit alternates between one and zero at the data rate of the original connection. V.22bis specifies that you should detect 231 to 308 ms of these scrambled reversals. A special algorithm must be designed for this purpose as outlined in section 7.1.5.2, Monitoring the Modem's Received Data Line. When you have detected the requisite period of the acknowledgement signal, we are at point (C). Now change the transmit signal of modem A from unscrambled binary ONES to scrambled binary ones. To do this, you need only clear the Bypass Scrambler bit (bit 4) in Control Register 1. If the remote modem is unable to respond to the request for an RDL, either by design or because it has been configured that way, it will not send the acknowledgement signal. Therefore start a timer in Modem A when you begin the initiation signal and if the timer expires before the acknowledgement signal is received, return the modem to normal operation. You can provide an indication to the operator that the test was not established. A value of two seconds for the timeout should be suitable in all cases.

Now, modem A is waiting for modem B to see that it has stopped the initiation signal and to make the loopback connection. This happens at point (D) in the figure. Now, modem A's transmitted data will be coming back so you will see scrambled binary ONES at the receiver here. V.22bis specifies that you should detect 231 to 308 ms of this signal. Again refer to section 7.1.5.2. Having done this at point (E), you can send test data and expect it to come back at the receiver. If you are going to provide the test data at the TXD pin, put the Transmit Pattern bits (bits 7 and 6) of Control Register 1 back to their normal data state of both ZERO.

To terminate the test, silence the transmitter for 77 ±10 ms as at point (F). Clear bit 1 of CR0 to ZERO and set a timer for 77 ms. If, during the test, you were using a transmit pattern generated in the modem chip, put the Transmit Pattern control bits (bits 7 and 6) in CR1 back to ZEROs to select the user data. On expiry of the timer, turn the transmitter back on by setting bit 1 of CR0 to ONE. Soon, at point (G), the data from the DTE at the remote end will reach the receiver and the test is over.

7.6.3.4. Control of the Looping Modem (Modem "B")

If you wish to allow RDL tests to be made, watch for an initiation signal from the other modem whenever you are in the normal data mode. V.22bis specifies that you should detect 154 to 231 ms of unscrambled binary ONES before considering it a valid RDL request. When the K-Series modem receiver finds a signal that looks like unscrambled binary ones, it sets the Unscr. Mark bit (bit 4) in the Detect Register. See section 7.1.5.1 for information on qualifying this bit, DSP-based and non-DSP K-Series devices have

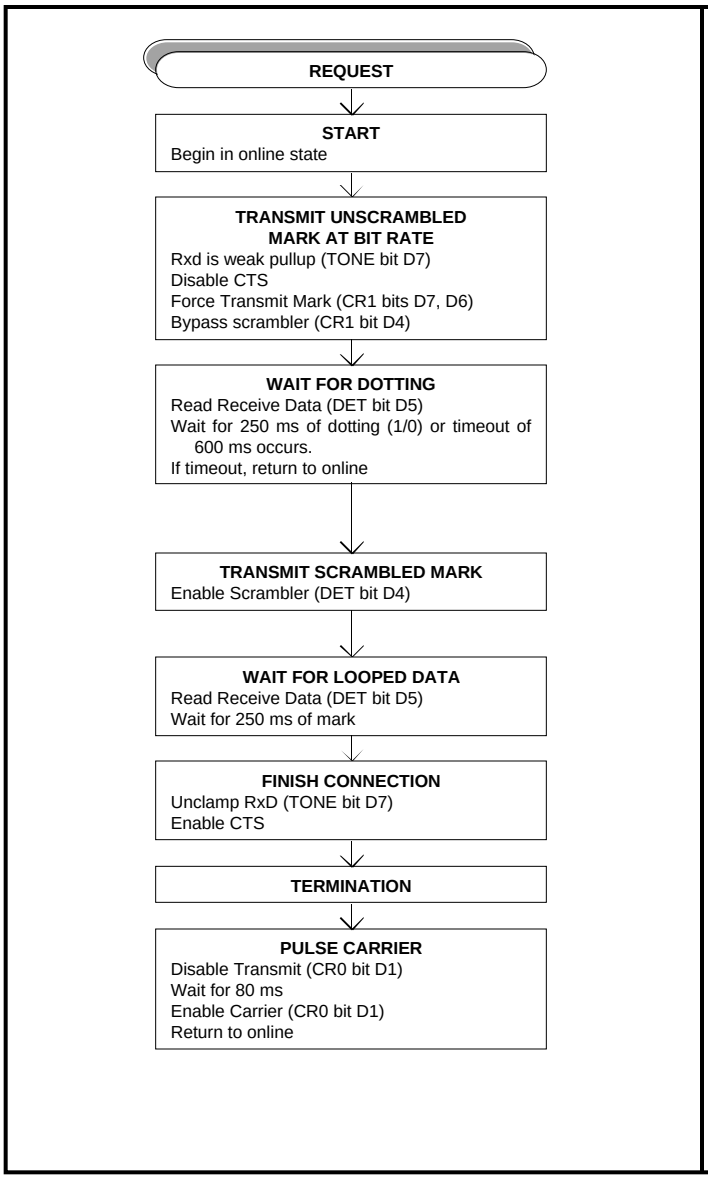


FIGURE 7 – 15: Flow-Chart for Initiating a Remote Digital Loop

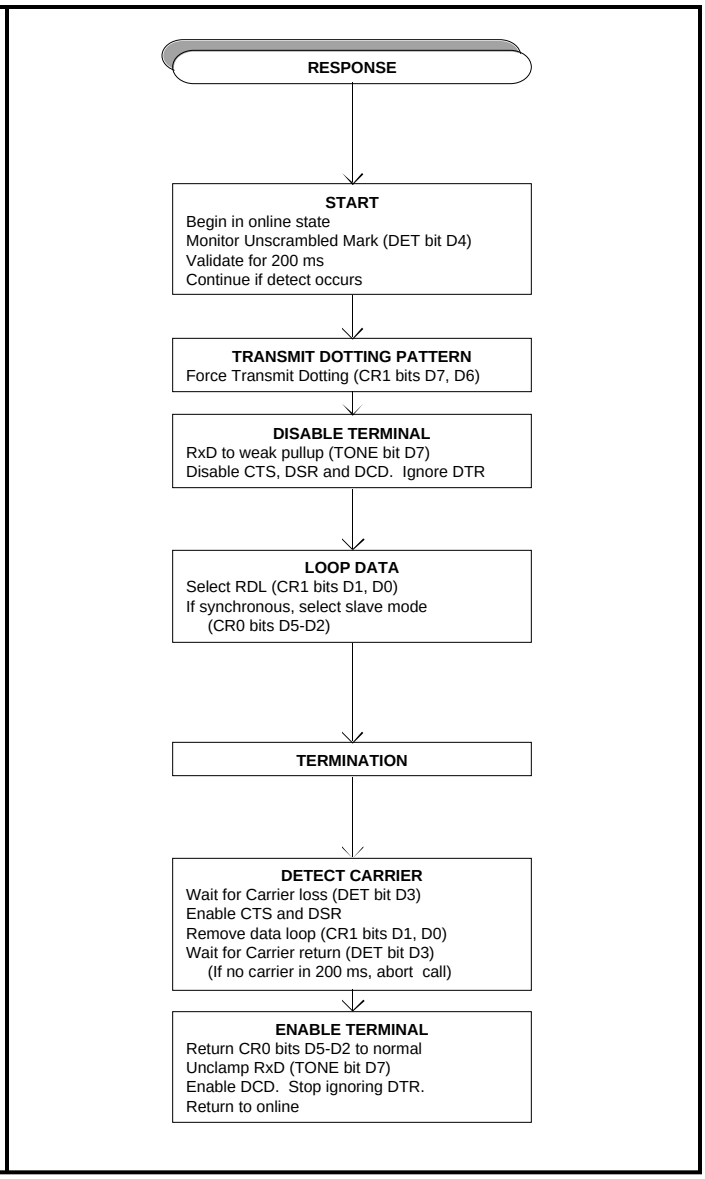


FIGURE 7 – 16: Flow-Chart for Acknowledging a Remote Digital Loop

differences in this area. If a request for RDL arrives as at point (A) in the figure and you qualify it for the necessary time at point (B), you are now a "modem B" as discussed above. Assuming that you will accept RDL tests, transmit the acknowledgement signal of scrambled reversals. Change the Transmit Pattern bits (bits 7 and 6) in Control Register 1 to be 01_2 to select alternating binary ONES and zeros as the transmitted data pattern.

Having started the acknowledgement signal, continue to look at the initiating signal from modem A. When this signal goes away at point (C), modem A has seen our acknowledgement and it is time to complete the loop. V.22bis is not specific about detecting the loss of the initiation signal. Do not simply look for Unscr. Marks to go low as a noise burst on the line could cause this. Wait for it to stay low for 100 ms or so before acting, or alternatively explicitly detect the next signal from modem A, which is scrambled binary ones. At point (D) in the figure, the decision has been made that the initiation signal has ended. To complete the loop, two things must be done. First, place the modem in loopback (or receiver slaved) timing mode. To do this, write the Transmit Mode bits (bits 5 to 2) in Control Register 0 with 0011_2. The transmitter will now run at the exact same rate as the receiver so that each received bit can successfully be sent back out. Secondly, loop the received data around to replace the data at the TXD pin as the transmitter input. Write 10_2 to the Test Mode bits (bits 1 and 0) in Control Register 1. It is also possible to make the loop in start/stop (character asynchronous) mode. To do this, leave the Transmit Mode bits alone and just write 10_2 to the Test Mode bits. The bit-synchronous to start/stop format converter circuits will now remain in circuit and will be tested along with everything else. However, only start/stop data of the correct character length will be looped without

error, you cannot use bit-synchronous test patterns such as reversals or pseudo-random 511. The synchronous loop described first will work for any data format transmitted by modem A.

Modem A will terminate the test by silencing its transmitter for 77 ±10ms as at point (F). At modem B you will see this by looking at the Carrier Detect bit (bit 3) in the Detect Register. After the silence, look for Carrier Detect to come back on and stay on for 155 ±50ms as required by V.22bis. Then return to normal operation at (G) by restoring the original Transmit Mode bits in Control Register 0 and writing ZEROs to the Test Mode bits in Control Register 1. If modem B is allowed to terminate the test, it should do so using the procedure described above for modem A.

7.6.4. Transmitting and Receiving Test Patterns

In either the Local Analog or Remote Digital loopback tests, the data output by the modem receiver should match the data sent by the transmitter. To verify that this is so, the normal source of data may be called upon to send a known data pattern and to check the resulting received data against it. For an operator initiated test at a normal modem, this amounts to hammering on the terminal keyboard and watching the screen. You could also program the processor in your system that generates the data to automatically perform a data test and to report on any errors received. If this is not convenient, the K-Series products provide a means of doing this from the control processor. The Transmit Pattern bits (bits 7 and 6) in Control Register 1 allow you to program the modem IC to ignore data at its TXD pin and send instead one of three data patterns. With bit 7 at ZERO and bit 6 at ONE the pattern is alternating binary ONES and zeros (reversals) and this is suitable for testing a connection. The controller can check the received data by looking at the Receive Data bit in the Detect Register. There is no way of knowing exactly when a new bit arrives here, but if you examine it fast enough you can account for any bits you sample twice or not at all by keeping track of the pattern.

The Hayes AT™ command set has provisions for entering loopback modes with automatic test pattern generation and checking. The AT&T8 command initiates a Local Analog Loopback in exactly the same way as the AT&T1 command, except that a data pattern self-test is performed. The modem ignores data at the input of its DTE port and does not present its received data at the data output. A data pattern is generated internally, the received data is compared to this and errors are reported to the DTE. In the same way, the AT&T7 command initiates a Remote Digital Loopback, as for the AT&T6 command, but with data pattern self-test. Many modems use the CCITT V.54 test pattern for self-tests. This is a pseudo-random pattern repeating every 511 bits. The K-Series products do not generate this pattern, if you wish to use it you must generate it in the controller. All tests, including self-test loopbacks, are terminated with the AT&T0 or AT&T command.

7.7. TERMINATING A CONNECTION

All good things must come to an end and sooner or later it will be time to terminate even a data connection using a Silicon Systems K-Series modem. In a standalone modem, this can be done by pressing the TALK/DATA switch, if one is present. Using the Hayes AT™ command set, you can escape to command mode (usually by typing "+++") and then type ATH. For modems controlled by the DTE, the modem may be instructed to go on-hook by putting the V.24 control line DTR from the terminal to the OFF state. The AT&D command allows the modem's response to DTR to be changed and the "S" register S25 allows you to set the response time to DTR going OFF (the default is 50 ms). In embedded modem systems, some other part of the system will indicate that the connection is to be terminated when the data exchange is complete. The CCITT Recommendations don't suggest any elegant ways to end a data call so we are indebted to AT&T for long space disconnect (See Section 7.7.2).

7.7.1. Hanging up the Line

The most common method of terminating a data connection is by one of the modems going on-hook (hanging up) to disconnect the call. Either modem may do this, however it is more often the calling modem as the answering modem may be unattended. The modem hanging up may or may not stop transmitting its signal first. It should put the V.24 control lines DSR, DCD and CTS to the OFF state, if implemented. The other modem in the connection detects the loss of carrier from the remote end and also goes on hook. A message or other signal may be transmitted to the operator or host equipment to indicate the end of the call. A modem should not disconnect immediately on sensing the loss of carrier as short interruptions can occur in the course of a call due to malfunctioning of network plant. The DCD control line may, if implemented, follow the state of the received line signal with a response time as required by the modulation standard. While DCD is OFF, the received data at RD should be clamped to one (mark), but DSR and CTS stay ON until the disconnect occurs. In Hayes™ compatible modems, the length of time for which the signal from the remote modem must be absent before disconnect occurs is programmable via "S" register S10. The default is often 7 in this register which corresponds to 0.7 seconds.

7.7.2. Long Space Disconnect

When a call is terminated by one of the modems hanging up, the other modem takes some short time to sense that carrier is no longer present. During this time, it may attempt to interpret noise on the line as data and output spurious data to the DTE or host system. A method of preventing this is long space disconnect, which was put forward by AT&T in Technical Publication 41214 (and previously in CB109) as part of the Bell 212A and Bell 103 specification. The modem that wishes to terminate the

connection sends continuous binary zeros (spaces) for 3.95 ±0.15 seconds (CB109 says 3.8 to 4.07, a typical value is four seconds) before going on-hook. When it begins sending spaces, it puts the V.24 control line DCD to the OFF state and clamps the received data at RD to one (mark). Control lines DSR and CTS, for some reason, remain ON during the spacing and go OFF when the modem goes on-hook. The other modem detects 1.6 ±0.15 seconds (CB109 says 1.49 to 1.77, a typical value is 1.6 seconds) of these spaces at its receiver, recognizes this as a disconnect signal and goes on–hook. At this time it also puts control signals DCD, DSR and CTS to the OFF state. The continuous spaces do not cause characters to appear at the modem output in a character asynchronous connection, although they do look like a break signal. Furthermore, when the remote modem disconnects, the modem sending the long space has already clamped its data output and will not be troubled by the sudden loss of carrier. In Hayes™ compatible modems, long space disconnect can be enabled or disabled with the ATYn command. ATY0 disables the feature and ATY1 enables it. It can also be selected or examined at bit 7 in "S" register S21. The default is a zero here, equivalent to an ATY0 command, which disables long space disconnect.

The transmission of continuous binary zeros presents no problem to K-Series modems. By writing ONES to bits 6 and 7 of Control Register 1, you can set the modem IC to ignore the data at the TXD pin and send zeros instead. Alternatively, you can present a continuous ZERO state at the TXD pin. In the character asynchronous mode, the signal will pass through the converters at both transmitter and receiver without the insertion of unwanted stop bits. Detecting 1.6 seconds of zeros is a little more difficult, but see section 7.1.5.2, Monitoring the Modem's Received Data Line.

7.7.3. Soft Carrier Turn-Off in Bell 202

Bell Standard 202 includes special provisions for ending a call without spurious characters being output by a modem when the other modem's data signal ends. Before dropping carrier to terminate a call, the modem stops sending data and sends marks instead for a short time. Then, it changes the transmitted frequency from the normal 1200 Hz marking signal to a special soft carrier tone of 900 Hz. This tone is still interpreted by the receiver of the other modem as a mark, so its output remains stable. However, a special detector senses the presence of this tone and enables the received data line to be clamped to mark. The first modem now ends its transmission without risk of spurious characters at the receiver before the carrier loss is sensed. This soft carrier turn-off is defined only in the forward channel.

The K-Series family members that support the Bell 202 standard, such as the 73K302L, include soft carrier turn-off features. The modem transmitting in the forward channel (bit 0 of Control Register 0 is ONE) must terminate the call. Make sure that the flow of data is over and the transmitter is marking. Switching to soft carrier in the middle of a character will cause spurious characters to be picked up at the receiver - the problem you are trying to avoid. Turn on the soft carrier by writing ONE to bit 6 of the Tone Register. The transition from the 1200 Hz marking tone to 900 Hz is phase-continuous to ensure that the remote receiver continues to see a mark. After a short time, it is now safe to disable the transmitter by clearing bit 1 of Control Register 0 to ZERO. The duration of the soft carrier tone is generally very short, down to 8 ms, but a longer duration cannot be harmful and will not perceptibly delay the call termination. The 73K302L can detect the tone in a maximum of 15 ms, so 20 ms would be a suitable duration. The modem receiving in the forward channel (bit 0 of Control Register 0 is ZERO), should examine bit 2 in the Detect Register during the data call. This is the Special Tone Detect bit, and will respond to the 900 Hz soft carrier tone if the K-Series chip is appropriately programmed. In addition to selecting the Bell 202 mode and receiving in the forward channel, it is necessary to clear bit 0 of the Tone Register to ZERO.

7.7.4. Powering-down the K-Series Modem IC

After a call has been terminated, it makes sense to conserve power by powering-down the K-Series modem IC. This is done very simply by writing a ONE to the RESET bit (bit 2) of Control Register 1. All Control Register bits and the Tone Register bits are forced to a safe default state as described in section 6.1.4, Resetting the K-Series Modem IC at Power-Up, and most of the internal circuitry of the chip is put into an idle mode. The CLK pin will revert to echoing the crystal frequency if it has been set otherwise. The register interface, however, stays active so that the controller may still write to the registers. To bring the part out of power-down, write something other than ZEROs to bits 2 to 5 of Control Register 0. You should not consider the loss of the configuration in the K-Series modem a disadvantage of power-down. It is good practice to totally renew the configuration on each call to avoid difficult to reproduce bugs which may appear in the controller firmware.

Section 8.0

K-SERIES DESIGN EVALUATION KITS

8.0. K-SERIES DESIGN EVALUATION KITS

To assist in evaluation and prototyping of modem designs, Silicon Systems has a variety of Design Evaluation Kits (DEK) based on Silicon Systems' 1-chip modem products. DEKs typically contain the following: a design manual and user's guide; a complete, functioning Modem Evaluation Board (MEB), which uses Silicon Systems modems in a design that emulates commercially available modem products; a modem controller IC or set of ICs, to provide "AT" commands and other modem protocol. DEKs are available from Silicon Systems' stocking distributors. For further information, contact the Silicon Systems distributor or sales representative nearest you. The following sections summarize features of currently available and planned products and demo vehicles.

PRODUCT	DESCRIPTION	DEMO AVAILABILITY
1201 DEK	Stand-Alone Modem, User's Manual for 12V supply 1200 bit/s K-Series Modem ICs – accepts 73K212, 221, and 222 products.	In Stock
73K222U DEK	IBM PC 1/2 Card Modem Evaluation Board, Design Manual, operating and demonstration software on diskette, 73D620L "AT" Controller for 73K222U Modem/UART products.	In Stock
2402 DEK	Stand-Alone Modem Evaluation Board, Design Manual, "AT" Controller (73D600) and demonstration software, for 5V 1200 and 2400 bit/s K-Series Modem ICs – accepts 73K224L, 222L, 221L, 212L products.	In Stock

TABLE 8.1: Silicon Systems Design Evaluation Kits (DEKs)

Silicon Systems controllers are marketed in device sets which include the controller device or devices, and the appropriate 1-chip modem IC which is suitable for the application. Table 8.2 shows modem/controller IC sets that will be available from Silicon Systems (MEB's will be available for most of these sets). For further information, contact your local Silicon Systems Sales office or distributor.

PRODUCT	INCLUDES	DESCRIPTION	DEMO AVAILABILITY
73D2180	73K222U 73D620L	1200 bit/s "AT" MODEM/UART for integral designs	In Stock
73D2240	73K224L 73D600	2400 bit/s "AT" modem for low power designs 2402 DEK includes 73D2240 chip-set	In Stock
73D2404	73M214 73D215 73D216	V.22 bis, V.22, V.21, Bell 212A, 103 high performance device set	In Stock
73D2407/17	73M214 73D218 73D221	MNP2-5, V.42, send only FAX chip set based on 2404 device set	In Stock
73D2247	73K224L 73D631 73D630 Source Code Diskette	V.22bis, MNP2-5, V.42, V.42bis device set, there are several versions of this device set.	In Stock
73D2247F	73K224, controller, source code diskette, FAX chip	Same as 73D2247 plus send/receive FAX	Q2, '91
73D2421	73K224, 73D680 73D681 73D682	V.22bis, MNP2-5, V.42, V.42bis, Hayes® AutoSync device set	In Stock

TABLE 8.2: Modem Device Sets

Section 9.0

K-SERIES COMPANION CONTROLLER PRODUCTS

9.0. K-SERIES COMPANION CONTROLLER PRODUCTS

All K-Series modem ICs require a microprocessor or microcontroller of some sort to control their operation. For some applications, this may be already present in the system and you will choose to add the necessary code to the existing program. However, there are some applications in which the controller must perform a standard function, such as the interpretation of an industry standard command set and perhaps error control. In these cases, Silicon Systems may have already programmed a controller to meet these needs.

To assist in evaluation and prototyping of modem designs, Silicon Systems has a variety of Design Evaluation Kits based on Silicon Systems' 1-chip modem products. DEKs typically contain the following: a design manual and user's guide; a complete, functioning evaluation board (MEB), which uses K-Series 1-chip modems in a design that emulates commercially available modem products; a modem controller IC or set of ICs, to provide "AT" commands and other modem protocol. DEKs are available from Silicon Systems' stocking distributors. For further information, contact the Silicon Systems distributor or sales representative nearest you. The following sections summarize features of currently available and planned Silicon Systems controllers, marketed in device sets which include the controller device or devices, and the appropriate 1-chip modem IC which is suitable for the application.

9.1. DEMO CODE FOR THE 73K224L

The 2402 DEK Design Evaluation Kit for the 73K224L is supplied with an external EPROM programmed with a special code that allows you to exercise more control over the modem chip than would be needed in an actual application. For example, the adaptive equalizer can be enabled and disabled from the keyboard and the transmitter output level can be changed during a connection. Also, the state of the modem chip's internal Detect Register can be monitored "real time" with an LED indicator or on an oscilloscope. Because this code allows the chip's operation to be demonstrated in a flexible way, it is known as the Demo Code. Note that it uses a custom command set and is in no way compatible with the Hayes AT™ command set. Versions available at the time of writing do not support dialing strings; the connection must be established by manual dialing or through a telephone line simulator.

The Demo Code can provide a useful model for the development of an application. By examining the code that monitors the status of the K-Series chip and steps it through the connect handshake, it is possible to see how you should do this in your own programs. However, you must remember that the code was written to demonstrate the capabilities of the modem chips and not to provide the robustness and full functionality of a product. There are many functions in the code that you will not need and also several features that, although they do not harm the usefulness of the Demo Code, would require review before being released in a product.

Section 10.0

OTHER SILICON SYSTEMS MODEM PRODUCTS

10.0. OTHER SILICON SYSTEMS MODEM AND MODEM SUPPORT PRODUCTS

In addition to Silicon Systems' 1-chip modem family, there are additional available or planned Silicon Systems products which you may want to take into consideration in your designs. These products are discussed briefly in the following sections. Current proposals are included in the Silicon Systems Communication Products Data Book. Data sheets on newer products are available separately. For further information, contact your local Silicon Systems representative.

10.1. THE 73D2404 V.22BIS MODEM CHIP SET

The 73D2404 provides a complete 2400 bit/s "AT" modem design in a compact 3-chip set. This is a proven, cost-effective, and high performance design which is suitable for turn-key "AT" modem designs. The "AT" command set is fixed by product design and may not be modified by the user.

This chip set consists of the SSI 73M214 analog front-end chip, an SSI 73D215 DSP chip and a pre-programmed microcontroller. With the addition of a telephone line interface circuit, such as that described here in section 6.5, these three chips implement a complete modem compatible with the Hayes Smartmodem 2400™ command set. An additional non-volatile memory chip is required for telephone number and user profile storage. The chip set supports CCITT V.22bis, V.22, V.21 and Bell 212A and 103 modulation standards. The advantage of the 2404 set is its low system cost and its strength as a turn-key solution.

10.2. HIGH SPEED K-SERIES COMPATIBLE MODEM PRODUCTS

Silicon Systems' present modem product line provides for speeds up to 2400 bit/s. New products are currently in development that will extend operation to additional standards and effective operating speeds up to 14.4 kbit/s. Where possible, these products will maintain design compatibility with Silicon Systems' existing 1-chip modem products, so design requirements using these higher speed products will be consistent with the information presented in this manual. Information on new products will be released as it becomes available. For further details, contact your local Silicon Systems sales representative.

10.3. THE 73M373 INTEGRATED DAA IC

Design of the DAA can vary significantly depending on the application and country of intended usage, adding to the complexity of the modem design. Silicon Systems' SSI 73M373 is a new product that simplifies DAA design for standardized applications by integrating many of the features required in typical applications. This product is designed to interface with any of Silicon Systems' 1-chip modem ICs and can reduce power, space, and overall complexity in typical modem applications. For further information, contact your local Silicon Systems sales representative.

10.4. SILICON SYSTEMS UARTS FOR MODEM APPLICATIONS

Silicon Systems has an extensive line of UART products to support PC- and PS/2-type microcomputer bus interfaces. These products are compatible versions of industry standard UARTs with enhancements needed in modem designs.

The SSI 73M450 is pin- and function-compatible with the NSC 16C450 UART. Higher output current permits the chip to directly drive large loads, and the chip's oscillator may be shut off to conserve power while retaining all memory. A fast version of the 73M450 is available, and both products are available in 40-pin DIP or 44-pin PLCC packages. An enhanced version of the part, the 73M450L, allows the oscillator to be turned off via software control.

For applications requiring smaller packaging, Silicon Systems created 28-pin versions of the 73M450L. The SSI 73M1450 and 73M2450 are identical except that the 73M2450 adds a µPRST pin (for hardware reset) at the expense of the XOUT pin, and therefore must be driven via external clock. Another added feature of both 28-pin chips is the ability to set the INTRO pin to a high impedence state via software. For PS/2 applications, Silicon Systems offers the SSI 73M1550 and 73M2550. These versions are analogous to their "450–type" counterparts. For further information, consult the Silicon Systems Communication Products Data Book.

Section 11.0

TROUBLESHOOTING THE MODEM DESIGN

11.0. TROUBLESHOOTING THE MODEM DESIGN

11.1. POSSIBLE CAUSES OF A TOTALLY DEAD SYSTEM

It is always particularly depressing when you power–up a new design for the first time and absolutely nothing happens. However, this is often the easiest type of fault to find. We will try to think of a few things that could cause this problem (apart from the obvious, like the plug falling out of the wall socket).

11.1.1. The K-Series Modem IC is Stuck in the Reset State

You will generally get very little cooperation from a K-Series modem IC while it is in the power-down state. It enters this state when a reset operation is performed, either by writing to the Reset bit (bit 2) in Control Register 1 or by taking the RESET input pin to logic ONE. Make sure that your firmware is bringing the part out of this state by writing something other than all ZEROs to bits 5 to 2 in Control Register 0. Also, make sure that this happens after the RESET pin has been returned to logic ZERO. A capacitor from this pin to VDD can hold the part in the reset state for many seconds, see section 6.1.4., Resetting the K-Series Modem IC at Power-Up. Attempts to program the part during this time will not take effect. For products with a DSP, check that the $\overline{\text{RESET}}$ $\overline{\text{DSP}}$ bit (CR2 bit D2) is also written with ONE when appropriate.

11.1.2. Crystal Oscillator Fails to Start

If a complete crystal oscillator is used to directly drive the K-Series modem, any starting problem should be addressed to the manufacturer of that device. If the internal oscillator is used with a crystal, there may be situations in which it will not start. Check the values of the capacitors from XTAL1 and XTAL2 to ground. If these are too high in value, 40 pF or above, the oscillator may not start. Such large values are not recommended and should not be necessary if the crystal is correctly specified. Also ensure that the circuit board is designed to minimize stray inductance and capacitance in the area of the oscillator. The crystal and both capacitors should be placed as close as possible to the XTAL pins of the K-Series modem IC and connected by direct traces. The ground connection of the capacitors should be via wide traces to the digital grounding system. It is also possible that the oscillator will not start or will be slow to start if the risetime of the power supply voltage is very long. The starting properties are helped by the asymmetry in the load capacitor values, the capacitor at XTAL1 should be about twice as large as that at XTAL2.

11.1.3. Clock to Microcontroller Isn't Getting Through

Using the K-Series modem ICs on-chip clock oscillator to generate timing for the entire system is very efficient from the point of view of component count and EMI generation. However, note that the CLK output of the modem chip is specified only to drive TTL compatible inputs. Many common microcontrollers require clock inputs that rise closer to the supply voltage for logic ONE. We have seen applications which use the CLK pin to drive these inputs without problem, however, the low-power (5V supply) parts may give a lower logic ONE level than is necessary at elevated temperature. We recommend that you use a TTL to CMOS level converting buffer between the CLK pin and the controller clock input in 5V systems. A pullup resistor to the 5V supply is not effective in increasing the logic high voltage.

11.2. CONNECT HANDSHAKE FAILS

If your system seems to be working well but cannot get into the situation of exchanging data with another modem, it is likely that you have a problem in the connect handshake. It is better to examine handshake problems using a "known good" modem at the remote end rather than another of your own systems. This helps isolate problems if more than one are present. Use a modem from an established and reputable manufacturer, as discounted generic modems may not conform fully to established specifications. Depending on the modulation mode, there may be many or few opportunities to fail so we can only offer general pointers to problems we have encountered in the past. It is very helpful to build extra diagnostic code into the handshake to diagnose unexpected conditions.

If things never start, check that the initial set-up of the chip is correct. The chip must be taken out of power-down before it will do anything and in DSP-based chips the DSP must have been reset after any previous call and then taken out of the reset state. (A DSP–based part cannot be used in a non-DSP socket without many such changes to the controller code; watch this when upgrading a 73K222 system to use a 73K224.) If in call mode the answer tone is not detected, check that you have selected the desired answer tone frequency by programming in the Tone Register. The selectivity of the answer tone detector is quite high, so verify that your answering modem is generating a frequency within the specifications of the modulation standard. You should be able to verify the operation of your various signal detectors with breakpoints in the controller code. If these do not fire at the appropriate point, the handshake is likely to hang-up or get out of step with the other modem. Be especially careful with the S1 detector, see section 7.1.5.3; if this is failing you may get connections at 1200 bit/s which were supposed to be at 2400 bit/s. With DSP-based chips in QAM or DPSK modes, make sure that you are enabling the adaptive equalizer at the appropriate time. Enabling it too early, when the received signal is unsuitable for training, and too late, when there is too little time left before the gear shift to 2400 bit/s, can both give connect problems. Finally, make sure the crystal oscillator frequency is in specification as a gross error here can cause failure of the handshake.

11.3. ERRORS COMMITTED IMMEDIATELY AFTER HANDSHAKE, WITH IMPROVEMENT

We have seen situations in which a DSP-based K-Series modem makes many data errors during the first few seconds of a connection, but then shapes up and performs normally thereafter. This is generally due to some problem in equalizer training in a DSP-based chip. The equalizer must be held in the initial state (bit 0 of CR2 = ZERO) up to the point in the handshake when scrambled PSK binary ONES first appear at the receiver. It must then be released promptly (bit 0 of CR2 = ONE) and allowed to adapt so that it is fully trained before the gear shift to 2400 bit / s and the transition to data mode occurs. Enabling the equalizer too early will cause it to train on an unsuitable unscrambled signal. Because it adapts more rapidly immediately after being enabled, it may take a long time to recover from a bad solution when the correct receiver signal arrives. Enabling the equalizer too late reduces the time available for training before the received data is relied upon to be correct. If you have to put the equalizer back into the initialized state after a period of training, make sure that Equalizer Enable (bit 0 of CR2) stays at ZERO for at least 2 ms. It is better to have the Receiver Gain Boost bit dealt with before the equalizer is enabled, otherwise transients caused by changing this bit may upset the equalizer solution.

11.3.2. Errors Experienced at High Receive Signal Levels

If the error rate gets worse at high receive signal levels, you should look for some source of clipping in the receive path. Injecting a signal of known level at the line coupling transformer and looking at the RXA pin with an oscilloscope should enable you to isolate any problem in the line interface. Look for excessive gain in the receiver buffer amplifier or other causes of clipping at this point such as badly chosen op-amps for single 5V supply operation. If the signal at RXA looks good and you are using a DSP-based modem chip, it is possible that the controller is incorrectly inserting the receiver gain boost even if the Receive Level bit in the Detect Register is set. Note that early data sheets for the 73K224L gave this bit the wrong sense, i.e., ONE for low level. Only set Receive Gain Boost if this bit is ZERO.

11.3.3. Errors Experienced at Low Receive Signal Levels

There can be many causes of data errors at low receive signal levels, almost all associated with the presence of some level of interference or noise in the receive path. If you are performing tests over the telephone network, make sure that the error rate you are experiencing is not to be expected from the background noise level on the line. It is best to use a line simulator or a direct connection through an attenuator if looking for system noise problems. The capacitor across the feedback resistor of the receiver buffer amplifier is important to attenuate out-of-band noise at the modem chip receiver input.

Distortion in the telephone line interface can be located by injecting low-level signals into the line terminals and examining the signal at the RXA pin with a spectrum analyzer. Look for crossover distortion in the receiver buffer amplifier. This can arise from a poorly chosen op–amp type, such as the LM324 which makes a transition from class A to class AB operation at low signal levels and is not suitable for this application. We have found 348 and 1458 type op-amps to be free from this problem. It is also possible for the line coupling transformer to introduce harmonic distortion, particularly when a large D.C. holding current is flowing.

In the absence of significant distortion, look for a high noise level at the RXA pin. Another symptom of this problem, apart from data errors, is that the Carrier Detect bit (bit 3 in DR) comes on or blinks when no signal is applied to the modem receiver. The system may also fail to disconnect at the end of a call. If this is your experience don't confine your search to the normal carrier bandwidth because the modem chip will also be susceptible to higher frequencies. Op-amps may be noisy or may self-oscillate at low level due to poor layout. If the op-amps themselves are not causing the noise, it may be due to poor circuit layout or grounding. If, finally, nothing suspicious is visible at the RXA pin then the noise must be getting into the receive signal inside the modem IC. This can be from the power supply and bias pins or from signals routed under the chip. Check the connections to GND, VDD, VREF and ISET pins for component values and placement and routing of decoupling components. You are more likely to have problems with supply noise if you are using a switching power supply. Look also for fast digital signals routed under the modem IC; these should be re–routed and a ground plane placed under the chip. Serious interference pickup problems can be created by two crystal oscillators producing beat frequencies in-band to the modem. We strongly recommend using one master crystal in the system. Check the gain in the receive path from the line terminals and, in DSP-based parts, the state of the Receive Gain Boost bit set by the controller. If either of these are incorrect, then noise in the chip will appear more significant compared to the signal.

The transmitter of the modem can be a source of noise in the receiver. It should not generate signals that are in–band to the receiver, but this can happen if either the buffer amplifier or the line transformer are causing harmonic distortion. This will be most noticeable in call mode, when the low band transmit signal has harmonics in the high band filter of the receiver. For 5V only systems, the choice of op-amps in the buffer amplifier and their D.C. bias point is crucial to obtaining a sufficient voltage swing without distortion. Because of its internal operation, a small amount of switching noise is present at the TXA pin. The capacitor across the buffer amplifier feedback resistor is important to prevent this signal from reaching the receiver. It is difficult to obtain good rejection of the transmit signal at the receiver for all practical line conditions, but you should check that

your four-wire to two-wire hybrid circuit is operating correctly. For most terminations, the transmit signal at the RXA pin minus the receive buffer gain should be 6 dB below the level at the line.

11.4. SUBTLE PROBLEMS IN CERTAIN MODES OF OPERATION

11.4.1. Modem Works in Loopback but Fails to Connect or Makes Errors in Bursts with Some Other Modems

If anything appears "flaky" about the modem operation it is a good idea to check the oscillator frequency with a counter capable of resolving to at least ten parts per million. Using an oscilloscope is of no use whatsoever; see section 6.2. Many systems that use crystal oscillators are not very particular about the exact frequency; this is not so of modems. Measure the frequency at the CLK pin and verify that it is between 11.0581MHz and 11.0603MHz. Do not measure at the XTL1 or XTL2 pins as the probe capacitance will alter the frequency of oscillation. Some causes of out–of–specification readings are: a) the wrong crystal frequency entirely, b) a series-resonant crystal, or c) a parallel-resonant crystal unmatched to the circuit capacitance. See section 6.2.2.1, Specifying a Crystal.

11.4.2. Problems Unique to FSK Modes

Most K-Series modems do not permit answer tone detection in FSK modes, so ensure that a mode other than FSK is selected before attempting to detect answer tones. Consult specific product data sheet for correct operating modes.

Section 12.0

VERIFYING MODEM PERFORMANCE

12.0. VERIFYING MODEM PERFORMANCE

Silicon Systems has tested each member of the K-Series modem family to ensure that it performs in a manner consistent with industry expectations. The results of these tests are published in the current Silicon Systems Communication Products Data Book. The results show that the modems we have built using these ICs have performance similar to modems employing multi-chip solutions to the data pump. It is, however, possible to construct a modem from a K-Series modem IC which has inferior performance, either by accident or as a result of cost / quality tradeoffs. This section is concerned with how you can test your system and compare it with our data to gain confidence in your design. Alternatively, the methods described can be used to evaluate a K-Series demonstration unit against other solutions.

12.1. EQUIPMENT NEEDED

Thorough testing of modems requires a considerable amount of test equipment, mostly designed specifically for that purpose. Complete setups can be obtained from a number of manufacturers and we assume that if you have such a modem test installation you will know how to use it. The most basic test of modem performance is the data error rate in the presence of random noise at the receiver. However, see section below if you wish to compare with Silicon Systems measurements.

12.2. TEST METHODS USED BY SILICON SYSTEMS

There are many variables in a modem test setup which are not usually reported in the results summary. These can be manipulated to show a particular modem to be better or worse depending on the motives of the testers. For those wishing to compare their results to those published by Silicon Systems, or to compare the performance figures of other modems, we include here a brief summary of our setup and methods. See also the current Silicon Systems Communication Products data book.

To measure bit error rate in DPSK and QAM modes at 2400, 1200 and 600 bit / s, the modem is configured for synchronous operation. The bit pattern transmitted is pseudo-random of length 511 bits as defined in CCITT recommendation V.52. The error rate recorded is that measured at the DTE ports of the modems under test, no allowance is made for the multiplication of demodulator decision errors in the decoders and descramblers internal to the modem. Final reported results are the average of several tests of length 10^6 bits.

In evaluating performance against line noise, the noise is injected at the input to the receiving modem, after all other line impairments. The spectrum of the noise is approximately white and of bandwidth from D.C. to 5 kHz. The level of the noise is measured through a "C-message" filter and the level of the received signal is measured wideband, both at the receiver input. This results in a "C-message weighted" signal-to-noise ratio as is standard practice in the industry. Popular methods of falsely reporting high-performance data are limiting the spectrum of injected noise, even to the point of passing it through a C-message filter before adding it to the receive signal, and measuring the noise level without the C-message filter before the measuring instrument. The best method for evaluating our Bit Error Rate (BER) is to use a "standard" modem as the reference (or "master") modem and compare other modems against it.

12.3. SILICON SYSTEMS' PERFORMANCE MEASUREMENTS

See Silicon Systems Communication Products Data Book.

APPENDIX A: Hayes™ Compatibility and the K-Series Modem Command Sets

The issue of Hayes™ compatibility is difficult to pin down. Many modems claim this compatibility because they use a version of the Hayes AT™ command set. Probably the only simple test of true Hayes compatibility at the time of writing is to see if the modem works with the desired version of Smartcom™, Crosstalk™, or Procomm™; this is entirely defined by the microcontroller code and supporting hardware so that the Silicon Systems K-Series modem ICs offer no barrier to building a Hayes compatible modem. The EIA standards group TR30.4 are working on a standard for modem command sets based on the Hayes AT™. When this is available, compliance will be easier to achieve. However, the huge installed base of Hayes compatible modems and PC communications packages that rely on compatibility will make it difficult to phase out the present de-facto standards.

The AT™ command set consists of:

1) Commands that allow the DTE to control the modem.
2) Responses that the modem provides back to the DTE.
3) "S" registers that maintain the modem configuration information.

The effectiveness of the command set also relies upon certain additional features such as:

1) A speaker for monitoring the signal on the telephone line.
2) Indicators on the front panel.
3) Specific DIP switch positions and functions in PC card modems.
4) Default definitions of some adjustable parameters.
5) Specific (currently non-standard) use of the V.24 (EIA-232D) interface.

Of particular importance in Hayes compatibility are the implementation of the "S" registers, the product ID code and the response to the DTE control lines. Using the "S" registers, it is possible to redefine the characters that will be interpreted as "carriage return," "line feed" and "backspace." It is also possible to set configurations, enter and exit modes, and examine status through the "S" registers when explicit AT™ commands already exist to perform these functions. Communications packages such as Smartcom™, which use these capabilities, will not work with improper implementation of the "S" registers. The ATI or ATI0 command is a request for the product ID code. Communications packages may examine this for an indication of the modem's data rate capabilities. If an inappropriate code is returned, the software may refuse to make calls at the modem's maximum rate. Smartcom uses the basic five wires of the DTE interface (TXD, RXD, DCD, RTS and CTS) in a particular way. A compatible modem should emulate this as closely as possible.

Hayes modems themselves have changed over the years since the first appearance of the AT™ command set. There are now several versions of the command set intended to support modems with different maximum data rates. Three major variations can be identified which are currently in widespread use.

1) The original 1200 bit/s AT™ command set.
2) The 1200 bit/s command set with Dial String Extensions.
3) The 2400 bit/s command set with "&" (ampersand) commands.

Each version is also provided in two slight variations for use with the internal, PC card and external, standalone hardware configurations. Many other modem manufacturers have also introduced their own variations, either to add functionality to their products or by incorrectly implementing a Hayes function.

Originally, Hayes 1200 bit/s modems used switches to set the configuration that the modem took on power-up. More recent 2400 bit/s modems from Hayes and compatible vendors use non-volatile RAM to store the default configuration. The factory defaults have in some cases changed from 1200 to 2400 bit/s modems. The lower speed modems implemented the carrier detect indicator and DCD signal in the DTE interface so that they followed the actual status of the carrier from the remote modem. 2400 bit/s modems are delivered from the factory with the DCD line forced permanently ON. These defaults can easily be altered by changing switch settings in the modem or by using the AT&C1 command, but the unsophisticated user can easily be befuddled by such inconsistencies. Finally, Smartcom™ itself has gone through several versions and has changed its expectations of the modem to which it is attached.

The sequence of actions in the execution of an AT™ command is as follows:

1) DTE transmits the command to the modem through the normal serial data port. All commands except /A and the escape code are prefixed by "AT" and end with Carriage Return.
2) The modem pauses for 125 ms before execution of the command, reading and dumping any further characters from the DTE. This avoids any line feed characters following the carriage return from arriving after the execution of the command, which would activate the "key abort" feature.
3) The modem executes the command and sends result codes back to the DTE as appropriate. The result code, either verbose (words) or numeric, must be followed by carriage return and line feed, in that order.

4) The modem now has a 500 µs "end time" during which the DTE should not send a new command. It must use this time to wrap up execution of the last command and be ready for the next. Software developed to drive AT controlled modems should implement this delay after recognizing the result code and before sending the next command character.

The major states of a Hayes AT™ command set modem are shown in Figure A-1. Passage from one state to another is by the entry of a command, the receipt of a signal from the telephone line or a timeout elapsing. Return to the IDLE state from the DIALING or HANDSHAKING states is possible by sending any character, or "key abort."

FAX V.23+ modems receive ATHI command.

For your reference, we include here a summary of the AT™ command set. The complete list represents the Hayes Smartmodem™ 2400/2400B command set, commands in bold are also recognized by the 1200/1200B modems. The Smartmodem™ 300 commands have not been separated out. Commands marked thus: * are not supported by the 2400B because this is an internal card modem for IBM PC™ which have no bit-synchronous capability. Don't use this list to build a command set, there are too many quirks in the various versions for us to explain here, but this should give you an idea of what a comprehensive serial command set can do.

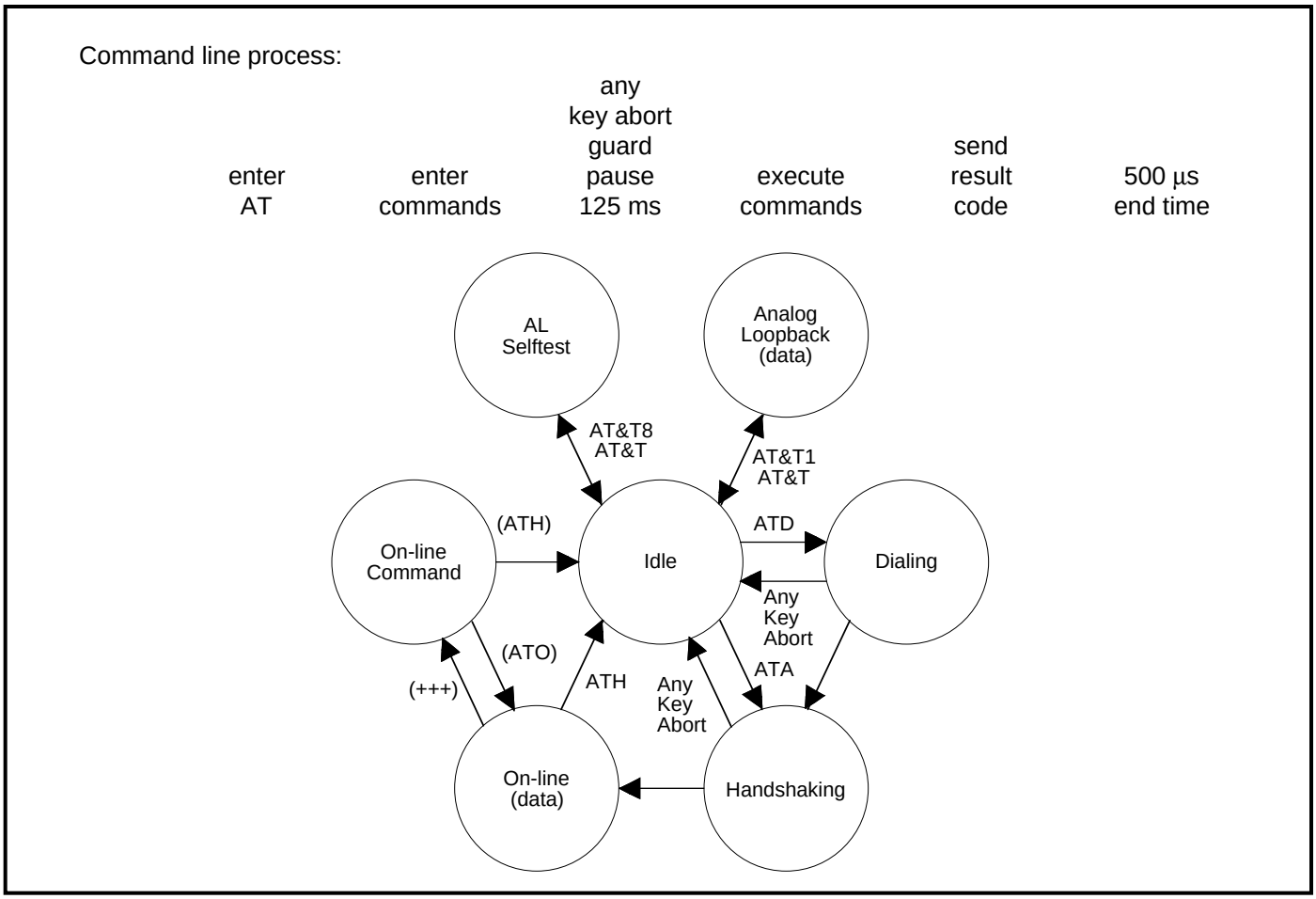


FIGURE A – 1: Major States of an AT Controlled Modem

AT	attention prefix; precedes all commands except the escape sequence (+++) and the repeat (A /) command. Entered alone, it causes no action but the return of result code 0, "OK."
A/	repeat last command.
+++	escape sequence; go to command state.
ATA	go into answer mode; attempt to go to on-line state.
ATB0	select CCITT **V.22** or V.22bis as communication standard.
ATB1	select Bell **103/212A** communication standard.
ATC0	carrier signal off until **ATC1** or **ATZ** (reset) command is issued. This command is not available on the 2400 / 2400B.
ATC1	carrier signal on; restores automatic carrier signal on / off switching; carrier signal remains on when modem originates or answers a call or is connected to another modem.
ATD	go into call (originate) mode; dial number that follows to go on-line.
The following dial modifiers can be used with the **ATD** command:	
0-9 #*	**ABCD** digits / characters for dialing.
P	pulse dial (factory setting).
T	tone dial.
!	hookflash.
@	wait for quiet answer (no dial tone transmitted).
W	wait for dial tone.
,	delay processing of next character by number of seconds in register S8.
R	reverse mode (to originate a call in answer mode).
;	return to command state after dialing.
S=n	dial number stored in location "n."
ATE0	disable character echo in command state.
ATE1	enable character echo in command state.
ATF0	enable character echo in on-line state (this command is not supported by 2400 / 2400B).
ATF1	disable character echo in on-line state.
ATH0	go on hook (hang up).
ATH1	line and auxiliary relays off-hook (not permitted by FCC Part 68).
ATH2	line relay only off-hook (not permitted by FCC Part 68, also not supported by 2400 / 2400B).
ATI0	request product identification code.
ATI1	perform checksum on firmware ROM; return checksum.
ATI2	perform checksum on firmware ROM; returns **OK** or **ERROR** result codes.
ATL0	low speaker volume (same as **ATL1**).
ATL1	low speaker volume.
ATL2	medium speaker volume.
ATL3	high speaker volume.
ATM0	speaker off.
ATM1	speaker on until carrier detected.
ATM2	speaker always on.
ATM3	speaker on until carrier detected, except off during dialing.

ATO0	go to on-line state.
ATO1	turn off remote digital loopback test function and return the modem on-line. In the 2400/2400B this command causes a return to the on-line state and initiates an equalizer retrain.
ATO2	request remote digital loopback test and return modem on-line.
ATQ0	modem returns result codes as selected by **ATVn** command.
ATQ1	modem does not return result codes.
ATSr	set pointer to address of register "r."
ATSr=n	set register "r" to value "n."
ATSr?	display value stored in register "r."
ATV0	display result codes in numeric form.
ATV1	display result codes in verbose form (as words).
ATX0	enable features represented by result codes **0-4**.
ATX1	enable features represented by result codes **0-5** and 10.
ATX2	enable features represented by result codes **0-6** and 10.
ATX3	enable features represented by result codes **0-5, 7** and 10.
ATX4	enable features represented by result codes **0-7** and 10.
NOTE: Result codes enabled are determined by specific result code set of each modem.	
ATY0	disable long space disconnect.
ATY1	enable long space disconnect.
ATZ	reset modem and recall factory configuration.
ATZ0	reset modem and recall user profile 0.
ATZ1	reset modem and recall user profile 1.
AT&C0	assume data carrier always present.
AT&C1	track presence of data carrier.
AT&D0	ignore DTR signal.
AT&D1	go to the command state when an ON-to-OFF transition on DTR occurs.
AT&D2	hang up and go to the command state when an ON-to-OFF transition on DTR occurs.
AT&D3	reset when an ON-to-OFF transition on DTR occurs.
AT&F	recall the factory settings as the active configuration.
AT&G0	do not transmit guard tone.
AT&G1	transmit 550 Hz guard tone.
AT&G2	transmit 1800 Hz guard tone.
AT&J0	RJ11, RJ41S or RJ45S telco jack (no A/A1).
AT&J1	RJ12 or RJ13 telco jack (A/A1 switching).
AT&M0	(used interchangeably with AT&Q0, below).
AT&M1*	(used interchangeably with AT&Q1, below).
AT&M2*	(used interchangeably with AT&Q2, below).
AT&M3*	(used interchangeably with AT&Q3, below).
AT&P0	set pulse dial make:break ratio to 39:61 (North America).
AT&P1	set pulse dial make:break ratio to 33:67 (rest of world).
AT&Q0*	set data transfer format to character asynchronous (start/stop).

AT&Q1*	set synchronous mode 1.
AT&Q2*	set synchronous mode 2.
AT&Q3*	set synchronous mode 3.
AT&Q4	set synchronous mode 4 (AutoSync).
AT&R0*	in synchronous mode, make CTS track RTS using register S26 time delay.
AT&R1*	in synchronous mode, ignore RTS, CTS remains ON throughout the connection.
AT&S0	assume presence of DSR signal.
AT&S1*	track presence of DSR signal.
AT&T0	terminate any test in progress and return to normal operation.
AT&T1	initiate local analog loopback test.
AT&T3	initiate digital loopback of received data to transmitter.
AT&T4	enable response to requests for remote digital loopback from other modem.
AT&T5	disable response to requests for remote digital loopback from other modem.
AT&T6	request remote digital loopback test and initiate if other modem responds.
AT&T7	request remote digital loopback test with self-test pattern.
AT&T8	initiate local analog loopback test with self-test pattern.
AT&V	view active configuration, user-defined profiles and stored numbers.
AT&W0	save storable parameters of active configuration as user profile 0.
AT&W1	save storable parameters of active configuration as user profile 1.
AT&X0	modem provides bit-synchronous transmit clock signal (internal timing).
AT&X1*	modem accepts bit-synchronous transmit clock signal from DTE (external timing).
AT&X2	modem uses receive bit-synchronous clock as transmit clock signal (loopback timing).
AT&Y0	recall user profile 0 on power-up.
AT&Y1	recall user profile 1 on power-up.
AT&Zn=x	store phone number “x” in location “n” (n = 0 to 3).

The following is a list of the Smartmodem™ 2400 and 2400B “S” Registers. Again, **bold** is used to distinguish 1200 and 1200B registers. In some modems of early manufacture, the range of register **S7** was 1-30 or 1-55 sec. S16 is not available in 2400 modems because the test modes are handled by the added AT&Tn commands.

Register	Description	Range
S0	Number of ring cycles before automatic answer.	0-255
S1	Ring cycle count (incremented at end of each ring cycle).	0-255
S2	ASCII code for escape sequence character.	0-127
S3	ASCII code for carriage return character.	0-127
S4	ASCII code for line feed character.	0-127
S5	ASCII code for backspace character.	0-32,127
S6	Wait time prior to blind dialing.	2-255 sec
S7	Wait time for carrier or dial tone.	2-255 sec
S8	Pause time for comma modifier in dial string.	0-255 sec
S9	Carrier Detect response time.	1-255 1/10 sec
S10	Delay from carrier loss to hanging up.	1-255 1/10 sec

Register	Description	Range
S11	Duration and spacing of DTMF tones.	50-255 ms
S12	Escape sequence guard time.	20-255 1/50 sec
S13-15	Reserved.	
S16 *	Test modes.	0, 1, 2 & 4
S17	Reserved.	
S18	Test timer.	0-255 sec
S19-24	Reserved.	
S25	DTR change detect time.	0-255 1/100 sec
S26	RTS to CTS delay.	0-255 1/100 sec

The following is a list of the Smartmodem™ 2400 and 2400B Result codes. Only the CONNECT 2400 code is not supported by the Smartmodem™ 1200 and 1200B.

No.	Words	Description
0	**OK**	Command executed.
1	**CONNECT**	Connection at 0 to 300 bit/s.
2	**RING**	Ring signal detected.
3	**NO CARRIER**	Carrier signal not detected or lost.
4	**ERROR**	Invalid command, error in command line, command line exceeds buffer or invalid checksum.
5	**CONNECT 1200**	Connection at 1200 bit/s.
6	**NO DIALTONE**	Dial tone was not detected.
7	**BUSY**	Busy signal returned from remote end after dial.
8	**NO ANSWER**	No silence detected when dialing a system not providing a dial tone.
10	CONNECT 2400	Connection at 2400 bit/s.

Many manufacturers have made their own additions to the Hayes Smartmodem™ command set to support their own added value features.

APPENDIX B: Source List of Parts, Services and Test Equipment

In this appendix, we present a list of suppliers of components, test equipment and services for data communications applications. We have often been asked for this information by our customers who are new to modem design. This listing should make it easier for you to obtain parts and services which are peculiar to modems. However, Silicon Systems cannot accept ultimate responsibility for the suitability to your particular application of the products of the companies named. Note also that the lists are by no means exhaustive; your existing suppliers may well have suitable offerings including products or services not mentioned here.

B1: COMPONENTS

Crystals and Crystal Oscillators

Crystek Corporation, Florida (813) 936-2109

M-tron Industries, Inc., South Dakota (605) 665-9321

SaRonix, California (415) 856-6900

Telephone Line Coupling Transformers

Microtran Company, Inc., Valley Stream, New York (516) 561-6050

Midcom, Inc., South Dakota. (605) 886-4385

Prem Magnetics Incorporated, McHenry, Illinois (815) 385-2700

Tamura, Carson, California (213) 532-1790

TDK Corp. of America (312) 803-6100

Modular Data Access Arrangements

Silicon Systems, Inc., (714) 731-7110

Cermetek Microelectronics, Sunnyvale, California (408) 752-5000

Clifford Electronic Technologies, California (408) 988-4668

Data Trek, Elkhart, Indiana (219) 522-8000

Relays for Telecommunications

American Zettler, California (714) 660-1670

Aromat Corporation, Mountainside, New Jersey (201) 232-4260

C.P. Clare Division, General Instr. Corp., Chicago, Illinois (312) 262-7700

Fujitsu Components of America, Inc., Lake Bluff, Illinois (312) 295-2610

NEC Electronics inc., California (800) 632-3531

Stetron International, Inc., Buffalo, New York (716) 854-3443

Solid-State Relays

AT&T Microelectronics, Reading Works, Pennsylvania (215) 939-7011

Theta-J, Wakefield, Massachusetts (617) 246-4000

Surge Arresters (Surge Protection Devices)

C.P. Clare Division, General Instr. Corp., Chicago, Illinois (312) 262-7700

Stetron International, Inc., Buffalo, New York (716) 854-3443

World Products, Inc., California (707) 996-5201

EMI Control Components

Fair-Rite Products Corp., Wallkill, New York (914) 895-2055

B2: TEST EQUIPMENT

Spectrum Analyzers

Hewlett Packard

Telephone Line Simulators

AEA Electronic, Ltd., Ontario, Canada (613) 838-2554
AEA Electronic, Ltd., California (408) 263-2600
Processing Telecom Technologies (PTT), Alabama (205) 837-7880
Telecom Analysis Systems, Inc., (TAS), Eatontown, New Jersey (201) 544-8700

Bit Error Rate Test Sets

Phoenix Microsystems, Huntsville, Alabama (205) 881-2173

Part 68 Workstation

Compliance Design, Inc., Massachusetts (508) 264-4208

B3: SERVICES

FCC Parts 68 and 15 Testing

Dash, Straus & Goodhue, Massachusetts (508) 263-2662

UL and other Safety Approvals testing

Standards Approval Group, Ontario, Canada (416) 890-2800

Telecommunications Product Design for PSTN

Patton and Associates, Arizona (602) 934-5458
Design for EMI Compliance
The Keenan Corporation, Florida (813) 544-2594

B4: TEST LABORATORIES

Eastern U.S.

Certelecom, E. Syracuse, New York (315) 437-1023
Custom Electronics, Concord, New Hampshire (603) 736-9061
Dash, Straus, R. Goodhue, Boxborough, Massachusetts (508) 263-8162
Hyak Associates, Springfield, Virginia (703) 451-1188
MET, Baltimore, Maryland (301) 354-2200
R & B Enterprises, W. Conshohocken, Pennsylvania (215) 825-1960
RETLIF, Ronkonkoma, New York (516) 737-1500
Underwriters, Melville, New York (516) 271-6200

Southern U.S.

Continental Testing Labs, Fern Park, Florida (407) 831-2700
Southwest Research Institute, San Antonio, Texas (512) 522-3631
Testmark Labs, Lexington, Kentucky (606) 223-3061
Timco, Miami, Florida (305) 255-2424
U.S. Technologies, Roswell, Georgia (404) 998-9454

Midwest U.S.

Amador Corporation, Almelund, Minnesota (612) 583-3322
Elite Electrical Engineering, Downers Grove, Illinois (709) 495-9770

Western U.S.

AAP Laborotories, Mountain View, California (415) 967-7579
Clifford Electronics, Santa Clara, California (408) 988-4668
Communications Certification Laboratory, Salt Lake City, Utah (801) 972-6146
Compatible Electronics, Brea, California (714) 579-0500
GMC Associates, Chatsworth, California (818) 998-9171
Northwest Phone Service, Renton, Washington (206) 235-7150
Rockford Engineering, Sunol, California (415) 862-2944
D. Reginald Tibletts, PE, Moraga, California (415) 376-2212

Canada

Aprel, Nepean, Ontario (613) 727-0334
Bell Northern Research, Ottawa, Ontario
Certelecom, Ottawa, Ontario (613) 737-9680
Electronic Test Centre, Edmonton, Alberta (403) 450-5370
Marshall Laboratory, Rexdale, Ontario (416) 746-2671
Standards Certification Lab, Concord, Ontario (416) 669-6685

Asia

Akzo Japan, Ltd., Tokyo 102, Japan
ERSO, Chu-Tung, Ssin-Chu, Taiwan
JMI, Tokyo, Japan
Kansai Electronic Center, Kita-Ku, Osaka 530, Japan
Training Research, Taipei, Taiwan

B5: REFERENCE MATERIALS AND BOOKS

The Theory and Practice of Modem Design, John A. C. Bingham, Wiley, ISBN 0-471-85108-6.

Data Set 212A Interface Specifications, Bell System Data Communications TECHNICAL REFERENCE, PUB 41214, January 1978.

Data Communication over the Telephone Network, Recommendations of the V Series, CCITT.

Code of Federal Regulations, Part 68, Connection of Terminal Equipment to the Telephone Network, Federal Communications Commission, last revised October 1st, 1988.

APPENDIX C: Glossary of Terms

ASCII
American Standard Code for Information Interchange. This is the USA version of the ISO (International Standards Organization) 7-bit code. The letters of the alphabet (upper- and lower-case), the numbers, punctuation and various control functions are all assigned unique 7 bit codes. In data transmission systems, an eighth bit, the parity bit, is often added to the code.

asynchronous
In general, an event is asynchronous if it can happen at any time, i.e., its occurrence is not related to a clock or timebase. An asynchronous data transmission system can accept and pass digital data in which the transitions between binary states (one and zero) occur at any time, up to a maximum rate. Modems using the Bell 103 or CCITT V.21 and V.23 transmission standards operate asynchronously. Medium- and high-speed modems, however, achieve their effectiveness in part by using synchronous transmission and cannot accept truly asynchronous data. Examples of such modems use the Bell 212A, CCITT V.22, V.22bis and V.32 standards. Fortunately, the common usage of the term "asynchronous" with reference to data transmission is a contraction of "character-asynchronous," also known as start / stop data. In this case, the character (small group of data bits) may begin at any time but the changes from one bit to the next within the character occur at closely defined intervals. The CCITT recommends certain procedures for sending such data over synchronous modems. See start / stop for more information.

autobaud
The generally used term for automatically detecting the bit rate of a start / stop (character asynchronous) communication format by measuring the length of the start bit of the first character transmitted. Some modems extend this to additionally determine the parity in use by stipulating that the first two characters from the DTE should be "AT." The word autobaud comes from a popular misuse of the incorrect term "baud rate" to mean bit rate.

baud
This is the unit of measure for the modulation rate of a modem, in other words, the rate at which the characteristics of the line signal are changed to represent data. For example, the modulation rate of a V.22bis modem is 600 baud and each "baud" contains 4 bits of information, thus 2400 bit / s. Baud is by far the most misused data communications term, it is often used in place of bits-per-second (bit / s) as in "V.22bis modems are 2400 baud." Even when used to express modulation rate, it is frequently combined with the word rate, as in "the baud rate of V.22bis is 600." This is similar to saying "the foot height of the Washington Monument is 555."

bit
Contraction of binary digit, the smallest unit of the binary code in which digital data is represented. A bit may have one of only two values, referred to as 1 and 0. Digital information of any complexity may be coded as an ordered sequence of bits in the same way that written information is coded as an ordered sequence of letters of the alphabet.

buffered
Data transfer mode in which data from the DTE is not directly sent over the telephone line but is first held in a temporary storage area (buffer) inside the modem. Similarly, data received from the remote system is held in a buffer before being passed to the DTE. This technique enables the data rate between the DTE and the modem to be different from the rate at which data is sent between modems. The speed disparity is absorbed by the filling and emptying of the buffer. If the buffer approaches fullness, then the modem must be able to stop the flow of data coming in before it fills up completely and data is lost. See "flow control" for further information.

byte
Small ordered group of bits, now generally accepted to be eight in length. Methods in use for representing the alphabet, numbers, punctuation, etc., in binary form use eight or fewer bits for each "character" so that the storage and manipulation of data in bytes, or multiple bytes, has become almost universal.

carrier, carrier signal
Telephone lines pass only a range of frequencies associated with the human voice. In order to send digital data over such a line, a modem generates a carrier signal at a frequency in this range. The data is sent by "modulating" this carrier, which means changing its frequency, phase and / or amplitude to represent a particular piece of data or data "symbol." The receiving modem "demodulates" the carrier by determining these characteristics of the carrier from moment to moment and reconstructing the data that each carrier state represents.

compressed, compression
Some types of digital data are coded in a way that does not make the most efficient use of the number of binary bits occupied. Examples are text or program source files which are made up of letters, numbers, punctuation and formatting characters. In ASCII, each character is given a seven bit code but a wasted eighth bit is often added to pad the length out to one byte. By using variable length codes such that frequently occurring characters are represented by fewer bits than rarely occurring characters, it is possible to re-code such data to use far fewer bits. This is known as compression and the compressed data can be stored in a smaller space and transmitted in less time over a data communication link. Modems providing compression accept data in a standard code such as ASCII, re-code the data for transmission and reverse the process at the other end. The result is

that data is sent faster than would be the case if the bits of the original code were sent at the modem bit rate, but this occurs transparently to the user. Speed improvements of a factor of two or more are achievable using sophisticated recoding algorithms on text data. Some data such as computer binary codes or graphics do not benefit from compression because all codes occur with approximately equal frequency. Compression must operate within a data protection scheme (see protected) because the effect of changing bits in variable length codes can be far more serious than with fixed length codes.

data link, data link rate

The data link is the connection of one modem to another over a telephone circuit. The data link rate is the rate at which data bits are moved from modem to modem over the telephone line. The rate depends on the modulation standard in use by the modems, i.e., V.22, V.22bis, etc. This may not be the same as the bit rate at which the DTE communicates with the modem or even the effective data throughput from DTE to DTE. The communications processor of the modem frequently offers features which isolate the DTE from the actual link data rate and provide buffering, error protection and compression.

DCE, data circuit-terminating equipment

In a data communications system, the equipment that converts digital data from a DTE into a form suitable for sending to another DCE. The other DCE converts it back into its original form and presents it to another DTE. Examples of a DCE are a modem or just a cable specially wired to interconnect two DTEs (a null-modem cable). In general, something is a DCE if it outputs data on the receive data pin (RXD, circuit 104) and accepts data on the transmit data pin (TXD, circuit 103) of the V.24 (EIA232D) connector and otherwise conforms to CCITT recommendation V.24 as a DCE.

direct

In direct data transfer mode, the DTE data lines are connected directly to the modulator and demodulator part of the modem. The communications processor, if one is present, is bypassed. The DTE data rate must now be the same as the data link rate and the result is as if the local DTE were cabled directly to the remote DTE. If the telephone line is noisy and causes errors in the received data, these will be passed to the DTE. This mode is useful where the DTE provides its own error protection and is the only mode available if the DTE uses bit-synchronous data format to communicate with the modem.

dotting, double dotting

The term "dotting" was coined by Bell to describe a data pattern consisting of alternate marks and spaces. The CCITT uses the full description of "alternating binary ONES and zeros" on first needing this idea in a recommendation, but then abbreviates this to "reversals." By extrapolation, "double dotting" has come into use to refer to the data pattern which is used in V.22bis to indicate 2400 bit/s capability. The correct CCITT term is "S1," which if not very descriptive, is at least concise. The full description is "Unscrambled double dibit 00 and 11 at 1200 bit/s for 100 ±3ms." This last is too long to say very often, but must be understood for a V.22bis modem to function properly. If the pattern 00110011, etc. is transmitted without making sure that the pairs of ZEROs and ONES are coded in the same symbol, the resulting signal will not appear to other V.22bis modems as an S1.

DTE, data terminal equipment

In a data communications system, the equipment that produces the digital data to be sent and/or accepts the digital data received. Examples of a DTE are a terminal, computer or a personal computer. In general, something is a DTE if it outputs data on the transmit data pin (TXD, circuit 103) and accepts data on the receive data pin (RXD, circuit 104) of the V.24 (EIA232D) connector and otherwise conforms to CCITT recommendation V.24 as a DTE.

EIA interface, EIA232D, RS232C

The logical, electrical and physical characteristics of the connection between a DTE and a modem is set out in EIA specification 232D. Previously this has been known as RS232C. The logical characteristics are essentially similar to those specified in CCITT recommendation V.24, the electrical characteristics to those in V.28 and the physical to ISO 2110.

flow control

The process of suspending the transmission of data from a sub-system in response to a command from another subsystem when the second determines that it cannot accept further data. A modem may flow control a DTE if the data rate from the DTE to the modem exceeds the data link rate and the buffers of the modem approach being full. This gives the modem time to catch up and empty out the buffers somewhat before allowing the DTE to continue. One modem may flow control another if its DTE is unable to accept data at the rate it is arriving over the link. Various methods of flow control exist. Where text data using ASCII is being transmitted, the XOFF and XON characters may be sent to the source of data to request that it cease and resume transmitting, respectively. For binary data transfer, where binary patterns may appear to be XOFF or XON characters, hardware flow control may be used by redefining the operation of certain signals in the V.24 interface to the DTE.

full-duplex

A data communication system capable of passing data between two points in both directions simultaneously. Modems achieve full-duplex operation in various ways. Four-wire modems employ a wire pair for transmission in each direction. Two-wire modems, such as dial-line modems, can divide the available frequency range into two and use separate carriers for each direction. Echo-cancelling modems are able to use the full frequency range by

subtracting signals due to echoes of their own transmission from the signals from the other modem. Some modems use a half-duplex data link but, by changing the direction of transmission frequently and using data buffers, give the impression to the DTE of being full-duplex. This is known as pseudo-full-duplex.

guard time
In Hayes™ compatible modems, a time period used to qualify the exit code to reduce the likelihood of an undesired escape to command mode. The exit code is entered from the DTE and causes the suspension of data transfer mode to allow access to command mode without the call being disconnected. The exit code character must be entered three times with a period of at least the guard time separating the first from any preceding character entered. The second must be entered within the guard time from the first and the third similarly from the second. If, after the third exit character, no further characters are entered for a period equal to the guard time, then the escape to command mode will take effect. Hayes has patents covering this application.

guard tone
In CCITT Recommendations V.22 and V.22bis, guard tones may optionally be transmitted along with the data signal from the answering modem. A single frequency of either 1800 Hz or 550 Hz is used and the data signal power must be reduced to keep the overall energy level the same as for transmission without guard tone. The purpose of the guard tone is to prevent the high-band data signal from interfering with the operation of billing apparatus in certain countries.

half-duplex
A data transmission system which passes data between two points in only one direction at a time. If data is to be passed the other way, then the transmitting modem must go silent and become the receiving modem and the original receiving modem must start transmitting. This is known as "turnaround." By turning around frequently and in a short time, some half-duplex modems are able to appear full-duplex to the DTE and are known as pseudo-full-duplex.

modem
Contraction of the words modulator and demodulator, referring to data communications equipment which modulates the data to be transmitted onto a carrier signal and demodulates at the other end to recover the data. The most common type of modem uses carrier signals in the frequency range used for voice communication over the telephone network and thus permits digital data to be sent over telephone circuits.

modulation
The process of varying the characteristics of a carrier signal in order to impress upon it some information or data. The purpose of this is normally that the carrier signal carrying the data may be stored or transmitted by some means which is not suitable for the original data. Voice band modems employ as a carrier one or more frequencies in the range passed by the telephone network. The characteristics varied to represent digital data are the frequency, phase or both amplitude and phase.

non-volatile storage
Storage area that has the same basic properties as random access memory, except that data is retained even if power is removed. This can be achieved by including a small battery along with a RAM component of very low power consumption or by using an EEPROM.

off-hook
By analogy with the normal household telephone, a modem is off-hook when it is using the telephone line to make a call. This is similar to raising the telephone handset, or taking it off the hook. Going off-hook is also known as "seizing the line."

on-hook
By analogy with the normal household telephone, a modem is on-hook when it is not using the telephone line. As with a telephone where the handset is on the hook, the line may be used by other equipment to make a call. Going on-hook is also known as "dropping the line."

parity bit
A bit associated with another group of bits to permit rudimentary error detection. The bit carries no information, but makes the count of binary ONES in the group as a whole either even or odd. The receiver, knowing whether the count should be even or odd, can tell if a single bit has been received in error. A parity bit may be added to the seven bit ASCII codes which represent text and in start / stop format is transmitted after the last useful bit and just before the stop bit. Because it is not possible to correct the error or detect multiple bit errors, parity is rarely used in earnest in data communications.

protected
Data transfer mode in which the modem is able to detect errors in received data, request retransmission by the sending modem and thus ensure that only correct data is passed to the DTE. Data is grouped into blocks of characters and sent with special framing characters and extra information to allow the integrity of the data to be checked and the block to be identified. If errors are detected, the data is not passed to the DTE, and a request is sent in a block going the other way, that the block in error be sent again. Only when correctly received does data reach the DTE. For protected mode to be effective, the modem must buffer the data and be able to flow control the DTE (see "flow control") to suspend the input of new data until previous data has been received without error at the remote end.

random access memory, RAM

Properly called read / write memory, this constitutes a data storage area the contents of which can be modified during the normal operation of the equipment. If power is removed, all stored data will be lost and the contents will be garbage on re-applying power. However, see non-volatile storage.

read-only memory, ROM
A data storage area in which the data is fixed into the component at manufacture. Removing power from the equipment has no effect on the data stored and the data may not be modified in the field.

ringer equivalence number, REN
This is a number that the FCC assigns to approved telecom equipment that measures how much load it places on the network during ringing. In the U.S.A. you can connect telephones, modems, FAX machines, etc. in parallel to the same telephone line only as long as the sum of their ringer equivalence numbers is less than five. Most countries have a similar regulating system in force, although the methods used to arrive at the number vary widely.

RS232-C
See EIA232D.

start bit
In start / stop (character-asynchronous) data transmission format, the bit of value ZERO that is transmitted prior to the group of useful data bits. The receiving system uses the transition from the ONE state of the stop bit or idle line to the ZERO state of the start bit to synchronize on the beginning of the character. It looks for the first data bit one-and-a-half bit times after the transition and for subsequent bits at one bit time intervals thereafter. Thus, it samples at the center of each bit and can tolerate some drift of the bits away from their nominal positions before the data is improperly received.

start/stop
Also known as character-asynchronous or (incorrectly) just asynchronous, this is a data format in which each character may occur at any time, but within the character the timing of individual bits is well defined. When no character is to be sent, the signal idles at the ONE state. Each character is framed by a start bit of value ZERO which precedes it and a stop bit of value ONE which follows it. Using the ONE-to-ZERO transition at the beginning of the start bit, the receiver is able to synchronize on each character individually. Thus, although the duration of each bit must be known to within a few percent, any difference in the rate at which the bits of the character are transmitted and the rate at which the receiver samples them is cleared away on each new character. Because timing error does not accumulate, transmitter and receiver can use independent timing sources and it is not necessary to send a timebase or clock along with the data. The simpler wiring that results together with the ease with which characters are identified makes start / stop a most popular data transmission format.

stop bit
In start / stop (character-asynchronous) data transmission format, the bit of value ONE that is transmitted following the group of useful data bits. The presence of this bit ensures that the signal is returned to the ONE state for at least one bit period so that the receiver can resynchronize on the next character using the transition to ZERO when the start bit occurs.

synchronous
A synchronous data transmission system uses a closely defined clock or timebase to apply new data to the telephone line at regular intervals. The receiving end recovers this clock from the signal and, knowing when to expect new data to arrive, is better able to identify each piece of data. This type of transmission is therefore more able to pass data correctly in the presence of noise and distortion on the telephone line than an asynchronous system. Also, it is possible to make each piece of data (or data symbol) represent several bits of information, thus achieving higher transmission rates. To make use of a synchronous data transmission system, the DTE must provide and accept data at a very precise rate, normally within 0.01% of the nominal value. The modem provides "bit clocks" to facilitate this and the DTE must provide a new data bit on each clock tick. Fortunately, the efficiency of a synchronous transmission system is available to DTEs that use start / stop (character asynchronous) data formats in various ways. Many modems incorporate a communications processor which re-formats the characters into larger groups of data bits (blocks) which are transmitted synchronously and at the same time checks the correctness of the received data and retransmits data in error. The CCITT also specifies a method for converting start / stop characters into a bit-synchronous data stream for transmission and reconstructing the characters at the receiver. For this to work, the rate of the bits that make up the character (the intra-character signaling rate) must be close to the synchronous transmission rate. A rate of 2.5% lower than nominal is permitted and either 1% or 2.3% higher.

V.24
see EIA232D.

working memory
In a Hayes compatible modem, the set-up parameters in use are held in a storage area called working memory. Because this area is random access memory, the contents are lost if the modem power is turned off. Commands are available to save the set-up in non-volatile storage prior to removing power so that they will automatically be restored into working memory when power is next applied.

SSI 73D2248/73D2348

DESIGN MANUAL

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Section 1

INTRODUCTION

1 INTRODUCTION

1.1 OBJECTIVE

The Silicon Systems SSI 73D2248 Modem Device Set is intended for use in developing communications products. By taking advantage of the "base" hardware and software design of the 73D2248 Evaluation System described in this manual, the customer avoids having to develop a modem design "from scratch" and reduces the time to market. The basic 73D2248 design implements the AT command set as well as V.22bis, V.22, V.21, Bell 212A, and Bell 103 modes of operation. MNP2-5, V.42, V.42bis and V.23 are optionally available. This manual is intended to serve as a guide to the modem designer wishing to enhance the basic 73D2248 functionality.

1.2 USE OF THIS DOCUMENT

It is assumed that the reader has basic familiarity with microprocessors, firmware and data communications. Prior experience with modems is not assumed but would be useful, particularly if extensive modifications to the basic 73D2248 design are required.

In addition to the information presented in this manual, it is suggested that the reader obtain data sheets for all the parts used in the basic design. Silicon Systems also publishes the "K-Series Modem Design Manual" which contains a great deal of application information on the K-Series devices. This manual can be obtained from Silicon Systems Sales Offices.

The firmware for the 73D2248 was assembled using the Intel MCS-51 Macro Assembler, version 2.2. If any software changes are anticipated, a copy of this program should be obtained. Note that since much of the code pertaining to data compression and data correction is supplied only in object code form, porting the code to a different assembler is only possible if that assembler is compatible with Intel's object code format.

Although the 73D2248 is not certified to be directly connected to a phone line, it was designed to meet FCC Part 68 requirements. If the modem being designed is for use outside the U.S.A., requirements for direct connection to the telephone network in the countries of interest should also be obtained.

1.3 LANGUAGE AND TERMINOLOGY

To a large extent, telecommunications and, by extension, data communications, has developed terminologies distinct from the rest of the electronics engineering community. The lack of worldwide standards until recent years has also hampered the adoption of widely accepted terms. North America, dominated by the earlier influence of Bell Telephone, has developed terminology which differs from that now used by the CCITT, the industry group responsible for setting international standards. As international data exchange grows in importance, the CCITT can be expected to grow in influence, even in North America. For this reason we have chosen to use the CCITT terminology in most cases. There will be some exceptions to our use of CCITT terms. For example, "mark" and "space" are much shorter than "binary one" and "binary zero" and these have been used where appropriate. Also, we may use Bell terminology when discussing Bell specifications. The Bell terminology is so pervasive that it is used by default in areas where the CCITT has yet to venture.

1.4 REGISTERED TRADEMARKS

Throughout this manual, we wish to acknowledge the following: Hayes, Hayes AT, Smartcom and Smartmodem are registered trademarks of Hayes Microcomputer Products; IBM, IBM PC, IBM AT, and PS / 2 are registered trademarks of IBM; MNP is a registered trademark of Microcom; Tri-state is a registered trademark of National Semiconductor Corporation; MCS-51 and 8052 are registered trademarks of Intel.

Section 2

USER'S MANUAL

2 USER'S MANUAL

2.1 "QUICK START"

This section is intended to provide just enough information to allow one to set up and operate the 73D2248 Demo Board in its basic modes. The modes supported are: Bell 103 (300 bit/s), Bell 212 (1200 bit/s),V.22 (1200 bit/s),and V.22bis (2400 bit/s). This modem also supports automatic speed buffering, V.42, V.42bis, and MNP 2-5 protocols.

Preparing Your Computer or Terminal

In order to use the 73D2248 modem you must have:

1. Either a terminal with RS-232 serial capabilities or a computer with an RS-232 serial port and communications software. Choosing a terminal or computer/software is a personal choice and is beyond the scope of this document.
2. An RS-232 cable. Use a cable with all 25 wires connected to avoid problems with flow control.
3. An RJ-11 phone cable.

Connecting the 73D2248 Demo Board to Your Computer

Make sure your computer or terminal and the 73D2248 modem are turned OFF before proceeding.

Connect the modem power supply cable to the power connector in the rear of the 73D2248. Make sure the power switch is in the OFF position (OUT). Plug the power supply into a wall outlet (110V 60 Hz AC).

Connect the RS-232 cable between your computer and the 73D2248 modem.

If the demo board has an FCC certification label, you may plug the RJ-11 phone cable into the LINE connector in the rear of the 73D2248 modem. Plug the other end of the cable into a phone wall outlet. Otherwise the RJ-11 line connection must be made through an appropriate line simulator capable of providing 20-100 mA loop current to the modem.

Optionally you may plug a phone into the PHONE connector in the rear of the 73D2248 modem. This is not required to operate the modem.

Setting up your computer or terminal

After connecting your computer or terminal to the 73D2248 modem, turn on your computer or terminal and load any communications software you will be using.

Turn on the 73D2248 modem by pushing in the power switch on the front panel of the modem.

Set your communications software or terminal to a speed of 2400 bit/s. For now do not exceed 2400 bit/s.

You should also determine the flow control options your software or terminal may require. Set the Flow Control to RTS/CTS. If your terminal does not support this, you may use XON/XOFF. If your terminal does not support flow control you will not be able to run the modem in protocol mode or above 2400 bit/s.

Setting up the Defaults

The initial state after power-up is the COMMAND MODE. At this time commands may be sent to the modem from your terminal.

All communications to set up the modem are done using "AT" commands. All commands are preceded by "AT." Most commands sent to the modem are one letter optionally followed by a number in the range of 0-255.

In order to set the factory default setting you must type:

AT&F&W <CR>

The modem should respond with:

OK

The commands you just sent to the modem are as follows:

&F Tells the modem to use the factory defaults

&W Tells the modem to store the current settings in its protected non-volatile memory.

To set your flow control options to RTS / CTS, type the following:

AT&K3 <CR>

If you are using XON / XOFF for flow control, instead type:

AT&K4 <CR>

if you do not have flow control then type:

AT&K0 <CR>

Now set the modem into asynchronous, no protocol mode by typing:

AT&Q0 <CR>

Making your first connection

You must now have the phone number of another 2400 bit / s modem. To instruct the modem to dial that number, type:

ATDTnnn <CR> (nnn = the telephone number)

The modem will attempt to make a connection. If the modem is successful it will respond:

CONNECT nnn (nnn = connect speed)

If nnn does not equal the terminal speed then change the speed of your terminal to the displayed connect speed.

If the connect attempt failed, you will get the following response:

NO CARRIER

If you get this response, the connect failed. Check the number and try again.

If the connect message is displayed, you will be in the DATA MODE. You can now exchange data with the remote modem.

Online Command Mode

After a connection has been established and you have finished sending data or if you would like to change one of the parameters of the modem, you must enter the ONLINE COMMAND MODE. To do this you should stop sending data for one second and type at a steady rate:

+++

Wait one second; the modem should respond with:

OK

If the modem does not respond, repeat the above but type a little faster.

Once the modem responds to the +++ input, you are in the ONLINE COMMAND MODE. While in this mode, the modem puts the line in an IDLE state so you can type commands to control the modem settings.

To return to DATA MODE type:

ATO <CR>

You should get the response:

CONNECT nnn (nnn = connect speed)

Terminating the Call

In order to terminate the call and return to COMMAND MODE you must go to ONLINE COMMAND MODE (see “Online Command Mode” above) and type:

ATH <CR>

The modem should respond with:

OK

You have now terminated the call and are back in the initial COMMAND MODE.

Making a V.42 call

For this exercise, set your DTE speed to 9600 bit/s.

To make a V.42bis call, you should get the phone number of a V.42bis modem and type the following commands:

AT&Q5W1&K3 <CR>

The above command instructs the modem as follows:

&Q5 Protocol mode. See protocol operation section below.

W1 Extended result codes.

&K3 RTS/CTS flow control. **IF YOUR TERMINAL DOES NOT SUPPORT THIS OPTION, USE &K4 (XON/XOFF).**

The modem should respond with:

OK

Next send the following command:

ATS36=7S46=138S48=7 <CR>

The above command instructs the modem as follows:

S36=7 If negotiation fails, try MNP and automatic speed buffering.

S46=138 Enable Compression

S48=7 Enable V.42

Now proceed with dialing...

ATDTnnn <CR>

If the modem you called can handle V.42bis or MNP2-5 the 73D2248 will make a protocol connection. If not the modem will fall back to automatic speed buffering.

Because we enabled extended result codes (W1) the modem will report the progress of the negotiation:

CARRIER nnn (nnn = carrier line speed)

PROTOCOL xxx (xxx = protocol type)

CONNECT bbb (Connect (DTE) Speed)

To terminate the call, see the section on terminating the call above.

Making an MNP only Connection

For this exercise, set your DTE to 9600 bit/s.

To make an MNP call, you should get the phone number of an MNP modem and type the following commands:

AT&Q5W1&K3 <CR>

The above command instructs the modem as follows:

&Q5 Protocol mode. See protocol operation section below.

W1 Extended result codes.

&K3 RTS/CTS flow control. **IF YOUR TERMINAL DOES NOT SUPPORT THIS OPTION, USE &K4 (XON/XOFF).**

The modem should respond with:

OK

Next send the following command:

ATS36=7S46=138S48=128 <CR>

The above command instructs the modem as follows:

S36=7	If negotiation fails, try MNP and automatic speed buffering.
S46=138	Enable Compression
S48=128	Force fall back option. In this case the fallback option is set to MNP.

Now proceed with dialing...

ATDTnnn <CR>

If the modem you called can handle MNP2-5 the modem will make a protocol connection. If not, the modem will fall back to automatic speed buffering.

Because we enabled extended result codes (W1) the modem will report the progress of the negotiation:

CARRIER nnn	(nnn = carrier line speed)
PROTOCOL xxx	(xxx = protocol type)
CONNECT bbb	(Connect (DTE) Speed)

To terminate the call, see the section on terminating the call above.

2.2 "AT" COMMAND SET

The 73D2248 firmware supports the Hayes AT command set which consists of three main sections:

1. Commands
2. Responses
3. S Registers

Originating and answering calls and setting up the various options are performed by sending one or more commands to the modem from the DTE. These commands are described in Section 2.2. Section 2.3 describes the possible responses to the commands, which may be in Terse (numeric) or Verbose (word) form. The S registers are storage locations which are used to provide storage for operating mode information. They may be written to or read from as described in section 2.4.

2.2.1 The AT Command Format

Each command follows the format below (with the exception of the A / command and the +++ command, which will be discussed later):

<AT><Command>{Argument}{=n}{More}<Enter>

Each element of the command line shown above is described below.

Note: Information in "angle" brackets <> must be included as part of the command line, while information in "curly" braces {} may or may not be necessary as part of the command line.

AT	This is the attention code to let the modem know that a command will follow. The AT may be in either upper or lower case letters. The modem uses this sequence of ASCII characters to determine the speed and parity of the DTE.
Command	A command consists of one letter or an ampersand followed by a letter.
Argument	Optional information that further defines the command.
=n	Used when setting a register. These registers are used to access certain 73D2248 operating parameters.

You may "string" commands together in one command line as long as the total length of the command line does not exceed 255 characters. The attention code, AT, is only required at the beginning of the command line. Therefore, the "more" command sequence follows the following format:

<Command>{Argument}{=n}

<Enter> This is the <Enter> or <Return> key on your computer's keyboard. Pressing <Enter> at the end of the command line will tell the modem to execute the command(s) in that command line.

For example, let's look at the command line.

AT DT 555-1234 ; <Enter>

Here, AT is the attention code; DT is the command to dial a number using the tone method; 555-1234 is the argument (a phone number); ";" is "more" (another command, this one instructing the modem to return to the command state after dialing); and <Enter> is the <Enter> key terminating the command line.

NOTE: If no argument is provided with a command that takes a numerical argument, an argument of zero is assumed. For example, the following commands are identical:

AT B <Enter> or AT B0 <Enter>

Also, for compatibility with earlier AT command formats, the &Z[n]=[x] command and the S=[n] dial string modifier can be issued in two different forms when referencing stored phone number 0. The following commands are identical:

AT &Z0=555-1234 <Enter> ATDs=0 <Enter>

AT &Z555-1234 <Enter>ATDs <Enter>

In the command descriptions below, r, n and x are used as variables and can have the values that are explained with the associated command.

"n...n" means that an item may be repeated as many times as necessary, as long as the entire command line does not exceed 255 characters.

NOTE: Although the command string is 255 characters in length, the stored dial string can only be 37 characters in length. See the "ATDS" command for more information.

2.2.2 A Answer

The A command causes the modem to immediately go on-line (off-hook) in the Answer mode and attempt to handshake regardless of the value of register S0. This command gives you a method of manually answering an incoming phone call.

2.2.3 A/ Repeat Last Command

The A / command causes the modem to re-execute the last command that was issued. For example, this command can be used to redial a number if the previous command was a dial command.

NOTE: A / and +++ are the only commands that are neither preceded by AT nor followed by <Enter>.

2.2.4 B[n] Bell or CCITT Operation

n = 0 or 1 (factory default = 1)

The B[n] command is used to select between Bell and CCITT protocols when originating a call at 300 or 1200 bit / s. The state of the B[n] command is ignored when the modem is operating at 2400 bit / s.

B0 Selects CCITT V.21 for 300 bit / s and CCITT for 1200 bit / s operation.

B1 Selects Bell 103 for 300 bit / s and Bell 212A for 1200 bit / s.

2.2.5 D[n...n] Dialing String

This command puts the modem into originate mode and instructs the modem to dial the phone number expressed by the string argument n...n. The number will be dialed with either tones or pulses depending on how the last number was dialed. On power up, this command will default to pulse dialing. (See the note in DT[n...n] command.) The allowable arguments for n...n differ for pulse and tone dialing; see the descriptions under DT[n...n] and DP[n...n].

DP[n...n] n = 0-9 , P T R ; @ ! W S=[n]

This command instructs the modem to dial the phone number expressed by the argument n...n using pulse dialing. (See the detailed description of the arguments under DT[n...n] below.)

DT[n...n] n = 0-9 A B C D * # , P T R ; @ ! W S=[n]

This command instructs the modem to dial the phone number expressed by the argument n...n using tone dialing.

In addition to 0-9 A B C D * #, which are the same as the keys on your phone, there are some special characters that can be included in a dialing string. They are called Dial String Modifiers, and they define how the phone number is to be dialed. These characters are P R T ; , @ ! W.

A-D * # The characters A B C D, and the symbols * and #, can be used only during tone dialing. They are typically used to access newer features of modern telephone systems.

P The modem pulse dials the digits that follow.

R The modem uses answer mode frequencies after dialing the number. This allows you to dial up an originate only modem. This character is only valid at the end of the dialing string.

T The modem tone dials the digits, characters, and symbols that follow.

; A ; (semicolon) causes the modem to go back into the Command State, allowing you to enter other commands while on-line. To do this, the ; must be the last character in the command line.

, When inserted into a dialing string, a , (comma) causes the modem to pause. The default time for the pause is two seconds, and can be changed by modifying register S8.

@ An @ (commercial "at") causes the modem to wait up to 30 seconds for a 5 second period of quiet before proceeding. This is often used to detect the end of a prerecorded message. The default wait time is 30 seconds, and can be changed by modifying register S7. Result Codes 7 and 8 will be reported regardless of which Result Code Set is selected.

! An ! (exclamation mark) causes a "hook flash." This simulates hanging up for 1/2 second and then reconnecting. It is typically used for transferring calls.

W Causes the modem to wait for a dial tone for a specified length of time before proceeding. The default is 30 seconds, and can be changed by modifying register S7. Result Code 6 will always be included regardless of which Result Code Set is selected.

S=[n] The S=[n] dial string modifier causes the modem to dial one of the four phone numbers previously stored in the modem non-volatile memory with the &Z[n]=[x] command.

NOTE: Although the command buffer is 255 characters in length, memory for stored numbers is limited to 37 characters per stored phone number (the "ATD" is not counted as part of the string). Because of this limitation, dialing strings should be limited to 37 characters.

2.2.6 E[n] Echo Commands On/Off

n = 0 or 1 (factory default = 1)

Causes the modem to either echo characters or not to echo characters while in the Command State.

E0 Command State Echo mode is OFF.

E1 Command State Echo mode is ON.

2.2.7 F[n] Full-Duplex/Local Echo

n = 0 or 1 (factory default = 1)

The F[n] command is not supported, i.e., Full-Duplex is always on.

F0 Half-Duplex; Returns ERROR.

F1 Full-Duplex; Returns OK.

2.2.8 H[n] On-Hook/Off-Hook Control

n = 0 or 1 (factory default = 0)

The H[n] command causes the modem to go off-hook or on-hook. (Going off-hook means that the modem "picks up" the telephone; going on-hook means that the modem "hangs up" the telephone.) The H[n] command applies only to asynchronous operation.

H0 Go On-hook (hang up).

H1 Go Off-hook (pick up the phone).

2.2.9 I[n] Identification and ROM Tests

n = 0 to 4

The I[n] command requests that the modem respond with certain product information.

I0 Returns product identification code.

I1 Returns the firmware ROM checksum number.

I2 Computes the firmware ROM checksum and returns with either an OK or ERROR result code message

I3 Returns firmware revision number.

I4 Returns copyright notice.

2.2.10 L[n] Speaker Volume

n = 0 to 3 (factory default = 2)

The L[n] command selects the speaker volume.

L0 Low volume.

L1 Low volume.

L2 Medium volume.

L3 High volume.

2.2.11 M[n] Speaker On/Off

n = 0 to 3 (factory default = 1)

The M[n] command turns the speaker ON or OFF.

M0 Speaker always OFF.

M1 Speaker ON until carrier is detected.

M2 Speaker always ON.

M3 Speaker goes ON after last digit is dialed; OFF after carrier is detected.

2.2.12 O[n] On-Line

n = 0 to 3

The O[n] command causes the modem to go on-line (off-hook) from the Command state. It can be used to go back on-line when the command state was entered by issuing the +++ escape sequence or turning DTR from ON to OFF with &D1 in effect. The O[n] command applies only to asynchronous operation.

O0 If you have returned to Command state from Data state without breaking a connection, the O0 command will return you on-line (Data state).

O1 Similar to O0, but also causes the modem to initiate an equalizer retrain sequence.

O2 Similar to O0 but enables the modem to respond to a remote request for retrain.

O3 Similar to O0 but prevents the modem from responding to a remote request for retrain.

2.2.13 P Pulse Dial

Causes the modem to pulse dial until tone dialing is selected or the modem is reset.

2.2.14 Q[n] Result Codes On/Off

n = 0 or 1 (factory default = 0)

The Q[n] command tells the modem to either report result codes or to remain quiet. Result codes acknowledge AT commands and call status events. Also refer to the V[n] and X[n] commands.

Q0 Report Result Codes.

Q1 Stay quiet.

2.2.15 S[r]? Show S-Register Value

r = 0 to 99

The S[r]? command requests the modem to report the current value of register [r]. These registers are used to set up various operating parameters of the modem as explained in Section 5. The value reported is in decimal notation.

S[r]=[n] Set S-Register Value r = 0 to 99, n = 0 to 255

The S[r]=[n] command allows you to set (modify) the value of any of register [r] to new value [n]. The value [n] is entered in decimal notation. See Section 5 for details of the S-Registers and their allowable range of values.

2.2.16 T Tone Dialing

Causes the modem to tone dial until pulse dialing is selected.

2.2.17 V[n] Select Result Codes Numbers/Words

n = 0 or 1 (factory default = 1)

The V[n] command instructs the modem to report either verbal (whole words) or numerical result codes. Also refer to the Q[n] and X[n] commands.

V0 Result codes reported as digits (reuse mode).

V1 Result codes reported as whole words (verbose mode).

2.2.18 W[n] Select Extended Result Code

n = 0, 1, 2 (factory default = 0)

The W[n] command determines which result codes will be used to describe the type of connection that was negotiated by the handshake.

W0 Do not return extended result codes (40-80). The message CONNECT followed by the data rate between the DTE and the modem will be sent to the DTE.

W1 The CONNECT message will report the DTE speed then enable the carrier and extended result codes.

W2 The CONNECT message will report the DCE speed. All extended result codes are disabled.

2.2.19 X[n] Select Result Code Set

n = 0 to 4 (factory default = 4)

The X[n] command selects normal or extended result code reporting and enables or disables advanced functions.

X0 Enable Result Codes 0-4.

X1 Enable Result Codes 0-5, 10-13.

X2 Enable Result Codes 0-6, 10-13.

X3 Enable Result Codes 0-5, 7, 10-13.

X4 Enable Result Codes 0-7, 10-13.

Result Code 0 = OK

Result Code 1 = CONNECT

Result Code 2 = RING

Result Code 3 = NO CARRIER

Result Code 4 = ERROR

Result Code 5 = CONNECT 1200

Result Code 6 = NO DIALTONE

Result Code 7 = BUSY

Result Code 8 = NO ANSWER

Result Code 10 = CONNECT 2400

Result Code 11 = CONNECT 4800

Result Code 12 = CONNECT 9600

If X0 or X1 modes are enabled, the modem will delay a number of seconds (determined by the value of register S6), not check for a dial tone, then dial.

When the X4 mode is enabled, Result Code 6 is disabled if the W command is in dialing string.

If the @ is used in the dialing string, and the X4 mode is enabled, result code 8 (NO ANSWER) is enabled. The modem dials, waits for a period of time (determined by the value of register S7) and during that wait looks for a five second period of silence. If the five seconds of silence are not detected, the modem reports the NO ANSWER Result Code.

When the X4 mode is used, result codes 7 and 8 are disabled when the @ command is in dialing string.

Dial string modifier W causes result code 6 to always be enabled.

Dial string modifier @ causes result codes 7 and 8 to always be enabled.

2.2.20 Y[n] Select Long Space Disconnect Option

n = 0 or 1 (factory default = 1)

The Y[n] command enables or disables long space disconnect. When enabled, the modem disconnects (goes off-line) if it receives a continuous BREAK (also known as a long space) from the remote modem for 1.5 seconds or more. It transmits a BREAK for 4 seconds prior to going off-line upon receiving an H0 command or detecting an ON to OFF transition of DTR if the &D2 option is selected. The Y[n] command applies to asynchronous operation only.

Y0 Long space disconnect disabled.

Y1 Long space disconnect enabled.

2.2.21 Z[n] Reset Modem

n = 0 or 1

The Z[n] command resets the modem and makes either stored profile #0 or #1 the active profile. Refer to the &W[n] command for details on storing user configuration profiles.

Z0 Reset modem and make the active profile = stored profile #0.

Z1 Reset modem and make the active profile = stored profile #1.

2.2.22 +++ Escape Command

During a data connection, the escape command (+++) or 3 “plus” keystrokes in sequence, returns you to Command state without terminating the data connection so you can enter AT commands. (Do not type AT before the pluses or <Enter> after them.)

You must wait for a period of time before and after typing the pluses. The length of this period is determined by the setting of register S12 and defaults to 1 second. The escape characters must be entered three times within one second of each other before they are recognized by the modem. The default escape character is the + (plus symbol, ASCII 43 decimal). Register S2 can be used to modify the escape character.

2.2.23 &C[n] Select Carrier Detect Option

n = 0 or 1 (factory default = 0)

The &C[n] command selects how the Carrier Detect (CD) signal is controlled.

&C0 CD forced ON.

&C1 CD ON in presence of valid carrier signal.

2.2.24 &D[n] Select Data Terminal Ready Option

n = 0 to 3 (factory default = 0)

The &D[n] command selects how the Data Terminal Ready (DTR) signal is used by the modem. Detection of a DTR state change (e.g., ON to OFF) requires that the new state persist for a period of time determined by the value of register S25 (factory default = 5 / 100 second).

&D0 Modem ignores DTR.

&D1 Modem assumes the Command State when DTR transitions from ON to OFF.

&D2 Modem goes on-hook (hangs up), disables the Auto- Answer mode, and assumes the Command State when DTR transitions from ON to OFF. Auto-Answer mode can be enabled by turning DTR back ON.

&D3 Modem is reset when DTR transitions from ON to OFF and loads the store configuration profile selected by the &Y[n] command.

2.2.25 &F Load Factory Defaults

The &F command replaces the current active configuration profile with the factory standard configuration profile stored in permanent memory. The &F command does not store the factory standard configuration profile in the modem non-volatile memory.

2.2.26 &G[n] Select Guard Tone

n = 0 to 2 (factory default = 0)

The &G[n] command selects which, if any, guard tones are to be generated. (Guard tones are not used in North America.)

&G0 No guard tones.

&G1 Select 550 Hz guard tone.

&G2 Select 1800 Hz guard tone.

2.2.27 &J[n] Auxiliary Relay Control

n = 0, 1

This command determines how the auxiliary relay is controlled.

&J0 Suitable for RJ-11, RJ-41S, or RJ-45S type phone jack. The auxiliary relay is never operated.

&J1 Suitable for RJ-12, or RJ-13 type phone jack; the A lead is connected to A1 lead while modem is off hook.

If &J0 is selected the auxiliary telco relay is opened. If &J1 is selected and the modem is off-hook, the auxiliary telco relay is closed, shorting A to A1.

2.2.28 &K[n] Select Flow Control Option

n = 0, 3, 4 (factory default = 3)

The &K[n] command is used to select the flow control method when the modem is operating in a speed buffered mode.

&K0 Local Flow Control Disabled.

&K3 RTS / CTS.

&K4 XON / XOFF.

2.2.29 &L[n] Dial Up/Leased Line option

n = 0, 1

The &L command instructs the modem to function in a leased line environment. The modem will not dial numbers or send answer tone. After receiving a D or A command, the modem goes to the originating or answering process. After handshaking, the modem tries to stay in the on-line state. If it loses carrier, it returns to the originating or answering process.

&L0 Select Dial up line operation

&L1 Select Leased line operation

2.2.30 &P[n] Select Make/Break Pulse Dial Ratio

n = 0 or 1 (default = 0)

The &P[n] command controls the ratio of pulse dialing off-hook (make) to on-hook (break) interval.

&P0 Select 39% / 61% make / break ratio (United States).

&P1 Select 33% / 67% make / break ratio (United Kingdom / Hong Kong).

2.2.31 &Q[n] Synchronous/Asynchronous Control

n = 0,1,2,3,5,6 (default = 5)

&Q0 Asynchronous Mode.

&Q1 Synchronous Mode.

&Q2 Dial when DTR=1, hang up when DTR=0, Synchronous Mode.

&Q3 Talk / data, DTR=0 / 1

&Q5 Error Control Mode.

&Q6 Asynchronous with speed buffering. Allows fixed DTE-DCE speed so the application program does not have to change UART data rate.

2.2.32 &R[n] Clear To Send Signal Control

n = 0 or 1 (default = 0)

In synchronous modes (&Q1, &Q2, and &Q3) this command affects the operation of the CTS line as follows:

&R0 CTS tracks RTS while the modem is on-line and observes the RTS-to-CTS delay determined by S26.

&R1 CTS is always ON.

2.2.33 &S[n] Data Set Ready Signal Control

n = 0 to 2 (default = 0)

The function of the DSR line is determined by the &S[x] command. When &Q0, &Q5, and &Q6 are in effect:

&S0 DSR is always ON.

&S1 DSR = 0 in the idle state and when in a test mode. DSR circuit is turned ON at start of the handshaking process. DSR is turned OFF when hangup process is started.

&S2 DSR = 0 in the idle state and when in a test mode. DSR circuit is turned ON at the end of handshake prior to issuing of the “CONNECT” result code. DSR is turned OFF when hangup process is started.

When &Q1 to &Q4 are in effect:

&S0, DSR = 0 in the Idle State. DSR circuit is turned ON at start of &S1 the Handshaking Process. DSR is turned OFF when Hangup Process is started.

&S2 DSR = 0 in the Idle State. DSR circuit is turned on at end of handshake prior to issuing of the “CONNECT” result code. DSR is turned OFF when Hangup Process is started.

2.2.34 &T[n] Select Test Mode

n = 0, 1, 3 to 8

The &T[n] command controls the following test modes:

&T0 Terminate any test in progress. The &T0 command must be the last command in the command line.

&T1 Initiate a Local Analog Loopback test (CCITT V.54 L3).

&T3 Initiate a Local Digital Loopback test.

&T4 Instructs the modem to grant a request from the remote modem for a Remote Digital Loopback test.

&T5 Instructs the modem to deny a request from the remote modem for a Remote Digital Loopback test.

&T6 Initiate a Remote Digital Loopback test (CCITT V.54 L2).

&T7 Initiate a Remote Digital Loopback Self-Test (CCITT V.54 L2).

&T8 Initiate a Local Analog Loopback Self-Test (CCITT V.54 L3).

2.2.35 &V View Active Configuration and User Profiles

The active and stored profiles are displayed (commands and S register settings) along with the stored telephone numbers. Inputs from the DTE are ignored while the view information is being sent to the DTE.

The information text is:

Active Profile:

B1 E1 L2 M1 Q0 V1 X4 Y0 &C0 &D0 &GO &J0 &L0 &P0 &Q0 &R0 &SO &X0 &Y0
S00:000 S01:000 S02:043 S03:013 S04:010 S05:008 S06:002 S07:030
S08:002 S09:006 S10:014 S11:095 S12:050 S18:000 S25:005 S26:001
S36:005 S37:000 S38:020 S44:003 S46:138 S48:007 S49:008 S50:016

Stored Profile 0:

B1 E1 L2 M1 Q0 V1 X4 Y0 &C0 &D0 &GO &J0 &L0 &P0 &Q0 &R0 &SO &X0
S00:000 S02:043 S06:002 S07:030 S08:002 S09:006 S10:014 S11:095
S12:050 S18:000 S25:005 S26:001 S36:005 S37:000 S38:020 S44:003
S46:138 S48:007 S49:008 S50:016

Stored Profile 1:

B1 E1 L2 M1 Q0 V1 X4 Y0 &C0 &D0 &GO &J0 &L0 &P0 &Q0 &R0 &SO &X0
S00:000 S02:043 S06:002 S07:030 S08:002 S09:006 S10:014 S11:095
S12:050 S18:000 S25:005 S26:001 S36:005 S37:000 S38:020 S44:003
S46:138 S48:007 S49:008 S50:016

Telephone Numbers:

0= 1=
2= 3=

2.2.36 &W[n] Write Active Profile to Non-Volatile RAM

n = 0 or 1

The &W[n] command causes the currently active configuration profile to be stored in one of the two non-volatile memory locations in the modem.

&W0 Store current active configuration profile as stored profile #0.

&W1 Store current active configuration profile as stored profile #1.

Once stored in the non-volatile memory, it will be automatically loaded each time the ATZ[n] command is issued. If selected using the &Y[n] command, it will be automatically loaded each time the modem is powered ON.

NOTE: The &W[n] command also saves the current (or the last) speed at which the modem received commands. This also means on power-up, the modem will send result codes or status messages at the last speed that was saved in non-volatile RAM.

2.2.37 &Y[n] Select Default Stored Profile

n = 0 or 1 (default = 0)

The &Y[n] command selects which of the two stored configuration profiles is considered the default user profile to be loaded as the active profile when the modem is powered ON.

&Y0 Select stored profile #0 as the default user profile.

&Y1 Select stored profile #1 as the default user profile.

2.3 RESULT CODES

Each command given to the modem can generated a result code from the list given below. Which result code is presented, or whether one is presented or not, is a function of the Q, V, X and W commands.

Result Code Terse Form (V=0)	Result Code Verbose Form (V=1)
0	OK
1	CONNECT
2	RING
3	NO CARRIER
4	ERROR
5	CONNECT 1200
6	NO DIALTONE
7	BUSY
8	NO ANSWER
10	CONNECT 2400
11	CONNECT 4800
12	CONNECT 9600
15	CONNECT 14400
16	CONNECT 19200
40	CARRIER 300
41	CARRIER 600
46	CARRIER 1200
47	CARRIER 2400
66	COMPRESSION: CLASS 5
67	COMPRESSION: V.42BIS
69	COMPRESSION: NONE
70	PROTOCOL: NONE
77	PROTOCOL: LAPM
80	PROTOCOL: ALT

2.4 73D2248 S-REGISTERS

2.4.1 S-Register Overview

The S-Registers allow you to customize the modem's performance. For example, you can use S-Registers to determine how may times the telephone will ring before the modem answers, how long the modem will wait for a dial tone before aborting a dialing sequence, how long the modem will pause during a "pause" command, and so on. S-Registers are changed with the S[r]=[n] command.

IMPORTANT NOTE: When you turn your modem ON, or reset it with the Z[n] command, the S-Registers are set to the factory default values that are stored in ROM. There are the following exceptions: the values for registers S0, S2, S6, S7, S8, S9, S10, S11, S12, S18, S25, S26, S30, S36, S37, S46, S48, S70, S82, S86 and S95 are stored in the modem non-volatile memory by the &W[n] command. These stored values are used when you turn your modem ON or reset it. Which of the two stored profiles is loaded when the modem is powered ON is determined by the &Y[n] command.

You can check your S-Register settings any time you are in Command State. To check an S-Register setting, enter a command consisting of the S-Register you want to check followed by a question mark. For example, to check how long the modem will wait for a dial tone before aborting a call, type in the following command:

AT S6? <Enter>

The screen will display the current setting of S-Register S6.

You can also check the current settings of all the S-Registers by issuing the following command:

AT &V <Enter>

In addition to all S-Register settings, you will be shown the current active profile and both of the stored profiles.

To change an S-Register setting, enter a command consisting of the S-Register, an equals (=) sign, and the desired value (in decimal). For example, to set the modem to answer after three rings, type the following command:

AT S0=3 <Enter>

If you wish to change an S-Register value and store it in non- volatile memory, you would add the &W[n] command after the S[n]=[r] command. For example, to set register S0 so that the modem automatically answers an incoming call after 3 rings, and store the new register S0 value in stored profile 0, type the following command:

AT S0=3 &W0 <Enter>

List Of S-Registers

The S-Registers you can change with the S[r]=[n] command, or whose value you can check with the S[r]? command, are listed below:

2.4.2 S0 AUTO-ANSWER

This register specifies the ring on which the modem will answer. A value of 1 to 255 will place the modem in auto-answer mode and cause it to answer on that many rings detected. A value of zero will disable auto-answer. The default is zero.

2.4.3 S1 RING COUNT

When the modem is set for Auto-Answer, register S1 keeps track of the number of times the phone rings. The S1 register resets to zero, eight seconds after the last ring. Range is 0 - 255 rings. Default is 0 rings.

2.4.4 S2 ESCAPE CODE CHARACTER

The S2 register contains the ASCII value of the Escape Command character. The default is 43, which is the ASCII "+". If you select a value greater than 127, the Escape feature is disabled and you cannot switch from the Data State to the Command State while maintaining your data connection. Range is 0 - 127 (ASCII). Default is 43 (+).

2.4.5 S3 CARRIAGE RETURN CHARACTER

The S3 register contains the ASCII value of the carriage return character. This character terminates both the command line and result codes. Range is 0 - 127 (ASCII). Default is 13 (carriage return).

2.4.6 S4 LINE FEED CHARACTER

The S4 register contains the ASCII value of the line feed character. It is used only when full result codes (V1) are selected. If you do not want a line feed to be automatically sent after the return following a verbal result code, set this value to 0. Range is 0 - 127 (ASCII). Default is 10 (line feed).

2.4.7 S5 BACKSPACE CHARACTER

The S5 register contains the ASCII value of the backspace character. Do not set S5 to ASCII 33 to 126 (ASCII printable characters) or to greater than ASCII 127. Range is 0 - 32 or 127 (ASCII). Default is 8 (backspace).

2.4.8 S6 WAIT FOR DIAL TONE

The S6 register sets the maximum number of seconds the modem waits to detect a dial tone before dialing. If the dial tone is not sensed within the S-Register time, the call is aborted. Range is 2 - 255 (seconds). Default is 2 (seconds).

2.4.9 S7 WAIT FOR CARRIER AFTER DIAL

The S7 register performs two functions. It sets the maximum time between dialing and responding to an incoming carrier signal. It also sets the duration of the pause generated by the W dial string modifier. Range is 1 -255 (seconds). Default is 30 (seconds).

2.4.10 S8 PAUSE TIME FOR COMMA

The S8 register sets the number of seconds the modem will pause during a pause created by a "," (comma) in the dialing sequence. Range is 1 - 255 (seconds). Default is 2 (seconds).

2.4.11 S9 CARRIER DETECT RESPONSE TIME

The S9 register sets (in 10ths of a second) how long a carrier signal must exist before the modem issues a carrier detect response. Range is 1 - 255 (1 / 10 seconds). Default is 6 (6 / 10 seconds).

2.4.12 S10 LOST CARRIER TO HANG UP DELAY

The S10 register sets (in 10ths of a second) the delay time between loss of carrier and the modem hanging up. After the S10 delay time, the modem hangs up and returns to Command State. Then you will see the NO CARRIER response. If the register is set with a value of 255, the modem will ignore carrier detect status and operate as if the carrier signal were present. If the value of S10 is less than the value of S9 a momentary loss of carrier will cause the modem to hang-up. Range is 0 - 255 (1 / 10 seconds). Default is 14 (1.4 seconds).

2.4.13 S11 DTMF DIALING SPEED

The S11 register sets the duration and spacing of touch-tones for tone dialing. (Setting this value lower than 50 will result in use of 50 milliseconds.) This register does not affect pulse dialing. Range is 50 - 255 (milliseconds). Default is 95 (milliseconds).

2.4.14 S12 ESCAPE CODE GUARD TIME

The S12 register establishes the length of the pause required before and after the escape sequence. This register also determines the time interval allowed for entering the escape Code characters (the entry time of each character must be less than the guard time). Setting register S12 to 0 disables the guard time entirely so you do not have to pause either before or after entering the escape sequence characters. Range is 0 - 255 measured in 1 / 50 second increments. Default is 50 (one second).

2.4.15 S13 - NOT USED

2.4.16 S14 OPTION REGISTER

Register S14 reflects the status of certain options. Do not write to this register. Register S14 is a bit mapped register whose bits are defined as follows:

bit 0 Not used.

bit 1 0 = No echo.

1 = Echo (see the E[n] command).

bit 2 0 = Result codes enabled.

1 = Result codes disabled (see the Q[n] command).

bit 3 0 = Numeric result codes.

1 = Verbal result codes (see the V[n] command).

bit 4 0 = Always zero when this register is read. (If you write a 1 to this bit, the modem will ignore all commands.)

bit 5 0 = Touch tone dialing.

1 = Pulse dialing.

bit 6 Always = 0.

bit 7 0 = Answer.

1 = Originate (See the A and D commands, the R dial string modifier, and register S0).

2.4.17 S15 - NOT USED

2.4.18 S16 SELF TEST

The S16 register controls and reports the status of the modem testing functions. Register S16 is a bit mapped register whose bits are defined as follows:

bit 0 0 = local analog loop disabled.

1 = local analog loop enabled (see &T1).

bit 1 0 = tone testing disabled.

1 = tone testing enabled.

bit 2 0 = local digital loopback disabled.

1 = local digital loopback enabled (see &T3).

bit 3 0 = remote digital loopback OFF.

1 = remote digital loopback in progress. Bit 3 is a status bit that indicates the modem is in remote digital loopback initiated by the remote modem (see &T4, &T5).

bit 4 0 = initiate remote digital loopback disabled.

1 = initiate remote digital loopback enabled (see &T6).

bit 5 0 = initiate remote digital loopback with test message and error count disabled.

1 = initiate remote digital loopback with test message and error count enabled (see &T7).

bit 6 0 = local analog loopback L3 with self-test disabled.

1 = local analog loopback L3 with self-test enabled (see &T8).

bit 7 Not used.

2.4.19 S17 - NOT USED

2.4.20 S18 TEST TIMER

Register S18 controls the duration of analog and remote digital loopback self-tests. After the test has continued for the time set in S18, the modem automatically terminates the test. Setting S18=0 disables the test timer, and requires manual termination of the self-tests. Range 0 - 255 (seconds). Default is 0.

2.4.21 S19 THROUGH S20 - NOT USED

2.4.22 S21 OPTION REGISTER

Register S21 controls various modem options. Register S21 is a bit mapped register whose bits are defined as follows:

bit 0 Not used.

bit 1 Not used.

bit 2 Not used.

bit 3/4 0/0 = modem ignores DTR.

0/1 = modem goes to Command State on DTR ON-to-OFF transition.

1/0 = modem hangs up on ON-to-OFF transition of DTR.

1/1 = modem goes to initialization state on DTR ON-to-OFF transition (see &D[n] command).

bit 5 0 = CD always ON (see &C[n] command).

1 = CD ON indicates presence of CD.

bit 6 Not used.

bit 7 0 = long space disconnect disabled.

1 = long space disconnect enabled (see the Y[n] command).

2.4.23 S22 OPTION REGISTER

Register S22 controls various modem options. Register S22 is a bit mapped register whose bits are defined as follows:

bit 0/1 0/1 = speaker volume low.

1/0 = speaker volume medium.

1/1 = speaker volume high (see the L command).

bit 2/3 0/0 = speaker disabled.

0/1 = speaker ON until carrier detected.

1/0 = speaker always ON.

1/1 = speaker ON until carrier detected but OFF during dialing (see the M[n] command).

bit 4-6 0/0/0 = selects 2400 bit/s result codes. When dialing, the modem goes off-hook, waits the number of seconds determined by S6 and “blind dials.”

1/0/0 = the modem selects appropriate connect result Code (CONNECT, CONNECT 1200, or CONNECT 2400). When dialing, the modem goes off-hook, waits the number of seconds determined by S6 and “blind dials.”

1/0/1 = identical to 1/0/0 except that the modem waits for dial tone before dialing.

1/1/0 = identical to 1/0/0 except the modem detects a busy signal and sends a BUSY result code. The modem blind dials.

1/1/1 = identical to 1/1/0 except the modem waits for dial tone before dialing. All result codes enabled. (See the X[n]).

bit 7 0 = pulse dialing make/break ratio = 39/91 (U.S.).

1 = pulse dialing make/break ratio = 33/67 (UK, Hong Kong) (see the &P[n] command).

2.4.24 S23 OPTION REGISTER

Register S23 controls various modem options. Register S23 is a bit mapped register whose bits are defined as follows:

bit 0 — 0 = obey request from remote modem for a remote digital loopback disabled.

1 = obey request from remote modem for a remote digital loopback enabled (see the &T4 and &T5 commands).

bit 1 / 2 — 0 / 0 = 0 to 300 bit / s.

0 / 1 = 2400 bit / s.

1 / 0 = 1200 bit / s.

1 / 1 = 2400 bit / s.

bit 3 — Not used.

bit 4 / 5 — 0 / 0 = even parity.

0 / 1 = space parity.

1 / 0 = odd parity.

1 / 1 = mark none parity.

bit 6 — Not used.

bit 7 — Not used.

2.4.25 S24 - NOT USED

2.4.26 S25 DELAY TO DTR

Register S25 sets the length of time that a change in the DTR state must persist in order for the change to be detected. Any change in DTR that continues for less than the time set in S25 is ignored. Range 0 - 255 (1 / 100 sec). Default is 5.

2.4.27 S26 RTS TO CTS TURN-AROUND DELAY

When the &R0 command has been issued, register S26 defines the time interval between an OFF to ON transition of RTS and when the modem turns CTS ON. The S26 setting applies to Synchronous modes 1,2 and 3 only. Range 0 - 255 (1 / 100 sec). Default is 1.

2.4.28 S27 OPTION REGISTER

Register S27 controls various modem options. Register S27 is a bit mapped register whose bits are defined as follows:

bit 0 — Reserved.

bit 1 — Reserved.

bit 2 — Reserved.

bit 3 — Reserved.

bit 4 — Reserved.

bit 5 — Reserved.

bit 6 — 0 = CCITT V.22bis, V.22, V.21.

1 = Bell 212A.

bit 7 — Reserved.

2.4.29 S28 THROUGH S29 - NOT USED

2.4.30 S30 NO ACTIVITY TIMEOUT

The modem will initiate the hangup process whenever both the DTE and DCE are inactive for a time greater than the value contained in the S30 register in tens of seconds. A value of zero disables this feature. Zero is the default.

2.4.31 S31 THROUGH S35 - NOT USED

2.4.32 S36 NEGOTIATION FAILURE TREATMENT

When an error control connection can not be negotiated between the two modems, this register indicates which operation mode the modem will use.

0 Drop call. (Assumes &Q5.)

1 Fall back to asynchronous connection (&Q0).

2 Reserved.

3 Fall back to &Q6.

4 Attempt MNP. If MNP fails, hang up.

5 Attempt MNP. If MNP fails, perform asynchronous connection (default).

6 Reserved.

7 Attempt MNP. If MNP fails, perform auto speed buffering.

2.4.33 S37 DESIRED DCE LINE SPEED

The modem will attempt to connect at the highest data rate that does not exceed the value of this register.

0 Last AT command speed.

1 Reserved.

2 110 bit/s.

3 300 bit/s.

4 Reserved.

5 1200 bit/s.

6 2400 bit/s.

2.4.34 S38 - NOT USED

2.4.35 S39 CURRENT FLOW CONTROL SETTING

The value in this register indicates the current flow control method selected. Flow control method is selected by the &Kn command. This register can only be read (not written). The default is 3.

0 No flow control.

3 RTS/CTS enabled.

4 XON/XOFF enabled.

5 Transparent XON/XOFF enabled.

2.4.36 S40 THROUGH S42 - NOT USED

2.4.37 S43 CURRENT DCE SPEED

The value in this register indicates the DCE speed of the last established connection. S43 is a read only register.

0 No connection.

1 Reserved.

2 110 bit/s.

3 300 bit/s.

4 Reserved.

5 1200 bit/s.

6 2400 bit/s.

2.4.38 S44 THROUGH S45 - NOT USED

2.4.39 S46 PROTOCOL/COMPRESSION SELECTION

This register selects which protocols are to be negotiated and whether or not compression should be negotiated.

136 LAPM only.

138 LAPM with data compression.

2.4.40 S47 CURRENT OPTION STATUS

This register indicates a feature negotiation after a connection has been made.

136 LAPM only: no compression

138 LAPM with V.42bis

2.4.41 S48 FEATURE NEGOTIATION ACTION

This S register controls feature negotiation.

7 Enable feature negotiation (default).

128 Disable negotiation and proceed to fall back defined in S36.

2.4.42 S49 THROUGH S69 - NOT USED

2.4.43 S70 - LINK LAYER N2 PARAMETER

This register sets the number of times a frame will be resent because of transmission errors. The call will be disconnected if the number of retransmissions exceeds the value in this register. The default value is 10.

2.4.44 S71 THROUGH S81 - NOT USED

2.4.45 S82 - BREAK SELECTION REGISTER

This register determines what type of break signal is sent during a V.42 connection. Three types of break signals can be selected. In-sequence breaks are delivered to the DTE without disrupting the data being transmitted. Expedited breaks will be delivered to the DTE before any buffered data while still maintaining the integrity of the data. Destructive breaks will flush out all buffered data before the break is sent.

In addition, breaks can be timed or untimed. Timed breaks will be in effect the length of time the break key is depressed up to 255 ms (rounded up to the nearest 10 ms). Untimed breaks are 180 ms or the time of the last time break.

The V.42 alternate protocol does not support timed breaks. If this protocol is in effect and a time break is selected and sent, the firmware will use the untimed break.

1,128 In-sequence breaks, timed

2 In-sequence breaks, untimed

3 Expedited breaks, timed

4 Expedited breaks, untimed

7 Destructive breaks, timed

8 Destructive breaks, untimed

2.4.46 S83 THROUGH S85 - NOT USED

2.4.47 S86 - CONNECTION FAILURE CAUSE CODE

This register will indicate the cause of a connection failure or why a connection was concluded. When a NO CARRIER result code is sent to the DTE, a value that indicates the cause of the termination is placed in this register.

0	Normal Hangup.
1,2,3	Reserved.
4	Physical carrier loss.
5	Feature negotiation failed to detect another error-control modem at the remote end.
6	Other error-control modem did not respond to feature negotiation message sent by this modem.
7	Other modem is synchronous only, this modem is asynchronous only.
8	Modems could not find common framing technique. (Sync or Async).
9	Modems could not find a protocol in common.
10	Feature negotiation message sent by remote modem was incorrect.
11	Synchronous information (data or flags) not received from other modem.
12	Normal disconnect initiated by remote modem.
13	Remote modem did not respond after many retransmissions of same message.
14	Protocol violation occurred.

2.4.48 S87 THROUGH S94 - NOT USED

2.4.49 S95 - EXTENDED RESULT CODE BIT MAP

This S-register can be used to override some characteristics of the Wn command. If a one is written to any of the bits described below, the corresponding result code will be sent regardless of the setting of the Wn command. See the Wn command above. Default is 0.

Bit 0	Verbose and terse CONNECT codes will indicate DCE speed rather that DTE speed.
Bit 1	Append "/ARQ" to the verbose CONNECT result code if the protocol is not done.
Bit 2	Enable the CARRIER result codes.
Bit 3	Enable the PROTOCOL result codes.
Bit 4	Not supported.
Bit 5	Enable the COMPRESSION result codes.
Bit 6	Reserved.
Bit 7	Reserved.

2.4.50 RESTORING THE DEFAULT S-REGISTER SETTINGS

The modem has three separate tables of default S-Register settings. One is the factory standard settings stored in permanent memory. This is a table covering all S-registers. The second and third are the register settings stored as part of the two stored profiles (0 and 1) in the non-volatile RAM memory. The tables of S-Register settings kept in the stored profiles are not complete.

There are two ways to restore your modem to the default S-Register settings stored in one of the stored profiles:

Turn the power to your modem OFF and back ON. Depending on the state of the &Y[n] command, you will automatically make the active profile equal to stored profile 0 or 1.

Issue the Z[n] command. [n] specifies which of the stored profiles is made the active profile when the modem is reset.

To restore the factory default S-Register settings, type the following command:

AT&F<Enter>

To restore the factory default register settings, and store them in stored profile 0, type the following command:

AT&F&W0<Enter>

2.5 LOOPBACK MODES

A communications setup is composed of many parts, including a computer, a modem, telephone cords, communication software, and the telephone line network itself. Any one of these components may have problems that interfere with communications.

To make "troubleshooting" easy, the 73D2248 comes with an internal analog loopback test that tests the modem transmit and receive circuitry while isolating the modem from the telephone line. Running this test makes it easier to determine if a problem exists with the modem or with another part of your communications system.

The 73D2248 modem also provides more sophisticated local and remote digital loopback modes that test the functioning of the telecommunications link and of the local and remote modems.

Also available are "self-test" versions of the local analog and remote digital loopback tests. These tests generate their own patterns of characters and automatically report the number of errors detected during the test.

When the modem responds with the connect message, CONNECT, CONNECT 1200 or CONNECT 2400 will be sent to the DTE depending on the bits per second (bit / s) rate selected and the X[n] command setting in effect at that time.

Register S18, Test Timer

Any of the following tests can be started and stopped manually or they can be halted at the end of a predetermined period of time. Register S18 is the Test Timer register and can be set from 0 to 255 seconds (slightly more than 4 minutes). Register S18's default setting is 0 (timer disabled).

While this feature can be used with each of the five tests described below, it is most useful with the Local Analog Loopback Self-Test and the Remote Digital Loopback Self-Test. Examples of S18 test timer use will be found in the descriptions of those two test procedures.

Analog Loopback Test

This test checks the modem operation in both the originate mode and in the answer mode. The modem transmit circuitry will be disconnected from the telephone line and connected to the modem receive circuitry. To run the analog loopback test, follow these steps:

Ensure that the modem has been installed according to the directions in the Quickstart section.

Turn ON the computer.

Load the communication software.

Go into "terminal mode," "local mode," "direct connect mode," or "terminal emulation mode." In this mode, commands typed at the keyboard go directly to the modem. The commands typed are the AT commands discussed in detail in the previous section on AT commands.

The Analog Loopback Test should be run at 1200 or 2400 bit / s. If the text is not "echoed" and displayed on the screen exactly as you entered it, the modem has failed the test and may be defective.

Once in "terminal mode," type the following commands:

Analog Loopback Test Procedure

Commands That You Enter	The Modem Responds	What Is Happening
ATZ0 <Enter>	OK	Resets the modem to stored profile 0.
AT&T1 <Enter>	CONNECT	Loopback connection has been made in the originate mode.
		Any characters now typed at the DTE will be echoed back to the DTE. Text that you enter is transmitted and then received by the modem.
+++	OK	Modem escapes back to the command state.
AT&T0 <Enter>	OK	Terminates the test.
AT&T1R <Enter>	CONNECT	Loopback connection has been made in the answer mode. Text that you enter is transmitted and then received by the modem.

+++	OK	"Escape" back to the command state.
AT&T0 <Enter>	OK	Terminates the test.
ATZ0 <Enter>	OK	Resets the modem to stored profile 0.

Local Digital Loopback Test

This test uses your modem to test the remote modem and the telephone network. You must be in contact with the operator of the remote modem. Prepare your modem as described in the Analog Loopback Test procedure. After establishing a connection with the remote modem enter the commands shown below.

Local Digital Loopback Test Procedure

Commands That You Enter	The Modem Responds	What Is Happening
+++	OK	"Escape" back to the command state.
AT&T3 <Enter>	OK	Local Digital Loopback connection has been made.
AT&TO <Enter>	OK	Characters sent by the remote modem will be echoed back to the remote modem. After the remote operator informs you that his test is complete, type: Terminates the test

Remote Digital Loopback Test

This test uses the remote modem to test your modem and the telephone network. You need not be in contact with the operator of the remote modem. Prepare your modem as described in the Analog Loopback Test procedure. Once in "terminal mode," type the following commands:

Remote Digital Loopback Test Procedure

Commands That You Enter	The Modem Responds	What Is Happening
+++	OK"	Escape" back to the command state.
AT&T6 <Enter>	CONNECT	Remote Digital Loopback connection has been made.
		Any characters now typed at your terminal will be sent to the remote modem and looped back to you.
+++	OK	"Escape" back to the command state.
AT&T0 <Enter>	OK	End the test.
ATO	CONNECT	Go back on-line with the remote modem.

Local Analog Loopback Self-Test

This test is equivalent to the analog loopback test described earlier in this section except that (a) the modem generates the test pattern, (b) when the test is terminated, the modem reports the number of errors detected. The test can be terminated either manually or under control of the test timer register S18.

Local Analog Loopback Self-Test Procedure

Commands That You Enter	The Modem Responds	What Is Happening
ATS18=0&T8<Enter>	CONNECT	Loopback connection has been made in the originate mode.
ATS18=30&T8<Enter>	(S18=0 selects manual termination. S18=30 selects timed termination after 30 seconds.) To use the answer mode, the command would end with an "R" e.g., ATS18=0&T8R<Enter>	(Modem generates a pattern.)

+++	OK	"Escape back to command state and display the number of digit number errors detected as a three digit number (automatic time-out)
AT&T0 <Enter>	OK	Terminate the test.

Remote Digital Loopback Self-Test

This test is equivalent to the remote digital loopback test described earlier in this section except that (a) the local modem generates the test pattern, (b) when the test is terminated, the local modem reports the number of errors detected by both modems. The test can be terminated either manually or under control of the test timer register S18 in the local modem.

Follow the procedure given above for the remote digital loopback test except that in step 3 you command your modem to go on-line in Remote Digital Loopback Self-Test mode by typing the following command:

AT&T7 <Enter>

The modem will automatically generate the test pattern. Remember that the test timer register S18 can be used to automatically terminate the test and report the number of errors detected.

Granting/Denying RDL Test Requests

By factory default, the 73D2248 modem grants a request from the remote modem to perform a remote digital loopback test The following commands can be used to control the granting or denying of remote digital loopback tests:

AT&T4 <Enter>	Grant request for remote digital loopback test factory (default).
AT&T5 <Enter>	Deny request for remote digital loopback test.
AT&T5&W0 <Enter>	Deny request for remote digital loopback test and write this configuration into stored profile 0.

2.6 73D2248 PROTOCOL OPERATION

Feature Negotiation (&Q,S36,S46,S48)

Immediately after a connection is established, the 73D2248 modem exchanges a sequence of characters with the remote modem to verify that the remote modem supports feature negotiation. If the remote modem supports feature negotiation, the modems exchange descriptive information (configuration, features, and protocols supported) to determine the highest level of protocol / compression supported by both modems.

The values in registers S46 and S48 select the desired connection type.

If detection fails or negotiation does not achieve the desired connection type, the values in register S36 specify the action to take (either hang up, attempt an MNP connection or communicate in standard asynchronous mode).

Feature negotiation also determines whether or not data compression is available for a particular error-control connection type and enables or disables data compression as necessary.

Negotiation Fallback (S36,S48)

The 73D2248 modem has an extended range of options for specifying the type of connection to attempt and what action to take if the desired connection cannot be made. The values in register S36 specify these options. To bypass feature negotiation and implement the fallback options immediately upon connection, set register S48 to 128.

Because some MNP only modems do not support the V.42 protocol handshake, negotiation may not result in an MNP connection. To connect with this type of modem it may be necessary to "Force" an MNP connection. To force an MNP connection, set register S48 to 128 and register S36 to 4,5, or 7.

Refer to Table 2-1 for descriptions of the &Q command and the S36,S46 and S48 registers.

Error Control (&Q,S36,S46,S48)

The 73D2248 modem can negotiate several connection types depending on the capabilities and configuration of the remote modem. The &Q5 command enables error control. The S36,S46, and S48 registers provide further control of this feature.

In the default configuration, the modem automatically attempts a connection using the error protocol specified by V.42, LAP-M. If a LAPM connection fails, the modem performs the action specified in register S36.

You can also instruct the modem to FORCE a connection using the "MNP" error control protocol, by setting register S48 to 128 and setting register S36 to 4,5, or 7. When configured to make an MNP connection, the modem first attempts an MNP class 3 or class 4 connection. Class 5 can be achieved by setting S46 to 138. The results of the negotiation depend on the capabilities and configuration of the remote modem.

Data Compression (&Q,S36,S46,S48)

The 73D2248 modem can compress data for transmission to a remote modem. For this capability to be enabled, the receiving modem must have the capability to decompress the data before sending it to the receiving terminal or computer. Because data compression provides higher throughput than the transmission rate being used to transfer data between the two modems, the computer or terminal must communicate with the modem at a speed greater than the modem's transmission rate.

If the modem using data compression can achieve as much as 4:1 compression rate, the data rate (DTE Speed) must be at least 4 times the communication rate (DCE Speed). For example, a modem connection speed of 2400 bit/s with a 4:1 compression ratio should have the DTE speed set to 9600 bit/s.

Two methods of data compression are available with the 73D2248 modem. MNP-5 data compression is automatically negotiated during the protocol negotiation phase of the modem communication handshake if S46 is set to 138 and the remote modem supports MNP-5. MNP-5 can support up to 2:1 compression. V.42bis data compression is also automatically negotiated if the remote modem supports V.42bis and S46 is set to 138. V.42bis can achieve as much as 4:1 compression.

Data compression is enabled by the &Q5 command. Further control of this feature is provided by S36,S46, and S48.

Table 2-1: &Q,S36,S46, and S48

&Qn	Selects asynchronous or synchronous modes. The default is &Q5.
&Q0 =	Asychronous mode. No speed buffering, no protocol.
&Q1-3 =	Synchronous mode. No speed buffering, no protocol.
&Q4 =	Not supported.
&Q5 =	Error control mode. See register S46.
&Q6 =	Asynchronous with speed buffering. Allows fixed DTE-DCE speed so applications do not need to change the communications rate based on connection results. NOT SUPPORTED AT 300 bit/s.
S36	Specifies the action to take in the event of negotiation failure.
0	Hang up line (Assumes &Q5).
1	Fall back to asynchronous connection (&Q0).
2	Reserved.
3	Fall back to Speed Buffering (&Q6).
4	Attempt MNP. If MNP fails, hang up.
5	Attempt MNP. If MNP fails, perform async connection (&Q0).
6	Reserved.
7	Attempt MNP. If MNP fails, perform &Q6.
S46	Protocol/Compression selection
136	LAPM only; no compression.
138	LAPM with V.42bis.
S48	Feature Negotiation Action.
7	Enable feature negotiation.
128	Disable negotiation and proceed with fallback as defined in S36.

Speed Buffering (&Q6,S36,S49, and S50)

Because the amount of data compression varies with the type of data being transferred, the 73D2248 modem employs a technique known as speed buffering to permit your computer or terminal to send data at a constant data rate. This data rate is generally 2 to 4 times the transmission speed between the two modems involved. The modem supports data rates up to and including 19,200 bit / s.

Speed buffering can also be used when the modem is communicating with a modem that does not have data compression. However, throughput is limited to the speed of the remote modem.

To enable speed buffering only, set &Q6. If speed buffering is required as a fallback option in a protocol attempt, set S36 to 7. Speed buffering is always selected in a protocol connection (MNP or V.42).

Because of the large buffer used for speed buffering in the 73D2248 modem, S registers S49 and S50 are not needed. However they are set to the default values provided in a Hayes V-Series modem. These registers can be changed by the application software but have no effect.

Local Flow Control (&K)

Error control connections and automatic speed buffering require a method of local flow control between the modem (DCE) and the terminal or computer (DTE). The V.42 recommendation specifies RTS / CTS and XON / XOFF as local flow control methods. The method of local flow control is selected with the &K command.

Table 2-2: Local Flow Control

&Kn	Determines flow control selection. The default is &K3.
&K0	No flow control.
&K1, K2	Not supported.
&K3	RTS/CTS.
&K4	XON/XOFF. (default =s, Q)
&K5	Not supported.

Negotiation Progress Messages (Wn and S95)

You may elect to have a negotiation progress message available. These messages can indicate the speed of data transfer between modems (carrier speed), the protocol being used, if any, and the speed between the computer or terminal and the modem (connect speed). In this way you may monitor the progress of a negotiated connection. The W1 command enables this feature. The default setting of W0 disables negotiation messages. W1 command is only effective if the X0 command is not in effect. The X command controls result codes.

Table 2-3: Negotiation Progress Messages

Wn	Determines whether or not to return negotiation progress result codes. The default is W0.
W0	Do not return extended result codes. The message CONNECT d is the data rate between the computer and modem.
W1	Return extended result codes.
W2	Do not return extended result codes. The message CONNECT d is the data rate between modems.
	NOTE: d = data rate 300,600,1200,2400,4800,9600,19200.

The extended result codes are displayed in the following manner:

CARRIER d

PROTOCOL x

COMPRESSION c

CONNECT d

where x = one of the following:

NONE

ERROR CONTROL / LAPM

ERROR CONTROL / ALT

and c = one of the following:

NONE

CLASS 5

V.42bis

S95 is a bit mapped register that gives even more flexibility to the extended result codes. The value in S95 OVERRIDES the Wn command. The following is a table describing the meaning of the bits in S95:

Bit 0	Result codes indicate DCE speed, not DTE speed
Bit 1	Ignored
Bit 2	Enable the CARRIER result code
Bit 3	Enable the PROTOCOL result code
Bit 4	Ignored
Bit 5	Enable the COMPRESSION result code
Bit 6	Reserved
Bit 7	Reserved

2.7 V.25BIS

To enable these commands set Dip SW1.3 on the mother board to the on position and cycle the power on the modem.

The following is a list of the 7 basic V.25bis commands supported in the 73M2248 demo board with Firmware Beta version TAK.01.00 9/22/92:

SET Auto baud to current DTE line speed - **SUPPORTED**

Same as AT command.

CIC Connect Incoming Call - **SUPPORTED**

Same as ATA command. Answers the phone regardless of the ring count set by the CNA command

CRN Call request with Number - **SUPPORTED**

Parameters: 0-9 * # T P = &: /

The V.25bis dial string is supplied with this command. This command functions the same as the ATD command. Valid Dial string parameters are as follows:

0-9 * # Dial Digits. These are the digits to be dialed.

T Use DTMF Dialing. When this command is encountered in a dial string the subsequent digits will be dialed in DTMF mode.

P Use PULSE Dialing. When this command is encountered in a dial string the subsequent digits will be dialed in Pulse mode.

< Short Pause. When this command is encountered in a dial string the firmware delays further action by the time specified in S8 (Default of 2 seconds.) NOTE: The value of S8 cannot be changed while in V.25bis mode.

= Long Pause. When this command is encountered in a dial string the firmware delays further action by double the time specified in S8. NOTE: See < modifier.

: Wait for dial tone. When this command is encountered in a dial string the mode will wait for the detection of dialtone. The modem will wait for the duration of the time specified by S7. NOTE: S7 cannot be changed while in V.25bis mode.

/ Comment. All characters in a dial string after this command will be ignored.

& Flash. This is the same as the Hayes ! flash character.

CRS Call Request with Stored number - **SUPPORTED**

Parameters: 1-20

This command dials using one of the stored phone numbers stored with the PRN command. If there is no number stored in the slot then the modem will respond with a CFINS indication.

DIC Disregard Incoming Call - **SUPPORTED**

Parameters: None

This command can be issued anytime during ringing but prior to the modem answering the call. This command only affects the current call. This condition may be canceled by the CIC command.

PRN Store/Delete Number - **SUPPORTED**

Parameters: 1-20

This command stores the ID number in one of 20 slots.

RLN Request List of Stored Numbers - **SUPPORTED**

Parameters: 1-20

This command requests either a single phone number if a parameter is specified or all 20 phone numbers stored with the PRN command if no number specified.

Section 3

HARDWARE DESIGN

silicon systems®
A TDK Group Company

SSI 73D2248/2348
MNP5, V.42bis Datacom Modem Device Set
Advance Information

January 1993

DESCRIPTION

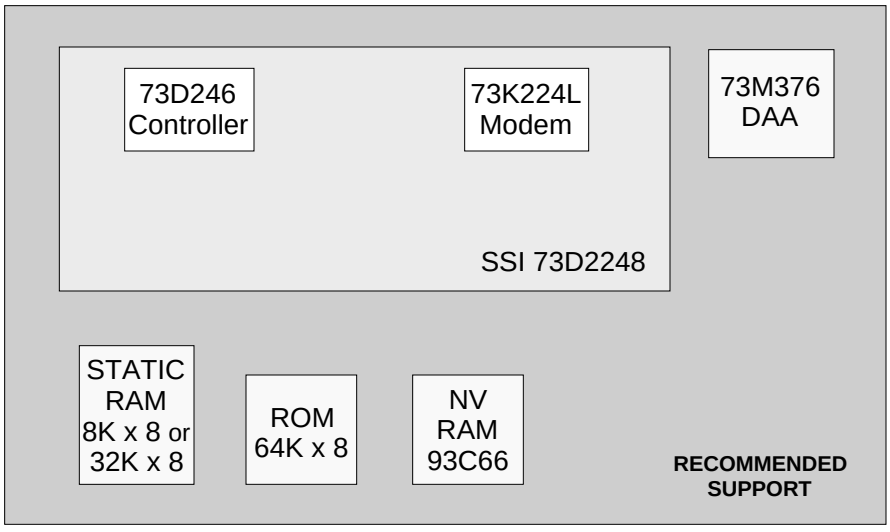
The SSI 73D2248/2348 Chip Sets consists of two CMOS integrated circuits which provide the data pump and protocol functions required to implement a high performance 2400 bit/s modem with error control and data compression. The 73D2248 basic modem function is provided by the SSI 73K224L modem chip and is compatible with CCITT V.21, V.22, V.22bis and Bell 103 and 212A protocols. The error control functions are provided by modular software running in the SSI 73D246 controller. Modules are available for MNP4, and V.42. Compression software modules can be can be added to the controller; MNP5 and V.42bis are available. Provisions for customization of the Command Set are provided, forming the basis for an International Modem.

The 73D2348 differs from the 73D2248 in that it uses the 73K324L instead of the 73K224L for the data pump. The 73K324L replaces the Bell 103 300 baud FSK mode of operation with the CCITT V.23 1200 baud FSK mode. The software is also modified to support V.23. The two products are otherwise identical.

FEATURES

- **Combines Modem and Protocol Controller**
- **Supports 0 - 300, 1200 and 2400 bit/s with both Sync and Async Modes**
- **Modular Software Design Allows Customization**
- **Modem Protocols:**
  - **Bell 103, 212A**
  - **CCITT V.22, V.22bis**
- **Error Control/Compression Protocols Available: MNP4, MNP5, CCITT V.42, V.42bis**
- **Supports Non-volatile Memory to Store User Configurations and Phone Numbers**
- **CMOS Design for Low Power Consumption**
- **TQFP packages available for PCMCIA applications**

MNP5, V.42bis Datacom Modem Device Set



0193

CAUTION: Use handling procedures necessary for a static sensitive component.

FUNCTIONAL DESCRIPTION

The SSI 73D2248/2348 chip set forms the basis for an international modem design incorporating the most advanced error control and compression algorithms. The set consists of two chips, the SSI 73K224L (73K324L) modem and the 73D246 controller. Customization of the controller is one of the features of this chip set; software modules allow the modem vendor to provide a range of features from a standard hardware platform.

The 73K224L (73K324L) provides the QAM, PSK and FSK modulator and demodulator functions, call progress and handshake tone monitors, test modes and a tone generator capable of producing DTMF, answer and CCITT guardtones. This single-chip modem supports the V.22bis, V.22, V.21 and Bell 103/ CCITT V.23/212A operating protocols in both sync and async modes. Low level functions of the controller provide for automatic detection of DTE speed, auto-dial, auto-answer, handshake with fallback and call progress detection.

The 73D246 controller handles both the low level modem functions as well as protocol negotiation and protocol operation. Software modules can be chosen to provide the desired protocols for product customization and differentiation. In addition, the "AT" command set source code will be available for those desiring to provide unique or country dependent features.

Basic capabilities of the modem are those found in the 73K224L (73K324L) Single-Chip Modem and are listed in the separate 73K224L (73K324L) data sheet.

AUTOMATIC HANDSHAKE

The 73D2248/2348 will automatically perform a complete handshake with a called or calling modem and enter the data transfer mode. After the link between the two modems has been established, the modems may remain in the normal data mode or negotiate a link which has error control and data compression. Commands are provided to inform the modem which action is appropriate.

TEST MODES

The 73D2248/2348 chip set has provisions for three test modes: analog loopback, digital loopback and remote digital loopback. Analog loopback allows data to be sent into the local modem, have it modulated and then demodulated and returned to the local terminal. Digital loopback requires the cooperation of the user at the remote end and allows data to be sent to the remote modem, demodulated, then remodulated and returned to the local end. Remote digital loopback allows the same capability, without the need for a remote operator; signals are sent to the remote modem which perform the switching task that a remote operator would have done.

AT COMMAND INTERPRETER

The SSI 73D2248/2348 includes an AT Command Interpreter which is a superset of the Hayes 2400 Smartmodem™ command set. Common application software will be able to control the modem though this interpreter. Additional commands have been added to provide for control of the MNP and CCITT V.42 modes.

NON-VOLATILE MEMORY

A serial NVRAM provides 256 bytes of storage for configuration information and telephone numbers. Current hardware provides for a 2K bit memory of which about 400 bytes are used for setup and telephone number storage. The remaining 1600 bytes are avaliable. Memory address space allocated to non-volatile RAM is 8K, so an expansion factor of 4 is available. Alternatively, the address space could be decoded for more hardware functionality.

PROTOCOLS

Microcom Networking Protocol (MNP)

MNP4 is a protocol offering error control while MNP5 offers data compression. Data to be transmitted is broken into blocks of varying sizes, depending on line conditions, and sent to the remote modem along with a 16-bit Cyclic Redundancy Check word. If the algorithm used to derive the CRC word at the transmitter does not produce an identical word when exercised on the received data, a line error is assumed, and the block is repeated. Data compression is obtained by transmitting a short set of characters for a longer redundant set. At the receiver, the short string is replaced with the longer string that it represented, and the data stream is returned to its original state.

CCITT V.42 and V.42bis

The CCITT has ratified a set of protocols which operate in a manner similar to MNP. MNP4 corresponds to V.42 while MNP5 corresponds with V.42bis. Greater efficiency is offered, but the tradeoff is a larger memory space requirement. MNP5 requires an 8K buffer, while V.42bis requires 32K. Data files which show compression ratios approaching 2:1 with MNP5 may show ratios of nearly 4:1 with V.42bis.

SSI 73D246
Microcontroller

Advance Information

November 1993

DESCRIPTION

The Silicon Systems 73D246 high performance microcontroller is based on the industry standard 8-bit 8052 implemented in Silicon Systems' advanced submicron CMOS process. The processor has the same attributes of the 8052 including Instruction cycle time, UART, timers, interrupts, 256 bytes of on-chip RAM and programmable I/O. The architecture has been optimized for low power portable modem or communication applications by integrating unique features with the core CPU.

The main feature is a user friendly HDLC packetizer, accessed through the special function registers. It has a serial I/O, hardware support for 16- and 32-bit CRC, zero insert/delete control, a dedicated interrupt and a clear channel mode for by-passing the packetizer.

Other features include additional user programmable I/O with programmable bank select and chip select logic, designed to eliminate board level glue logic.

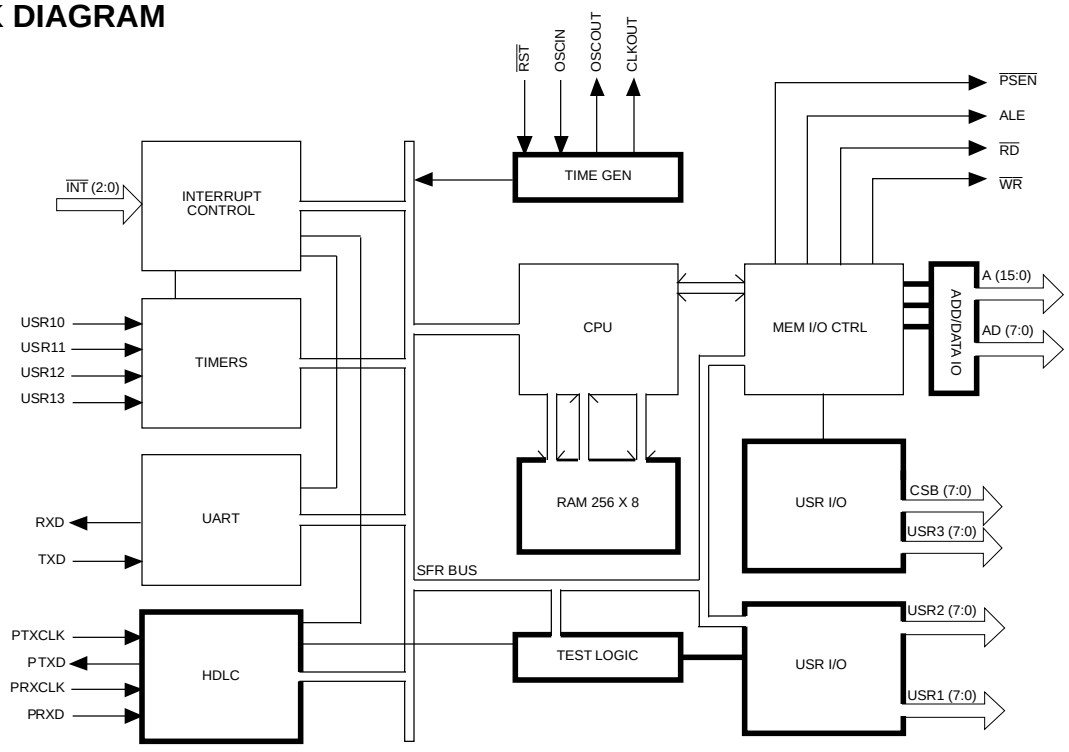
For devices that require non-multiplexed address and data buses, eight latched outputs for the low byte of the address are available.

(continued)

FEATURES

- **8052 Compatible construction set**
- **22 MHz Operation**
- **HDLC Support logic (Packetizer, 16 and 32 CRC, zero ID)**
- **24 pins for user programmable I/O ports**
- **8 pins programmable chip select logic for memory mapped peripheral eliminating glue logic**
- **3 external interrupt sources (programmable polarity)**
- **16 dedicated latched address pins**
- **Multiplexed data/address bus**
- **Instruction cycle time identical to 8052**
- **Buffered oscillator (or OSC/2) output pin**
- **Bank select circuitry to support up to 128K of external program memory**
- **100-Lead TQFP package available for PCMCIA applications**
- **Also available in 100-Lead QFP package**

BLOCK DIAGRAM



1193

DESCRIPTION (continued)

The 73D246 has two extra interrupt sources, an external interrupt and a HDLC interrupt. The HDLC interrupt has two registers associated with it: the HDLC Interrupt Register which is used to determine the source of the interrupt, and the HDLC Interrupt Enable Register that enables the source of the interrupt.

The interrupt pins INT0 and INT1 can be either negative edge, positive edge or level triggered. INT2 pin is always edge triggered.

A buffered clock output has been added to support peripheral functions such as UARTs, modems and other clocked devices.

Additional internal special function registers are used for firmware control over the HDLC Packetizer, and the programmable I/O ports.

For low power applications the 73D246 supports two power conservation modes: Idle and Power-down. In the Power-down state the total current consumption is less than 1 μA at room temperature.

This device is offered in small form factor 100-lead TQFP packages for PCMCIA applications and 100- lead QFP packages.

DEVELOPER'S NOTE:

The 73D246 is also available in a 100-pin PGA package for system developers. The PGA package is more convenient and reliable for development emulation systems than the other package styles. Emulation systems for the 73D246 are available through Signum Systems, 171 E. Thousand Oaks Blvd., # 202, Thousand Oaks, CA 91360 (805) 371-4608.

8052 REFERENCE

This Document will describe the features unique to the 73D246. Please refer to an 8052 Programmer's Guide, Architectural Overview and Hardware Description for details on the instruction set, timers, UART, interrupt control, and memory structure.

REGISTER DESCRIPTION

INTERRUPTS

The core chip provides 8 sources of interrupt; 3 external interrupts, 3 timer interrupts, a serial port interrupt, and an HDLC interrupt. An external interrupt and an HDLC interrupt are unique to the 73D246. They do not exist in a normal 8052 product. Previously unused bits in the IE and IP registers are now serving functions for these additional interrupt sources. The interrupt vector addresses are as follows:

SOURCE	VECTOR ADDRESS
$\overline{\text{INT0}}$ (IE0)	003H
TF0	00BH
$\overline{\text{INT1}}$ (IE1)	013H
TF1	01BH
RI + TI	023H
TF2 + EXF2	02BH
$\overline{\text{INT2}}$ - ADDED INTERRUPT	033H
HDLC - ADDED INTERRUPT	03BH

The external interrupt sources, $\overline{\text{INT}}$(2:0), come from dedicated input pins. The apparent polarity of these pins is individually controlled by bits in a special interrupt direction register, IDIR (address A9). The interrupt pins $\overline{\text{INT1}}$ and $\overline{\text{INT0}}$ can be either edge or level generated interrupts as indicated by bits 1 and 3 in the TCON register (address 88). Pin $\overline{\text{INT2}}$ is always an edge generated interrupt. A flag is set when a falling transition (rising if IDIR bit 2 is set) on this pin is detected. This flag is automatically cleared when the interrupt is processed.

INTERRUPT ENABLE REGISTER (IE) SFR ADDRESS A8
Bit Addressable
Reset State 00h

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
EA	EX2	ET2	ES	ET1	EX1	ET0	EX0

Note: BIT 6 differs from the 8052. This is a reserved bit in the 8052 and is used as a mask bit for external interrupt 2 in the core implementation. When BIT 6 is set to a 0, external interrupt 2 is disabled.

The mask bit for the HDLC interrupt source is BIT 0 of the HDLC control register.

INTERRUPT PRIORITY REGISTER (IP) SFR ADDRESS B8
Bit Addressable
Reset State 00h

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
PHDLC	PX2	PT2	PS	PT1	PX1	PT0	PX0

Note: BIT 6 and BIT 7 differ from the 8052. These are reserved bits in the 8052 and are used to determine the priority of external interrupt 2 and the HDLC in the core implementation. When BIT 6 is set to a 1, the interrupt is set to the higher priority level.

REGISTER DESCRIPTION (continued)

EXTERNAL INTERRUPT DIRECTION REGISTER (IDIR) SFR ADDRESS 92
Byte Addressable
Reset State 00h

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
0	0	0	0	0	INTD2	INTD1	INTD0

These bits determine the polarity of the corresponding external signals INT(2:0) which will result in an interrupt.

BITS(2:0) Interrupt Polarity Control

If the bit is set to a 0, a falling edge will trigger the interrupt. If the bit is set to a 1, a rising edge will trigger the interrupt. Also, if the bit is set to a 1, level generated interrupts will occur when the corresponding pin is high and the internal pin signal to the timer controls will be inverted.

Bits 6 and 7 will always be read as 0's.

POWER SAVING MODES

Low Power Modes

The SSI 73D246 supports two power conservation modes, which are controlled by the PCON.1 and PCON.0 control bits of the PCON register.

If PCON.0 is set, the SSI 73D246 will go into a power saving mode where the oscillator is running, clocks are supplied to the UART, timers, HDLC, and interrupt blocks, but no clocks are supplied to the CPU. Instruction processing and activity on the address and data ports is halted. Normal operation is resumed when an unmasked interrupt is requested or when a reset occurs.

If PCON.1 is set, the SSI 73D246 goes into its lowest power mode where the oscillator is halted. The total current consumption in this state should be less than 1 μa. The SSI 73D246 will start its oscillator and begin to return to normal operation when either a reset occurs, when a falling (rising if corresponding direction bit is set) edge of an unmasked external interrupt from pins INT(2:0) is detected. Edges used in wakeup modes are not filtered in the SSI 73D246 so the user must be cautious of noise or small glitches inadvertently waking up the chip. From the time the edge that results in the wake up occurs, to the point at which an instruction is executed, depends on the oscillator start-up time. Three good oscillator pulses must be detected before the main internal clocks are generated.

USER PROGRAMMABLE I/O

Port Control USR1, USR2, USR3, USR4

The core chip provides 32 user I/O pins. Each pin is programmed separately as either an input or as an output by a bit in a direction register. If the bit in the direction register is set to a 1, the I/O control will treat the corresponding pin as an input. If it is a 0, the pin will be treated as an output whose value is determined by the port data register. The USR1 and USR2 port registers are accessed through the internal SFR bus. The USR3 and USR4 ports are accessed through the external memory bus by a MOVX instruction. The USR4 port provides the user with an automatic chip select function if selected by the user. If the user does not require some (or any) of the chip select pin options, he may program the USR4 port pins to operate in the same way as USR3 port pins.

The USR DATA register contents determine pin values if chosen as an output. When reading from the DATA register's SFR address, the pin logic values are returned as data except when the port address is the destination address for a read-modify-write instruction. In this case, the latched register values are returned as data. When reading data from a DATA register that is mapped in the external memory space, the pin values are always returned as data.

USER 1 PORT

USR1 DATA SFR Address 90
Bit Addressable
Reset State 00h

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
USR1 7	USR1 6	USR1 5	USR1 4	USR1 3	USR1 2	USR1 1	USR1 0

Bits in this register will be asserted on the USR1(7:0) pins if the corresponding direction register bit is a 0. Reading this SFR's address will return data reflecting the values of pins USR1(7:0) except when address 90h is the destination address for a read-modify-write instruction. In this case, the latched register values are returned as data.

USR1 port signals are also used as timer controls. In applications where the external signals are required for timer count modes, the corresponding port pin should be configured as an input.

USR1 BIT0 = TIMER 0 T0 PIN
USR1 BIT1 = TIMER 1 T1 PIN
USR1 BIT2 = TIMER 2 T2EX PIN
USR1 BIT3 = TIMER 2 T2 PIN

USR1 Port Direction (DIR1) SFR Address 91
Byte Addressable
Reset State FFh

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
DIR1 7	DIR1 6	DIR1 5	DIR1 4	DIR1 3	DIR1 2	DIR1 1	DIR1 0

This register is used to designate the USR1 pins as either inputs or outputs. If the register bit is reset to a 0, the corresponding USR1 pin is programmed as an output that will be driven by the corresponding USR1 DATA register bit. If the register bit is a 1, the corresponding pin will be treated as an input.

After a reset, the USR1 pins will present a high impedance output state and the input values will not be driven from the pin, but will be driven to a 0 internally. The pins will assume normal I/O operation once the processor has written the port direction register. This feature will ensure the core chip is in a low current state at reset (you don't want to drive out against external inputs, and you don't want floating inputs).

REGISTER DESCRIPTION (continued)

USER2 PORT

USR2 Port Data SFR Address D8
Bit Addressable
Reset State 00h

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
USR2 7	USR2 6	USR2 5	USR2 4	USR2 3	USR2 2	USR2 1	USR2 0

Bits in this register will be asserted on the USR2(7:0) pins if the corresponding direction register bit is a 0. Reading this SFR's address will return data reflecting the values of pins USR2(7:0) except when address D8h is the destination address for a read-modify-write instruction. In this case, the latched register values are returned as data.

USR2 Port Direction (DIR2) SFR Address D9
Byte Addressable
Reset State FFh

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
DIR2 7	DIR2 6	DIR2 5	DIR2 4	DIR2 3	DIR2 2	DIR2 1	DIR2 0

This register is used to designate the USR2 pins as either inputs or outputs. If the register bit is reset to a 0, the corresponding USR2 pin is programmed as an output that will be driven by the corresponding USR2 I/O DATA register bit. If the register bit is a 1, the corresponding pin will treated as an input.

After a reset, the USR2 pins will present a high impedance output state and the input values will not be driven from the pin, but will be driven to a 0 internally. The pins will assume normal I/O operation once the processor has written the port direction register. This feature will ensure the core chip is in a low current state at reset (you don't want to drive out against external inputs, and you don't want floating inputs).

USR3 Port Data External address 0000
Byte Addressable
Reset State 00h

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
USR3 7	USR3 6	USR3 5	USR3 4	USR3 3	USR3 2	USR3 1	USR3 0

Bits in this register will be asserted on the USR3(7:0) pins if the corresponding direction register bit is a 0. Reading this SFR's address will return data reflecting the values of pins USR3(7:0).

If the bank select feature is chosen, USR3 PIN7 acts as address bit 17 and USR3 data bit 7 is ignored.

USR3 I/O Port Direction (DIR3) External Address 0001
Byte Addressable
Reset State FFh

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
DIR3 7	DIR3 6	DIR3 5	DIR3 4	DIR3 3	DIR3 2	DIR3 1	DIR3 0

This register is used to designate the USR3 pins as either inputs or outputs. If the register bit is reset to a 0, the corresponding USR3 pin is programmed as an output that will be driven by the corresponding USR3 DATA register bit. If the register bit is a 1, the corresponding pin will be treated as an input.

After a reset, the USR3 pins will present a high impedance output state and the input values will not be driven from the pin, but will be driven to a 0 internally. The pins will assume normal I/O operation once the processor has written the port direction register. This feature will ensure the core chip is in a low current state at reset (you don't want to drive out against external inputs, and you don't want floating inputs).

If the bank select feature is chosen, USR3 PIN7 is forced to be an output.

Bank Select (BNKSEL) External Address 0002
Byte Addressable
Reset State 00h

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
B7	B6	B5	B4	B3	BSEN	BS1	BS0

This resister is used to accommodate systems where more than 64 Kbytes (up to 128 Kbytes) of program memory are required. USR3 PIN 7 acts as an address pin, A16, if BSEN is set to a 1 and if the processor is fetching an instruction and not data memory. If BSEN is set to a 1, A15 is also modified during instruction fetches as shown. If BSEN is a 0, no alterations to address bit A15 are made, and USR3 PIN 7 is a function of USER3 bit 7 and DIR3 bit 7.

Bits (7-3) are general purpose read/write register bits.

A15 is the value of the 16th address bit as it appears at pin A15.

A15' is the address from port 2 internal logic, the value that will appear as the most significant address bit if no bank select feature is chosen.

A16 is the value of the 17th and MSB of the instruction address seen at the USR3 7 port pin, if the bank select feature is selected. If the bank select feature is not selected, USR3 7 acts as a normal USR3 I/O port pin.

BSEN	BS1	BS0	A15'	A15	A16	ADDRESS
0	*	*	0	0	USR37	0K - 32K
0	*	*	1	1	USR37	32K - 64K
1	0	0	0	0	0	0K - 32K
1	0	0	1	1	0	32K - 64K
1	0	1	0	0	0	0K - 32K
1	0	1	1	0	1	64K - 96K
1	1	0	0	0	0	0K - 32K
1	1	0	1	1	1	96K - 128K
1	1	1	0	0	0	0K - 32K
1	1	1	1	0	1	64K - 96K

* = Don't care.

REGISTER DESCRIPTION (continued)

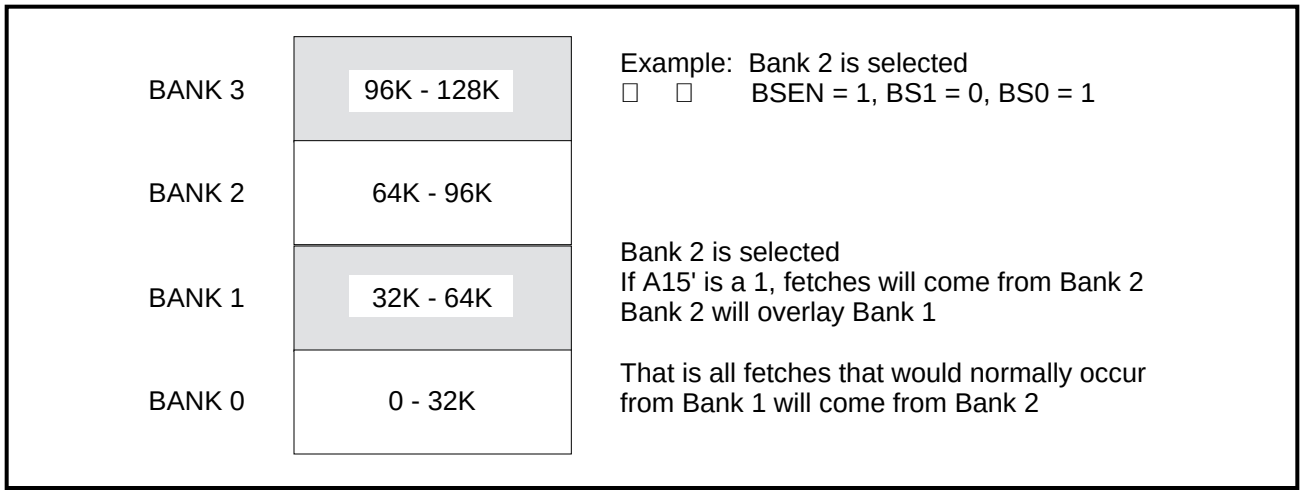


FIGURE 8: Bank Select

USER4 PORT

USR4 Port Data External Address 0003
Byte Addressable
Reset State 00h

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
USR4 7	USR4 6	USR4 5	USR4 4	USR4 3	USR4 2	USR4 1	USR4 0

Bits in this register will be asserted on the USR4(7:0) pins if the corresponding direction register bit is a 0 and if the corresponding bit in the chip select enable register, 0005, is set to a 0. Reading this register will return data reflecting the values of pins USR4(7:0).

USR4 I/O Port Direction (DIR4) External Address 0004
Byte Addressable
Reset State FFh

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
DIR4 7	DIR4 6	DIR4 5	DIR4 4	DIR4 3	DIR4 2	DIR4	1 DIR4 0

This register is used to designate the USR4 pins as either inputs or outputs. If the register bit is reset to a 0, the corresponding USR4 pin is programmed as an output that will be driven by the corresponding USR4 I/O DATA register bit if the corresponding bit in the chip select enable register, 005, is set to a 0. If the register bit is a 1, the corresponding pin will treated as an input only if the corresponding bit in register 005 is set to a 0.

After a reset, the USR4 pins will act as chip select outputs.

USR4 Port Chip Select Enable (CSEN) External Address 0005
Byte Addressable
Reset State FFh

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
CSEN 7	CSEN 6	CSEN 5	CSEN 4	CSEN 3	CSEN 2	CSEN 1	CSEN 0

This register is used to designate the USR4 pins as either user programmable I/Os or as chip select (CS0B - CS7B) functions on a pin by pin basis. This feature is designed to help reduce external glue logic for peripheral memory mapped devices. The chip select function is programmed by setting the appropriate bits in the CSEN register. When a chip select pin is enabled by setting the corresponding CSEN bit to a 1, all data and direction information from registers 0003 and 0004 for this bit are ignored and the selected port becomes an output. If the bit is reset to a 0, the pin will be treated as a normal programmable user I/O pin as defined by registers 0003 and 0004.

The chip select pins have a defined memory map. The intent is that the outputs can be wire ORed together for a flexible selection of peripheral chip selects. All chip selects will be disabled (forced to a logic 1. It is assumed that all chip selects are active low) after the read or write is completed, and the appropriate chip select will be enabled as the next new external addresses is asserted. After a reset, the CSB pull-up devices are all enabled, that is, all chip select outputs are high. Users must account for this if these pins are intended to be general purpose I/Os.

The chip selects partition a 64K memory space as follows:

CHIP SELECT PIN	ADDRESS	# BYTES
RESERVED FOR INTERNAL USE	0000H - 00FFH	256
CS0 (USR4.0)	0100H - 01FFH	256
CS1 (USR4.1)	0200H - 03FFH	512
CS2 (USR 4.2)	0400H - 07FFH	1K
CS3 (USR 4.3)	0800H - 0FFFH	2K
CS4 (USR 4.4)	1000H - 1FFFH	4K
CS5 (USR 4.5)	2000H - 3FFFH	8K
CS6 (USR 4.6)	4000H - 7FFFH	16K
CS7 (USR 4.7)	8000H - FFFFH	32K

Note: You can’t read from external addresses 0000H-00FFH. These are reserved for SSI 73D246 internally defined registers

REGISTER DESCRIPTION (continued)

HDLC CONTROL REGISTER 0

HDLC Control Register 0 (HDLC0) SFR Address C0
Bit Addressable Reset State 00XX 0000 b
Bits 5 and 4 are read only bits

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
WRXD	WPTXD	TXD R	PRXD R	RXD CTRL1	RXD CTRL0	PTX CTRL1	PTX CTRL0

This register controls the basic set-up of the DTE and modem pins RXD, TXD, PRXD, and PTXD.

BIT 7 WRXD

BIT 7 allows the processor to write directly to the SSI 73D246 RXD output pin. The value of BIT 7 will appear at the PTXD pin only if BIT 1 is a 1 and BIT 0 is a 0.

BIT 6 WPTXD

BIT 6 allows the processor to write directly to the SSI 73D246 PTXD output pin. The value of BIT 6 will appear at the PTXD pin only if BIT 1 is a 1 and BIT 0 is a 0.

BIT 5 TXD

BIT 5 is a read only bit that reflects the value at the SSI 73D246 TXD input pin.

BIT 4 PRXD

BIT 4 is a read only bit that reflects the value at the SSI 73D246 PRXD input pin.

BIT 3 BIT 2 RXD Control

BIT 3 and BIT2 control the source of the SSI 73D246 RXD output pin. This output goes to the DTE's RS232 interface. The source of this signal can be the core's UART TXD output, the PRXD output from a modem peripheral (clear channel), the DTE's TXD(echo), or the value written into bit 7 of this register.

BIT 3	BIT 2	RXD OUTPUT
0	0	UART TXD OUTPUT
0	1	PRXD BUFFERED (CLEAR CHANNEL)
1	0	TXD BUFFERED (ECHO)
1	1	WRXD (BIT 7)

BIT 1 BIT 0 PTXD Control

BIT 1 and BIT0 control the source of the SSI 73D246 PTXD output pin. This output goes to the modem's TX data input. The source of this signal can be the core's HDLC TX output, the DTE's TXD output (clear channel), or the value written into bit 6 of this register.

BIT 1	BIT 0	PTXD Output
0	0	HDLC TX Output
0	1	TXD Buffered (Clear Channel)
1	0	WPTXD (BIT 6)
1	1	0

HDLC CONTROL REGISTER 1

HDLC Control Resister 1 (HDLC1) SFR Address C1
Byte Addressable
Reset State 00h

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
HDLC RST	CLK CRTL	CLK EN	RXCRC 32	RXCRC 16	TXCRC 32	ZERO ID	HDLC EN

This register controls the basic set-up of the HDLC block. This register will be written during initialization and not during normal message processing.

BIT 7 HDLC Software Set

When BIT 7 is a 1, the HDLC circuit is reset and held in a low power state and no interrupts from the HDLC circuitry will be generated. When a 0 is written to this bit, the HDLC circuit will behave according to its control bits. BIT 7 and the power on reset signal are OR'ed together to form a reset signal for the HDLC block.

BIT 7 is cleared to a 0 upon a power up reset.

BIT 6 CLK CRTL Clock Out Control

Bit 6 controls the frequency of the clock output pin. The clock output is either the oscillator's output signal divided by two or a buffered ocscillator output signal.

BIT 6	CLOCK OUT
0	OSC
1	OSC/2

BIT 6 is cleared to a 0 upon a reset.

BIT 5 CLK Clock Out Enable

BIT 5 enables the clock at the clock output pin if it is set to a 1. The clock pin output can be held to a 0, without halting the oscillator, by writing this bit to zero. This will reduce system power if the clock pin is not used or if a power reduction mode is required.

BIT 5 is cleared to a 0 upon a reset.

HDLC CONTROL REGISTER 1 (continued)

BIT 4 BIT 3 RX CRC Control

BIT 4 and BIT 3 determine the type of CRC remainder that will be checked at the end of a received frame. There is a 16-bit CRC, and a 32-bit CRC that the HDLC block can support. If both BIT 4 and BIT 3 are reset, bits 7 and 6 of the HDLC STATUS register will be held to a 0. If both BIT 4 and BIT 3 are 1s, a special CRC search mode is enabled where both bits 7 and 6 of the HDLC status register are enabled. This mode is used during a connection to determine which CRC is used by the initiating modem. If the 16-bit CRC remainder is not matched at the end of the received frame, then BIT 6 of the HDLC STATUS register is set. If the 32-bit CRC remainder is not matched at the end of the received frame, then BIT 7 of the HDLCSTATUS register is set. Once the correct CRC type is established during a connection, either BIT 4 or BIT 3 should be set to a 1 enabling the appropriate INVALID CRC status bit.

BIT 4	BIT 3	CRC TYPE
0	0	NO CRC Check
0	1	Enable CRC16 Status
1	0	Enable CRC32 Status
1	1	Enable CRC16 Status and CRC32 Status

BIT 2 TXCRC Control

BIT 2 controls the CRC type to be transmitted. If BIT 2 is reset to a 0, a 16-bit CRC will be transmitted with the SEND CRC command. If BIT 2 is set to a 1, a 32 bit CRC will be transmitted.

BIT 1 Zero Insert/Delete Control

When BIT 1 is set to a 1, a 0 will be transmitted if either the SEND DATA or SENDCRC bits of the HDLCTX CONTROL are set after five consecutive 1s have been transmitted. Also, when this bit is set, a 0 will be removed from the received data stream if it immediately follows a pattern of a 0 followed by five consecutive ones. If BIT 1 is reset to a 0, no 0s will be inserted during transmission, and no 0s will be deleted during reception.

BIT 1 is cleared to a 0 upon a reset.

BIT 0 HDLC Interupt Enable

When BIT 0 is reset to a 0, the HDLC will be prevented from generating an interrupt. The status bits that indicate the source of the interrupt can still be set allowing the HDLC block to be serviced in a polled mode.

BIT 0 is cleared to a 0 upon reset.

HDLC TX Control Resister (HTXC) SFR Address C2
Byte Addressable
Reset State 00h

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
0	0	0	DIV16 CLK	SEND ABORT	SEND CRC	SEND DATA	SEND FLAG

This register is used to control the source of data that appears on the PTXD pin. Bits are shifted out on every rising edge of the PTXCLK pin input. If no control bits are set, or more than 1 TX CONTROLbit is set, the PTXD pin will go to a binary 1.

BIT 7 - BIT 5 Always 0

BIT 4 16X Clock Select

Under normal synchronous operation, the PTXCLKand PRXCLK are used to receive and transmit data PRXD and PTXD. The clock rate is equal to the data rate. In asynchronous modes, a clock 16 times the bit rate is provided at PTXCLK and PRXCLK.

When BIT 4 is set to a 1 for asynchronous operation, the clocks at the PTXCLK and PRXCLK pins are divided by 16 to provide transmit and receive shift clocks. An internal clock for sampling incoming PRXD data is synchronized by detecting any falling edge on the PRXD data pin. The rising edge of this internal clock, which used to sample incoming data, is delayed from the falling data edge by 8 PRXCLK periods and will continue at this phase and at a PRXCLK/16 frequency until another falling PRXD edge is detected.

If BIT 4 is reset to a 0, the rising edge of PTXCLK is used to sample the data at PRXD, and the falling edge of PTXCLK is used to shift new data onto PTXD.

BIT 3 is cleared to a 1 upon a reset.

BIT 3 Abort

When BIT 3 is set to a 1, a series of consecutive 1s will immediately be transmitted through the PTXD pin on every falling edge of PTXCLK. The message will have been aborted after 2 TX ready interrupts are received. No 0s will be inserted during the abort transmission.

BIT 3 is cleared to a 1 upon a reset.

BIT 2 Send CRC

When BIT 2 is set, the bytes in the TX CRC generator will be inverted and serially transmitted to the PTXD output on the falling edge on PTXCLK as soon as the present data byte transmission is completed. If BIT 1 of the HDLC control register is a 0, a 0 will be inserted into the CRC data stream after five consecutive 1s are transmitted. As soon as the last bit of the CRC is sent, a series of Flags will be automatically sent until another TX control bit is set. No TX Ready interrupts will be generated during the transmission of the CRC bytes. A TX Ready interrupt will be generated as the first bit of each Flag byte is transmitted indicating that the CRC transmission has been completed. This should be cleared by a dummy write to the TX DATA register.

BIT 2 will be cleared to a 0 upon a reset.

BIT 1 Send Data

When BIT 1 is set, the data is the TX data register will be serially transmitted through the PTXD pin on every falling edge of PTXCLK, LSB first. If BIT 1 ofthe HDLC control register is a 0, a 0 will be inserted into the data stream after five consecutive 1s are transmitted. After all eight data register bits have been sent, the HDLC will continue to send data by loading the parallel serial transmit register with new transmit register data, unless either a TX underrun is detected or one of the other TX control bits has been set. This bit will be cleared by the HDLC circuitry as soon as a TX underrun is detected. A TXRDY interrupt will be generated at as the first data of each data byte is transmitted. BIT 1 will be cleared to a 0 upon a reset.

BIT 0 Send Flag

When BIT 0 is set, a pattern of 7E will be transmitted to the PTXD output as soon as either the next data byte or CRC has completed transmission. No 0s will be inserted during the flag transmission. When BIT 0 is reset back to a 0, the HDLC circuitry will complete the flag byte in progress and then transmit according to bits in the TX CONTROL register. TX Ready interrupts will be generated as each byte of flag transmission is initiated.

BIT 0 will be cleared to a 0 upon a reset.

REGISTER DESCRIPTION (continued)

HDLC STATUS REGISTER

HDLC Status Register (HSTAT) SFR Address C3
Byte Addressable
Reset state 00h
Read only register

If any of the HDLC status bits are set, BIT 1 of the HDLC INTERRUPT register (NEW STATUS) will be set if the corresponding bit in the HDLC INTERRUPT ENABLE register is set.

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
INVAL CRC32	INVAL CRC16	TX UNDRN	RX OVRN	INVAL FLAG	ABORT DET	IDLE DET	FLAG DET

BIT 7 Invalid CRC32

BIT 7 will be set if the CRC search mode or the 32-bit CRC is enabled by the HDLC control register and an incorrect remainder for the 32-bit CRC is detected at the last received byte prior to receiving a flag.

BIT 7 will by cleared upon a reset and is cleared by a read of the HDLCSTAT register.

BIT 6 Invalid CRC16

BIT 6 will be set if the CRC search mode or the 16-bit CRC is enabled by the HDLC CONTROL register and an incorrect remainder for the 16-bit CRC is detected at the last received byte prior to receiving a flag.

BIT 6 will by cleared upon a reset and is cleared by a read of the HDLC STAT register.

BIT 5 TX Underrun

When BIT 5 is set, a transmit underrun condition has been detected. This is a condition where the HDLC has finished transmitting a message byte, but no new data has been loaded into the TX DATA register, and no other transmit control bit has been set. This bit will be set only if the SEND DATA bit, BIT 1 of the TXCONTROL register is set. The transmit data is double buffered since the TX data register is downloaded into a TX serial register when the HDLC begins to transmit a new data byte. At the time of loading the TX serial register, a TX READY interrupt is generated. This interrupt must be serviced by either loading a new data byte (the next data byte to be transmitted) into the TX data register, or by setting another TX control bit, before the current data byte has completed transmission (at which point another TX READY interrupt would be generated). If a TX UNDERRUN is detected, the HDLC will abort the current transmission by sending continuous 1s and will reset the SEND DATA control bit in the TX CONTROL register.

BIT 5 will by cleared upon a reset and is cleared by a read of the HDLCSTAT register.

BIT 4 RX Overrun

When BIT 4 is set, a receive overrun condition has been detected. This is a condition where the HDLC has received a new byte, but the last received data byte has not yet been read from the RX data register. As soon as a new data byte has been received in an eight bit serial register, it is loaded into the RX data register and a NEW RX DATA interrupt is generated. If this interrupt is not serviced by reading the RX data register during the time another new data byte is received, the RX OVERRUN status bit will be set. The new received data will not overwrite the older unread data.

BIT 4 will by cleared upon a reset and is cleared by a read of the HDLCSTAT register.

BIT 3 Invalid Flag

When BIT 3 is set, an invalid flag has been detected. This is a condition where a 7E pattern with no inserted 0s is detected, and this pattern did not originate on a byte boundary. Note, two consecutive flags may share a 0, so that the second (or subsequent) flag may not appear to be on a byte boundary. This condition does not result in an invalid flag indication. Instead, the bit counter is reset to 0.

BIT 3 will by cleared upon a reset and is cleared by a read of the HDLC STAT register.

BIT 2 Abort Detect

When BIT 2 is set, an abort condition has been detected. This is a condition where seven consecutive 1s, with no inserted 0s, are received after an active state. BIT 2 will be cleared upon a reset and is cleared by a read of the HDLC STAT register.

BIT 1 Idle Detect

When BIT 1 is set, the first indication of an idle state is detected. An idle state is declared when 15 consecutive 1s, with no inserted 0s, are received after an active state.

BIT 1 will be cleared upon a reset and is cleared by a read of the HDLC STAT register.

BIT 0 Flag Detect

When BIT 0 is set, the HDLC has received a 7E pattern with no inserted 0's. BIT 0 will by cleared upon a reset and is cleared by a read of the HDLCSTAT register.

HDLC INTERRUPT ENABLE REGISTER

HDLC Interrupt Enable Register (HIE) SFR Address C4
Byte Addressable
Reset state 00h

If the bit is set, the corresponding interrupt source is enabled.

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
TX RDY IE	RX RDY IE	TX RDY EN	RX RDY EN	INVAL FLG IE	ABORT IE	IDLE IE	FLAG IE

BIT 7 Transmitter Ready Interrupt Enable

When BIT 7 is set, an HDLC interrupt will be generated if BIT 0 (TX RDY) of the HDLC INTERRUPT register is also set. If BIT 7 is reset to a 0, no HDLC interrupt indication will be given as TX RDY is set. This interrupt enable allows the TX RDY to be a polled bit. Note that BIT 5 of this register is a pre-mask to the TX RDY bit, that is, it will prevent the TX RDY bit from ever being set.

BIT 7 will be cleared upon a reset.

BIT 6 Receiver Ready Interrupt Enable

When BIT 6 is set, an HDLC interrupt will be generated if BIT 1 (RXRDY) of the HDLC INTERRUPT register is also set. If BIT 6 is reset to a 0, no HDLC interrupt indication will be given as RX RDY is set. This interrupt enable allows the RX RDY to be a polled bit. Note that BIT 4 of this register is a pre-mask to the RX RDY bit, that is, it will prevent the RX RDY bit from ever being set.

BIT 6 will be cleared upon a reset.

HDLC INTERRUPT ENABLE REGISTER (continued)

BIT 5 Transmit Ready Enable

BIT 5 is used to enable the TX RDY and TX UNDERRUN interrupt sources. When BIT 5 is set, the transmitter ready indication will set BIT 0 of the HDLC interrupt register. The TX RDY indication will go active as the first bit of a message byte is being transmitted, except during CRC transmission. Also, if this bit is set, the TX underrun condition will result in a NEW STATUS interrupt. If IT5 is reset to a 0, BIT 0 of the HDLC INTERRUPT register will not be set, and no corresponding HDLC interrupt will be generated. Also, a Tx underrun condition, as indicated by BIT 5 of the HDLC STATUS register, will not result in an HDLC interrupt or in setting the NEW STATUS interrupt bit.

BIT 5 will be cleared upon a reset.

BIT 4 Receiver Ready Enable

BIT 4 is used to enable the RX RDY and RX OVERRUN interrupt sources. When BIT 4 is set, the receiver ready indication will set BIT 1 of the HDLC INTERRUPT register. The RX RDY indication will go active when a data byte (a byte that is not a flag, idle, or an abort pattern) is loaded into the RX DATA register. Also, if this bit is set, the RX overrun condition will result in a NEW STATUS interrupt. If BIT 4 is reset to a 0, BIT 1 of the HDLC INTERRUPT register will not be set, and no corresponding HDLC interrupt will be generated. Also, a Rx overrun condition, as indicated by BIT 4 of the HDLC STATUS register, will not result in a HDLC interrupt or in setting the NEW STATUS interrupt bit.

BIT 4 will be cleared upon a reset.

BIT 3 Invalid Flag Interrupt Enable

When BIT 3 is set, a HDLC interrupt will be generated if BIT 3 (INVALID FLAG) of the HDLC STATUS register is also set. If BIT 3 is reset to a 0, BIT 2 (NEW STATUS) of the HDLC INTERRUPT register will not be set as a result of an invalid flag boundary detection and no HDLC interrupt will be generated.

BIT 3 will be cleared upon a reset.

BIT 2 Abort Detect Interrupt Enable

When BIT 2 is set, a HDLC interrupt will be generated if BIT 2 (ABORT DETECT) of the HDLC STATUS register is also set. If BIT 2 is reset to a 0, BIT 2 (NEW STATUS) of the HDLC INTERRUPT register will not be set as a result of an abort pattern detection and no HDLC interrupt will be generated.

BIT 2 will be cleared upon a reset.

BIT 1 Idle Detect Interrupt Enable

When BIT 1 is set, an HDLC interrupt will be generated if BIT 1 (IDLE DETECT) of the HDLC STATUS register is also set. If BIT 1 is reset to a 0, BIT 2 (NEW STATUS) of the HDLC INTERRUPT register will not be set as a result of an idle pattern detection and no HDLC interrupt will be generated.

BIT 1 will be cleared upon a reset.

BIT 0 Flag Detect Interrupt Enable

When BIT 0 is set, a HDLC interrupt will be generated if BIT 0 (FLAG DETECT) of the HDLC STATUS register is also set. If BIT 0 is reset to a 0, BIT 2 (NEW STATUS) of the HDLC INTERRUPT register will not be set as a result of a flag pattern detection and no HDLC interrupt will be generated.

BIT 0 will be cleared upon a reset.

HDLC INTERRUPT REGISTER

HDLC Interrupt Register (HINT) SFR Address C5
Byte Addressable
Read Only register
Reset State 00h

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
0	0	0	0	0	NEW STAT	DATA RDY	TX RDY

This register is used to determine the source of HDLC interrupts. If one or more of these register bits are set, the HDLC interrupt will go active if BIT 0 of the HDLC CONTROL register is set to a 1.

BIT 2 New Status

When BIT 2 is set, an unmasked HDLC status bit from the HDLC STATUS register is set.

BIT 2 will by cleared upon a reset and is cleared by a read of the HDLC STATUS register.

BIT 1 Data Ready

When BIT 1 is set, a new received byte has been loaded into the RX DATA register. Note, received bits that are flag, abort, or idle patterns are not considered data, and will not be loaded into the RX DATA register. All inserted 0s have been removed from this byte. The RX DATA register must be read prior to the completed reception of the next data byte.

BIT 1 will by cleared upon a reset and is cleared by a read of the RX DATA register.

BIT 0 TX READY

BIT 0 is set if any TX control bit is set as the first bit of data, flag or an idle byte is being transmitted. While transmitting the current byte, the HDLC state machines are ready for commands pertaining to the next byte to be transmitted. A new data byte must be loaded into the TX DATA register to clear the TX READY status bit.

BIT 0 will by cleared upon a reset and is cleared by writing to the TX DATA register.

RX DATA REGISTER

RX Data Register (RXD) SFR Address C6
Byte Addressable
Reset state XXh
Read Only

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
RX DAT7	RX DAT6	RX DAT5	RX DAT4	RX DAT3	RX DAT2	RX DAT	RX DAT0

BIT 7 - BIT 0 Received Data Byte

BIT 7 through BIT 0 is the received data byte (LSB is received first) with all inserted 0s removed. A DATA READY interrupt will be generated when a new data byte is received. Reading this register will clear the DATA READY interrupt.

REGISTER DESCRIPTION (continued)

TX DATA REGISTER

TX Data Register (TXD) SFR Address C7
Byte Addressable
Reset state XXh
Write Only

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
TX DAT7	TX DAT6	TX DAT5	TX DAT4	TX DAT3	TX DAT2	TX DAT1	TX DAT0

BIT 7 - BIT 0 Transmit Data Byte

BIT 7 through BIT 0 will be transmitted at the next byte boundary (LSB first) if the TX CONTROL SEND DATA bit is set. The HDLC will insert all necessary 0s. A TX READY interrupt will be generated when a new data byte can be loaded into the TX DATA register. Writing this register will clear the TX READY interrupt.

REGISTER	ADDRESS	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
HDLC CONTROL 0	C0	WRXD	WPTXD	TXD	PRXD	RXD CTRL1	RXD CTRL0	PTXD CTRL1	PTX CTRL0
HDLC CONTROL1	C1	RESET	CLK CTRL	CLK EN	RXCRC32	RXCRC16	TXCRC32	ZERO ID	HDLC EN
TX CONTROL	C2	0	0	0	DIV16 CLK	SEND ABORT	SEND CRC	SEND DATA	SEND FLAG
HDLC STATUS	C3	INVAL CRC32	INVAL CRC16	TX UNDERRUN	RX UNDERRUN	INVAL FLAG	ABORT DETECT	IDLE DETECT	FLAG DETECT
HDLC INT ENABLE	C4	TX RDY IE	RX RDY IE	TX RDY EN	RX RDY EN	INVAL FLAG IE	ABORT IE	IDLE IE	FLAG IE
HDLC INT SOURCE	C5	0	0	0	0	0	NEW STATUS	RX READY	TX READY
RX DATA	C6	RXDAT7	RXDAT6	RXDAT5	RXDAT4	RXDAT3	RXDAT2	RXDAT1	RXDAT0
TX DATA	C7	TXDAT7	TXDAT6	TXDAT5	TXDAT4	TXDAT3	TXDAT2	TXDAT1	TXDAT0

FIGURE 9: HDLC SFR Registers

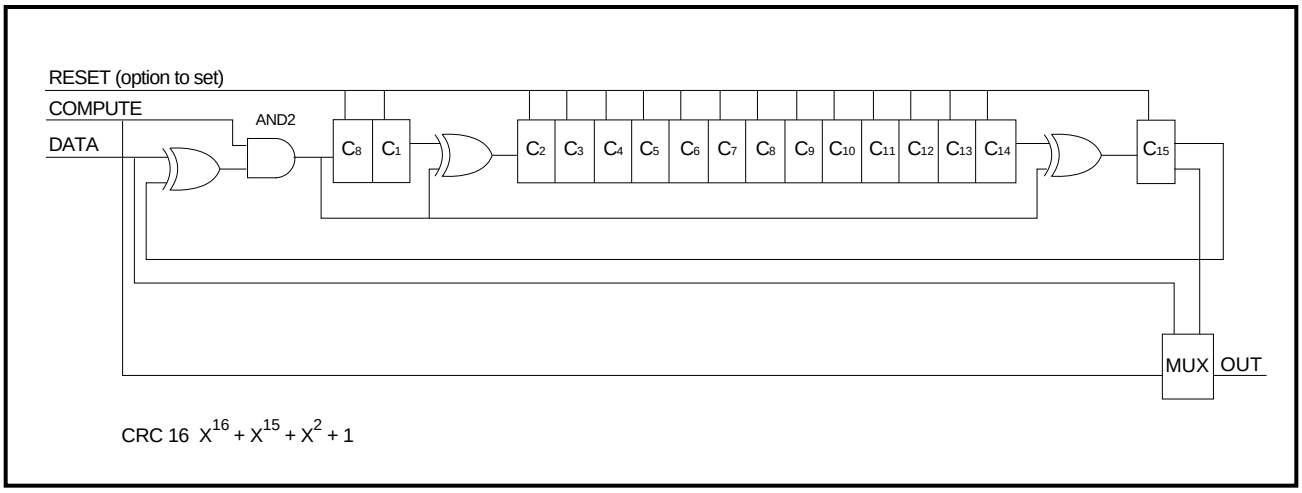


FIGURE 11: CRC 16

The CRC check field is generated by the transmitter. The computation starts with the first transmitted bit after the opening flag and stops at the last data bit prior to the frame check sequence bytes, and excludes inserted 0s. The CRC generating logic is initialized to all 0s. The bits are shifted in and operated on by the generating polynomial, $X^{16} + X^{12} + X^5 + 1$. During CRC transmission, the bytes in the CRC generating logic are transmitted, high order bit first.

The receiver also initializes its CRC computation logic to all ones after the beginning flag. Its polynomial generator (also $X^{16} + X^{12} + X^5 + 1$) should see the same value as the transmitter's polynomial generator as the last data bit is received. Note the receiver's polynomial generator does not process inserted 0s. After the bytes are received in the frame check sequence, a remainder of 1111 0000 1011 1000 should be detected in the receiver's polynomial generator. If this is not the case, it is assumed that the preceding frame was in error and an invalid CRC is declared.

REGISTER DESCRIPTION (continued)

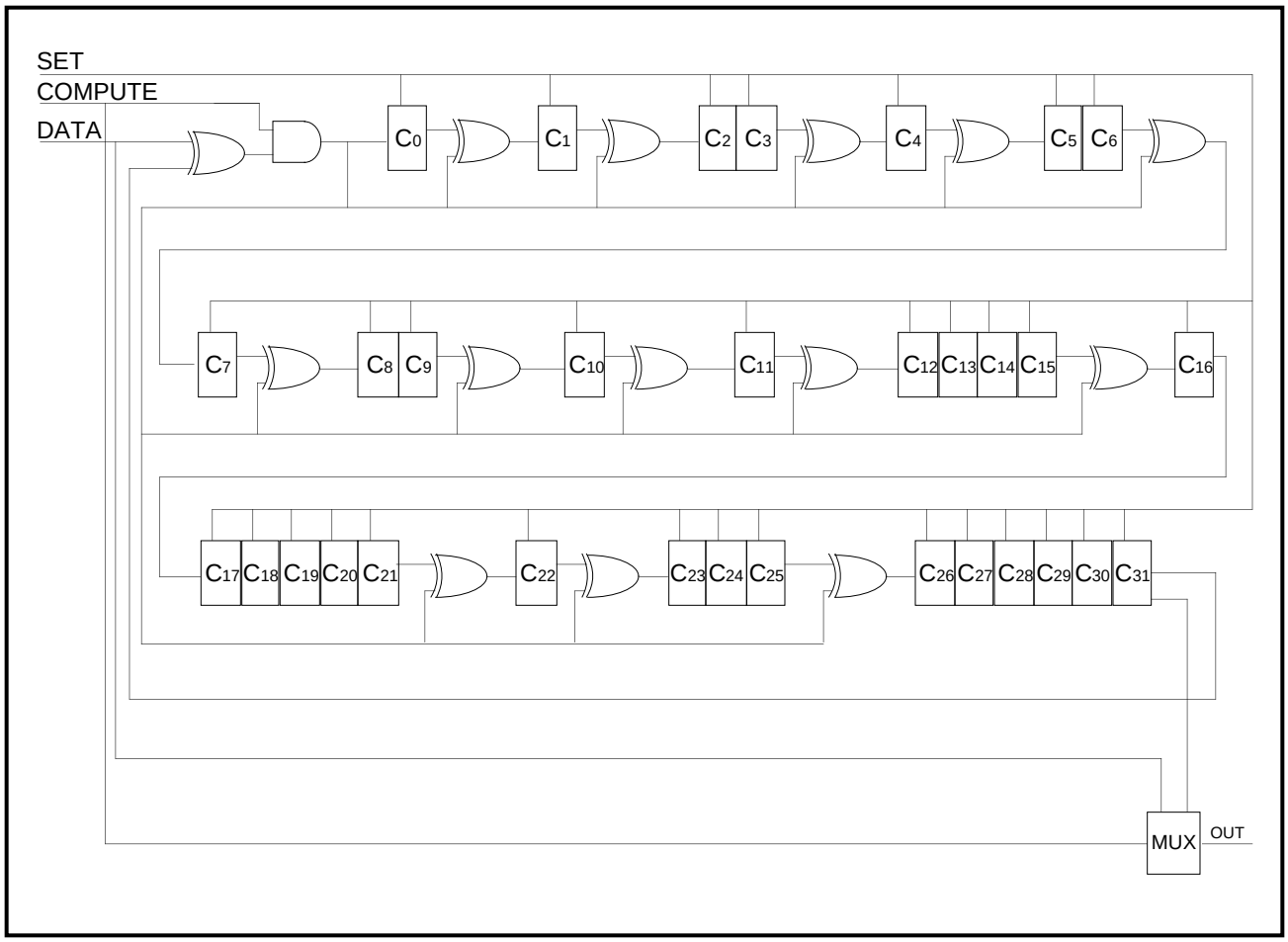


FIGURE 12: 32 Bit CRC

The CRC check field is generated by the transmitter. The computation starts with the first transmitted bit after the opening flag and stops at the last data bit prior to the frame check sequence bytes, and excludes inserted 0s. The CRC generating logic is initialized to all ones. The bits are shifted in and operated on by the generating polynomial, $X^{32} + X^{26} + X^{23} + X^{22} + X^{16} + X^{12} + X^{11} + X^{10} + X^8 + X^7 + X^5 + X^4 + X^2 + X + 1$. During CRC transmission, the bytes in the CRC generating logic are inverted and transmitted, high order bit first. The receiver also initializes its CRC computation logic to all ones after the beginning flag. Its polynomial generator should see the same value as the transmitter's polynomial generator as the last data bit is received. Note the receiver's polynomial generator does not process inserted 0s. After the bytes are received in the frame check sequence, a remainder of 1101 1110 1011 1011 0010 0000 1110 0011 (X^0) through X^{32}, respectively) should be detected in the receiver's polynomial generator. If this is not the case, it is assumed that the preceding frame was in error and an invalid CRC is declared.

PIN DESCRIPTION

NAME	TYPE	DESCRIPTION
$\overline{PSEN}$	O	Program store enable. This output occurs only during a fetch to external program memory. (Active low)
RESET	I	Input which is used to initialize the processor. (Active high)
VND	GND	Negative digital voltage. (Digital Ground)
OSCIN	I	Crystal input for internal oscillator, also input for external source.
OSCOUT	O	Crystal oscillator output.
VPD	I	Positive digital voltage (+5V Digital Supply)
CLKOUT	O	Clock output programmable either OSC/2, OSC/1 or logic 0.
TXD	I	Serial input port to 73D246 from DTE same as RXD UART input.
RXD	O	Serial output port of 73D246 UART to DTE.
PTXCLK	I	Input clock used to transmit data PTXD.
PTXD	O	HDLC Packetizer TX output. This pin can also be programmed to the DTE's TXD output (clear channel) or the value written into bit 6 of the HDLC control register. Connects to modem device TXD.
PRXCLK	I	Input clock used to receive data PRXD.
PRXD	I	Serial input port (from modem device).
$\overline{INT}(\overline{0})$-$\overline{INT}(\overline{2})$	I	External interrupt 0,1 and 2.
USR1(0) -USR1(7)	I/O	User programmable I/O port.
USR2(0) -USR2(7)	I/O	User programmable I/O port.
USR3(0) -USR3(7)	I/O	User programmable I/O port. If the bank select feature is chosen, USR (7) acts as address bit 17 and USR3 data bit 7 is ignored. Register BNKSEL bit 2 (BSEN) enables bank select, bit 1 (BS1) and bit 0 (BS0) select the appropriate bank.
USR4(0) -USR4(7)	I/O	User programmable I/O port also Chip select enable.
$\overline{RD}$	O	Output strobe activated during a bus read. Can be used to enable data onto the bus from an external device. Used as a read strobe to external data memory. (Active low)
$\overline{WR}$	O	Output strobe during a bus write. Used as a write strobe to external data memory. (Active low)
ALE	O	Address Latch Enable output pulse for latching the low byte of the address during accesses to external memory.
AD(0)-AD(7)	I/O	Data bus lines-I/O for devices that require multiplexed address and data bus.
A(0)-A(15)	O	Address bus lines-output latched address for devices that require separate data and address bus.
NO CONNECTS		No connections, leave open.

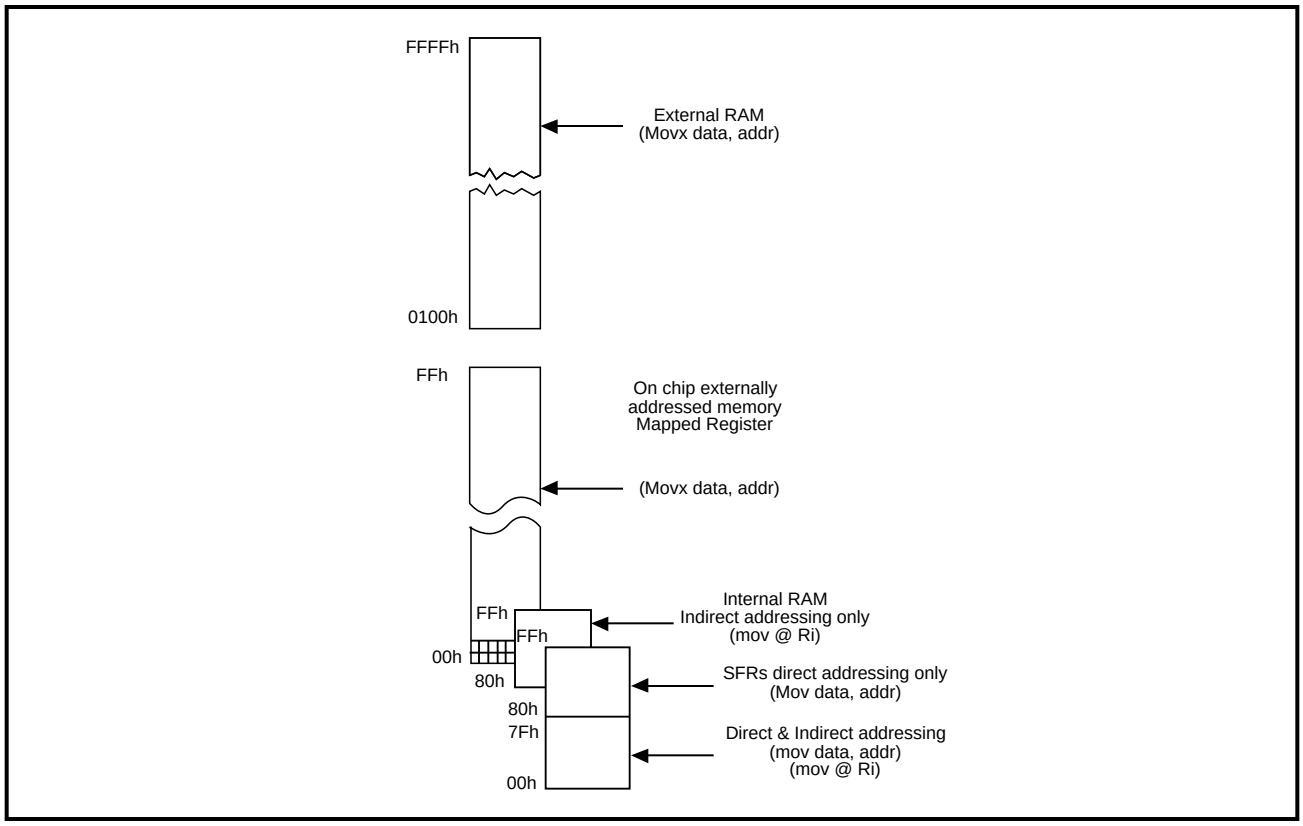


FIGURE 1: Memory Map

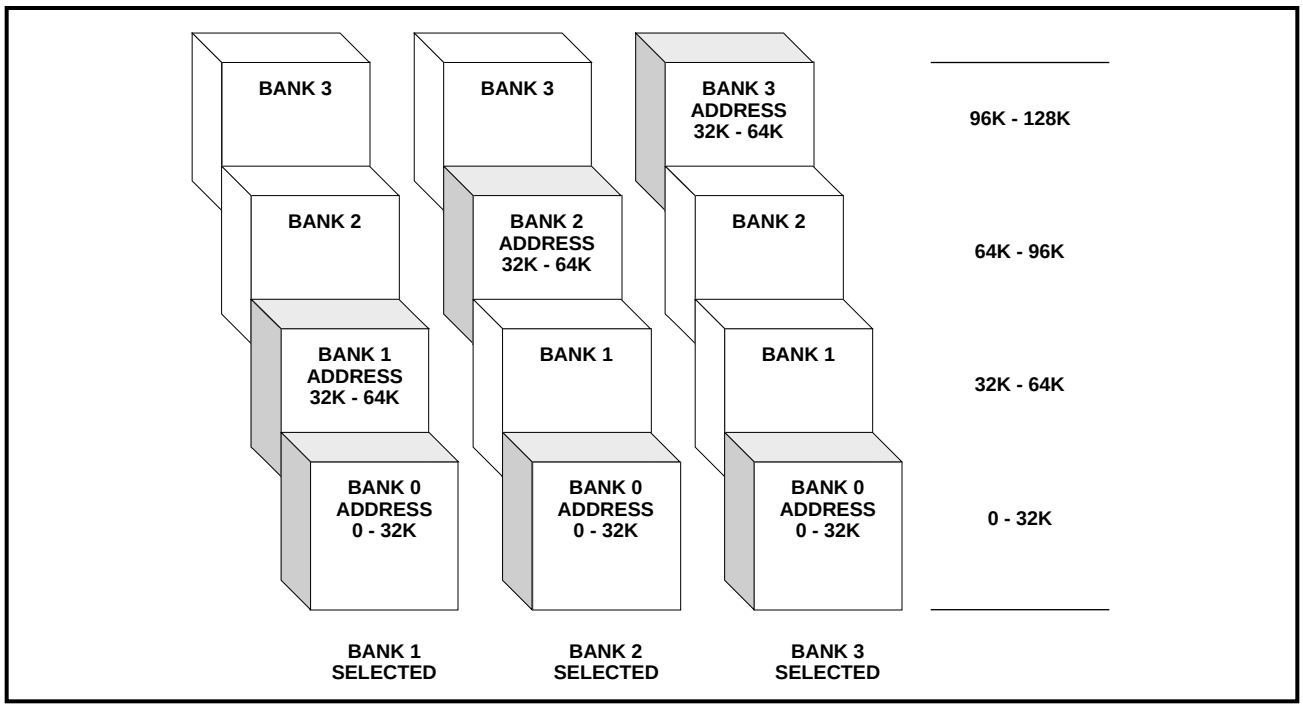


FIGURE 2: 128K of Bank-Selected Program Memory

Address locations 0008 - 00FF are reserved for future use

0008									000F
0000	USER3	DIR3	BNKSEL	USER4	DIR4	CSEN			0007

FIGURE 3: Memory Mapped Registers

F8									FF
F0	B								F7
E8									EF
E0	ACC								E7
D8	*USER2	*DIR2							DF
D0	PSW								D7
C8	T2CON		RCAP2L	RCAP2H	TL2	TH2			CF
C0	*HDLC0	*HDLC1	*TXC	*HSTAT	*HIE	*HINT	*HRXD	*HTXD	C7
B8	IP								BF
B0	P3								B7
A8	IE								AF
A0	P2								A7
98	SCON	SBUF							9F
90	*USER1	*DIR1	*IDIR						97
88	TCON	TMOD	TL0	TL1	TH0	TH1			8F
80	P0	SP	DPL	DPH				PCON	87

BIT ADDRESSABLE

* Unique to the SSI 73D246. There may not be an equivalent function on an 8052.

FIGURE 4: 73D246 SFR Map

ELECTRICAL SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Operation outside these rating limits may cause permanent damage to this device.

PARAMETER	RATING
Supply Voltage	-0.5 to +7.0V
Pin Input Voltage	-0.5 to Vcc +0.5V
Storage Temperature	-55 to +150°C

RECOMMENDED OPERATING CONDITIONS

Supply Voltage	4.5 to 5.5V
Oscillator Frequency	DC to 22 MHz
Operating Temperature	-40 to +85°C

DC CHARACTERISTICS

PARAMETER		CONDITION	MIN	NOM	MAX	UNIT
Input Low Voltage (Except OSCIN, RESET, TEST)	VIL		-0.5		0.2 Vcc - 0.1	V
Input Low Voltage OSCIN, RESET, TEST	VIL		-0.5		0.2 Vcc	V
Input High Voltage (Except OSCIN, RESET, TEST)	VIH		0.2 Vcc + 0.9		Vcc + 0.5	V
Input High Voltage OSCIN, RESET, TEST	VIH		0.7 Vcc		Vcc + 0.5	V
Output Low Voltage (Except OSCOUT)	VOL	Iol = 3.2 mA			0.45	V
Output Low Voltage OSCOUT	VOLOSC	Iol = 2.0 mA			0.45	V
Output High Voltage (Except OSCOUT)	VOH	Ioh = 3.2 mA	Vcc - 0.45			V
Output High Voltage OSCOUT	VOHOSC	Ioh = 2.0 mA	Vcc - 0.45			V
Input Leakage Current (Except OSCIN)	IIL	Vss < Vin < Vcc			±1	µA
Input Leakage Current OSCIN	IIL	Vss < Vin < Vcc	±1		60	µA
Maximum Power Supply Normal Operation	IDD1	22 MHz 30 pF/pin			40	mA
Maximum Power Supply Idle Mode	IDD2	22 MHz			6	mA
Maximum Power Supply Power Down Mode	IDD3				10	µA
Pin Capacitance	CIO	@1 MHz			10	pF

AC TIMING

PARAMETER		CONDITION	MIN	NOM	MAX	UNIT
Oscillator Frequency	FOSC		0		22.2	MHz
Oscillator Period	TOSC		45			ns
ALE Pulse Width	TLHLL		2TOSC - 10			ns
Address Valid To ALE low	TAVLL		TOSC			ns
Address Valid to ALE low	TLLAX		TOSC - 10			ns
ALE low to $\overline{\text{PSEN}}$ low	TLLPL		TOSC - 10			ns
$\overline{\text{PSEN}}$ Pulse width low	TPLPH		3TOSC - 20			ns
$\overline{\text{PSEN}}$ Low to Valid Inst In	TPLIV				3TOSC - 50	ns
Address to Valid Inst In	TAVIV				5TOSC - 50	ns
Input Instr Hold-$\overline{\text{PSEN}}$ Hi	TPXIX		0			ns
$\overline{\text{PSEN}}$ Instr Float-$\overline{\text{PSEN}}$ Hi	TPXIZ				20+	ns
PSEN Low to Address HIZ	TPLAZ				10	ns
$\overline{\text{RD}}$ Pulse Width	TRLRH		6TOSC - 20			ns
$\overline{\text{WR}}$ Pulse Width	TWLWH		6TOSC - 20			ns
$\overline{\text{RD}}$ Low to Valid Data In	TRLDV				5TOSC - 50	ns
Data Hold After $\overline{\text{RD}}$	TRHDX		0			ns
Data Float After $\overline{\text{RD}}$	TRHDZ				20+	ns
ALE Low to Valid Data In	TLLDV				8TOSC - 50	ns
ALE low to $\overline{\text{RD}}$ or $\overline{\text{WR}}$ low	TLLWL		3TOSC - 20		3TOSC + 20	ns
Data Valid to $\overline{\text{WR}}$ low	TQVWX		TOSC			ns
Data Hold After $\overline{\text{WR}}$ Hi	TWHQX		TOSC - 10			ns
$\overline{\text{RD}}$ low to Address Float	TRLAZ				10	ns

The SSI 73D246 timing is very similar to the 8051 except in AD(7:0), the multiplexed address data port known as port 0 in the 8051. Its timing has been altered somewhat to allow more address setup time for peripheral program ROM and memory mapped peripherals. This is important at 22 MHz operation. The 8052 has a "dead" cycle of one oscillator period between the time $\overline{\text{PSEN}}$ goes high, indicating that the instruction ROM will release the AD(7:0) bus, to the time the processor will assert address on the AD(7:0) bus. This dead time of one whole oscillator cycle has been shortened to approximately 15 ns after the $\overline{\text{PSEN}}$ (or $\overline{\text{RD}}$) signal is sensed to be high.

The timing specification for TPXIZ and TRHDZ of a maximum of 15 ns can be violated at the expense of increased operating current. The SSI 73D246 will begin asserting the AD(7:0) bus approximately 20 ns after $\overline{\text{PSEN}}$ or $\overline{\text{RD}}$ go high. This should be ample time for the control signals in the peripheral device to turn off their pad drivers. If the peripheral device does not release the bus promptly, there will be a short time where there is contention on the AD(7:0) bus between the processor and peripheral. This should not prevent proper operation, but it will increase operating current slightly.

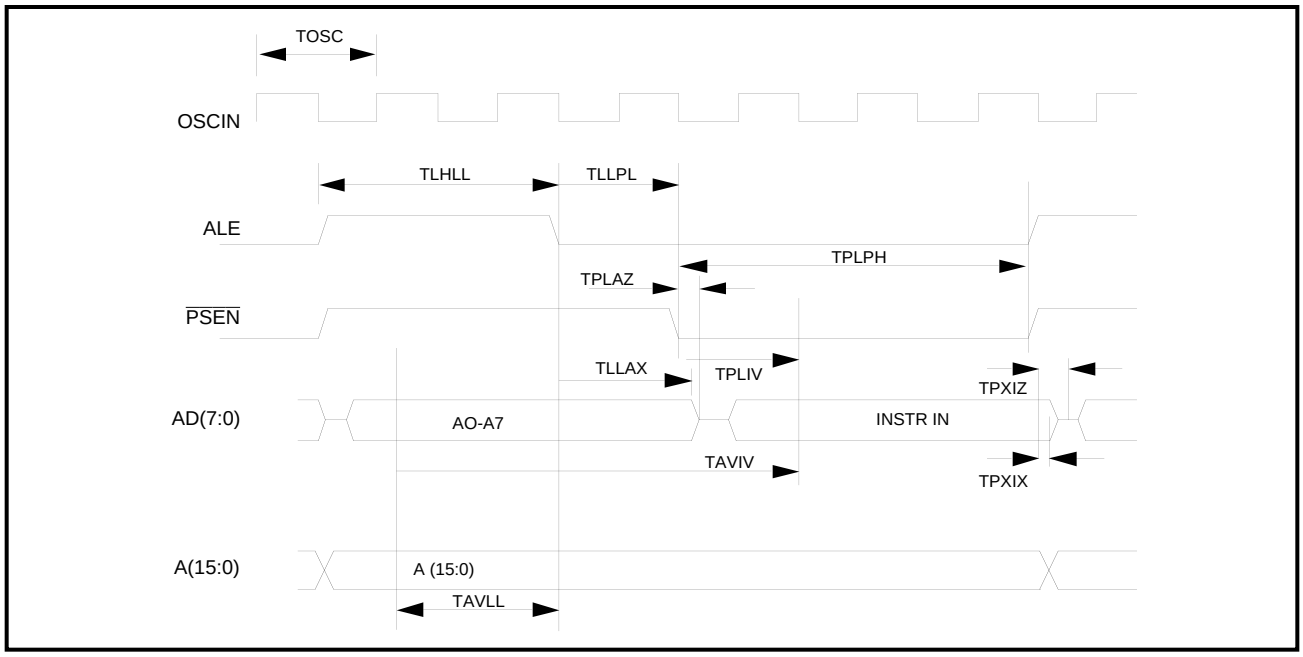


FIGURE 5: External Program Memory Read Cycle

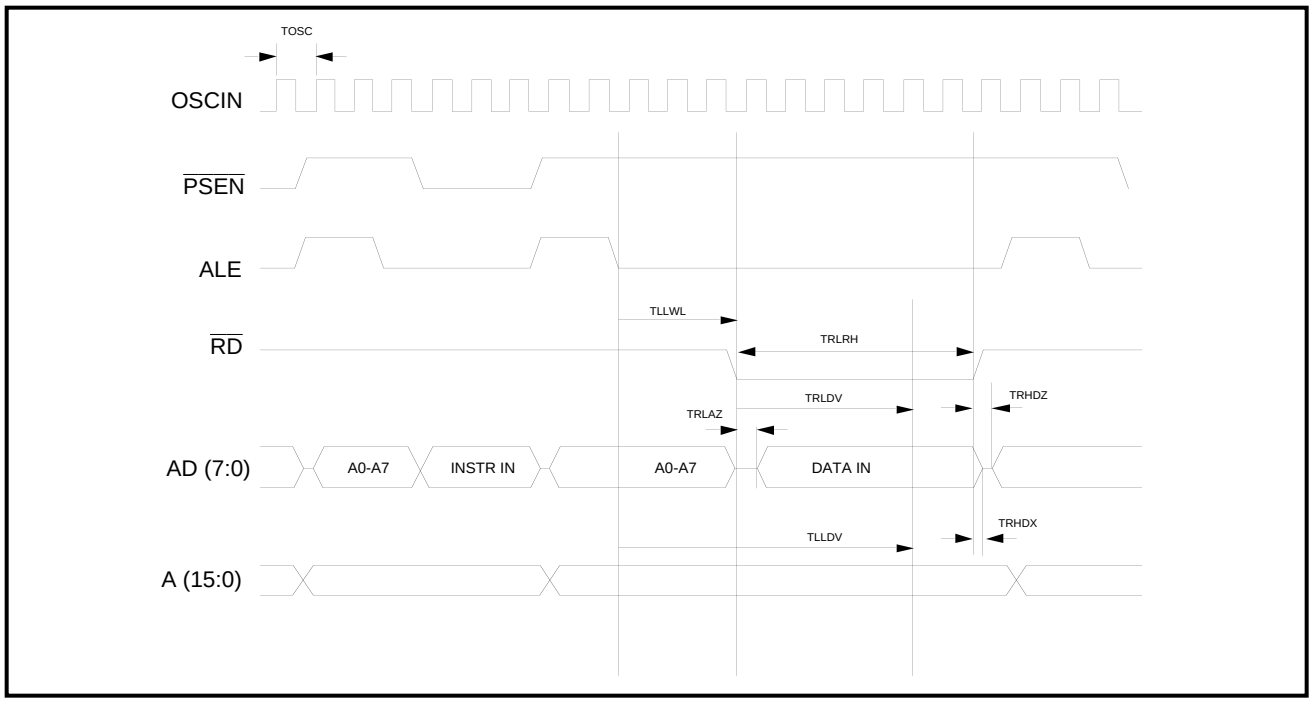


FIGURE 6: External Data Memory Read Cycle

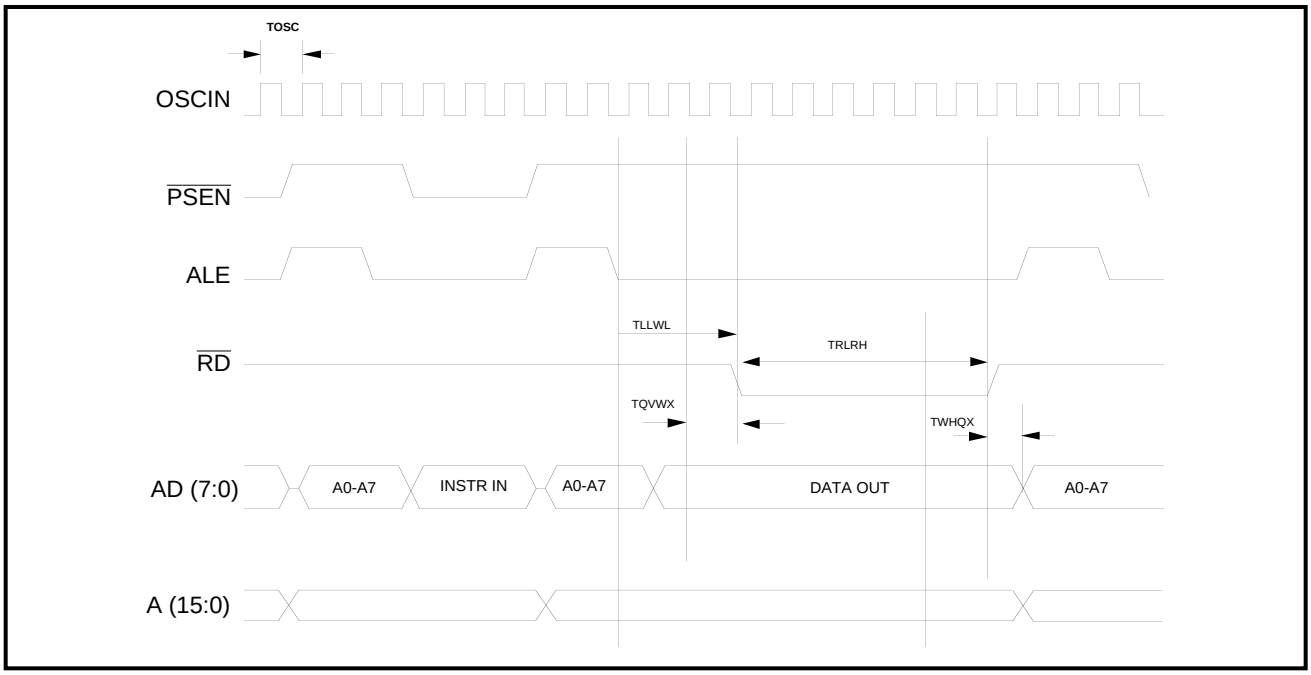


FIGURE 7: External Data Memory Write Cycle

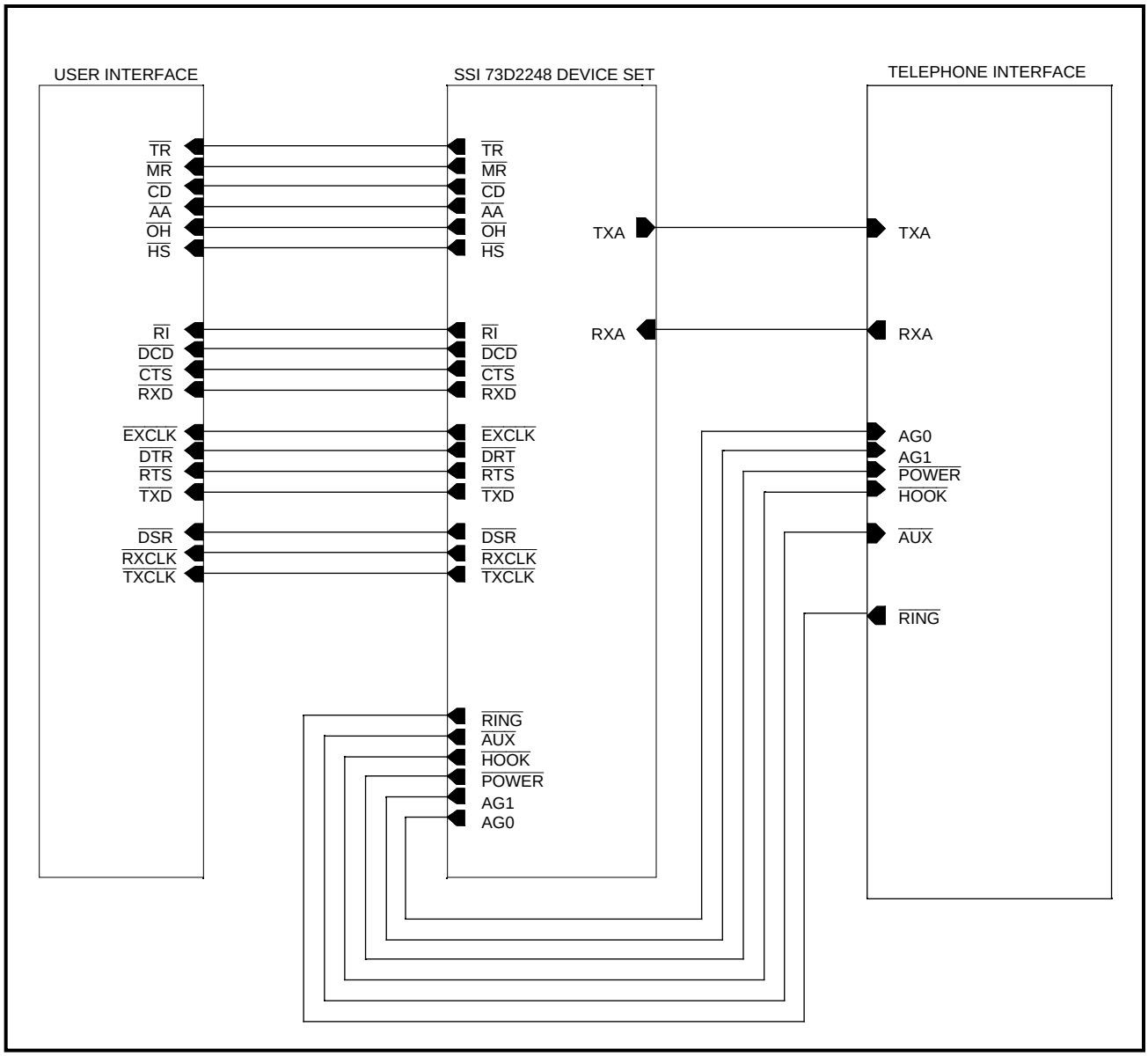


FIGURE 13: Modem Block Diagram

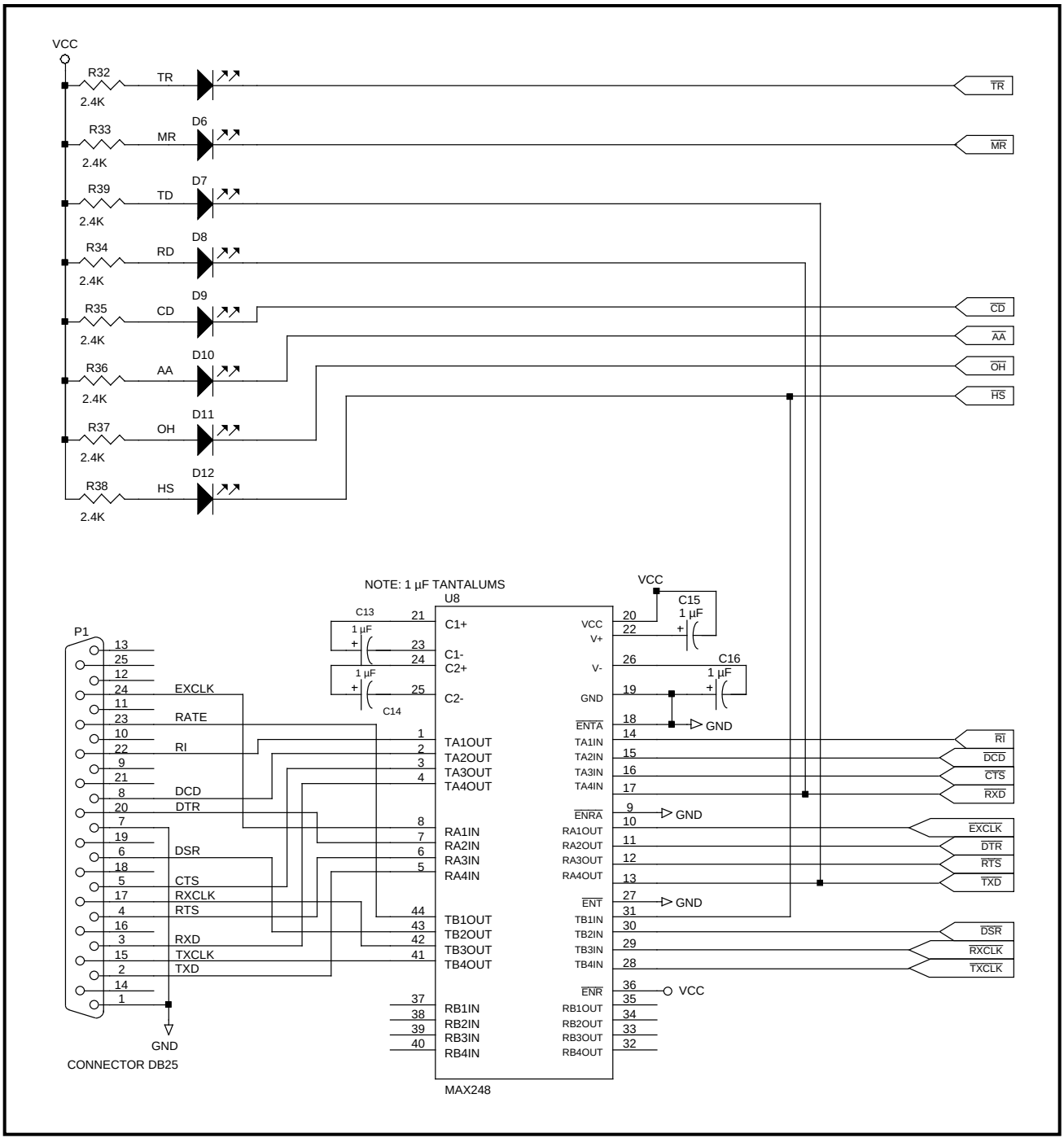
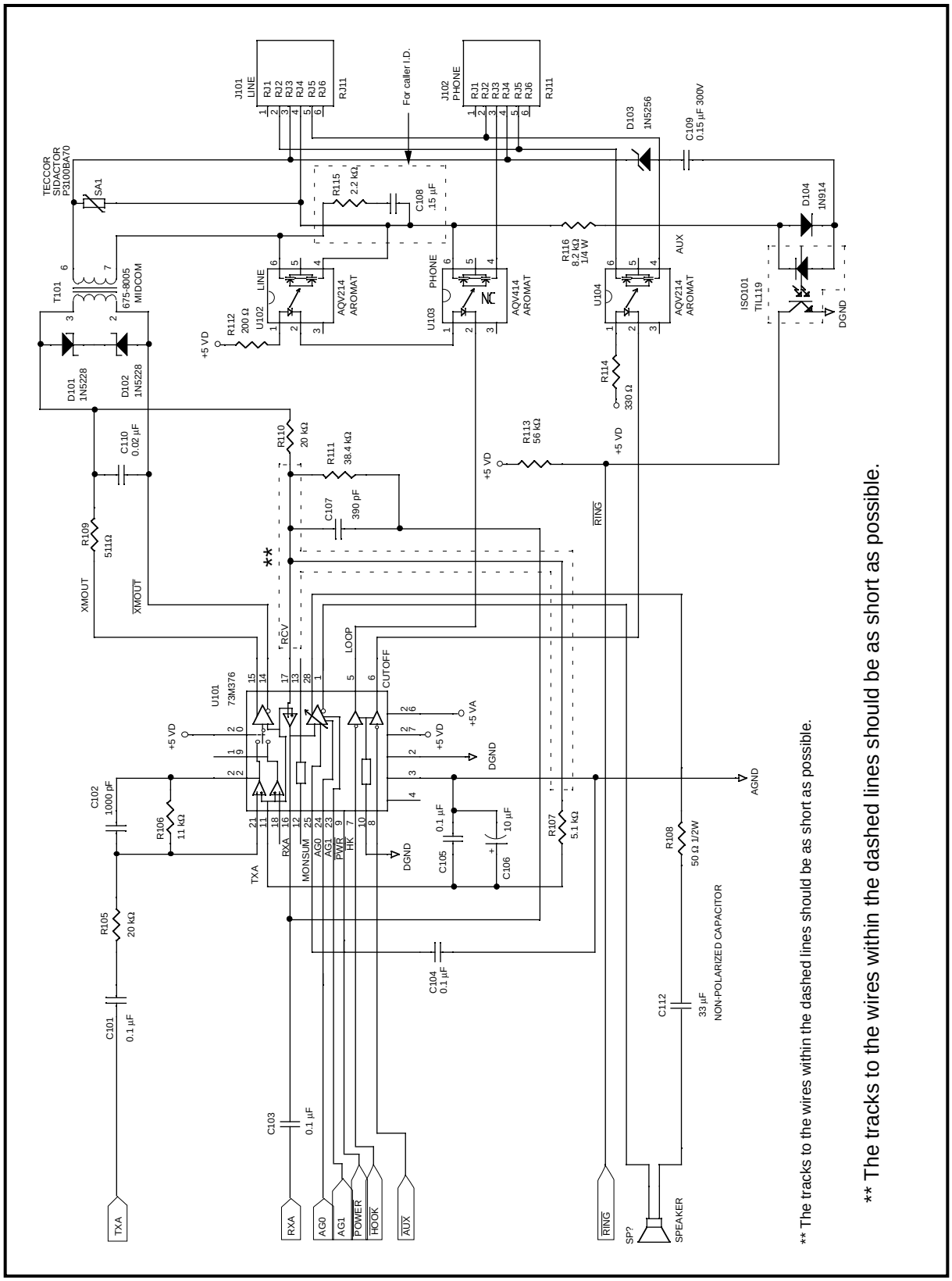


FIGURE 14: Display and User Interface



** The tracks to the wires within the dashed lines should be as short as possible.

FIGURE 15: Telephone Interface

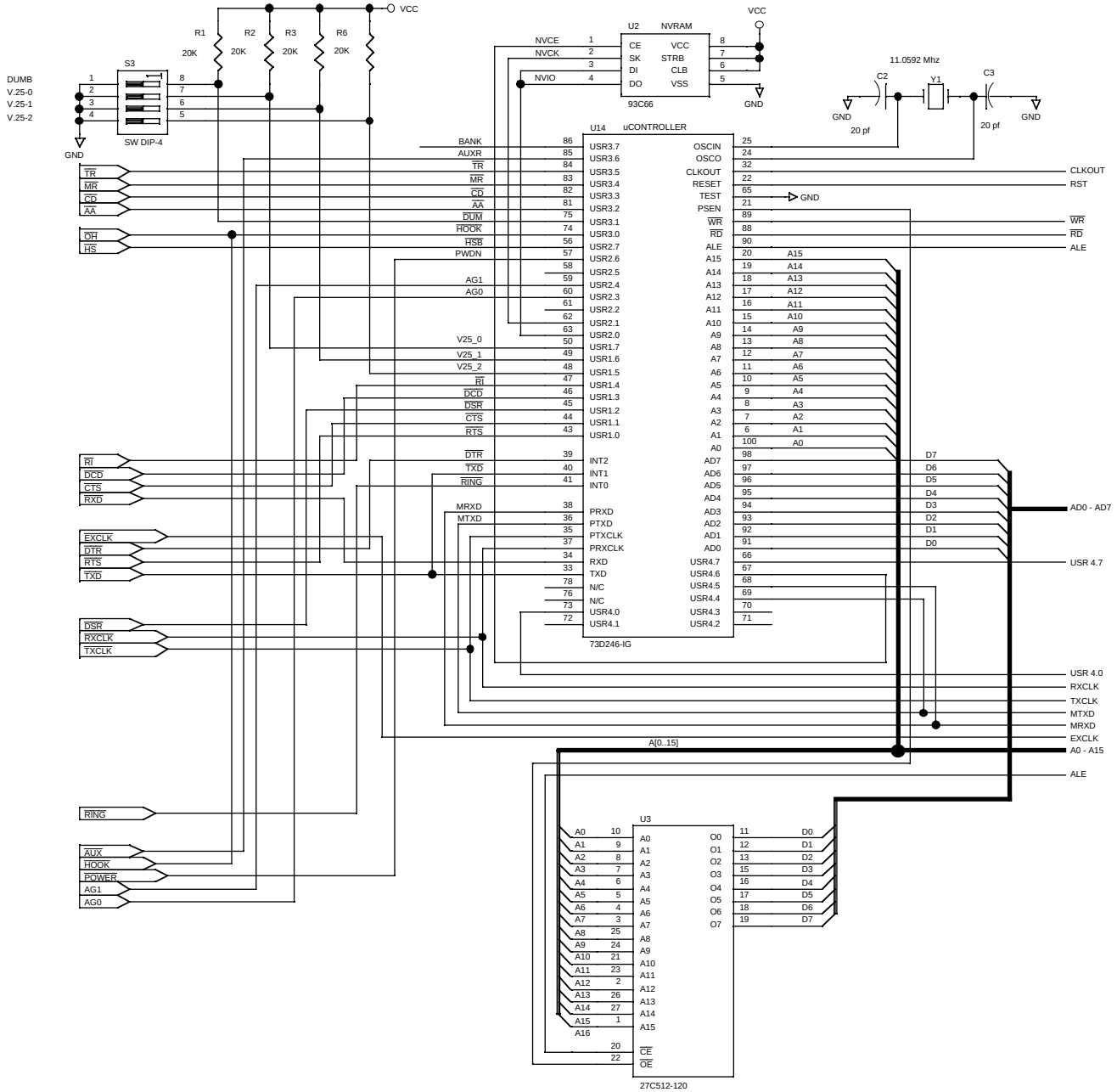


FIGURE 16A: 2248 Modem System Interconnect - Front End

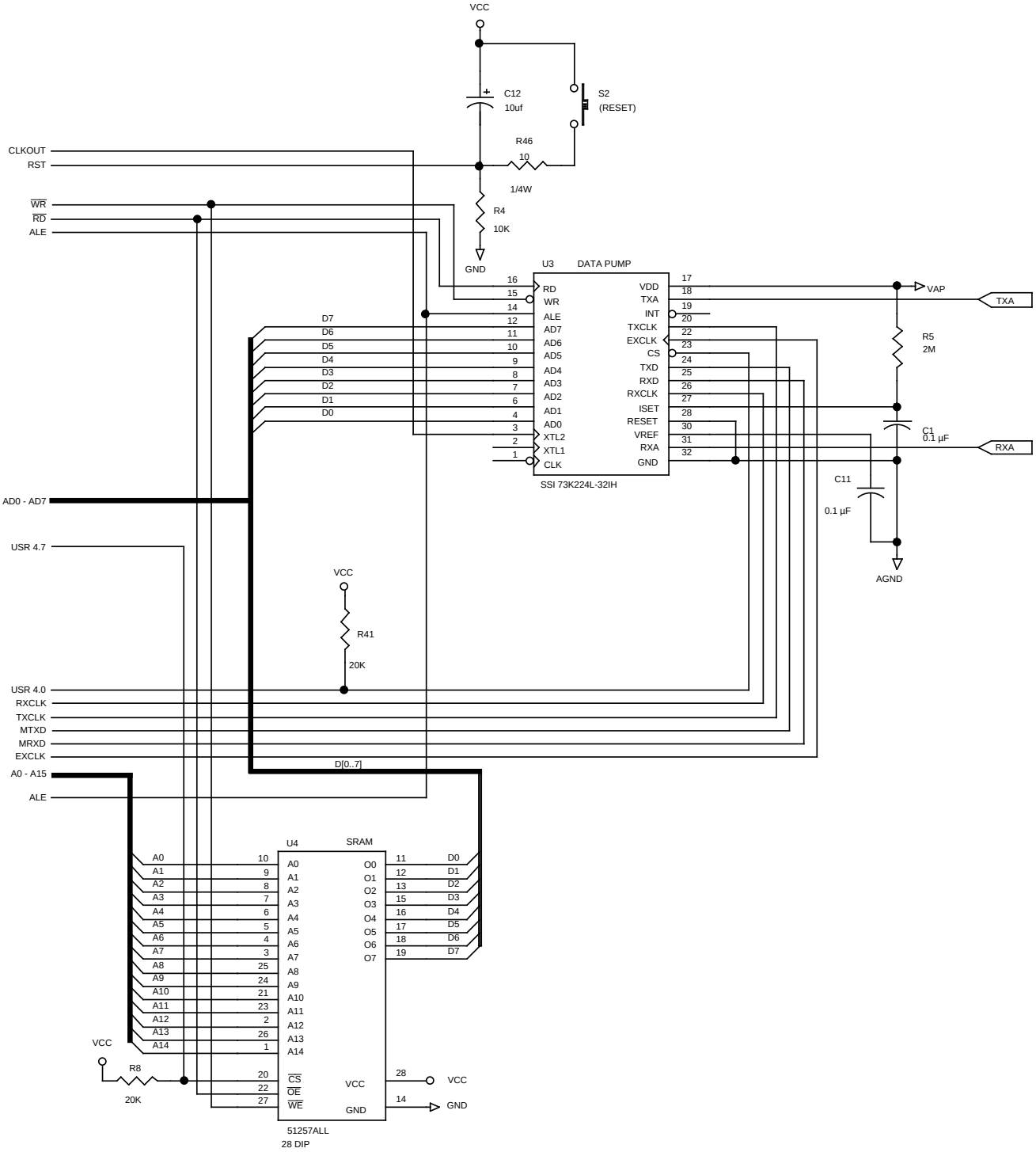


FIGURE 16B: 2248 Modem System Interconnect - Back End

100-Pin PGA (For developement purposes only; not a production package.)

BOND PRD	PIN #	SIGNAL NAME
1	B2	NO CONNECT
2	B1	NO CONNECT
3	C1	USR26
4	C2	USR27
5	D2	USR25
6	D1	USR24
7	E2	USR23
8	E1	USR22
9	F3	USR21
10	F2	USR20
11	F1	VPD
12	G2	GND
13	G3	USR47
14	G1	USR46
15	H1	USR45
16	H2	USR44
17	H3	USR43
18	J1	USR42
19	J2	USR41
20	K1	USR40
21	K2	USR30
22	L1	USR31
23	M1	NO CONNECT
24	L2	NO CONNECT
25	N1	NO CONNECT
26	M2	NO CONNECT
27	N2	NO CONNECT
28	M3	NO CONNECT
29	N3	USR32
30	M4	USR33
31	N4	USR34
32	M5	USR35
33	N5	USR36
34	L6	USR37
35	M6	GND
36	N6	$\overline{RD}$

BOND PRD	PIN #	SIGNAL NAME
37	M7	$\overline{WR}$
38	L7	ALE
39	N7	D0
40	N8	D1
41	M8	D2
42	L8	D3
43	N9	D4
44	M9	D5
45	N10	D6
46	M10	D7
47	N11	VPD
48	N12	A0
49	M11	NO CONNECT
50	N13	NO CONNECT
51	M12	NO CONNECT
52	M13	NO CONNECT
53	L12	NO CONNECT
54	L13	A1
55	K12	A2
56	K13	A3
57	J12	A4
58	J13	A5
59	H11	A6
60	H12	A7
61	H13	A8
62	G12	A9
63	G11	A10
64	G13	A11
65	F13	A12
66	F12	A13
67	F11	A14
68	E13	A15
69	E12	$\overline{PSEN}$
70	D13	RESET
71	D12	GND
72	C13	OSCOUT

100-Pin PGA (continued)

BOND PRD	PIN #	SIGNAL NAME
73	B13	OSCIN
74	C12	NO CONNECT
75	A13	NO CONNECT
76	B12	NO CONNECT
77	A12	NO CONNECT
78	B11	VPD
79	A11	CLKOUT
80	B10	TXD
81	A10	RXD
82	B9	PTXCLK
83	A9	PTXD
84	C8	PRXCLK
85	B8	PRXD
86	A8	$\overline{INT}$2

BOND PRD	PIN #	SIGNAL NAME
87	B7	$\overline{INT}$1
88	C7	$\overline{INT}$0
89	A7	GND
90	A6	USR10
91	B6	USR11
92	C6	USR12
93	A5	USR13
94	B5	USR14
95	A4	USR15
96	B4	USR16
97	A3	USR17
98	A2	NO CONNECT
99	B3	NO CONNECT
100	A1	NO CONNECT

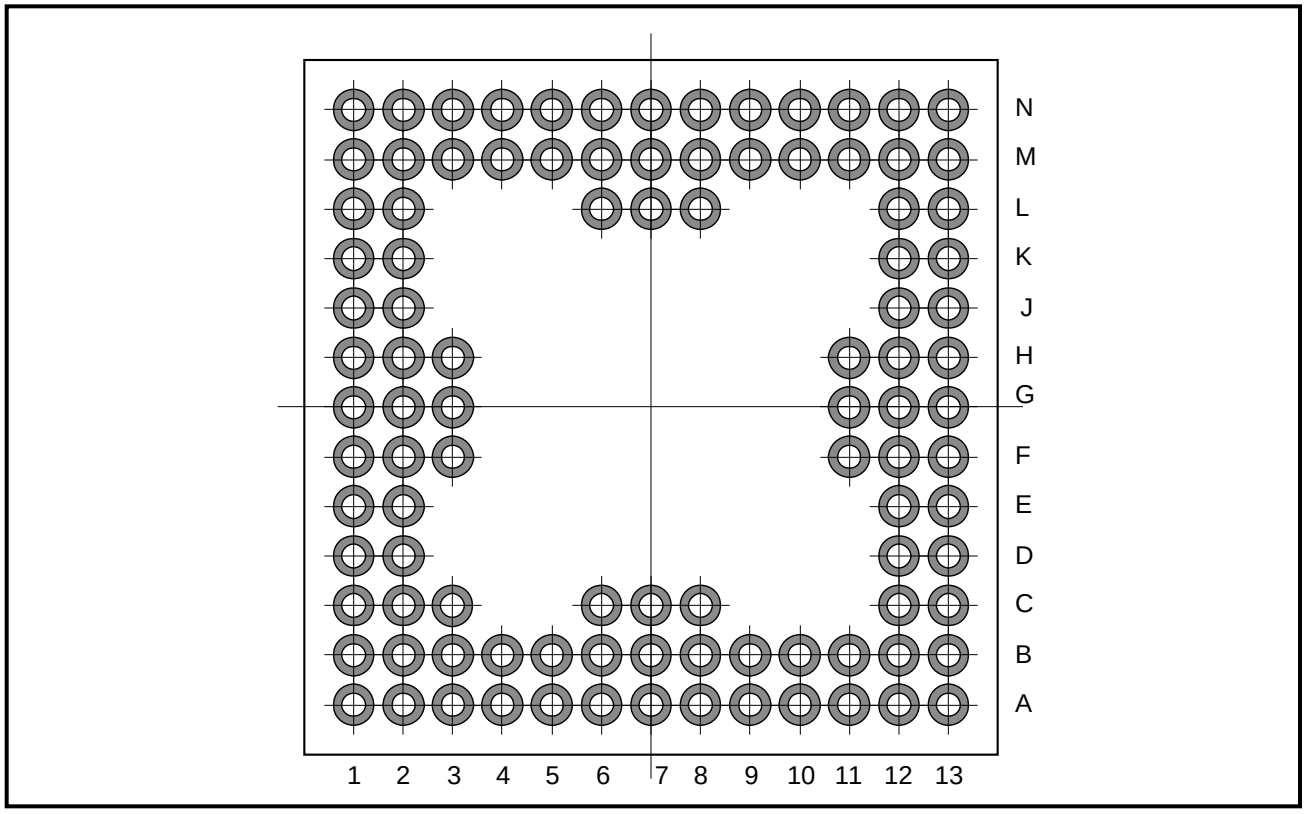
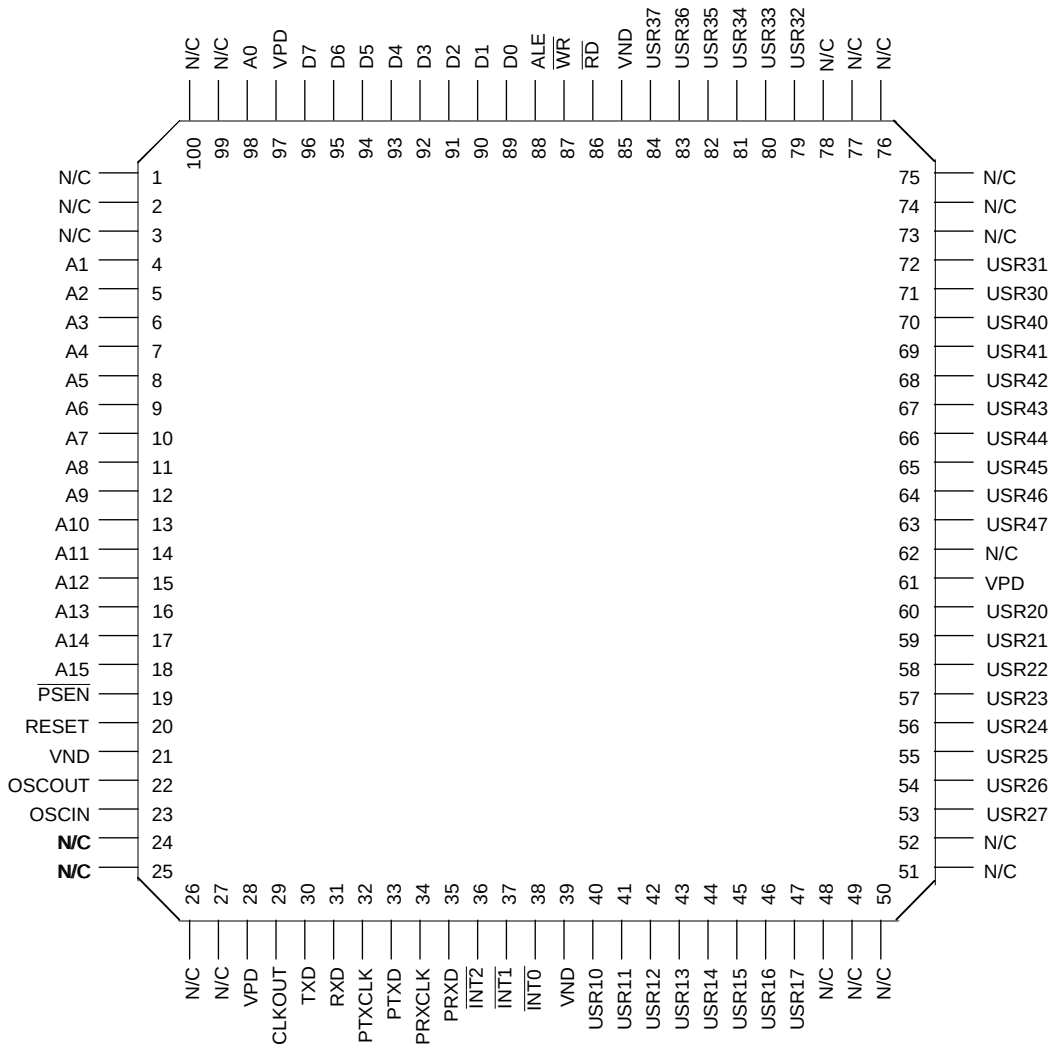


FIGURE 17: 100-Pin Plug-In Package

PACKAGE PIN DESIGNATIONS

(Top View)

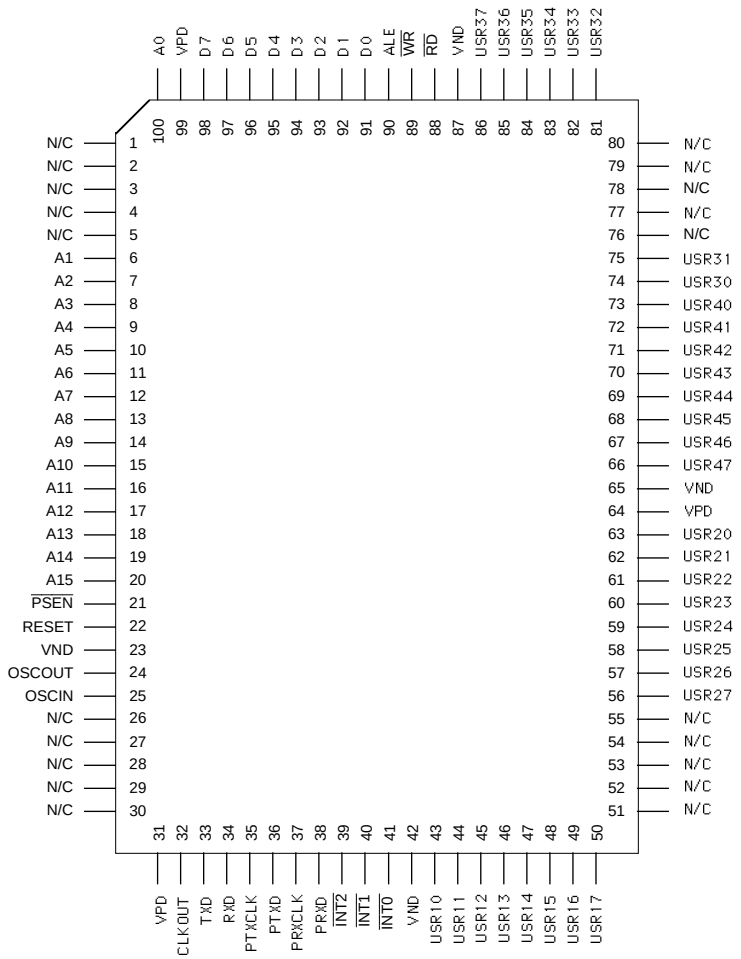


100-Lead TQFP

CAUTION: Use handling procedures necessary for a static sensitive component.

PACKAGE PIN DESIGNATIONS

(Top View)



100-Lead QFP

CAUTION: Use handling procedures necessary for a static sensitive component.

Advance Information: Indicates a product still in the design cycle, and any specifications are based on design goals only. Do not use for final design.

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SSI 73D2910 VERSUS SSI 73D246

The 73D2910 and the 73D246 are basically the same microprocessor with the following exceptions:

ALE GOES HIGH IN POWER DOWN MODE

In the 73D246, ALE goes low in Power Down mode. For the ROM to be in its lowest current state both ALE and PSEN must be high. The 73D2910 has been changed so that ALE will go high. The 73D2910 has been changed so that ALE will go high during the Power mode.

MODIFICATIONS TO PORT1 (D (7:0) DIRECTION CONTROL

The 73D246 complies with the 8052 timing.

To accommodate processor peripherals when operating at 22 MHz, the 73D2910 can provide a 1.8432 MHz clock.

The USR5 register allows for 2 additional input pins. In normal operation these pins can be used as general purpose inputs. In Power Down mode, the user can program either rising or falling transitions or logical combinations of these pins to wake up the chip.

CHANGES TO ALLOW READING OF THE INTERRUPT PINS

The 37D246 does not allow reading of the interrupt pins through a register. The 73D2910 has added capability so that the values of the INT (2:0) pins can be read through a register. The value of these pins are reflected in BIT (5:3) of register 92h.

ADDITIONAL REGISTER FOR CLOCK CONTROLS

The 73D246 does not include a register for clock control. The 73D2910 has an additional register for clock control and an additional clock output used for supplying a 1.8432 MHz clock to an external UART. The clock control bits in the 73D246 HDLC control register 1 (bits 5 and 6) have been moved to this register. A new feature that allows the programmer to divide the processor clock by 2 has been added. This may be useful for saving processor power.

CHANGES TO HDLC BLOCK

The 73D246 does not support CCITT 16-bit polynominal. The 73D2910 allows a CRC16 polynomial as well as the CCITT 16-bit polynomial. The HDLC control register 1 was altered for programming CRC type. These bits replace CLK1 outputs controls, which moved to the clock control register.

73D246 HDLC Control Register

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
HDLC RST	CLK CTRL	CLK EN	RX CRC 32	RX CRC 16	TX CRC CTRL	ZERO ID	HDLC EN

73D2910 HDLC Control Register

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
HDLC RST	CCITT	CRC PRE	RX CRC 32	RX CRC 16	TX CRC CTRL	ZERO ID	HDLC EN

NOTE: The 73D246 will be available until June 1994.

CHANGES TO HDLC BLOCK (continued)

The 73D2910 will reset the SEND DATA bit in the TX CONTROL register. The 73D246 will indicate an abort by sending 7 continuous ones. Depending on the data in the transmit buffer when the overrun occurred, the data stream may contain a zero followed by 7 ones, or may be continuous stream of ones. The zero is unacceptable in asynchronous protocols. This has been fixed so that an abort is followed by a continuous stream of ones until the processor writes the TX CONTROL register.

A problem was found in asynchronous modes when the 16x clock control bit was set. The 73D246 would resynchronize on any falling edge of data, count 8 16x clock pulses, and then shift in the data to the serial parallel register receive register. The delay through the synchronization circuit would allow a possible double sample of a 0-bit if the HDLC lost synchronization with the data stream (long delay between characters.) This was a random failure.

FIXED PROBLEMS

The interrupt controller did not handle a return from a level 1 interrupt into an existing level 0 interrupt correctly. The processor lost track of the fact that it was in an existing interrupt, hence another level 0 interrupt condition (it could also interrupt itself again if level or condition sensitive) was presented. This will send the processor into an unkown invalid state. The problem was found in the interrupt controller PLA state equations. A software work around was implemented in the 73D2248. The PLA was regenerated for the 73D2910 with the appropriate fix.

A problem was found in the TIMER0/1 interval mode where the lsb. of the upper 8 bits could be corrupted. The external signal level of the INT signal that enables the timer was synchronized to the processor's internal states in the 73D2910.

NOTE: The 73D246 will be available until June 1994.

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SSI 73K224L
V.22bis/V.22/V.21, Bell 212A/103 Single-Chip Modem

December 1992

DESCRIPTION

The SSI 73K224L is a highly integrated single-chip modem IC which provides the functions needed to construct a V.22bis compatible modem, capable of 2400 bit/s full-duplex operation over dial-up lines. The SSI 73K224L offers excellent performance and a high level of functional integration in a single 28-pin DIP. This device supports V.22bis, V.22, V.21, Bell 212A and Bell 103 modes of operation, allowing both synchronous and asynchronous communication.The SSI 73K224L is designed to appear to the systems designer as a microprocessor peripheral, and will easily interface with popular single-chip microprocessors (80C51 typical) for control of modem functions through its 8-bit multiplexed address/data bus or via an optional serial control bus. An ALE control line simplifies address demultiplexing. Data communications normally occur through a separate serial port. The SSI 73K224L is pin and software compatible with the SSI 73K212L and SSI 73K222L single-chip modem ICs, allowing system upgrades with a single component change.

The SSI 73K224L operates from a single +5 V supply for low power consumption.

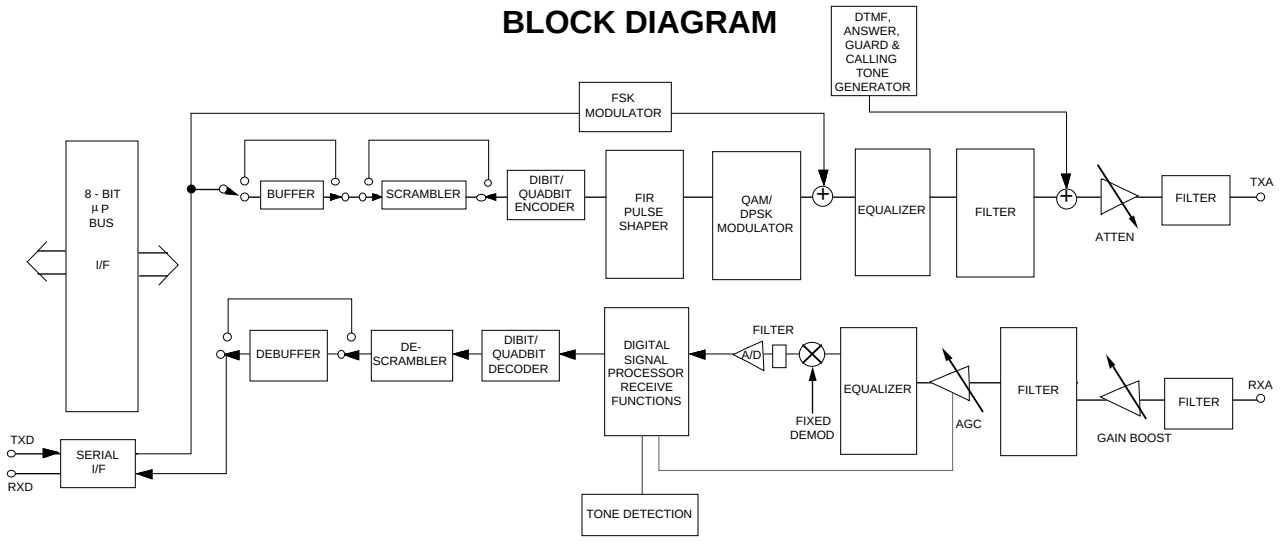
The SSI 73K224L is ideal for use in either free-standing or integral system modem products where full-duplex

(Continued)

FEATURES

- **One-chip multi-mode V.22bis/V.22/V.21 and Bell 212A/103 compatible modem data pump**
- **FSK (300 bit/s), DPSK (600, 1200 bit/s), or QAM (2400 bit/s) encoding**
- **Pin and software compatible with other SSI K-Series 1-chip modems**
- **Interfaces directly with standard microprocessors (8048, 80C51 typical)**
- **Parallel microprocessor bus for control with a wide range of package options**
- **Selectable asynch/synch with internal buffer/ debuffer and scrambler/descrambler functions**
- **All synchronous and asynchronous operating modes (internal, external, slave)**
- **Adaptive equalization for optimum performance over all lines**
- **Programmable transmit attenuation (16 dB, 1 dB steps), selectable receive boost (+18 dB)**
- **Call progress, carrier, answer tone, unscrambled mark, S1, and signal quality monitors**
- **DTMF, answer and guard tone generators**
- **Test modes available: ALB, DL, RDL, Mark, Space, Alternating bit, S1 pattern**
- **CMOS technology for low power consumption (typically 100 mW @ 5V) with power-down mode (15 mW @ 5V)**
- **TTL and CMOS compatible inputs and outputs**

BLOCK DIAGRAM



DESCRIPTION (Continued)

2400 bit/s data communications over the 2–wire switched telephone network is desired. Its high functionality, low power consumption, and efficient packaging simplify design requirements and increase system reliability.

The SSI 73K224L is designed to be a complete V.22bis compatible modem on a chip. The complete modem requires only the addition of the phone line interface, a control microprocessor, and RS-232 level converter for a typical system. Many functions were included to simplify implementation of typical modem designs. In addition to the basic 2400 bit/s QAM, 600/1200 bit/s DPSK and 300 bit/s FSK modulator/demodulator sections, the device also includes SYNCH/ASYNCH converters, scrambler/descrambler, call progress tone detect, DTMF tone generator capabilities and handshake pattern detectors. V.22bis, V.22, V.21 and Bell 212A/103 modes are supported (synchronous and asynchronous) and test modes are provided for diagnostics. Most functions are selectable as options and logical defaults are provided.

OPERATION

QAM MODULATOR/DEMODULATOR

The SSI 73K224L encodes incoming data into quadbits represented by 16 possible signal points with specific phase and amplitude levels. The baseband signal is then filtered to reduce intersymbol interference on the bandlimited telephone network. The modulator transmits this encoded data using either a 1200 Hz (originate mode) or 2400 Hz (answer mode) carrier. The demodulator, although more complex, essentially reverses this procedure while also recovering the data clock from the incoming signal. Adaptive equalization corrects for varying line conditions by automatically changing filter parameters to compensate for line characteristics.

DPSK MODULATOR/DEMODULATOR

The SSI 73K224L modulates a serial bit stream into di-bit pairs that are represented by four possible phase shifts as prescribed by the Bell 212A/V.22 standards. The base-band signal is then filtered to reduce intersymbol interference on the bandlimited 2-wire PSTN line. Transmission occurs on either a 1200 Hz (originate mode) or 2400 Hz carrier (answer mode). Demodulation is the reverse of the modulation process, with the incoming analog signal eventually decoded into di-bits and converted back to a serial bit stream. The demodulator also recovers the clock which was encoded into the analog signal during modulation.Demodulation occurs using either a 1200 Hz carrier (answer mode or ALB originate mode) or a 2400 Hz carrier (originate mode or ALB answer mode). Adaptive equalization is also used in DPSK modes for optimum operation with varying line conditions.

FSK MODULATOR/DEMODULATOR

The FSK modulator produces a frequency modulated analog output signal using two discrete frequencies to represent the binary data. The Bell 103 standard frequencies of 1270 and 1070 Hz (originate mark and space) and 2225 and 2025 Hz (answer mark and space) are used when this mode is selected. V.21 mode uses 980 and 1180 Hz (originate, mark and space) or 1650 and 1850 Hz (answer, mark and space). Demodulation involves detecting the received frequencies and decoding them into the appropriate binary value. The rate converter and scrambler/descrambler are automatically bypassed in the FSK modes.

PASSBAND FILTERS AND EQUALIZERS

High and low band filters are included to shape the amplitude and phase response of the transmit and receive signals and provide compromise delay equalization and rejection of out-of-band signals. Amplitude and phase equalization are necessary to compensate for distortion of the transmission line and to reduce intersymbol interference in the bandlimited receive signal. The transmit signal filtering corresponds to a 75% square root of raised Cosine frequency response characteristic.

ASYNCHRONOUS MODE

The asynchronous mode is used for communication with asynchronous terminals which may communicate at 600,1200, or 2400 bit/s +1%, -2.5% even though the modem's output is limited to the nominal bit rate ±.01% in DPSK and QAM modes. When transmitting in this mode the serial data on the TXD input is passed through a rate converter which inserts or deletes stop bits in the serial bit stream in order to output a signal that is the nominal bit rate ±.01%. This signal is then routed to a data scrambler and into the analog modulator where quad-bit/di-bit encoding results in the out-

put signal. Both the rate converter and scrambler can be bypassed for handshaking, and synchronous operation as selected. Received data is processed in a similar fashion except that the rate converter now acts to reinsert any deleted stop bits and output data to the terminal at no greater than the bit rate plus 1%. An incoming break signal (low through two characters) will be passed through without incorrectly inserting a stop bit.

The SYNC/ASYNC converter also has an extended overspeed mode which allows selection of an output overspeed range of either +1% or +2.3%. In the extended overspeed mode, stop bits are output at 7/8 the normal width.

Both the SYNC/ASYNC rate converter and the data descrambler are automatically bypassed in the FSK modes.

SYNCHRONOUS MODE

Synchronous operation is possible only in the QAM or DPSK modes. Operation is similar to that of the asynchronous mode except that data must be synchronized to a provided clock and no variation in data transfer rate is allowable. Serial input data appearing at TXD must be valid on the rising edge of TXCLK.

TXCLK is an internally derived 1200 or 2400 Hz signal in internal mode and is connected internally to the RXCLK pin in slave mode. Receive data at the RXD pin is clocked out on the falling edge of RXCLK. The asynch/synch converter is bypassed when synchronous mode is selected and data is transmitted at the same rate as it is input.

PARALLEL BUS INTERFACE

Eight 8-bit registers are provided for control, option select, and status monitoring. These registers are addressed with the AD0, AD1, and AD2 multiplexed address lines (latched by ALE) and appear to a control microprocessor as seven consecutive memory locations. Six control registers are read/write memory. The detect and ID registers are read only and cannot be modified except by modem response to monitored parameters.

SERIAL CONTROL INTERFACE

The serial command mode allows access to the SSI 73K324 control and status registers via a serial control port. In this mode the A0, A1, and A2 lines provide register addresses for data passed through the DATA pin under control of the $\overline{RD}$ and $\overline{WR}$ lines. A read operation is initiated when the $\overline{RD}$ line is taken low. The next eight cycles of EXCLK will then transfer out eight bits of the selected addresss location LSB first. A write takes place by shifting in eight bits of data LSB first for eight consectuive cycles of EXCLK. $\overline{WR}$ is then pulsed low and data transfer into the selected register occurs on the rising edge of $\overline{WR}$.

DTMF GENERATOR

The DTMF generator controls the sending of the sixteen standard DTMF tone pairs. The tone pair sent is determined by selecting TRANSMIT DTMF (bit D4) and the 4 DTMF bits (D0-D3) of the TONE register. Transmission of DTMF tones from TXA is gated by the TRANSMIT ENABLE bit of CR0 (bit D1) as with all other analog signals.

PIN DESCRIPTION

POWER

NAME	TYPE	DESCRIPTION
GND	I	System Ground.
VDD	I	Power supply input, 5V -5% +10%. Bypass with .22 µF and 22 µF capacitors to GND.
VREF	O	An internally generated reference voltage. Bypass with .22 µF capacitor to GND.
ISET	I	Chip current reference. Sets bias current for op-amps. The chip current is set by connecting this pin to VDD through a 2 MΩ resistor. Iset should be bypassed to GND with a .22 µF capacitor.

PARALLEL MICROPROCESSOR INTERFACE

ALE	I	Address latch enable. The falling edge of ALE latches the address on AD0-AD2 and the chip select on $\overline{CS}$.
AD0-AD7	I/O / Tristate	Address/data bus.These bidirectional tri-state multi-plexed lines carry information to and from the internal registers.
$\overline{CS}$	I	Chip select. A low on this pin allows a read cycle or a write cycle to occur. AD0-AD7 will not be driven and no registers will be written if $\overline{CS}$ (latched) is not active. $\overline{CS}$ is latched on the falling edge of ALE.
CLK	O	Output clock. This pin is selectable under processor control to be either the crystal frequency (for use as a processor clock) or 16 x the data rate for use as a baud rate clock in QAM/DPSK modes only. The pin defaults to the crystal frequency on reset.
$\overline{INT}$	O	Interrupt. This open drain weak pullup, output signal is used to inform the processor that a detect flag has occurred. The processor must then read the detect register to determine which detect triggered the interrupt. $\overline{INT}$ will stay active until the processor reads the detect register or does a full reset.
$\overline{RD}$	I	Read. A low requests a read of the SSI 73K224L internal registers. Data cannot be output unless both $\overline{RD}$ and the latched $\overline{CS}$ are active or low.
RESET	I	Reset. An active high signal on this pin will put the chip into an inactive state. All control register bits (CR0, CR1, CR2, CR3, Tone) will be reset. The output of the CLK pin will be set to the crystal frequency. An internal pull down resistor permits power on reset using a capacitor to VDD.
$\overline{WR}$	I	Write. A low on this informs the SSI 73K224L that data is available on AD0-AD7 for writing into an internal register. Data is latched on the rising edge of $\overline{WR}$. No data is written unless both $\overline{WR}$ and the latched $\overline{CS}$ are active (low).

Note: The serial control mode is provided in the parallel versions by tying ALE high and $\overline{CS}$ low. In this configuration AD7 becomes DATA and AD0, AD1 and AD2 become A0, A1 and A2, respectively.

DTE USER INTERFACE

NAME	TYPE	DESCRIPTION
EXCLK	I	External Clock. This signal is used in synchronous transmission when the external timing option has been selected. In the external timing mode the rising edge of EXCLK is used to strobe synchronous transmit data available on the TXD pin. Also used for serial control interface.
RXCLK	O/Tristate	Receive Clock. Tri-stateable. The falling edge of this clock output is coincident with the transitions in the serial received data output. The rising edge of RXCLK can be used to latch QAM or DPSK valid output data. RXCLK will be active as long as a carrier is present.
RXD	O	Received Digital Data Output. Serial receive data is available on this pin. The data is always valid on the rising edge of RXCLK when in synchronous mode. RXD will output constant marks if no carrier is detected.
TXCLK	O/Tristate	Transmit Clock. Tri-stateable. This signal is used in synchronous transmission to latch serial input data on the TXD pin. Data must be provided so that valid data is available on the rising edge of the TXCLK. The transmit clock is derived from different sources depending upon the synchronization mode selection. In Internal Mode the clock is generated internally. In External Mode TXCLK is phase locked to the EXCLK pin. In Slave Mode TXCLK is phase locked to the RXCLK pin. TXCLK is always active.
TXD	I	Transmit Digital Data Input. Serial data for transmission is input on this pin. In synchronous modes, the data must be valid on the rising edge of the TXCLK clock. In asynchronous modes (2400/1200/600 bit/s or 300 baud) no clocking is necessary. DPSK data must be +1%, -2.5% or +2.3%, -2.5 % in extended overspeed mode.

ANALOG INTERFACE AND OSCILLATOR

RXA	I	Received modulated analog signal input from the phone line.
TXA	O	Transmit analog output to the phone line.
XTL1	I	These pins are for the internal crystal oscillator requiring a 11.0592 MHz parallel mode crystal. Two capacitors from these pins to ground are also required for proper crystal operation. Consult crystal manufacturer for proper values. XTL2 can also be driven from an external clock.
XTL2	I/O	

PIN DESCRIPTION (continued)

SERIAL MICROPROCESSOR INTERFACE

NAME	TYPE	DESCRIPTION
A0-A2	I	Register Address Selection. These lines carry register addresses and should be valid during any read or write operation.
DATA	I/O	Serial Control Data. Data for a read/write operation is clocked in or out on the falling edge of the EXCLK pin. The direction of data flow is controlled by the $\overline{RD}$ pin. $\overline{RD}$ low outputs data. $\overline{RD}$ high inputs data.
$\overline{RD}$	I	Read. A low on this input informs the SSI 73K322L that data or status information is being read by the processor. The falling edge of the $\overline{RD}$ signal will initiate a read from the addresses register. The $\overline{RD}$ signal must continue for eight falling edges of EXCLK in order to read all eight bits of the referenced register. Read data is provided LSB first. Data will not be output unless the $\overline{RD}$ signal is active.
$\overline{WR}$	I	Write. A low on this input informs the SSI 73K322L that data or status information has been shifted in through the DATA pin and is available for writing to an internal register. The normal procedure for a write is to shift in data LSB first on the DATA pin for eight consecutive falling edges of EXCLK and then to pulse $\overline{WR}$ low. Data is written on the rising edge of $\overline{WR}$.

Note: In the serial, 22-pin version, the pins AD0-AD7, ALE and $\overline{CS}$ are removed and replaced with the pins; A0, A1, A2, DATA, and an unconnected pin. Also, the $\overline{RD}$ and $\overline{WR}$ controls are used differently.

REGISTER DESCRIPTIONS

Eight 8-bit internal registers are accessible for control and status monitoring. The registers are accessed in read or write operations by addressing the A0, A1 and A2 address lines in serial mode, or the AD0, AD1 and AD2 lines in parallel mode. The address lines are latched by ALE. Register CR0 controls the method by which data is transferred over the phone line. CR1 controls the interface between the microprocessor and the SSI 73K224L internal state. DR is a detect register which provides an indication of monitored modem status conditions. TR, the tone control register, controls the DTMF generator, answer and guard tones and RXD output gate used in the modem initial connect sequence. CR2 is the primary DSP control interface and CR3 controls transmit attenuation and receive gain adjustments. All registers are read/write except for DR and ID which are read only. Register control and status bits are identified below:

REGISTER BIT SUMMARY

	ADDRESS	DATA BIT NUMBER							
REGISTER	AD - A0	D7	D6	D5	D4	D3	D2	D1	D0
CONTROL REGISTER 0 CR0	000	MODULATION OPTION	MODULATION TYPE 1	MODULATION TYPE 0	TRANSMIT MODE 2	TRANSMIT MODE 1	TRANSMIT MODE 0	TRANSMIT ENABLE	ANSWER/ ORIGINATE
CONTROL REGISTER 1 CR1	001	TRANSMIT PATTERN 1	TRANSMIT PATTERN 0	ENABLE DETECT INTERRUPT	BYPASS SCRAMBLER	CLK CONTROL	RESET	TEST MODE 1	TEST MODE 0
DETECT REGISTER DR	010	RECEIVE LEVEL	PATTERN S1 DET	RECEIVE DATA	UNSCR. MARK DETECT	CARRIER DETECT	SPECIAL TONE DETECT	CALL PROGRESS DETECT	SIGNAL QUALITY
TONE CONTROL REGISTER TR	011	RXD OUTPUT CONTROL	TRANSMIT GUARD TONE	TRANSMIT ANSWER TONE	TRANSMIT DTMF	DTMF3	DTMF2	DTMF1/ EXTENDED OVERSPEED	DTMF0/GUARD/ ANSWER
CONTROL REGISTER 2 CR2	100		SPECIAL REGISTER ACCESS	CALL INITIALIZE	TRANSMIT S1	16 WAY	RESET DSP	TRAIN INHIBIT	EQUALIZER ENABLE
CONTROL REGISTER 3 CR3	101	TXDALT	TRISTATE TX/RXCLK		RECEIVE GAIN BOOST	TRANSMIT ATTEN. 3	TRANSMIT ATTEN. 2	TRANSMIT ATTEN. 1	TRANSMIT ATTEN. 0
SPECIAL REGISTER SR	101		TX BAUD CLOCK	RX UNSCR. DATA		TXD SOURCE	SQ SELECT 1	SQ SELECT 0	
ID REGISTER ID	110	ID	ID	ID	ID	USER DEFINABLE PERSONALITY			

NOTE: When a register containing reserved control bits is written into, the reserved bits must be programmed as 0's.

REGISTER ADDRESS TABLE

REGISTER	ADDRESS AD2 - AD0	D7	D6	D5	D4	D3	D2	D1	D0
CONTROL REGISTER 0 CR0	000	MODULATION OPTION	MODULATION TYPE 1	MODULATION TYPE 0	TRANSMIT MODE 2	TRANSMIT MODE 1	TRANSMIT MODE 0	TRANSMIT ENABLE	ANSWER/ ORIGINATE
		QAM: 0=2400 BIT/S DPSK: 0=1200 BIT/S 1=600 BIT/S FSK: 0=103 MODE 1=V.21	10=QAM 00=DPSK 01=FSK	0000=PWR DOWN 0001=INT SYNCH 0010=EXT SYNCH 0011=SLAVE SYNCH 0100=ASYCH 8 BITS/CHAR 0101=ASYCH 9 BITS/CHAR 0110=ASYCH 10 BITS/CHAR 0111=ASYCH 11 BITS/CHAR 1X00=FSK				0=DISABLE TXA OUTPUT 1=ENABLE TXA OUTPUT	0=ANSWER 1=ORIGINATE
CONTROL REGISTER 1 CR1	001	TRANSMIT PATTERN 1	TRANSMIT PATTERN 0	ENABLE DETECT INTERRUPT	BYPASS SCRAMBLER	CLK CONTROL	RESET	TEST MODE 1	TEST MODE 0
		00=TX DATA 01=TX ALTERNATE 10=TX MARK 11=TX SPACE		0=DISABLE 1=ENABLE	0=NORMAL 1=BYPASS SCRAMBLER	0=XTAL 1=16 X DATA RATE OUTPUT AT CLK PIN IN QAM/DPSK MODE ONLY	0=NORMAL 1=RESET	00=NORMAL 01=ANALOG LOOPBACK 10=REMOTE DIGITAL LOOPBACK 11=LOCAL DIGITAL LOOPBACK	
DETECT REGISTER DR	010	RECEIVE LEVEL INDICATOR	S1 PATTERN DETECT	RECEIVE DATA	UNSCR. MARKS DETECT	CARRIER DETECT	ANSWER TONE DETECT	CP TONE DETECT	SIGNAL QUALITY INDICATOR
		0=SIGNAL BELOW THRESHOLD 1=ABOVE THRESHOLD	0=NOT PRESENT 1=PATTERN FOUND	OUTPUTS RECEIVED DATA STREAM		0=CONDITION NOT DETECTED 1=CONDITION DETECTED			0=GOOD 1=BAD
TONE CONTROL REGISTER TR	011	RXD OUTPUT CONTROL	TRANSMIT GUARD/ CALLING TONE	TRANSMIT ANSWER TONE	TRANSMIT DTMF	DTMF3	DTMF2	DTMF1/ EXTENDED OVERSPEED	DTMF0/ GUARD/ ANSWER
		RXD PIN 0=NORMAL 1=OPEN	0=OFF 1=ON	0=OFF 1=ON	0=DATA 1=TX DTMF	4 BIT CODE FOR 1 OF 16 DUAL TONE COMBINATIONS			0=1800 Hz G.T. □□□□□□2225 Hz ANS TON □□□□□ GENERATED. 1=550 Hz G.T. □□□□□□2100 Hz ANS TON □□□□□ GENERATED & □□□□□ DETECTED (V.21,
CONTROL REGISTER 2 CR2	100	0	SPECIAL REGISTER ACCESS	CALL INITIALIZE	TRANSMIT S1	16 WAY	$\overline{\text{RESET}}$ DSP	TRAIN INHIBIT	EQUALIZER ENABLE
			0=ACCESS CR3 1=ACCESS □□□□SPECIAL □□□□REGISTER	0=DSP IN DEMOD MODE 1=DSP IN CALL PROGRESS MODE	0=NORMAL DOTTING 1=S1	0=RX=TX 1=RX=16 WAY	0=DSP INACTIVE 1=DSP ACTIVE	0=ADAPT EQ ACTIVE 1=ADAPT EQ FROZEN	0=ADAPT EQ IN INIT 1=ADAPT EQ OK TO ADAPT
CONTROL REGISTER 3 CR3	101	TXDALT	TRISTATE TX/RXCLK	0	RECEIVE GAIN BOOST	TRANSMIT ATTEN. 3	TRANSMIT ATTEN. 2	TRANSMIT ATTEN. 1	TRANSMIT ATTEN. 0
		ALTERNATE TRANSMIT DATA SOURCE	0=NORMAL 1=TRISTATE		0=NO BOOST 1=18 dB BOOST	0000-1111, SETS TRANSMIT ATTENUATOR 16 dB RANGE DEFAULT=0100 = -10 dBm0			
SPECIAL REGISTER SR	101		TX BAUD CLOCK	RX UNSCR. DATA		TXD SOURCE	SQ SELECT1	SQ SELECT0	
			OUTPUTS TXBAUD CLOCK	OUTPUTS UNSCR. DATA		0=TXD PIN 1=TXALT BIT	00=10^{-5} BER 01=10^{-6} BER 10=10^{-4} BER 11=10^{-3} BER		
ID REGISTER 10	110	ID	ID	ID	ID				

00XX=73K212, 322, 321
01XX=73K221, 302
10XX=73K222
1100=73K224
1110=73K324
1101=73K312

CONTROL REGISTER 0

	D7	D6	D5	D4	D3	D2	D1	D0
CR0 000	MODUL. OPTION	MODUL. TYPE 1	MODUL. TYPE 0	TRANSMIT MODE 2	TRANSMIT MODE 1	TRANSMIT MODE 0	TRANSMIT ENABLE	ANSWER/ ORIGINATE

BIT NO.	NAME	CONDITION	DESCRIPTION
D0	Answer/ Originate	0	Selects answer mode (transmit in high band, receive in low band).
		1	Selects originate mode (transmit in low band,receive in high band).
D1	Transmit Enable	0	Disables transmit output at TXA.
		1	Enables transmit output at TXA.
			Note: Transmit Enable must be set to 1 to allow activation of Answer Tone or DTMF.
D5, D4, D3, D2	Transmit Mode	D5 D4 D3 D2	
		0 0 0 0	Selects power down mode. All functions disabled except digital interface.
		0 0 0 1	Internal synchronous mode. In this mode TXCLK is an internally derived 600,1200 or 2400 Hz signal. Serial input data appearing at TXD must be valid on the rising edge of TXCLK. Receive data is clocked out of RXD on the falling edge of RXCLK.
		0 0 1 0	External synchronous mode. Operation is identical to internal synchronous, but TXCLK is connected internally to EXCLK pin, and a 600, 1200 or 2400 Hz clock must be supplied externally.
		0 0 1 1	Slave synchronous mode. Same operation as other synchronous modes. TXCLK is connected internally to the RXCLK pin in this mode.
		0 1 0 0	Selects asynchronous mode - 8 bits/character (1 start bit, 6 data bits, 1 stop bit).
		0 1 0 1	Selects asynchronous mode - 9 bits/character (1 start bit, 7 data bits, 1 stop bit).
		0 1 1 0	Selects asynchronous mode - 10 bits/character (1 start bit, 8 data bits, 1 stop bit).
		0 1 1 1	Selects asynchronous mode - 11 bits/character (1 start bit, 8 data bits, Parity and/or 1 or 2 stop bits).
		1 X 0 0	Selects FSK operation.
D6,D5	Modulation Type	D6 D5	
		1 0	QAM
		0 0	DPSK
		0 1	FSK

CONTROL REGISTER 0 (Continued)

	D7	D6	D5	D4	D3	D2	D1	D0
CR0 000	MODUL. OPTION	MODUL. TYPE 1	MODUL. TYPE 0	TRANSMIT MODE 2	TRANSMIT MODE 1	TRANSMIT MODE 0	TRANSMIT ENABLE	ANSWER/ ORIGINATE

BIT NO.	NAME	CONDITION	DESCRIPTION
D7	Modulation Option	0	QAM selects 2400 bit/s. DPSK selects 1200 bit/s. FSK selects 103 mode.
		1	DPSK selects 600 bit/s. FSK selects V.21 mode.

CONTROL REGISTER 1

	D7	D6	D5	D4	D3	D2	D1	D0
CR1 001	TRANSMIT PATTERN 1	TRANSMIT PATTERN 0	ENABLE DETECT INT.	BYPASS SCRAMB	CLK CONTROL	RESET	TEST MODE 1	TEST MODE 0

BIT NO.	NAME	CONDITION	DESCRIPTION
D1, D0	Test Mode	D1 D0	
		0 0	Selects normal operating mode.
		0 1	Analog loopback mode. Loops the transmitted analog signal back to the receiver, and causes the receiver to use the same carrier frequency as the transmitter. To squelch the TXA pin, TRANSMIT ENABLE bit as well as Tone Reg bit D2 must be low.
		1 0	Selects remote digital loopback. Received data is looped back to transmit data internally, and RXD is forced to a mark. Data on TXD is ignored.
		1 1	Selects local digital loopback. Internally loops TXD back to RXD and continues to transmit data carrrier at TXA pin.
D2	Reset	0	Selects normal operation.
		1	Resets modem to power down state. All control register bits (CR0, CR1, CR2, CR3 and Tone) are reset to zero except CR3 bit D2. The output of the clock pin will be set to the crystal frequency.
D3	Clock Control	0	Selects 11.0592 MHz crystal echo output at CLK pin.
		1	Selects 16 X the data rate, output at CLK pin in DPSK/ QAM modes only.

CONTROL REGISTER 1 (Continued)

	D7	D6	D5	D4	D3	D2	D1	D0
CR1 001	TRANSMIT PATTERN 1	TRANSMIT PATTERN 0	ENABLE DETECT INT.	BYPASS SCRAMB	CLK CONTROL	RESET	TEST MODE 1	TEST MODE 0

BIT NO.	NAME	CONDITION	DESCRIPTION
D4	Bypass Scrambler	0	Selects normal operation. DPSK and QAM data is passed through scrambler.
		1	Selects Scrambler Bypass. Bypass DPSK and QAM data is routed around scrambler in the transmit path.
D5	Enable Detect Interrupt	0	Disables interrupt at $\overline{INT}$ pin. All interrupts are normally disabled in power down mode.
		1	Enables $\overline{INT}$ output. An interrupt will be generated with a change in status of DR bits D1-D4 and D6. The answer tone and call progress detect interrupts are masked when the TX enable bit is set. Carrier detect is masked when TX DTMF is activated. All interrupts will be disabled if the device is in power down mode.
D7, D6	Transmit Pattern	D7 D6	
		0 0	Selects normal data transmission as controlled by the state of the TXD pin.
		0 1	Selects an alternating mark/space transmit pattern for modem testing and handshaking. Also used for S1 pattern generation. See CR2 bit D4.
		1 0	Selects a constant mark transmit pattern.
		1 1	Selects a constant space transmit pattern.

DETECT REGISTER

	D7	D6	D5	D4	D3	D2	D1	D0
DR 010	RECEIVE LEVEL INDICATOR	S1 PATTERN DETECT	RECEIVE DATA	UNSCR. MARK DETECT	CARR. DETECT	ANSWER TONE DETECT	CALL PROG. DETECT	SIGNAL QUALITY INDICATOR

BIT NO.	NAME	CONDITION	DESCRIPTION
D0	Signal Quality Indicator	0	Indicates normal received signal.
		1	Indicates low received signal quality (above average error rate). Interacts with special register bits D2, D1.
D1	Call Progress Detect	0	No call progress tone detected.
		1	Indicates presence of call progress tones. The call progress detection circuitry is activated by energy in the normal 350 to 620 Hz call progress bandwidth.

DETECT REGISTER (Continued)

	D7	D6	D5	D4	D3	D2	D1	D0
DR 010	RECEIVE LEVEL INDICATOR	S1 PATTERN DETECT	RECEIVE DATA	UNSCR. MARK DETECT	CARR. DETECT	ANSWER TONE DETECT	CALL PROG.	SIGNAL QUALITY INDICATOR

BIT NO.	NAME	CONDITION	DESCRIPTION
D2	Answer Tone Received	0	No answer tone detected.
		1	In Call Init mode, indicates detection of 2225 Hz answer tone in Bell mode (TR bit D0=0) or 2100 Hz if in CCITT mode (TR bit D0=1). The device must be in originate mode for detection of answer tone. Both answer tones are detected in demod mode.
D3	Carrier Detect	0	No carrier detected in the receive channel.
		1	Indicated carrier has been detected in the received channel.
D4	Unscrambled Mark Detect	0	No unscrambled mark.
		1	Indicates detection of unscrambled marks in the received data. Should be time qualified by software.
D5	Receive Data		Continuously outputs the received data stream. This data is the same as that output on the RXD pin, but it is not disabled when RXD is tri-stated.
D6	S1 Pattern Detect	0	No S1 pattern being received.
		1	S1 pattern detected. Should be time qualified by software. S1 pattern is defined as a double di-bit (001100..) unscrambled 1200 bit/s DPSK signal. Pattern must be aligned with baud clock to be detected.
D7	Receive Level Indicator	0	Received signal level below threshold, (typical ≈ -25 dBm0); can use receive gain boost (+18 dB).
		1	Received signal above threshold.

TONE REGISTER

	D7	D6	D5	D4	D3	D2	D1	D0
TR 011	RXD OUTPUT CONTR.	TRANSMIT GUARD TONE	TRANSMIT ANSWER TONE	TRANSMIT DTMF	DTMF 3	DTMF 2	DTMF 1/ EXTENDED OVER-SPEED	DTMF 0/ ANSWER/ GUARD

BIT NO.	NAME	CONDITION	DESCRIPTION
D0	DTMF 0/ Answer/ Guard Tone	D6 D5 D4 D0	D0 interacts with bits D6, D5, and D4 as shown.
		X X 1 X	Transmit DTMF tones.
		X 1 0 0	Select Bell mode answer tone. Interacts with DR bit D2 and TR bit D5.
(Continued)		X 1 0 1	Select CCITT mode answer tone. Interacts with DR bit D2 and TR bit D5.

TONE REGISTER (Continued)

	D7	D6	D5	D4	D3	D2	D1	D0
TR 011	RXD OUTPUT CONTR.	TRANSMIT GUARD TONE	TRANSMIT ANSWER TONE	TRANSMIT DTMF	DTMF 3	DTMF 2/ 4 WIRE FDX	DTMF 1/ EXTENDED OVER-SPEED	DTMF 0/ ANSWER/ GUARD

BIT NO.	NAME	CONDITION	DESCRIPTION
D0	DTMF 0/ Answer/ Guard Tone	D6 D5 D4 D0	D0 interacts with bits D6, D5, and D4 as shown.
		1 0 0 0	Select 1800 Hz guard tone.
		1 0 0 1	Select 550 Hz guard tone.
D1	DTMF 1/ Extended Overspeed	D4 D1	D1 interacts with D4 as shown.
		0 0	Asynchronous QAM or DPSK +1.0% -2.5%. (normal)
		0 1	Asynchronous QAM or DPSK +2.3% -2.5%. (extended overspeed)
D2	DTMF 2/ 4 WIRE FDX	D4 D2	
		0 0	Selects 2 wire duplex or half duplex
		0 1	D2 selects 4 wire full duplex in the modulation mode selected. The receive path corresponds to the ANS/ ORIG bit CR0 D0 in terms of high or low band selection. The transmitter is in the same band as the receiver, but does not have magnitude filtering or equalization on its signal as in the receive path.

TONE REGISTER (Continued)

	D7	D6	D5	D4	D3	D2	D1	D0
TR 011	RXD OUTPUT CONTR.	TRANSMIT GUARD TONE	TRANSMIT ANSWER TONE	TRANSMIT DTMF	DTMF 3	DTMF 2/ 4 WIRE FDX	DTMF 1/ EXTENDED OVER-SPEED	DTMF 0/ ANSWER/ GUARD

BIT NO.	NAME	CONDITION	DESCRIPTION
D3, D2, D1, D0	DTMF 3, 2, 1, 0	D3 D2 D1 D0 0 0 0 0 - 1 1 1 1	Programs 1 of 16 DTMF tone pairs that will be transmitted when TX DTMF and TX enable bit (CR0, bit D1) is set. Tone encoding is shown below:
D4	TX DTMF (Transmit DTMF)	0	Disable DTMF.
		1	Activate DTMF. The selected DTMF tones are transmitted continuously when this bit is high. TX DTMF overrides all other transmit functions.

KEYBOARD EQUIVALENT	DTMF CODE D3 D2 D1 D0	TONES LOW HIGH
1	0 0 0 1	697 1209
2	0 0 1 0	697 1336
3	0 0 1 1	697 1477
4	0 1 0 0	770 1209
5	0 1 0 1	770 1336
6	0 1 1 0	770 1477
7	0 1 1 1	852 1209
8	1 0 0 0	852 1336
9	1 0 0 1	852 1477
0	1 0 1 0	941 1336
*	1 0 1 1	941 1209
#	1 1 0 0	941 1477
A	1 1 0 1	697 1633
B	1 1 1 0	770 1633
C	1 1 1 1	852 1633
D	0 0 0 0	941 1633

Note: DTMF0 - DTMF2 should be set to an appropriate state after DTMF dialing to avoid unintended operation.

TONE REGISTER (Continued)

D7	D6	D5	D4	D3	D2	D1	D0	
TR 011	RXD OUTPUT CONTR.	TRANSMIT GUARD TONE	TRANSMIT ANSWER TONE	TRANSMIT DTMF	DTMF 3	DTMF 2/ 4 WIRE FDX	DTMF 1/ EXTENDED OVER-SPEED	DTMF 0/ ANSWER/ GUARD

BIT NO.	NAME	CONDITION	DESCRIPTION
D5	Transmit Answer Tone	D5 D4 D0	D5 interacts with bits D4 and D0 as shown. Also interacts with DR bit D2 in originate mode. See Detect Register description.
		0 0 X	Disables answer tone generator.
		1 0 0	In answer mode, a Bell 2225 Hz tone is transmitted continuously when the Transmit Enable bit is set.
		1 0 1	Likewise, a CCITT 2100 Hz answer tone is transmitted.
D6	Transmit Guard Tone	0	Disables guard tone generator.
		1	Enables guard tone generator. (See D0 for selection of guard tones.) Bit D4 must be zero.
D7	RXD Output Control	0	Enables RXD pin. Receive data will be output on RXD.
		1	Disables RXD pin. The RXD pin reverts to a high impedance with internal weak pull-up resistor.

CONTROL REGISTER 2

	D7	D6	D5	D4	D3	D2	D1	D0
CR2 100	0	SPEC REG ACCESS	CALL INIT	TRANSMIT S1	16 WAY	$\overline{\text{RESET}}$ DSP	TRAIN INHIBIT	EQUALIZER ENABLE

BIT NO.	NAME	CONDITION	DESCRIPTION
D0	Equalizer Enable	0	The adaptive equalizer is in its initialized state.
		1	The adaptive equalizer is enabled. This bit is used in handshakes to control when the equalizer should calculate its coefficients.
D1	Train Inhibit	0	The adaptive equalizer is active.
		1	The adaptive equalizer coefficients are frozen.
D2	$\overline{\text{RESET DSP}}$	0	The DSP is inactive and all variables are initialized.
		1	The DSP is running based on the mode set by other control bits
D3	16 Way	0	The receiver and transmitter are using the same decision plane (based on the Modulator Control Mode).
		1	The receiver, independent of the transmitter, is forced into a 16 point decision plane. Used for QAM handshaking.

CONTROL REGISTER 2 (Continued)

	D7	D6	D5	D4	D3	D2	D1	D0
CR2 100	0	SPEC REG ACCESS	CALL INIT	TRANSMIT S1	16WAY	$\overline{\text{RESET}}$ DSP	TRAIN INHIBIT	EQUALIZER ENABLE

BIT NO.	NAME	CONDITION	DESCRIPTION
D4	Transmit S1	0	The transmitter when placed in alternating mark/space mode transmits 0101..... scrambled or not dependent on the bypass scrambler bit.
		1	When this bit is 1 and only when the transmitter is placed in alternating mark/space mode by CR1 bits D7, D6, and in DPSK or QAM, an unscrambled repetitive double dibit pattern of 00 and 11 at 1200 bit/s (S1) is sent.
D5	Call Init	0	The DSP is setup to do demodulation and pattern detection based on the various mode bits. Both answer tones are detected in demod mode concurrently; TR-D0 is ignored.
		1	The DSP decodes unscrambled mark, answer tone and call progress tones.
D6	Special Register Access	0	Normal CR3 access.
		1	Setting this bit and addressing CR3 allows access to the SPECIAL REGISTER. See the SPECIAL REGISTER for details.
D7	Not used at this time	0	Only write zero to this bit.

CONTROL REGISTER 3

	D7	D6	D5	D4	D3	D2	D1	D0
CR3 101	TXDALT	TRISTATE TX/RXCLK		RECEIVE BOOST ENABLE	TRANSMIT ATTEN. 3	TRANSMIT ATTEN. 2	TRANSMIT ATTEN. 1	TRANSMIT ATTEN. 0

BIT NO.	NAME	CONDITION	DESCRIPTION
D3, D2, D1,D0	Transmit Attenuator	D3 D2 D1 D0 0 0 0 0 - 1 1 1 1	Sets the attenuation level of the transmitted signal in 1dB steps. The default (D3-D0=0100) is for a transmit level of -10 dBm0 on the line with the recommended hybrid transmit gain. The total range is 16 dB.
D4	Receive Gain Boost	0	18 dB receive front end boost is not used.
		1	Boost is in the path. This boost does not change reference levels. It is used to extend dynamic range by compensating for internally generated noise when receiving weak signals. The receive level detect signal and knowledge of the hybrid and transmit attenuator setting will determine when boost should be enabled.
D5	Not used at this time	0	Only write zero to this bit.
D6	TRISTATE TXCLK/RXCLK	0	TXCLK and RXCLK are driven.
		1	TXCLK and RXCLK are tristated.
D7	TXDALT	Spec. Reg. Bit D3=1	Alternate TX data source. See Special Register.

SPECIAL REGISTER

	D7	D6	D5	D4	D3	D2	D1	D0
SR 101		TXBAUD CLOCK	RXUN-DSCR DATA		TXD SOURCE	SIGNAL QUALITY LEVEL SELECT1	SIGNAL QUALITY LEVEL SELECT0	

BIT NO.	NAME	DESCRIPTION
D7, D4, D0		NOT USED AT THIS TIME. Only write ZEROs to these bits.
D6	TXBAUD CLK	TXBAUD clock is the transmit baud-synchronous clock that can be used to synchronize the input of arbitrary quad/di-bit patterns. The rising edge of TXBAUD signals the latching of a baud-worth of data internally. Synchronous data to be entered via the TXDALT bit, CR3 bit D7, should have data transitions that start 1/2 bit period delayed from the TXBAUD clock edges.
D5	RXUNDSCR DATA	This bit outputs the data received before going to the descrambler. This is useful for sending special unscrambled patterns that can be used for signaling.
D3	TXD SOURCE	This bit selects the transmit data source; either the TXD pin if ZERO or the TXDALT if this bit is a ONE. The TRANSMIT PATTERN bits D7 and D6 in CR1 override either of these sources.
D2, D1	SIGNAL QUALITY LEVEL SELECT	The signal quality indicator is a logical ZERO when the signal received is acceptable for low error rate reception. It is determined by the value of the Mean Squared Error (MSE) calculated in the decisioning process when compared to a given threshold. This threshold can be set to four levels of error rate. The SQI bit will be low for good or average connections. As the error rate crosses the threshold setting, the SQI bit will toggle at a 1.66 ms rate. Toggling will continue until the error rate indicates that the data pump has lost convergence and a retrain is required. At that point the SQI bit will be a ONE constantly. The SQI bit and threshold selection are valid for QAM and DPSK only and indicates typical error rate.

D2	D1	THRESHOLD VALUE	UNITS
0	0	10^{-5}	BER (default)
0	1	10^{-6}	BER
1	0	10^{-4}	BER
1	1	10^{-3}	BER

NOTE: This register is "mapped" and is accessed by setting CR2 bit D6 to a ONE and addressing CR3. This register provides functions to the 73K224L user that are not necessary in normal communications. Bits D7-D4 are read only, while D3-D0 are read/write. To return to normal CR3 access, CR2 bit D6 must be returned to a ZERO.

ID REGISTER

	D7	D6	D5	D4	D3	D2	D1	D0
ID 110	ID 3	ID 2	ID 1	ID 0	USER DEFINABLE PERSONALITY			

BIT NO.	NAME	CONDITION	DESCRIPTION
D7, D6, D5, D4	Device Identification Signature	D7 D6 D5 D4	Indicates Device:
		0 0 X X	SSI 73K212(L), 73K321L or 73K322L
		0 1 X X	SSI 73K221(L) or 73K302L
		1 0 X X	SSI 73K222(L)
		1 1 0 1	SSI 73K312L
		1 1 0 0	SSI 73K224L
		1 1 1 0	SSI 73K324L

ELECTRICAL SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING
VDD Supply Voltage	7V
Storage Temperature	-65 to 150°C
Soldering Temperature (10 sec.)	260°C
Applied Voltage	-0.3 to VDD+0.3V
Note: All inputs and outputs are protected from static charge using built-in, industry standard protection devices and all outputs are short-circuit protected.	

RECOMMENDED OPERATING CONDITIONS

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNITS
VDD Supply voltage		4.5	5	5.5	V
External Components (Refer to Application section for placement.)					
VREF Bypass capacitor	(VREF to GND)	0.22			µF
Bias setting resistor	(Placed between VDD and ISET pins)	1.8	2	2.2	MΩ
ISET Bypass capacitor	(ISET pin to GND)	0.22			µF
VDD Bypass capacitor 1	(VDD to GND)	0.22			µF
VDD Bypass capacitor 2	(VDD to GND)	22			µF
XTL1 Load Capacitance	Depends on crystal requirements		18	39	pF
XTL2 Load Capacitance	Depends on crystal requirements		18	27	pF
Clock Variation	(11.0592 MHz) Crystal or external clock	-0.01		+0.01	%
TA, Operating Free-Air Temperature		-40		85	°C

DC ELECTRICAL CHARACTERISTICS
(TA = -40°C to 85°C, VDD = recommended range unless otherwise noted.)

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNITS
IDD, Supply Current	CLK = 11.0592 MHz				
	ISET Resistor = 2 MΩ				
IDD1, Active	Operating with crystal oscillator,		18	25	mA
IDD2, Idle	< 5 pF capacitive load on CLK pin		3	5	mA
Digital Inputs					
VIL, Input Low Voltage				0.8	V
VIH, Input High Voltage					
All Inputs except Reset XTL1, XTL2		2.0		VDD	V
Reset, XTL1, XTL2		3.0		VDD	V
IIH, Input High Current	VI = VDD			100	µA
IIL, Input Low Current	VI = 0V	-200			µA
Reset Pull-down Current	Reset = VDD	2		50	µA
Digital Outputs					
VOH, Output High Voltage	IO = IOH Min IOUT = -0.4 mA	2.4		VDD	V
VOL, Output Low Voltage	IO = IOUT = 1.6 mA			0.4	V
RXD Tri-State Pull-up Curr.	RXD = GND	-2		-50	µA
Capacitance					
Maximum Capacitive Load					
CLK	Maximum permitted load			25	pF
Input Capacitance	All Digital Inputs			10	pF

DYNAMIC CHARACTERISTICS AND TIMING

(TA = -40°C to +85°C, VDD = recommended range unless otherwise noted.)

PARAMETERS	CONDITIONS	MIN	NOM	MAX	UNITS
QAM/DPSK Modulator					
Carrier Suppression	Measured at TXA	35			dB
Output Amplitude	TX scrambled marks ATT=0100 (default)	-11.5	-10.0	-9	dBm0
FSK Modulator/Demodulator					
Output Freq. Error	CLK = 11.0592 MHz	-.31		+.20	%
Transmit Level	ATT = 0100 (Default) Transmit Dotting Pattern	-11.5	-10.0	-9	dBm0
TXA Output Distortion	All products through BPF			-45	dB
Output Bias Distortion at RXD	Dotting Pattern measured at RXD Receive Level -20 dBm, SNR 20 dB	-10		+10	%
Output Jitter at RXD	Integrated for 5 seconds	-15		+15	%
Sum of Bias Distortion and Output Jitter	Integrated for 5 seconds	-17		+17	%
Answer Tone Generator (2100 or 2225 Hz)					
Output Amplitude	ATT = 0100 (Default Level) Not in V.21	-11.5	-10	-9	dBm0
Output Distortion	Distortion products in receive band			-40	dB
DTMF Generator	Not in V.21				
Freq. Accuracy		-0.03		+0.25	%
Output Amplitude	Low Band, ATT = 0100, DPSK Mode	-10		-8	dBm0
Output Amplitude	High Band, ATT = 0100, DPSK Mode	-8		-6	dBm0
Twist	High-Band to Low-Band, DPSK Mode	1.0	2.0	3.0	dB
Receiver Dynamic Range	Refer to Performance Curves	-43		-3.0	dBm0
Call Progress Detector	In Call Init mode				
Detect Level	460 Hz test signal	-34		0	dBm0
Reject Level				-40	dBm0
Delay Time	-70 dBm0 to -30 dBm0 STEP			25	ms
Hold Time	-30 dBm0 to -70 dBm0 STEP			25	ms

NOTE: Parameters expressed in dBm0 refer to the following definition:

0 dB loss in the Transmit path to the line.

2 dB gain in the Receive path from the line.

Refer to the Basic Box Modem diagram in the Applications section for the DAA design.

DYNAMIC CHARACTERISTICS AND TIMING (Continued)

PARAMETERS		CONDITIONS	MIN	NOM	MAX	UNITS
Carrier Detect		**Receive Gain = On for lower input level measurements**				
Threshold		All Modes	-48		-43	dBm0
Hysteresis		All Modes	2			
Delay Time	FSK	70 dBm0 to -6 dBm0	25		37	ms
		70 dBm0 to -40 dBm0	25		37	ms
	DPSK	-70 dBm0 to -6 dBm0	7		17	ms
		-70 dBm0 to -40 dBm0	7		17	ms
	QAM	-70 dBm0 to -6 dBm0	25		37	ms
		-70 dBm0 to -40 dBm0	25		37	ms
Hold Time	FSK	-6 dBm0 to -70 dBm0	25		37	ms
		-40 dBm0 to -70 dBm0	15		30	ms
	DPSK	-6 dBm0 to -70 dBm0	20		29	ms
		-40 dBm0 to -70 dBm0	14		21	ms
	QAM	-6 dBm0 to -70 dBm0	25		32	ms
		-40 dBm0 to -70 dBm0	18		28	ms
Answer Tone Detectors		**DPSK Mode**				
Detect Level			-48		-43	dBm0
Detect Time		Call Init Mode, 2100 or 2225 Hz	6		50	ms
Hold Time			6		50	ms
Pattern Detectors		**DPSK Mode**				
S1 Pattern						
Delay Time		For signals from -6 to -40 dBm0,	10		55	ms
Hold Time		-6 to -40 dBm0, Demod Mode	10		45	ms
Unscrambled Mark						
Delay Time		For signals from -6 to -40	10		45	ms
Hold Time		call Init Mode	10		45	ms
Receive Level Indicator						
Detect On			-22		-28	dBm0
Valid after Carrier Detect		DPSK Mode	1	4	7	ms
Output Smoothing Filter						
Output Impedance		TXA pin		200	300	Ω
Output load		TXA pin; FSK Single	10			KΩ
		Tone out for THD = -50 dB in .3 to 3.4 kHz range			50	pF
Maximum Transmitted Energy		4 kHz, Guard Tones off			-35	dBm0
		10 kHz, Guard Tones off			-55	dBm0
		12 kHz, Guard Tones off			-65	dBm0

DYNAMIC CHARACTERISTICS AND TIMING (Continued)

PARAMETERS	CONDITIONS	MIN	NOM	MAX	UNITS
Anti Alias Low Pass Filter					
Out of Band Signal Energy (Defines Hybrid Trans-Hybrid loss requirements)	Level at RXA pin with receive Boost Enabled				
	Scrambled data at 2400 bit/s in opposite band		-14		dBm
	Sinusoids out of band		-9		dBm
Transmit Attenuator					
Range of Transmit Level	Default ATT=0100 (-10 dBm0) 1111-000	-21		-6	dBm0
Step Accuracy		-0.15		+0.15	dB
Output Impedance			200	300	Ω
Clock Noise					
	TXA pin; 153.6 kHz			1.5	mVrms
Carrier Offset					
Capture Range	Originate or Answer		±5	±7	Hz
Recovered Clock					
Capture Range	% of frequency (originate or answer)	-0.02		+0.02	%
Guard Tone Generator					
Tone Accuracy	550 Hz		+1.2		%
	1800 Hz		-0.8		
Tone Level	550 Hz	-4.5	-3.0	-1.5	dB
(Below QAM/DPSK Output)	1800 Hz	-7.5	-6.1	-4.5	dB
Harmonic Distortion	550 Hz			-50	dB
(700 to 2900 Hz)	1800 Hz			-50	dB
Timing (Refer to Timing Diagrams)					
Parallel Mode					
TAL	$\overline{CS}$/Addr. setup before ALE Low	30			ns
TLA	$\overline{CS}$/Addr. hold after ALE Low	10			ns
TLC	ALE Low to $\overline{RD}$/$\overline{WR}$ Low	40			ns
TCL	$\overline{RD}$/$\overline{WR}$ Control to ALE High	10			ns
TRD	Data out from $\overline{RD}$ Low			90	ns
TLL	ALE width	25			ns
TRDF	Data float after $\overline{RD}$ High			40	ns
TRW	$\overline{RD}$ width	70			ns

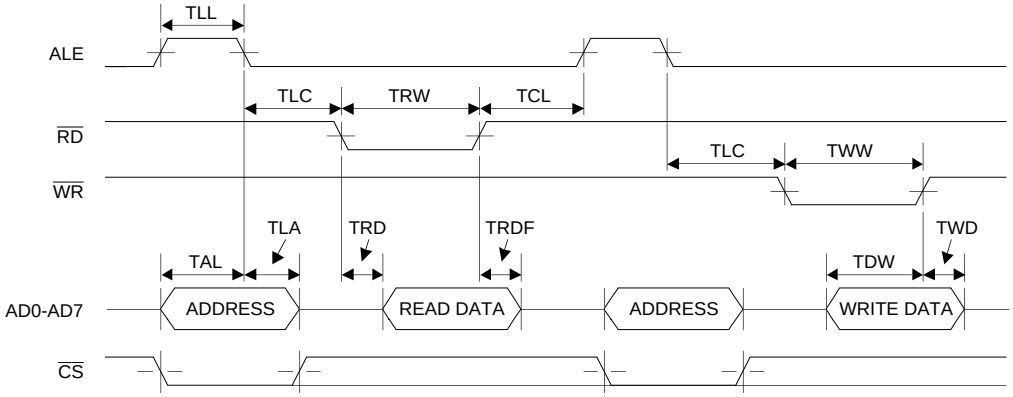
DYNAMIC CHARACTERISTICS AND TIMING (Continued)

PARAMETERS	CONDITIONS	MIN	NOM	MAX	UNITS
Parallel Mode (Continued)					
TWW	$\overline{WR}$ width	70			ns
TDW	Data setup before $\overline{WR}$ High	70			ns
TWD	Data hold after $\overline{WR}$ High	20			ns
Serial Mode					
TRCK	Clock High after $\overline{RD}$ Low	250		T1	ns
TAR	Address setup before $\overline{RD}$ Low	0			ns
TRA	Address hold after $\overline{RD}$ Low	350			ns
TRD	$\overline{RD}$ to Data valid			300	ns
TRDF	Data float after $\overline{RD}$ High			40	ns
TCKDR	Read Data out after Falling Edge of EXCLK			300	ns
TWW	$\overline{WR}$ width	350			ns
TAW	Address setup before $\overline{WR}$ Low	50			ns
TWA	Address hold after Rising Edge of $\overline{WR}$	50			ns
TCKDW	Write Data hold after Falling Edge of EXCLK	200			ns
TCKW	$\overline{WR}$ High after Falling Edge of EXCLK	330		T1 + T2	ns
TDCK	Data setup before Falling Edge of EXCLK	50			ns
T1, T2	Minimum Period	500			ns

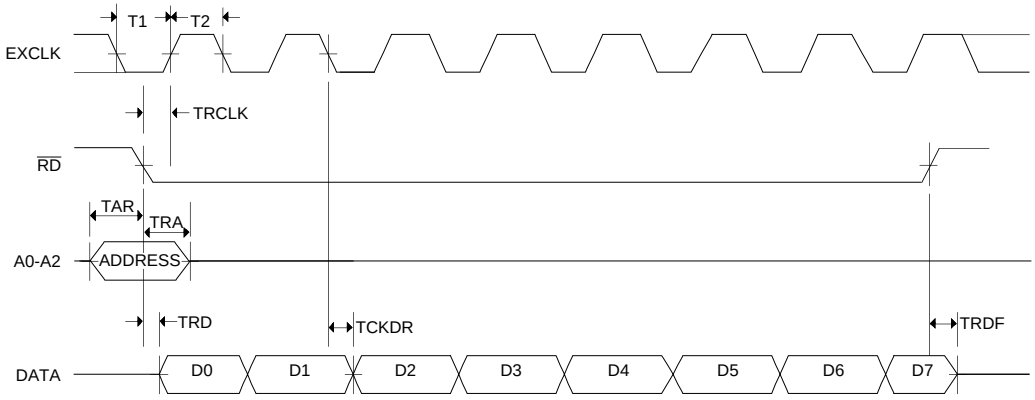
NOTE: T1 and T2 are the low/high periods, respectively, of EXCLK in serial mode.

TIMING DIAGRAMS

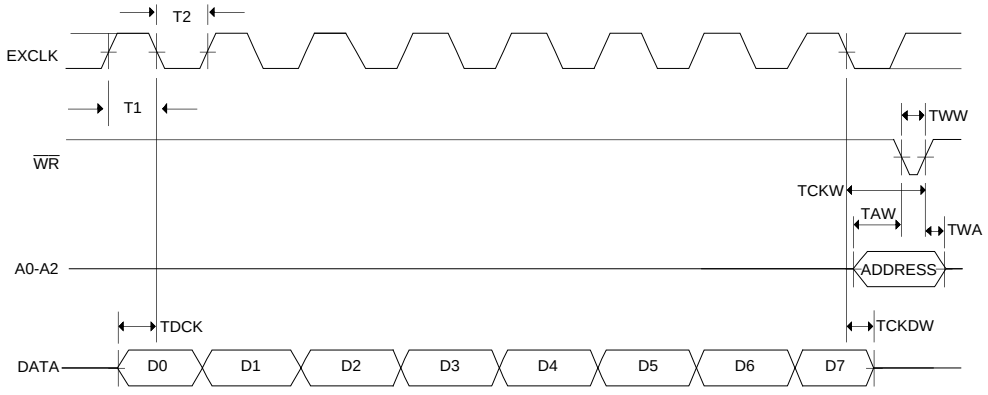
BUS TIMING DIAGRAM (PARALLEL VERSION)



READ TIMING DIAGRAM (SERIAL VERSION)



WRITE TIMING DIAGRAM (SERIAL VERSION)



APPLICATIONS INFORMATION

GENERAL CONSIDERATIONS

Figures 1 and 2 show basic circuit diagrams for K-Series modem integrated circuits. K-Series products are designed to be used in conjunction with a control processor, a UART or RS-232 serial data interface, and a DAA phone line interface to function as a typical intelligent modem. The K-Series ICs interface directly with Intel 8048 and 80C51 microprocessors for control and status monitoring purposes. Two typical DAA arrangements are shown: one for a split ±5 or ±12 V design and one for a single 5 V design. These diagrams are for reference only and do not represent production-ready modem designs.

K-Series devices are available with two control interface versions: one for a parallel multiplexed address/data interface, and one for a serial interface. The parallel version is intended for use with 8039/48 or 8031/51 microcontrollers from Intel or many other manufacturers. The serial interface 22-pin version can be used with other microcontrollers or in applications where only a limited number of port lines are available or the application does not lend itself to a multiplexed address/data interface. The parallel versions may also be used in the serial mode, as explained in the data sheet pin description.

In most applications the controller will monitor the serial data for commands from the DTE and the received data for break signals from the far end modem. In this way, commands to the modem are sent over the same line as the transmitted data. In other applications the RS-232 interface handshake lines are used for modem control.

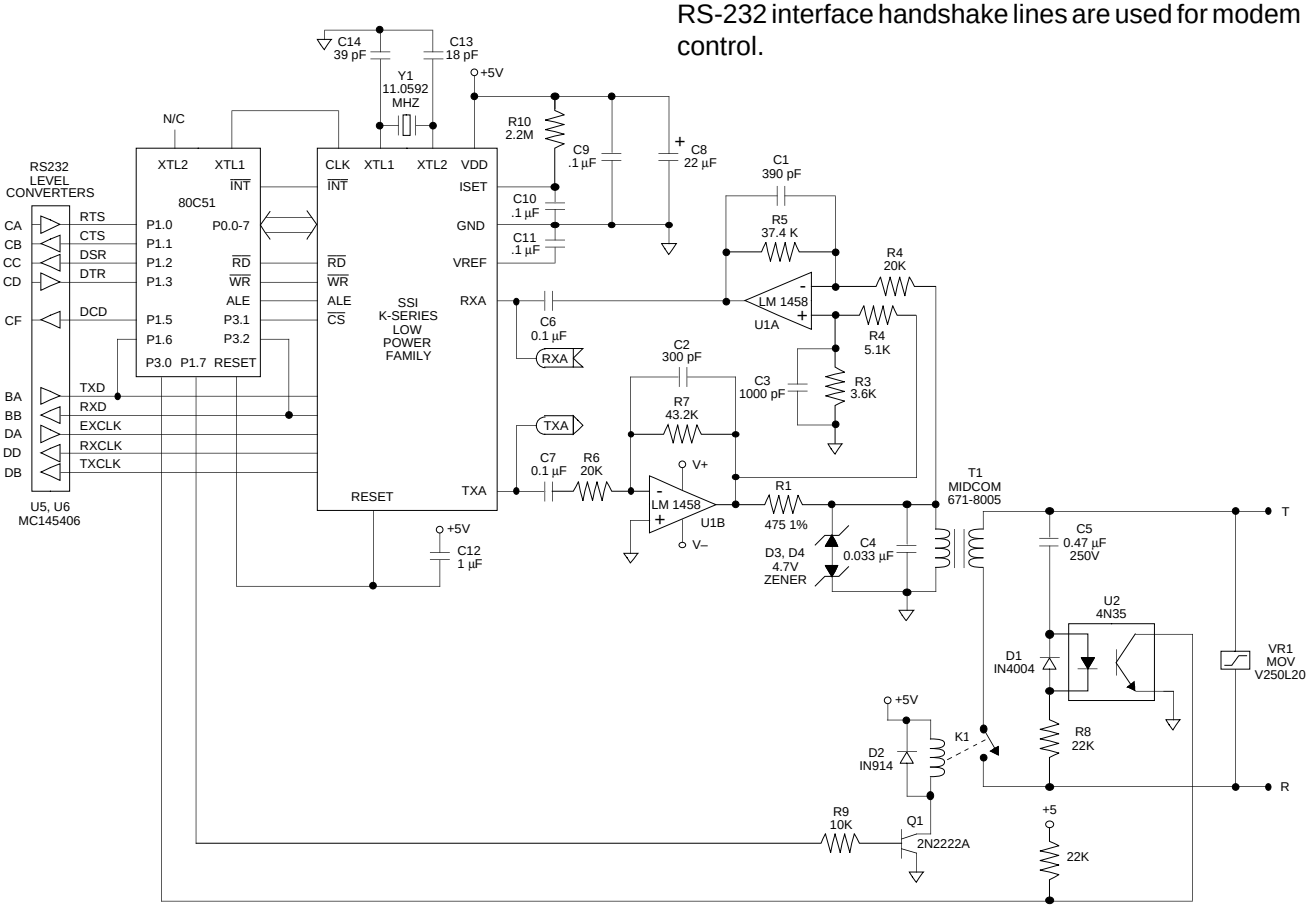


FIGURE 1: Basic Box Modem with Dual-Supply Hybrid

DIRECT ACCESS ARRANGEMENT (DAA)

The telephone line interfaces show two examples of how the "hybrid" may be implemented. The split supply design (Figure 1) is a typical two op-amp hybrid. The receive op-amp serves two purposes. It supplies gain to amplify the receive signal to the proper level for the modem's detectors and demodulator, and it removes the transmitted signal from the receive signal present at the transformer. This is done by supplying a portion of the transmitted signal to the non-inverting input of the receive op-amp at the same amplitude as the signal appearing at the transformer, making the transmit signal common mode.

The single-supply hybrid is more complex than the dual-supply version described above, but its use eliminates the need for a second power supply. This circuit (Figure 2) uses a bridged drive to allow undistorted signals to be sent with a single 5 volt supply. Because DTMF tones utilize a higher amplitude than data, these signals will clip if a single-ended drive approach is used. The bridged driver uses an extra op-amp (U1A) to invert the signal coming from the gain setting op-amp (U1B) before sending it to the other leg of the transformer. Each op-amp then supplies half the drive signal to the transformer. The receive amplifier (U1C) picks off its signal at the junction of the impedance matching resistor and the transformer. Because the bottom leg of the transformer is being driven in one direction by U1A and the resistor is driven in the opposite direction at the same time by U1B, the junction of the transformer and resistor remains relatively constant and the receive signal is unaffected.

DESIGN CONSIDERATIONS

Silicon Systems' 1-chip modem products include all basic modem functions. This makes these devices adaptable for use in a variety of applications, and as easy to control as conventional digital bus peripherals.

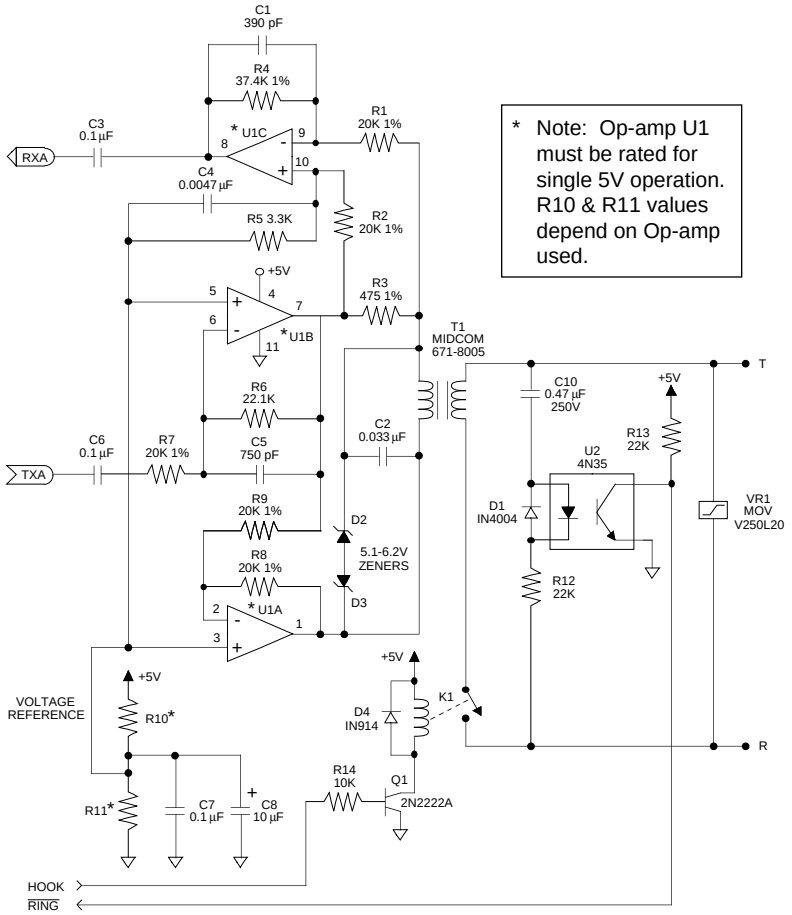


FIGURE 2: Single 5V Hybrid Version

Unlike digital logic circuitry, modem designs must properly contend with precise frequency tolerances and very low level analog signals, to ensure acceptable performance. Using good analog circuit design practices will generally result in a sound design. Following are additional recommendations which should be taken into consideration when starting new designs.

CRYSTAL OSCILLATOR

The K-Series crystal oscillator requires a parallel mode (antiresonant) crystal which operates at 11.0592 MHz. It is important that this frequency be maintained to within ±0.01% accuracy.

In order for a parallel mode crystal to operate correctly and to specification, it must have a load capacitor connected to the junction of each of the crystal and internal inverter connections, terminated to ground. The values of these capacitors depend primarily on the crystal's characteristics, and to a lesser degree on the internal inverter circuit. The values used affect the accuracy and start up characteristics of the oscillator.

LAYOUT CONSIDERATIONS

Good analog/digital design rules must be used to control system noise in order to obtain highest performance in modem designs. The more digital circuitry present on the PC board, the more this attention to noise control is needed. The modem should be treated as a high impedance analog device. A 22 µF electrolytic capacitor in parallel with a 0.22 µF ceramic capacitor between VDD and GND is recommended. Liberal use of ground planes and larger traces on power and ground are also highly favored. The ISET resistor and capacitor should be mounted near the ISET pin, away from digital signals. High speed digital circuits tend to generate a significant amount of EMI (Electro-Magnetic Interference) which must be minimized in order to meet regulatory agency limitations. To accomplish this, high speed digital devices should be locally bypassed, and the telephone line interface and K-Series device should be located close to each other near the area of the board where the phone line connection is accessed. To avoid problems, power supply and ground traces should be routed separately to the analog and digital functions on the board, and digital signals should not be routed near low level or high impedance analog traces. The analog and digital grounds should only connect at one point near the K-Series device ground pin to avoid ground loops. The K–Series modem IC's should have both high frequency and low frequency bypassing as close to the package as possible.

MODEM PERFORMANCE CHARACTERISTICS

The curves presented here define modem IC performance under a variety of line conditions while inducing disturbances that are typical of those encountered during data transmission on public service telephone lines. Test data was taken using an AEA Electronics' "Autotest I" modem test set and line simulator, operating under computer control. All tests were run full-duplex, using a Hayes SmartModem™ 2400 as the reference modem. A 511 pseudo-random-bit pattern was used for each data point. Noise was C-message weighted and all signal-to-noise (S/N) ratios reflect total power measurements similar to the CCITT V.56 measurement specification. The individual tests are defined as follows.

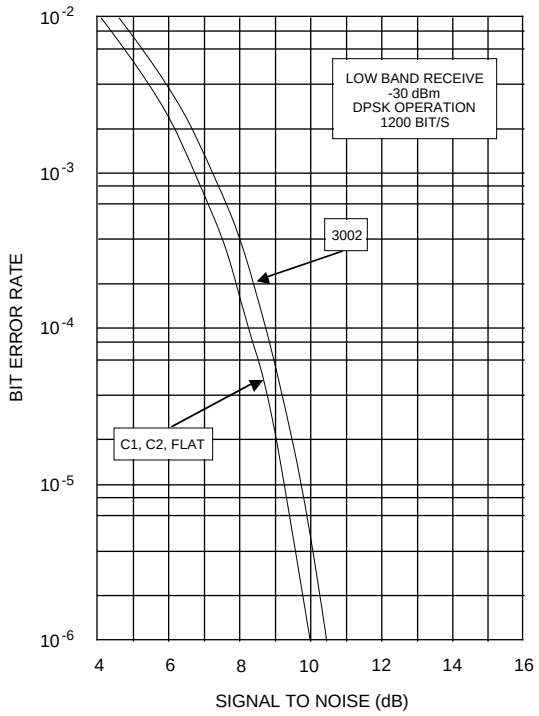
BER vs. S/N

This test measures the ability of the modem to operate over noisy lines with a minimum of data-transfer errors. Since some noise is generated in the best of dial-up lines, the modem must operate with the lowest S/N ratio possible. Better modem performance is indicated by test curves that are closest to the BER axis. A narrow spread between curves representing the four line parameters indicates minimal variation in performance while operating over a range of aberrant operating conditions. Typically, a modem will exhibit better BER-performance test curves receiving in the low band than in the high band.

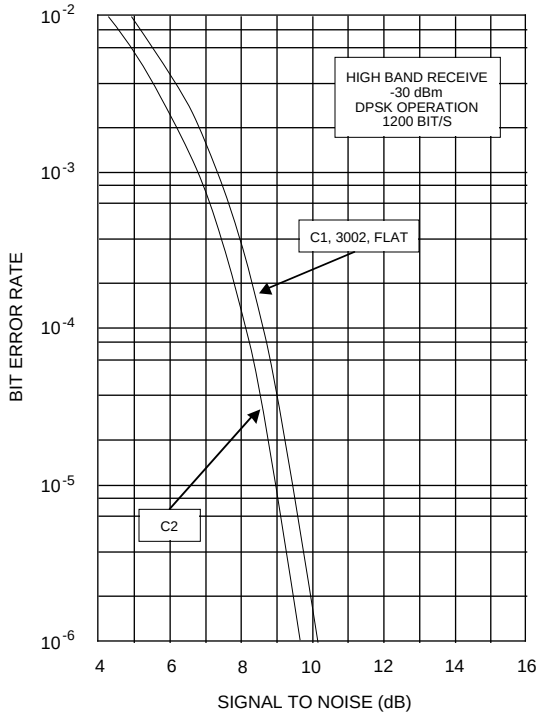
BER vs. Receive Level

This test measures the dynamic range of the modem. Because signal levels vary widely over dial-up lines, the widest possible dynamic range is desirable. The minimum Bell specification calls for 36 dB of dynamic range. S/N ratios are held constant at the indicated values while the receive level is lowered from a very high to very low signal levels. The width of the "bowl" of these curves, taken at the BER point, is the measure of dynamic range.

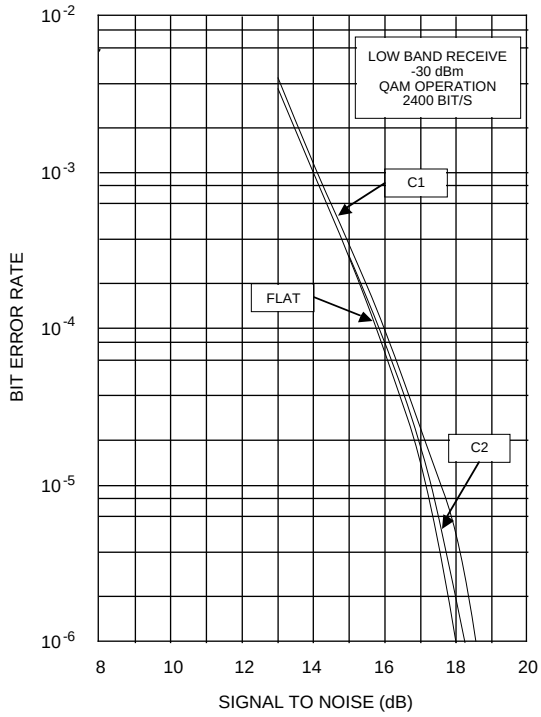
SSI 73K224L BER vs S/N-DPSK LOW BAND



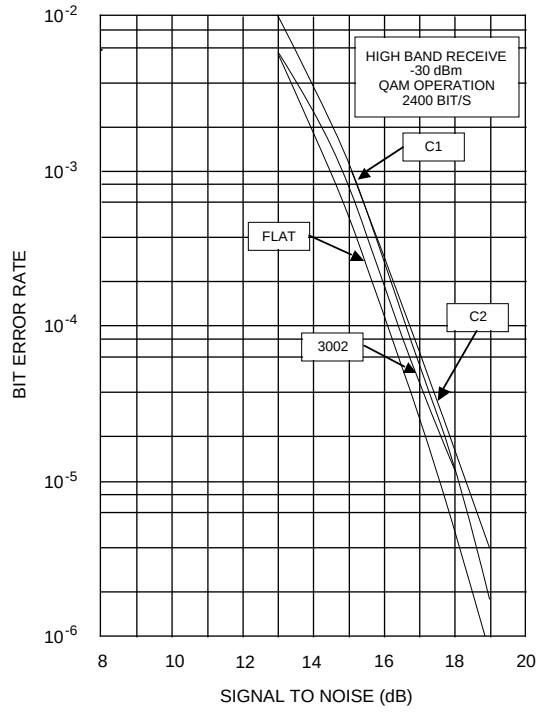
SSI 73K224L BER vs S/N-DPSK HIGH BAND

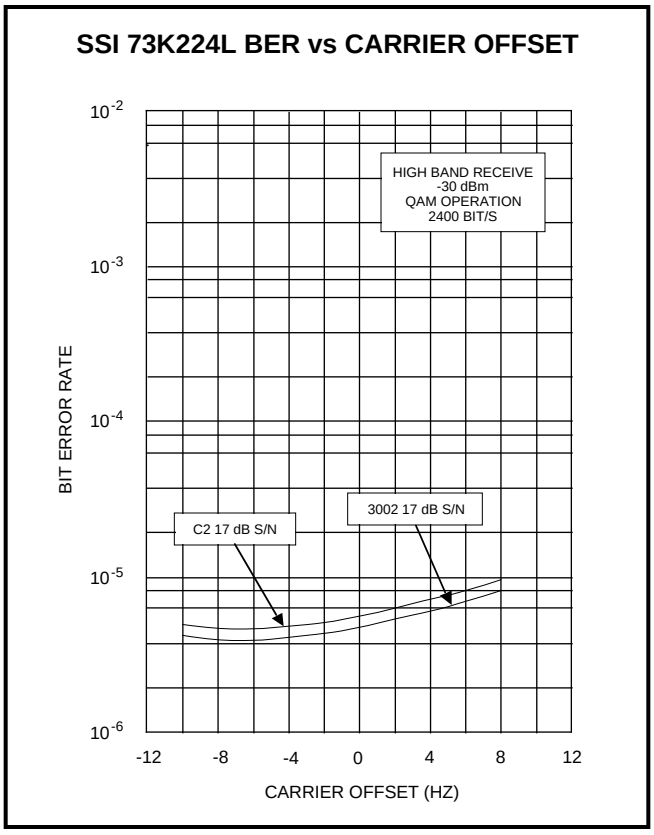


SSI 73K224L
BER vs S/N-QAM-LOW BAND



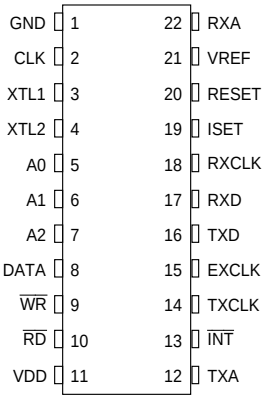
SSI 73K224L
BER vs S/N-QAM-HIGH BAND



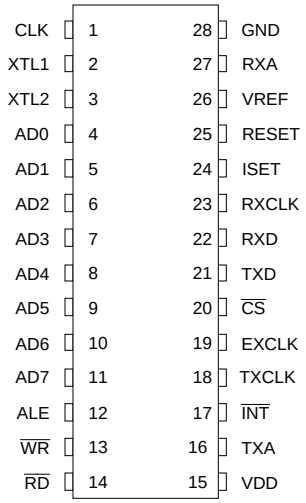

SSI 73K224L BER vs CARRIER OFFSET
HIGH BAND RECEIVE
-30 dBm
QAM OPERATION
2400 BIT/S
C2 17 dB S/N
3002 17 dB S/N
BIT ERROR RATE
10-2
10-3
10-4
10-5
10-6
-12
-8
-4
0
4
8
12
CARRIER OFFSET (HZ)

PACKAGE PIN DESIGNATIONS

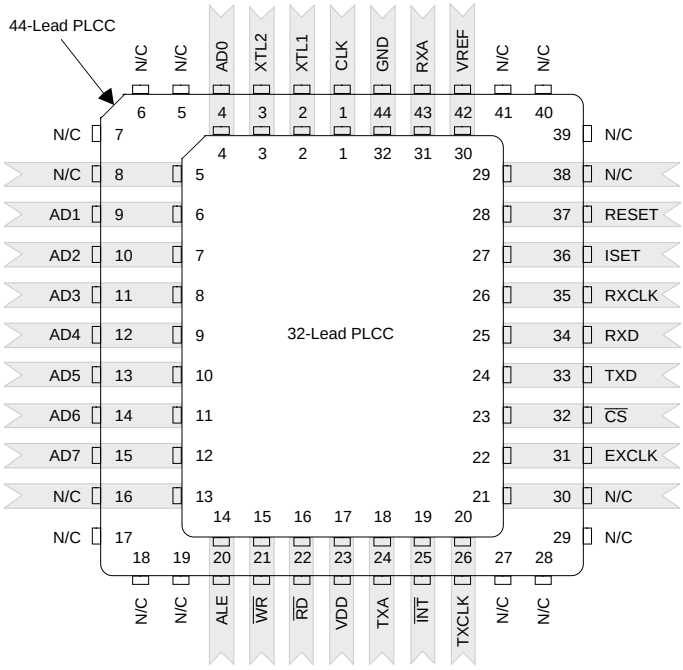
(Top View)



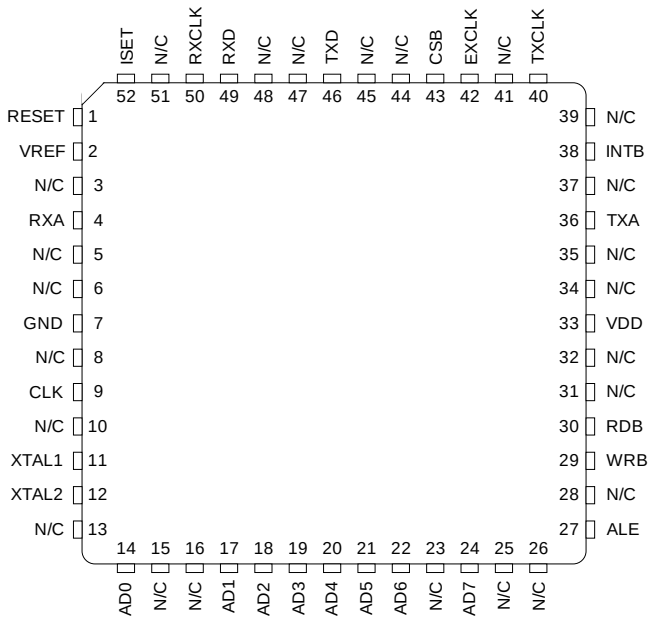
400-Mil
22-Pin DIP



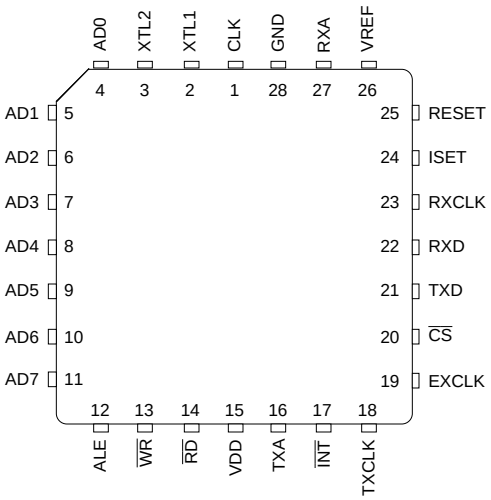
600-Mil
28-Pin DIP



32, 44-Pin PLCC

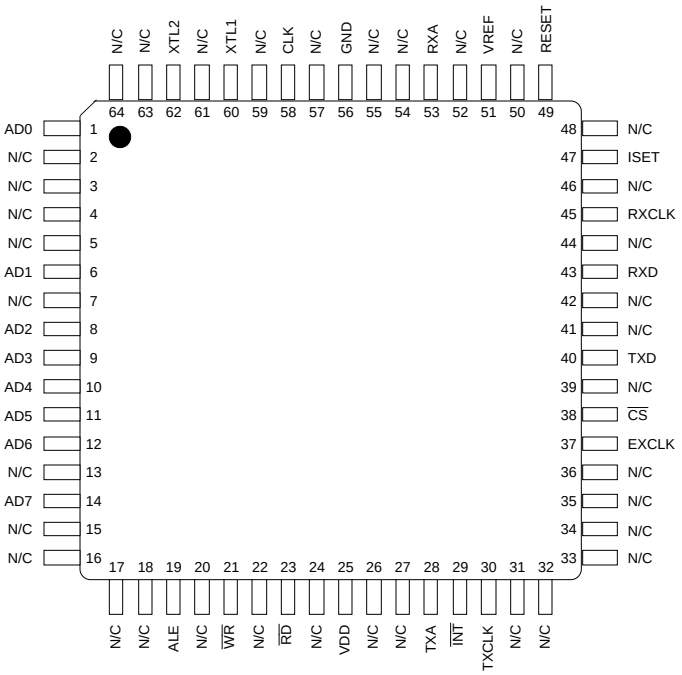


52-Lead QFP



28-Pin PLCC

CAUTION: Use handling procedures necessary for a static sensitive component.



64-Lead TQFP

ORDERING INFORMATION

PART DESCRIPTION	ORDER NO.	PKG. MARK
SSI 73K224L with Serial Bus Interface		
22-Pin Plastic Dual-In-Line	73K224LS-IP	73K224LS-IP
SSI 73K224L with Parallel Bus Interface		
28-Pin Plastic Dual-In-Line	73K224L-IP	73K224L-IP
28-Pin Plastic Leaded Chip Carrier	73K224L-28IH	73K224L-28IH
32-Pin Plastic Leaded Chip Carrier	73K224L-32IH	73K224L-32IH
44-Pin Plastic Leaded Chip Carrier	73K224L-IH	73K224L-IH
52-Lead Quad Flat Pack Package	73K224L-IG	73K224L-IG
64-Lead Thin Quad Flat Pack Package	73K224L-IGT	73K224L-IGT

Silicon Systems, Inc. 14351 Myford Road, Tustin, CA 92680, (714) 573-6000, FAX (714) 573-6914

SSI 73K324L

CCITT V.22bis, V.22, V.21, V.23, Bell 212A Single-Chip Modem

Preliminary Data

December 1992

DESCRIPTION

The SSI 73K324L is a highly integrated single-chip modem IC which provides the functions needed to design a quad-mode CCITT and Bell 212A compatible modem capable of operation over dial-up lines. The SSI 73K324L adds V.23 capability to the CCITT modes of Silicon Systems' 73K224 one-chip modem, allowing a one-chip implementation in designs intended for European markets which require this added modulation mode. The SSI 73K324L offers excellent performance and a high level of functional integration in a single IC. The device supports V.22bis, V.22, Bell 212A, V.21, and V.23 operating modes, allowing both synchronous and asynchronous operation as defined by the appropriate standard.

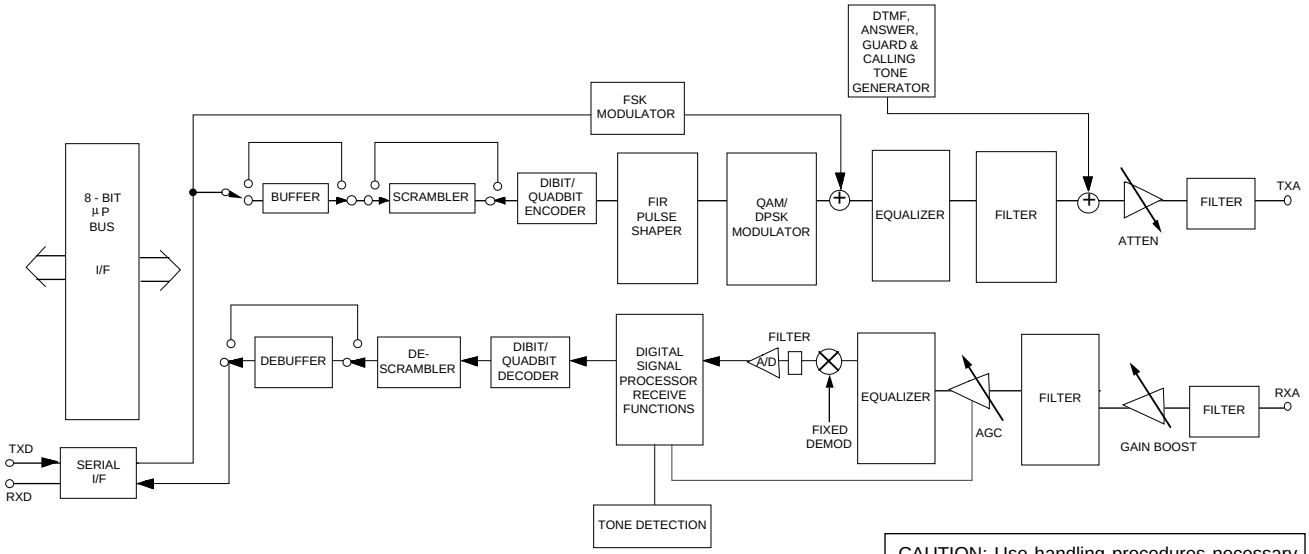
The SSI 73K324L is designed to appear to the Systems Engineer as a microprocessor peripheral, and will easily interface with popular one-chip microcontrollers (80C51 typical) for control of modem functions through its 8-bit multiplexed address/data bus. A serial control bus is available for applications not requiring a parallel interface. An optional package with only the serial control bus is also available. Data communications occurs through a separate serial port.

(Continued)

FEATURES

- **One chip multi-mode CCITT V.22bis, V.22, V.21, V.23 and Bell 212A compatible modem data pump**
- **FSK (75, 300, 1200 bit/s), DPSK (600, 1200 bit/s), or QAM (2400 bit/s) encoding**
- **Pin and software compatible with other SSI K-Series family one-chip modems**
- **Interfaces directly with standard microprocessors (8048, 80C51 typical)**
- **Serial and parallel microprocessor bus for control**
- **Selectable asynch/synch with internal buffer/ debuffer and scrambler/descrambler functions**
- **All synchronous (internal, external, slave) and asynchronous operating modes**
- **Adaptive equalization for optimum performance over all lines**
- **Programmable transmit attenuation (16 dB, 1 dB steps), and selectable receive boost (+18 dB)**
- **Call progress, carrier, answer tone, unscrambled mark, S1, SCT (900 Hz) calling tone (1300 Hz) and signal quality monitors**
- **DTMF, answer, calling, SCT and guard tone generators**
- **Test modes available: ALB, DL, RDL; Mark, Space and Alternating bit pattern generators**
- **CMOS technology for low power consumption**
- **4-wire full duplex operation in all modes**

BLOCK DIAGRAM



CAUTION: Use handling procedures necessary for a static sensitive component.

DESCRIPTION (Continued)

The SSI 73K324L offers full hardware and software compatibility with other products in Silicon Systems' K-Series family of single-chip modems, allowing system upgrades with a single component change. The SSI 73K324L is ideal for use in free-standing or integral system modem products where full-duplex 2400 bit/s operation with alternate mode capability is required. Its high functionality, low power consumption, and efficient packaging simplify design requirements and increase system reliability. A complete modem requires only the addition of the phone line interface, a control microprocessor, and RS-232 level converters for a typical system.

The SSI 73K324L is designed to provide a complete V.22bis, V.22, Bell 212A, V.21, and V.23 compatible modem on a chip. Many functions were included to simplify implementation in typical modem designs. In addition to the basic 2400 bit/s QAM, 1200/600 bit/s DPSK and 1200/300/75 bit/s FSK modulator/demodulator sections, the device also includes synch/asynch buffering, DTMF, answer, soft carrier, guard, and calling tone generator capabilities. Handshake pattern detectors simplify control of connect sequences, and precise tone detectors allow accurate detection of call progress, answer, calling, and soft carrier turn off tones. All operating modes defined by the incorporated standards are included, and test modes are provided. Most functions are selectable as options, and logical defaults are provided. The device can be directly interfaced to a microprocessor via its 8-bit multiplexed address/data bus for control and status monitoring. Data communications takes place through a separate serial port. Data may also be sent and received through the control registers. This simplifies designs requiring speed buffering, error control and compression.

FUNCTIONAL DESCRIPTION

QAM MODULATOR/DEMODULATOR

The SSI 73K324L encodes incoming data into quadbits represented by 16 possible signal points with specific phase and amplitude levels. The baseband signal is then filtered to reduce intersymbol interference on the bandlimited telephone network. The modulator transmits this encoded data using either a 1200 Hz (originate mode) or 2400 Hz (answer mode) carrier. The demodulator, although more complex, essentially reverses this procedure while also recovering the data clock from the incoming signal. Adaptive equalization corrects for varying line conditions by automatically changing filter parameters to compensate for line characteristics.

DPSK MODULATOR/DEMODULATOR

The SSI 73K324L modulates a serial bit stream into di-bit pairs that are represented by four possible phase shifts as prescribed by the Bell 212A/V.22 standards. The baseband signal is then filtered to reduce intersymbol interference on the bandlimited 2-wire PSTN line. Transmission occurs on either a 1200 Hz (originate mode) or 2400 Hz carrier (answer mode). Demodulation is the reverse of the modulation process, with the incoming analog signal eventually decoded into di-bits and converted back to a serial bit stream. The demodulator also recovers the clock which was encoded into the analog signal during modulation. Demodulation occurs using either a 1200 Hz carrier (answer mode or ALB originate mode) or a 2400 Hz carrier (originate mode or ALB answer mode). The SSI 73K324L use a phase locked loop coherent demodulation technique that offers excellent performance. Adaptive equalization is also used in DPSK modes for optimium operation with varying lines.

FSK MODULATOR/DEMODULATOR

The FSK modulator/demodulator produces a frequency modulated analog output signal using two discrete frequencies to represent the binary data. V.21 frequencies of 980 and 1180 Hz (originate mark and space), or 1650 and 1850 Hz (answer mark and space) are used in V.21 mode. V. 23 mode uses 1300 and 2100 Hz for the main channel or 390 and 450 Hz for the back channel. Demodulation involves detecting the received frequencies and decoding them into the appropriate binary value. The rate converter and scrambler/descrambler are automatically bypassed in the FSK modes.

PASSBAND FILTERS AND EQUALIZERS

High and low band filters are included to shape the amplitude and phase response of the transmit and receive signals and to provide compromise delay equalization as well as rejection of out-of-band signals. The transmit signal filtering corresponds to a $\sqrt{75\%}$ raised cosine frequency response characteristic.

ASYNCHRONOUS MODE

The asynchronous mode is used for communication with asynchronous terminals which may transfer data at 600, 1200, or 2400 bit/s +1%, -2.5% even though the modem's output is limited to the nominal bit rate ±.01% in DPSK and QAM modes. When transmitting in this mode the serial data on the TxD input is passed through a rate converter which inserts or deletes stop bits in the serial bit stream in order to output a signal that is the nominal bit rate ±.01%. This signal is then routed to a data scrambler and into the analog modulator where di-bit or quad-bit encoding results in the output signal. Both the rate converter and scrambler can be bypassed for handshaking and synchronous operation as selected. Received data is processed in a similar fashion except that the rate converter now acts to reinsert any deleted stop bits and output data to the terminal at no greater than the bit rate plus 1%. An incoming break signal (low through two characters) will be recognized and passed through without incorrectly inserting a stop bit.

The SYNC/ASYNC converter has an extended overspeed mode which allows selection of an output speed range of either +1% or +2.3%. In the extended overspeed mode, some stop bits are output at 7/8 the normal width.

Both the SYNC/ASYNC rate converter and the data descrambler are automatically bypassed in the FSK modes.

SYNCHRONOUS MODE

Synchronous operation is possible only in the QAM or DPSK modes. Operation is similar to that of the asynchronous mode except that data must be synchronized to a clock and no variation in data transfer rate is allowable. Serial input data appearing at TXD must be valid on the rising edge of TXCLK.

TXCLK is an internally derived 1200 or 2400 Hz signal in internal mode and is connected internally to the RXCLK pin in slave mode. Receive data at the RXD pin is clocked out on the falling edge of RXCLK. The asynch/synch converter is bypassed when synchronous mode is selected and data is transmitted out at essentially the same rate as it is input.

PARALLEL CONTROL INTERFACE

Eight 8-bit registers are provided for control, option select, and status monitoring. These registers are addressed with the AD0, AD1, and AD2 multiplexed address lines (latched by ALE) and appear to a control microprocessor as seven consecutive memory locations. Six contol registers are read/write. The detect and ID registers are read only and cannot be modified except by modem response to monitored parameters.

SERIAL CONTROL INTERFACE

The serial command mode allows access to the SSI 73K324 control and status registers via a serial control port. In this mode the A0, A1, and A2 lines provide register addresses for data passed through the DATA pin under control of the $\overline{RD}$ and $\overline{WR}$ lines. A read operation is initiated when the $\overline{RD}$ line is taken low. The next eight cycles of EXCLK will then transfer out eight bits of the selected addresss location LSB first. A write takes place by shifting in eight bits of data LSB first for eight consectuive cycles of EXCLK. $\overline{WR}$ is then pulsed low and data transfer into the selected register occurs on the rising edge of $\overline{WR}$.

TONE GENERATOR

The DTMF generator controls the sending of the sixteen standard DTMF tone pairs. The tone pair sent is determined by selecting TRANSMIT DTMF (bit D4) and the 4 DTMF bits (D0-D3) of the TONE register. Transmission of DTMF tones from TXA is gated by the TRANSMIT ENABLE bit of CR0 (bit D1) as with all other analog signals.

FULL DUPLEX OPERATION

Four-wire full duplex operation is allowed in all modes. This feature allows transmission and reception in the same band for four wire applications only.

PIN DESCRIPTION

POWER

NAME	TYPE	DESCRIPTION
GND	I	System Ground.
VDD	I	Power supply input, 5V -5% +10%. Bypass with .22 µF and 22 µF capacitors to GND.
VREF	O	An internally generated reference voltage. Bypass with .22 µF capacitor to GND.
ISET	I	Chip current reference. Sets bias current for op-amps. The chip current is set by connecting this pin to VDD through a 2 MΩ resistor. Iset should be bypassed to GND with a .22 µF capacitor.

PARALLEL MICROPROCESSOR INTERFACE

ALE	I	Address latch enable. The falling edge of ALE latches the address on AD0-AD2 and the chip select on $\overline{CS}$.
AD0-AD7	I/O / Tristate	Address/data bus.These bidirectional tri-state multi-plexed lines carry information to and from the internal registers.
$\overline{CS}$	I	Chip select. A low on this pin allows a read cycle or a write cycle to occur. AD0-AD7 will not be driven and no registers will be written if $\overline{CS}$ (latched) is not active. $\overline{CS}$ is latched on the falling edge of ALE.
CLK	O	Output clock. This pin is selectable under processor control to be either the crystal frequency (for use as a processor clock) or 16 x the data rate for use as a baud rate clock in QAM/DPSK modes only. The pin defaults to the crystal frequency on reset.
$\overline{INT}$	O	Interrupt. This open drain weak pullup, output signal is used to inform the processor that a detect flag has occurred. The processor must then read the detect register to determine which detect triggered the interrupt. $\overline{INT}$ will stay active until the processor reads the detect register or does a full reset.
$\overline{RD}$	I	Read. A low requests a read of the SSI 73K324L internal registers. Data cannot be output unless both $\overline{RD}$ and the latched $\overline{CS}$ are active or low.
RESET	I	Reset. An active high signal on this pin will put the chip into an inactive state. All control register bits (CR0, CR1, CR2, CR3, Tone) will be reset. The output of the CLK pin will be set to the crystal frequency. An internal pull down resistor permits power on reset using a capacitor to VDD.
$\overline{WR}$	I	Write. A low on this informs the SSI 73K224L that data is available on AD0-AD7 for writing into an internal register. Data is latched on the rising edge of $\overline{WR}$. No data is written unless both $\overline{WR}$ and the latched $\overline{CS}$ are low.

Note: The serial control mode is provided in the parallel versions by tying ALE high and $\overline{CS}$ low. In this configuration AD7 becomes DATA and AD0, AD1 and AD2 become A0, A1 and A2, respectively.

RS-232 INTERFACE

NAME	TYPE	DESCRIPTION
EXCLK	I	External Clock. This signal is used in synchronous transmission when the external timing option has been selected. In the external timing mode the rising edge of EXCLK is used to strobe synchronous transmit data available on the TXD pin. Also used for serial control interface.
RXCLK	O/Tristate	Receive Clock Tri-statable. The falling edge of this clock output is coincident with the transitions in the serial received DPSK/QAM data output. The rising edge of RXCLK can be used to latch the valid output data. RXCLK will be valid as long as a carrier is present. In V.23 or V.21 mode a clock which is 16 x 1200/ 75 or 16 x 300 Hz data rate is output, respectively.
RXD	O	Received Data Output. Serial receive data is available on this pin. The data is always valid on the rising edge of RXCLK when in synchronous mode. RXD will output constant marks if no carrier is detected.
TXCLK	O/Tristate	Transmit Clock Tri-statable. This signal is used in synchronous DPSK/QAM transmission to latch serial input data on the TXD pin. Data must be provided so that valid data is available on the rising edge of the TXCLK. The transmit clock is derived from different sources depending upon the synchronization mode selection. In Internal Mode the clock is generated internally (2400 Hz for QAM, 1200 Hz for DPSK or 600 Hz for half-speed DPSK). In External Mode TXCLK is phase locked to the EXCLK pin. In Slave Mode TXCLK is phase locked to the RXCLK pin. TXCLK is always active. In V.23 or V.21 mode the output is a 16 x 1200/75 or 16 x 300 Hz clock, respectively.
TXD	I	Transmit Data Input. Serial data for transmission is input on this pin. In synchronous modes, the data must be valid on the rising edge of the TXCLK clock. In asynchronous modes (2400/1200/600 bit/s, or 75/300 baud) no clocking is necessary. DPSK/QAM data must be +1%, -2.5% or +2.3%, -2.5 % in extended overspeed mode.

ANALOG INTERFACE

RXA	I	Received modulated analog signal input from the phone line.
TXA	O	Transmit analog output to the phone line.
XTL1	I	These pins are for the internal crystal oscillator requiring a 11.0592 MHz parallel mode crystal. Two capacitors from these pins to ground are also required for proper crystal operation. Consult crystal manufacturer for proper values. XTL2 can also be driven from an external clock.
XTL2	I/O	

PIN DESCRIPTION (continued)

SERIAL MICROPROCESSOR INTERFACE

NAME	TYPE	DESCRIPTION
A0-A2	I	Register Address Selection. These lines carry register addresses and should be valid during any read or write operation.
DATA	I/O	Serial Control Data. Data for a read/write operation is clocked in or out on the falling edge of the EXCLK pin. The direction of data flow is controlled by the $\overline{RD}$ pin. $\overline{RD}$ low outputs data. $\overline{RD}$ high inputs data.
$\overline{RD}$	I	Read. A low on this input informs the SSI 73K322L that data or status information is being read by the processor. The falling edge of the $\overline{RD}$ signal will initiate a read from the addressed register. The $\overline{RD}$ signal must continue for eight falling edges of EXCLK in order to read all eight bits of the referenced register. Read data is provided LSB first. Data will not be output unless the $\overline{RD}$ signal is active.
$\overline{WR}$	I	Write. A low on this input informs the SSI 73K322L that data or status information has been shifted in through the DATA pin and is available for writing to an internal register. The normal procedure for a write is to shift in data LSB first on the DATA pin for eight consecutive falling edges of EXCLK and then to pulse $\overline{WR}$ low. Data is written on the rising edge of $\overline{WR}$.

Note: In the serial, 22-pin version, the pins AD0-AD7, ALE and $\overline{CS}$ are removed and replaced with the pins; A0, A1, A2, DATA, and EXCLK. Also, the $\overline{RD}$ and $\overline{WR}$ controls are used differently.

REGISTER DESCRIPTIONS

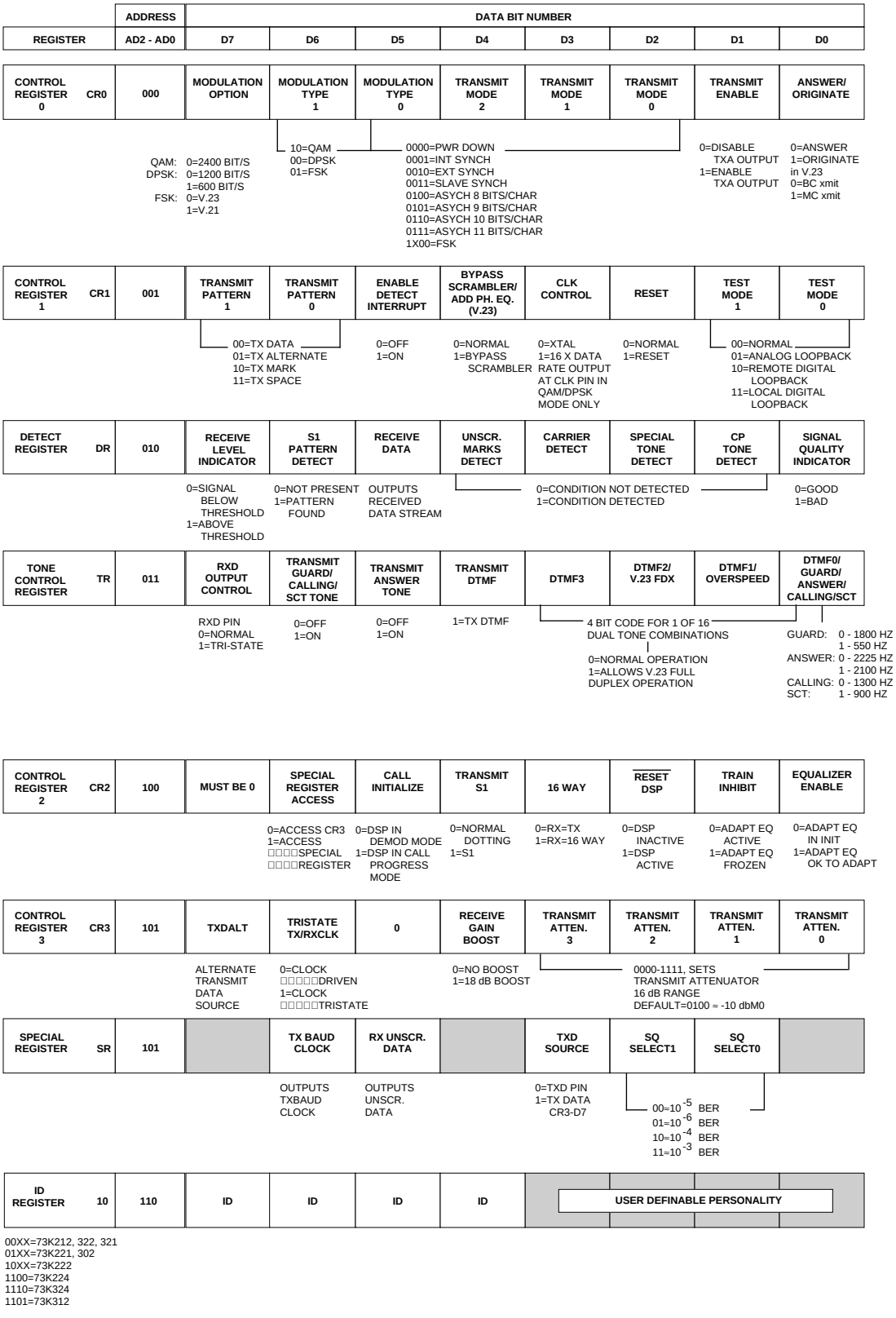
Eight 8-bit internal registers are accessible for control and status monitoring. The registers are accessed in read or write operations by addressing the A0, A1 and A2 address lines in serial mode, or the AD0, AD1 and AD2 lines in parallel mode. The address lines are latched by ALE. Register CR0 controls the method by which data is transferred over the phone line. CR1 controls the interface between the microprocessor and the SSI 73K324L internal state. DR is a detect register which provides an indication of monitored modem status conditions. TR, the tone control register, controls the DTMF generator, answer, guard tones, SCT, calling tone, and RXD output gate used in the modem initial connect sequence. CR2 is the primary DSP control interface and CR3 controls transmit attenuation and receive gain adjustments. All registers are read/write except for DR and ID which are read only. Register control and status bits are identified below:

REGISTER BIT SUMMARY

		ADDRESS	DATA BIT NUMBER							
REGISTER		AD - A0	D7	D6	D5	D4	D3	D2	D1	D0
CONTROL REGISTER 0	CR0	000	MODULATION OPTION	MODULATION TYPE 1	MODULATION TYPE 0	TRANSMIT MODE 2	TRANSMIT MODE 1	TRANSMIT MODE 0	TRANSMIT ENABLE	ANSWER/ ORIGINATE
CONTROL REGISTER 1	CR1	001	TRANSMIT PATTERN 1	TRANSMIT PATTERN 0	ENABLE DETECT INTERRUPT	BYPASS SCRAMBLER/ ADD PH. EQ. (V.23)	CLK CONTROL	RESET	TEST MODE 1	TEST MODE 0
DETECT REGISTER	DR	010	RECEIVE LEVEL	PATTERN S1 DET	RECEIVE DATA	UNSCR. MARK DETECT	CARRIER DETECT	SPECIAL TONE DETECT	CALL PROGRESS DETECT	SIGNAL QUALITY
TONE CONTROL REGISTER	TR	011	RXD OUTPUT CONTROL	TRANSMIT GUARD TONE/ SCT/CALLING TONE	TRANSMIT ANSWER TONE	TRANSMIT DTMF	DTMF3	DTMF2/ 4 WIRE FDX	DTMF1/ OVERSPEED	DTMF0/GUARD/ ANSWER/ CALLING/SCT
CONTROL REGISTER 2	CR2	100	0	SPECIAL REGISTER ACCESS	CALL INITIALIZE	TRANSMIT S1	16 WAY	RESET DSP	TRAIN INHIBIT	EQUALIZER ENABLE
CONTROL REGISTER 3	CR3	101	TXDALT	TRISTATE TX/RXCLK	0	RECEIVE GAIN BOOST	TRANSMIT ATTEN. 3	TRANSMIT ATTEN. 2	TRANSMIT ATTEN. 1	TRANSMIT ATTEN. 0
SPECIAL REGISTER	SR	101		TX BAUD CLOCK	RX UNSCR. DATA		TXD SOURCE	SQ SELECT 1	SQ SELECT 0	
ID REGISTER	ID	110	ID	ID	ID	ID	USER DEFINABLE PERSONALITY			

NOTE: When a register containing reserved control bits is written into, the reserved bits must be programmed as 0's.

REGISTER ADDRESS TABLE



CONTROL REGISTER 0

	D7	D6	D5	D4	D3	D2	D1	D0
CR0 000	MODUL. OPTION	MODUL. TYPE 1	MODUL. TYPE 0	TRANSMIT MODE 2	TRANSMIT MODE 1	TRANSMIT MODE 0	TRANSMIT ENABLE	ANSWER/ ORIGINATE

BIT NO.	NAME	CONDITION	DESCRIPTION
D0	Answer/ Originate	0	Selects answer mode (transmit in high band, receive in low band or in V.23 HDX mode, receive at 1200 bit/s and transmit at 75 bit/s.)
		1	Selects originate mode (transmit in low band,receive in high band or in V.23 HDX mode, receive at 75 bit/s and transmit at 1200 bit/s.)
			Note: This bit works with Tone Register bits D0 and D6 to program special tones detected in the Detect Register. See Detect and Tone Registers.
D1	Transmit Enable	0	Disables transmit output at TXA.
		1	Enables transmit output at TXA.
			Note: Transmit Enable must be set to 1 to allow activation of Answer Tone, DTMF, or Carrier.
D5, D4, D3, D2	Transmit Mode	D5 D4 D3 D2	
		0 0 0 0	Selects power down mode. All functions disabled except digital interface.
		0 0 0 1	Internal synchronous mode. In this mode TXCLK is an internally derived 600, 1200 or 2400 Hz signal. Serial input data appearing at TXD must be valid on the rising edge of TXCLK. Receive data is clocked out of RXD on the falling edge of RXCLK.
		0 0 1 0	External synchronous mode. Operation is identical to internal synchronous, but TXCLK is connected internally to EXCLK pin, and a 600, 1200 or 2400 Hz clock must be supplied externally.
		0 0 1 1	Slave synchronous mode. Same operation as other synchronous modes. TXCLK is connected internally to the RXCLK pin in this mode.
		0 1 0 0	Selects asynchronous mode - 8 bits/character (1 start bit, 6 data bits, 1 stop bit).
		0 1 0 1	Selects asynchronous mode - 9 bits/character (1 start bit, 7 data bits, 1 stop bit).
		0 1 1 0	Selects asynchronous mode - 10 bits/character (1 start bit, 8 data bits, 1 stop bit).
		0 1 1 1	Selects asynchronous mode - 11 bits/character (1 start bit, 8 data bits, Parity and/or 1 or 2 stop bits).
		1 X 0 0	Selects FSK operation.

CONTROL REGISTER 0 (Continued)

BIT NO.	NAME	CONDITION	DESCRIPTION
D6,D5	Modulation Type	D6 D5	
		1 0	QAM
		0 0	DPSK
		0 1	FSK
D7	Modulation Option	0	QAM selects 2400 bit/s. DPSK selects 1200 bit/s. FSK selects V.23 mode.
		1	DPSK selects 600 bit/s. FSK selects V.21 mode.

CONTROL REGISTER 1

	D7	D6	D5	D4	D3	D2	D1	D0
CR1 001	TRANSMIT PATTERN 1	TRANSMIT PATTERN 0	ENABLE DETECT INT.	BYPASS SCRAMB/ ADD PH.EQ	CLK CONTROL	RESET	TEST MODE 1	TEST MODE 0

BIT NO.	NAME	CONDITION	DESCRIPTION
D1, D0	Test Mode	D1 D0	
		0 0	Selects normal operating mode.
		0 1	Analog loopback mode. Loops the transmitted analog signal back to the receiver, and causes the receiver to use the same carrier frequency as the transmitter. To squelch the TXA pin, transmit enable bit must be low. Tone Register bit D2 must be zero.
		1 0	Selects remote digital loopback. Received data is looped back to transmit data internally, and RXD is forced to a mark. Data on TXD is ignored.
		1 1	Selects local digital loopback. Internally loops TXD back to RXD and continues to transmit data carrrier at TXA pin.
D2	Reset	0	Selects normal operation.
		1	Resets modem to power down state. All control register bits (CR0, CR1, CR2, CR3 and Tone) are reset to zero except CR3 bit D2. The output of the clock pin will be set to the crystal frequency.
D3	CLK Control (Clock Control)	0	Selects 11.0592 MHz crystal echo output at CLK pin.
		1	Selects 16 X the data rate output at CLK pin in QAM and DPSK only.

CONTROL REGISTER 1 (Continued)

	D7	D6	D5	D4	D3	D2	D1	D0
CR1 001	TRANSMIT PATTERN 1	TRANSMIT PATTERN 0	ENABLE DETECT INT.	BYPASS SCRAMB/ ADD PH.EQ.	CLK CONTROL	RESET	TEST MODE 1	TEST MODE 0

BIT NO.	NAME	CONDITION	DESCRIPTION
D4	Bypass Scrambler/ Add Ph. Eq.	0	Selects normal operation. DPSK and QAM data is passed through scrambler.
		1	Selects Scrambler Bypass. DPSK and QAM data is routed around scrambler in the transmit path. In the V.23 mode, additional phase equalization is added to the main channel filters when D4 is set to 1.
D5	Enable Detect Interrupt	0	Disables interrupt at $\overline{INT}$ pin. All interrupts are normally disabled in power down mode.
		1	Enables $\overline{INT}$ output. An interrupt will be generated with a change in status of DR bits D1-D4 and D6. The answer tone and call progress detect interrupts are masked when the TX enable bit is set. Carrier detect is masked when TX DTMF is activated. All interrupts will be disabled if the device is in power down mode.
D7, D6	Transmit Pattern	D7 D6	
		0 0	Selects normal data transmission as controlled by the state of the TXD pin.
		0 1	Selects an alternating mark/space transmit pattern for modem testing and handshaking. Also used for S1 pattern generation. See CR2 bit D4.
		1 0	Selects a constant mark transmit pattern.
		1 1	Selects a constant space transmit pattern.

DETECT REGISTER

	D7	D6	D5	D4	D3	D2	D1	D0
DR 010	RECEIVE LEVEL INDICATOR	S1 PATTERN DETECT	RECEIVE DATA	UNSCR. MARK DETECT	CARRIER DETECT	SPECIAL TONE DETECT	CALL PROG. DETECT	SIGNAL QUALITY INDICATOR

BIT NO.	NAME	CONDITION			DESCRIPTION
D0	Signal Quality Indicator	0			Indicates normal received signal.
		1			Indicates low received signal quality (above average error rate). Interacts with Special Register SQ bits D2, D1.
D1	Call Progress Detect	0			No call progress tone detected.
		1			Indicates presence of call progress tones. The call progress detection circuitry is activated by energy in the normal 350 to 620 Hz call progress band.
D2	Special Tone Detect	0			Condition not detected
		1			Condition detected
		CR0 D0	TR D0	CR2 D5	
		1	0	1	2225 Hz ±10 Hz answer tone detected in V.22bis, V.22, V.21 modes.
		1	1	1	2100 Hz ±21 Hz answer tone detected in V.22bis, V.22, V.21 modes.
		0	0	1	1300 Hz calling tone detected in V.22 bis, V.22, V.21, V.23 modes.
		0	X	0	900 Hz SCT tone detected in V.23 mode.
		I	X	O	2100 Hz or 2225 Hz answer tone detected in QAM, DPSK, or V.21 Mode.
D3	Carrier Detect	0			No carrier detected in the receive channel.
		1			Indicated carrier has been detected in the received channel. Should be time qualified by software.
D4	Unscr. Mark Detect	0			No unscrambled mark being received.
		1			Indicates detection of unscrambled marks in the received data. Should be time qualified by software.
D5	Receive Data				Continuously outputs the received data stream. This data is the same as that output on the RXD pin, but it is not disabled when RXD is tri-stated.
D6	S1 Pattern Detect	0			No S1 pattern being received.
		1			S1 pattern detected. Should be time qualified by software. S1 is an unscrambled double dibit (11001100...) sent in DPSK 1200 bit/s mode. Generated pattern must be properly aligned to transmitter baud clock to be detected.
D7	Receive Level Indicator	0			Received signal level below threshold, (≈ -25 dBm0);can use receive gain boost (+18 dB.)
		1			Received signal above threshold.

TONE REGISTER

	D7	D6	D5	D4	D3	D2	D1	D0
TR 011	RXD OUTPUT CONTR.	TRANSMIT GUARD/ CALLING/SCT TONE	TRANSMIT ANSWER TONE	TRANSMIT DTMF	DTMF 3	DTMF 2/ WIRE FDX	DTMF 1/ OVER-SPEED	DTMF 0/ G.T./ANSW./ CALLING/SCT TONE/SEL

BIT NO.	NAME	CONDITION	DESCRIPTION
D0, D4, D5, D6	DTMF 0/ Guard Tone/ Answer Tone/ Calling/SCT Tone/ Transmit Select	D6 D5 D4 D0	D0 interacts with bits D6, D5, D4, and CR0 as shown.
		X X 1 X	Transmit DTMF tones (overides all other functions).
		1 0 0 0	Select 1800 Hz guard tone if in V.22bis or V.22 and answer mode in CR0.
		1 0 0 1	Select 550 Hz guard tone if in V.22bis or V.22 and answer mode in CR0.
		Note: Bit D0 also selects the answer tone detected in originate mode, see Detect Register Special Tone Detect (bit D2) for details.	
		1 0 0 0	1300 Hz calling tone will be transmittted if V.21, V.22, V.22bis or V.23 originate mode is selected in CR0.
		X 1 0 0	Transmit 2225 Hz Answer Tone. Must be in DPSK answer mode.
		X 1 0 1	Transmit 2100 Hz Answer Tone. Must be in DPSK answer mode.
		1 0 0 1	900 Hz SCT (soft carrier turnoff) tone transmitted in V.23 75 bit/s receive mode. (CR0 bit D0 = 1).
D1	DTMF 1/ Overspeed	D4 D1	D1 interacts with D4 as shown.
		0 0	Asynchronous QAM/DPSK +1% -2.5%. (Normal).
		0 1	Asynchronous QAM/DPSK, 2400, 1200 or 600 bit/s +2.3% -2.5%. (Extended overspeed).
D2	DTMF 2/ 4 WIRE FDX	D4 D2	
		0 0	Selects 2-wire full-duplex or half-duplex.
		0 1	D2 selects 4 wire full duplex in the modulation mode selected. The receive path corresponds to the ANS/ ORIG bit CR0 D0 in terms of high or low band selection. The transmitter is in the same band as the receiver, but does not have magnitude filtering or equalization on its signal as in the receive path.

Note: DTMF0 - DTMF2 should be set to an appropriate state after DTMF dialing to avoid unintended operation.

TONE REGISTER (Continued)

	D7	D6	D5	D4	D3	D2	D1	D0
TR 011	RXD OUTPUT CONTR.	TRANSMIT GUARD/ CALLING/SCT TONE	TRANSMIT ANSWER TONE	TRANSMIT DTMF	DTMF 3	DTMF 2/ WIRE FDX	DTMF 1/ OVER-SPEED	DTMF 0/ GUARD/ CALLING/SCT TONE SEL

BIT NO.	NAME	CONDITION	DESCRIPTION
D3, D2, D1, D0	DTMF 3, 2, 1, 0	D4 = 1	Programs 1 of 16 DTMF tone pairs that will be transmitted when TX DTMF and TX enable bit (CR0, bit D1) is set. Tone encoding is shown below:

KEYBOARD EQUIVALENT	DTMF CODE D3	D2	D1	D0	TONES LOW	HIGH
1	0	0	0	1	697	1209
2	0	0	1	0	697	1336
3	0	0	1	1	697	1477
4	0	1	0	0	770	1209
5	0	1	0	1	770	1336
6	0	1	1	0	770	1477
7	0	1	1	1	852	1209
8	1	0	0	0	852	1336
9	1	0	0	1	852	1477
0	1	0	1	0	941	1336
*	1	0	1	1	941	1209
#	1	1	0	0	941	1477
A	1	1	0	1	697	1633
B	1	1	1	0	770	1633
C	1	1	1	1	852	1633
D	0	0	0	0	941	1633

D7	RXD Output Control	0	Enables RXD pin. Receive data will be output on RXD.
		1	Disables RXD pin.The RXD pin reverts to a high impedance with internal weak pull-up resistor.

CONTROL REGISTER 2

	D7	D6	D5	D4	D3	D2	D1	D0
CR2 100	0	SPEC REG ACCESS	CALL INIT	TRANSMIT S1	16 WAY	$\overline{\text{RESET}}$ DSP	TRAIN INHIBIT	EQUALIZER ENABLE

BIT NO.	NAME	CONDITION	DESCRIPTION
D0	Equalizer Enable	0	The adaptive equalizer is in its initialized state.
		1	The adaptive equalizer is enabled. This bit is used in handshakes to control when the equalizer should calculate its coefficients.
D1	Train Inhibit	0	The adaptive equalizer is active.
		1	The adaptive equalizer coefficients are frozen.
D2	$\overline{\text{RESET DSP}}$	0	The DSP is inactive and all variables are initialized.
		1	The DSP is running based on the mode set by other control bits
D3	16 Way	0	The receiver and transmitter are using the same decision plane (based on the Modulator Control Mode).
		1	The receiver, independent of the transmitter, is forced into a 16 point decision plane. Used for QAM handshaking.
D4	Transmit S1	0	The transmitter when placed in alternating mark/space mode transmits 0101 . . . . scrambled or not dependent on the bypass scrambler bit and modulation mode.
		1	When this bit is 1 and only when the transmitter is placed in alternating mark/space mode by CR1 bits D7, D6, an unscrambled repetitive double dibit pattern of 00 and 11 at 1200 bit/s (S1) is sent.
D5	Call Init	0	The DSP is setup to do demodulation and pattern detection based on the various mode bits. Both answer tones are detected in Demod Mode concurrently; TR D0 is ignored.
		1	The DSP decodes call progress, calling tones, unscrambled mark, and 2100 Hz and 2225 Hz answer tones.
D6	Special Register Access	0	Normal CR3 access.
		1	Setting this bit and addressing CR3 allows access to the SPECIAL REGISTER. See the SPECIAL REGISTER for details.
D7	N/A	0	Must be 0 for normal operation.

CONTROL REGISTER 3

	D7	D6	D5	D4	D3	D2	D1	D0
CR3 101	TXDALT	TRISTATE TX/RXCLK	0	RECEIVE ENABLE BOOST	TRANSMIT ATTEN. 3	TRANSMIT ATTEN. 2	TRANSMIT ATTEN. 1	TRANSMIT ATTEN. 0

BIT NO.	NAME	CONDITION	DESCRIPTION
D3, D2, D1,D0	Transmit Attenuator	D3 D2 D1 D0 0 0 0 0 - 1 1 1 1	Sets the attenuation level of the transmitted signal in 1dB steps. The default (D3-D0=0100) is for a transmit level of -10 dBm0. The total range is 16 dB.
D4	Receive Gain Boost (18 dB)	0	18 dB receive front end boost is not used.
		1	Boost is in the path. This boost does not change reference levels. It is used to extend dynamic range by compensating for internally generated noise when receiving weak signals. The receive level detect signal and knowledge of the hybrid and transmit attenuator setting will determine when boost should be enabled.
D5	Not Used	0	Not used. Only write zeros this location.
D6	Tristate TXCLK/RXCLK	0	TXCLK, RXCLK outputs driven
		1	TXCLK, RXCLK outputs in Tristate mode
D7	TXDALT	Spec. Reg. bit D3=1	Alternate TX data source. See Special Register.

ID REGISTER

SPECIAL REGISTER

	D7	D6	D5	D4	D3	D2	D1	D0
SR 101		TXBAUD CLOCK	RXUN- DSCR DATA		TXD SOURCE	SIGNAL QUALITY LEVEL SELECT1	SIGNAL QUALITY LEVEL SELECT0	

BIT NO.	NAME	DESCRIPTION
D7, D4, D0		NOT USED AT THIS TIME. Only write ZEROs to these bits.
D6	TXBAUD CLK	TXBAUD clock is the transmit baud-synchronous clock that can be used to synchronize the input of arbitrary quad/di-bit patterns. The rising edge of TXBAUD signals the latching of a baud-worth of data internally. Synchronous data to be entered via the TXDALT bit, CR3 bit D7, should have data transitions that start 1/2 bit period delayed from the TXBAUD clock edges.
D5	RXUNDSCR DATA	This bit outputs the data received before going to the descrambler. This is useful for sending special unscrambled patterns that can be used for signaling.

SPECIAL REGISTER (Continued)

BIT NO.	NAME	DESCRIPTION	
D3	TXD SOURCE	This bit selects the transmit data source; either the TXD pin if ZERO or the TXDALT if this bit is a ONE. The TRANSMIT PATTERN bits D7 and D6 in CR1 override either of these sources.	
D2, D1	SIGNAL QUALITY LEVEL SELECT	The signal quality indicator is a logical zero when the signal received is acceptable for low error rate reception. It is determined by the value of the Mean Squared Error (MSE) calculated in the decisioning process when compared to a given threshold. This threshold can be set to four levels of error rate. The SQI bit will be low for good or average connections. As the error rate crosses the threshold setting, the SQI bit will toggle at a 1.66 ms rate. Toggling will continue until the error rate indicates that the data pump has lost convergence and a retrain is required. At that point the SQI bit will be a ONE constantly. The SQI bit and threshold selection are valid for QAM and DPSK only.	
	D2 D1	**TYPICAL THRESHOLD VALUE**	**UNITS**
	0 0	10^{-5}	BER (default)
	0 1	10^{-6}	BER
	1 0	10^{-4}	BER
	1 1	10^{-3}	BER

NOTE: This register is "mapped" and is accessed by setting CR2 bit D6 to a ONE and addressing CR3. This register provides functions to the 73K324L user that are not necessary in normal communications. Bits D7-D4 are read only, while D3-D0 are read/write. To return to normal CR3 access, CR2 bit D6 must be returned to a ZERO.

	D7	D6	D5	D4	D3	D2	D1	D0
ID 110	ID 3	ID 2	ID 1	ID 0	USER DEFINABLE PERSONALITY			

BIT NO.	NAME	CONDITION	DESCRIPTION
D7, D6, D5, D4	Device Identification Signature	D7 D6 D5 D4	Indicates Device:
		0 0 X X	SSI 73K212(L) or 73K322L or 73K321L
		0 1 X X	SSI 73K221(L) or 73K302L
		1 0 X X	SSI 73K222(L)
		1 1 0 0	SSI 73K224L
		1 1 1 0	SSI 73K324L
		1 1 0 1	SSI 73K312L

ELECTRICAL SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING
VDD Supply Voltage	7V
Storage Temperature	-65 to 150°C
Soldering Temperature (10 sec.)	260°C
Applied Voltage	-0.3 to VDD+0.3V
Note: All inputs and outputs are protected from static charge using built-in, industry standard protection devices and all outputs are short-circuit protected.	

RECOMMENDED OPERATING CONDITIONS

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNITS
VDD Supply voltage		4.5	5	5.5	V
External Components (Refer to Application section for placement.)					
VREF Bypass capacitor	(VREF to GND)	0.22			µF
Bias setting resistor	(Placed between VDD and ISET pins)	1.8	2	2.2	MΩ
ISET Bypass capacitor	(ISET pin to GND)	0.22			µF
VDD Bypass capacitor 1	(VDD to GND)	0.22			µF
VDD Bypass capacitor 2	(VDD to GND)	22			µF
XTL1 Load Capacitance	Depends on crystal requirements		18	39	pF
XTL2 Load Capacitance	Depends on crystal requirements		18	27	pF
Clock Variation	(11.0592 MHz) Crystal or external clock	-0.01		+0.01	%
TA, Operating Free-Air Temperature		-40		85	°C

DC ELECTRICAL CHARACTERISTICS
(TA = -40°C to 85°C, VDD =recommended range unless otherwise noted.)

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNITS
IDD, Supply Current	CLK = 11.0592 MHz				
	ISET Resistor = 2 MΩ				
IDD1, Active	Operating with crystal oscillator.		18	25	mA
IDD2, Idle	< 5 pF capacitive load on CLK pin.			5	mA
Digital Inputs					
VIL, Input Low Voltage				0.8	V
VIH, Input High Voltage					
All Inputs except Reset XTL1, XTL2		2.0		VDD	V
Reset, XTL1, XTL2		3.0		VDD	V
IIH, Input High Current	VI = VDD			100	µA
IIL, Input Low Current	VI = 0V	-200			µA
Reset Pull-down Current	Reset = VDD	-2	-30	-70	µA
Digital Outputs					
VOH, Output High Voltage	IO = IOH Min IOUT = -0.4 mA	2.4		VDD	V
VOL, Output Low Voltage	IO = IOUT = 1.6 mA			0.4	V
RXD Tri-State Pull-up Curr.	RXD = GND	-2		-50	µA
Capacitance					
Maximum Capacitive Load					
CLK				25	pF
Input Capacitance	All Digital Inputs			10	pF

DYNAMIC CHARACTERISTICS AND TIMING
(TA = -40°C to +85°C, VDD = recommended range unless otherwise noted.)

PARAMETERS	CONDITIONS	MIN	NOM	MAX	UNITS
QAM/DPSK Modulator					
Carrier Suppression	Measured at TXA	35			dB
Output Amplitude	TX scrambled marks ATT=0100 (default)	-11.5	-10.0	-9	dBm0
FSK Modulator/Demodulator					
Output Freq. Error	CLK = 11.0592 MHz	-.31		+0.20	%
Transmit Level	ATT = 0100 (Default) Transmit Dotting Pattern	-11.5	-10.0	-9	dBm0
TXA Output Distortion	All products through BPF			-45	dB
Output Bias Distortion at RXD	Dotting Pattern measured at RXD Receive Level -20 dBm, SNR 20 dB	-10		+10	%
Output Jitter at RXD	Integrated for 5 seconds	-15		+15	%
Sum of Bias Distortion and Output Jitter at RXD	Integrated for 5 seconds	-15		+15	%
2100 Hz Answer Tone Generator					
Output Amplitude	ATT = 0100 (Default Level) Not in V.21 or V.23 Mode	-11.5	-10	-9	dBm0
Output Distortion	Distortion products in receive band			-40	dB
DTMF Generator	Not in V.21 or V.23 mode				
Freq. Accuracy		-0.03		+0.25	%
Output Amplitude	Low Band, ATT = 0100	-10		-8	dBm0
Output Amplitude	High Band, ATT = 0100	-8		-6	dBm0
Twist	High-Band to Low-Band	1.0	2.0	3.0	dB
Receiver Dynamic Range	Refer to Performance Curves	-43		-3.0	dBm0
Call Progress Detector	In Call Init mode				
Detect Level	460 Hz input signal	-34		0	dBm0
Reject Level				-40	dBm0
Delay Time	-70 dBm0 to -30 dBm0 STEP			25	ms
Hold Time	-30 dBm0 to -70 dBm0 STEP			25	ms
Hysteresis	@ 460 Hz input signal	2			dB

NOTE: Parameters expressed in dBm0 refer to the following definition:

0 dB loss in the Transmit path to the line.

2 dB gain in the Receive path from the line.

Refer to the Basic Box Modem diagram in the Applications section for the DAA design.

DYNAMIC CHARACTERISTICS AND TIMING (continued)

PARAMETERS		CONDITIONS	MIN	NOM	MAX	UNITS
Carrier Detect Receive Gain Boost "On" for Lower Input Level Measurements						
Threshold		QAM/DPSK or FSK receive data	-48		-43	dBm0
Hysteresis		All Modes	2			dB
Delay Time	FSK	70 dBm0 to -6 dBm0	25		37	ms
		70 dBm0 to -40 dBm0	25		37	ms
	DPSK	-70 dBm0 to -6 dBm0	7		17	ms
		-70 dBm0 to -40 dBm0	7		17	ms
	QAM	-70 dBm0 to -6 dBm0	25		37	ms
		-70 dBm0 to -40 dBm0	25		37	ms
Hold Time	FSK	-6 dBm0 to -70 dBm0	25		37	ms
		-40 dBm0 to -70 dBm0	15		30	ms
	DPSK	-6 dBm0 to -70 dBm0	20		29	ms
		-40 dBm0 to -70 dBm0	14		21	ms
	QAM	-6 dBm0 to -70 dBm0	25		32	ms
		-40 dBm0 to -70 dBm0	8		28	ms
Special Tone Detectors						
Detect Level		See definitions for D0 of Tone Register	-48		-43	dBm0
Delay and Hold Time						
2225 or 2100 Hz answer tone		Call INIT mode 2225 ± 10 Hz 2100 ± 21 Hz	6		50	ms
1300 Hz calling tone		Tone Accuracy +3, -5%	10		45	ms
900 Hz SCT Receive V.23 main channel		Tone Accuracy ±9 Hz	10		45	ms
Hysteresis			2			dB
Pattern Detectors		DPSK Mode				
S1 Pattern						
Delay Time		For signals from -6 to -40 dBm0,	10		55	ms
Hold Time		Demod Mode	10		45	ms
Unscrambled Mark						
Delay Time		For signals from -6 to -40	10		45	ms
Hold Time		Demod or call Init Mode	10		45	ms
Receive Level Indicator						
Detect On			-22		-28	dBm0
Valid after Carrier Detect		DPSK Mode	1	4	7	ms

DYNAMIC CHARACTERISTICS AND TIMING (Continued)

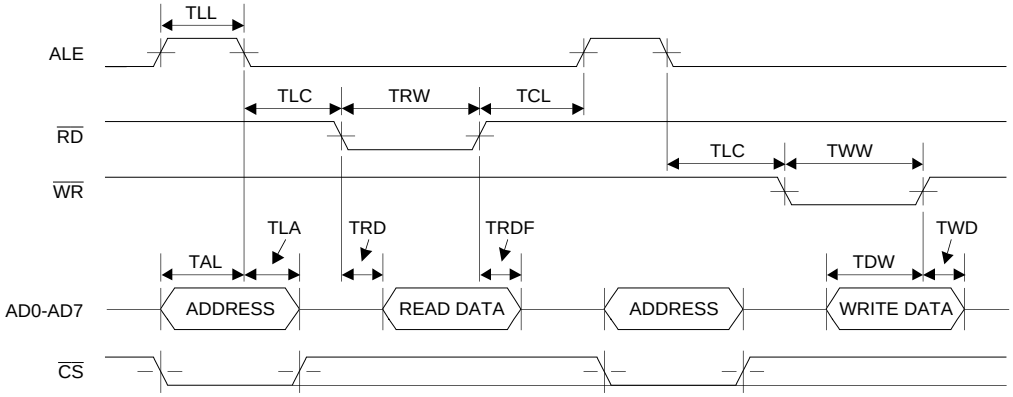
PARAMETERS	CONDITIONS	MIN	NOM	MAX	UNITS
Output Smoothing Filter					
Output Impedance	TXA pin		200	300	Ω
Output Load	TXA pin; FSK Single	10			kΩ
	Tone out for THD = -50 dB in .3 to 3.4 kHz range			50	pF
Maximum Transmitted Energy	4 kHz, Guard Tones off			-35	dBm0
	10 kHz, Guard Tones off			-55	dBm0
	12 kHz, Guard Tones off			-65	dBm0
Anti Alias Low Pass Filter					
Maximum allowed Out-of-Band Signal Energy (Defines Hybrid Trans-Hybrid loss requirements)	Scrambled data at 2400 bit/s in opposite band		-14		dBm
	Sinusoids out of band		-9		dBm
Transmit Attenuator					
Range of Transmit Level	Default ATT = 0100 (-10 dBm0) 1111-0000	-21		-6	dBm0
Step Accuracy		-0.15		+0.15	dB
Clock Noise	TXA pin; 153.6 kHz		1.5		mV rms
Carrier Offset					
Capture Range	Originate or Answer	-7	±5	+7	Hz
Recovered Clock					
Capture Range	% of data rate originate or answer	-.02		+.02	%
Guard Tone Generator					
Tone Accuracy	550 Hz		+1.2		%
	1800 Hz		-0.8		%
Tone Level	550 Hz	-4.5	-3.0	-1.5	dB
(Below QAM/DPSK Output)	1800 Hz	-7.5	-6.1	-4.5	dB
Harmonic Distortion (700 to 2900 Hz)	550 or 1800 Hz			-50	dB

DYNAMIC CHARACTERISTICS AND TIMING (Continued)

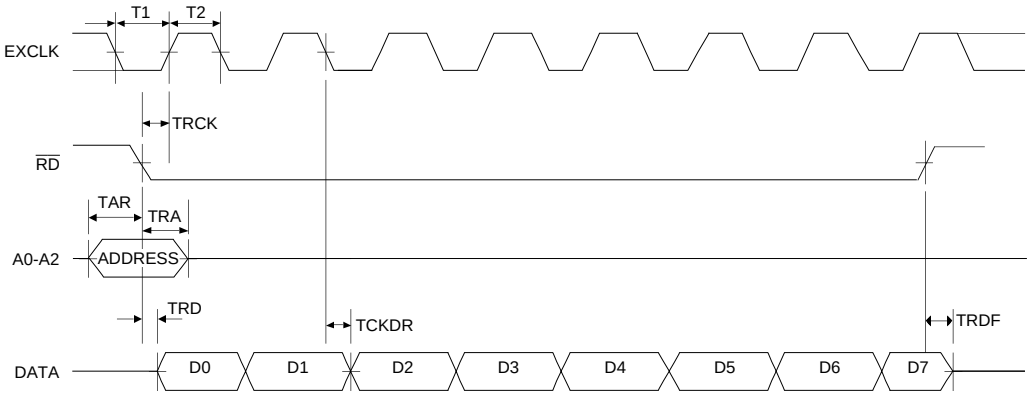
PARAMETERS	CONDITIONS	MIN	NOM	MAX	UNITS
Timing (Refer to Timing Diagrams)					
Parallel Mode:					
TAL	$\overline{CS}$/Addr. setup before ALE Low	30			ns
TLA	$\overline{CS}$/Addr. hold after ALE Low	10			ns
TLC	ALE Low to $\overline{RD}$/$\overline{WR}$ Low	40			ns
TCL	$\overline{RD}$/$\overline{WR}$ Control to ALE High	10			ns
TRD	Data out from $\overline{RD}$ Low			90	ns
TLL	ALE width	25			ns
TRDF	Data float after $\overline{RD}$ High			40	ns
TRW	$\overline{RD}$ width	70			ns
TWW	$\overline{WR}$ width	70			ns
TDW	Data setup before $\overline{WR}$ High	70			ns
TWD	Data hold after $\overline{WR}$ High	20			ns
Serial Mode:					
TRCK	Clock high after $\overline{RD}$	250		T1	ns
TAR	Address setup before $\overline{RD}$ low	0			ns
TRA	Address hold after $\overline{RD}$ low	350			ns
TRD	$\overline{RD}$ to data valid			110	ns
TRDF	Data float after $\overline{RD}$ high			50	ns
TCKDR	Read data out after falling edge of EXCLK			300	ns
TWW	$\overline{WR}$ width	350			ns
TAW	Address setup before $\overline{WR}$	50			ns
TWA	Address hold after rising edge of $\overline{WR}$	50			ns
TCKDW	Write data hold after falling edge of EXCLK	200			ns
TCKW	$\overline{WR}$ high after falling edge of EXCLK	330		T1& T2	ns
TDCK	Data setup before falling edge of EXCLK	50			ns
T1, T2	Minimum period	500			ns
Note: T1 and T2 are the low/high periods, respectively, of EXCLK in serial mode.					

TIMING DIAGRAMS

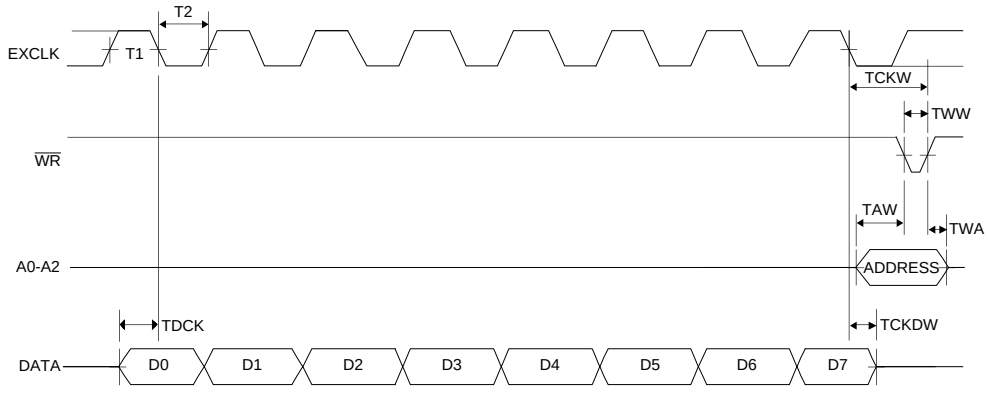
BUS TIMING DIAGRAM (PARALLEL VERSION)



READ TIMING DIAGRAM (SERIAL VERSION)



WRITE TIMING DIAGRAM (SERIAL VERSION)



APPLICATIONS INFORMATION

GENERAL CONSIDERATIONS

Figures 1 and 2 show basic circuit diagrams for K-Series modem integrated circuits. K-Series products are designed to be used in conjunction with a control processor, a UART or RS-232 serial data interface, and a DAA phone line interface to function as a typical intelligent modem. The K-Series ICs interface directly with Intel 8048 and 80C51 microprocessors for control and status monitoring purposes.Two typical DAA arrangements are shown: one for a split ±5 or ±12 volt design and one for a single 5 volt design. These diagrams are for reference only and do not represent production-ready modem designs.

K-Series devices are available with two control interface versions: one for a parallel multiplexed address/data interface, and one for a serial interface. The parallel version is intended for use with 8039/48 or 8031/51 microcontrollers from Intel or many other manufacturers. The serial interface 22-pin version can be used with other microcontrollers or in applications where only a limited number of port lines are available or the application does not lend itself to a multiplexed address/data interface. The parallel versions may also be used in the serial mode, as explained in the data sheet pin description.

In most applications the controller will monitor the serial data for commands from the DTE and the received data for break signals from the far end modem. In this way, commands to the modem are sent over the same line as the transmitted data. In other applications the RS-232 interface handshake lines are used for modem control.

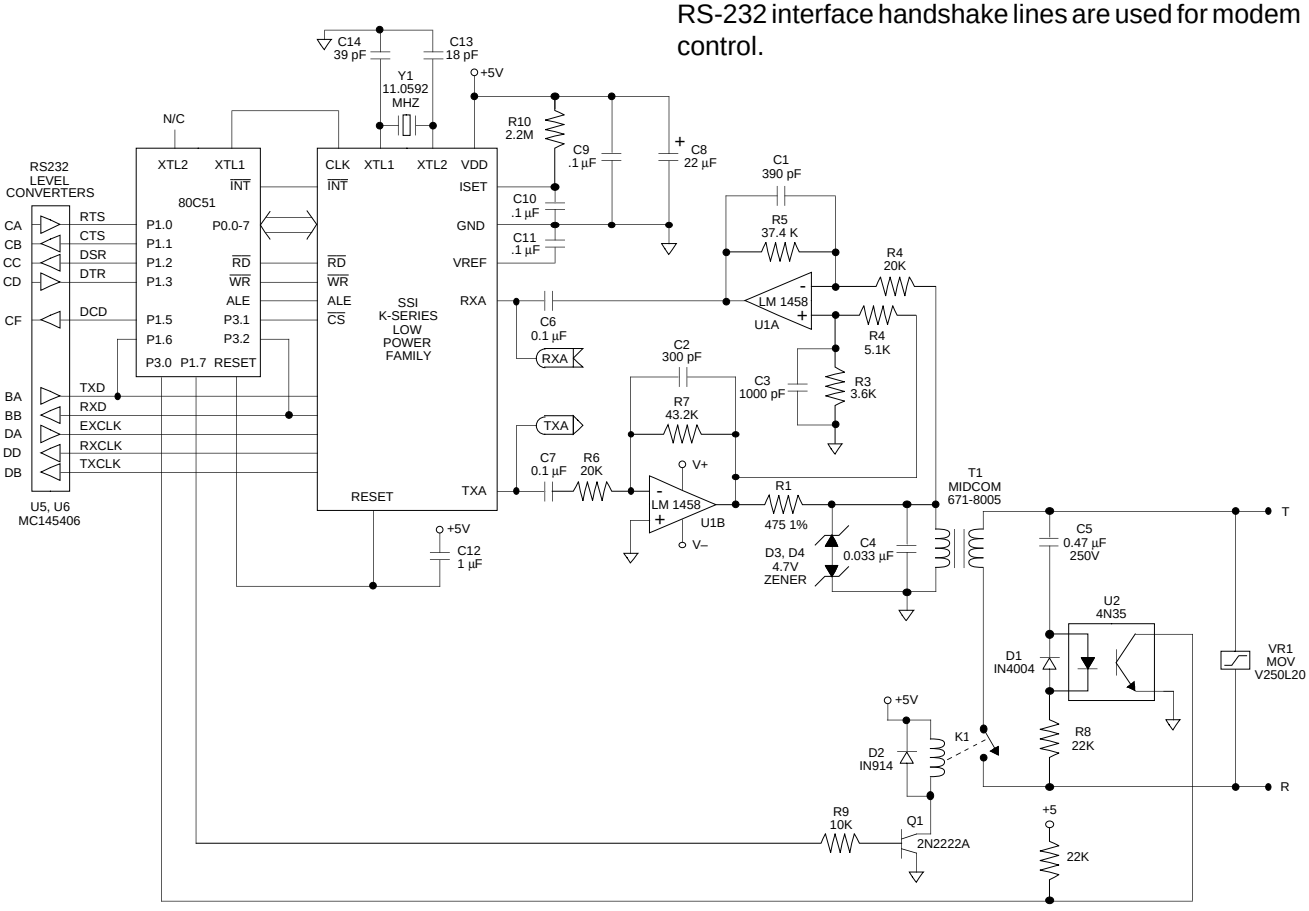


FIGURE 1: Basic Box Modem with Dual-Supply Hybrid

DIRECT ACCESS ARRANGEMENT (DAA)

The telephone line interfaces show two examples of how the "hybrid" may be implemented. The split supply design (Figure 1) is a typical two op-amp hybrid. The receive op-amp serves two purposes. It supplies gain to amplify the receive signal to the proper level for the modem's detectors and demodulator, and it removes the transmitted signal from the receive signal present at the transformer. This is done by supplying a portion of the transmitted signal to the non-inverting input of the receive op-amp at the same amplitude as the signal appearing at the transformer, making the transmit signal common mode.

The single-supply hybrid is more complex than the dual-supply version described above, but its use eliminates the need for a second power supply. This circuit (Figure 2) uses a bridged drive to allow undistorted signals to be sent with a single 5 volt supply. Because DTMF tones utilize a higher amplitude than data, these signals will clip if a single-ended drive approach is used. The bridged driver uses an extra op-amp (U1A) to invert the signal coming from the gain setting op-amp (U1B) before sending it to the other leg of the transformer. Each op-amp then supplies half the drive signal to the transformer. The receive amplifier (U1C) picks off its signal at the junction of the impedance matching resistor and the transformer. Because the bottom leg of the transformer is being driven in one direction by U1A and the resistor is driven in the opposite direction at the same time by U1B, the junction of the transformer and resistor remains relatively constant and the receive signal is unaffected.

DESIGN CONSIDERATIONS

Silicon Systems' 1-chip modem products include all basic modem functions. This makes these devices adaptable for use in a variety of applications, and as easy to control as conventional digital bus peripherals.

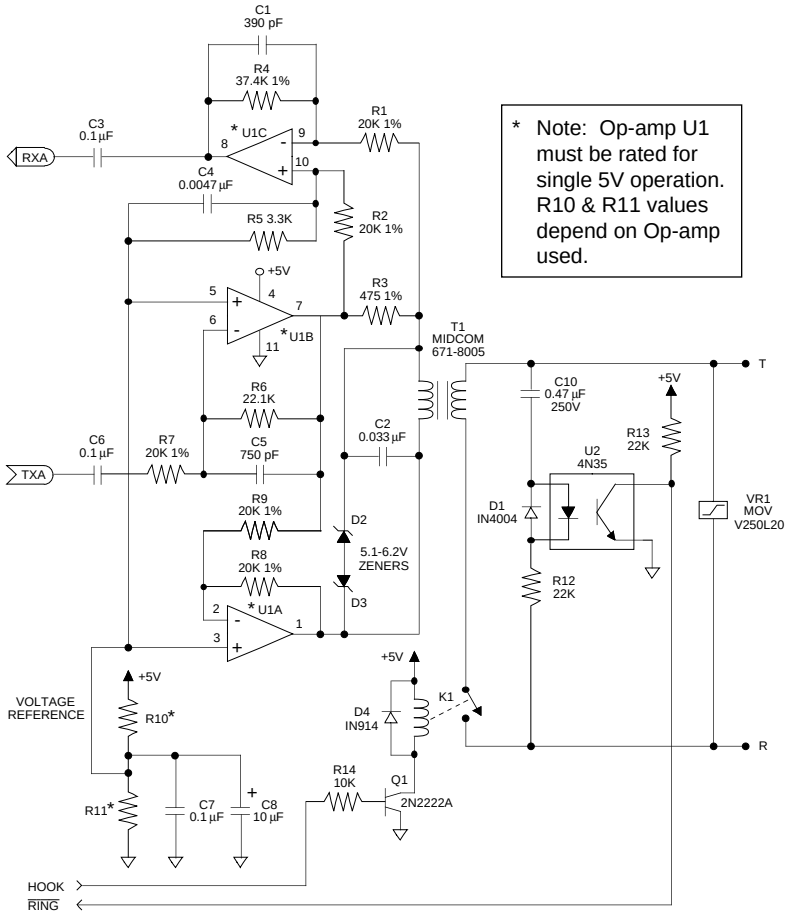


FIGURE 2: Single 5V Hybrid Version

Unlike digital logic circuitry, modem designs must properly contend with precise frequency tolerances and very low level analog signals, to ensure acceptable performance. Using good analog circuit design practices will generally result in a sound design. Following are additional recommendations which should be taken into consideration when starting new designs.

CRYSTAL OSCILLATOR

The K-Series crystal oscillator requires a parallel mode (antiresonant) crystal which operates at 11.0592 MHz. It is important that this frequency be maintained to within ±0.01% accuracy.

In order for a parallel mode crystal to operate correctly and to specification, it must have a load capacitor connected to the junction of each of the crystal and internal inverter connections, terminated to ground. The values of these capacitors depend primarily on the crystal's characteristics, and to a lesser degree on the internal inverter circuit. The values used affect the accuracy and start up characteristics of the oscillator.

LAYOUT CONSIDERATIONS

Good analog/digital design rules must be used to control system noise in order to obtain highest performance in modem designs. The more digital circuitry present on the PC board, the more this attention to noise control is needed. The modem should be treated as a high impedance analog device. A 22 µF electrolytic capacitor in parallel with a 0.22 µF ceramic capacitor between VDD and GND is recommended. Liberal use of ground planes and larger traces on power and ground are also highly favored. High speed digital circuits tend to generate a significant amount of EMI (Electro-Magnetic Interference) which must be minimized in order to meet regulatory agency limitations. To accomplish this, high speed digital devices should be locally bypassed, and the telephone line interface and K-Series device should be located close to each other near the area of the board where the phone line connection is accessed. To avoid problems, power supply and ground traces should be routed separately to the analog and digital functions on the board, and digital signals should not be routed near low level or high impedance analog traces. The analog and digital grounds should only connect at one point near the K-Series device ground pin to avoid ground loops. The K–Series modem IC's should have both high frequency and low frequency bypassing as close to the package as possible. The ISET resistor and bypass capacitor need to be as close to device as possible.

MODEM PERFORMANCE CHARACTERISTICS

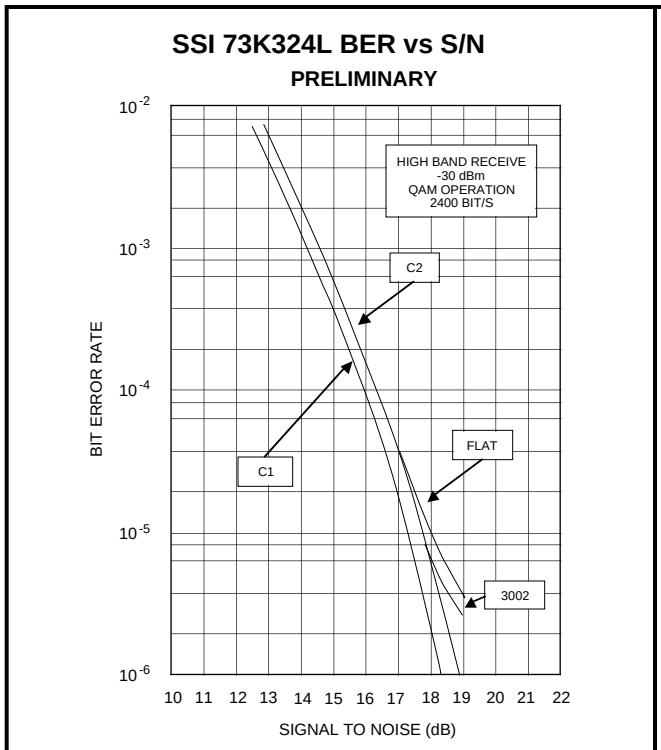
The curves presented here define modem IC performance under a variety of line conditions while inducing disturbances that are typical of those encountered during data transmission on public service telephone lines. Test data was taken using an AEA Electronics' "Autotest I" modem test set and line simulator, operating under computer control. All tests were run full-duplex, using a Hayes 2400 Smartmodem™ as the reference modem. A 511 pseudo-random-bit pattern was used for each data point. Noise was C-message weighted and all signal-to-noise (S/N) ratios reflect total power measurements similar to the CCITT V.56 measurement specification. The individual tests are defined as follows.

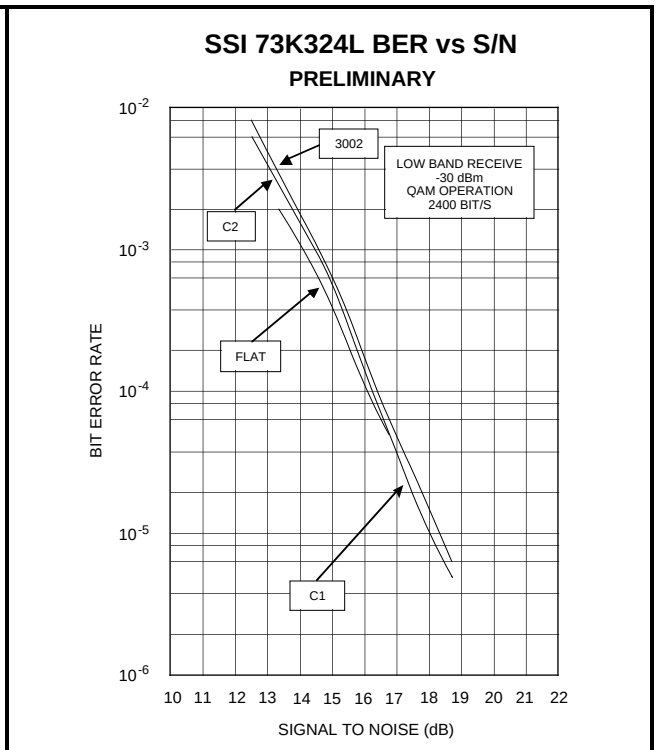
BER vs. S/N

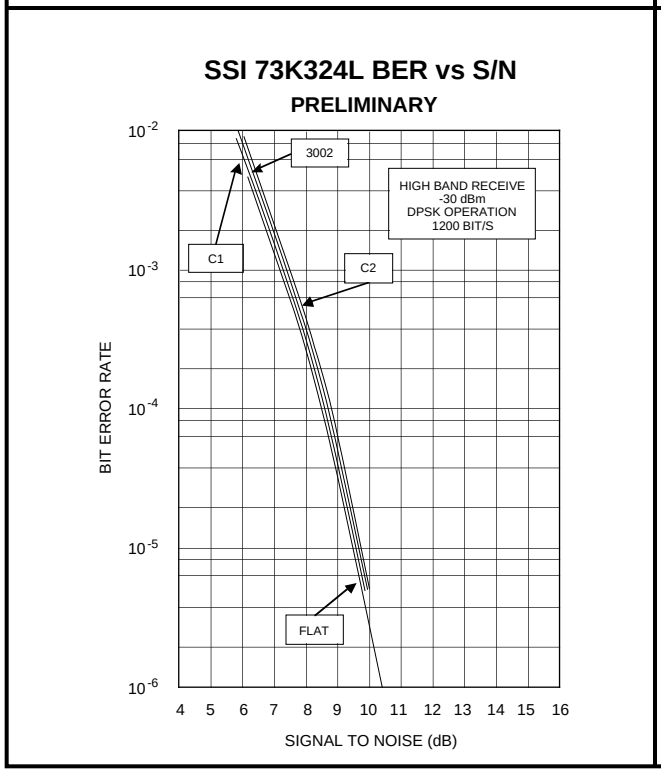
This test measures the ability of the modem to operate over noisy lines with a minimum of data-transfer errors. Since some noise is generated in the best of dial-up lines, the modem must operate with the lowest S/N ratio possible. Better modem performance is indicated by test curves that are closest to the BER axis. A narrow spread between curves representing the four line parameters indicates minimal variation in performance while operating over a range of aberrant operating conditions. Typically, a modem will exhibit better BER-performance test curves receiving in the low band than in the high band.

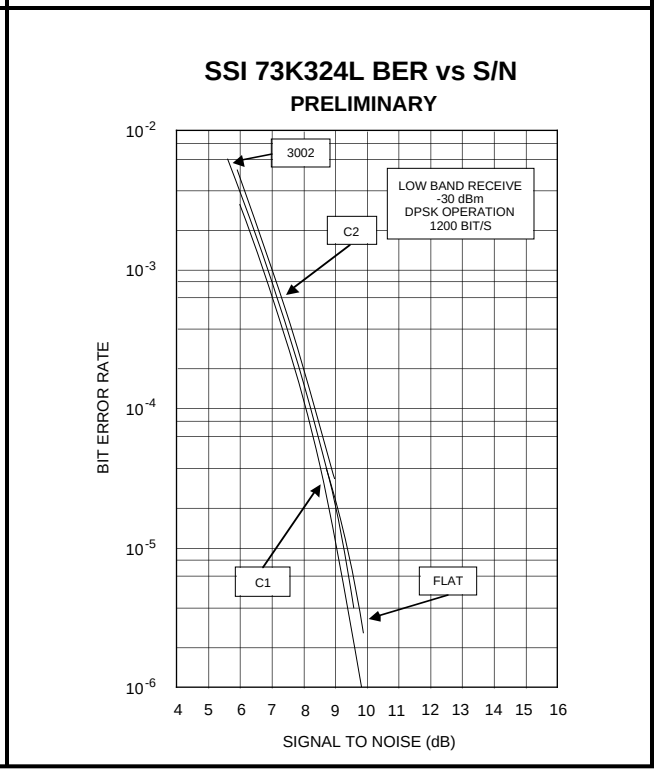
BER vs. Receive Level

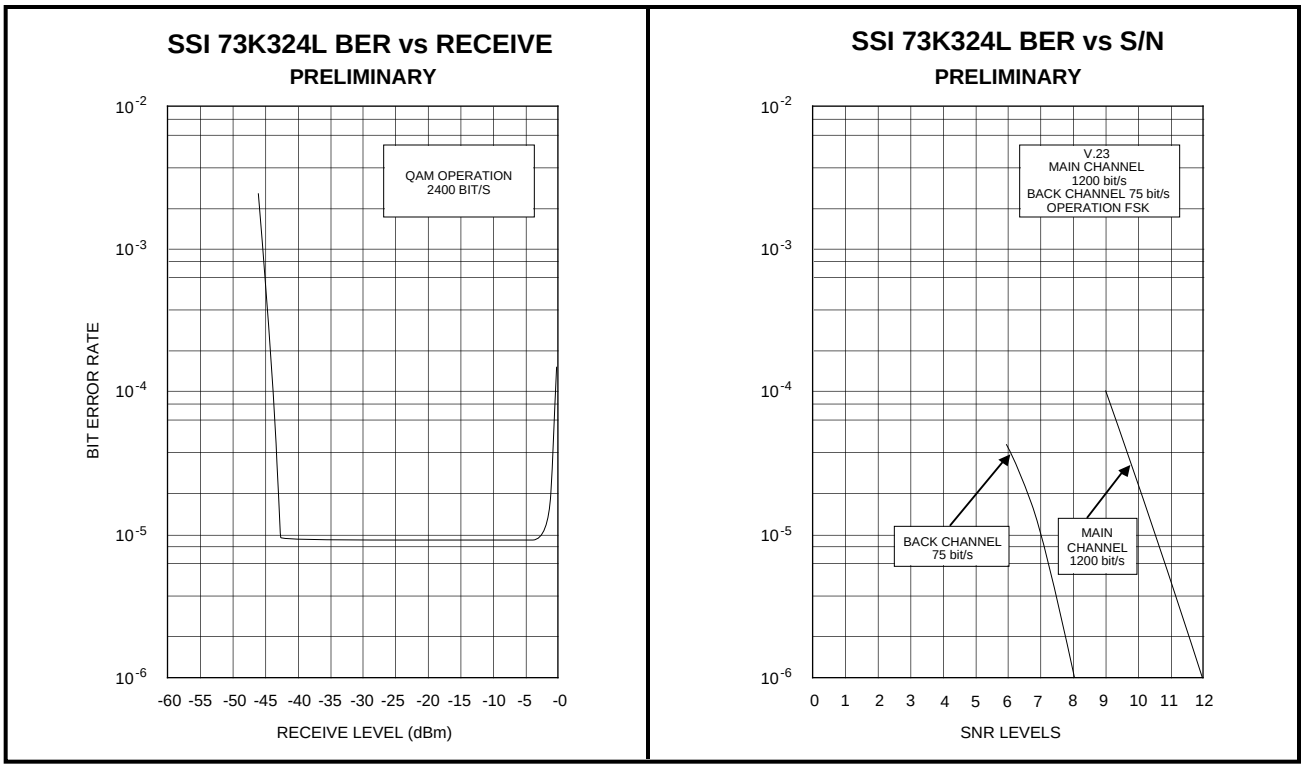
This test measures the dynamic range of the modem. Because signal levels vary widely over dial-up lines, the widest possible dynamic range is desirable. The minimum Bell specification calls for 36 dB of dynamic range. S/N ratios are held constant at the indicated values while the receive level is lowered from a very high to very low signal levels. The width of the "bowl" of these curves, taken at the BER point, is the measure of dynamic range.


SSI 73K324L BER vs S/N
PRELIMINARY
HIGH BAND RECEIVE
-30 dBm
QAM OPERATION
2400 BIT/S
C2
C1
FLAT
3002
BIT ERROR RATE
SIGNAL TO NOISE (dB)


SSI 73K324L BER vs S/N
PRELIMINARY
3002
LOW BAND RECEIVE
-30 dBm
QAM OPERATION
2400 BIT/S
C2
FLAT
C1
BIT ERROR RATE
SIGNAL TO NOISE (dB)

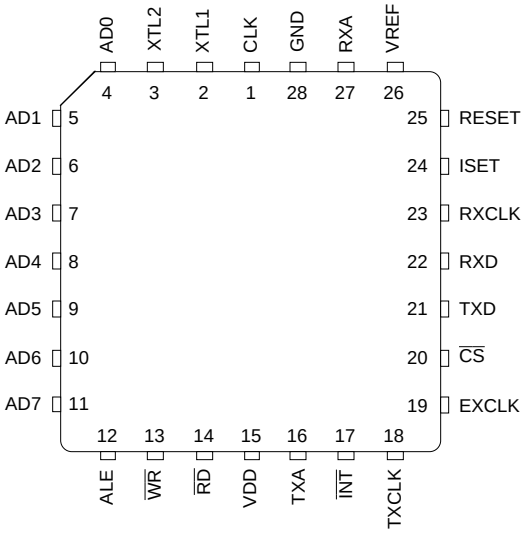

SSI 73K324L BER vs S/N
PRELIMINARY
3002
HIGH BAND RECEIVE
-30 dBm
DPSK OPERATION
1200 BIT/S
C1
C2
FLAT
BIT ERROR RATE
SIGNAL TO NOISE (dB)


SSI 73K324L BER vs S/N
PRELIMINARY
3002
LOW BAND RECEIVE
-30 dBm
DPSK OPERATION
1200 BIT/S
C2
C1
FLAT
BIT ERROR RATE
SIGNAL TO NOISE (dB)

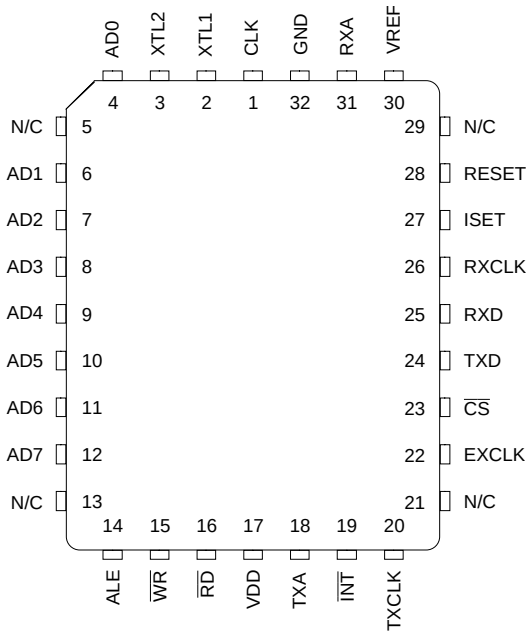

SSI 73K324L BER vs RECEIVE
PRELIMINARY
BIT ERROR RATE
10^{-2}
10^{-3}
10^{-4}
10^{-5}
10^{-6}
QAM OPERATION
2400 BIT/S
-60 -55 -50 -45 -40 -35 -30 -25 -20 -15 -10 -5 -0
RECEIVE LEVEL (dBm)
SSI 73K324L BER vs S/N
PRELIMINARY
10^{-2}
10^{-3}
10^{-4}
10^{-5}
10^{-6}
V.23
MAIN CHANNEL
1200 bit/s
BACK CHANNEL 75 bit/s
OPERATION FSK
BACK CHANNEL
75 bit/s
MAIN
CHANNEL
1200 bit/s
0 1 2 3 4 5 6 7 8 9 10 11 12
SNR LEVELS

PACKAGE PIN DESIGNATIONS

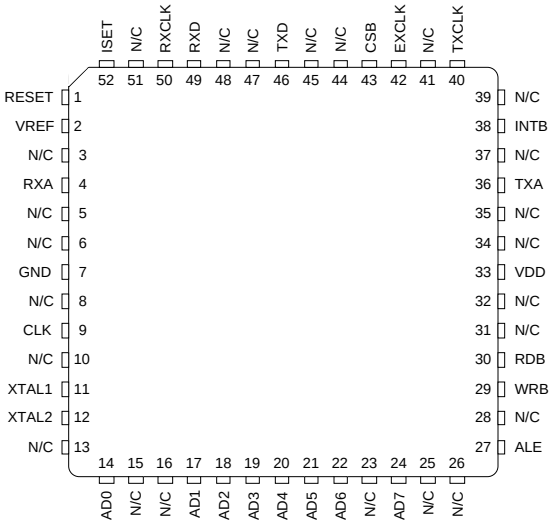
(Top View)



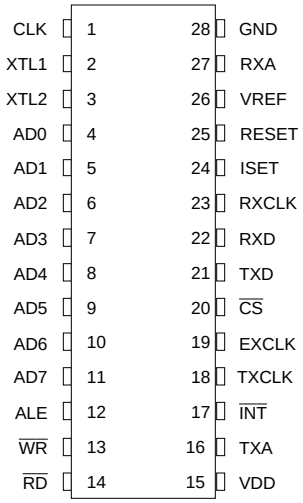
28-Pin PLCC



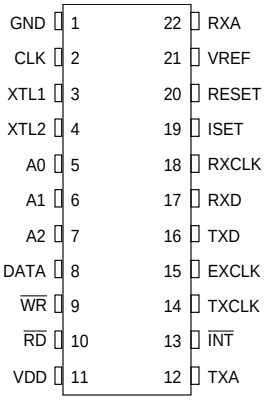
32-Pin PLCC



52-Lead QFP

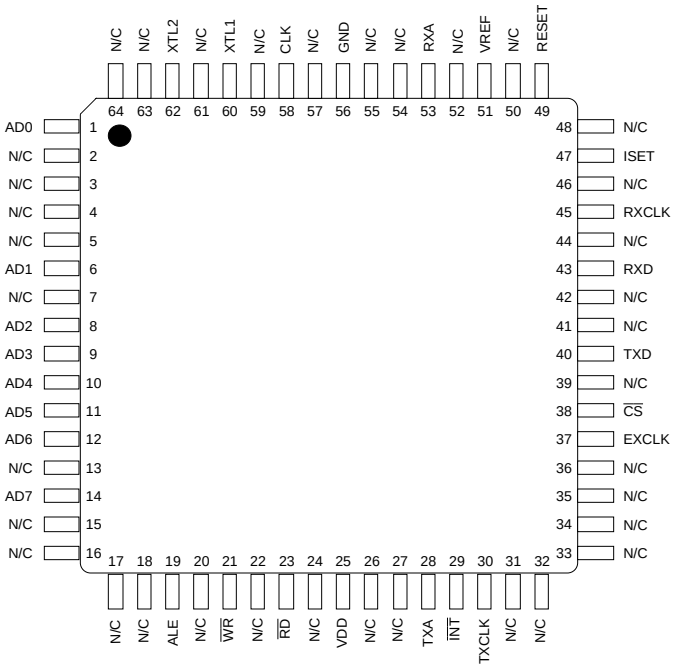


28-Pin DIP



400-Mil
22-Pin DIP

SSI 73K324L
CCITT V.22bis, V.22, V.21, V.23, Bell 212A
Single-Chip Modem



64-Lead TQFP

ORDERING INFORMATION

PART DESCRIPTION	ORDER NO.	PKG. MARK
SSI 73K324L with Serial Bus Interface		
22-Pin Plastic Dual-In-Line	73K324LS-IP	73K324LS-IP
SSI 73K324L with Parallell Bus Interface		
28-Pin Plastic Dual-In-Line	73K324L-IP	73K324L-IP
28-Pin Plastic Leaded Chip Carrier	73K324L-28IH	73K324L-28IH
32-Pin Plastic Leaded Chip Carrier	73K324L-32IH	73K324L-32IH
44-Pin Plastic Leaded Chip Carrier	73K324L-IH	73K324L-IH
52-Pin Quad Flat Pack Package	73K324L-IG	73K324L-IG
64-Lead Thin Quad Flat Pack Package	73K324L-IGT	73K324L-IGT

Preliminary Data: Indicates a product not completely released to production. The specifications are based on preliminary evaluations and are not guaranteed. Small quantities are available, and Silicon Systems should be consulted for current information.

Silicon Systems, Inc., 14351 Myford Road, Tustin, CA 92680, (714) 573-6000, FAX: (714) 573-6914

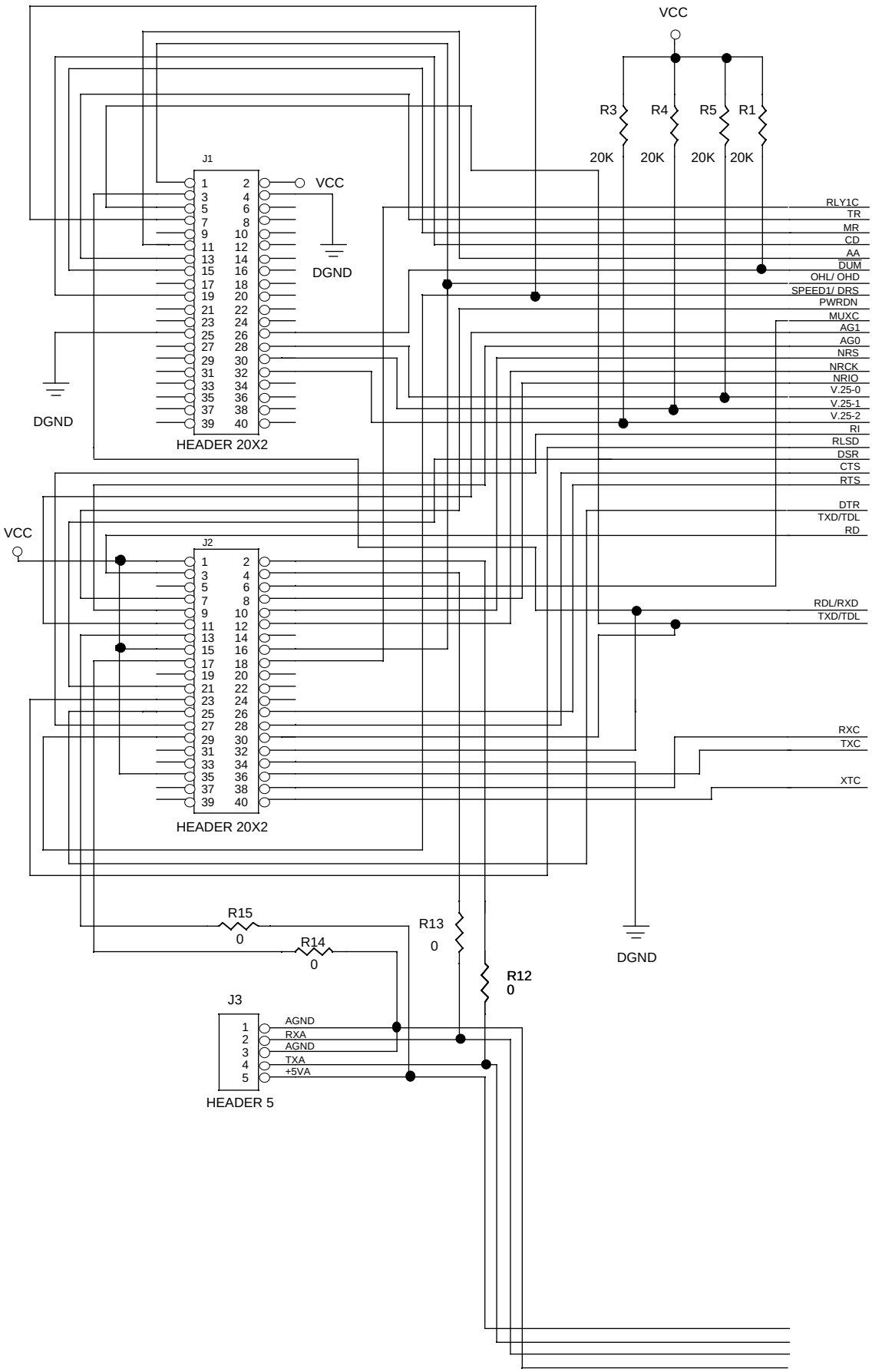


FIGURE 3-1A: SSI 73D2248 Transmit Module

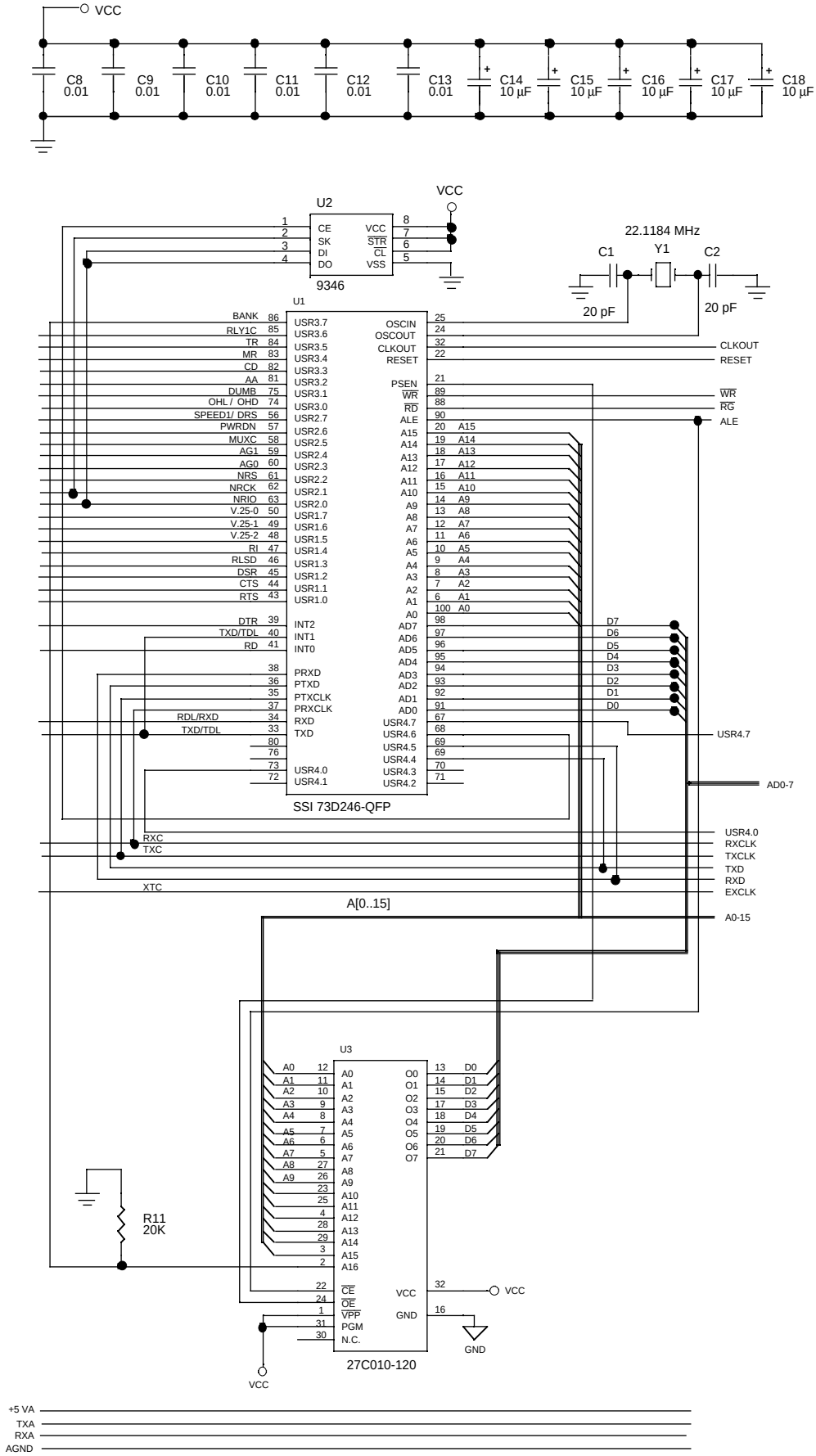


FIGURE 3-1B: SSI 73D2248 Transmit Module

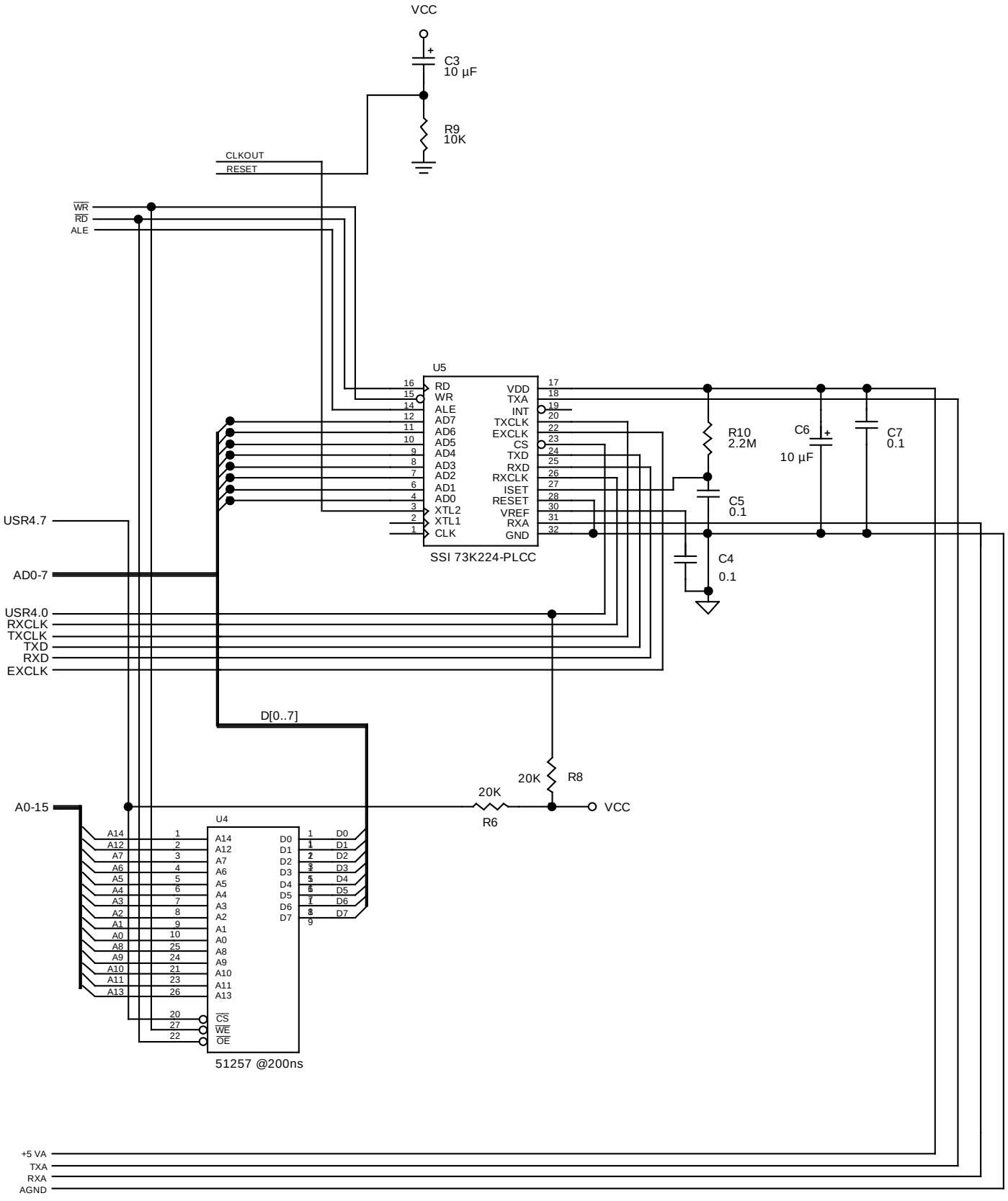


FIGURE 3-1C: SSI 73D2248 Transmit Module

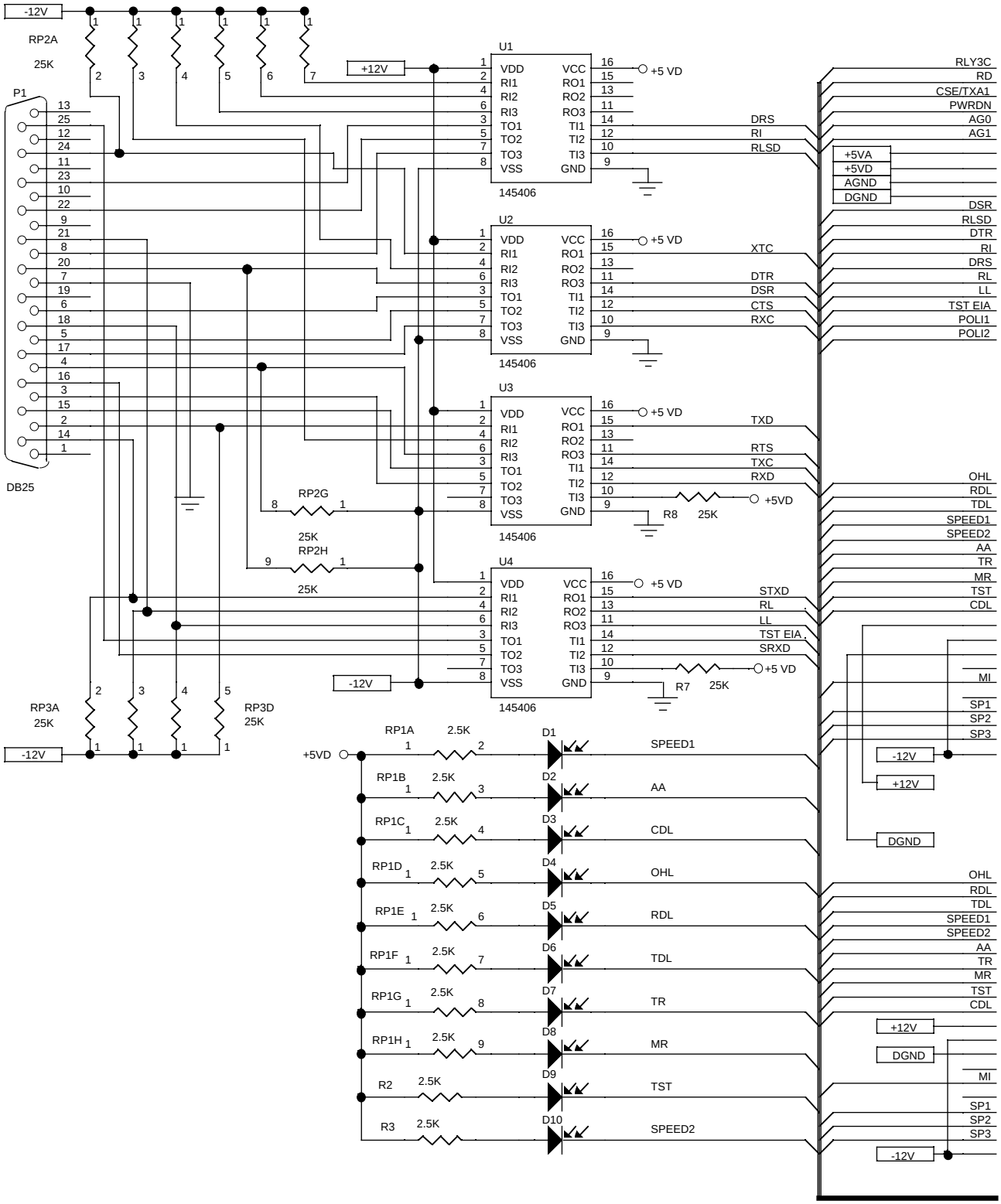


FIGURE 3-2A: Modem Motherboard

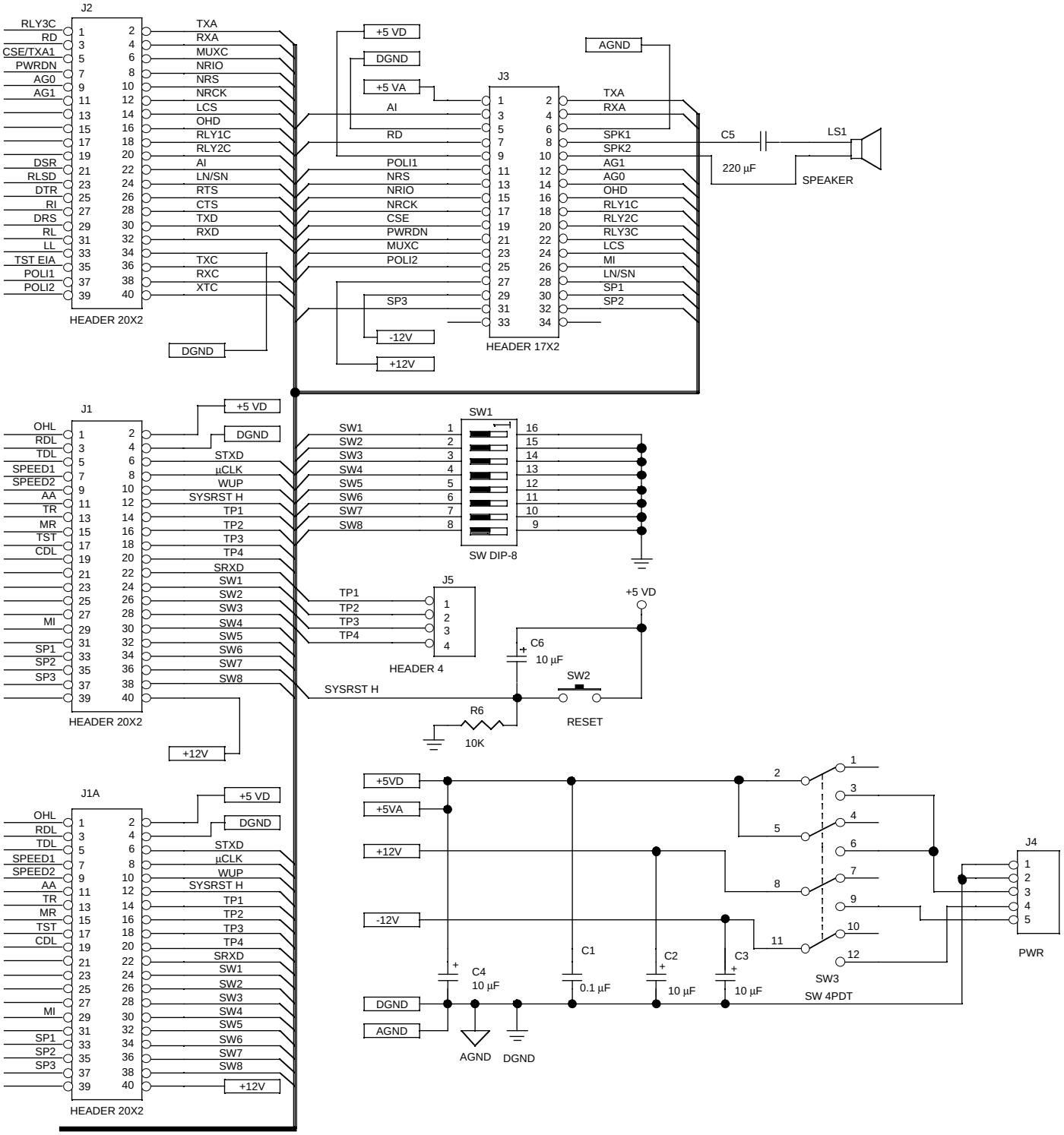


FIGURE 3-2B: Modem Motherboard

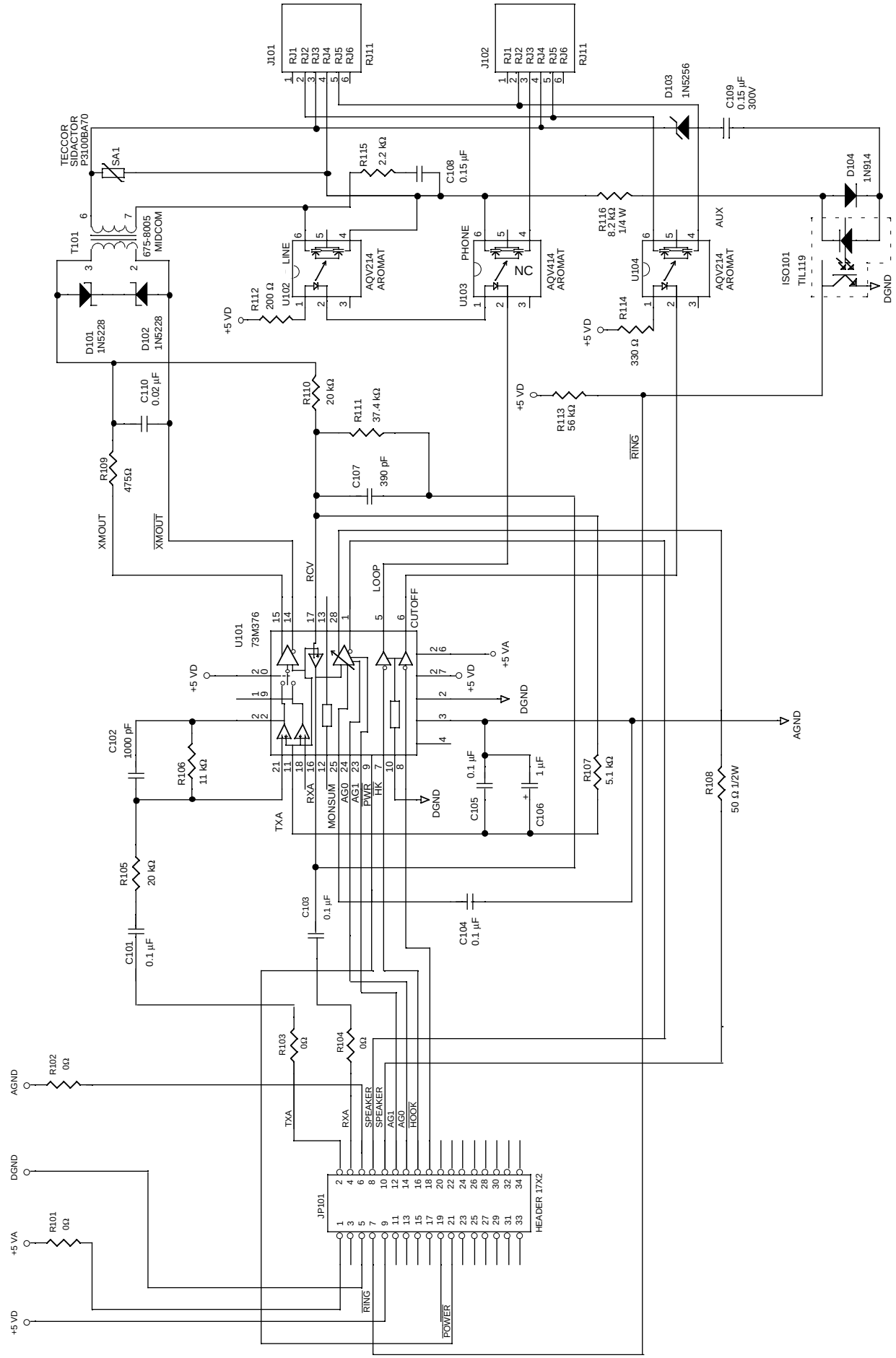


FIGURE 3-3: Telephone Interface

Section 4

SOFTWARE OVERVIEW

4 SOFTWARE OVERVIEW

4.1 MAJOR MODEM STATES

The operation of the modem firmware can be modeled as a state machine having several states. While a "state machine" per se is not implemented in this firmware, the modem does indeed have several states. The state of the modem is changed by calling the appropriate routine in SUBS.A51 (see below). Each of the states is discussed in detail below.

4.1.1 OFFLINE COMMAND A-SEARCH STATE

In offline command a-search state, the modem is "on-hook" (i.e., not connected to another modem) and looking for the letter "A" from the DTE. In this state, external interrupt 1 is enabled to measure the length of the start bit of the "A," timer 2 external interrupt is enabled to detect ringing, timer 2 is active to update the general purpose timers and the serial port is enabled.

4.1.2 OFFLINE COMMAND A-FOUND STATE

In the offline command a-found state, an "A" has been received by the modem and the rest of the command string is being placed in the buffer or a command is being processed. For this mode timer 2 is enabled so the general purpose timers will run and the serial port is enabled so that characters received by the UART can be placed in the command buffer.

4.1.3 LINE HANDSHAKE STATE

In the line handshake state, the modem has either been commanded to originate a connection or is responding to detection of a ring signal. The modem will attempt to handshake with a remote modem. In this state, timer 0 provides a 9600 interrupts / second sampling timer that is used to poll the 73K224L / 73K324L status bits. Timer 2 is enabled to update the general purpose timers and the serial port is enabled.

4.1.4 ONLINE DATA WITH AUTO SPEED BUFFERING STATE

In this state, a connection with a remote modem has been made and data from the DTE and the 73K224L / 73K324L is processed in a protocol mode. External interrupt 0 is enabled to generate an interrupt on the rising TX clock edge of the 73K224L / 74K324L. Timer 0 is configured to generate an interrupt on the rising edge of the RX clock edge. Timer 2 is enabled to update the general purpose timers and the serial port is enabled.

4.1.5 ONLINE DATA WITH CLEAR CONNECTION STATE

In this state a connection has been made with a remote modem but no protocols are in effect. The DTE is "hardwired" to the 73K224L / 324L and data passed between the two is not processed by the protocol code. In this state, timer 0 is used to generate a 9600 interrupt / second sampling timer that polls the status of the 73K224L / 324L. Timer 2 is used to update the general purpose timers and the serial port is enabled so the microprocessor firmware can look for the escape sequence.

4.1.6 ONLINE COMMAND WITH CLEAR CONNECTION A-SEARCH STATE

In this state a connection has been made with a remote modem and no protocols are in effect (clear connection). An escape sequence has been detected ("+++" or DTE transition in &D1 mode) but an "A" has not been detected by the microprocessor firmware. External interrupt 1 is enabled to measure the length of the start bit of the "A" for autobaud detection. Timer 0 is used to generate a 9600 interrupts / second sampling timer to poll the status of the 73K224L / 324L. Timer 2 is enabled to update the general purpose timers and the serial port is enabled.

4.1.7 ONLINE COMMAND MODE WITH AUTO SPEED BUFFERING A-SEARCH STATE

This state is similar to the Online Command with Clear Connection A-Search State except the modem protocol firmware is in operation. Timer 0 is used to generate RX clock interrupts and external interrupt 0 is used for TX clock interrupts.

4.1.8 ONLINE COMMAND MODE CLEAR CONNECTION A-FOUND STATE

In this state a connection has been made to a remote modem and no protocols are in use. An escape sequence has been received by the modem and an "A" has been detected. The modem will read in the rest of the command line and execute the commands. The interrupts are set up as in the Online Data with Clear Connection state. Timer 0 is used to generate a 9600 interrupt / second timer to poll the 73K224L / 324L, timer 2 is used to update the general purpose timers and the serial port is enabled.

4.1.9 ONLINE COMMAND MODE AUTO SPEED BUFFERING A-FOUND STATE

In this state a connection has been made to a remote modem and protocols are in use. An escape sequence has been detected and the modem has received an "A." The serial port has been set up for the detected rate of the "A." Timer 0 is used to generate RX clock interrupts and external interrupt 0 is used for TX clock interrupts.

4.2 INTERRUPT STRUCTURE

Processing in the modem firmware can be divided into two groups. A "main-loop" in the module main polls variables and will execute functions based on the status of these variables. (e.g., When the command buffer contains a complete command string the main loop will invoke the command line interpreter). This "polled" processing comprises the first group and is discussed in the MAIN.A51 section. The second group involves processing that occurs as part of an interrupt service routine. In this design, much of the processing occurs in response to an interrupt (e.g., an interrupt is generated every time the 73K224L / 324L receives a data bit in auto speed buffering mode). A description of the processing that occurs in the interrupt service routines is given below.

4.3 EXTERNAL INTERRUPT 0 - TXCLK

This interrupt will occur every time a bit is required by the 73K224L / 324L modem chip. Control is passed to DCE_TX_INT. If speed buffering is being performed, this code will provide a data bit to the 73K224L / 324L through the alternate data bit interface in the chip registers. Otherwise, no processing need occur in response to this interrupt. Note that the code for DCE_TX_INT is provided in object form only.

4.4 EXTERNAL INTERRUPT 1 - AUTOBAUD

External interrupt 1 is used to perform the "autobaud" function in the modem. When the modem is in command mode and the character "A" is input from the DTE, the rate of the serial connection from the DTE to the modem is determined by measuring the width of the start bit. The interrupt service routine is contained in the file INTS.A51

Timer 1 is programmed to begin counting when the TXD line is low. On the rising edge of TXD, external interrupt 1 will read timer 1 to determine the period of time TXD was low. From this measurement, a "guess" of the DTE line rate is determined and timer 1 is used to read in the next 9 bits. If the character read is an upper or lower case "A," the DTE line rate is stored in a special function register and a value corresponding to the UART rate is stored in a variable called SPEED. If the character received is determined not to be an "A," external interrupt 1 is initialized to process the next character from the DTE. The program flow of external interrupt 1 follows:

```
EXT_INT1:
    Set A_SRCH flag to indicate autobaud is taking place
    Clear TR1 to disable serial port
    Save Registers
    IF not in dumb mode
        Read Timer 1
        Estimate DTE line rate from timer 1
        Store estimate of one bit period in TIMERH and TIMERL
            Load Timer 1 with value corresponding to 1.5 bit periods
        FOR the next nine bits
                Wait for Timer 1 to expire
                Read in bit from DTE and build character in ACC
            If "wrong" bit, clean up and exit
            Reload timer 1 with one bit period
        ENDFOR
        Update SPEED variable and special function register 23
        Set up the UART
    ENDIF
    Clear A_SRCH flag
    Return from interrupt
```

4.5 TIMER 0 - RXCLK & 9600 SAMPLING

The timer 0 interrupt is used in two different modes depending on the state of the modem. During handshaking or during a "clear" connection, timer 0 generates an interrupt at a 9600/second rate that is used to trigger monitoring of the 73K224L/324L IC. If a connection has been made and a protocol is running (i.e., V.42, MNP, or autospeed buffering), timer 0 is set up to generate interrupts coincident with received bits from the 73K224L/73K324L IC. This interrupt signals the protocol code that a bit is ready at the receiver.

4.6 T2EX - RING DETECT

In the controller, one interrupt vector is provided for both an edge detected on the T2EX pin and for timer 2 events. The source of the interrupt can be determined by reading the status of T2CON register in the microprocessor. In the 73D2248, this interrupt vector is used for ringing detection and general purpose timer updating. A description of how ring detection is performed follows. Discussion of the general purpose timers is in the next section.

```
TIMERS:
    IF NOT in command mode or if autobauding
        return from interrupt
    ENDIF
    IF TIMER 2 overflow
        JUMP to timer service  (See Timer 2 Section)
    ELSE
        IF NOT external interrupt
            return from interrupt
        ELSE IF online or command mode or pulse dial or offhook
            return from interrupt
        ELSE
            Increment variable RING_QUAL
            Initialize variable RING_TIMER = 10
            Set flag RING_FLAG
            Return from interrupt
        ENDIF
    ENDIF
```

4.7 TIMER 2 - GENERAL PURPOSE TIMER

The general purpose timers interrupt service routine runs at a 1 ms interrupt rate. The interrupt vector is shared with the T2EX pin used for ring detection and the software is responsible for determining if the interrupt is due to a ringing signal or the 1 ms timer expiration (see the T2EX section above). Program flow for the general purpose timers is given below:

```
GPT:
    Clear the timer 2 flag
    Preserve Registers
    Reload Timer 2 to interrupt again in 1 ms
    Update DELAY_VAL timer
    Update TMR_1MS_1 timer
    Update DTR_TMR
    Update TMR_1MS_CNTR
    IF TMR_1MS_CNTR == 0                ;At 10 ms interval
        Reload TMR_1MS_CNTR
        Update TMR_10MS_1
        Update TMR_10MS_2
        CALL DTE_TIMER  (for V42 support)
        CALL LINE_TIMER (for V42 support)
        Read TMR_10MS_CNTR
        IF even
            Update TMR_20MS_1
        ENDIF
        Update TMR_10MS_CNTR
        IF TMR_10MS_CNTR == 0           ;At 100 ms interval
            Update TIMER_TICK2
            Update TIMER_TICK
            Update LAPM_TIMER_TICK
```

```
            Update TMR_100MS_1
            Update TMR_100MS_2
            Update TMR_100MS_3
            IF RING_FLAG == TRUE
                Turn on RI indicator
                IF RING_TIMER == 0
                    IF RING_QAUL >= 21
                        Turn off RI indicator
                        Reset RING_QUAL
                        Clear RING_FLAG
                    ENDIF
                ELSE
                    Update RING_TIMER
                ENDIF
            ENDIF
            Update TMR_100MS_CNTR
            IF TMR_100MS_CNTR == 0          ;At 1 Second interval
                Update TMR_1SEC_1
                Update TMR_1SEC_2
                Update TMR_S1
            ENDIF
        ENDIF
    ENDIF
    Restore registers
    Return from interrupt
```

4.8 SERIAL PORT

The serial port interrupt is generated whenever a character is received from the DTE or after a character has been transmitted to the DTE and the transmit buffer is empty. The interrupt service code is located in file (INTS.A51) starting at label ES_INT. The program flow of the interrupt service routine is diagramed below:

```
ES_INT:
    IF transmit interrupt
        IF sending result code
            Send next result code character
            Update pointers
        ELSE IF online & NOT clear connection
            CALL DTE_TX_INT             ;Entry into V.42bis code
            Reset Interrupt
        ELSE
            Reset interrupt
        ELSE IF receive interrupt
            IF NOT Command mode
                IF NOT clear connection
                    CALL DTE_RX_INT     ;Entry into V.42bis code
                    Reset Interrupt
                ELSE
                    Do escape sequence processing
                    Reset Interrupt
                ENDIF
            ELSE                        (CLI_RX:)
                Stuff character into command buffer
                ENDIF
        ENDIF
```

DTE_RX_INT and DTE_TX_INT handle online character processing if the modem is in V.42, MNP or speed buffering mode. Note the “clear connection” means the modem is not in any of the above modes.

4.9 V.42BIS REQUIREMENTS

The code required to implement V.42, V.42bis, MNP and autospeed buffering is provided in object code form only. It should be linked with the rest of the source modules using the provided batch files described in the “Assembling and Linking the Source Code” section. In order for the protocol code to operate properly, calls must be made to entry

points in the protocol code, and entry points for performing housekeeping must exist in the source for the protocol code to call. An overview of the requirements is given below.

The setup of the modem for V.42, V.42bis, MNP and autospeed buffering takes place in the function SETV42, located in DEVICE.INT. This function will send the appropriate setup information to the protocol code based on the setting of certain S registers. Four functions are used to pass data to and from the modem and the protocol code: DTE_TX_INT, DTE_RX_INT, DCE_TX_INT and DCE_RX_INT. DTE_RX_INT is called when a byte has been received from the terminal and is to be transmitted to the remote modem. DTE_TX_INT is called when a byte of data has been processed by the protocol code and is ready to be sent to the terminal. DCE_TX_INT is called every time a symbol is required to be sent to the remote modem. DCE_RX_INT is called every time a symbol has been received from the remote modem.

4.10 SOURCE CODE OVERVIEW

Nine modules are provided in source code form for implementing and customizing the modem firmware. The nine modules are MAIN.A51, CLI.A51, CLI2.A51, CLI_INT.A51, DEV1.A51, DEV2.A51, DEV_INT.A51, EEPROM.A51, INTS.A51, SUBS.A51, and MACROS.A51.

MAIN contains the main foreground loop for the modem. It polls various flags to determine if a change in modem state has occurred.

CL1 & CLI2 is the command line interface. All the code required to parse and perform the “AT” commands is contained in this module.

CLI_INT contains code to process interrupts from the microprocessor UART.

DEV1 & DEV2 has the code specific to controlling the 73K224L / 324L modem IC. Functions are provided to allow the chip to be set up in various states as well as code to support handshaking.

DEV_INT contains interrupt code required to support the 73K224L / 324L. This code is primarily used to monitor the state of the modem chip during handshaking.

EEPROM contains the code to read and write configuration data from the non-volatile EEPROM. Modem configuration data can be written to the EEPROM so the configuration is saved when power is turned off.

INTS contains interrupt code for many of the hardware interrupts. Code for escape code detection, ring detection and general purpose time-keeping is contained in this module.

SUBS contains general purpose subroutines used by the other modules.

MACROS contains some assembly language macros for accessing external memory on a bit-wide and byte-wide basis.

HDLCRX device driver for the HDLC packetizer.

A detailed description of the functions contained in each of these modules follows.

4.10.1 MAIN.A51

MAIN contains the primary foreground loop for the controller. The microprocessor reset vector will also jump to initialization code located in this module.

On power-on initialization, code sets the controller ports, clears internal and external RAM and initializes the stack pointer. Various functions are called to perform initialization in the other firmware modules. Special function registers are updated with values read from the EEPROM if present. The HS LED is updated and the RLSD line is set according to values in the special function registers. Control is then passed to the main foreground loop at label MAIN.

MAIN also contains code that optionally supports program memory bank switching. By using this feature, it is possible to for the executable code to exceed 64K in size. The bank switching is implemented by using the USER3.7 line of the microprocessor to select either the lower or upper bank of a 128K byte EPROM. The SYS_RESET startup vector must be contained in both the lower and upper bank at the same address (relative to the start of the 64K boundry). The vector will set up the microprocessor to address the lower bank by setting USER3.7 low. This is required because there is no way to guarantee the state of the USER3.7 line at power up.

Two additional routines and a jump table need to reside at identical locations in the upper and lower banks. The jump table contains addresses of the routines in the upper bank to be called by the lower bank. CONTEXT_SWITCH is called with the index to the jump table in the accumulator. The return address of the caller is stored in memory and control is passed from the lower bank to the desired routine in the upper bank. When the upper bank routine is ready to return control to the caller, a jump is made to the label CONTEXT_RETURN. The return address of the last call to CONTEXT_SWITCH is read and program control is returned there.

A description of CONTEXT_SWITCH and CONTEXT_RETURN follows:

CONTEXT_SWITCH(index:[Acc])

This function is used to call a routine in the upper memory bank from the lower memory bank. Index is the number of the routine in the table CONTEXT_JUMP_TABLE. The return address in pulled off the stack and stored in memory (see CONTEXT_RETURN below). Note that the contents of the accumulator and the data pointer are destroyed by this operation.

CONTEXT_RETURN( )

This function is used to return control from the upper memory bank to the lower memory bank. When a jump is made to this label, the return address of the last call to CONTEXT_SWITCH is read from memory and pushed on the stack and a return is executed. Note that the contents of the accumulator and the data pointer are destroyed by this operation.

The current implementation allows code from the lower bank to call code in the upper bank but not vice-versa.

The MAIN foreground loop polls variables and updates the modem hardware on a round robin basis. It will also drive a state machine when handshaking is being performed. If the modem is in Offline Command mode it will go into a Power IDLE state and wait for either a Serial port interrupt or a Ring Detect interrupt. The structure of the MAIN loop is outlined below:

```
MAIN:
    Call Update                 ;Update the RS232 lines and LEDs
    Call Monitor                ;Check for auto-answer, check self-test
                                ;timers, check DTR line, check long-space
                                ;disconnect, send result codes
    If Command Mode
        If Command Pending
            CALL CLI            ;Process command string
        Else if NOT connected
            If Power Idle timer = 0
                turn off timer 2
                set power Idle bit in PCON
                Wait here for next interrupt
                    ***
                    ***
                INTERUPT...
                Reset power Idle Timer
                Jump to MAIN
            ENDIF
        ENDIF
    Else if cnctfl = 1          ;If modem is connected
        CALL NEXT_STATE         ;Go do connected loop
    ENDIF
    JUMP MAIN                   ;Loop Forever
```

4.10.2 CLI1.A51 & CLI2.A51

This file contains the “Command Line Interpreter” used to parse “AT” commands, code to implement the AT commands and initialization code used to set up the S-registers.

Initialization of the special function registers takes place in routine CLI_INIT. SFR_TABLE contains offsets into external memory for the special function registers 0 through 99. Some values are not used, however, and the offset for these registers is set to 0FF hex. The initialization routine reads the offset for the SFRs and, if not 0FF hex, the corresponding value from the SFR_VALUE table is read and then written to the SFR in external memory.

When the command buffer is full, control is passed to this module at label CLI. Starting at the beginning of the command buffer, each command character is read and control is passed via a jump table (VALID_TABLE) to the routine responsible for executing the command. These routines are responsible for reading and range checking any parameters, executing the command and updating the command buffer pointer (CLI_INDEX) to the next command in the command buffer. If an error is detected in the command string the current command and all subsequent commands in the buffer are aborted.

The basic structure of the ATB command appears below. Note from jump table VALID_TABLE that execution of this command begins at label CMD_B.

```
CMD_B:
    If DIAL_CMD flag is set          ;B is part of dialing string
        Register R0 = #14            ;code for dtmf "B"
        Jump dial_num
    Else if AMPER_CMD flag set       ;Actually an AT&Bx command
        Clear AMPER_CMD flag         ;Reset flag
        Jump CLI_ERROR               ;AT&B is not a valid command
    Else                             ;ATBx command
        TEMP_REG = 0                 ;Default value
        Call GET_NUM                 ;Read parameter (if any)
    If TEMP_REG
        Clear ccittb bit in S27      ;V.22 mode at 1200 bit/s
        Jump CLI_END                 ;Now process next command
    Else if TEMP_REG = 1
        Set ccittb bit in S27        ;212A mode at 1200 bit/s
        Jump CLI_END                 ;Now process next command (if any)
    Else
        Jump to CLI_ERROR            ;invalid parameter
```

The basic structure given above is common to many of the AT commands implemented. When control is passed to the command routine two flags are checked to determine how to handle the command, DIAL_CMD and AMPER_CMD. If DIAL_CMD is set, the command is part of a dialing string. In the example above, this would be the case if "ATDB" was typed at the DTE. The routine dials the DTMF digit "B" by jumping to DIAL_NUM. The AMPER_CMD flag indicates that the command was preceded by an ampersand (&). This would be true if "AT&B" was typed at the DTE. The AT&B command is not valid for the 73D2248 firmware so control is passed to command error handling code (CLI_ERROR).

A brief description of some of the routines used to implement the AT command line interpreter follows. For examples of how to use these routines, study CLI.A51.

CLI_END(CLI_RESULT:[var])

This routine is the "normal" exit point for most of the AT command routines. It checks CLI_RESULT to see if it is zero. If it is, control is passed to CLI_LOOP and the next command in the buffer is processed. If CLI_RESULT is non-zero the command line interpreter is reinitialized to process the next command string entered into the command buffer from the DTE.

CLI_ERROR( )

Set up the result code to be ERROR. The processing of any commands remaining in the command buffer is aborted. The command line interpreter is reinitialized to process the next command string entered into the command buffer from the DTE.

CMD_BIT(default:[c]) Returns (0 or 1:[c])

Reads the next character in the command buffer. If the character read is a letter (e.g., the next command) the default value passed in the carry bit is returned. If the character is a "1," the carry bit is set and CLI_INDEX is advanced. If the character read is a "0," the carry bit is cleared and CLI_INDEX is advanced. Otherwise, CLI_RESULT is set to ERROR and the passed value in the carry bit is returned.

DIAL_NUM(digit:[r0])

Dials the digit passed in R0. Checks to see if pulse or tone dialing is enabled. If R0 contains an invalid value, the command line interpreter is reinitialized to process the next command string entered into the command buffer from the DTE.

GET_NUM(default:[TEMP_REG]) Returns (number:[TEMP_REG])

The next digit(s) in command buffer is read. GET_NUM will continue to read characters out of the command buffer until a non-numeric character is read. The value of the ASCII digits read will be returned in variable TEMP_REG. If no numeric digits are read, the TEMP_REG value passed will be returned. The pointer to the next character in the command buffer (CLI_INDEX) will be advanced to point to the next command in the buffer.

SEND_RESULT (result code:[cli_result])

Returns (pointer:[result_ptrl,result_ptrh)

This routine determines if verbose or numeric result code mode is selected and if result codes are enabled. It then initializes variables RESULT_PTRL and RESULT_PTRH to point to the desired result code string. A transmit interrupt is generated to "prime" the serial port to output the result code.

4.10.3 CLI_INT.A51

Routines to process interrupts due to serial interface connected to the DTE are handled in this module.

4.10.4 DEV1.A51 & DEV2.A51

This module contains code specific to controlling the 73K224L / 73K324L modem IC as well as the code to perform "on-line" functions. Rather than writing to the 73K224L / 73K324L registers directly, calls to the routines in DEVICE should be made to maintain a consistent interface between this device driver and the rest of the modem. In general, whenever a write to the 73K224L / 73K324L occurs, shadow bits are also updated. The correct status of these shadow bits can be assured by using the functions provided in this module. Some of the routines in this module operate during a connection when a protocol (e.g., V.42bis) is running. Because of the limited time available to perform processing when a protocol is running, extreme care must be taken when modifying these routines. The bulk of the code in this module can be described by defining a few "Entry Points."

Two functions are provided to read or write a single bit from the modem IC; GET_RXBIT and PUT_TXBIT. When speed buffering is being performed (e.g., when V.42 is enabled) the protocol code uses these entry points to read and write data to and from the 73K224L / 73K324L.

INIT_MODEM performs the initialization of the modem IC. It is called from main whenever a reset is done.

CONNECT is the entry point to perform a handshake. It is called from the main loop when the modem is not in command mode and is not connected. The type of handshake performed is determined from the the state of the special function registers. The function will perform call progress monitoring (if appropriate) and invoke the handshake state machine.

A brief description of some of the functions available in this module follows:

GET_RXBIT( ) Returns received_bit:[C]

This entry point is used by the protocol code to read a single bit received over the remote modem. In addition to reading the data bit, data patterns are monitored and the signal quality bit is updated. Note that in 11 MHz mode, only the carrier bit is monitored as there is insufficient time to do additional processing. The bit read is returned in the carry flag.

PUT_TXBIT(transmitted_bit:[C])

This entry point is also used by the protocol code to write a single bit to the 73K224L / 73K324L alternate transmit bit. The bit to be written is passed in the carry flag.

CONNECT( )

This is the primary entry point to command the modem to attempt a handshake. The code will determine the desired mode of operation from the setting of the special function registers, initialize the 73K224L / 73K324L appropriately, do call progress detection (if in originate mode) and finally enter the handshake state machine. Any request to attempt a handshake should be made through this entry point. The "online loop" is also located in the state machine (state 16). The microprocessor will continuously loop through this code as long as it is connected and in data mode.

INIT_MODEM( )

This routine performs the power-on initialization of the 73K224L / 73K324L.

CALL_PROGRESS(timeout:[S7]) Returns status:[acc]

Looks for a busy or carrier signal on the line. Called after dialing is complete. This function will return one of the following values in the accumulator.

0FF (hex)	S7 timeout or keypress abort
01	Busy
02	Carrier

GET_DIALTONE(qualify:[Acc],window:[B]) Returns status:[Acc, C]

Looks for a valid dialtone for a specified period of time in B (tenths of seconds). The dialtone must be present for specified time passed in Acc (tenths of seconds). The accumulator and carry bit will return status as follows:

Acc	0	Dialtone detected
Acc	0FFH	Timeout
C = 1		Keypress Abort

WAIT_DIALTONE(window:[S7]) Returns status:[Acc}

Looks for dialtone or busy for the time specified in the S7 special function register. Status will be returned in the accumulator as follows:

00 (hex)	Successful
01	Busy
0FFH	Timeout
C = 1	Keypress Abort

WAIT_SILENCE(timeout:[S7]) Returns status:[Acc,C]

Looks for a silent period of duration of 5 seconds for the time specified in the S7 register. Status is returned in the accumulator as follows:

00 (hex)	Success
01	Busy
0FFH	Timeout
C = 1	Keypress Abort

SETSYNC( )

Sets up the 73K224L / 73K324L for internal synchronous mode of operation.

SETASYNC( )

Sets up the 73K224L / 73K324L for 10 bit asynchronous mode of operation.

RESET_V42( )

Set V.42 code back to idle state.

SETV42( )

Sets up the 73K224L / 73K324L for a V.42 connection. Sets up the special function registers related to V.42. Should be called after a connection is established prior to sending a result code.

WRTKCR0( )

Writes the contents of variable CR0 to control register CR0 of the 73K224L / 73K324L.

WRTCKR1( )

Writes the contents of variable CR1 to control register CR1 of the 73K224L / 73K324L.

WRTCKR2( )

Writes the contents of variable CR2 to control register CR2 of the 73K224L / 73K324L.

WRTCKR3( )
Writes the contents of variable CR3 to control register CR3 of the 73K224L / 73K324L.

SET_RDLB( )
Places chip into remote digital loopback mode.

CLEAR_RDLB( )
Puts 73K224L / 73K324L back into normal mode.

RUN( )
CCITT V.22bis handshake entry point.

RUN12( )
Bell 212A and CCITT V.22 handshake entry point.

RUN6( )
CCITT V.22 half speed 600 bit / s entry point.

RUN3( )
Bell 103 or CCITT V.21 handshake entry point.

ONL_RET( )
Return from the command state to the online state.

GO_CONNECT( )
Entry into the handshake state machine. This code should not be called directly but accessed through one of the RUNX( ) functions outlined above.

HANG_UP( )
Tests to see if the modem is connected and if so forces the state machine to state 40 (see state machine description below).

RETRAIN( )
Forces the state machine to attempt a retrain request by going to state 36 (see state machine description below).

LOSS_CAR( )
Toggles the hang up on loss of carrier bit.

SET_16( )
Sets up the 73K224L / 73K324L receiver for 16-way decisions and updates the shadow bits.

SET_4( )
Sets up the 73K224L / 73K324L receiver for 4-way decisions and updates the shadow bits.

ATTN(gain:[Acc])
Adjusts the transmit gain of the 73K224L / 73K324L to the level specified in the least significant four bits of the accumulator.

ENDTMF( )
Enables the 73K224L / 73K324L to transmit DTMF tones.

DIDTMF( )
Disables the transmission of DTMF tones in the 73K224L / 73K324L.

SP24( )
Sets up the 73K224L / 73K324L for 2400 bit / s operation. Normally invoked from state machine.

SP12( )
Sets up the 73K224L / 73K324L for 1200 bit / s operation. Normally invoked from state machine.

SP6( )
Sets up the 73K224L / 73K324L for 600 bit / s operation. Normally invoked from state machine.

SP3( )
Sets up the 73K224L / 73K324L for 300 bit / s operation. V.21 or BELL 103 is not selected by this command. Normally invoked from state machine.

XMTMODE( )
Selects the synchronous or asynchronous mode of the 73K224L / 73K324L as follows:

0 Power Down

1 Internal Synchronous Mode

2 External Synchronous Mode

3 Slave Synchronous Mode

4 8 Bit Asynchronous Mode

5 9 Bit Asynchronous Mode

6 10 Bit Asynchronous Mode

7 11 Bit Asynchronous Mode

For a description of the above modes, see the hardware section on the 73K224L / 73K324L modem IC.

RL_XT( )
Squelches the transmitter for 77 milliseconds. Used to cancel a remote digital loopback.

MOOR( )
Sets up the 73K224L / 73K324L for originate mode.

MOAN( )
Sets up the 73K224L / 73K324L for answer mode.

MODR( )
Reset the 73K224L / 73K324L digital signal processor.

MOMR( )
Reset the 73K224L / 73K324L modem IC.

MODG( )
Enable the 73K224L / 73K324L modem IC.

MOED( )
Reset the equalizer.

MOEE( )
Enable the equalizer.

MOTI( )
Inhibit equalizer training.

MOTR( )
Allow equalizer training.

TRICLOCK( )
Tristate the TXCLK and RXCLK pins of the 73K224L / 73K324L.

ENCLOCK( )
Enables the TXCLK and RXCLK pins of the 73K224L / 73K324L.

GDDI( )
Disables guard tone transmission in the 73K224L / 73K324L.

GD55( )
Sets up the 73K224L / 73K324L for transmission of 550 Hz guard tone.

GD1800( )
Sets up the 73K224L / 73K324L for transmission of 1800 Hz guard tone.

GDEN( )
Enables transmission of guard tones by the 73K224L / 73K324L.

ANDI( )
Disables transmission of answer tone by the 73K224L / 73K324L.

AN21( )
Sets up the 73K224L / 73K324L for transmission of a 2100 Hz answer tone.

AN22( )
Sets up the 73K224L / 73K324L for transmission of a 2225 Hz answer tone.

ANEN( )
Enables transmission of the answer tones.

XMDI( )
Squelches the transmitter of the 73K224L / 73K324L.

XMEN( )
Enables the transmitter of the 73K224L / 73K324L.

XMMA( )
Sets up the 73K224L / 73K324L to transmit a marking pattern.

XMDA( )
Sets up the 73K224L / 73K324L for transmission of data.

XMDO( )
Sets up the 73K224L / 73K324L to transmit a dotting pattern.

XMS1( )
Sets up the 73K224L / 73K324L to transmit a double dotting (S1) pattern.

XMSP( )
Sets up the 73K224L / 73K324L to transmit spaces.

SETALB( )
Sets up the 73K224L / 73K324L for analog loopback mode.

CLRALB( )
Clears analog loopback mode from the 73K224L / 73K324L.

RD3EN( )
Enables the receive data pin on the 73K224L / 73K324L.

RD33S( )
Tristates the receive data pin on the 73K224L / 73K324L.

RGDI( )
Bypasses the 12 dB gain block in the receive processing path in the 73K224L / 73K324L.

RGFO( )
Enables the 12 dB gain block in the receive processing path in the 73K224L / 73K324L.

SCDI( )
Disables the scrambler in the 73K224L / 73K324L.

SCEN( )
Enables the scrambler in the 73K224L / 73K324L.

CADI( )
Sets up the 73K224L / 73K324L DSP for demodulation mode.

CADN( )
Sets up the 73K224L / 73K324L DSP for detection of call progress tones.

FSBE( )
Sets up the 73K224L / 73K324L to work in BELL 103 mode if FSK operation is selected.

FSV21( )
Sets up the 73K224L / 73K324L to work in CCITT V.21 mode if FSK operation is selected.

73D2248 Handshake State Machine

The following is a description of the handshake state machine, which defines those decisions and actions that must be performed by controller software to execute the handshake. Each "state" typically refers to a set of software instructions which control the functions specific to that state. Complex "online" functions, such as handshaking, are performed by setting up the special function registers and entering the state machine at the appropriate state. For operations that involve transitioning between off-line command mode to on-line data mode, this would be state zero. The state machine will then transition through its states until the handshake is complete or has failed. In the case of a successful handshake, the state machine will idle at state 16. Some operations will force the state machine to a specific state (e.g., a request to hang-up). A brief description of each of the states follows:

STATE_0:

Main entry point into handshake routines
start 30 second connect timer
    *** if this timer expires before the handshake
    is completed then the connect sequence
    will be terminated
initialize the 73K224L/73K324L
set speed of chip to 1200
enable S0 debounce timer
clear DTMF0 bit to set answer tone detector to 2225 Hz

if call/originate then
    if 1200 or 2400 goto STATE1
    if BELL 103 goto STATE 1
    if V.21 set 73K224L/73K324L to V.21 mode and goto STATE 31
    if V.22 half speed, set 73K224L/73K324L to 600 bit/s and
    goto STATE1
if answer then
    if 600, set 73K224L/73K324L to 600 bit/s
    if Bell 103 then set Bell mode in 73K224/73K324L
    if V.21 then set V.21 mode in 73K224L/73K324L
    set up 2 second billing delay
    goto STATE 17

STATE_1:

Call/originate MODE ENTRY POINT
search for 155 ms of Bell answer tone or
PSK unscrambled marks (2225 Hz or S0)
If Received 2225 Hz
if 600 goto STATE 40 (hang up)
if V.21 goto STATE 40 (hang up)
if Bell 103, set Bell mode, goto STATE 31
else
set timer for 450 ms and goto STATE 4
If Received S0
if 300 goto STATE 28
set up DSP for demodulation mode (not call init)
set up 450 ms delay
goto STATE 4

STATE_2:

RDLB REQUEST ENTRY POINT...
Send scrambled marks at 1200 or 2400
Set timeout timer to 20 seconds
Clear baud counter
Goto STATE 3

STATE_3:

If timeout timer is still valid
look for 231 ms of dotting pattern
if dotting received
send scrambled marks
goto STATE 27
If timer times out
send NO RDLB RESPONSE
return to MAIN

STATE_4:

wait for 450 ms, check speed
if 2400 goto STATE 5 (send S1)
else goto STATE 7 (600 or 1200, do not send S1)

STATE_5:

2400 BPS MODE SO SEND OUT 100 MS OF S1
set pattern to S1
turn of transmitter
enable S1 debounce timer
set wait timer to 100 ms and goto STATE 6

STATE_6:

If S1 received (early) goto STATE 8
If wait timer expired goto STATE 7
else goto STATE 6

STATE_7:

SEND SCRAMBLED MARKS....
turn on scrambler
set pattern to marks
turn on transmitter (in case from STATE 4)
turn on equalizer
set up 2 second timer for fallback timeout
clear baud timer
goto STATE 9

STATE_8:

got S1 early, wait out 100 ms, send scrambled marks enable equalizer
turn on scrambler
set pattern to marks
goto STATE 11

STATE_9:

LOOK FOR S1 OR PSK MARK WHILE 2 SECOND TIMER IS RUNNING
If receive S1 and 2400
goto STATE 11
If receive MARKS
set timer to 765 ms and goto STATE 10
If Timer Expired
if retrain
increment retrain counter
if retrain counter >= 40 then goto STATE 40 (hang up)
if CCITT mode goto state 40 (hand up)
else set 73K224L/73K324L for Bell mode goto STATE 31 (attempt 300)

STATE_10:

got MARKS must be 1200 or 600
wait for timer to expire
if originally 600 then goto STATE 15
else (could be fallback from 2400)
set speed bit to 1200
goto STATE 15

STATE_11:

wait for S1 to go away
set up 73K224L/324L for 2400
set up wait timer for 450 ms
goto STATE 15

STATE_12:

wait 450 ms
enable 16 way decisions in receiver
set up 150 ms
goto STATE 13

STATE_13:

wait out 150 ms
set speed of chip to 2400 and send QAM marks
set up wait timer for 200 ms
clear baud counter
goto STATE 14

STATE_14:

look for 32 consecutive marks
make sure timer has expired
goto STATE 15

STATE_15:

COMMON ENTRY POINT TO GO ONLINE
send connect message
enable RxD
allow transmitter to send data
turn off the speaker
clear the baud counter
goto STATE 16

STATE_16:

ONLINE DATA MODE MAIN LOOP STATE
- if not 1200 or 2400 then just check for carrier
  - if RDLB flag is set then just exit (loop)
  - if RETRAIN is enabled then
  - look for S1
    - GOT S1
      - set pattern to marks
      - DISABLE receive DATA
      - set speed to 1200
      - disable the equalizer
      - set receiver for 4-way decisions
      - goto STATE 22
    - if SQI bit set then set retrain flag
    - if retrain flag is set (forced or SQI bit)
      - set wait timer to 1 second
      - go force a retrain (STATE 36)
  - Look for S0...
  - if S0 then
    - clear the baud counter
    - goto STATE 37
  - if LCD is enabled look for carrier
  - if no carrier hang up
  - else loop forever...

STATE_17:

ANSWER MODE
- wait for 2 second billing delay
- if 2400 or CCITT
  - set wait timer to 3.3 seconds
  - set tone bit to 2100 hz
  - enable answer tones
  - turn on the transmitter
  - goto STATE 18
- if Bell
  - if 300 goto STATE 28
  - if 1200 goto STATE 20

STATE_18:

CCITT ANSWER MODE
- wait out 3.3 second timer
- turn off answer tone
- set up wait for 75 ms silence
- goto STATE 19

STATE_19:

- wait for 75 ms silence
- if 300 V.21 goto STATE 28
- else set TxD pattern to MARKS
  - turn on transmitter
  - enable equalizer
  - start 3 second validation timer
  - enable S1 debounce timer
  - clear baud counter
  - goto STATE 21

STATE_20:

BELL ANSWER MODE
set 2225 Hz answer tone bit
enable answer tones
turn on transmitter
enable equalizer
start 2 second validation timer
enable S1 debounce timer
clear baud counter
goto STATE 21

STATE_21:

during 3 second validation time
if we are 2400, look for S1 or PSK MARKS
if 1200, just look for PSK MARKS
if S1 received
goto STATE 22
if PSK MARKS
set up 765 ms timer
set DCD
turn off answer tones
set TxD pattern to MARKS
turn on the scrambler
goto STATE 10
if 3 second timer expires...
look for carrier...
if carrier found
if CCITT mode goto STATE 40 (hang up)
else set up 73K224L/324L for Bell mode goto STATE 28 else
reset 3 second timer and keep looking...

STATE_22:

wait for S1 to go away
set pattern to S1
set wait timer for 100 ms
goto STATE 23

STATE_23:

wait out 100 ms delay
set TxD pattern to MARKS
turn on the scrambler
set up wait timer for 350 ms
goto STATE 24

STATE_24:

wait for 350 ms
enable 16 way decisions in receiver
set up wait timer for 150 ms
goto STATE 24

STATE_25:

look for 32 consecutive QAM marks
wait for timer to expire
set TxD pattern to MARKS
change chip speed to 2400 (QAM MARKS)
set wait timer for 200 ms
goto STATE 26

STATE_26:

wait out 200 ms delay
goto STATE 15

STATE_27:

Check for timer timeout...
Look for 231 ms of MARKS
GOT MARKS...
set RDLB flag
return to online state (STATE 15)
NO MARKS
reset baud counter and exit
TIMER TIMEOUT...
send no RDLB response
return to main

STATE_28:

300 BAUD ANSWER MODE ENTRY POINT
disable call init mode
set chip speed to 300
disable equalizer
disable to scrambler
set pattern to MARKS
turn on the transmitter
clear the baud counter
goto STATE 29

STATE_29:

COMBINED ANSWER / Call / originate MODE
look for 155 ms of FSK marks
set speed bits to 300
if call/originate mode
set up 450 ms timer
goto STATE 33
if answer mode
goto STATE 15

STATE_30:

wait for timer to expire
make sure speed bits are set to 300
goto STATE 15

STATE_31:

300 BAUD CALL ORIGINATE ENTRY POINT
disable call init mode
disable equalizer
disable the scrambler
set chip speed to 300
goto STATE 29

STATE_32:

300 BPS BUG WORKAROUND
set up to send dotting in ALB mode
if dotting received
goto STATE 29
else
reset DSP

STATE_33:

wait out 450 ms timer
set pattern to MARKS
turn on transmitter
set up wait timer for 300 ms
goto STATE 30

STATE_34:

EXIT POINT FOR ONLINE COMMAND MODE. WHEN SERIAL INTERRUPT DETECTS AN ESCAPE SEQUENCE IT FORCES THE STATE MACHINE HERE.

set up 500 ms wait
wait out 500 ms timer
tristate RxD
set TxD pattern to MARKS
set command mode flag
reset receive and transmitter buffers
exit state machine and go to MAIN

NOTE: RE-ENTRY IS DONE THROUGH STATE 15 (ONLINE) OR STATE 40 (HANG UP).

STATE_35:

NOT USED AT THIS TIME

STATE_36:

WAIT FOR TIMER TO EXPIRE AND INITIATE A RETRAIN

wait for timer to expire
Tristate RxD
set TxD pattern to marks
set speed to 1200
disable the equalizer
set for 4 way decisions
goto STATE 5

STATE_37:

LOOK FOR S0 ON-TIME TO DISTINGUISH BETWEEN RETRAIN AND RDLB REQUESTS

NOTE: Some modems send a double dotting pattern (S1) that is not synchronized with its BAUD clock. Because the 73K224L looks at spectral response for its detectors and not data patterns the S1 pattern for retrain sometimes looks like S0. Our solution for this problem is to qualify S0 so that a response of 100 ms or less is taken as an S1 or retrain request, and an S0 of 155 ms or greater is taken as an RDLB request from the remote modem.

```
is S0 is on for at least 155 ms then
        send dotting pattern
        goto STATE 38
if S0 is on for 100 ms or less
        if retrain enable flag is set
                setup for retrain
                goto state 22
otherwise return to state 16 online...
```

STATE_38:

WAIT FOR S0 TO GO AWAY

set RDLB flag
stop sending dotting
put chip in RDLB
goto STATE 39

STATE_39:

LOOK FOR 77 MS CARRIER DROP...

```
wait for carrier to drop
        clear test modes
        clear RDLB flag
        wait 1 second for things to settle
                return online (STATE 15)
```

STATE_40:

turn off the speaker
reset buffers
tristate RxD
turn off transmitter
go On-Hook
send “No Carrier” message
clear DCD
clear CD LED
return to main

STATE_41:

LEASED LINE ENTRY
if speed is 2400
set up 73K224L/324L for 2400 bit/s
enable 16 way decisions
goto STATE 44
else if speed is 1200
set up 73K224L/324L for 1200 bit/s
enable 4 way decisions
goto STATE 44
else if speed is 600
set up 73K224L/324L for 600 bit/s
enable 4 way decisions
goto STATE 44
else if speed is 300 and BELL mode
set up 73K224L/324L for Bell 103 operation
else
set up 73K224L/324L for CCITT V.21 operation

STATE_42:

NOT USED AT THIS TIME

STATE_43:

turn on DSP
disable call init mode
set modulation to 300 bit/s
disable equalizer
disable scrambler
set up to transmit MARKS
turn on the transmitter
clear baud timer
goto STATE 45

STATE_44:

enable DSP for demodulation
turn on DSP
turn on scrambler
turn on equalizer
set up to transmit MARKS
turn on transmitter
clear the baud timer
goto STATE 45

STATE_45:

if carrier detected
if baud timer indicates 155 ms of carrier
enable S0 timer
enable S1 timer
enable SQI timer
goto STATE 15
else
reset baud timer

4.10.5 DEV_INT.A51

This module includes interrupt service functions that are specific to the 73K224L / 324L. The entry point of this module is INT96 and is called from the interrupt service routine located in INTS. Timer 0 is set up to interrupt at a rate of 9600 times per second and each interrupt results in a call to INT96. Each time the timer interrupt occurs, one of the 16 operations is sequentially executed. Since the symbol rate of the 73K224L / 73K324L is 600 baud and 9600 divided by 16 equals 600, each of the 16 operations is executed once per symbol. A description of the program flow follows:

```
INT96:
    Reload timer 0 to interrupt 1/9600 Hz from now
    Read the 73K224L/73K324L Detect Register
    Index Jump to one of 16 operations
        .
        .
        .
EXIT:
    Increment operation index
    Return from Interrupt
```

The 16 operations are outline below:

```
INTR0:
    IF not in selftest
    Read receive data bit from detect register
    Store bit in variable MRK1
    Adjust the speaker volume
    Jump to EXIT

INTR1:
    Update the external latches
    Jump to EXIT

INTR2:
    Test (debounce) Unscrambled Mark Bit from detect register
    IF TRUE
        Set FS0TST
    JUMP to EXIT

INTR3:
    Test (debounce) Answer Tone Bit from detect register
    IF TRUE
        SET FANSTTST
    JUMP to EXIT

INTR4:
    Read received data bit from detect register
    Store bit in variable MRK2
    JUMP to EXIT

INTR5:
    Update external latches
    JUMP to EXIT
```

```
INTR6:
    IF not in command mode
        Read Carrier Detect bit from Detect Register
        Store in variable FCD
    JUMP to EXIT

INTR7:
    Service “wait” timer.
    Service “gp timer 1” timer.
    JUMP to EXIT

INTR8:
    Read received data bit from detect register
    Store bit in variable MRK3
    JUMP to EXIT

INTR9:
    Decrement S1 Bridge Timer
    JUMP to EXIT

INTR10:
    Process S1 Bit from detect register
    JUMP to EXIT

INTR11:
    Test (debounce) Call Progress Detector bit from detect register
    JUMP to EXIT

INTR12:
    Read received data bit from detect register
    IF bit * MRK1 * MRK2 * MRK3 == 1
        Set variable MARKS
    ELSE
        Clear variable MARKS
    ENDIF
    IF bit + MRK1 + MRK2 + MRK3 == 1
        Clear variable SPACES
    ELSE
        Set variable SPACES
    ENDIF
    JUMP to EXIT

INTR13:
    Update External latches
    JUMP to EXIT

INTR14:
    Test (debounce) Signal Quality Indicator
    JUMP to Exit
```

```
INTR15:
    decrement the transition timer
    if transition timer = 0 then
        reload transition timer to 8
        get the transition counter
        if not 1200 or 2400
            reset dotting bit and exit
        if 2400 then compare transition counter to 31
            if transition  counter >= 31 then set dotting
            else reset dotting
            exit
        if 1200 then compare transition counter to 15
            if transition >= 15 then set dotting
            else reset dotting
    exit
```

4.10.6 EEPROM.A51

This module contains the functions used to read and write to the EEPROM. The EEPROM is used to store the value of certain S-registers as well as other modem settings while power is off. The contents of the EEPROM are read when the modem is powered on or whenever the modem is reset. The functions in EEPROM.A51 that support this functionality are described below.

INIT_EEPROM( )

This routine currently performs no function. It will simply return to the caller.

EEP_STORE(stored_profile:[Acc])

This function writes the current configuration to the EEPROM. The accumulator indicates which of two stored profiles will be updated.

EEP_RECALL(stored_profile:[Acc])

This function will read one of the two stored profiles and update the modem configuration with the stored profile. The value passed in the accumulator determines which profile is read. A value of 0 will read stored profile 0 and a value of 1 will read stored profile 1.

EEP_P_STORE(stored_profile:[Acc])

This function selects which stored profile will be read from the EEPROM on power-up. The accumulator indicates which stored profile and should be 0 for stored profile 0 and 1 for stored profile 1.

EEP_P_RECALL( )

Reads the EEPROM configuration at power up. If it is determined that the EEPROM is empty, the default configuration will be written to the EEPROM and loaded into the modem.

STORED_PROFILE( )

This function will print the formatted contents of the EEPROM to the DTE. It is used to implement the &V command.

GET_STORED_BMR(stored_profile:[Acc]) Returns: S14[ts1], S21[ts2], S22[ts3], S23[ts4], S27[ts5]

This function reads five bit-mapped registers from the stored profile indicated by the accumulator and writes their contents to RAM. S-register to RAM Variable mapping is as follows:

S Register	RAM Variable
S14	ts1
S21	ts2
S22	ts3
S23	ts4
S27	ts5

An accumulator value of 0 returns stored profile 0 and 1 will return stored profile 1.

EEP_WRITE(EEPROM address[DPTR], value[Acc])

This function will write a single byte to the EEPROM. The address to be written should be in the data pointer and the value to be written should be in the accumulator.

PHONE_ADDRESS(phone number slot [acc], offset[r1]) Returns: EEPROM address[DPTR]

This function will return the address plus offset of the passed telephone number slot. The EEPROM will store up to 10 phone numbers in non-volatile memory. To determine the address of a particular digit of a stored phone number, a value that corresponds to the desired phone number slot (0 through 9) should be passed in the accumulator and the desired digit should be passed in the r1 register. The address of the desired digit will be returned in the data pointer.

E_DIAL_STORE(phone number slot[Acc])

This function will write the phone number contained in the accumulator to the passed phone number slot. The desired phone number slot should be passed in the accumulator and can take a value from 0 to 9.

E_DIAL_RECALL(phone number slot[Acc], dial[DIAL_CMD])

This function will read the phone number from the passed phone number slot and write it to the DTE. If the dial_cmd bit variable is set, the phone number will be written into the command buffer. The desired phone number slot should be passed in the accumulator and takes on a value from 0 to 9.

4.10.7 INTS.A51

This module contains the interrupt service routine code. Much of the discussion on the operation of this code is contained in the section on interrupts. Additional information on the entry points in this module is contained below.

ES_INT( )

This interrupt service routine is called every time a character is received by the microprocessor UART or the microprocessor UART has completed transmitting a character. If the modem is online and in clear mode (no auto-speed buffering or protocols are in effect) this routine need only do escape code detection and then return to the caller. This is because the 73K224L / 234 is “hard-wired” to the serial interface and data need not pass through the microprocessor.

In command mode, received characters will be placed in the command buffer. If a result code is being sent, the pointers to the result code string are updated and the next character is placed in the UART transmitter.

If a protocol is in effect and the modem is in online data mode, control is passed to DTE_RX_INT for every character received from the DTE and to DTE_TX_INT for every character that is transmitted to the DTE. A pseudo-code description of this routine is given in the section on interrupts.

TIMERS( )

This interrupt service routine is called in response to a timer 2 interrupt. The cause of the interrupt can be a transition of ring detect line or expiration of timer 2. The former is used to detect and qualify ringing signals and the latter is used for general purpose time keeping. TF2 and EXF2 indicate the source of the interrupt and TIMERS uses these flags in order to determine if it should process ringing or do general purpose timekeeping. The ringing code starts at label GOTR and the general purpose timer code starts at GPT. More details of the processing in this routine is contained in the section on interrupts.

EX_INT1( )

External interrupt 1 is used to perform the “auto-baud” function of the modem. When in command mode and an “AT” is entered at the DTE, the modem will determine the bit rate and parity of the the DTE from the incoming bit stream. The DTE rate is calculated by measuring the width of the start bit of the “A.” Provided that an “A” followed by a “T” is received, this number is used to set the receive rate of the microprocessor serial port. A complete description of this code is given on the section on interrupts.

EX_INT0( )

This interrupt is tied to the transmit clock line of the 73K224L / 324L IC. In online data modes running a protocol, it is used to signal the protocol code that a symbol is required for transmission over the phone line. A call is made to DCE_TX_INT to get the symbol. If a protocol is not running, this interrupt is ignored.

TIMER_0_INT( )

This interrupt service routine has two functions. Timer 0 is programmed to interrupt the microprocessor 9600 times per second during handshaking. Control will be passed to INT96 that checks that status of the modem receiver and performs various housekeeping functions during handshaking. INT96 is in the DEV_INT.A51 module and that code is described in the corresponding section of this document.

The second function is to service receive clock interrupts from the modem chip when the modem is online in auto speed buffering mode (a protocol is running). The receive clock will generate an interrupt every time a symbol is ready. A call will be made to DCE_RX_INT to process the received symbol.

ESC_PROCESS( ) Returns: escape detected[ESC_FLAG]

This function monitors the data stream from the DTE to detect an escape sequence. The escape sequence is used to place the modem in the online command mode from the online data mode. It consists of a guard time (1 second of no data) followed by three escape characters ("+" is the default escape character) followed by another guard time. This routine should be called every time a character is received by the modem from the DTE. When an escape sequence is detected, the flag ESC_FLAG is set to signal the foreground task to switch to the command mode.

4.10.8 SUBS.A51

INIT_ASRCH( )

Used to setup the modem to autobaud. When transitioning from a data mode to a command mode, the modem must be initialized to measure the start bit length of an "A" in a command to determine the DTE bit rate.

INIT_UART( )

Used to set up the UART for data mode. When the modem transitions from command to data mode, the serial UART of the microprocessor needs to be set up (in autospeed buffering) or disabled (clear mode). This function will determine how to set up the modem from flag variables when transitioning from command to data mode.

INIT( )

Power-on initialization code. Initializes all the microprocessor registers and general purpose timers.

INIT_TIMERS( )

Power-on initialization for the general purpose timers.

INIT_MODE_1( )

This function will set up the modem for the offline command mode a-search state (see section on Major Modem States).

INIT_MODE_2( )

This function will set up the modem for the offline command mode a-found state (see section on Major Modem States).

INIT_MODE_3( )

This function will set up the modem for the online handshake state (see section on Major Modem States).

INIT_MODE_4( )

This function will set up the modem for the online data with auto speed buffering state (see section on Major Modem States).

INIT_MODE_5( )

This function will set up the modem for the online command with auto speed buffering, a-found state (see section on Major Modem States).

INIT_MODE_6( )

This function will set up the modem for the online command with auto speed buffering, a-search state (see section of Major Modem States).

INIT_MODE_7( )

This function will set up the modem for online command, clear connection, a-search state (see section of Major Modem States).

INIT_MODE_8( )
This function will set up the online command, clear connection, a-found state (see section of Major Modem States).

INIT_RS232( )
This function performs power-on initialization of the modem RS-232 control lines and other hardware I/O.

UPDATE( )
This routine updates the RS-232 leads and the LEDs with information located in internal variables.

UPPERCASE(character:[Acc])
Converts the character passed in the accumulator to upper case.

GET_VALUE( ) Returns value:[Acc]
Reads a number from the command line. Value is returned in the accumulator. Values preceded by '$' are assumed to be hexidecimal; values preceded by '#' are assumed to be binary.

CONVERT_DIGIT(ASCII digit:[Acc]) Returns value:[Acc]
Converts a single ASCII digit (0-9,A-F) to a value (0 - 15). Values are both passed and returned in the accumulator.

GET_DIGIT( ) Returns value:[Acc]
Reads a single ASCII hex digit from the command line. Returns the value of the digit in the accumulator.

GET_NUMBER(radix:[variable base]) Returns: number:[Acc]
Reads number from command line and returns the value in the accumulator. Radix must be stored in variable base before calling this function.

SEND_NUM(number:[Acc])
Sends the number in the accumulator to the DTE as an ASCII result code. Checks to see if verbose mode is enabled, sends a carriage return if it is, then sends the value to the DTE.

SEND_CRLF( )
Sends a carriage return - line feed sequence to the DTE.

DTR_MODES( ) Returns DTR_MODE:[Acc]
Determines and returns the DTR mode of the modem based on the setting of the &Q and &M commands. Mode (0-5) is returned in the accumulator. The DTR mode determines the function of the DTR and DSR lines. See the &Q command for details.

SEND_1BIT(binary value:[C])
Sends an ASCII "zero" or "one" to the accumulator followed by a space.

SEND_1NUM(decimal digit:[B])
Send an ASCII digit to the DTE. The b register must contain a value from 0 to 9.

SEND_AMPER( )
Sends and ASCII "&" to the DTE.

SEND_CONFIG( )
Sends the state of the B, E, L, M, Q, V, X, Y, &C, &D, &G, &J, &L, &P, &Q, &R, &S, &X, and &Y commands to the DTE.

SEND_CARRIER( )
Sends the "CARRIER" result code to the DTE. If extended result codes are set, the "CARRIER xxx" will be sent where xxx is the DCE speed.

SEND_RES_CODES( )
Based on the setting of the S95 register and the "W" command in effect, sends the results codes for compression, protocol and connect to the DTE.

CLEAR_CONNECT( )
Sends result code for a clear connection to the DTE (i.e., no protocol or compression).

SEND_PROTOCALL( )
Sends result code for the DCE protocol to the DTE.

SEND_COMPRESSION( )
Sends result code for the DCE data compression selected to the DTE.

SEND_DTE_SPEED( )
Sends result code for the DTE speed.

SEND_DCE_SPEED( )
Sends result code for the DCE speed.

4.10.9 MACROS.A51

The following macros are used to manipulate variables in external memory.

%CLRXBIT(address, bit)
Clears a single bit in external memory. Address is a location in external memory and bit is an eight bit "shadow" that indicates which bit position to clear.

%GETXBIT(address, bit) Returns: bit:[c]
Reads a single bit from external memory. Address is a location in external memory and bit is an eight bit "shadow" that indicates the bit position to be read. The value of the bit is returned in the carry flag.

%GETSFR(sfr) Returns: value:[a]
Reads the value of a special function register located in external memory. SFR is an eight bit index to the special function register.

%PUTXBIT(address, bit, value:[c])
Writes a single bit to external memory. Address is a location in external memory and bit is "shadow" that indicates the bit position to be written.

%SETXBIT(address, bit)
Sets a single bit in external memory. Address is a location in external memory and bit is an eight bit "shadow" that indicates the bit position to be set.

4.10.10 ASSEMBLING AND LINKING THE SOURCE CODE

There are currently four versions of firmware that can be compiled with the makefile (V42SYS.MAK) supplied on the firmware disk. The four options are as follows:

V.42bis - V.42bis, V.42, MNP2-5, and AT command set

V.42 - V.42, MNP2-5, and AT command set

MNP - MNP2-5, and AT command set

AT - AT command set only

These options are determined at link time. As an example to compile for V.42bis version, type:

```
MAKE -fv42sys.mak -DV.42bis
```

The -f option in make determines the makefile to use.

The -D option sets V.42bis flag true for compiling. Note the -D command is case sensitive. The "D" must be uppercase, "-d" will cause make to compile the wrong version. Four batch files have been created to use the make utility. They are as follows:

masmv42b.bat - V.42bis, V.42, MNP2-5, and AT command set

masmv42.bat - V.42, MNP2-5, and AT command set

masmmnp.bat - MNP2-5, and AT command set

masmat.bat - AT command set only

If a version of MAKE is not available, one of the batch files described below can be used.

Batch file compiling

There are four batch files used to compile and link the code for the four versions of firmware. They are as follows:

asmv42b.bat - V.42bis, V.42, MNP2-5, and AT command set

asmv42.bat - V.42, MNP2-5, and AT command set

asmmnp.bat - MNP2-5, and AT command set

asmat.bat - AT command set only

These batch files assemble and link all of the files associated with making the selected version of firmware. Because of this it may take some time to compile and link the code.

Automatic Version Number Revision.

Included on the disk is a version of Silicon Systems' version number utility. This program is called from the makefile to automatically increment the version number every time the code is assembled and linked. The program looks for a file called "version.dat." If this file is not found, the program will prompt the user for a version string. The string can consist of any string of ASCII characters and must take the form:

anystring.number

Examples of valid strings are:

TAD.01.01.00

Version 2.0

K6113 73D2248 Version 1.9

The program will not increment the string if the string file "version.dat" did not exist. If, however, the file version.dat does exist, it searches for the last "." in the string and increments the number following it. As an example, if the following file did exist:

TAD.01.01.00

and you executed Version.EXE the file would be changed to:

TAD.01.01.01

^^ the last field incremented

VERSION.EXE also allows you to add an extension field to the version string. Executing version.exe with a command argument will append the argument onto the version string. As an example the string:

TAD.01.01.05

exists and the source is being compiled for V.42bis, version.exe could be called with the argument "-V.42bis." The resulting string would look like this:

TAD.01.01.06 -V.42bis

Notice that the last field of the version number was incremented and the argument was added to the line. If no argument is added to the command line then any old extension on the current string is removed.

The makefile "V42SYS.MAK" uses the VERSION.EXE program to automatically increment the version number every time the code is compiled. In addition it uses the extension command to add the type of firmware it is compiling to the version number. If an MNP version of the code is being compiled and the previous version number was:

TAD.01.01.09 -V.42bis

the next version number will be:

TAD.01.01.10 -MNP

The ASSEMOPS.A51 File

The ASSEMOPS.A51 file is used for assembly options. Some of these options may be used and some are to be left alone.

ELMER

The first option "ELMER" is for Silicon Systems internal use and must be left as 0. Changing this equate to a 1 may cause your modem to error.

DEBUG

The DEBUG option assembles an added command ATKn. This command is for debugging the code and should always be set to 0. However if you wish to use this option, a 1 will cause the following to occur when ATKn is sent to the modem.

n = 0 = Lower RAM

n = 1 = Upper RAM

n = 2 = 73K224L internal registers

n = 3 = interrupt registers

n >= 4 = Returns an ERROR

MICKEY

This option is also an Silicon Systems internal option and should be set to 0. A value of 1 will cause your modem to error.

NEWBRD

This option is also an Silicon Systems internal option and should be set to 0. A value of 1 will cause your modem to error.

FAXCMD

This is the FAX command switch. If this is set to 1, FAX commands will be assembled into the code. See the 73D2248F literature for descriptions of the FAX commands. This value is set to 0 in the original source code.

CONSW

This equate enables or disables the Context switch section of the code. If set to 1 the code for controlling the upper 64K bank of program ROM is enabled. This option is set to 0 in the original source code.

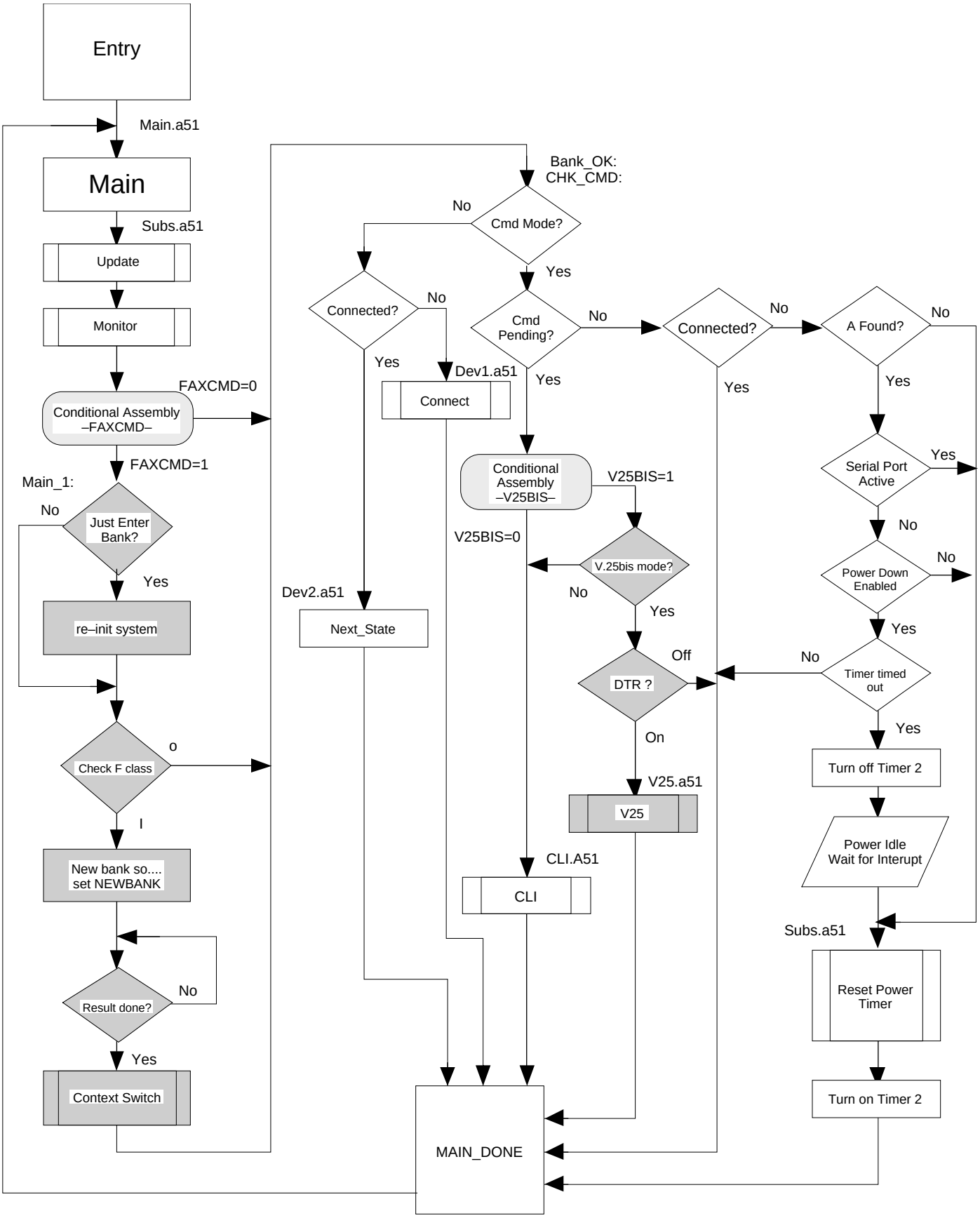


Figure 4-1: Controller Main Loop

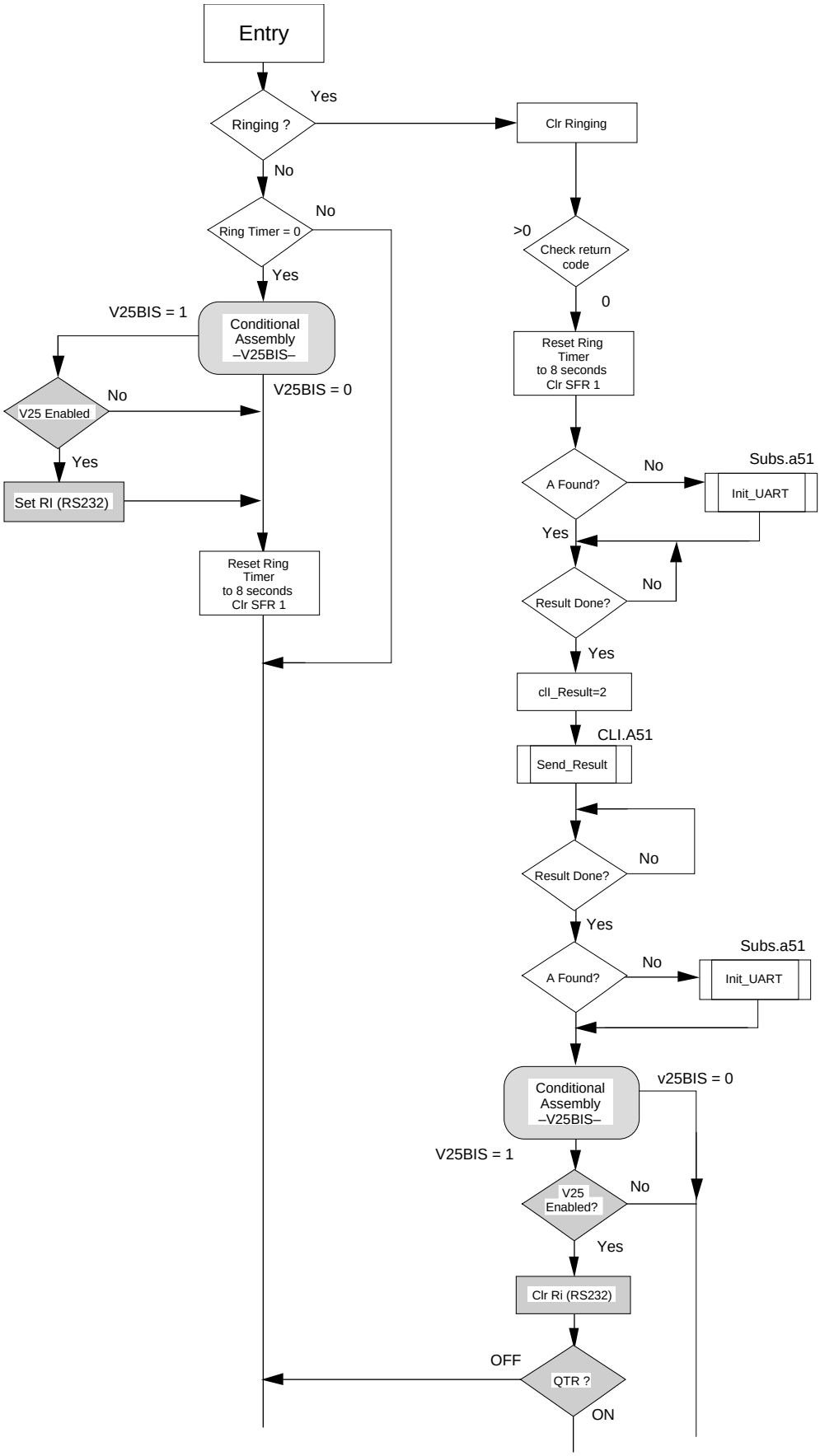


Figure 4-2A: Controller Monitor Loop

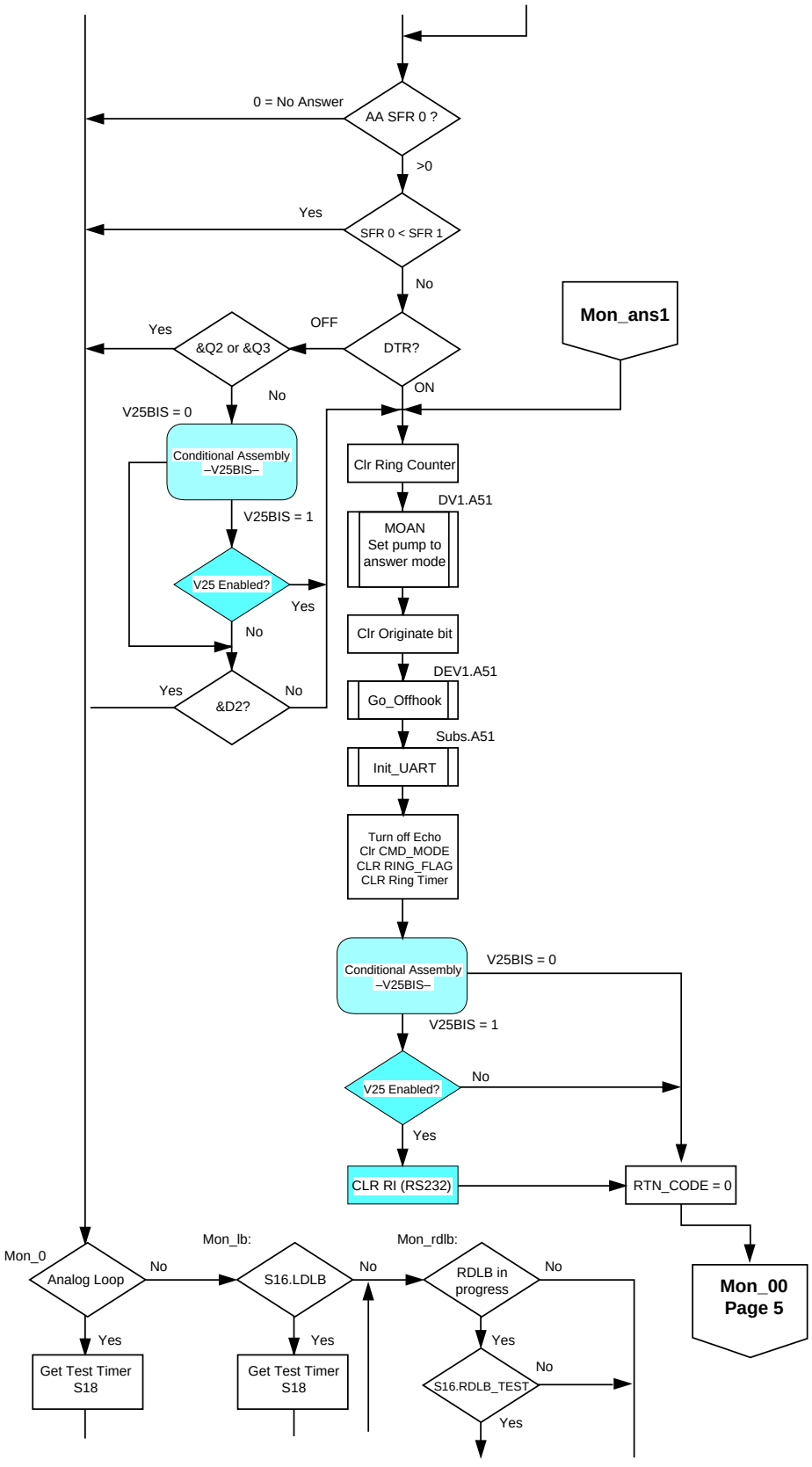


Figure 4-2B: Controller Monitor Loop

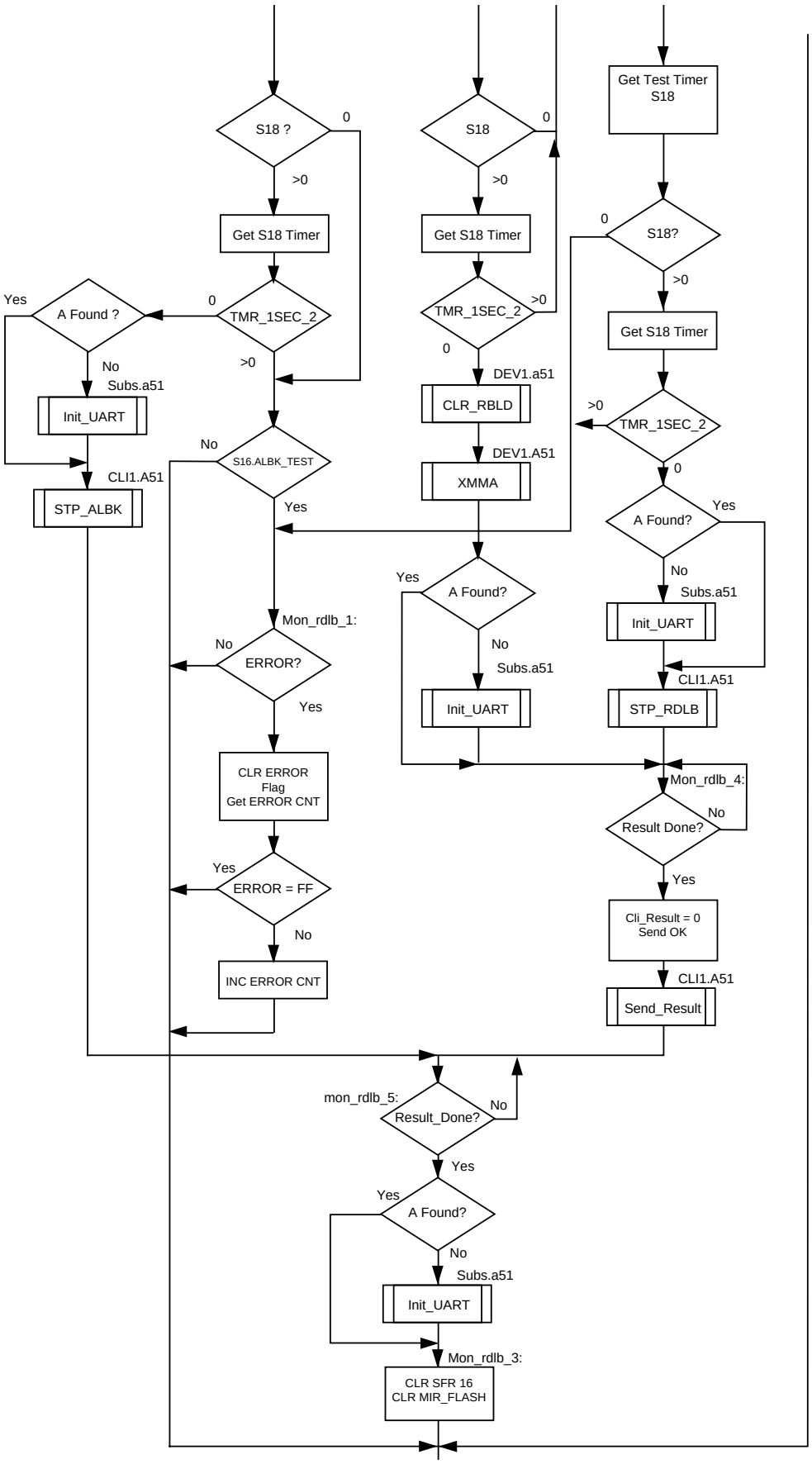


Figure 4-2C: Controller Monitor Loop

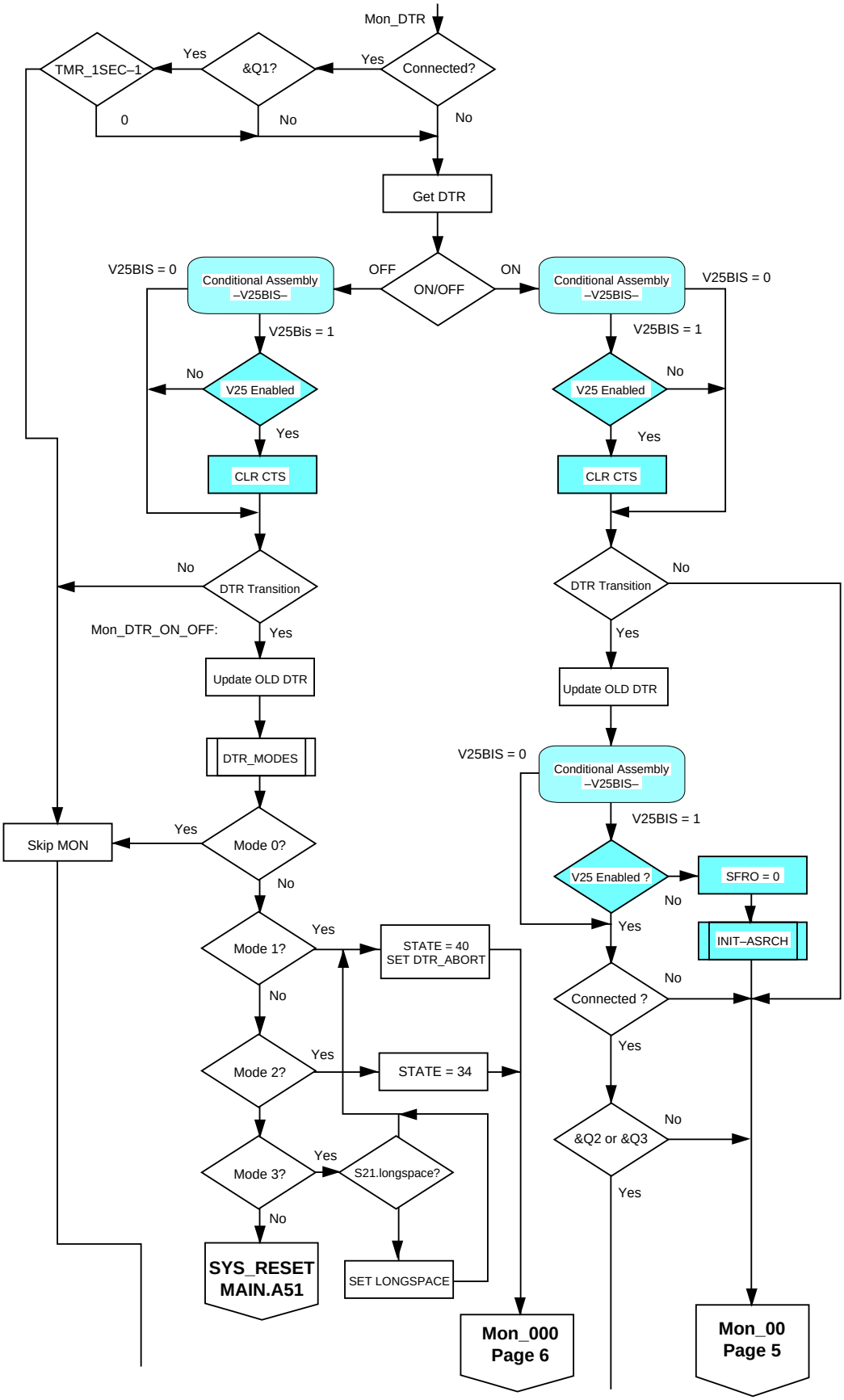


Figure 4-2D: Controller Monitor Loop

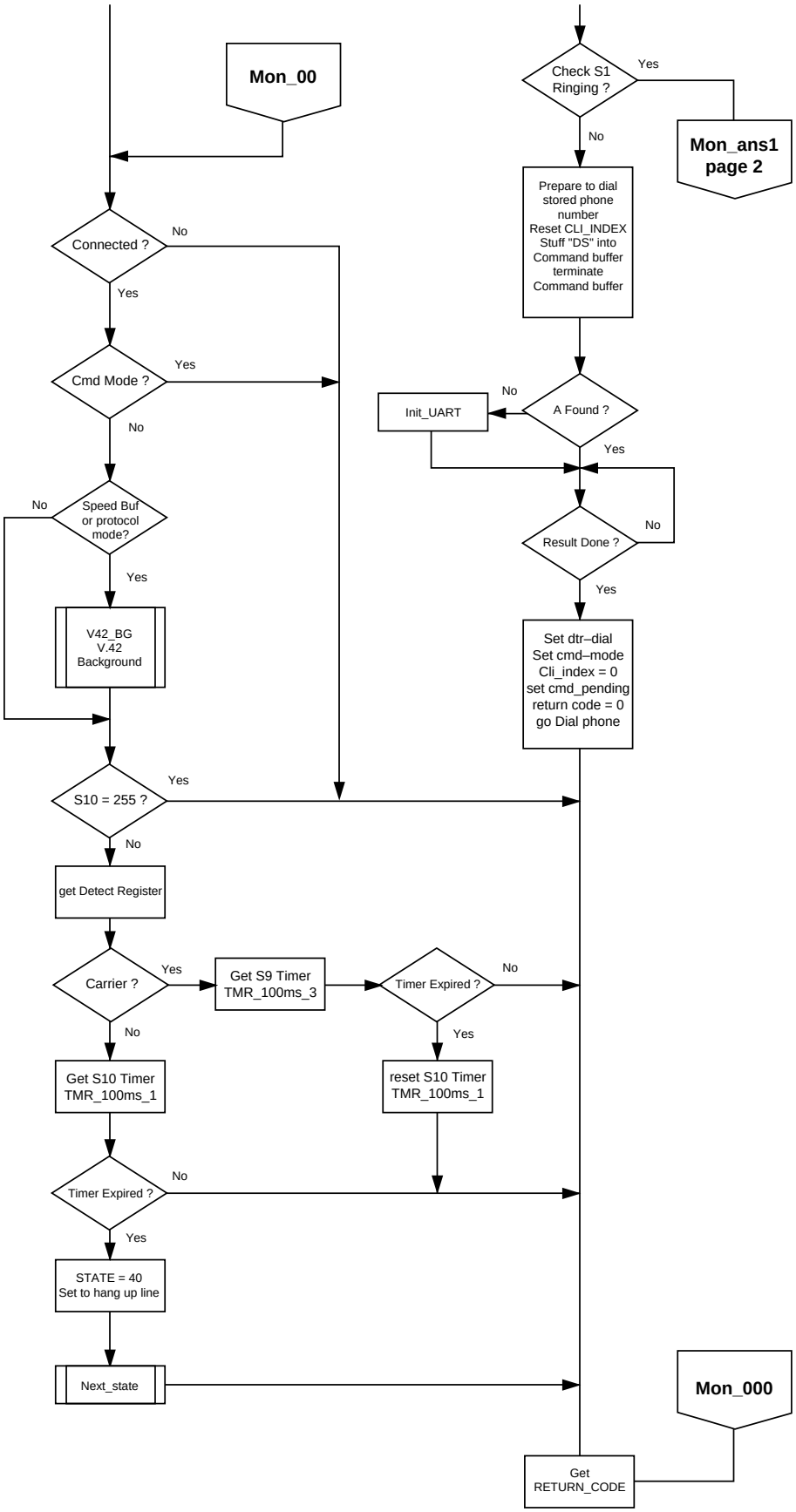


Figure 4-2E: Controller Monitor Loop

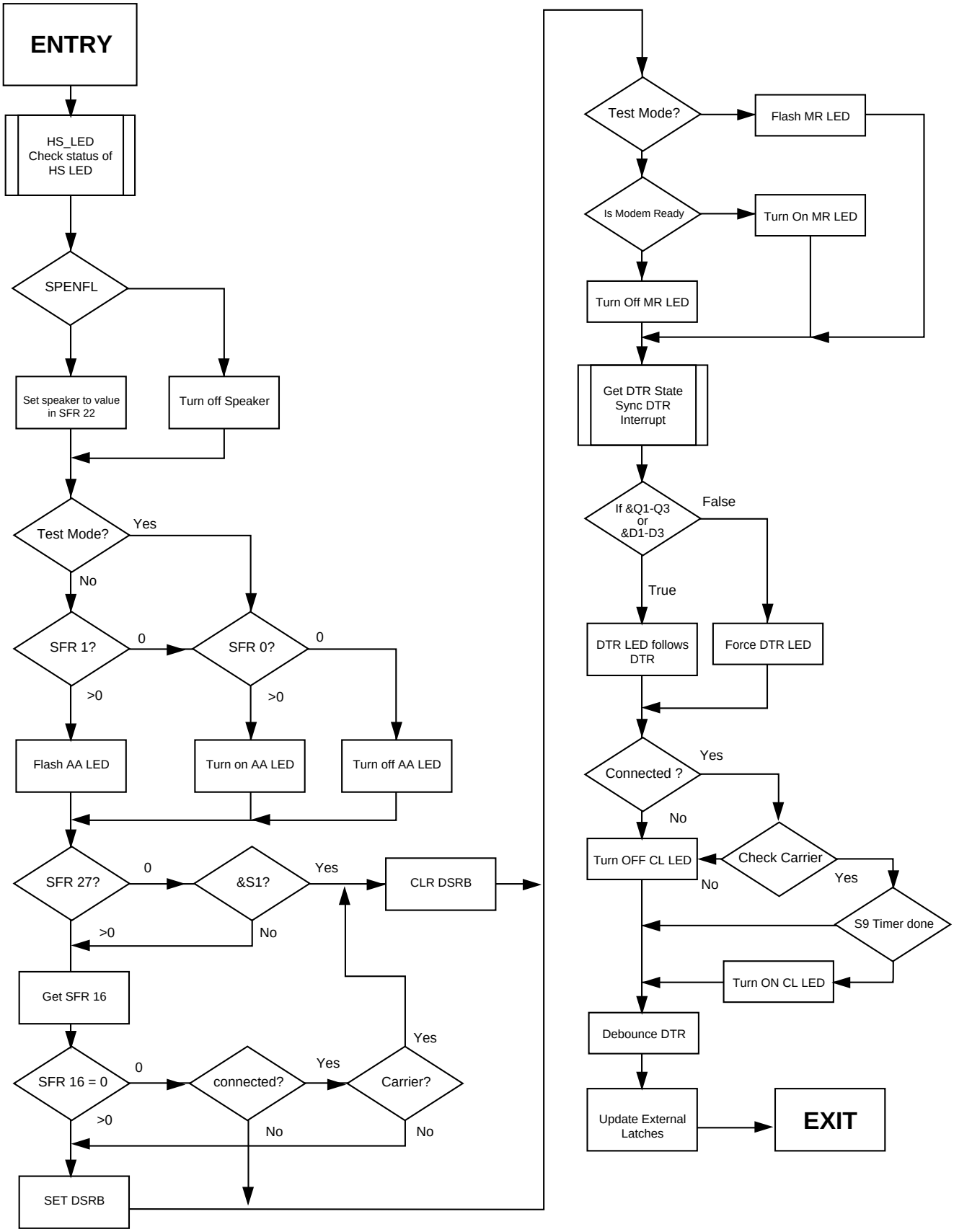


Figure 4-3: Controller Update Routine. Subs.a51

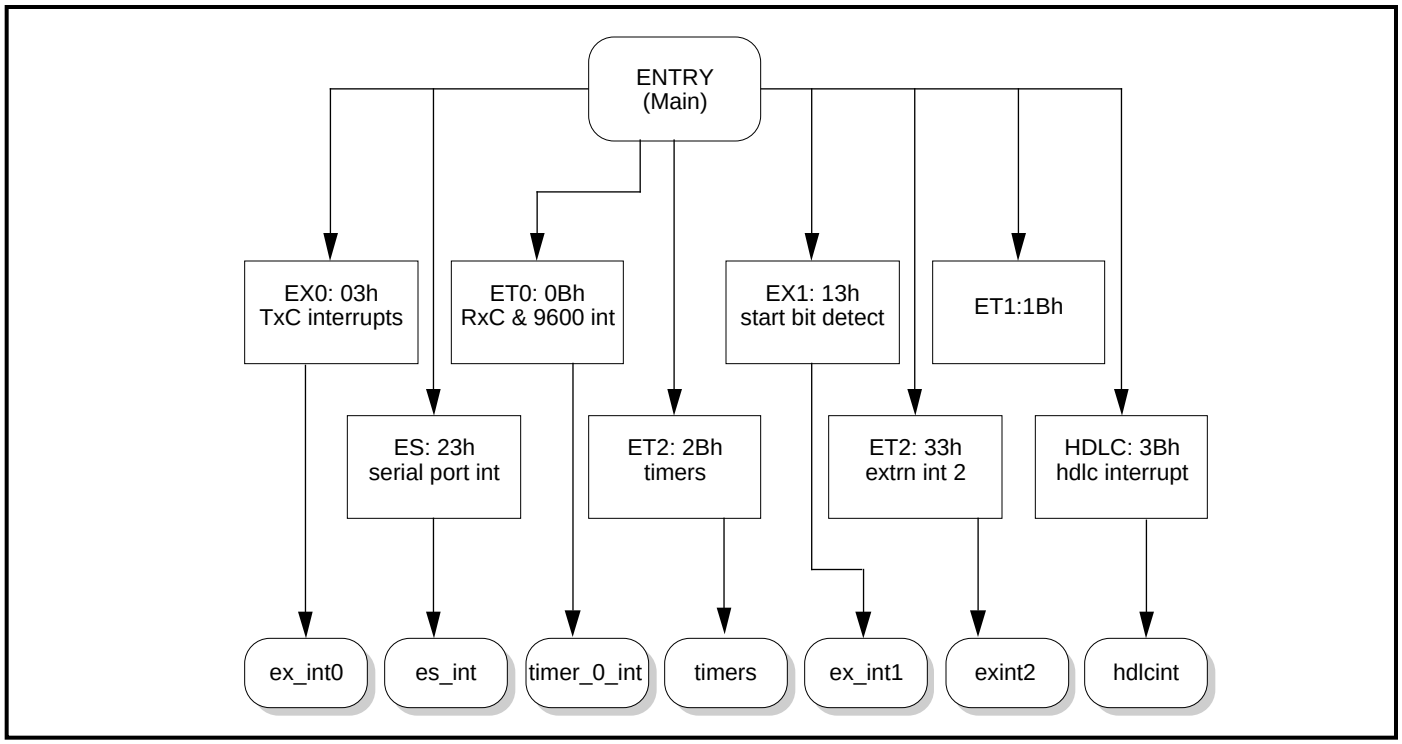


Figure 4-4: Controller Interrupt Structure (Main)

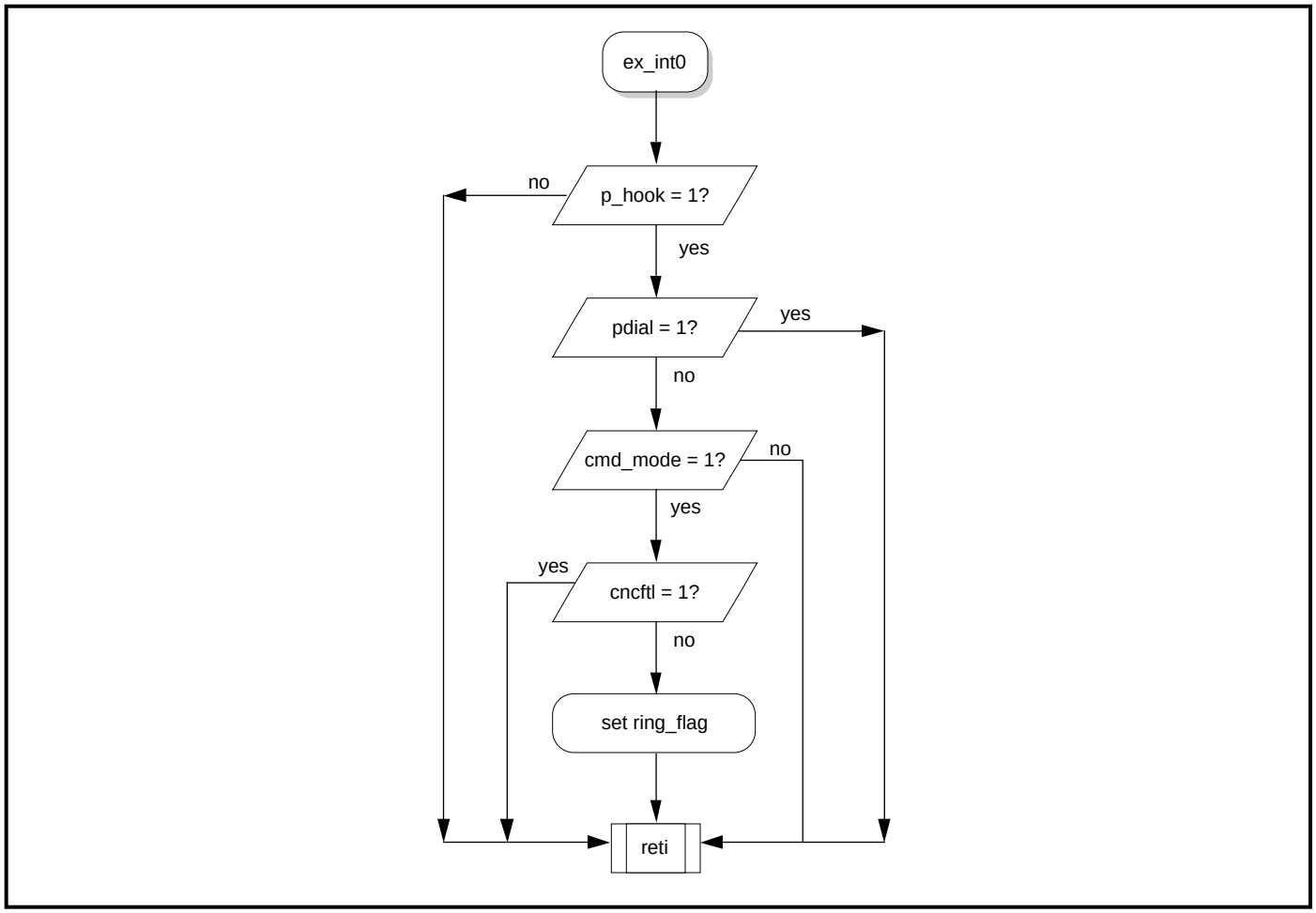


Figure 4-5: Controller Interrupt Structure (ex_int0)

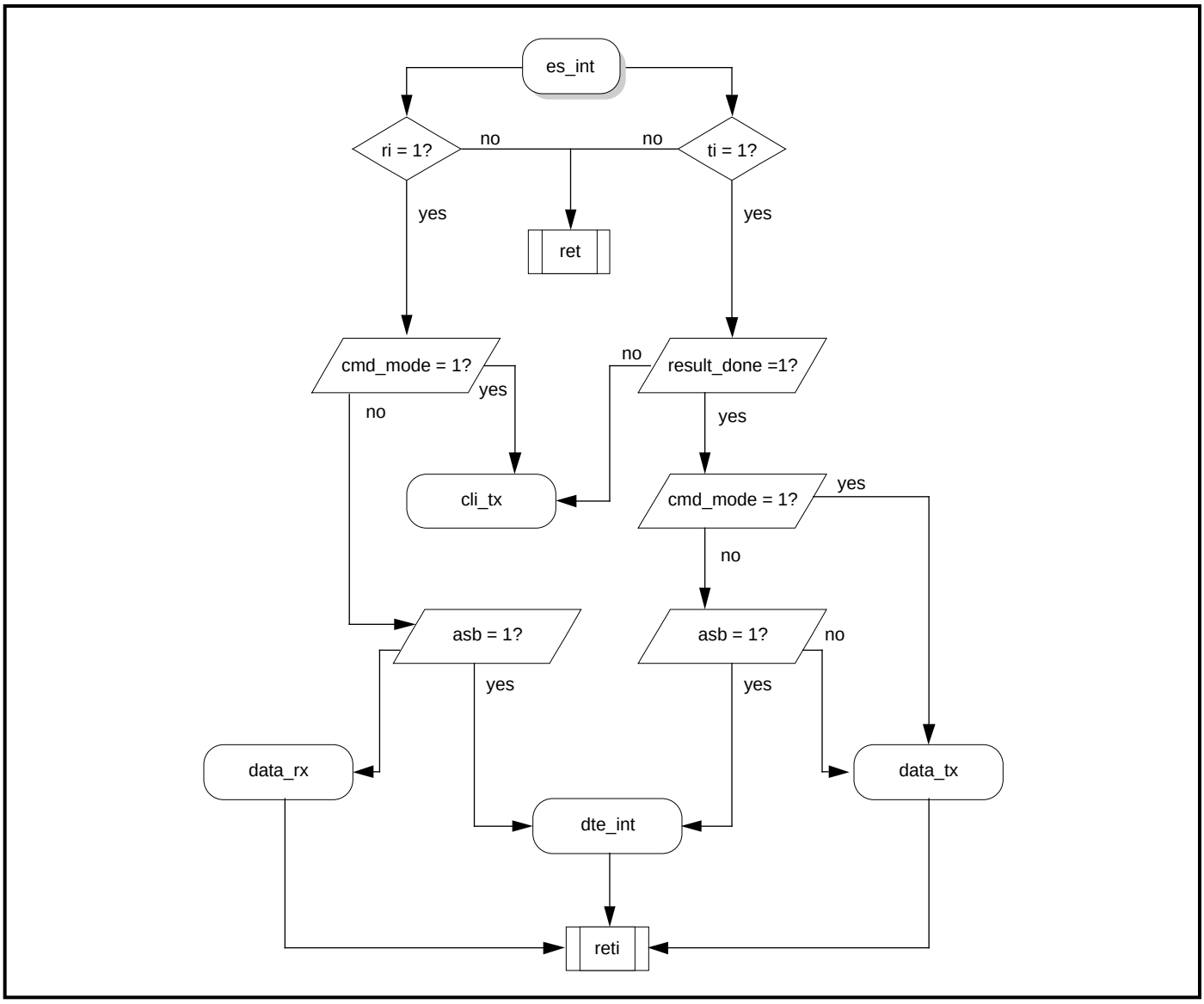


Figure 4-6: Controller Interrupt Structure (es_int)

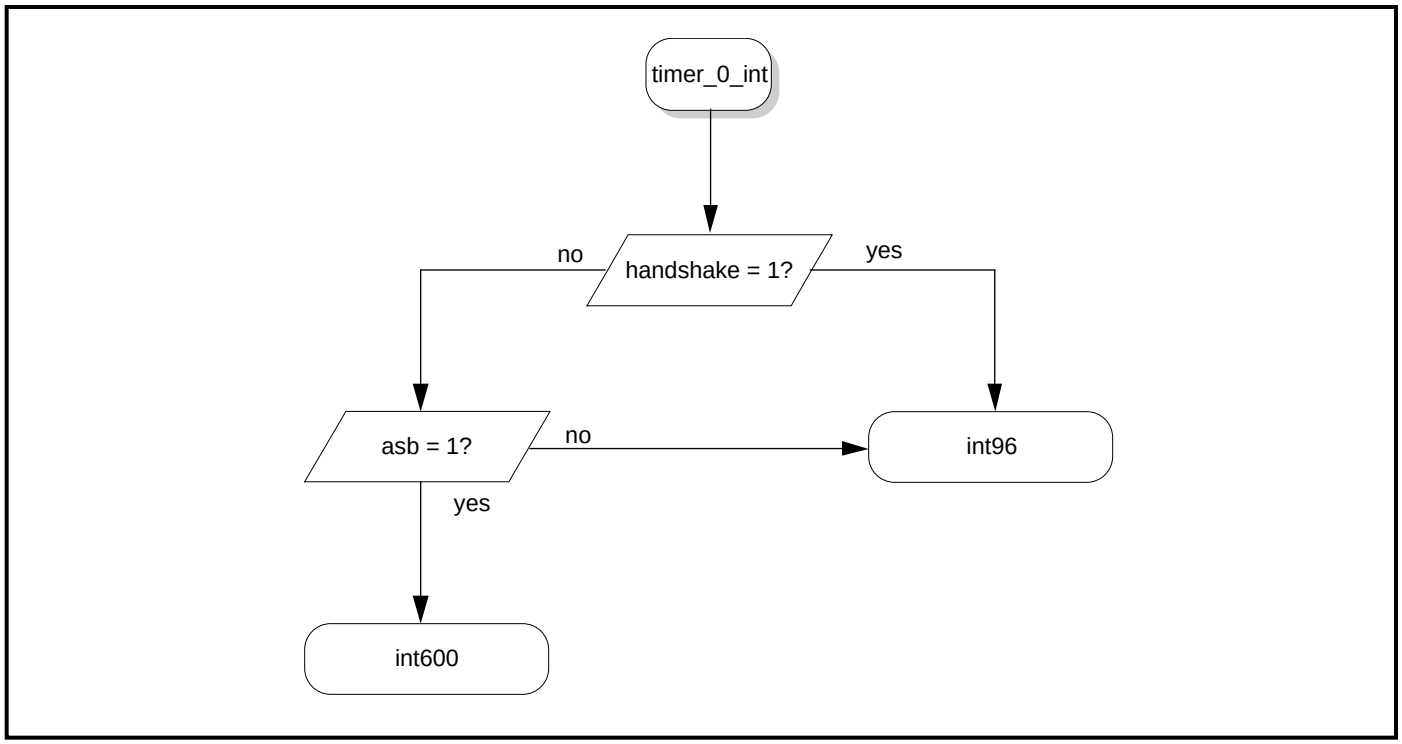


Figure 4-7: Controller Interrupt Structure (timer_0_int)

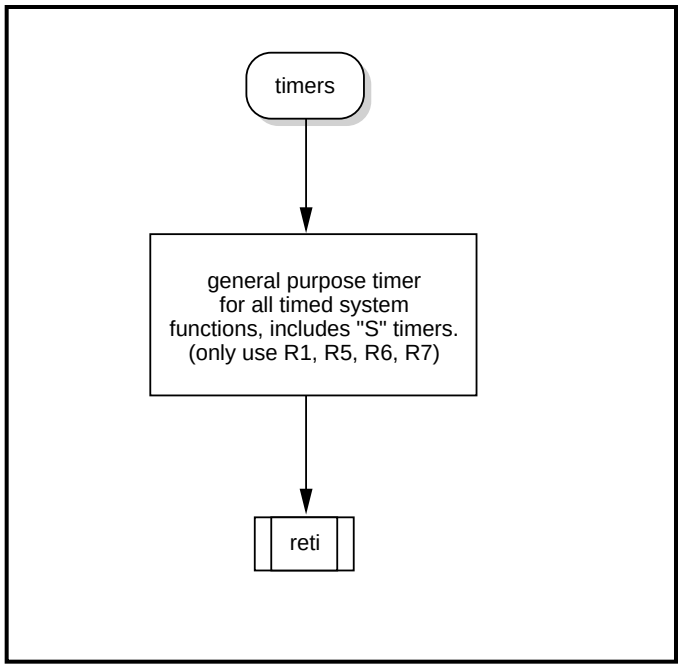


Figure 4-8: Controller Interrupt Structure (timers)

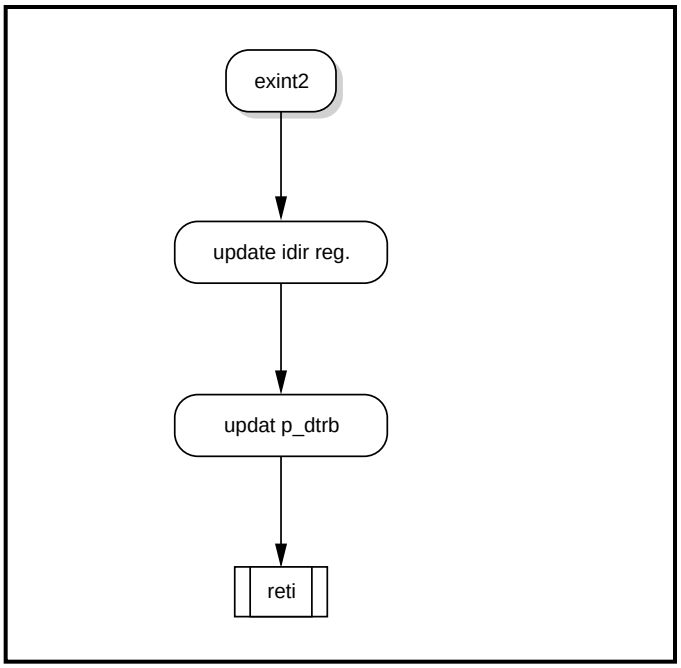


Figure 4-9: Controller Interrupt Structure (exint2)

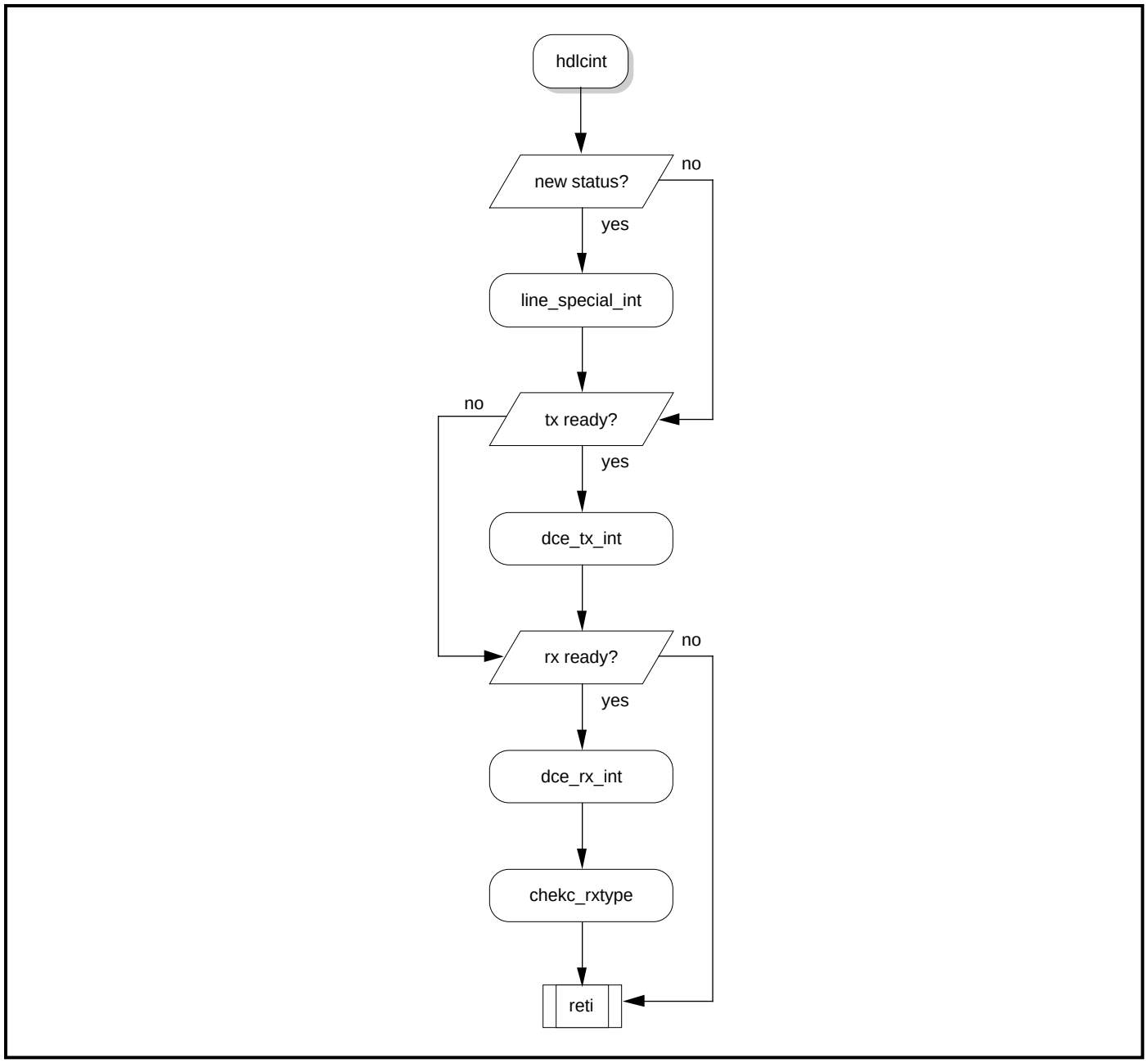


Figure 4-10: Controller Interrupt Structure (hdlcint)

4.11 V.23

V.23 has been implemented in 73D2348. Please refer to section: 4.10.10 “Assembling and Linking The Source Code” for instructions on how to add the V.23 function.

Once the V.23 code has been assembled and linked into the system you can enable this function by entering the following commands:

ATB2&Q6 (B2 for V.23 handshake and &Q6 for speed buffering)

When connected at V.23, results code “CONNECT 1275” will be displayed. This implementation of V.23 is based on the current 73D2248 code. The 73K3224L data pump is used instead of 73K224L so the modem can perform the V.23 function. The V.23 code added for this function is about 0.5k, which leaves little space for other implementations. (e.g. Caller ID.)

The V.23 half-duplex mode is not implemented at this time. Only the normal mode is available:

Originate: 75bps Tx / 1200bps Rx

Answering: 1200bps Tx / 75bps Rx

NOTE: the CCITT book does not preclude the modem from originating and transmitting at 1200 bps / receive at 75 bps, no modem manufacturer in the industry is implementing V.23 in this way.

4.12 CALLER ID

Calling Number Delivery (CND) and (Automatic Number Identification) (ANI) are services provided by the telephone companies to identify the calling party's telephone number. ANI exists today as a part of the interstate telephone network's long distance billing and control functions in the signaling channel (not the message carrying channel), and is a component of the ISDN standard. The local operating companies send this data to the long distance carriers who then pass it along. CND or caller ID is a service of the local telephone companies similar to call forwarding or call waiting, and is a billable service. The calling station phone number, date, and time are sent to the called station in a burst of Bell 202 FSK between the first and second ring during the silent period only if the answering station remains on hook. Going off hook immediately after the first ring will stop transmission of the CND carrier. The calling party telephone number for CND is the ANI data sent to or by the long distance carriers. The term ANI is often incorrectly used when CND is the service being discussed, but people familiar with these services will usually not complain if it is used in the caller ID context.

CND was originally a part of CLASS (Custom Local Area Signalling Service), as is DTMF dialing and a number of other current and future services. Analog Display Services Interface (ADSI) is a new service that was developed to take advantage of emerging "smart telephone" features and is backward compatible with CLASS. CLASS includes distinctive ring, call forwarding, message waiting, and CND. CLASS and ADSI signals, such as call waiting, can be sent while off hook, although automatic detection of these can be complicated by voice conversations during data transmission. These off-hook functions will not be discussed here, but they may exist in the future. BELLCORE document TR-TSY-000031 "SPCS / Customer Premises Equipment Data Interface" describes the on-hook features and functions of CLASS. ADSI is described in Bellcore document TR-NWT-001273. ADSI allows for the future use of higher speed full duplex (2400 bit / s V.22bis) as the need arises in the future.

4.12.1 THE CALLER ID MESSAGE

As mentioned above, the CND data is sent by the local office's Stored Program Control Switching System (SPCS) to the Customer Premises Equipment (CPE). Bellcore document TR-TSY-000030 describes the format of the caller ID message as well as other still to be defined service messages. The CPE must have the capability to receive this CND data, meaning special circuitry must be present in order to automatically decode and display or use the message data whenever this service is required. In some cases the calling station must first enable the sending of CND data, on a call by call basis, or an activation signal may be sent to enable it until another code is sent to deactivate (block) the service.

Caller ID data is sent in Bell 202 FSK format. CCITT V.23 is very similar to Bell 202 and a V.23 receiver can also be used to decode the CND information. Silicon Systems' modem products that can be used for demodulating caller ID signals include the SSI 73M223 V.23 main channel modem, and all five of the SSI 73K3xxL series modem data pumps. This gives many choices for possible modem operating modes as well as decoding caller ID messages.

Channel Seizure Signal 250 ms010101...	Marking Carrier 150 ms	Message Type CND-00000100	Message Length In Bytes	Caller ID Message MM-DD-HH-` NNNNNNNNN	Check SUM Mod. 256
SINGLE MESSAGE FORMAT					

FIGURE 4-1. The Caller ID Message Format

Figure 1 shows the format of the caller ID message. It begins with an alternating one / zero pattern at 1200 bit / s for 250 ms. This may be detected as either the alternating data pattern or as a repeating ASCII "U" if sent to a UART. This signal conditions the receiver and gives an easily detected signal for software to detect. At the end of this period the signal changes to 150 ms of constant marks before the beginning of the data segment. Again this makes finding the beginning data's first start bit easy. As the data is received, start and stop bits should be stripped off and the remaining message stored in RAM buffer. This data is sometimes termed raw data, as opposed to cooked data, and is stored to allow analysis of the information before it is used or displayed. The term "cooked data" is sometimes used to describe the data after it has had labels added for display. A check sum is sent at the end of the data and this should be verified to assure the data has been received correctly. If it is not correct it should not be displayed or used. Caller ID may be blocked by the calling party or for other reasons, and if, a special character is sent to indicate this is the case.

4.12.2 HARDWARE REQUIREMENTS FOR CALLER ID

The first thing to consider is the requirement to remain in an on-hook condition but at the same time receive the caller information. This implies that the connection must be made such that the DC loop current does not flow and the AC impedance remains greater than 2 kΩ at 1660 Hz in order to satisfy Canadian DOC CS-03 regulations. This may be accomplished in different ways depending on the characteristics of the DAA.

FCC Part 68 and DOC CS-03 have requirements for on hook AC impedance. The FCC and DOC require that the impedance from Tip to Ring be between 10 kΩ and 40 kΩ when a ringing signal is applied which has a frequency between 15.3 Hz to 68 Hz, amplitude of 40 to 150 Vrms with a DC offset of 52.5 VDC. It is permissible to exceed the 40 Kohm maximum tip ring impedance at ringing frequencies if the device will always be in parallel with another device which meets the 40 Kohm maximum. DOC CS-03 has an additional specification (DOC CS-03 3.7.1.1 (4)) which pertains to caller ID signals. At 1660 Hz the AC impedance from Tip to Ring, with a 1 Vrms signal applied, must be greater than 2 kΩ.

The caller ID signal itself is transmitted from the central office at -13dBm. This signal consists of Bell 202 FSK signaling, using 1200 Hz for marks and 2200 Hz for spaces. The standard design criterion for minimum receive level in typical modems, when the other modem is transmitting at -9 dBm, is -43 dBm. This is a maximum loss, end to end, of 34 dB. If we assume that half of this loss is from the central office to your modem, then the maximum loss from the central office to your modem is 17 dB. Therefore the minimum caller ID signal you will see is -13 dBm - 17 dB or -30 dBm. Assuming your modem front end can receive down to -43 dBm, the maximum loss from Tip / Ring to the modem IC analog input can be 13 dB.

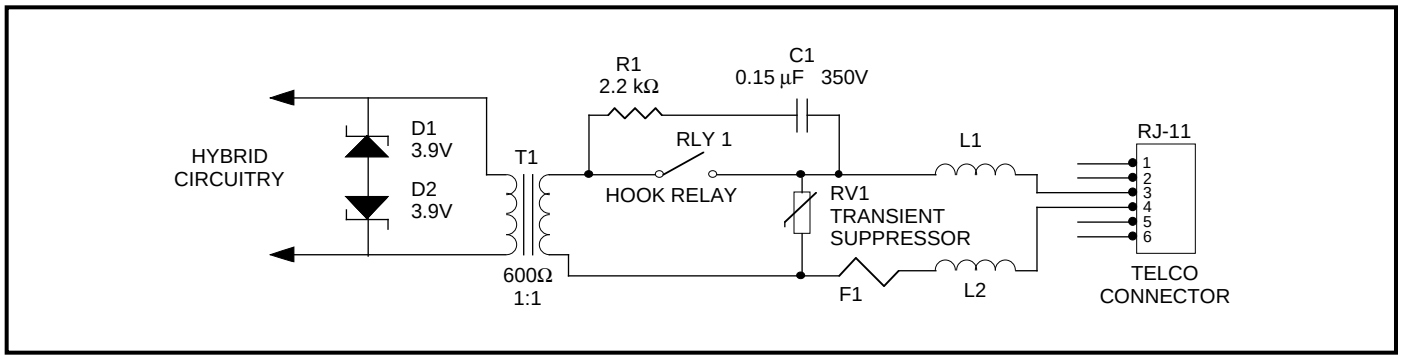


FIGURE 4-2: Snubber Network and Protection Devices for Non-Switched Caller ID

Generally it is preferable, but not required, to not couple the relatively high voltage ringing signals through to the modem. On the other hand, the additional relay required to switch in the CND receiver and coupling components can be eliminated in most cases if proper measures are taken. Ringer voltages may exceed 100 VAC on top of the 48 volt DC battery voltage. In non-CND applications there usually will be a resistor / capacitor network (or snubber) to protect the relay contacts from arcing. By substituting component values that are suitable for passing the caller ID signals, the hardware needed for CND are essentially free. Figure 2 show the necessary circuitry to receive caller ID signals and provide protection from voltage transients, but does not include ring detection. Referring to figure 2, the coupling capacitor, C1, must be able to withstand 320 V peak if used across the hook relay. The circuitry on the modem side of the transformer should be protected by clamp diodes, D1 and D2, to prevent damage to sensitive modem or analog input circuitry. This protection already exists in good designs, so there is no additional cost for these either. Additional protection from high voltages is provided by RV1 and F1. If voltages above the threshold of RV1 are applied between Tip and Ring, the suppressor will conduct and blow F1. RV1 may be any of a number of different transient suppressors including spark gap, MOVs, or Sidactors. L1 and L2 are included for FCC Part 15 EMI suppression to the telephone system.

Capacitor C1 must present a low impedance path for the Bell 202 signal in the frequency range of 1200 Hz to 2200 Hz. C1 must look like a high impedance path at the ringing frequencies of 15.3 Hz to 68 Hz in order to pass the AC on-hook impedance requirements at ringing frequencies. The maximum voltage C1 will see is the ringing voltage. If U1 is closed during ringing (which should not be the case), C1 could see as much as 150 Vrms on top of 105 VDC which is a peak voltage of 317 V.

The resistor R2 is added to satisfy the DOC CS-03 requirement for AC on-hook impedance at 1660 Hz, however it also reduces the receive level for the caller ID signal. The impedance at 1660 Hz will be, using the Aromat AQW214 opto relay, 2.45 kΩ. At 68 Hz (maximum ringing frequency) the impedance will be 15.8 kΩ.

During the first ring the modem should be prepare for the reception of the caller ID data. If the modem receiver is in power down mode it should be brought up into an active state and put into V.23 or Bell 202 mode depending on the device used. After the detection of the end of the first ring the CND receiver begins looking for the 250 ms of the alternating one/zero conditioning signal that proceeds the data. After the carrier has gone to a one or marking condition for 150 ms data begins.

This data is sent at 1200 bit/s with 8-bit characters and one start and one stop bit. TR-TSY-000030 states that the bit duration is 833 us $\pm$50 µs. A quick calculation reveals that this implies after the start bit and 8 data bits the data transitions could be greater than one half-bit period out of synch with the data. This would almost always cause errors at the receiver if data sampling were done only at the bit cell centers. This can be overcome by over sampling and resynchronization on every data transition. Although this may seem tedious, it is the best way to operate with this level of timing error.

On the other hand, ADSI has a much better timing accuracy defined in its specification. If you are an optimist, then you can use the ADSI spec as your reference document. This document states the timing error is a maximum of 12 baud or 1% for the 1200 baud signalling rate. Special Report SR-NWT-002024, dated April 1992, also states that the data rate will not vary more than 1%. This timing error cannot accumulate to a level that will cause loss of synch with the data before the end of a character. In this case only the start bit falling edge needs to be found to trigger a timer that will sample the data in the bit cell centers. After the first edge is found, a delay of one half-bit is introduced before data sampling is started continuing at a 1200 Hz rate to detect each data bit. Occasionally an oversampling technique is used to sample several times (usually 3) during the middle of the bit cell; best two out of three wins.

Section 5

SSI 73D2248 CUSTOMIZATION EXAMPLE

5 SSI 73D2248 CUSTOMIZATION EXAMPLE

The basic 73D2248 firmware implements an "AT" compatible 2400 bit/s modem with support for V.42, V.42bis and MNP 5. While this feature set should provide for a wide variety of needs, it may be desired to add features to the basic 73D2248 to differentiate it from other modems on the market.

This section describes in detail how to modify the the firmware to support "Distinctive Ringing." In order to implement this feature an additional module (RINGING.A51) was written and linked with the code provided by Silicon Systems. An additional "AT" command was added in CLI.A51 and firmware "hooks" were added to the interrupt code (INTS.A51) and the foreground loop (MAIN.A51). By studying this example, the designer should be able to write and add firmware to support many different features. A complete description of the changes made to the firmware is given below.

5.1 "DISTINCTIVE RINGING"

The Bell operating companies offer various services to customers for a small additional fee added to their phone bill. One popular service in some areas is "distinctive ringing." The service providers market this service under different names such as Ring Master (Bell South), IndentaRing (Bell Atlantic), Ring Mate (NYNEX) and Personal Ringing (Southwestern Bell). Subscribers to this service have multiple numbers assigned to a single phone line. When a call is made to this line, the subscriber can determine which number was dialed by the calling party from the cadence of the ringing. Using this service, a user could assign one number to his telephone and a second number to his modem provided the modem had a way to differentiate the rings.

Typical ringing cadences used are as follows:

Type 1: 2 seconds of continuous ringing followed by;
four seconds of silence.

Type 2: 1 second of continuous ringing followed by;
one-half second of silence followed by;
1 second of continuous ringing followed by;
3.5 seconds of silence.

Type 3: 0.4 seconds of ringing followed by;
0.2 seconds of silence followed by;
1 second of ringing followed by;
0.2 seconds of silence followed by;
0.4 seconds of ringing followed by;
3 seconds of silence.

The different ring types can be differentiated by counting the periods of continuous ringing in a "ring interval" where a ring interval is defined at the time from the onset of ringing until 1 second of silence has been detected.

In order to make use of this service, there must be a way to command the modem to only answer if a particular ringing cadence is received. The ATU command will be defined to control the distinctive ringing function as follows:

ATU0 - Normal ring detection.	Answer any type ring.
ATU1 - Distinctive ring detection.	Answer type 1 ring.
ATU2 - Distinctive ring detection.	Answer type 2 ring.
ATU3 - Distinctive ring detection.	Answer type 3 ring.

An ATU command with no parameter or an out of range parameter will cause the modem to default to normal ring detection.

In the example below, the firmware is modified to recognize different ringing cadences. The ATU command is added to select on which ringing cadences the modem will answer.

5.2 ADDING AN AT COMMAND

Adding commands to the basic AT set is straight forward. The command line interpreter is in the file CLI.A51. The table starting at label VALID_TABLE is a list of addresses for each possible ASCII value received by the command line interpreter. When the character corresponding to that value is parsed by the command line interpreter, control will pass to the address listed. In the current 73D2248 design, the "ATU" command is not used so it will be used to control distinctive ringing. There are actually two entries for the letter "U," one for upper case and one for lower case. It would be possible to have a different command for each case but, by convention, case is ignored in AT commands.

At the locations for upper and lower case "U," CMD_ERROR is replaced by CMD_U, a routine that handles the ATU command. The code for CMD_U is listed below:

```
;     FUNCTION:
;          CMD_U

;     MODIFIES:
;          temp_reg, Acc, dial_cmd, amper_cmd
;     DESCRIPTION:
;          This routine is called in response to a "U" being parsed in the command line. A test
           is made to see if the U is part of a dialing string or an AT&U command. If it is, an error
           message is sent. Otherwise, processing is passed to SetupRing.
cmd_u:
     jb    dial_cmd,cmd_u_err          ;U is not valid in dial string
     jbc        amper_cmd,cmd_u_err    ;AT&U is not a valid command
     mov        temp_reg,#0            ;default is zero
     call       get_num                ;get next number
     mov        a,temp_reg
     call       SetupRing              ;Go process this command
     jmp        cli_end                ;Now Exit
cmd_u_err:
     jmp        cli_error              ;otherwise error
cmd_u_end:
     jmp        cli_end
```

The DIAL_CMD and AMPER_CMD flags are checked to make sure that the command is not part of a dialing sequence or that the U is not preceded by an "&." Either case is considered invalid for the "U" and control will be passed to CLI_ERROR. Next the parameter for the U command is read. By convention, a decimal number can follow the U or, if the default value is desired, the next command or carriage return can follow the "U." The default of zero is written to the variable TEMP_REG and call is made to GET_NUM. This function will return the value of the parameters following the "U" in the command string in the variable TEMP_REG. If no parameters follow the "U," TEMP_REG will be unchanged.

The parameter value in TEMP_REG is copied to the A register and the function SETUPRING is called. This routine is where the distinctive ringing function is enabled and is in the RINGING.A51 file. A complete listing of the contents of that file are given in a later section.

SETUPRING first does range checking of the passed parameter. Values of 0, 1, 2 and 3 are considered valid. Other values will default to zero. The parameter is then written to a variable RINGTYPE. RAM space for this variable has been made just below the stack by adding an equate in the EQUATES.A51 module. Once this variable is written, SETUPRING will return to the caller.

5.3 MODIFYING THE RING DETECTION CODE

The next step is to modify the interrupt code that does the ring detection. Ring detection is done in two steps. A rising transition from the hardware ring detector will generate an interrupt. The following code is located in the module INTS.A51 under the label GOTR. It is not necessary to modify this section of code but an understanding of it is required to add support for distinctive ringing.

```
gotr:
        clr     exf2                    ;ring indicator
        jnb     p_hook,ex_int2_ext ;    ignore if offhook
        jb      pdial,ex_int2_ext       ;ignore if pulse dialing
        jnb     cmd_mode,ex_int2_ext    ;ignore if NOT in command mode
        jb      cnctfl,ex_int2_ext      ;ignore if online cmd mode
gotr1:
        inc     ring_qual               ;add one to ring qualification counter
        mov     ring_timer,#10          ;reset ring timer to 1 second
        setb    ring_flag               ;enable ring timer
ex_int2_ext:
        RETI
```

The interrupt is cleared by resetting the EXF2 flag. If any of the following conditions exist, the interrupt routine is exited and no further action is taken. The modem is off-hook, the modem is pulse dialing, the modem is in command mode or a connection has been made (e.g., a test mode). If none of those conditions exists, a variable called RING_QUAL is incremented by one. Next, RING_TIMER is set to expire in one second and RING_FLAG is set to enable RING_TIMER.

Provided that the conditions for valid ringing are met, every time a rising edge of the hardware ring detector occurs, one will be added to RING_QUAL and RING_TIMER will be reset to expire in 1 second. The variable RING_QUAL will be used to qualify the ringing frequency and RING_TIMER will be used to determine the end of the ring interval.

Ring qualification occurs in the same module just under the label T_RING until the label T_100MS_3. The general purpose timer generates interrupts that are used to perform various time keeping functions in the modem. The code under the T_RING label will be executed once every 100 ms. The existing code will be replaced by the following code fragment:

```
T_ring:
        jnb     ring_flag,t_100ms_3     ;did we get a ring interrupt ?
        call    DetectRing              ;do ring processing
T_100MS_3:
```

If RING_FLAG is set then the function DETECTRING (see RINGING.A51) is called to determine if valid ringing energy is present. Note that RING_FLAG is set by the routine described above whenever a rising edge on the ring detect hardware occurs and the conditions for ringing are valid.

DETECTRING updates the variable RING_TIMER by subtracting one from it every time this function is called. Since DETECTRING is called ten times per second after ringing has been detected and RING_TIMER is set to 10, RING_TIMER will expire after one second of silence. The timer is checked for zero under the COUNTRINGS label and the foreground loop will be notified of a ring interval when this occurs.

A state machine is also implemented in the DETECTRING function. The variable RINGSTATE contains the current state. States are defined as follows:

0 - Idle State

10 - Energy detected for 100 ms

20 - Energy detected for 200 ms

1 - Energy detected for 300 ms

2 - Silence detected for 100 ms

3 - 2nd ringing period for at least 100 ms

4 - 2nd silence period for at least 100 ms

5 - 3rd ringing period for at least 100 ms

6 - 3rd silence period for at least 100 ms

States 10, 20, and 1 are used for noise immunity to protect against false rings. At least 300 ms of continuous ringing must be present before a valid ring is detected. Of the remaining states, even states indicate a silence period and odd states indicate a ringing period. Since the end of a ring interval is defined as 1 second of silence and the foreground will not be signaled until the end of the ring period, the state machine will always be at an even state at the end of the ringing period. The ring type is determined by dividing RINGSTATE by two.

Each time DETECTRING is called, it must determine if ringing energy was present during the last 100 ms interval. This is done using the variable RING_QUAL. RING_QUAL contains the number of rising edges detected by the ring detect hardware during the last 100 ms. If four or more edges were detected during the last 100 ms period, valid energy is considered present. Otherwise, no ringing energy is considered present. RING_QUAL is cleared every time DETECTRING is exited.

The variable RINGING is used to signal the foreground loop that the end of ringing interval has occurred. The modification to the foreground loop in MAIN.A51 is shown below.

```
monitor:
                                    ; monitors data pump
    jbc     ringing,mon_ring        ;check for ringing
    mov     r0,#tmr_s1
    mov     a,@r0                   ;no rings so check ring timer
    jnz     mon_no_ring
    mov     @r0,#8                  ;reset ring timer to 8 seconds
    mov     a,#0
    %put_sfr(1)                     ;reset sfr_1 to 0
mon_no_ring:
    ljmp  mon_0                     ;if no ring then continue...

mon_ring:                           ;GOT RING...
    %xread(rtn_code)                ;check for connection
    jnz     mon_no_ring             ;if so skip ring result
    mov     r0,#tmr_s1
    mov     @r0,#8                  ;reset ring timer to 8 seconds
    call    TestRing                ;support for distinctive ringing
    jnz     mon_no_ring             ;non-zero indicates not valid ring
    %inc_sfr(1)                     ;increment the ring counter
    jb    a_found,mon_ring2
    call    init_uart               ;if a not found then set up uart
mon_ring2:
```

The foreground loop will test RINGING to determine if a ring has been detected. If RINGING is set, a call is made to the function TESTRING. If TESTRING returns a zero, one is added to the S1 register and a ring result code is sent to the DTE.

TESTRING in RINGING.A51 checks the received ring type compared with the valid rings in RINGTYPE. Remember that RINGTYPE is set by the "ATU" command. If RINGTYPE is set to zero (default), any ring type is valid and zero is returned to the caller. If RINGTYPE is non-zero, its value is compared against RINGTYPE divided by two (shift right one bit). If the values compare, a zero value is returned indicating a ring. If the values do not compare, a non-zero value is returned.

Section 6

RINGING

6 RINGING.A51

```
;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;
;
;     MODULE: RINGING.A51
;
;     AUTHOR: CLIFF BROWN
;
;     REVISION HISTORY: Created May 22, 1991
;
;     This file contains the functions necessary to support "Distinctive Ringing" detection by the
;     73D2247 modem. Many of the Bell operating companies offer a service where multiple
;     phone numbers can be assigned to a single phone line. When a call is made to a
;     subscriber of this service, the cadence of the ringing identifies the number dialed.
;     Typically, three different ringing cadences are used:
;
;     1.    One long ring followed by approximately four seconds of silence
;     2.    Two short rings followed by approximately four seconds of silence
;     3.    Three short rings followed by approximately four seconds of silence
;
;     The type of incoming ring can be determined by the number of "Rings" in a ringing period.
;     For ease in implementing the detection algorithm, a ringing period will be defined as the
;     time from the onset of ringing until one second of continuous silence (no ringing) has been
;     detected. Three subroutines will be added to the 73D2247 to support this new feature:
;
;     DetectRing   -   Used to detect valid ringing energy and count the number of rings in
;                      a ringing period.
;     TestRing     -   Determines if the distinctive ringing feature is enabled and, if so,
;                      determines if the ringing type received is the one currently being
;                      detected.
;     SetupRing    -   Enables and disables distinctive ringing capability and allows
;                      selection of the type of ring detected.
;
;     DetectRing must be called in response to an edge on the external interrupt 2 input. This
;     line is connected to a opto-isolator that will generate an edge on every cycle of the ringing
;     signal. In the INTS.A51 file, a call to this subroutine is made just under the label "T_ring"
;     if potential ringing energy was detected.
;
;     TestRing is called from MAIN.A51 every time DetectRing signals the foreground loop that
;     valid ringing energy was detected. A call to this routine is made near the label "monitor."
;     SetupRing is called as a result of the appropriate "AT" command being parsed in the
;     command buffer. For this example ATU is used. In CLI.A51 a table of all the possible
;     commands and the address of the routine to process that command is given. A call to
;     CMD_U is made which first determines that the command is "ATU" and not "AT&U" and
;     then calls SetupRing.
;
$NOLIST
$INCLUDE(ASSEMOPS.A51)        ;ASSEMBLY OPTIONS
$INCLUDE(RG51FA.PDF)          ;PIN DEFINITIONS FOR 73D630/631
$include(equates.a51)
$INCLUDE(MACROS.A51)          ;Macro definitions
$LIST

        ring_seg segment code
        rseg ring_seg
        public DetectRing,TestRing,SetupRing
        extrn code(send_value,send_crlf)
```

```
;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;
;
;
;       FUNCTION:
;             DetectRing( ) : Ring Detected[ringing]
;
;       MODIFIES:
;             A,R1,RingState,ring_timer,ring_qual,ring_flag,p_ri
;
;       DESCRIPTION:
;             This function should be called every 100 ms if ring_flag is true. This portion of the
;             code detects and processes ringing signals. A provision has been added to count
;             the number of "rings" received during any ringing period. A ringing is defined at the
;             time that ringing energy is first detected until one second of silence is detected. Some
;             services provided by the phone company will generate different ringing cadences
;             depending on the number dialed or the number from which the calling party is dialing
;             (distinctive ringing). The code below counts the number of rings in each period in a
;             variable called RingState. Note also that the RI line will follow the ringing cadence.
;             The variable ringing' will be set any time a valid ring signal is detected (any type)
;
DetectRing:
      dec     ring_timer          ;update ring timer
      mov     r1,#ringState       ;point to ringState variable
      mov     a,@r1               ;read ringState variable
      anl     a,#0fh              ;ignore most significant four bits
      jnz     countRings          ;if not in idle state go count
                                  ;the number of rings this interval
      mov     a,@r1               ;read ringState variable again
      cjne    a,#0,detRng1        ;test for state 0
      mov     @r1,#10h            ;next initial detect state
      jmp     lookRingEng         ;go look for ring energy
detRng1:
      cjne    a,#10h,detRng2      ;test for state 10 hex
      mov     @r1,#20h            ;next initial detect state
      jmp     ookRingEng          ;go look for ring energy
detRng2:
      cjne    a,#20h,detRng3      ;test for state 20 hex
      mov     @r1,#1h             ;valid energy detected for 300 ms
lookRingEng:
      mov     a,ring_qual         ;get number of ring interrupts
      cjne    a,#3,testRingQual   ;see if more than 3
testRingQual:
      jnc     validRing           ;jump if 300 ms of valid ring energy
detRng3:
      mov     @r1,#0h             ;reset state machine
      setb    p_ri                ;clear ri (rs-232 line)
      clr     ring_flag           ;disable ring_timer
      jmp     exitRing            ;leave routine
validRing:
      clr     p_ri                ;set ri to indicate ringing
      jmp     exitRing            ;finish ring processing
countRings:
      mov     a,ring_timer        ;see if no ring energy for 1 second
      jz      sendRingResult      ;signal foreground of ring
      mov     a,@r1               ;get ringState
      jb      acc.0,ringEnergy    ;odd states mean ring energy
noRingEnergy:
      mov     a,ring_qual         ;see if there is ring energy
      cjne    a,#3,testNoEnergy
testNoEnergy:
      jc      exitRing            ;no energy, don't change state
      clr     p_ri                ;indicate ringing
      inc     @r1                 ;update ringState
      jmp     exitRing            ;initialize ring_qual and leave
ringEnergy:
      mov     a,ring_qual         ;get # of ring interrupts
      cjne    a,#3,testRingQual2  ;see if <= 3
testRingQual2:
      jnc     exitRing            ;ringing energy, don't change state
      setb    p_ri                ;indicate not ringing
      inc     @r1                 ;next ring state
      jmp   exitRing              ;cleanup and leave function
```

```
sendRingResult:
      etb        inging                 ;inform foreground of ring
      clr        ring_flag              ;disable ring_timer
exitRing:
      mov        ring_qual,#0           ;reset ring interrupt counter
      ret                               ;return to the caller
;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;
;
;     FUNCTION:
;           TestRing( ) : valid ring[Acc]
;
;     MODIFIES:
;
;     DESCRIPTION:
;     This code determines if distinctive ring has been enabled and, if so, if the ring received is
;     of the specified ring type. The accumulator will contain zero if the desired ring type has
;     been detected and a non-zero value otherwise.
;     TestRing:
;           mov        r1,#RingType         ;point to the ringType variable
;           mov        A,@r1                ;read the ring type
;           jnz        checkRingType        ;if Distinctive Ringing Enable, jump
;           mov        ,#0                  ;indicate valid ring
;           jmp  exitTestRing               ;return to caller
;     checkRingType:
;           mov r1,#RingState               ;point to RingState
;           mov a,@r1                       ;read RingState
;           mov r1,#RingState               ;point to RingState
;           mov @r1,#0                      ;clear RingState
;           clr   c                         ;clear carry flag
;           rrc   a                         ;RingState divided by 2 equals the
;                                           ;received ring type
;           mov r1,#RingType                ;point to ringType
;           xrl   ,@r1                      ;test for equality
;     exitTestRing:
;           ret                             ;zero for valid ring
;                                           ;non-zero otherwise

;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;
;
;     FUNCTION:
;           SetupRing( Ring Type[Acc] )
;     MODIFIES:
;           A, R1, RingType
;     DESCRIPTION:
;           Sets the RingType variable to the value passed in the accumulator. The value must
;           be less than four or RingType will be set to zero.
SetupRing:
            cjne  a,#4,testRange       ;Acc must contain 0, 1, 2 or 3
testRange:
            jc    setRingType          ;if valid, jump
            clr   a                    ;otherwise, disable distinctive ringing
setRingType:
            mov r1,#RingType           ;point to RingType
            mov @r1,a                  ;set RingType
            ret                        ;return to caller
;
;*****************************************************************************************************
;     Copyright, 1988,1989,1990 Silicon Systems, inc. All rights reserved.
;     This program is fully protected by the United States copyright
;     laws and is the property of Silicon Systems, incorporated.
;*****************************************************************************************************
END
```

Section 7

APPENDIX

7 APPENDIX I

TECHNICAL SPECIFICATIONS

300, 1200, 2400 BIT/S SPECIFICATIONS

Input Data Format	:	Serial, binary, character asynchronous
Dialer Type	:	Rotary Pulse or DTMF Tone
Dial Pulse Rate	:	10 pulses per second ± 10%
Pulse Dial Duty Cycle	:	61% ± 3% (percent break)
Pulse Dialing Interdigit Delay	:	750 ± 50 ms
DTMF Tone Duration	:	70 ms ± 5 ms (see register S11)
Tone Dialing Interdigit Delay	:	70 ms ± 5 ms (refer to register S11)
Command Buffer	:	40 characters
Audio Monitor	:	Programmable volume

1200 BIT/S SPECIFICATIONS

1200 bit / s (Bell 212A)	:	Four Level Differential Phase Shift Keyed
1200 bit / s (CCITT V.22)	:	(DPSK) or its equivalent Quadrature Amplitude Modulation (QAM).
Input Data Rate	:	1170 - 1212 bit / s
	:	Bell 212A 1170 - 1212 bit / s
Line Data Rate	:	CCITT V.22 1200 bit / s ± 0.01%
	:	Bell 212A 1200 bit / s ± 0.01%
Carrier Frequencies	:	Originate Mode: 1200 Hz ± 0.01%
	:	Answer Mode: 2400 Hz ± 0.01%

2400 BIT/S SPECIFICATIONS

2400 bit / s	:	Quadrature Amplitude Modulation (QAM) (CCITT V.22bis)
Input Data Rate	:	2340 - 2424 bit / s
Line Data Rate	:	CCITT V.22bis 2400 bit / s ± 0.01%
Carrier Frequencies	:	Originate Mode: 1200 Hz ± 0.01%
	:	Answer Mode: 2400 Hz ± 0.01%

APPENDIX FACTORY PROFILE SUMMARY

In the following table, the "Saved in memory" column lists which AT commands and S-Registers can be saved in non-volatile memory.

Factory Profile Configuration

Saved in Memory		Default
YES	Bell 212A (1200) and 103 (300) mode	B1
YES	Command Echo ON	E1
YES	Speaker volume set to medium	L2
YES	Speaker enabled; OFF when CD TRUE	M1
YES	Pulse dialing enabled	P
YES	All result codes enabled and reported	Q0
YES	Full word (verbal) result codes	V1
YES	Detects busy signal	X4
YES	Waits for dial tone before dialing	X4
YES	Long Space Disconnect disabled	Y0
YES	CD true during presence of Carrier Signal	&C1
YES	DTR OFF = off-hook, no Auto-Answer, command state	&D2
YES	Pulse dial make/break ratio = 39/61 (US)	&P0
YES	No guard tones generated	&G0
YES	Local modem will grant RDL test request	&T4
YES	Auto-Answer mode disabled	S0=0
NO	Ring Count = 0	S1=0
NO	Escape code character = 43	S2=43
NO	Carriage return character = 13	S3=13
NO	Line feed character = 10	S4=10
NO	Back space character = 8	S5=8
NO	Wait time for dial tone = 2 seconds	S6=2
YES	Wait for CD after dialing = 30 seconds	S7=30
NO	Wait time of pause (comma) = 2 seconds	S8=2
YES	Carrier detect response time = .6 seconds	S9=6
YES	Lost Carrier hang-up delay = 1.4 seconds	S10=14
YES	Tone dial spacing = 70 milliseconds	S11=70
YES	Escape code guard time = 1 second	S12=50
NO	Test modes disabled	S16=0
YES	Test timer = 0	S18=0
YES	DTR detect delay = .05 seconds	S25=5
YES	Modem Line Speed	S37=0

APPENDIX II RS-232 PIN ASSIGNMENTS

To connect your modem to your terminal, printer or computer, you need a standard male EIA RS-232C cable.

A shielded EIA RS-232C cable can be used in order to help comply with FCC part 15 class B requirements.

EIA RS-232C cable wiring to the 73D2248 serial interface is based on the EIA RS-232C specifications for Data Communications Equipment (DCE). Almost all terminal and computer asynchronous serial ports intended for connection to a modem follow the EIA RS-232C specification for Data Terminal Equipment (DTE).

When 25-pin DB-25 type connectors are on both the modem (DCE) and the terminal or computer (DTE), you can usually connect them with a "straight through" EIA RS-232C serial cable. That is, pin 1 on the DCE end is connected to pin 1 on the DTE end, and the same follows for each of the other pins.

While IBM PC, PC / XT, PS / 2 and compatible computers usually have 25-pin connectors for their RS-232C serial ports, the IBM AT, some AT compatible computers, and some third party plug-in boards use a 9-pin DB-9 connector for their serial port. This is acceptable since you can usually establish full communications while using 9 or fewer of the EIA RS-232C specified signals. When connecting a 9-pin serial port on an IBM AT to your modem, you will need an adapter to mate the 9-pin connector to the 25-wire cable. They are readily available from computer supply retailers and mail order suppliers.

There may be occasions when the above advice is not sufficient to describe the serial cable you need for your exact hardware configuration. The following detailed description of the EIA RS-232C serial interface should allow you to construct the serial cable you require.

EIA RS-232C Signal Connections

PIN	Description			
1	Protective Gnd (GND)	AA	101	N / A
2	Transmitted Data (TD)	BA	103	INPUT
3	Received Data (RD)	BB	104	OUTPUT
4	Request To Send (RTS)	CA	105	INPUT
5	Clear To Send (CTS)	CB	106	OUTPUT
6	Data Set Ready (DSR)	CC	107	OUTPUT
7	Signal Ground (SG)	AB	102	N / A
8	Carrier Detect (CD)	CF	109	OUTPUT
9	Not connected			
10	Not connected			
11	Not connected			
12	Speed Indications	CI	122	OUTPUT
13	Not connected			
14	Not connected			
15	Xmit Signal Timing (DCE)	DB	114	OUTPUT
16	Not connected			
17	Receive Signal Timing	DD	115	OUTPUT
18	Not connected			
19	Not connected			
20	Data Terminal Ready (DTR)	CD	108 / 2	INPUT
21	Not connected			
22	Ring Indicator (RI)	CE	125	OUTPUT
23	Not connected			
24	Xmit Signal Timing (DTE)	DA	113	NPUT
25	Not connected			

In the signal descriptions below, DTE (Data Terminal Equipment) refers to your local computer or terminal and DCE (Data Communications Equipment) refers to your 73D2248 modem. The pin numbers refer to a DB-25 connector.

Pin 1: Protective Ground (AA)

Protective Ground is connected to the equipment chassis and the power cord ground terminal.

Pin 2: Transmitted Data (BA)

Serial data transmitted from the terminal or computer to the 73D2248 modem.

Pin 3: Received Data (BB)

Serial data transmitted from the 73D2248 modem to the terminal or computer.

Pin 4: Request To Send (CA)

In asynchronous mode, RTS is always ignored. In synchronous mode, the &R[n] command defines how the modem uses RTS and CTS. &R1 causes the modem to ignore RTS. In data state, &R0 causes the modem to sense an OFF to ON transition of RTS, wait a period of time defined by register S26, and then turn CTS ON. During command state, with &R0 in effect, the modem ignores RTS. In protocol modes, RTS performs the function of flow control for the modem receiver.

Pin 5: Clear To Send (CB)

In asynchronous mode, CTS is always ON. In synchronous mode command state, CTS is ON. CTS is turned OFF when the modem goes off-hook. If the &R1 command is in effect, CTS will be turned back ON when both DCD and DSR are ON and the modem is ready to transmit and receive synchronous data. If the &R0 command is in effect, CTS is turned ON when an OFF to ON transition of RTS is sensed and the register S26 delay has been executed. In protocol modes, CTS is output by the modem to provide flow control for the modem transmitter.

Pin 6: Data Set Ready (CC)

In asynchronous mode, the use of the DSR signal is controlled by the &S[n] command. &S0 causes DSR to always be ON. &S1 causes DSR to turn ON when the modem goes off-hook, and back OFF when the modem goes on-hook. With &S1 in effect, when the remote modem disconnects from the line, the local modem will also disconnect and turn DSR OFF.

In synchronous mode, DSR always operates as described above for the &S1 command (regardless of the actual state of the &S[n] command).

Pin 7: Signal Ground (AB)

Is the common electrical ground reference for all data and control signals.

Pin 8: Data Carrier Detect (CF)

In asynchronous mode, the &C[n] command defines how the modem uses the DCD signal. &C0 causes DCD (sometimes referred to as CD) to always be ON. &C1 causes DCD to be ON only when a valid carrier signal from the remote modem is detected by the modem.

In synchronous mode, DCD is ON only when a valid carrier signal from the remote modem is detected by the modem (&C[n] is ignored).

Pin 12: Speed Indication (CI)

The output signal CI (Speed Indication) is ON when the 73D2248 modem is communicating at 2400 bit / s. The CI signal remains ON after termination of a 2400 bit / s communication. The CI signal is ON after the modem is powered ON. The CI signal is turned OFF when a 1200 bit / s (or lower rate) operation is begun.

Pin 15: Transmit Signal Timing, DCE (DB)

The output signal Transmit Signal Timing (DCE source) is used in synchronous mode only. The 73D2248 uses this signal to tell the DTE (computer or terminal) to transfer the next bit of data to the modem on EIA RS-232C pin 2.

Pin 17: Receive Signal Timing (DD)

The output signal Receive Signal Timing is used in synchronous mode only. This signal is derived by the 73D2248 from the incoming synchronous data. The 73D2248 uses this signal to tell the DTE (computer or terminal) to receive the next bit of data being transferred from the modem to the DTE equipment on EIA RS-232C pin 3.

Pin 20: Data Terminal Ready (CD)

The DTR (Data Terminal Ready) input signal can be used in many different ways by the 73D2248 modem. Refer to the explanation of the &D[n] command for uses of DTR.

Pin 22: Ring Indicator (CI)

The output signal RI (Ring Indicator) is true when a ring signal is present on the phone line.

Pin 24: Transmit Signal Timing, DTE (DA)

The input signal Transmit Signal Timing (DTE source) is used in synchronous mode only. Its leading edge can be used by the local DTE (terminal or computer) to tell the local modem to send the next bit of data, currently on EIA RS-232C pin 2, to the remote modem.

CONTINUOUS IMPROVEMENT MISSION & OBJECTIVE STATEMENT

Mission

Be the supplier of choice by exceeding customer expectations through continuous improvements in our products, systems and services.

Objectives

Provide world class quality in our products and services through focus on:

Customer Partnering
Cycle Time Improvement
Process and System Improvements

Develop a culture that ensures the consistent use of continuous improvement tools and fact based decision methodology by:

Senior Management Leadership
Employee Empowerment
Aggressive Goal Setting and Performance Measurement
Communication and Celebration of Successes

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