## FEATURES

- Operate From 1.65 V to 3.6 V
- Inputs Accept Voltages to 5.5 V
- Max $\mathrm{t}_{\mathrm{pd}}$ of 7.4 ns at 3.3 V
- Typical $\mathrm{V}_{\text {olp }}$ (Output Ground Bounce)
$<0.8$ at $\mathrm{V}_{\mathrm{cC}}=3.3 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$
- Typical $\mathrm{V}_{\mathrm{OHV}}$ (Output $\mathrm{V}_{\mathrm{OH}}$ Undershoot)
$>2 \mathrm{~V}$ at $\mathrm{V}_{\mathrm{CC}}=3.3 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$
- Support Mixed-Mode Signal Operation on All Ports (5-V Input/Output Voltage With $3.3-\mathrm{V} \mathrm{V}_{\mathrm{cc}}$ )

SN54LVC646A...JT OR W PACKAGE SN74LVC646A... DB, DW, NS, OR PW PACKAGE (TOP VIEW)

| CLKAB | $1 \cup_{24}$ | $\mathrm{V}_{\mathrm{CC}}$ |
| :---: | :---: | :---: |
| SAB | 23 | CLKBA |
| DIR 3 | 322 | SBA |
| A1 4 | 421 | OE |
| A2 5 | 520 | B1 |
| A3 6 | 619 | B2 |
| A4 7 | 718 | B3 |
| A5 8 | $8 \quad 17$ | B4 |
| A6 9 | $9 \quad 16$ | B5 |
| A7 | $10 \quad 15$ | B6 |
| A8 | $11 \quad 14$ | B7 |
| GND | $12 \quad 13$ | B8 |

- $\mathrm{I}_{\text {off }}$ Supports Partial-Power-Down Mode Operation
- Latch-Up Performance Exceeds 250 mA Per JESD 17
- ESD Protection Exceeds JESD 22
- 2000-V Human-Body Model (A114-A)
- 200-V Machine Model (A115-A)
- 1000-V Charged-Device Model (C101)


NC - No internal connection

## DESCRIPTION/ORDERING INFORMATION

The SN54LVC646A octal bus transceiver and register is designed for $2.7-\mathrm{V}$ to $3.6-\mathrm{V} \mathrm{V}_{\mathrm{CC}}$ operation, and the SN74LVC646A octal bus transceiver and register is designed for $1.65-\mathrm{V}$ to $3.6-\mathrm{V} \mathrm{V}_{\mathrm{CC}}$ operation.

ORDERING INFORMATION

| TA | PACKAGE ${ }^{(1)}$ |  | ORDERABLE PART NUMBER | TOP-SIDE MARKING |
| :---: | :---: | :---: | :---: | :---: |
| $-40^{\circ} \mathrm{C}$ to $85^{\circ} \mathrm{C}$ | SOIC - DW | Tube of 25 | SN74LVC646ADW | LVC646A |
|  |  | Reel of 2000 | SN74LVC646ADWR |  |
|  | SOP - NS | Reel of 2000 | SN74LVC646ANSR | LVC646A |
|  | SSOP - DB | Reel of 2000 | SN74LVC646ADBR | LC646A |
|  | TSSOP - PW | Tube of 60 | SN74LVC646APW | LC646A |
|  |  | Reel of 2000 | SN74LVC646APWR |  |
|  |  | Reel of 250 | SN74LVC646APWT |  |
| $-55^{\circ} \mathrm{C}$ to $125^{\circ} \mathrm{C}$ | CDIP - JT | Tube of 15 | SNJ54LVC646AJT | SNJ54LVC646AJT |
|  | CFP - W | Tube of 85 | SNJ54LVC646AW | SNJ54LVC646AW |
|  | LCCC - FK | Tube of 42 | SNJ54LVC646AFK | SNJ54LVC646AFK |

(1) Package drawings, standard packing quantities, thermal data, symboliztion, and PCB design guidelines are available at www.ti.com/sc/package. WITH 3-STATE OUTPUTS

## DESCRIPTION/ORDERING INFORMATION (CONTINUED)

These devices consist of bus-transceiver circuits, D-type flip-flops, and control circuitry arranged for multiplexed transmission of data directly from the input bus or from the internal registers. Data on the A or B bus is clocked into the registers on the low-to-high transition of the appropriate clock (CLKAB or CLKBA) input. Figure 1 illustrates the four fundamental bus-management functions that are performed with the 'LVC646A devices.

Output-enable ( $\overline{\mathrm{OE}}$ ) and direction-control (DIR) inputs control the transceiver functions. In the transceiver mode, data present at the high-impedance port is stored in either register or in both.
The select-control (SAB and SBA) inputs can multiplex stored and real-time (transparent mode) data. DIR determines which bus receives data when $\overline{\mathrm{OE}}$ is low. In the isolation mode ( $\overline{\mathrm{OE}}$ high), A data is stored in one register and B data can be stored in the other register.

When an output function is disabled, the input function still is enabled and can be used to store and transmit data. Only one of the two buses, A or B, can be driven at a time.
Inputs can be driven from either $3.3-\mathrm{V}$ or $5-\mathrm{V}$ devices. This feature allows the use of these devices as translators in a mixed $3.3-\mathrm{V} / 5-\mathrm{V}$ system environment.
These devices are fully specified for partial-power-down applications using $\mathrm{I}_{\text {off }}$. The $\mathrm{I}_{\text {off }}$ circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.
To ensure the high-impedance state during power up or power down, $\overline{O E}$ should be tied to $\mathrm{V}_{\mathrm{CC}}$ through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

FUNCTION TABLE

| INPUTS |  |  |  |  |  | DATA I/O |  | OPERATION OR FUNCTION |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| $\overline{O E}$ | DIR | CLKAB | CLKBA | SAB | SBA | A1-A8 | B1-B8 |  |
| X | X | $\uparrow$ | X | X | X | Input | Unspecified ${ }^{(1)}$ | Store A, B unspecified ${ }^{(1)}$ |
| X | X | X | $\uparrow$ | X | X | Unspecified ${ }^{(1)}$ | Input | Store B, A unspecified ${ }^{(1)}$ |
| H | X | $\uparrow$ | $\uparrow$ | X | X | Input | Input | Store and B data |
| H | X | H or L | H or L | X | X | Input disabled | Input disabled | Isolation, hold storage |
| L | L | X | X | X | L | Output | Input | Real-time B data to A bus |
| L | L | X | H or L | X | H | Output | Input | Stored B data to A bus |
| L | H | X | X | L | X | Input | Output | Real-time $A$ data to $B$ bus |
| L | H | H or L | X | H | X | Input | Output | Stored A data to B bus |

(1) The data-output functions can be enabled or disabled by various signals at $\overline{O E}$ and DIR. Data-input functions always are enabled; i.e., data at the bus terminals is stored on every low-to-high transition of the clock inputs.


Figure 1. Bus-Management Functions


Pin numbers shown are for the DB, DW, JT, NS, PW, and W packages.

SN54LVC646A, SN74LVC646A
INSTRUMENTS
www.ti.com

## Absolute Maximum Ratings ${ }^{(1)}$

over operating free-air temperature range (unless otherwise noted)

|  |  |  | MIN | MAX | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: |
| $\mathrm{V}_{\mathrm{CC}}$ | Supply voltage range |  | -0.5 | 6.5 | V |
| $V_{1}$ | Input voltage range ${ }^{(2)}$ |  | -0.5 | 6.5 | V |
| $\mathrm{V}_{0}$ | Voltage range applied to any outpur | wer-off state ${ }^{(2)}$ | -0.5 | 6.5 | V |
| $\mathrm{V}_{0}$ | Voltage range applied to any outpur |  | -0.5 | $\mathrm{V}_{\mathrm{CC}}+0.5$ | V |
| $\mathrm{I}_{\mathrm{IK}}$ | Input clamp current | $\mathrm{V}_{1}<0$ |  | -50 | mA |
| $\mathrm{I}_{\text {OK }}$ | Output clamp current | $\mathrm{V}_{\mathrm{O}}<0$ |  | -50 | mA |
| $\mathrm{l}_{0}$ | Continuous output current |  |  | $\pm 50$ | mA |
|  | Continuous current through $\mathrm{V}_{\mathrm{CC}}$ |  |  | $\pm 100$ | mA |
|  |  | DB package |  | 63 |  |
|  | Package thermal impedance ${ }^{(4)}$ | DW package |  | 46 | ${ }^{\circ} \mathrm{C} / \mathrm{W}$ |
| $ө^{\text {JA }}$ | Package thermal impedance ${ }^{(4)}$ | NS package |  | 65 | O, |
|  |  | PW package |  | 88 |  |
| $\mathrm{T}_{\text {stg }}$ | Storage temperature range |  | -65 | 150 | ${ }^{\circ} \mathrm{C}$ |

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.
(3) The value of $\mathrm{V}_{\mathrm{Cc}}$ is provided in the recommended operating conditions table.
(4) The package thermal impedance is calculated in accordance with JESD 51-7.

Recommended Operating Conditions ${ }^{(1)}$

(1) All unused inputs of the device must be held at $\mathrm{V}_{\mathrm{CC}}$ or GND to ensure proper device operation. Refer to the TI application report, Implications of Slow or Floating CMOS Inputs, literature number SCBA004.

## Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

(1) All typical values are at $\mathrm{V}_{\mathrm{CC}}=3.3 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$.
(2) For I/O ports, the parameter IOz includes the input leakage current.
(3) This applies in the disabled state only.

## Timing Requirements

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 2)

|  |  |  | SN4L | 46A |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | $\mathrm{V}_{\mathrm{cc}}$ |  | $\mathrm{v}_{\mathrm{cc}}$ |  | UNIT |
|  |  | MIN | MAX | MIN | MAX |  |
| $\mathrm{f}_{\text {clock }}$ | Clock frequency |  | 150 |  | 150 | MHz |
| $\mathrm{t}_{\mathrm{w}}$ | Pulse duration | 3.3 |  | 3.3 |  | ns |
| $\mathrm{t}_{\text {su }}$ | Setup time, data before CLK $\uparrow$ | 1.6 |  | 1.5 |  | ns |
| $\mathrm{t}_{\mathrm{h}}$ | Hold time, data after CLK $\uparrow$ | 1.7 |  | 1.7 |  | ns |

## Timing Requirements

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 2)

(1) This information was not available at the time of publication.

## Switching Characteristics

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 2)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | SN54LVC646A |  |  | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  |  | $\mathrm{V}_{\mathrm{CC}}=2.7 \mathrm{~V}$ | $\begin{gathered} \mathrm{V}_{\mathrm{CC}}=3.3 \mathrm{~V} \\ \pm 0.3 \mathrm{~V} \end{gathered}$ |  |  |
|  |  |  | MIN MAX | MIN | MAX |  |
| $\mathrm{f}_{\text {max }}$ |  |  | 150 | 150 |  | MHz |
| $\mathrm{t}_{\mathrm{pd}}$ | A or B | B or A | 7.9 | 1 | 7.4 | ns |
|  | CLK | $A$ or B | 8.8 | 1 | 8.4 |  |
|  | SBA or SAB |  | 9.9 | 1 | 8.6 |  |
| $\mathrm{t}_{\text {en }}$ | OE | A | 10.2 | 1 | 8.2 | ns |
| $\mathrm{t}_{\text {dis }}$ | $\overline{\mathrm{OE}}$ | A | 8.9 | 1 | 7.5 | ns |
| $\mathrm{t}_{\text {en }}$ | DIR | B | 10.4 | 1 | 8.3 | ns |
| $\mathrm{t}_{\text {dis }}$ | DIR | B | 8.7 | 1 | 7.9 | ns |

## Switching Characteristics

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 2)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | SN74LVC646A |  |  |  |  |  |  |  | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  |  | $\begin{gathered} \mathrm{V}_{\mathrm{cc}}=1.8 \mathrm{~V} \\ \pm 0.15 \mathrm{~V} \end{gathered}$ |  | $\begin{gathered} \mathrm{V}_{\mathrm{cc}}=2.5 \mathrm{~V} \\ \pm 0.2 \mathrm{~V} \end{gathered}$ |  | $\mathrm{V}_{\mathrm{cc}}=2.7 \mathrm{~V}$ |  | $\begin{gathered} \mathrm{V}_{\mathrm{CC}}=3.3 \mathrm{~V} \\ \pm 0.3 \mathrm{~V} \end{gathered}$ |  |  |
|  |  |  | MIN | MAX | MIN | MAX | MIN | MAX | MIN | MAX |  |
| $\mathrm{f}_{\text {max }}$ |  |  | (1) |  | (1) |  | 150 |  | 150 |  | MHz |
| $\mathrm{t}_{\mathrm{pd}}$ | A or B | $B$ or $A$ | (1) | (1) | (1) | (1) |  | 7.9 | 1 | 7.4 | ns |
|  | CLK | A or B | (1) | (1) | (1) | (1) |  | 8.8 | 1 | 8.4 |  |
|  | SBA or SAB |  | ${ }^{(1)}$ | (1) | (1) | (1) |  | 9.9 | 1 | 8.6 |  |
| $\mathrm{t}_{\mathrm{en}}$ | OE | A | (1) | (1) | (1) | (1) |  | 10.2 | 1 | 8.2 | ns |
| $\mathrm{t}_{\text {dis }}$ | OE | A | (1) | (1) | (1) | (1) |  | 8.9 | 1 | 7.5 | ns |
| $\mathrm{t}_{\text {en }}$ | DIR | B | (1) | (1) | (1) | (1) |  | 10.4 | 1 | 8.3 | ns |
| $\mathrm{t}_{\text {dis }}$ | DIR | B | ${ }^{(1)}$ | (1) | (1) | (1) |  | 8.7 | 1 | 7.9 | ns |

(1) This information was not available at the time of publication.

SN54LVC646A, SN74LVC646A
OCTAL BUS TRANSCEIVERS AND REGISTERS
WITH 3-STATE OUTPUTS
SCAS302J-JANUARY 1993-REVISED AUGUST 2005

## Operating Characteristics

$\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$

| PARAMETER |  |  | TEST CONDITIONS | $\mathrm{V}_{\mathrm{CC}}=1.8 \mathrm{~V}$ | $\mathrm{V}_{\mathrm{CC}}=2.5 \mathrm{~V}$ | $\mathrm{V}_{\mathrm{cc}}=3.3 \mathrm{~V}$ | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  |  | TYP | TYP | TYP |  |
| Cpd | Power dissipation capacitance per transceiver | Outputs enabled |  | $\mathrm{f}=10 \mathrm{MHz}$ | (1) | (1) | 75 | pF |
|  |  | Outputs disabled | (1) |  | (1) | 9 |  |  |

(1) This information was not available at the time of publication.

## PARAMETER MEASUREMENT INFORMATION




VOLTAGE WAVEFORMS PULSE DURATION


VOLTAGE WAVEFORMS PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS


VOLTAGE WAVEFORMS SETUP AND HOLD TIMES


[^0]NOTES: A. $C_{L}$ includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: $\mathrm{PRR} \leq 10 \mathrm{MHz}, \mathrm{Z}_{\mathrm{O}}=50 \Omega$.
D. The outputs are measured one at a time, with one transition per measurement.
E. $t_{P L Z}$ and $t_{P H Z}$ are the same as $t_{\text {dis }}$.
F. tpzL and tpze are the same as ten.
G. $t_{P L H}$ and $t_{P H L}$ are the same as $t_{p d}$.
H. All parameters and waveforms are not applicable to all devices.

Figure 2. Load Circuit and Voltage Waveforms

## PACKAGING INFORMATION

| Orderable Device | Status ${ }^{(1)}$ | Package Type | Package Drawing | Pins | Package Qty | Eco Plan ${ }^{(2)}$ | Lead/Ball Finish | MSL Peak Temp ${ }^{(3)}$ |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| 5962-9762601Q3A | ACTIVE | LCCC | FK | 28 | 1 | TBD | POST-PLATE | N/ A for Pkg Type |
| 5962-9762601QKA | ACTIVE | CFP | W | 24 | 1 | TBD | A42 | N/ A for Pkg Type |
| 5962-9762601QLA | ACTIVE | CDIP | JT | 24 | 1 | TBD | A42 SNPB | N/A for Pkg Type |
| SN74LVC646ADBLE | OBSOLETE | SSOP | DB | 24 |  | TBD | Call TI | Call TI |
| SN74LVC646ADBR | ACTIVE | SSOP | DB | 24 | 2000 | $\begin{gathered} \text { Green (RoHS \& } \\ \text { no } \mathrm{Sb} / \mathrm{Br} \text { ) } \end{gathered}$ | CU NIPDAU | Level-1-260C-UNLIM |
| SN74LVC646ADBRE4 | ACTIVE | SSOP | DB | 24 | 2000 | $\begin{gathered} \hline \text { Green (RoHS \& } \\ \text { no } \mathrm{Sb} / \mathrm{Br} \text { ) } \\ \hline \end{gathered}$ | CU NIPDAU | Level-1-260C-UNLIM |
| SN74LVC646ADBRG4 | ACTIVE | SSOP | DB | 24 | 2000 | Green (RoHS \& no $\mathrm{Sb} / \mathrm{Br}$ ) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74LVC646ADW | ACTIVE | SOIC | DW | 24 | 25 | $\begin{gathered} \hline \text { Green (RoHS \& } \\ \text { no Sb/Br) } \\ \hline \end{gathered}$ | CU NIPDAU | Level-1-260C-UNLIM |
| SN74LVC646ADWE4 | ACTIVE | SOIC | DW | 24 | 25 | $\begin{gathered} \hline \text { Green (RoHS \& } \\ \text { no Sb/Br) } \\ \hline \end{gathered}$ | CU NIPDAU | Level-1-260C-UNLIM |
| SN74LVC646ADWG4 | ACTIVE | SOIC | DW | 24 | 25 | $\begin{gathered} \text { Green (RoHS \& } \\ \text { no } \mathrm{Sb} / \mathrm{Br} \text { ) } \end{gathered}$ | CU NIPDAU | Level-1-260C-UNLIM |
| SN74LVC646ADWR | ACTIVE | SOIC | DW | 24 | 2000 | $\begin{gathered} \text { Green (RoHS \& } \\ \text { no Sb/Br) } \end{gathered}$ | CU NIPDAU | Level-1-260C-UNLIM |
| SN74LVC646ADWRE4 | ACTIVE | SOIC | DW | 24 | 2000 | Green (RoHS \& no $\mathrm{Sb} / \mathrm{Br}$ ) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74LVC646ADWRG4 | ACTIVE | SOIC | DW | 24 | 2000 | $\begin{gathered} \text { Green (RoHS \& } \\ \text { no } \mathrm{Sb} / \mathrm{Br}) \\ \hline \end{gathered}$ | CU NIPDAU | Level-1-260C-UNLIM |
| SN74LVC646ANSR | ACTIVE | SO | NS | 24 | 2000 | $\begin{gathered} \text { Green (RoHS \& } \\ \text { no } \mathrm{Sb} / \mathrm{Br}) \end{gathered}$ | CU NIPDAU | Level-1-260C-UNLIM |
| SN74LVC646ANSRE4 | ACTIVE | So | NS | 24 | 2000 | $\begin{gathered} \hline \text { Green (RoHS \& } \\ \text { no } \mathrm{Sb} / \mathrm{Br}) \\ \hline \end{gathered}$ | CU NIPDAU | Level-1-260C-UNLIM |
| SN74LVC646ANSRG4 | ACTIVE | SO | NS | 24 | 2000 | $\begin{gathered} \text { Green (RoHS \& } \\ \text { no Sb/Br) } \\ \hline \end{gathered}$ | CU NIPDAU | Level-1-260C-UNLIM |
| SN74LVC646APW | ACTIVE | TSSOP | PW | 24 | 60 | $\begin{gathered} \text { Green (RoHS \& } \\ \text { no Sb/Br) } \\ \hline \end{gathered}$ | CU NIPDAU | Level-1-260C-UNLIM |
| SN74LVC646APWE4 | ACTIVE | TSSOP | PW | 24 | 60 | $\begin{gathered} \text { Green (RoHS \& } \\ \text { no Sb/Br) } \end{gathered}$ | CU NIPDAU | Level-1-260C-UNLIM |
| SN74LVC646APWG4 | ACTIVE | TSSOP | PW | 24 | 60 | $\begin{gathered} \text { Green (RoHS \& } \\ \text { no } \mathrm{Sb} / \mathrm{Br} \text { ) } \\ \hline \end{gathered}$ | CU NIPDAU | Level-1-260C-UNLIM |
| SN74LVC646APWLE | OBSOLETE | TSSOP | PW | 24 |  | TBD | Call TI | Call TI |
| SN74LVC646APWR | ACTIVE | TSSOP | PW | 24 | 2000 | $\begin{gathered} \hline \text { Green (RoHS \& } \\ \text { no Sb/Br) } \\ \hline \end{gathered}$ | CU NIPDAU | Level-1-260C-UNLIM |
| SN74LVC646APWRE4 | ACTIVE | TSSOP | PW | 24 | 2000 | $\begin{gathered} \hline \text { Green (RoHS \& } \\ \text { no } \mathrm{Sb} / \mathrm{Br}) \\ \hline \end{gathered}$ | CU NIPDAU | Level-1-260C-UNLIM |
| SN74LVC646APWRG4 | ACTIVE | TSSOP | PW | 24 | 2000 | $\begin{gathered} \hline \text { Green (RoHS \& } \\ \text { no Sb/Br) } \\ \hline \end{gathered}$ | CU NIPDAU | Level-1-260C-UNLIM |
| SN74LVC646APWT | ACTIVE | TSSOP | PW | 24 | 250 | $\begin{gathered} \text { Green (RoHS \& } \\ \text { no } \mathrm{Sb} / \mathrm{Br} \text { ) } \end{gathered}$ | CU NIPDAU | Level-1-260C-UNLIM |
| SN74LVC646APWTE4 | ACTIVE | TSSOP | PW | 24 | 250 | $\begin{gathered} \hline \text { Green (RoHS \& } \\ \text { no } \mathrm{Sb} / \mathrm{Br} \text { ) } \\ \hline \end{gathered}$ | CU NIPDAU | Level-1-260C-UNLIM |
| SN74LVC646APWTG4 | ACTIVE | TSSOP | PW | 24 | 250 | Green (RoHS \& no $\mathrm{Sb} / \mathrm{Br}$ ) | CU NIPDAU | Level-1-260C-UNLIM |
| SNJ54LVC646AFK | ACTIVE | LCCC | FK | 28 | 1 | TBD | POST-PLATE | N/ A for Pkg Type |


| Orderable Device | Status $^{(1)}$ | Package <br> Type | Package <br> Drawing | Pins Package <br> Qty | Eco Plan ${ }^{(2)}$ | Lead/Ball Finish | MSL Peak Temp ${ }^{(3)}$ |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| SNJ54LVC646AJT | ACTIVE | CDIP | JT | 24 | 1 | TBD | A42 SNPB | N/A for Pkg Type |
| SNJ54LVC646AW | ACTIVE | CFP | W | 24 | 1 | TBD | A42 | N / A for Pkg Type |

${ }^{(1)}$ The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.
${ }^{(2)}$ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS \& no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The $\mathrm{Pb}-\mathrm{Free} / \mathrm{Green}$ conversion plan has not been defined.
Pb -Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed $0.1 \%$ by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb -Free products are suitable for use in specified lead-free processes.
Pb -Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb -Free (RoHS compatible) as defined above.
Green ( RoHS \& no $\mathrm{Sb} / \mathrm{Br}$ ): TI defines "Green" to mean Pb -Free (RoHS compatible), and free of Bromine ( Br ) and Antimony ( Sb ) based flame retardants ( Br or Sb do not exceed $0.1 \%$ by weight in homogeneous material)
${ }^{(3)}$ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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## TAPE AND REEL BOX INFORMATION



TAPE DIMENSIONS


| A0 | Dimension designed to accommodate the component width |
| :--- | :--- |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


| Device | Package | Pins | Site | Reel <br> Diameter <br> $(\mathbf{m m})$ | Reel <br> Width <br> $(\mathbf{m m})$ | A0 (mm) | B0 (mm) | K0 (mm) | P1 <br> $(\mathbf{m m})$ | $\mathbf{W}$ <br> $(\mathbf{m m})$ | Pin1 <br> Quadrant |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| SN74LVC646ADBR | DB | 24 | SITE 41 | 330 | 16 | 8.2 | 8.8 | 2.5 | 12 | 16 | Q1 |
| SN74LVC646ADWR | DW | 24 | SITE 60 | 330 | 24 | 10.75 | 15.7 | 2.7 | 12 | 24 | Q1 |
| SN74LVC646ANSR | NS | 24 | SITE 41 | 330 | 24 | 8.2 | 15.4 | 2.5 | 12 | 24 | Q1 |
| SN74LVC646APWR | PW | 24 | SITE 41 | 330 | 16 | 6.95 | 8.3 | 1.6 | 8 | 16 | Q1 |



| Device | Package | Pins | Site | Length (mm) | Width (mm) | Height (mm) |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| SN74LVC646ADBR | DB | 24 | SITE 41 | 346.0 | 346.0 | 33.0 |
| SN74LVC646ADWR | DW | 24 | SITE 60 | 346.0 | 346.0 | 41.0 |
| SN74LVC646ANSR | NS | 24 | SITE 41 | 346.0 | 346.0 | 41.0 |
| SN74LVC646APWR | PW | 24 | SITE 41 | 346.0 | 346.0 | 33.0 |



NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification.
E. Falls within MIL STD 1835 GDIP3-T24, GDIP4-T28, and JEDEC MO-058 AA, MO-058 AB


NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice
C. This package can be hermetically sealed with a ceramic lid using glass frit.
D. Falls within MIL-STD-1835 GDFP2-F24 and JEDEC MO-070AD
E. Index point is provided on cap for terminal identification only.

FK (S-CQCC-N**)


NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a metal lid.
D. The terminals are gold plated.
E. Falls within JEDEC MS-004

DW (R-PDSO-G24)

## PLASTIC SMALL-OUTLINE PACKAGE



NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed $0.006(0,15)$.
D. Falls within JEDEC MS-013 variation AD.

NS (R-PDSO-G**)
14-PINS SHOWN


| DIM PINS ** | 14 | 16 | 20 | 24 |
| :---: | :---: | :---: | :---: | :---: |
| A MAX | 10,50 | 10,50 | 12,90 | 15,30 |
| A MIN | 9,90 | 9,90 | 12,30 | 14,70 |

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.


| DIM PINS ** | $\mathbf{1 4}$ | $\mathbf{1 6}$ | $\mathbf{2 0}$ | $\mathbf{2 4}$ | $\mathbf{2 8}$ | $\mathbf{3 0}$ | $\mathbf{3 8}$ |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| A MAX | 6,50 | 6,50 | 7,50 | 8,50 | 10,50 | 10,50 | 12,90 |
| A MIN | 5,90 | 5,90 | 6,90 | 7,90 | 9,90 | 9,90 | 12,30 |

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
D. Falls within JEDEC MO-150


| PIMS $^{* *}$ | $\mathbf{8}$ | $\mathbf{1 4}$ | $\mathbf{1 6}$ | $\mathbf{2 0}$ | $\mathbf{2 4}$ | $\mathbf{2 8}$ |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| A MAX | 3,10 | 5,10 | 5,10 | 6,60 | 7,90 | 9,80 |
| A MIN | 2,90 | 4,90 | 4,90 | 6,40 | 7,70 | 9,60 |

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0,15 .
D. Falls within JEDEC MO-153


[^0]:    VOLTAGE WAVEFORMS
    ENABLE AND DISABLE TIMES LOW- AND HIGH-LEVEL ENABLING

