

# DATA SHEET

For a complete data sheet, please also download:

- The IC04 LOCMOS HE4000B Logic Family Specifications HEF, HEC
- The IC04 LOCMOS HE4000B Logic Package Outlines/Information HEF, HEC

Datasheet.Company

## **HEF4027B** **flip-flops** Dual JK flip-flop

Product specification  
File under Integrated Circuits, IC04

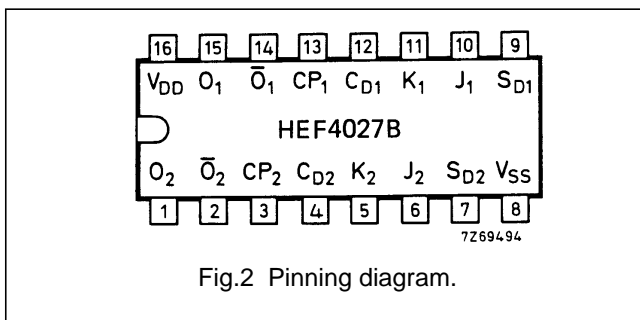
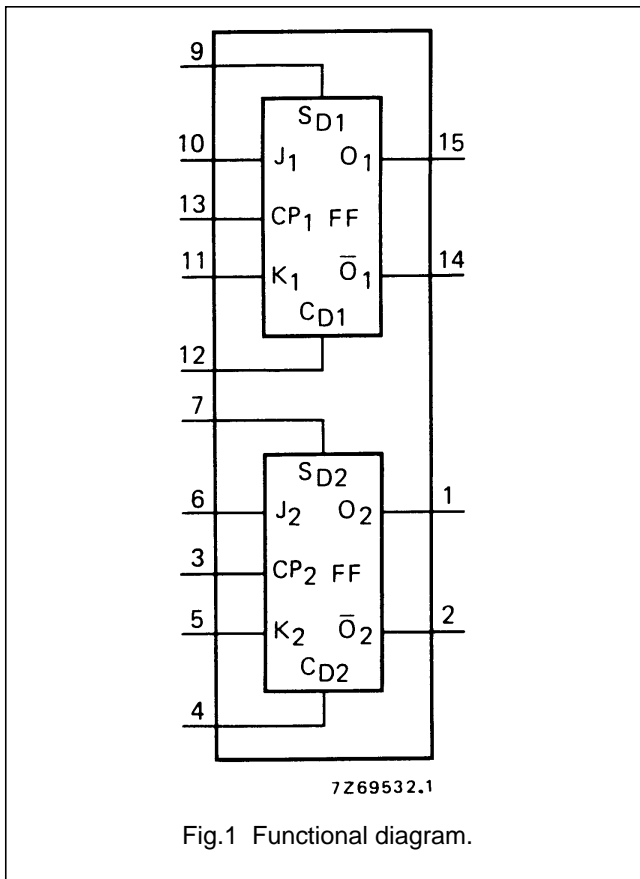
January 1995

# Dual JK flip-flop

# HEF4027B flip-flops

### DESCRIPTION

The HEF4027B is a dual JK flip-flop which is edge-triggered and features independent set direct ( $S_D$ ), clear direct ( $C_D$ ), clock (CP) inputs and outputs ( $O, \bar{O}$ ). Data is accepted when CP is LOW, and transferred to the output on the positive-going edge of the clock. The active HIGH asynchronous clear-direct ( $C_D$ ) and set-direct ( $S_D$ ) are independent and override the J, K, and CP inputs. The outputs are buffered for best system performance. Schmitt-trigger action in the clock input makes the circuit highly tolerant to slower clock rise and fall times.



### FUNCTION TABLES

| INPUTS |       |    |   |   | OUTPUTS |           |
|--------|-------|----|---|---|---------|-----------|
| $S_D$  | $C_D$ | CP | J | K | O       | $\bar{O}$ |
| H      | L     | X  | X | X | H       | L         |
| L      | H     | X  | X | X | L       | H         |
| H      | H     | X  | X | X | H       | H         |

| INPUTS |       |    |   |   | OUTPUTS     |                 |
|--------|-------|----|---|---|-------------|-----------------|
| $S_D$  | $C_D$ | CP | J | K | $O_{n+1}$   | $\bar{O}_{n+1}$ |
| L      | L     | ↗  | L | L | no change   |                 |
| L      | L     | ↗  | H | L | H           | L               |
| L      | L     | ↗  | L | H | L           | H               |
| L      | L     | ↗  | H | H | $\bar{O}_n$ | $O_n$           |

### Notes

- H = HIGH state (the more positive voltage)  
L = LOW state (the less positive voltage)  
X = state is immaterial  
↗ = positive-going transition  
 $O_{n+1}$  = state after clock positive transition

### PINNING

- J,K synchronous inputs
- CP clock input (L to H edge-triggered)
- $S_D$  asynchronous set-direct input (active HIGH)
- $C_D$  asynchronous clear-direct input (active HIGH)
- O true output
- $\bar{O}$  complement output

- HEF4027BP(N): 16-lead DIL; plastic (SOT38-1)
- HEF4027BD(F): 16-lead DIL; ceramic (cerdip) (SOT74)
- HEF4027BT(D): 16-lead SO; plastic (SOT109-1)
- ( ): Package Designator North America

### FAMILY DATA, $I_{DD}$ LIMITS category FLIP-FLOPS

See Family Specifications

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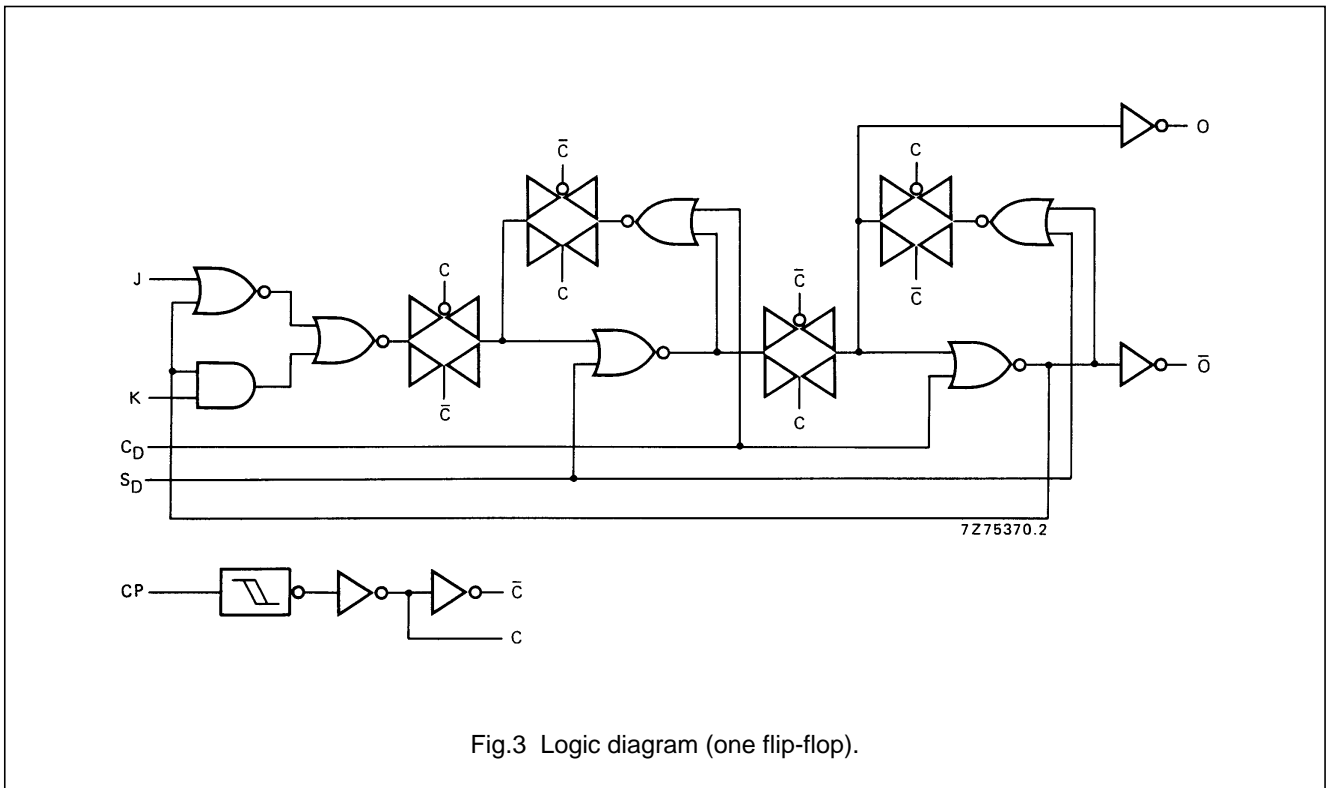


Fig.3 Logic diagram (one flip-flop).

AC CHARACTERISTICS

V<sub>SS</sub> = 0 V; T<sub>amb</sub> = 25 °C; C<sub>L</sub> = 50 pF; input transition times ≤ 20 ns

|                            | V <sub>DD</sub><br>V | SYMBOL           | MIN. | TYP. | MAX.   | TYPICAL EXTRAPOLATION<br>FORMULA     |
|----------------------------|----------------------|------------------|------|------|--------|--------------------------------------|
| Propagation delays         |                      |                  |      |      |        |                                      |
| CP → O, $\bar{O}$          | 5                    |                  |      | 105  | 210 ns | 78 ns + (0,55 ns/pF) C <sub>L</sub>  |
| HIGH to LOW                | 10                   | t <sub>PHL</sub> |      | 40   | 80 ns  | 29 ns + (0,23 ns/pF) C <sub>L</sub>  |
|                            | 15                   |                  |      | 30   | 60 ns  | 22 ns + (0,16 ns/pF) C <sub>L</sub>  |
| LOW to HIGH                | 5                    |                  |      | 85   | 170 ns | 58 ns + (0,55 ns/pF) C <sub>L</sub>  |
|                            | 10                   | t <sub>PLH</sub> |      | 35   | 70 ns  | 27 ns + (0,23 ns/pF) C <sub>L</sub>  |
|                            | 15                   |                  |      | 30   | 60 ns  | 22 ns + (0,16 ns/pF) C <sub>L</sub>  |
| S <sub>D</sub> → O         |                      |                  |      |      |        |                                      |
| LOW to HIGH                | 5                    |                  |      | 70   | 140 ns | 43 ns + (0,55 ns/pF) C <sub>L</sub>  |
|                            | 10                   | t <sub>PLH</sub> |      | 30   | 60 ns  | 19 ns + (0,23 ns/pF) C <sub>L</sub>  |
|                            | 15                   |                  |      | 25   | 50 ns  | 17 ns + (0,16 ns/pF) C <sub>L</sub>  |
| C <sub>D</sub> → O         |                      |                  |      |      |        |                                      |
| HIGH to LOW                | 5                    |                  |      | 120  | 240 ns | 93 ns + (0,55 ns/pF) C <sub>L</sub>  |
|                            | 10                   | t <sub>PHL</sub> |      | 45   | 90 ns  | 33 ns + (0,23 ns/pF) C <sub>L</sub>  |
|                            | 15                   |                  |      | 35   | 70 ns  | 27 ns + (0,16 ns/pF) C <sub>L</sub>  |
| S <sub>D</sub> → $\bar{O}$ |                      |                  |      |      |        |                                      |
| HIGH to LOW                | 5                    |                  |      | 140  | 280 ns | 113 ns + (0,55 ns/pF) C <sub>L</sub> |
|                            | 10                   | t <sub>PHL</sub> |      | 55   | 110 ns | 44 ns + (0,23 ns/pF) C <sub>L</sub>  |
|                            | 15                   |                  |      | 40   | 80 ns  | 32 ns + (0,16 ns/pF) C <sub>L</sub>  |

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|  | V <sub>DD</sub><br>V | SYMBOL                                   | MIN. | TYP. | MAX.   | TYPICAL EXTRAPOLATION<br>FORMULA    |
|--|----------------------|--|------|------|--------|-------------------------------------|
| C <sub>D</sub> → $\bar{O}$<br>LOW to HIGH                    | 5                    | t <sub>PLH</sub>                         |      | 75   | 150 ns | 48 ns + (0,55 ns/pF) C <sub>L</sub> |
|  | 10                   |  |      | 35   | 70 ns  | 24 ns + (0,23 ns/pF) C <sub>L</sub> |
|  | 15                   |  |      | 25   | 50 ns  | 17 ns + (0,16 ns/pF) C <sub>L</sub> |
| Output transition times<br>HIGH to LOW                       | 5                    | t <sub>THL</sub>                         |      | 60   | 120 ns | 10 ns + (1,0 ns/pF) C <sub>L</sub>  |
|  | 10                   |  |      | 30   | 60 ns  | 9 ns + (0,42 ns/pF) C <sub>L</sub>  |
|  | 15                   |  |      | 20   | 40 ns  | 6 ns + (0,28 ns/pF) C <sub>L</sub>  |
| LOW to HIGH  | 5                    | t <sub>TLH</sub>                         |      | 60   | 120 ns | 10 ns + (1,0 ns/pF) C <sub>L</sub>  |
|  | 10                   |  |      | 30   | 60 ns  | 9 ns + (0,42 ns/pF) C <sub>L</sub>  |
|  | 15                   |  |      | 20   | 40 ns  | 6 ns + (0,28 ns/pF) C <sub>L</sub>  |
| Set-up time<br>J,K → CP                                      | 5                    | t <sub>su</sub>                          | 50   | 25   | ns     | see also waveforms<br>Figs 4 and 5  |
|  | 10                   |  | 30   | 10   | ns     |                                     |
|  | 15                   |  | 20   | 5    | ns     |                                     |
| Hold time<br>J,K → CP  | 5                    | t <sub>hold</sub>                        | 25   | 0    | ns     |                                     |
|  | 10                   |  | 20   | 0    | ns     |                                     |
|  | 15                   |  | 15   | 5    | ns     |                                     |
| Minimum clock<br>pulse width; LOW                            | 5                    | t <sub>WCPL</sub>                        | 80   | 40   | ns     |                                     |
|  | 10                   |  | 30   | 15   | ns     |                                     |
|  | 15                   |  | 24   | 12   | ns     |                                     |
| Minimum S <sub>D</sub> , C <sub>D</sub><br>pulse width; HIGH | 5                    | t <sub>WSDH</sub> ,<br>t <sub>WCDH</sub> | 90   | 45   | ns     |                                     |
|  | 10                   |  | 40   | 20   | ns     |                                     |
|  | 15                   |  | 30   | 15   | ns     |                                     |
| Recovery time<br>for S <sub>D</sub> , C <sub>D</sub>         | 5                    | t <sub>RSD</sub> ,<br>t <sub>RCD</sub>   | 20   | -15  | ns     |                                     |
|  | 10                   |  | 15   | -10  | ns     |                                     |
|  | 15                   |  | 10   | -5   | ns     |                                     |
| Maximum clock<br>pulse frequency<br>J = K = HIGH             | 5                    | f <sub>max</sub>                         | 4    | 8    | MHz    | see also waveforms<br>Fig.4         |
|  | 10                   |  | 12   | 25   | MHz    |                                     |
|  | 15                   |  | 15   | 30   | MHz    |                                     |

|   | V <sub>DD</sub><br>V | TYPICAL FORMULA FOR P (μW)  |   |
|---|----------------------|---|---|
| Dynamic power<br>dissipation per<br>package (P) | 5                    | 900 f <sub>i</sub> + ∑ (f <sub>o</sub> C <sub>L</sub> ) × V <sub>DD</sub> <sup>2</sup>    | where<br>f <sub>i</sub> = input freq. (MHz)<br>f <sub>o</sub> = output freq. (MHz)<br>C <sub>L</sub> = load capacitance (pF)<br>∑ (f <sub>o</sub> C <sub>L</sub> ) = sum of outputs<br>V <sub>DD</sub> = supply voltage (V) |
|   | 10                   | 4 500 f <sub>i</sub> + ∑ (f <sub>o</sub> C <sub>L</sub> ) × V <sub>DD</sub> <sup>2</sup>  |   |
|   | 15                   | 13 200 f <sub>i</sub> + ∑ (f <sub>o</sub> C <sub>L</sub> ) × V <sub>DD</sub> <sup>2</sup> |   |

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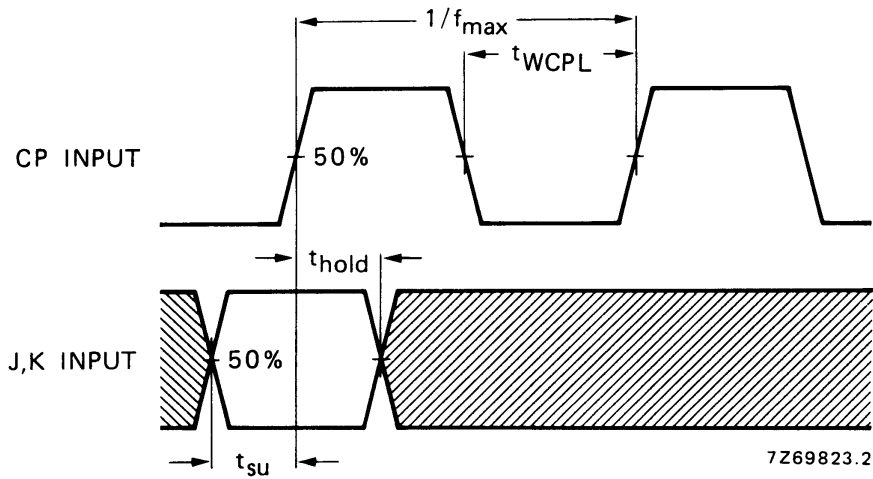


Fig.4 Waveforms showing set-up times, hold times and minimum clock pulse width. Set-up and hold times are shown as positive values but may be specified as negative values.

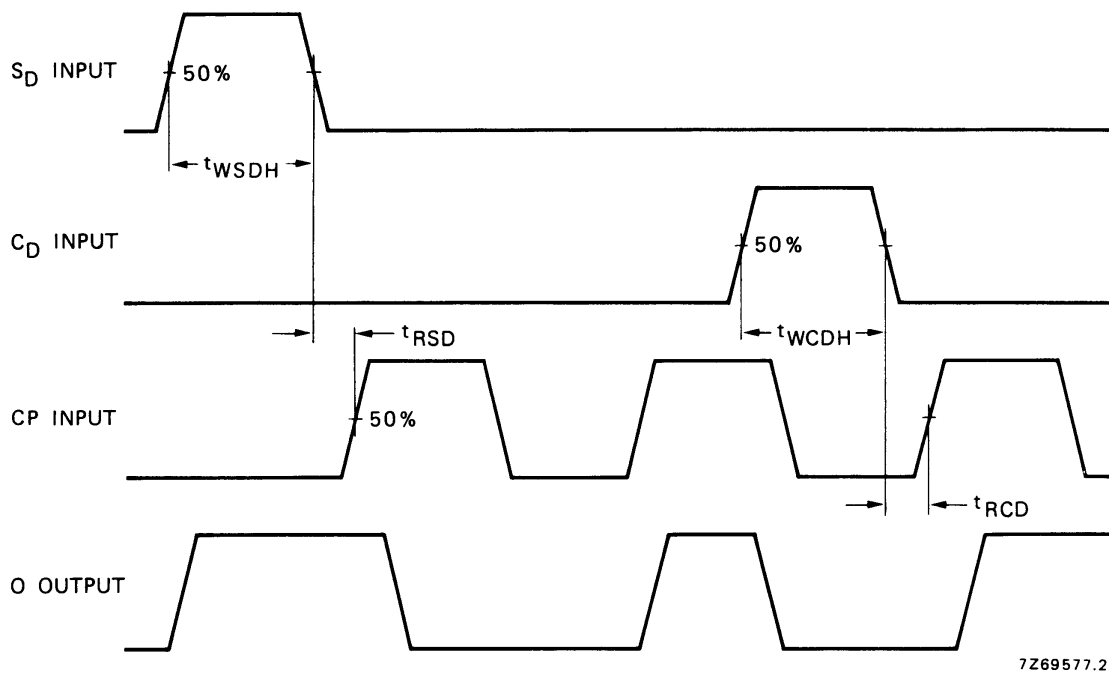


Fig.5 Waveforms showing recovery times for  $S_D$  and  $C_D$ ; minimum  $S_D$  and  $C_D$  pulse widths.

APPLICATION INFORMATION

Some examples of applications for the HEF4027B are:

- Registers
- Counters
- Control circuits