The RF Power MOS Line **Power Field Effect Transistor**N-Channel Enhancement Mode

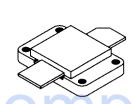
Designed primarily for linear large-signal output stages to 80 MHz.

Specified 50 Volts, 30 MHz Characteristics
 Output Power = 600 Watts
 Power Gain = 21 dB (Typ)
 Efficiency = 45% (Typ)

MRF157

600 W, to 80 MHz MOS LINEAR RF POWER FET





CASE 368-03, STYLE 2

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Drain-Source Voltage	VDSS	125	Vdc
Drain-Gate Voltage	V _{DGO}	125	Vdc
Gate-Source Voltage	VGS	±40	Vdc
Drain Current — Continuous	ID	60	Adc
Total Device Dissipation @ T _C = 25°C Derate above 25°C	PD	1350 7.7	Watts W/ C
Storage Temperature Range	T _{stg}	-65 to +150	, C
Operating Junction Temperature	TJ	200	С

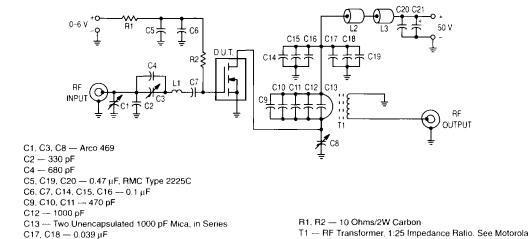
THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	R _B JC	0.13	"C/W

NOTE — <u>CAUTION</u> — MOS devices are susceptible to damage from electrostatic charge. Reasonable precautions in handling and packaging MOS devices should be observed.

ELECTRICAL CHARACTERISTICS (T_C = 25 °C unless otherwise noted)

Characteristic	Symbol	Min	Тур	Max	Unit
OFF CHARACTERISTICS			<u> </u>	<u> </u>	
Drain-Source Breakdown Voltage (V _{GS} = 0, I _D = 100 mA)	V _{(BR)DSS}	125	_	_	Vdc
Zero Gate Voltage Drain Current (VDS = 50 V, VGS = 0)	loss l	_	_	20	mAdc
Gate-Body Leakage Current (V _{GS} = 20 V, V _{DS} = 0)	Igss			5.0	μAdc
ON CHARACTERISTICS					
Gate Threshold Vollage (V _{DS} = 10 V, I _D = 100 mA)	V _{GS(th)}	1.0	3.0	5.0	Vdc
Drain-Source On-Voltage (V _{GS} = 10 V. I _D = 40 A)	V _{DS(on)}	1.0	3.0	5.0	Vdc
Forward Transconductance (V _{DS} = 10 V, I _D = 20 A)	9fs	16	24	_	mhos
DYNAMIC CHARACTERISTICS			•	•	•
Input Capacitance (VDS = 50 V, VGS = 0 V, f = 1.0 MHz)	C _{iss}	-	1800	and the same of th	pF
Output Capacitance (V _{DS} = 50 V, V _{GS} = 0, f = 1.0 MHz)	Coss		750	_	pF
Reverse Transfer Capacitance (V _{DS} = 50 V, V _{GS} = 0, f = 1.0 MHz)	C _{rss}	_	75	_	pF
FUNCTIONAL TESTS			I		1
Common Source Amplifier Power Gain (V _{DD} = 50 V, P _{out} = 600 W, I _{DQ} = 800 mA, f = 30 MHz)	G _{ps}	15	21	_	dB
Drain Efficiency (V _{DD} = 50 V, P _{OUt} = 600 W, t = 30 MHz, t _{DQ} = 800 mA)	h	40	45	_	0.0
Intermodulation Distortion (V _{DD} = 50 V. P _{Out} = 600 W(PEP), 11 = 30 MHz, 12 = 30.001 MHz, 1 _{DQ} = 800 mA)	IMD _(d3)		-25	_	dB



L2, L3 — Ferrite Beads, Fair–Rite Products Corp. #2673000801

All capacitors ATC type 100/200 chips or equivalent unless otherwise noted.

Figure 1. 30 MHz Test Circuit

C21 — 10 µF/100 V Electrolytic L1 — 2 Turns #16 AWG, 1/2" ID, 3/8" Long Application Note AN749, Figure 4 for details.

Ferrite Material: 2 Each, Fair-Rite Products

Corp. #2667540001

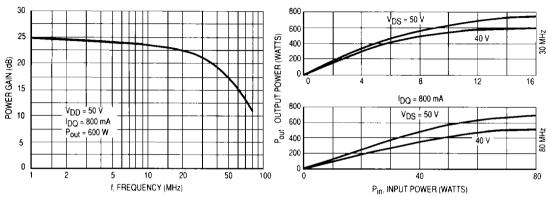


Figure 2. Power Gain versus Frequency

Figure 3. Output Power versus Input Power

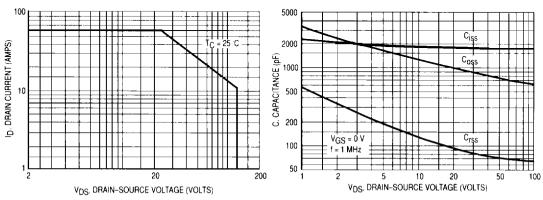


Figure 4. DC Safe Operating Area

Figure 5. Capacitance versus Drain Voltage

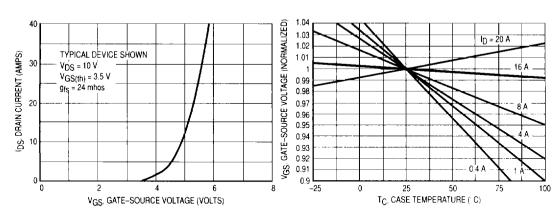


Figure 6. Gate Voltage versus Drain Current

Figure 7. Gate-Source Voltage versus Case Temperature

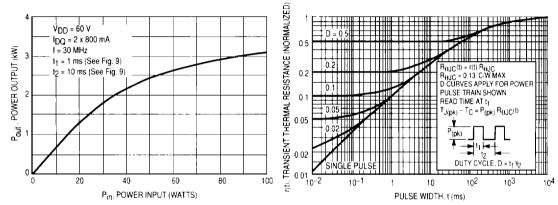


Figure 8. Output Power versus Input Power Under Pulse Conditions (2 x MRF157)

Figure 9. Thermal Response versus
Pulse Width

Note: Pulse data for this graph was taken in a push-pull circuit similar to the one shown. However, the output matching network was modified for the higher level of peak power.

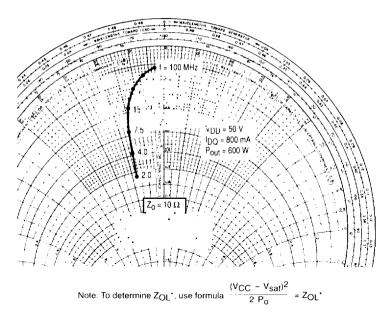
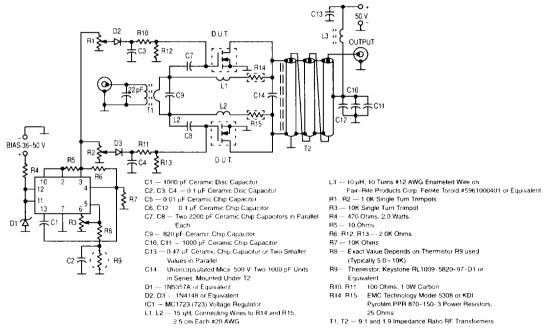


Figure 10. Series Equivalent Impedance



Unless otherwise noted, all resistors are 1/2 watt metal film type. All chip capacitors except C13 are ATC type 100/2009 or Dielectric Laboratories type C17

Figure 11. 2.0 to 50 MHz, 1.0 kW Wideband Amplifier

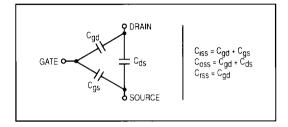
RF POWER MOSFET CONSIDERATIONS

MOSFET CAPACITANCES

The physical structure of a MOSFET results in capacitors between the terminals. The metal oxide gate structure determines the capacitors from gate–to–drain (Cgd), and gate–to–source (Cgs). The PN junction formed during the fabrication of the TMOS^(H) FET results in a junction capacitance from drain–to–source (Cds).

These capacitances are characterized as input ($C_{\rm ISS}$), output ($C_{\rm OSS}$) and reverse transfer ($C_{\rm ISS}$) capacitances on data sheets. The relationships between the interterminal capacitances and those given on data sheets are shown below. The $C_{\rm ISS}$ can be specified in two ways:

- 1. Drain shorted to source and positive voltage at the gate.
- Positive voltage of the drain in respect to source and zero volts at the gate. In the latter case the numbers are lower. However, neither method represents the actual operating conditions in RF applications.



LINEARITY AND GAIN CHARACTERISTICS

In addition to the typical IMD and power gain data presented, Figure 5 may give the designer additional information on the capabilities of this device. The graph represents the small signal unity current gain frequency at a given drain current level. This is equivalent to f \uptau for bipolar transistors. Since this test is performed at a fast sweep speed, heating of the device does not occur. Thus, in normal use, the higher temperatures may degrade these characteristics to some extent

DRAIN CHARACTERISTICS

One figure of merit for a FET is its static resistance in the full—on condition. This on–resistance, $V_{DS(on)}$, occurs in the linear region of the output characteristic and is specified under specific test conditions for gate—source voltage and drain current. For MOSFETs, $V_{DS(on)}$ has a positive temperature coefficient and constitutes an important design consideration at high temperatures, because it contributes to the power dissipation within the device.

GATE CHARACTERISTICS

The gate of the TMOS FET is a polysilicon material, and is electrically isolated from the source by a layer of oxide. The input resistance is very high — on the order of 10⁹ ohms — resulting in a leakage current of a few nanoamperes.

Gate control is achieved by applying a positive voltage slightly in excess of the gate-to-source threshold voltage, VGS(th)-

Gate Voltage Rating — Never exceed the gate voltage rating. Exceeding the rated V_{GS} can result in permanent damage to the oxide layer in the gate region.

Gate Termination — The gates of these devices are essentially capacitors. Circuits that leave the gate open-circuited or floating should be avoided. These conditions can result in turn-on of the devices due to voltage build-up on the input capacitor due to leakage currents or pickup.

Gate Protection — These devices do not have an internal monolithic zener diode from gate—to—source. The addition of an internal zener diode may result in detrimental effects on the reliability of a power MOSFET. If gate protection is required, an external zener diode is recommended.

IMPEDANCE CHARACTERISTICS

Device input and output impedances are normally obtained by measuring their conjugates in an optimized narrow band test circuit. These test circuits are designed and constructed for a number of frequency points depending on the frequency coverage of characterization. For low frequencies the circuits consist of standard LC matching networks including variable capacitors for peak tuning. At increasing power levels the output impedance decreases, resulting in higher RF currents in the matching network. This makes the practicality of output impedance measurements in the manner described questionable at power levels higher than 200-300 W for devices operated at 50 V and 150-200 W for devices operated at 28 V. The physical sizes and values required for the components to withstand the RF currents increase to a point where physical construction of the output matching network gets difficult if not impossible. For this reason the output impedances are not given for high power devices such as the MRF154 and MRF157. However, formulas like $\frac{(VDS - V_{sat})^2}{2}$ for a single ended design $\underline{^2((V_{DS}-V_{sat})^2)}$ for a push–pull design can be used to

obtain reasonably close approximations to actual values.

MOUNTING OF HIGH POWER RF

The package of this device is designed for conduction cooling. It is extremely important to minimize the thermal resistance between the device flange and the heat dissipator.

If a copper heatsink is not used, a copper head spreader is strongly recommended between the device mounting surfaces and the main heatsink. It should be at least 1/4" thick and extend at least one inch from the flange edges. A thin layer of thermal compound in all interfaces is, of course, esential. The recommended torque on the 4-40 mounting screws should be in the area of 4-5 lbs.-inch, and spring type lock washers along with flat washers are recommended.

For die temperature calculations, the Δ temperature from a corner mounting screw area to the bottom center of the flange is approximately 5°C and 10°C under normal operating conditions (dissipation 150 W and 300 W respectively).

The main heat dissipator must be sufficiently large and have low R_{θ} for moderate air velocity, unless liquid cooling is employed.

CIRCUIT CONSIDERATIONS

At high power levels (500 W and up), the circuit layout becomes critical due to the low impedance levels and high RF currents associated with the output matching. Some of the components, such as capacitors and inductors must also withstand these currents. The component losses are directly proportional to the operating frequency. The manufacturers specifications on capacitor ratings should be consulted on these aspects prior to design.

Push-pull circuits are less critical in general, since the ground referenced RF loops are practically eliminated, and the impedance levels are higher for a given power output. High power broadband transformers are also easier to design than comparable LC matching networks.

EQUIVALENT TRANSISTOR PARAMETER TERMINOLOGY

Collector	Drain
Emitter	Source
Base	Gate
V(BR)CES	
V _{CBO}	VDGO
lc	ID
lces	IDSS
^I EBO	IGSS
V _{BE(on)}	VGS(th)
VCE(sat) · · · · · · · · · · · · · · · · · · ·	VDS(on)
C _{ib}	Ciss
C _{ob}	Coss
h _{fe}	9fs
$RCE(sat) = \frac{VCE(sat)}{IC} \cdots$	$R_{DS(on)} = \frac{V_{DS(on)}}{I_{D}}$